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Designing of Low Power RF-Receiver Front-end with CMOS Technology

School of Electrical Engineering

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ABSTRACT OF THE
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This thesis studies how to design ultra low power radio-receiver front-end circuit consisting of a low-noise CMOS amplifier and mixer for low power Bluetooth applications. This system is designed in 65-nm CMOS technology with voltage source of 1.2 V, and it operates at 2.4 GHz. This research project includes the design of radio frequency integrated circuit with CMOS technology using CAD software for circuit design, layout design, pre and post-layout simulations. Firstly, brief study about both Low noise amplifier (LNA) and mixer has been done, and then the design structure such as, input matching network of LNA, noise of system, gain and linearity have been discussed. Later, next section reports simulation results of LNA, mixer and eventually their combination. Furthermore, the effect of packaging and non-ideal on-chip circuit performance has been considered and shown in comparison tables for more clarity. Finally, after the layout design, the obtained results of both post-layout and pre-layout simulations are compared and shown the stability of the design with parasitics consideration.

Keywords: Ultra low power front-end receiver, Low noise CMOS amplifier, Gilbert mixer, Bluetooth, Radio frequency receiver

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Sareh Salari Shahrbabaki

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Contents

Abbreviations and Acronyms

AC	Alternating Current
CS	Common Source
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FET	Field Effect Transistor
GHz	Giga Hertz
IC	Integrated Circuit
IF	Intermediate Frequency
IIP2	Input Reffered Second-Order Intercept Point
IIP3	Input Reffered Third-Order Intercept Point
IP2	Input Reffered Second-Order Intercept Point
IP3	Input Reffered Third-Order Intercept Point
LC	Inductor-Capacitor
LO	Local Oscillator
LNA	Low Noise Amplifier
MHz	Mega Hertz
mm	Millimetre
NF	Noise Figure
RF	Radio Frequency

Symbols

A	Gain
A_{v}	Voltage gain
$\mathrm{BW}_{-3\mathrm{dB}}$	-3dB bandwidth
C_L	Load capacitance
C_c	Coupling capacity
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
C_{bs}	Bulk-source capacitance
C_{in}	Input capacitance
C_{par}	Parasitic capacitance
F	Noise factor
f	Frequency
f_{LO}	Frequency local oscillator
f_{RF}	Frequency radio frequency
$f_{\mathrm{S_{11}=-10dB}}$	Frequency where S_{11} equals -10 dB
γ	Process-dependent noise factor
g_m	Transconductance
$g_{m,\mathrm{RF}}$	Transconductance RF stage
I_{bias}	Bias current
I_{D}	Drain current
L	Channel length
L	Inductor
L_{d}	Drain Inductor
L_{S}	Source Inductor
L_{g}	Gate Inductor
M_n	MOS transistor, n=1,2,3,...
$\mathrm{N}_{\mathrm{dsb}}$	double-sideband noise factor
NF	Noise figure
P_{dc}	Dc power
Q	Quality factor
R	Resistor
R_{in}	Equivalent Resistor
R_{S}	Source Resistor
R_{B}	Bias Resistor
R_{L}	Load Resistor
S_{11}	Input matching coefficient or reflection coefficient
V_{DD}	Supply voltage
V_{DS}	Drain-source voltage
V_{in}	input voltage
V_{RF}	RF voltage
V_{IF}	IF voltage
V_{th}	threshold voltage
W	Channel width

Z	Impedance
Z_{in}	Input Impedance
α	Noise parameter
ω	Angular frequency
ω_0	Center angular frequency
$\varkappa$	Ratio of the transistor substrate transconductance

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1 Introduction

Low power, low-voltage and highly integrated circuits are always the most important subjects for integrated circuit design. Especially, in sensor design due to the crucial need for minimal size and low power circuits. These properties result in remarkable development in sensors' applications such as personal health care, home automation and short distance devices (Bluetooth applications). Therefore, sensor industries require minimized transceiver power consumption.

Since the wireless communication system is very lossy, the received signal from the antenna has very weak strength. Therefore, low noise amplifier (LNA) has to be used after and close to the antenna to amplify the signal for appropriate operation. Furthermore, in order to translate the amplified signal to the desire lower center frequency to permit channel-selection filtering, usage of another block in receiver topology is necessary which is a mixer. In fact, the mixer multiplies the signal to another signal that generated by a local oscillator (LO) and since the multiplication in the time domain corresponding to the convolution in the frequency domain, thus the frequency shift is performed by $\pm\omega_{\mathrm{LO}}$. Finally, by filtering we would have amplified signal at the desired frequency. Figure 1 shows the schematic front-end receiver.

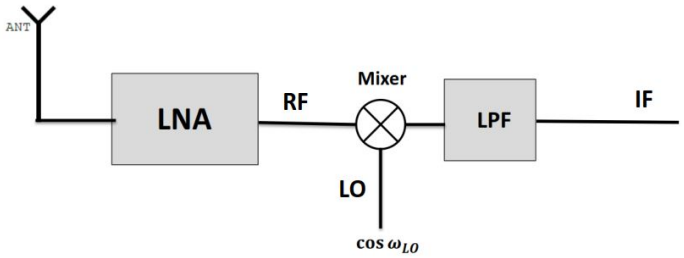


Figure 1: Front-end receiver.

A front-end receiver should operate at a low supply voltage with a small battery or environment energy. In the last few years, plenty of low power receiver implementations have been reported [1–4]. However, their power dissipation is still too high. Therefore, in this work, we tried to minimize the power dissipation as much as possible. This work is a part of low-power transceiver design for short distance devices. It presents the design of a low power LNA+ mixer which are the main parts of the front-end receiver. This receiver is designed for Bluetooth applications, thus the performance frequency is at 2.4 GHz. The conventional architecture of receiver generally integrated discrete and coupled together with inter-stage matching network, balun or filters. These intermediate stages lead to additional power consumption and unwanted parasitics due to the complexity of the system. This work reports ultra-low power fully differential LNA connected to an active down-conversion mixer. Active mixers have a capacitive input impedance, therefore the

only issue is to re-evaluate the LC load of LNA. The integrated architecture is designed, simulated and verified in a 65-nm CMOS technology.

The thesis is organized as follows. Section 2 and 3 introduce LNA and mixer respectively and describe the most common LNA and mixer topologies. Section 4 explains the design procedure and important factors which should be considered during the design. Moreover, section 4 shows the simulation results and performance comparison with other existing systems. Section 5 demonstrates the layout design of the integrated system, followed by post-layout simulation results in contrast with pre-layout simulation. At the end, this thesis is concluded and briefly discussed future work in section 6.

2 Low Noise Amplifier (LNA)

Low Noise Amplifier (LNA) which is usually the first amplifying stage of RF receiver is the most challenging part. Based on Friis' equation the LNA sets the minimum noise figure of the receiver [5]. The Friis' equation is used to calculate the total noise figure of a successive system, each stage with its noise figure and gain. The total noise figure is expressed as Equation 1:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_n}, \tag{1}$$

where the F_i and G_i are the noise figure and gain of the i_{th} stage respectively. As a result of this equation, the total noise of a receiver is generated dominated by the first stage of the system which is the LNA. The noise of subsequent stages degrade by LNA gain as Equation 2 shows.

$$F_{\text{receiver}} = F_{\text{LNA}} + \frac{F_{\text{rest}} - 1}{G_{\text{LNA}}}, \tag{2}$$

in which F_{rest} is the noise of next stages. Thus, the LNA should provide enough gain in order to overcome the noise of the next stages, while it may threaten the sensitivity of receiver.

In addition to the noise figure and gain, enough broad bandwidth is an important issue. To cover the whole reception band with some design margin, but narrow enough to filter unwanted interferers. In order to fulfill the filtering role of LNA a good input impedance matching with source input is also required.

Moreover, linearity performance of total front-end or receiver typically is dependent on the linearity of this stage (LNA). Linearity like bandwidth should be sufficient to tolerate large blockers and not to produce undesired inter-modulation tones in the considered band.

Therefore, to design a proper LNA there are several conditions to be satisfied. Whereas, fulfillment of all requirements together because of simultaneous parameter

optimization is difficult, thus designers have to find compromise according to their own desires. A large number of various LNA topologies is presented in Ref. [6]. Here, we just present and compare the most useful structures the common gate and common source LNAs.

2.1 Common gate

The common gate (CG) LNA is shown in Figure 2.1 and some details related to the CG LNA performance are discussed here in this section. The CG LNA is well-known for being robust and also having a wide frequency range which makes it suitable topology for ultra wide band applications. This topology provides resistive input without the need of using an inductor. The input impedance of CG amplifier is equal to $R_{\text{in}} = \frac{1}{G_m}$, where G_m is the transistor transconductance of the transistor, if the channel length modulation and body effect are neglected.

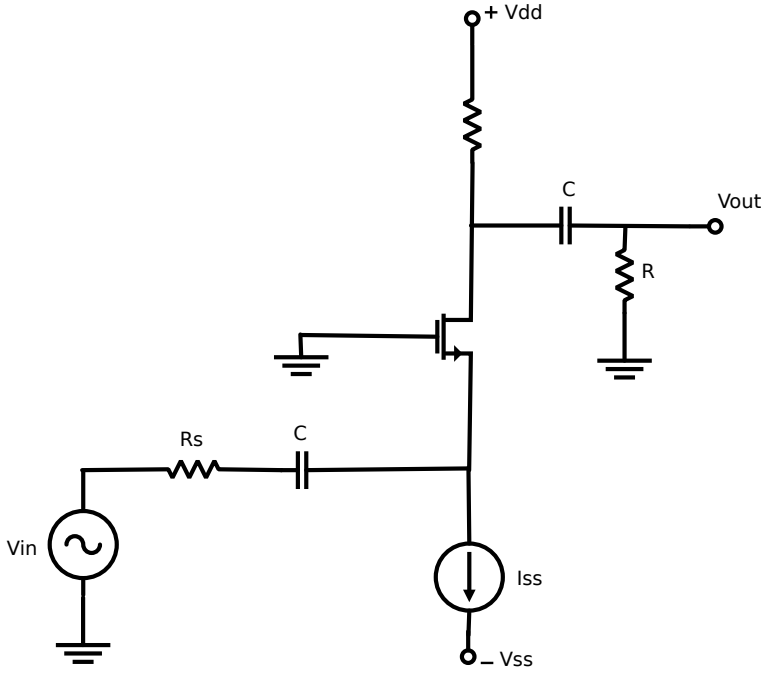


Figure 2: Common-gate LNA.

The input impedance of low noise amplifier should be matched with source resistance R_{S} that is in the majority of cases 50 Ω. Impedance matching has to be done for transferring the maximum power from input to the amplifier. Therefore, dimensions of the amplifier and bias current should be chosen so as $G_m = \frac{1}{R_{\text{S}}}$ or G_m=20 ms, which results in high power consumption or large $\frac{W}{L}$ ratio. Thus, we have some limitations in order to choose the design parameters. The CG stage does not suffer from the Miller effect and hence a sufficient reverse isolation can be achieved with a single transistor stage. Therefore, the input matching network and load can be designed separately. For instance in Refs. [7–10] shunt feedback resistor

used to adjust input impedance. In other words, shunt resistance improves the input matching, while the size of the transistor or its power consumption is not large.

One of the main limitations of CG amplifier is the noise performance. The minimum noise figure is given by,

$$F_{\min,\mathrm{CG}} = 1 + \frac{\gamma}{\alpha}\frac{1}{(\varkappa+1)^2}\cdot\frac{1}{g_m R_\mathrm{S}} = 1 + \frac{\gamma}{\alpha}. \tag{3}$$

According to Equation 3, where γ is the channel thermal noise coefficient and it is 2/3 for long channel devices and considerably larger for short channel devices. $\varkappa$ is the ratio of the transistor substrate transconductance g_{mb} and g_m, R_S is the source resistance and α for the long channel devices is equal to $\frac{g_m}{g_{\mathrm{ds0}}}$. According to Equation 3, the noise performance of the common-gate stage is independent of the operation frequency. Thus, CG can be a good option for high frequencies [11]. α is ideally one and it is smaller for short channel devices. Theoretically, achievable noise figure (NF) is around 3 dB or larger [12]. Therefore, the NF limits the usage of common-gate LNA. However, according to Ref. [13], NF can be lowered by imperfect input matching as

$$F_{min,CG} = 1 + \gamma\frac{1+S_{11}}{1-S_{11}}, \tag{4}$$

where α is neglected and S_{11} is the return loss coefficient (reflection coefficient). In addition, if the load of LNA is resistive we have to take into account contribution of its noise in the noise figure as given by Equation 5

$$F = 1 + (\frac{\gamma}{\alpha} + \frac{(1+g_m R_\mathrm{S})^2}{g_m R_\mathrm{L}})\cdot\frac{1}{g_m R_\mathrm{S}} = 1 + \frac{\gamma}{\alpha} + \frac{4R_\mathrm{S}}{R_\mathrm{L}}. \tag{5}$$

Therefore, as it is explained explicitly in Ref. [11] the resistive load has significant role in overall NF.

There is a possibility to improve the noise performance by using differential CG LNA. In this method, gates are driven by the opposite polarity input which halves the required g_m and reduces the minimum noise as expressed in Equation 6 [14]

$$F_{\min,\mathrm{CG}} = 1 + \frac{\gamma}{2\alpha}. \tag{6}$$

2.2 Inductively degenerated common-source LNA

The inductively degenerated common-source (IDCS) amplifier depicted in Figure 3(a) is one of the most popular CMOS LNA topologies. In Refs. [15–19] this type of LNA has been used and has been explained with details. This topology has very

good NF and it provides both current and voltage gain which results in reducing the noise of next stages [16]. According to the equivalent circuit of this amplifier which has been shown in Figure 3(b), the transistor M_1 is simply replaced with the small signal model having only gate-source capacitance $C_{\rm gs}$ and transconductance g_m. In order to improve and optimize noise performance of this structure another capacitor ($C_{\rm d}$) can be connected parallelly with the $C_{\rm gs}$ of the input device, as indicated in Ref. [20, 21].

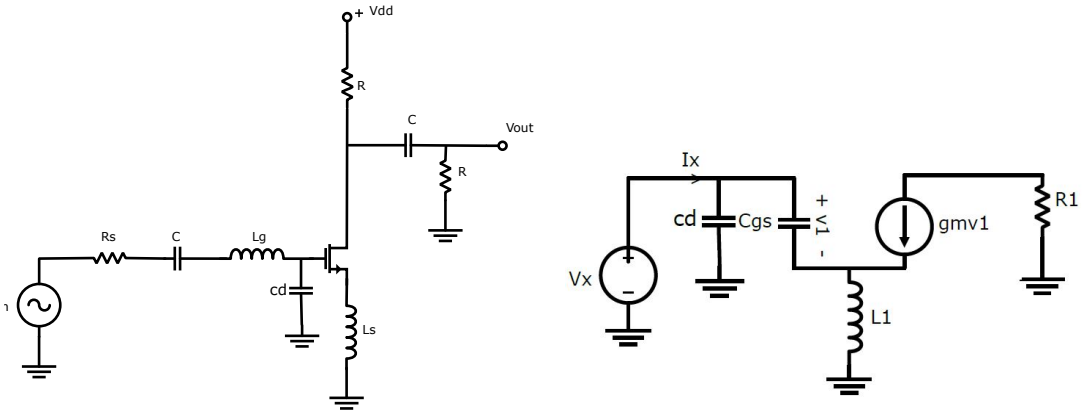


Figure 3: (a) Inductive degenerated common-source LNA–(b) equivalent circuit neglecting $C_{\rm gd}$ and $C_{\rm sb}$.

2.2.1 Input impedance

Input impedance of IDCS low noise amplifier can be expressed as below [22]

$$Z_{\rm in} = j\omega L_{\rm g} + j\omega L_{\rm s} - \frac{j}{\omega C_{\rm gs}} + \frac{g_m L_{\rm s}}{C_{\rm gs}}. \tag{7}$$

The resistive term of Equation 7 is directly proportional to the source inductor value. Therefore, this amplifier can provide the specified input impedance without using a physical resistor which causes noise to the amplifier. Reactance is almost noiseless, thus it does not generate thermal noise. However, the series resistance of inductors $L_{\rm g}$ and $L_{\rm s}$ would have a slight effect on NF. For having 50 Ω input impedance, the real part ($\frac{g_m L_{\rm s}}{C_{\rm gs}}$) should be equal to 50 Ω and imaginary part should be zero at the frequency of interest, thus it results in

$$\begin{aligned} R_s &= \frac{g_m L_{\rm s}}{C_{\rm GS}}, \\ {\omega_0}^2 &= \frac{1}{(L_{\rm s} + L_{\rm g}) C_{\rm GS}}, \end{aligned} \tag{8}$$

where C_{GS} is the sum of C_{gs} and C_d. If the size of the transistor is small, using C_d is a useful way to realize input matching network. In other words, L_{s}, L_{g} and $C_d + C_{\mathrm{gs}}$ can be adjusted simultaneously to obtain the best matching performance. Typically, L_{g} is realized as wire-bond inductance with high quality factor (Q) and L_{s} has low value with smaller Q which is implemented as an on-chip spiral inductor. The effect of the series resistance of L_{s} can be lowered by using bond-wire [23, 24].

2.2.2 Gain

Voltage gain is defined as a ratio of output and input voltages as follows

$$A_{\mathrm{v}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}, \tag{9}$$

The output voltage at the load impedance (Z_{L}) is $V_{\mathrm{out}} = I_{\mathrm{out}} Z_{\mathrm{L}}$, where I_{out} is the output current of the input stage, thus the voltage gain can be written as

$$A_{\mathrm{v}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{I_{\mathrm{out}} Z_{\mathrm{L}}}{V_{\mathrm{in}}} = g_{m,\mathrm{eff}} Z_{\mathrm{L}}, \tag{10}$$

where the $g_{m,\mathrm{eff}}$ is the effective transconductance of the input stage. The $g_{m,\mathrm{eff}}$ of common source LNA is evaluated as

$$g_{m,\mathrm{eff}} = \frac{I_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{g_m V_{\mathrm{gs}}}{V_{\mathrm{in}}} = \frac{g_m I_{\mathrm{in}}}{s C_{\mathrm{gs}} V_{\mathrm{in}}} = \frac{g_m}{s C_{\mathrm{gs}} Z_{\mathrm{in}}}, \tag{11}$$

in which g_m is the transconductance of transistor and C_{gs}, is the gate-source capacitance of the transistor. Moreover, Z_{in} is the input impedance that is presented in Equation 7.

Therefore, according to the calculation in Ref. [13], at resonance frequency the $g_{m,\mathrm{eff}}$ is independent of g_m of the input stage transistor, although g_m has effect on the resistive part of the input impedance as given in Equation 8. Additionally, $g_{m,\mathrm{eff}}$ can be written as

$$g_{m,\mathrm{eff}} = \frac{I_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{g_m V_{\mathrm{gs}}}{V_{\mathrm{in}}} = g_m Q_{\mathrm{in}}, \tag{12}$$

where Q_{in} is the voltage gain between the input of the matching network and the gate-source voltage of the input transistor. By increasing this gain we can decrease the g_m value which leads to a smaller input transistor and then a smaller C_{gs}. In this situation, the matching network becomes sensitive to the parasitic capacitances at the input matching circuits. Therefore, the use of inductor at the source of CS is practically effectless, when the input transistor is very small.

2.2.3 Linearity

Linearity is an important factor which shows the stable performance of the circuit. The most commonly used receiver linearity test is 1-dB compression point and third-order intercept point (IP3). These concepts are clearly explained in Refs. [13, 22, 25].

Inductive degeneration common source amplifier has linear performance. Inductive degeneration induces negative feedback at input transistor's source node. Since negative feedback reduces the distortion, thus causes more linear performance. This amplifier provides even more linear performance than the resistive degeneration with the same bias current.

2.2.4 Cascode stage

Common source amplifiers often have a cascode stage as shown in Figure 2.2.4. We can utilize the advantages of this stage in our design. For instance, a cascode transistor has a smaller input impedance than the load impedance. Thus, the Miller effect of the input stage is reduced, which improves the LNA stability.

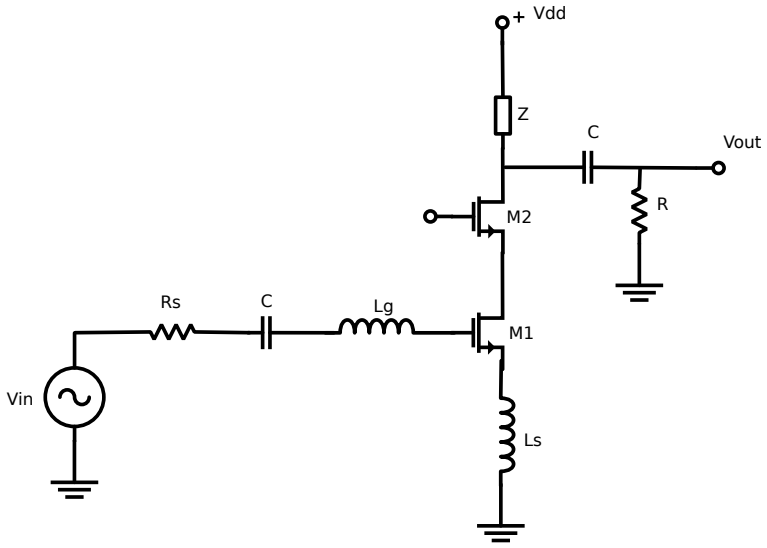


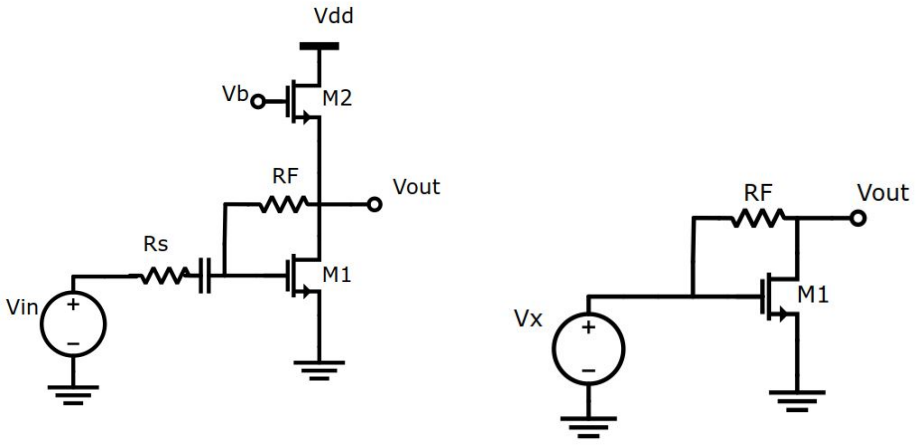
Figure 4: Inductively degenerated common source LNA with cascode stage.

The noise contribution of a cascode stage to the overall noise of the LNA is small but it is not negligible. At high frequencies, the impedance looking into the drain of M_1 is low [16]. The noise contribution of this stage would even decrease by minimizing the parasitic capacitances between input and cascode transistors. Several methods for minimizing the parasitic effects have been presented in Refs. [26–29].

For the load of cascode we use the LC resonator tuned at the carrier frequency f_0. Therefore, at resonance the tank impedance is large which results in a narrowband and large gain. The loss is minimized by having a large inductor value with a high Q-value and a small capacitor. The supply voltage reduction has the price of larger layout due to the extra inductor. The inductor and capacitor values of the resonator are determined by considering the values of parasitic capacitors of the transistor M_2 and carrier frequency similar to the method as shown in Equation 8.

2.2.5 Common source with resistive feedback

The source inductor in a common source LNA limits the achievable bandwidth. If we remove the source inductor, we would need another input matching network. Using the resistive input termination due to increasing noise is not a good option. However, the LNA matching network can be realized by using resistive feedback as shown in Figure 5(a). M_2 acts as a current source and R_F senses the output voltage and returns current to the input.



(a) (b)

Figure 5: (a) Common-source with resistive feedback LNA–(b) simplified circuit [22].

Since R_F is in series with the current source (M_2) and M_1 is seen as diode connected device, thus the $g_{m1} = \frac{1}{R_{in}}$. If the input resistance is considered equal to the R_s, then $g_{m1} = \frac{1}{R_s}$. The gain of this topology according to Figure 5(b) is evaluated as

$$A_v = 1 - \frac{R_F}{R_s}. \tag{13}$$

Practically, the R_F is much larger than R_s, therefore the voltage gain is approximately

$$A_v \approx -\frac{R_F}{R_s}. \tag{14}$$

This circuit is independent of supply voltage effect because the R_F does not carry bias current, while this LNA has relatively large NF based on the Equation is given by 15

$$NF \approx 1 + (\frac{4R_s}{R_F} + \gamma + \gamma g_{m2} R_s). \tag{15}$$

For $\gamma \approx 1$, the NF is larger than 3 dB even if the second term is less than 1 [22]. Therefore, this topology is not a good choice in order to minimize the noise figure.

3 Mixer

Mixer is another important part of almost all receivers and transmitters. The main role of a mixer is frequency translation by multiplication of two waveforms and possibly their harmonics. In the receiver, the down-conversion mixer senses the RF signal at its "RF port" and the local oscillator waveform at its "LO port" and the output that is called "IF" is at "IF port". Typically, the down-conversion receiver mixer moves RF signal to much lower frequency by multiplication to the LO signal, thus, IF signal which is in lower frequency can be more easily amplified. A mixer can simply be realized as Figure 6(a), where V_{LO} works as a switch on and off. Mixers can be accomplished with any non-linear devices (diodes, transistors) or time-varying elements (switches), while due to the high performance of a transistor as a switch, it is the most applicable method. Abrupt switching is a significant factor to be considered, if switching becomes slower mixer suffers from lower gain and higher noise.

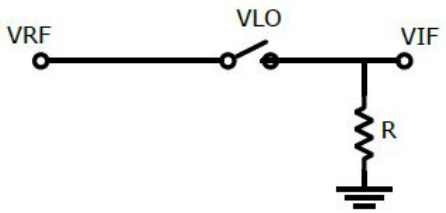


Figure 6: Simple mixer model.

Generally, mixers are classified into passive and active topology, each can be formed as a single-balanced or a double-balanced circuit. When the transistor in mixer does not amplify, a mixer is known as passive as Figure 7 shows. Typically, active mixers can produce gain, while passive mixers are lossy but more linear. An active mixer can be realized so as to obtain conversion gain in one stage. However, the main drawback of an active mixer is generating noise, especially $1/f$ noise for direct conversion receiver since the output signals are at baseband. The mixer noise is mainly created in switching process by switching transistors.

A passive mixer does not consume any power. In addition, there is a claim that since there is no DC current flowing through the mixer, passive mixers are free of $1/f$ noise. However, according to Refs. [30–32] passive mixer has flicker noise and the authors showed that the magnitude of it, is proportional to the input signal amplitude and inversely proportional to the slope of the gate voltage waveforms at LO transitions. Therefore, choosing the type of mixer depends on the system requirements and application.

A mixer can be implemented with a single device, while single balanced mixers suffer from lack of isolation between RF and LO signal which can be minimized by

replacing the differential output instead of single to convey IF signal close to the DC. There is still some leakage from the LO or RF to IF port which is not important in direct conversion receiver, because of high frequency differences that can be simply filtered.

Doubled-balanced mixers are more complicated, they need differential RF input which needs an LNA with differential output. This requires more power for having low noise, or using a balun at the output node of the single-ended LNA in order to convert a single-ended output to a differential one.

However, balun has a complex structure and practically it is not easy to realize because if it is made of transformer it would increase the size of on-chip devices and also parasitics [33]. Moreover, there is another way to convert a single-ended output to a differential one, which is using CG transistor in order to shift the output of LNA 180 degree as shown in Ref. [34], while this method causes frequency phase shift, thus due to the sensitivity of mixer to the frequency it is not a proper topology. Therefore, using a differential LNA with an off-chip balun for the input of LNA in order to have a balanced signal from the antenna is the preferable architecture.

In this thesis, the main focus is the most common active mixer topology, the Gilbert cell mixer, therefore at the first glance, a short overview of other types of the mixer is given.

3.1 Down-conversion mixers

To design a down-conversion mixer there are several concerns that should be considered such as gain, noise and linearity. Designing a mixer is demanding due to the non-linearity and noise requirement. In the direct conversion receiver, dc offsets and $1/f$ noise of the mixer are the biggest problems. Since the most important data is located close to dc. Down-conversion mixers must provide sufficient gain to adequately suppress the noise contributed by subsequent stages. Additionally, because the output of LNA goes to the input of the mixer, thus mixer linearity should be higher than the LNA linearity by the gain of the LNA.

In a receiver chain, the input noise of the mixer following the LNA is divided by the LNA gain when referred to the receiver input while the IP3 of the mixer is reduced by the gain of the LNA [22]. As a result, there will always be a compromise between the noise figure and IP3. Generally, in designing of the mixer the aim is to maximize the linearity, while not raising its NF. Mixer is usually a dominant source for the second-order nonlinearity especially for down-conversion or low IF as explained in Ref. [35].

Moreover, there is another important issue that we should consider, which is the port to port feedthrough. Mixers suffer from coupling (feedthrough) from one port to another. For instance, in direct conversion RF-LO and RF-IF feedthroughs are problematic, thus to avoid these effects, a buffer is typically placed between the LO and the mixer. Furthermore, when ω_{LO} and ω_{IF} are too close to each other LO-IF feedthrough can be a big problem, while when they have enough difference to be separated by filtering, thus in this case LO-IF feedthrough is not an important problem. This issue is strongly dependent on the mixer architecture. For example, if

the mixer is made of a MOSFET, then the gate-source and gate-drain capacitances create feedthrough from the LO port to the RF and IF ports.

3.1.1 Single-balanced and double-balanced mixers

Single-balanced mixers suffer from significant LO-IF feedthrough. Figure 7 illustrates single-balanced mixer. The coupling V_{RF} to V_{Out1} by αV_{LO} and $-\alpha V_{\mathrm{LO}}$ to V_{Out2}, then $V_{\mathrm{Out1}} - V_{\mathrm{Out2}} = 2\alpha V_{\mathrm{LO}}$ to eliminate this effect, we connect two single-balanced mixers such that their output LO feedthrough cancel but the input signals do not. This topology builds double-balanced mixer. This topology as shown in Figure 8 operates with both balanced LO waveform and balanced RF inputs. Single-ended RF is possible with grounding one port at the price of higher input noise. In

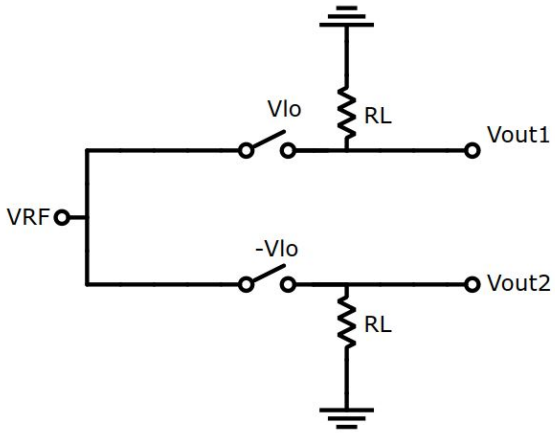


Figure 7: Single-balanced passive mixer.

comparison of these two mixers in terms of conversion gain, Ref. [22] shows that the conversion gain of a double-balanced mixer is half of the single-balanced counterpart. Moreover, the input noise of single-balanced is lower than in a double-balanced.

3.2 Passive mixers

A typical passive mixer is built of four NMOS transistors as analog switches as shown in Figure 8. These transistors act as switch and their work is to be on or off. There is no need for a bias current, thus this structure is low power and has low noise. The DC bias voltage of the gate of switch transistors has an important role in mixer performance. Gate voltage should be chosen somehow close to the threshold of conduction in order to obtain the lowest on-resistance. Therefore, noise from the switches is minimized and good linearity is achieved. Furthermore, if the voltage swing across the switch transistors is kept as small as possible, linearity performance would be maximized. For instance, in Ref. [36] this type of a passive mixer is discussed.

A passive mixer has non-unilateral nature, i.e. the signal flows bidirectionally from input to output, thus causing several problems. For example, while the passive mixer is connected to the output of the LNA, the circuit after the mixer can load the LNA and degrade its gain and selectivity [32]. Furthermore, the passive mixer needs large LO amplitude in order to minimize the overlap period when all switches are on [37]. As a result, the output impedance of the mixers is lowered, which increases the noise of first baseband stage. Additionally, the parasitic capacitances at the switch source and drain nodes lower the mixer's output impedance. With larger switches, there will be larger source-drain junction capacitances, which results in larger stored noise. These capacitances cause an equivalent resistor, which is inversely proportional to the LO frequency and the value of parasitic capacitances [30].

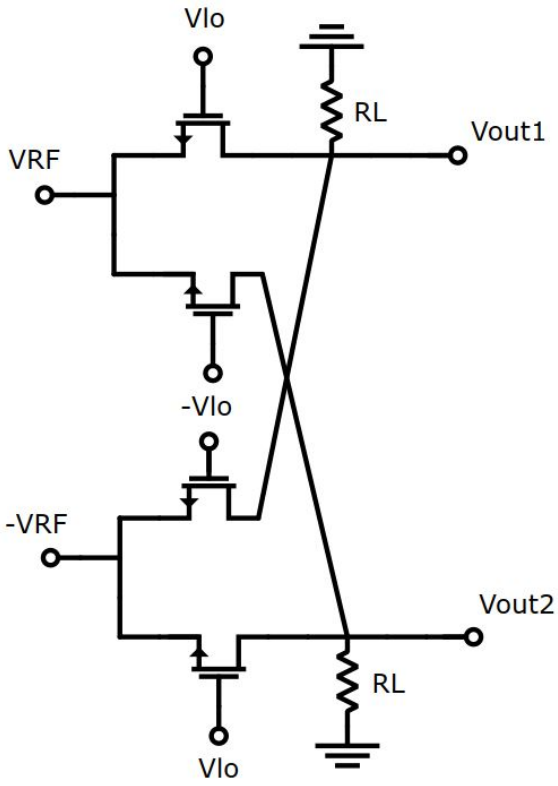


Figure 8: Double-balanced passive mixer.

3.3 Active down-conversion mixers

Active mixers can provide gain and they can convert RF voltage to the current, and then multiply RF current by the LO, and convert IF current to voltage. Figures 9 and 10 illustrate single-balanced and double-balanced mixers respectively.

The most common mixer is probably the Gilbert-cell mixer and its variants. This type of mixer was proposed by Barrie Gilbert as a four-quadrant multiplier in

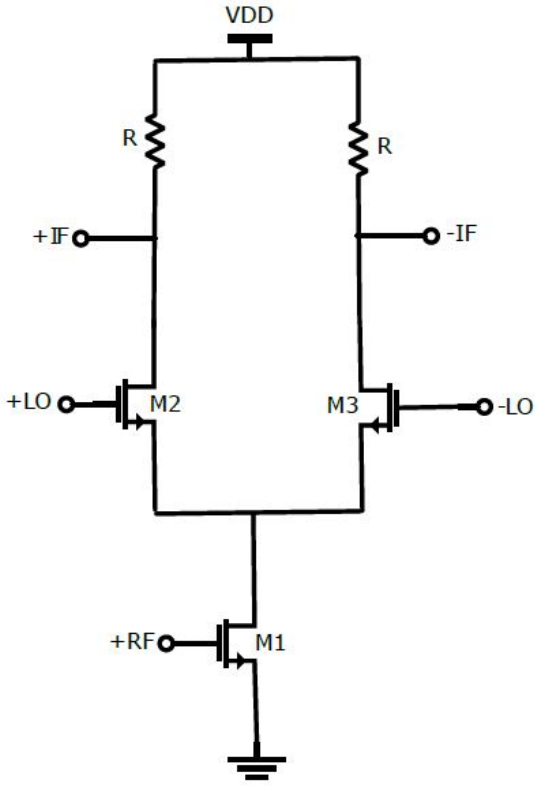


Figure 9: single-balanced active mixer.

1968 [38]. Gilbert mixer as shown in Figure 9 is composed of a balanced grounded transconductance stage, which converts the input voltage signal to the current mode. After input transconductor, the signal is fed to the switching stage, which is driven by a large LO (i.e. 150 mV_{pp}).

Typically the Gilbert-cell mixer is driven with balanced RF and LO signals. If a double-balanced structure either of the RF or LO signals are supplied alone, there is no output signal. Whereas, either of the input signals can be single-ended and the other sides can be ac-grounded. Therefore, The output of the single-ended LNA can be connected to the mixer like in Ref. [39]. In this case, the conversion gain is decreased because only half of the mixer input stage transconductance is utilized. Usually, double-balanced mixers are more interesting for down-conversion receivers, since they generate less even-order distortion, provide high port-to-port isolation, and usually have better noise performance than the single-balanced ones. In addition, single-balanced mixer despite being low power has big problem, which is large LO feedthrough at its output that may saturate the following stage [37].

3.3.1 Mixer input stage

The mixer input stage consists of a balanced grounded CS amplifier or a differential pair with a tail current source as shown in Figures 11(a) and 11(b), respectively.

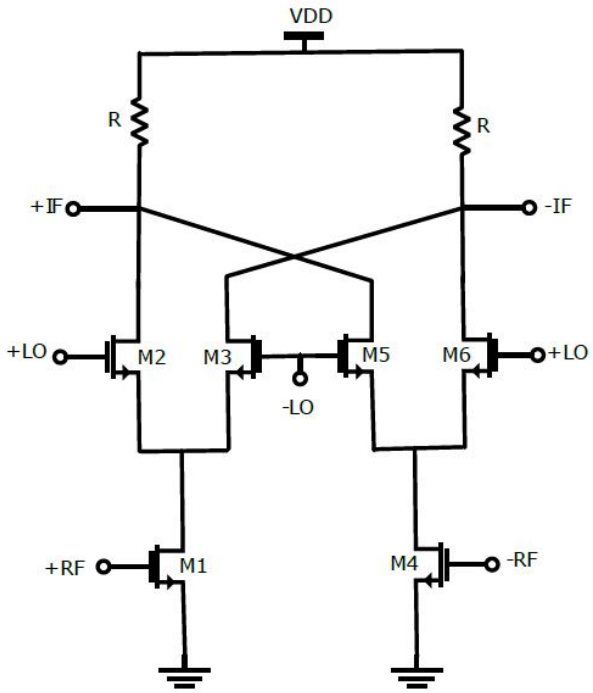


Figure 10: Double-balanced active mixer (Gilbert mixer).

It is crucial that all transistors work in their active mode in order to have a linear system. Typically, each MOS transistor should work in its active mode if the V_{GS} is larger than the threshold voltage and also, V_{DS} is more than the subtraction of gate-source voltage (V_{GS}) and the threshold voltage (V_{th}). Thus, if two structures are biased with the same current and device dimensions, the grounded CS stage has better IIP3 (third-order nonlinearity) performance than the differential pair with a tail current source [40]. However, the tail current source offers a common-mode rejection ratio, and the trade-off of the grounded CS stage is greater sensitivity to supply noise [40].

3.3.2 Conversion gain

The ratio of the output voltage signal at the IF frequency to the RF input voltage signal is called voltage conversion gain. The conversion gain based on the presentation in Ref. [22] is calculated as

$$\frac{V_{\mathrm{IF}}}{V_{\mathrm{RF}}} = \frac{2}{\pi} g_{m1} R_{\mathrm{D}}. \tag{16}$$

Now, it is important to understand the limiting factors of conversion gain. The gain is related to the linearity and voltage headroom. To provide linearity it is important that switching stage transistors perform in their active region.

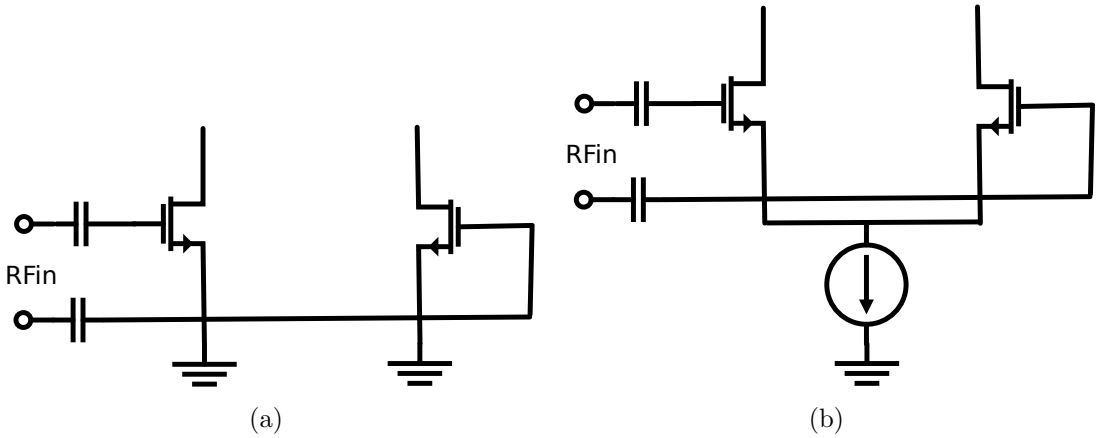


Figure 11: Transconductance stage of mixer: (a) grounded CS stage and (b) differential pair with a tail current source.

On the other hand, size of the input transistor is determined with respect to the overdrive voltage, $V_{\mathrm{GS1}} - V_{\mathrm{TH1}}$ and then $V_{\mathrm{DS,min}}$. The transconductance of M_1 depends on the drain current and it is expressed as $g_{m1} = \frac{2I_{\mathrm{D1}}}{V_{\mathrm{GS}} - V_{\mathrm{TH1}}}$. Also, the value of R_{D} is limited by the maximum allowable dc voltage across it. Therefore, according to the analysis performed in Ref. [22] the conversion gain is given by

$$A_{\mathrm{V,max}} = \frac{2}{\pi} g_{m1} R_{\mathrm{D,max}} = \frac{8}{\pi} \frac{V_{\mathrm{R,max}}}{V_{\mathrm{GS1}} - V_{\mathrm{TH1}}}, \tag{17}$$

which shows that the low supply voltages strongly limit the gain of the active mixer. Thus, a question arises how we can improve the gain. The overdrive of input transistor has limited flexibility unless both the LNA gain and noise of mixer can be lowered. The overdrive of switching transistors can be reduced by widening these transistors, while raising the parasitic capacitors.

When switching transistors are close to equilibrium, the RF current is split approximately equal between them, thus it performs as a common-mode current and it causes small conversion gain. Eliminating the LO swing would reduce the gain.

Another factor that degrades the gain is related to the capacitance seen at the drain of the input transistor. Let us consider a single-balanced mixer as illustrated in Figure 12. When fast LO switching causes M_2 on and M_3 off, total capacitance at node P is

$$C_P = C_{\mathrm{DB1}} + C_{\mathrm{GS2}} + C_{\mathrm{GS3}} + C_{\mathrm{BS2}} + C_{\mathrm{SB3}}, \tag{18}$$

where C_{DB1}, C_{GS2}, C_{GS3}, C_{BS2} and C_{SB3} are the parasitic capacitances of three transistors seen at node P.

Therefore, RF current splits between C_p and resistance has seen at source of M_2, which is $1/g_{m2}$, that causes the reduction of gain by the factor of $\frac{g_{m2}}{SC_p + g_{m2}}$. As it is discussed in Ref. [22] the effect of the C_p may become significant for relatively large frequencies.

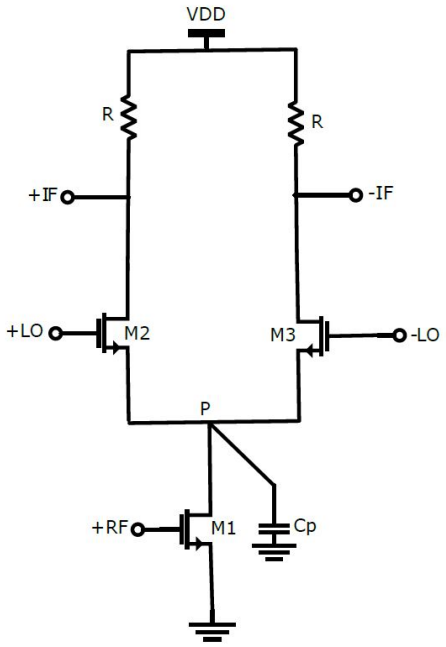


Figure 12: Loss of RF current to ground through C_p.

3.3.3 Mixer noise

Switching transistors can be counted as one of the main sources of noise in the mixer, if they are not sufficiently fast. The thermal noise due to the transconductor stage is at the same frequency as the input RF signal. In down-conversion receiver, it will be down-converted to around DC frequency, just where the IF signal is located. Similarly, any periodic LO waveform down-converts the noise from the odd-harmonics of the LO signal.

Noise of the switching capacitances should be noted, since the noise of these transistors increase by the factor of the differential gain. However, as explained before practically these switches are not fast enough, thus the large LO swing saturates the differential pair, thereby lowering the gain.

3.3.4 Linearity

The linearity, more specifically IIP3, is controlled by both the transconductance stage and the switching stage. As explained before, the linearity of an active mixer is directly proportional to the drive current and the input transistor overdrive voltage. The IIP3 of a common source; increases when the overdrive voltage increases and subsequently this also increases the noise as it is illustrated in the following equations

[22]

$$\begin{aligned} IIP3 &\propto (V_{\mathrm{GS}} - V_{\mathrm{TH}}), \\ \overline{V_{\mathrm{n,in}}{}^2} &= \frac{4KT\gamma}{2I_{\mathrm{D}}}(V_{\mathrm{GS}} - V_{\mathrm{TH}}). \end{aligned} \tag{19}$$

Last but not the least, linearity degrades if the switching transistors enter the triode region.

4 Design Description

4.1 LNA design procedure

In this section, various steps of designing an ultra low power LNA with specific characteristics are introduced and discussed. To obtain our purpose in this project, based on the explanations in the previous sections 2.2 and 2.2.4, the inductively degenerated common source LNA with a cascode stage shown in Figure 13 has been chosen. This project is implemented in a 65-nm CMOS technology. Since this

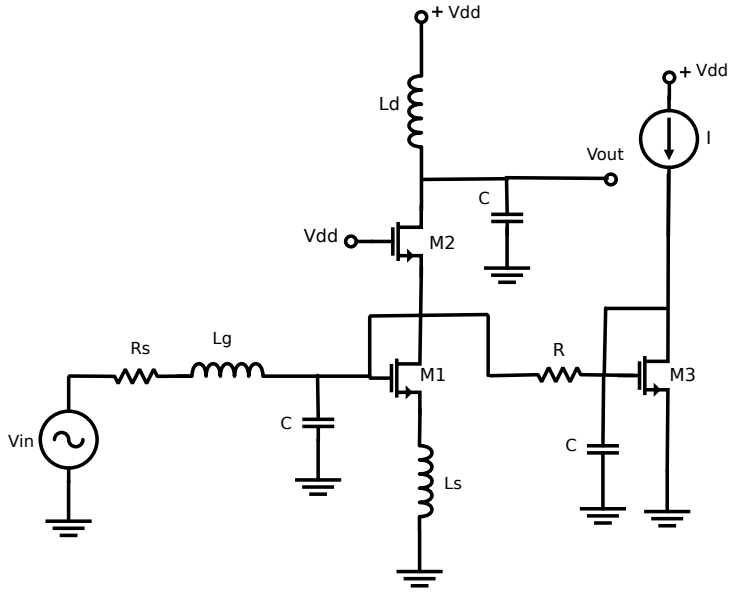


Figure 13: Low noise amplifier with bias system.

receiver is going to be used in Bluetooth applications, the operation frequency is 2.4 GHz and the needed bandwidth is around 100 MHz.

Firstly, we started the work with the design of input matching network in order to to achieve high gain, low noise and low return loss. Figure 14 shows the impedance seen from input which should be equal to 50 Ω. The method used to achieve low noise and impedance matching simultaneously is explained here. Such type of input system is well-studied, and it is common for the most RF receiver designers especially for the ones who choose IDCS-LNA. Figure 13 indicates the considered LNA for our design.

Later in this section, output load design and bias system for this LNA is explained and discussed.

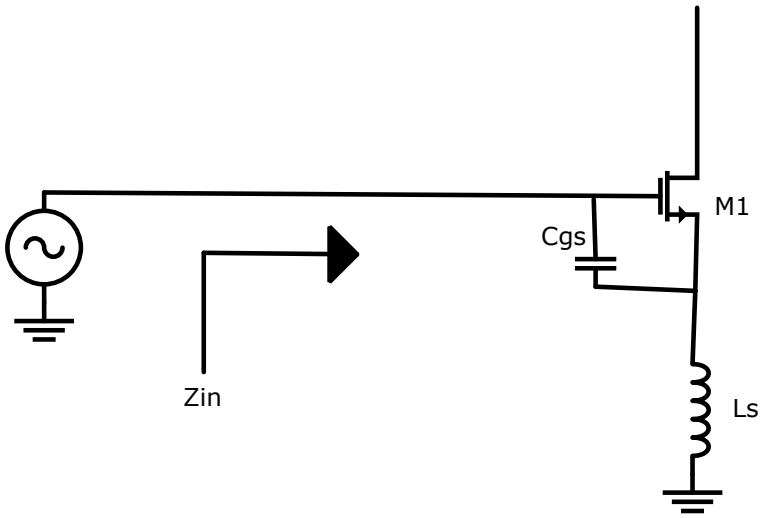


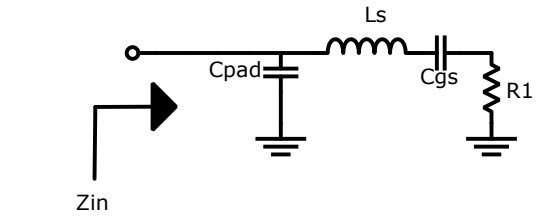
Figure 14: Input impedance of inductively-degenerated CS stage.

For matching, we need to find a topology in which the input is isolated from the inductive load with active devices to provide 50 Ω input resistance without the noise of a resistor. According to the expression for the input impedance which is written in Equation 7, L_{S}, L_{g} and C_{gs} are the main components that have to be noted during input matching adjustment. As we explained before, the real part of the equation should be equal to 50 Ω. Since $\frac{g_m}{C_{\mathrm{gs}}} \approxeq \omega_T$ ($\omega_T = 2\pi f_T$, where f_T is the maximum operating frequency of the transistor), the input resistance is approximately equal to $L_{\mathrm{S}}\omega_T$ and directly related to the f_T of the transistor. In our case for the used 65-nm technology, $\omega_T \approxeq 2\pi\times160$ GHz, thus L_{S} is calculated to be 50 pH [22].

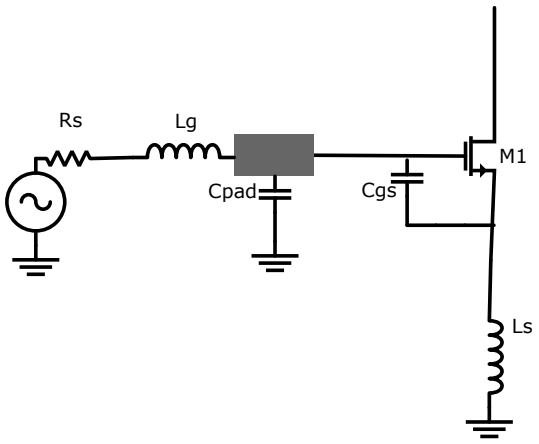
Practically, the degenerating inductor (L_{S}) is often realized as a bond wire, since the use of packaging is inevitable in the design. In order to minimize the inductance, the source can connect to the ground plane in the package directly. However, the value of inductor from geometry is around 1nH, therefore, in this case the input impedance is much higher than 50 Ω. In order to obtain input matching at a frequency lower than f_T we can use a capacitor in parallel with C_{gs}. Moreover, one of the important aims of this work is to design ultra low power amplifier. To realize this goal transistors dimensions should be small which results in small parasitic capacitances in femto farad range or even smaller. Therefore, a parallel capacitor can be used in order to neglect the effect of these parasitic capacitors. The value of this capacitor can be chosen with respect to two issues: firstly, to overcome the effect of parasitic capacitors, and secondly to maintain the impedance matching.

In addition, the effect of pad capacitance lowers the input resistance. Usually, a pad is modelled by a capacitor. Figure 15(a) shows the equivalent circuit of the input stage, where R_1 is the resistance of the transistor. The effect of the parasitic and pad capacitances cannot be matched just by L_{s}, thus another inductor must be placed in series with the gate as shown in Figure 15.

Let us explain about our LNA, since the transistors are small, then for matching we used a parallel capacitor (C=113 fF) which can be equal the summation of pad



(a)



(b)

Figure 15: Input stage of LNA: (a) equivalent circuit for inclusion of pad capacitance and (b) input stage with pad.

capacitor and $C_{\rm gs}$. Also, $L_{\rm g}$ is added in the gate that is off-chip inductor. The value of these components are calculated from Equation 20 with respect to the frequency of 2.4 GHz.

$$\omega_0{}^2 = \frac{1}{LC} = \frac{1}{(L_{\rm S} + L_{\rm g})(C_{\rm gs} + C_{pad})}. \tag{20}$$

Therefore, after finding out the component values, we began the simulation in order to obtain the best impedance matching. Figure 16 shows the final schematic we obtained without considering the pad effect.

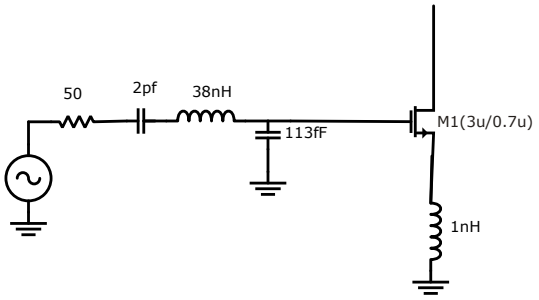


Figure 16: Input stage without pad.

Later, after including the bonding pad connection to the schematic the simulation results changed, thus, we had to adjust the matching network again, and hence the component values have changed. Figure 15(a) illustrates the equivalent circuit of used pad connection. in other words, the practical pad connection has some other parasitic effects than just capacitance as it is depicted in Figure 17.

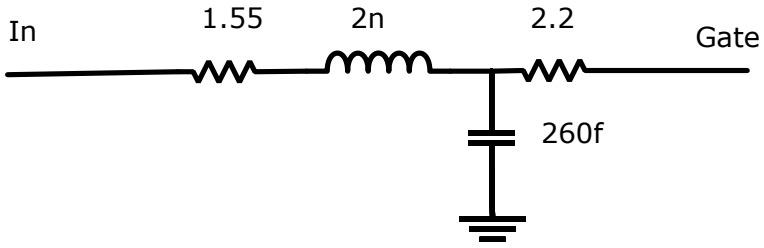


Figure 17: Pad equivalent circuit in our design.

As a consequence, the components that depicted in Figure 17 have also contributed in impedance matching. Therefore, the repetition of the whole optimization stages is necessary to gain the best possible input matching. We must admit this structure degrade the NF of the system while in reality avoiding all parasitic effects are impossible.

Now, it is the turn of designing the output node of the topology. As explained earlier, an inductive load connected to the common source stage produces a negative resistance due to the feedback through C_{GD}. Thus, we add a cascode transistor in the output in order to abolish this effect. Figure 18 shows the resulting circuit, where R_1 model the loss of L_{D}. The voltage gain is dependent on the R_1 and the circuit transconductance which has been analysed in Ref. [22].

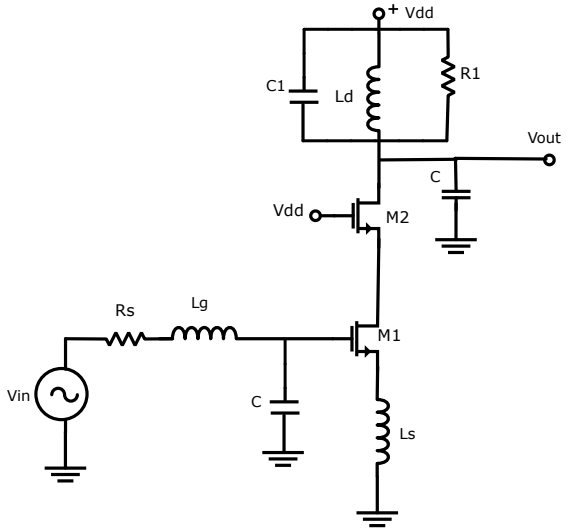


Figure 18: Inductively-degenerated cascode common-source LNA.

However, in our design, we use non-ideal inductor which has its own model like Figure 19. As the Figure shows non-ideal inductor has capacitance and resistance,

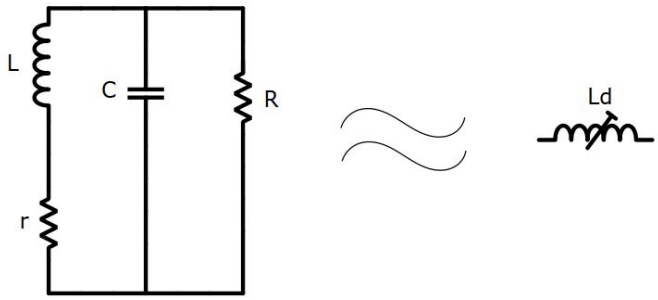


Figure 19: Equivalent circuit of non-ideal inductor.

therefore R_1 and C_1 can be removed. In this part by using simulations we try to obtain maximum gain at the resonant frequency of (2.4 GHz). The best option here is to use a capacitor in output bigger than all parasitic capacitances (drain-bulk and drain-gate of M_2 and L_D)in order to neglect the effect of parasitic capacitances. Thus, this capacitor would resonate at resonance frequency with respect to the value of L_D.

Furthermore, the dimensions of the cascode device are chosen equal to the input transistor. Therefore, in the layout stage since the source of cascode device is connected to the drain of the input transistor they can be placed on each other.

Finally, the overall LNA appears as shown in Figure 20, where the antenna is capacitively tied to the receiver to isolate the LNA bias from external connections. The bias current of M_1 is formed by M_B and I_B, and resistor R_B and capacitor C_B to isolate the signal from the noise of M_B and I_B. R_B is chosen much larger than R_S to avoid noise contribution. The dark gray box represents the pad that has been introduced in Figure 17. Moreover, the pad should be placed between all on-chip and off-chip components and connections such as ground, V_{dd} and the bias current source. We avoid drawing whole pad equivalent circuit for simplicity and the convenience of the reader. Table 1 indicates the component values of inductively degenerated LNA in either with pad consideration or without the pad.

4.1.1 Stability of LNA

The stability is an important issue for an amplifier. It can be determined using S-parameters, matching network and termination. This system becomes unstable if either output or input sees negative impedance [25]. The stability of a system can be determined by Stern stability factor,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{21}$$

where the $\Delta = S_{11}S_{22} - S_{12}S_{21}$. A system is stable provided that two important conditions $K > 1$ and $\Delta < 1$ are valid. Based on the Equation 21 the designed

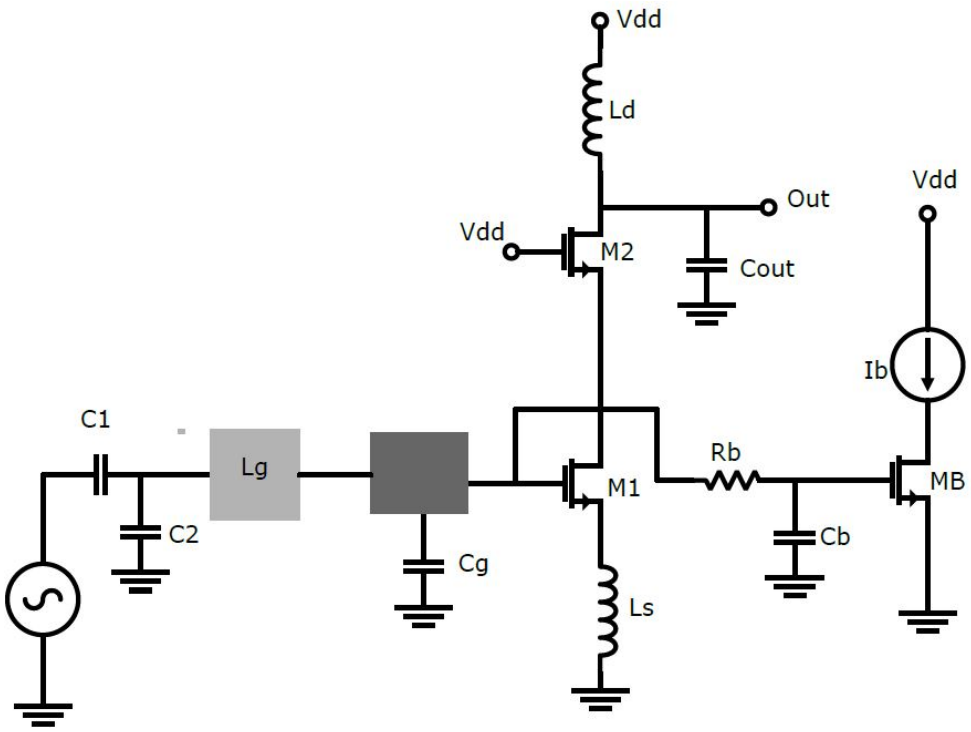


Figure 20: Equivalent circuit of non-ideal inductor.

inductively degenerated LNA is stable since $K = 980$ and $|\Delta| = 0.1$.

4.1.2 Simulation result

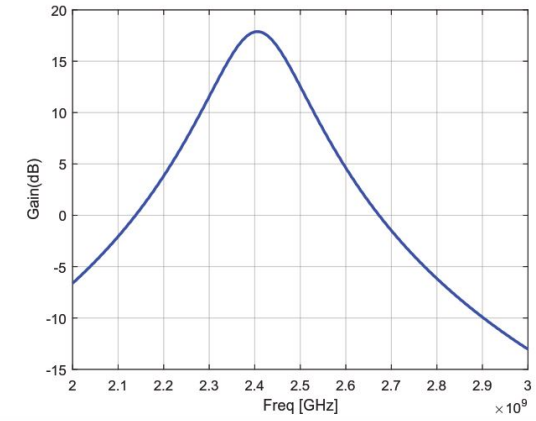
Here in this section obtained simulation results have been collected and shown. Figure 21 shows the simulated characteristics of designed LNA drawn in Figure 20. Obtained gain is demonstrated in Figure 21(a), Figure 21(b) indicates achieved return loss (S_{11}), and Figure 21(c) shows the noise figure (NF) of this topology. Furthermore, simulated gain, 1-dB comparison point and IIP3 of the LNA are collected in Table 2. Further, In Figures 22(a) and 22(b), S_{11} and NF in the two situations with and without pad effect have been shown. As it can be seen and explained, NF is slightly smaller when we have not considered pad affects in addition to the NF, input band-width has compressed.

Table of transistor parameters and component values		
Component	in simulation without pad	in simulation with pad
M_1	$\frac{4\mu m}{0.07\mu m}$	$\frac{4\mu m}{0.07\mu m}$
M_2	$\frac{4\mu m}{0.07\mu m}$	$\frac{4\mu m}{0.07\mu m}$
M_B	$\frac{2.8\mu m}{0.07\mu m}$	$\frac{2.5\mu m}{0.07\mu m}$
I_B	70 μA	55 μA
R_B	7 KΩ	7 KΩ
Supply Voltage	1.2 V	1.2 V
L_s	1 nH	1 nH
L_d	2.95 nH	5.16 nH
L_g	38 nH	16 nH
C_{out}	960 fF	480 fF
C_g	113 fF	260 fF
C_1	2 pF	10 pF
C_2	-	2.2 pF

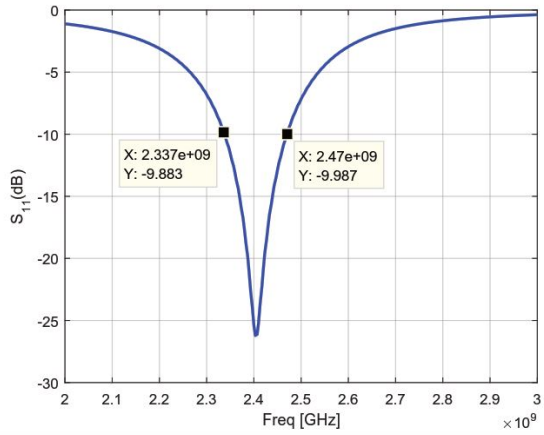
Table 1: Component values of LNA in both conditions when the pad has considered and has not.

Simulation results table	
I_{dc}	70 μA
Supply Voltage	1.2 V
I_{ds}	95 μA
P_{dc}	114 μW
$1-dB$ *compression point*	-18 dBm
BW	130 MHz
NF	5.09 dB
IIP3	-8.44 dBm
Gain	17.33 dB

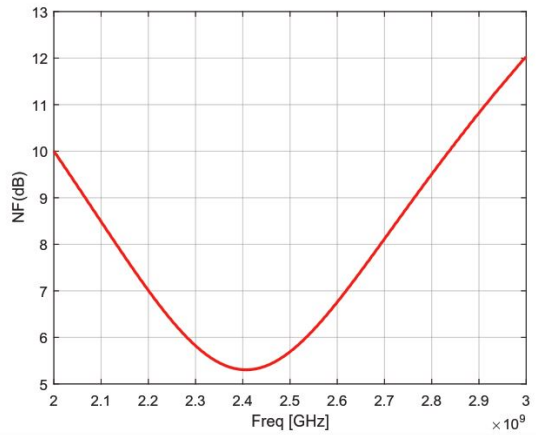
Table 2: Obtained properties of single-ended LNA.



(a) Gain

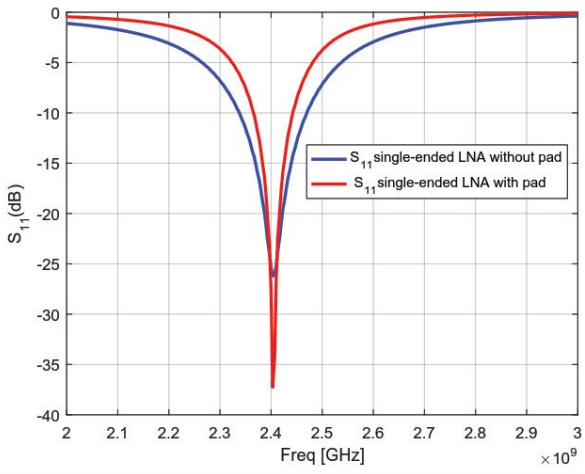


(b) Return loss

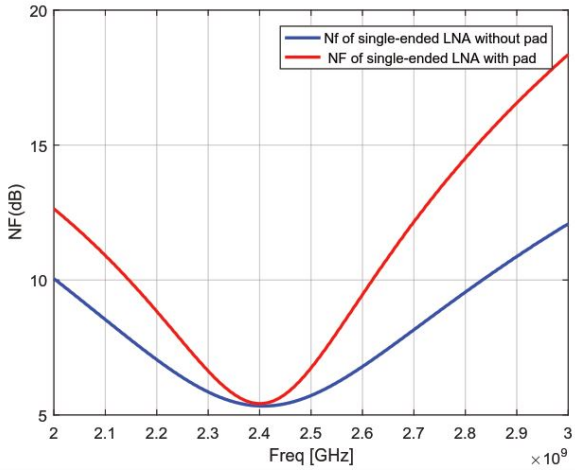


(c) Noise figure

Figure 21: Properties of Single-ended amplifier with pad inclusion.



(a) Return loss



(b) Noise figure

Figure 22: Comparison of single-ended amplifiers with pad inclusion and without pad.

4.2 Differential cascode LNA

In previous sections, the advantage of the double-balance mixer compares to the single-balance counterpart have been explained. Furthermore, we discussed that in practice with our technology using differential LNA is more efficient than using single-ended LNA. Additionally, the preference towards using differential LNA architecture due to the ability in rejecting common-mode noise is derived in Ref. [41].

Therefore, we duplicated our single-ended LNA to provide fully differential LNA with the same characteristics which we had for the single-ended LNA. Figure 23 demonstrates the differential LNA schematic and Figure 24 shows the simulation results of this system.

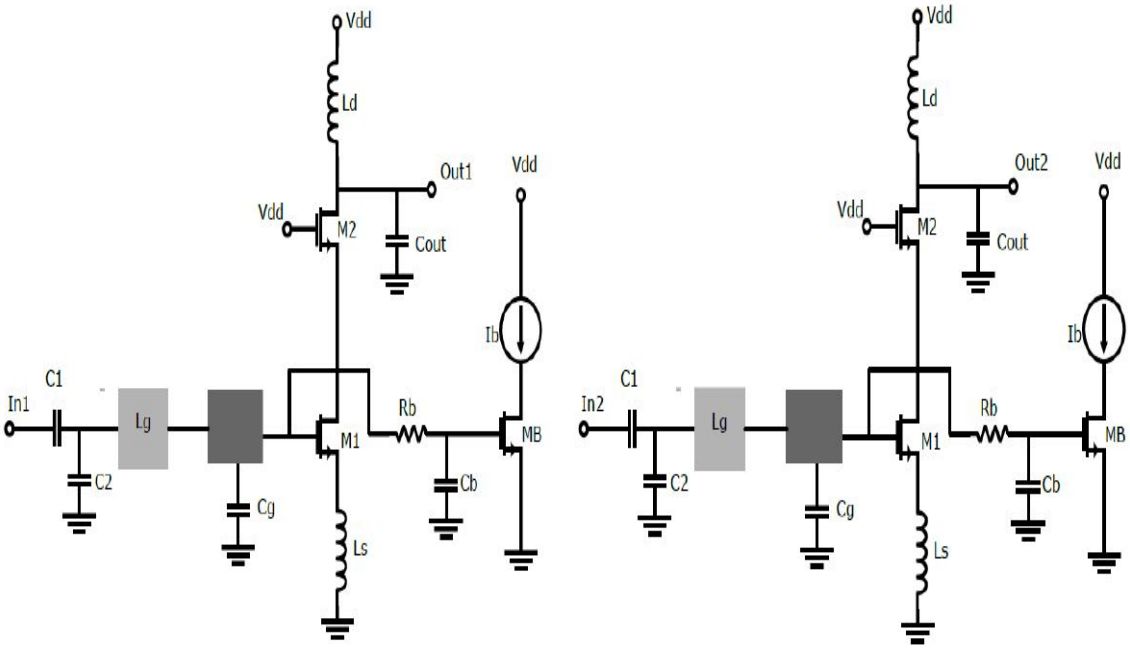
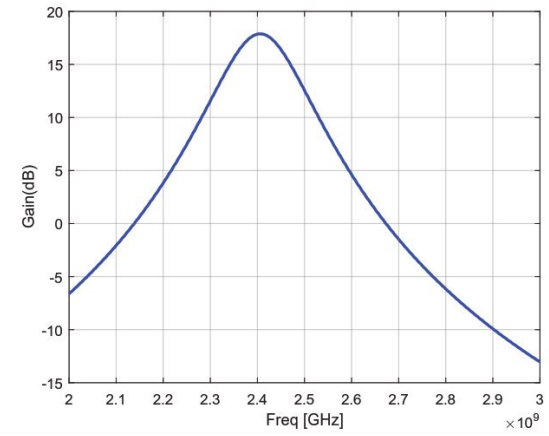
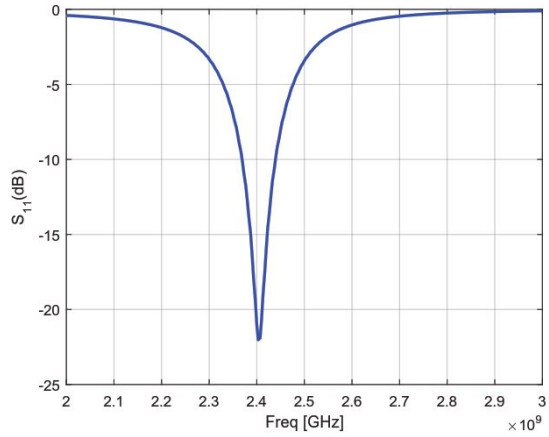


Figure 23: Differential LNA which consists of two single-ended LNA that introduced in the previous section.

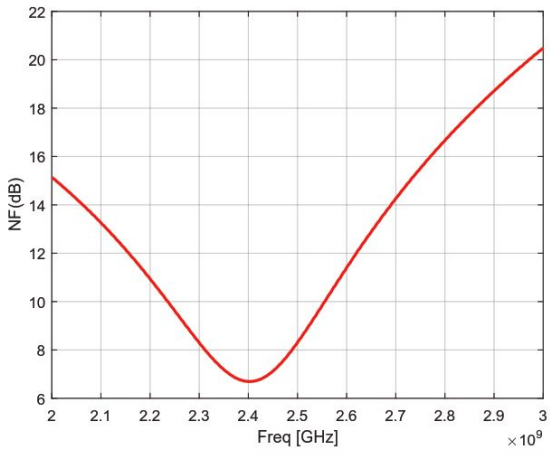
Moreover, In Table 3 the simulated performance of the designed LNA is compared with other similar LNAs found from the literature.



(a) Gain



(b) Return loss



(c) Noise figure

Figure 24: Properties of differential amplifier with pad inclusion.

Comparison Table					
Parameter	LNA of This work	[42]	[43]	[44]	[45]
CMOS Technology	65 nm	65 nm	18 μm	18 μm	13 μm
Frequency	2.4 GHz	2.45 GHz	2.57 GHz	2.44 GHz	2.4 GHz
Gain [dB]	17.5	27.5	16.6	12.5	13.1
NF [dB]	6.5	9	3.5	3.9	5.3
S_{11} $[dB]$	-22	-	-	-16	-
Supply Voltage [V]	1.2	0.8	1.8	1.8	0.4
P_{dc}	228 μW	100 μW	12.6 mW	2.7 mW	60 μW
IIP3 [dBm]	-8.44	-9	-	-	-

Table 3: Result comparison of various LNA design.

4.3 Mixer design procedure

In this section, we discuss some practical steps in the design of the down-conversion mixer that we have chosen and also some details of simulations. Furthermore, mixer properties and then the obtained results are shown in Tables 4 and 5, respectively.

In this work according to what we have discussed earlier in section 3, we decided to choose the active double-balanced mixer, Gilbert-cell mixer, as depicted in Figure 10.

As we explained overdrive voltage and operation region of the transistors are very important in mixer performance. Therefore, transistor sizes in both transconductance and switching stages are significant. We start our design with some simultaneous changes for the size of transistors and bias voltages in order to ensure that all transistors are performing in the active region. Moreover, the value of R should be selected carefully, since very large value reduces voltage head-room of switching transistors and small one degrades the conversion gain. In Table 4 mixer properties has been gathered and shown.

Table of component values of Figure 10		
Component	in simulation without pad	in simulation with pad
M_{RF}	$\frac{1.5\mu m}{0.07\mu m}$	$\frac{3\mu m}{0.07\mu m}$
M_{LO}	$\frac{2.4\mu m}{0.07\mu m}$	$\frac{3\mu m}{0.07\mu m}$
$V_{Bias,LO}$	1.2 V	1.2 V
$V_{Bias,RF}$	700 mV	700 mV
f_{RF}	2.4 GHz	2.4 GHz
f_{LO}	2.41 GHz	2.41 GHz
R	4 KΩ	4 KΩ
I_{RF}	94.5 μA	96 μA
Supply Voltage	1.2 V	1.2 V

Table 4: Table of Gilbert mixer value when the pad has been considered and has not.

Furthermore, ideal LO waveforms are a square wave from a zero source impedance with a large voltage swing, the time which four devices are on at the same time is zero. This guarantees for fast switching and then maximum conversion gain. However, at very high frequency, the LO wavefront is similar to a sinusoid, therefore there is a period of time that all transistors are on which causes wasting of the input signal. As a result, we choose large amplitude for LO so as to achieve high slew rate and minimize overlap time [22].

Our desire is to design direct-conversion mixer, but due to some simulation problems in zero frequency we select LO frequency close to the RF frequency but not equal to it, as it can be seen in Table 4.

Now, after ensure about the DC operation of all transistors we can check other performance of our topology such as conversion gain, noise figure and linearity. The

achieved results of the simulation are classified in Table 5. As it can be seen that the noise of our topology is high, while LNA gain is almost close to the noise of the mixer, thus it is acceptable.

Table of Gilbert mixer results	
Parametert	result
Conversion Gain	5 dB
NF	18 dB
IIP3	-5.46 dBm

Table 5: Obtained results from simulation of Gilbert mixer.

Now we connect the designed differential LNA and Gilbert mixer. These two systems are going to be placed on the same chip with a short distance, and since our frequency is not that high we do not need intermediate impedance matching. Therefore, we just need to consider the effect of the input capacitance of RF transistor of mixer in the output of LNA. Additionally, we need to add a coupling capacitor to block DC and to be shorted in AC. Figure 25 illustrates the whole circuit.

In this design, we have used the same pad as in the LNA, therefore the component values and results in both with pad and without pad design are collected and indicated in Table 6. Additionally, we have to remind the reader that, the pad should be connected to all nodes which are going out from the chip. However, as in LNA design, we avoid drawing all pad connections in Figure 25 in order to have more understandable and clear schematic view.

Furthermore, some simulation results of this architecture such as $(\frac{V_{IF1}-V_{IF2}}{V_{in1}-V_{in2}})$ conversion gain of LNA+ mixer and $(\frac{V_{IF1}-V_{IF2}}{V_{RF1}-V_{RF2}})$, conversion gain of mixer and noise (NF) are shown in Table 6. Corresponding figures from the simulations of the whole system are shown in the next section in Figure 31 in order to ease the comparing of pre-layout and post-layout simulation results.

Table2 of component values of Figure 25		
Component	in simulation without pad	in simulation with pad
M_{RF}	$\frac{1.5\mu m}{0.07\mu um}$	$\frac{1.5\mu m}{0.07\mu m}$
M_{LO}	$\frac{2.4\mu m}{0.07\mu m}$	$\frac{2.4\mu m}{0.07\mu m}$
M_1	$\frac{4\mu m}{0.07\mu m}$	$\frac{3\mu m}{0.07\mu m}$
M_2	$\frac{4\mu m}{0.07\mu m}$	$\frac{3\mu m}{0.07\mu m}$
M_3	$\frac{2.8\mu m}{0.07\mu m}$	$\frac{2.5\mu m}{0.07\mu m}$
V_B	1.2 V	1.2 V
$g_{m,RF}$	460.8 $\mu\upsilon$	709.3 $\mu\upsilon$
g_{m1}	1.04 $\mu\upsilon$	987 $\mu\upsilon$
$V_{th,RF}$	585.2 mV	583.5 mV
$V_{th,LO}$	657.7 mV	651 mV
I_B	70 μA	55 μA
$V_{Bias,LO}$	1.2 V	1.2 V
$V_{Bias,RF}$	700 mV	700 mV
f_{RF}	2.4 GHz	2.4 GHz
f_{LO}	2.41 GHz	2.41 GHz
R	6 KΩ	4 KΩ
I_{RF}	94.5 μA	96 μA
$(\frac{V_{IF1}-V_{IF2}}{V_{in1}-V_{in2}})$	21.9 dB	20 dB
$(\frac{V_{IF1}-V_{IF2}}{V_{RF1}-V_{RF2}})$	2.1 dB	3.6 dB
NF	14.4 dB	16 dB
Supply Voltage	1.2 V	1.2 V
C_{out}	450 fF	450 fF
C_c	2 pF	2 pf

Table 6: Table of Gilbert mixer value when the pad has been considered and has not.

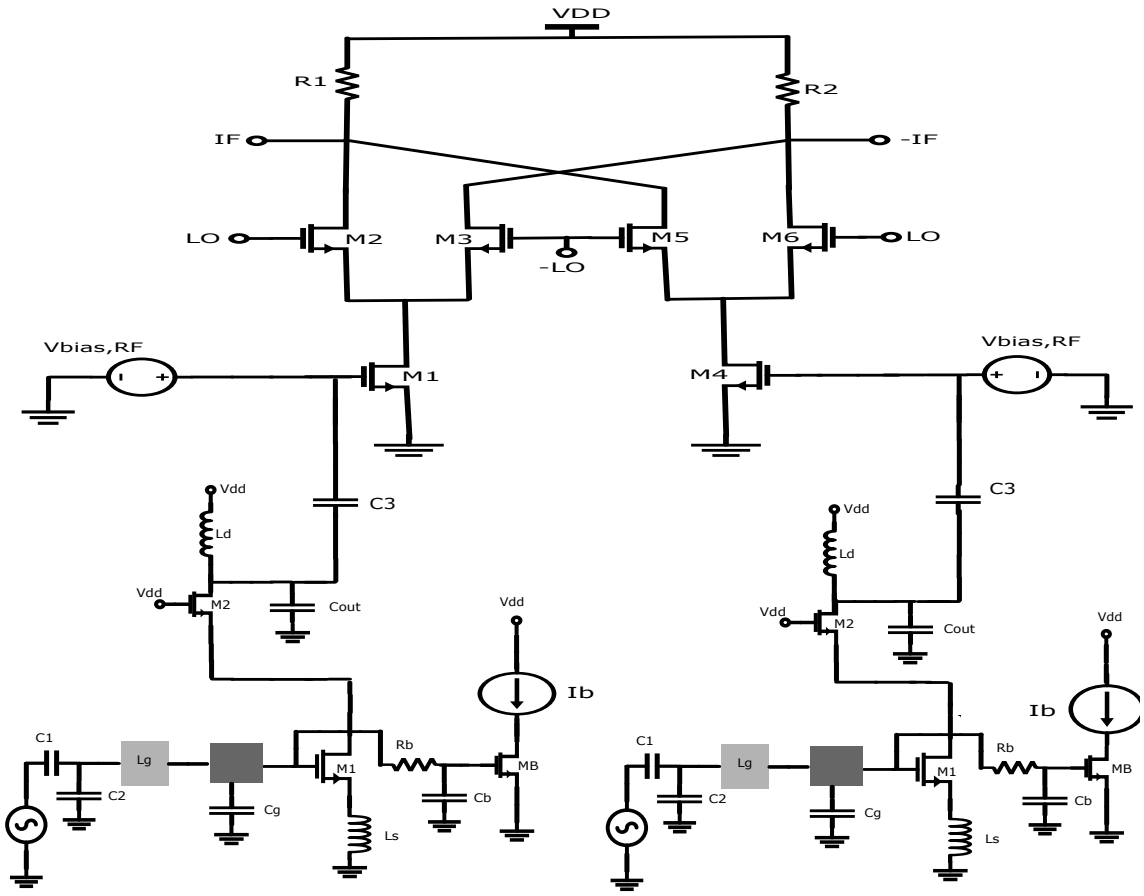


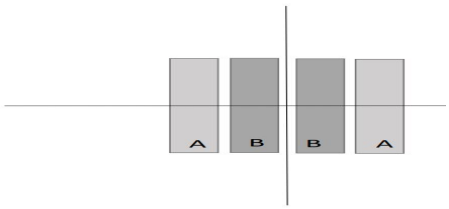
Figure 25: Differential LNA connected to the gilbert mixer.

5 Physical Layout and Post-Layout Simulation Results

5.1 Layout design

In this section, the LNA+mixer layout and post-layout simulations are discussed. The tool used for the layout and post-layout simulation is virtuoso layout editor.

In layout design there are some issues which should be noted in order to obtain the best performance. Microscopic fluctuations in dimensions, doping, oxide thickness and other parameter cause random mismatches which affect on the component values. Although these effects cannot be entirely eliminated, but they can be minimized. Therefore, there is a method called common-centroid layout that can be used in order to firstly reduce some mismatches, and secondly to shrink large devices to smaller ones with the same properties. The common-centroid layout is the most useful technique for minimizing stress-centroid mismatches. In this arrangement, device should be split into two identical parts which are located symmetrically compared to the center axis. Figure 26 shows an example of common-centroid layouts produced by arraying segments of matched elements along one dimension. This type of layouts are called interdigitated arrays. Since the sections of one element interpenetrate the section of the other like the intermeshed fingers of two hands, more details about matching and this type of arrangement can be found in Ref. [46].



(a)

Figure 26: Example of common-centroid array.

In addition to device mismatches, the wiring also causes parasitic effect in the circuit. Generally, the on-chip wires are characterized as RC lines, thus the signals attenuate over the long signal paths, and may also couple to each other. Therefore, the following considerations must be taken into account to avoid unwanted parasitic effects.

Firstly, metal selection for connection is an important issue. For instance, the path between devices and supply voltage must be wide and with low impedance in order to minimize the voltage variation. This is a noticeable issue since it may lead the transistors in the triode region and degrade the linearity.

Secondly, to protect the structure from coupling and cross-talk, an appropriate distance between two metal paths should be always kept. Moreover, we have to avoid using long parallel paths with the same type of metal.

In our design due to limited number and small size of transistors we prefer to

use interconnection method. Due to the large size of the resistors, we divided them to the several smaller resistors and then connected them in series. Therefore, we created a more compact structure with smaller resistors. The designed resistor R_{B} is indicated in Figure 27, the 7 KΩ resistor is divided to the eight 875 Ω resistors and then they are connected in series. By the help of this method size of the resistor has reduced significantly.

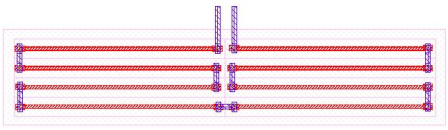


Figure 27: Modeled R_B layout.

Initially, we started with the single-ended LNA layout, we tried to design symmetrical architecture to minimize the parasitics and size of the structure. During the design we run DRC (design-rule-checking) Calibre regularly, to be sure that the designed layout satisfies the parameters of design rules such as proper distances and size of elements. After that, LVS(Layout versus schematic) Calibre was run in order to confirm the similarity of layout and schematic. The parasitics of the designed layout was extracted by running PEX Calibre, and then these parasitics were imported into the simulation as in section 5.2.

After finding proper performance from the single-ended layout, with duplication the differential LNA layout was created. Later, we designed mixer layout as shown in Figure 28 and then we combined the two systems as depicted in Figure 29. This Figure shows the final layout of the differential inductively degenerated common source LNA connected to the Gilbert mixer. Due to the large area of inductors, the other components are hardly seen.

After all, the on-chip parasitics cannot be completely removed, thus the on-chip performance usually differs from circuit-level simulation results. Therefore, post-layout simulations must be carried out in order to obtain more realistic results. The following section describes the post-layout simulation results.

5.2 Post-layout simulation results

Here in this section, all of the simulations in previous sections are repeated with the on-chip parasitic extraction.

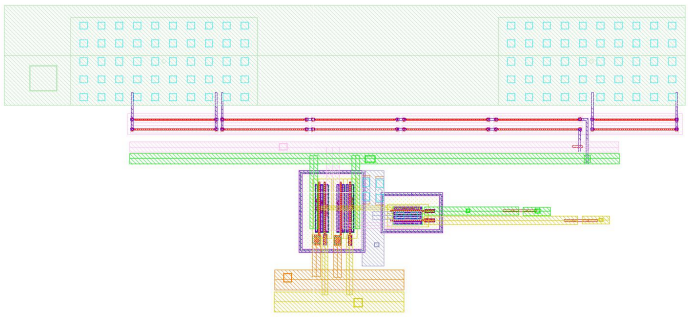


Figure 28: Mixer layout.

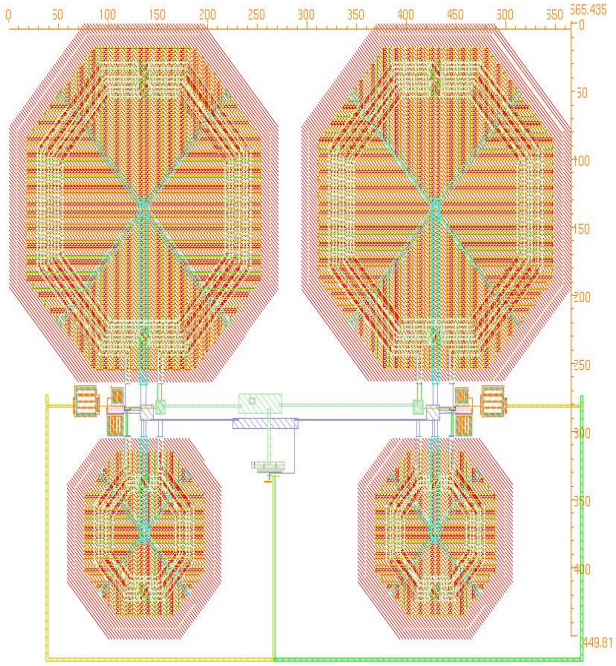


Figure 29: Differential LNA connected to the Gilbert mixer layout.

In Figure 30 the comparison of the pre-layout simulation and the post-layout simulation of differential LNA is reported. As it can be clearly seen, the results are very close in both conditions, thus the parasitics do not affect the performance of the differential LNA so much. However, according to Figure 30(a) The gain of the LNA in the post-layout simulation has dropped by 2 dB, but it has considerably larger bandwidth. The second plot illustrates S_{11} comparison, where the induced parasitics have changed the matching slightly, thus resonance has shifted gently, while S_{11} is still very good at the frequency of resonance. Finally, the noise figure of the differential LNA has increased approximately by 1 dB based on Figure 30(c). From all of these results, we can conclude that in the LNA layout design, we relatively

eliminated the parasitic effects in good extent.

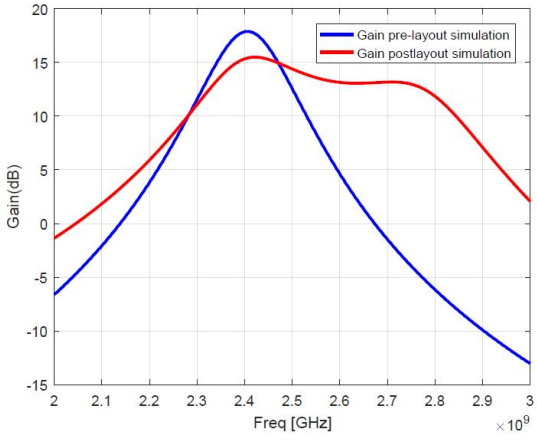
Finally, the post-layout simulation results of the whole system are compared with the simulation results of the pre-layout simulations. Table 7 reports the conversion gain of the system. It is obvious that, the conversion gain ($\frac{V_{\rm IF}}{V_{\rm in}}$) after consideration of parasitics has reduced by 4 dB. However the conversion gain of mixer ($\frac{V_{\rm IF}}{V_{\rm RF}}$)has not changed considerably. In addition to the table, Figure 31 depicts and compares the obtained noise figure and S_{11} of the topology.

Figure 31(d) shows the input voltage of the system versus the IF voltage, and it is clear that the pre-layout system works linearly for $V_{\rm in} < 90$ mV, while after consideration of parasitics the linear performance is for $V_{\rm in} < 40$ mV.

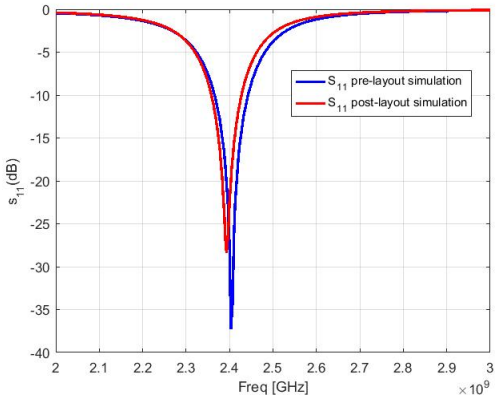
Finally, Figure 32 depicts the variations of S_{11}, NF of LNA and conversion gain of the whole system in Monte Carlo simulation respectively. From these figures one can see even by variation of operation points the achieved results are close to the desired results, therefore designed system is reliable.

Table of conversion gain comparison of whole system		
Parameter	Pre-layout simulation	Post-layout simulation
Conversion Gain ($\frac{V_{\rm IF}}{V_{\rm RF}}$)	3.17 dB	3.2 dB
Conversion Gain ($\frac{V_{\rm IF}}{V_{\rm in}}$)	20 dB	16 dB

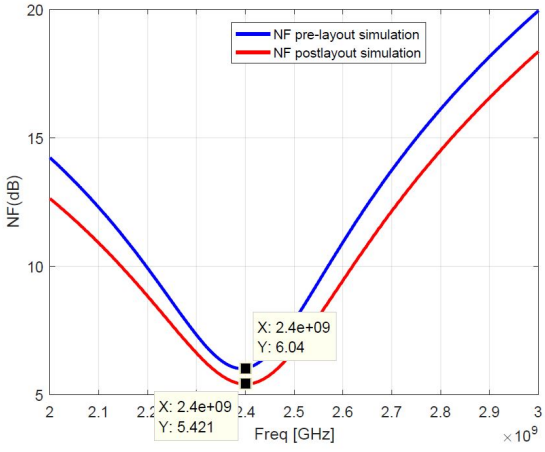
Table 7: Achieved conversion gain conversion in pre-layout and post-layout simulation.



(a) Gain

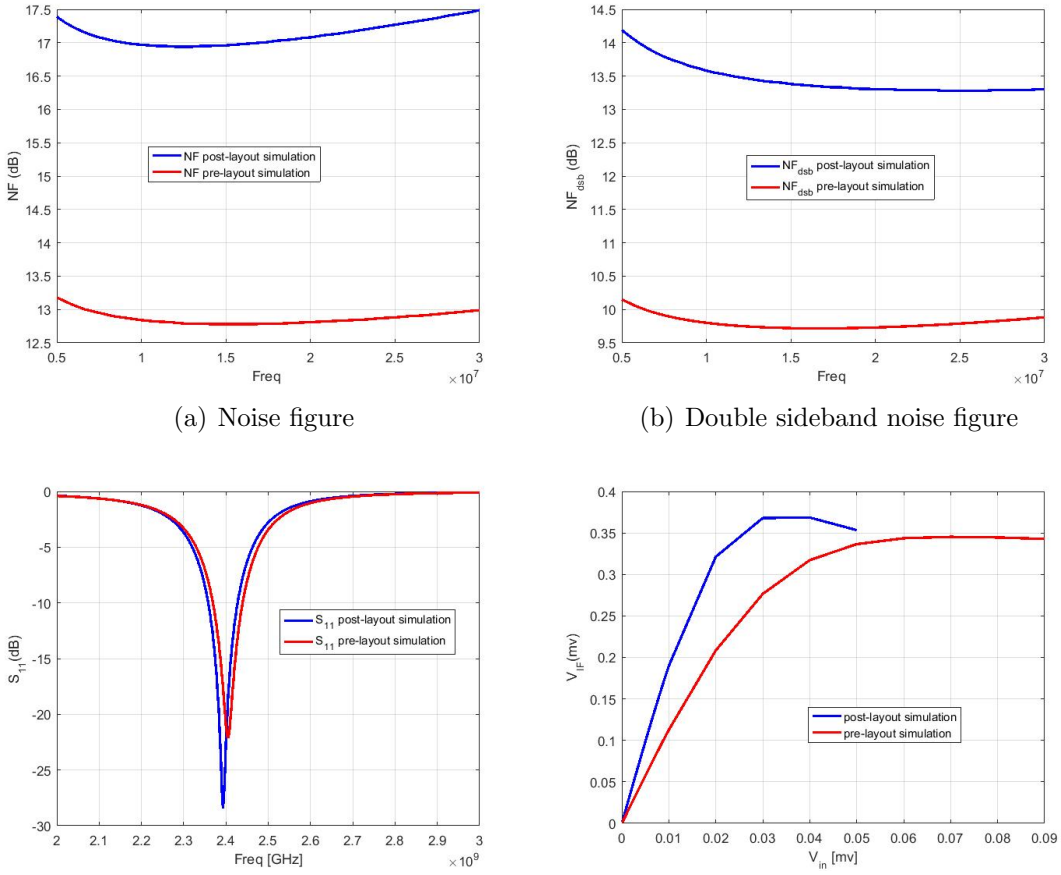


(b) Return Loss



(c) Noise figure

Figure 30: Comparison of pre-layout simulation and post-layout simulation results of differntial LNA.



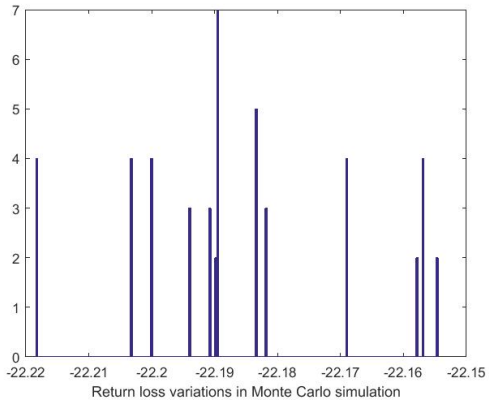
(a) Noise figure

(b) Double sideband noise figure

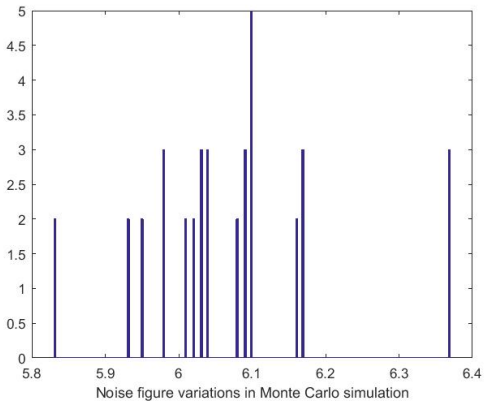
(c) Return loss

(d) Linearity

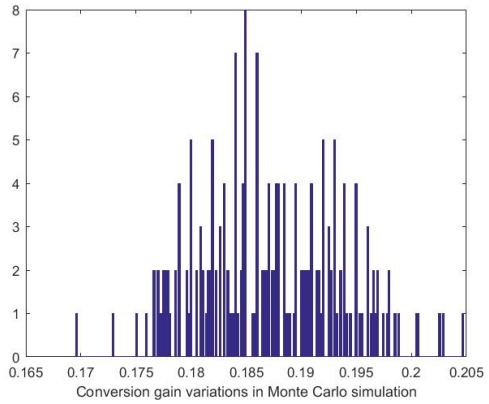
Figure 31: Comparison of pre-layout simulation and post-layout simulation of whole system.



(a) Return loss



(b) Noise figure



(c) Conversion gain

Figure 32: Variations in Monte Carlo simulation.

6 Conclusion and Future Work

The main aim of this work was to investigate and to design an ultra-low power LNA and mixer for a front-end receiver for Bluetooth applications. These structures are capable to achieve simultaneously high gain, low noise and high linearity using a 65nm CMOS technology. As it was expected ultra-low power system was designed.

In the first part, a very low power single-ended LNA with a proper input matching network was designed which yielded the input return loss of -26 dB and noise Figure of almost 5 dB. Moreover, this LNA by consuming just 114 μW provides good gain around 17.5 dB. Then, the fully differential LNA was designed by combination of two single-ended LNAs. Since the performance of single-ended LNA was very good, the obtained differential LNA also worked similarly, while it consumed twice more power, around 228 μW.

In the second part of the work down-conversion active mixer was designed. This mixer is built so as to work with approximately the same power consumption of the differential LNA. Therefore, the whole consumed DC power is less than 500 μW which is the lowest power for such architecture until now. Furthermore, the mixer performed very good as itself alone with the conversion gain of around 3 dB.

In the third part of the design, differential LNA was connected to the designed mixer. This structure with low power produces 20 dB voltage gain and 6 dB noise figure.

In the last part, the layout of all explained devices was designed and calibrated. This level has to be done in order to consider the parasitic effects of the design and also, simulate the design in the most similar condition to the real chip built in a factory. The obtained results of post-layout and pre-layout simulations were compared. Subsequently the enough accuracy of the design is confirmed.

It is worth noting that in continuation of this work, one should design local oscillator and finalize the receiver design, because this work is a part of the whole transceiver. Therefore, all blocks must be designed and implemented.

References

[1] V. H. Le, S. -K. Han, J. -S. Lee, and S. -G. Lee, "Current-reused ultra low power, low noise LNA mixer", *IEEE Microw. Wireless Compon. Lett.,* vol. 19, no. 11, Nov. 2009, pp. 755–757.

[2] H. -K. Chiou, K. -C. Lin, W. -H. Chen, and Y. -Z. Juang, "A 1-V 5-GHz self-bias folded-switch mixer in 90-nm cmos for WLAN receiver", *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 59, no. 6, 2012, pp. 1215–1227.

[3] I. Kwon, "A single-chip CMOS transceiver for UHF mobile RFIC reader", *IEEE J. of Solid-Satate Circuits,* vol. 43, no. 3, March 2008, pp. 729–738.

[4] W. -K. Chong, H. Ramiah, G. -H. Tan, N. Vitee, and J. Kanesan, "Design of ultra-low voltage integrated CMOS based LNA and mixer for ZigBee application", *Int. J. Electron. Commun.,* vol. 68, no. 2, Feb. 2014, pp. 138–142.

[5] H. T. Friis, " Noise Figures of Radio Receivers", *Proceedings of the IRE,* vol. 32, no. 7, 1944, pp. 419–422.

[6] E. A. M. Klumperink, F. Bruccoleri, and B. Nauta, "Finding all elementary circuits exploiting transconductance", *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 48, no. 11, Nov. 2001, pp. 1039–1053.

[7] G. Cusmai, M. Brandolini, P. Rossi and F. Svelto, "A 0.18-um CMOS selective receiver front-end for UWB applications", *IEEE J. of Solid-Satate Circuits,* vol. 41, no. 8, Aug. 2006, pp. 1764–1771.

[8] A. Liscidini, M. Brandolini, D. Sanzogni and R. Castello, "A 0.13-um CMOS front-end for DCS1800/UMTS/802.11b-g with multiband positive feedback low-noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 41, no. 4, April 2006, pp. 981–989.

[9] R. -F. Ye, T.-S. Horng, J.-M. Wu, "Two CMOS dual-feedback common-gate low-noise amplifiers with wideband input and noise matching", *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, Oct. 2013, pp. 3690–3699.

[10] J. Kim, S. Hoyos, J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise gain and bandwidth optimization", *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, Sep. 2010, pp. 2340–2351.

[11] C.-F. Liao and S.-I. Liu, "A broad band noise canceling CMOS LNA for 3.1-10.6 GHz UWB receivers", *IEEE J. of Solid-State Circuits*, vol. 42, no. 2, Feb. 2007, pp. 329–339.

[12] D. K. Shaeffer and T. H. Lee, "A 0.5-V 1.5-GHz CMOS low noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, May 1997, pp. 745–759.

[13] J. Kaukovuori, *CMOS Radio Frequency Circuits for Short-Range Direct-Conversion Receiver, TKK Doctoral Dissertation*, Espoo, 2008.

[14] W. Zhuo, S. Embabi, J. de Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down conversion mixer design", in *Solid-State Circuits Conference, 2000. ESS-CIRC '00. Proceeding of the 26rd European*, pp. 77–80, 2000.

[15] H. Hashemi, and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory design, and application", *IEEE Trans. On microwave Theory and techniques*, vol. 50, no. 1, Jan. 2002, pp. 228–301.

[16] J.-C. Rudell, J.-J. Ou, T.-B. Cho, G. Chien, F. Brianti, J.-A. Weldon and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications", *IEEE J. of Solid-State Circuits*, vol. 32, no. 12, Dec. 1997, pp. 2071–2088.

[17] D.-K. Shaeffer and T. H. Lee, "A 1.5-GHz CMOS low noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, May 1997, pp. 745–759.

[18] D. H and T. H. Lee, "Corrections to A 1.5-V, 1.5-GHz CMOS low noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 40, no. 6, June 2005, pp. 1397–1398.

[19] -, "Corrections to A 1.5-V, 1.5-GHz CMOS low noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 41, no. 10, Oct. 2006, p. 2359.

[20] P. Andreani and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier", *IEEE Trans. on Circuits and systems - II: Analog and Digital Signal Processing*, vol. 48, no. 9, Sept. 2001, pp. 835–841.

[21] L. Belostotski and J. W. Haslett "Noise figure optimization of inductively degenerated CMOS LNAs with integrated gate inductors", *IEEE Trans. on Circuits and systems*, vol. 53, no. 7, July 2006, pp. 1409–1422.

[22] B. Razavi, *RF Microelectronics*, Pearson-Prentice Hall, 1998.

[23] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, and K. A. I. Halonen, "A 2-GHz wide-band direct conversion receiver for WCDMA applications", *IEEE J. of Solid-State Circuits*, vol. 34, no. 12, Dec. 1999, pp. 1893–1903.

[24] F. S. Lee and A. P. Chandrakasan, "A BICMOS ultra-wideband 3.1-10.6-GHz front-end", *IEEE J. of Solid-State Circuits*, vol. 41, no. 8, Aug. 2006, pp. 1784–1791.

[25] D. M. Pozar, *Microwave Engineering*, New York: John Wiley & Sons, 2005.

[26] C. Tinella and J. M. fournier, "Design of a SOI fully integrated 1V, 2.5 GHz front-end receiver", *IEEE International SOI Conference(SOI'01)*, Durango, CO, 1-4 Oct. 2001, pp. 139–140.

[27] F. Behbahani, J. C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, and A. A. Abidi, "A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-μm CMOS-Architecture and front-end", *IEEE J. of Solid-State Circuits*, vol. 35, no. 12, Dec. 2000, pp. 1908–1916.

[28] R. Fujimoto, K. Kojima, and S. Otaka, "A 7-GHz 1.8-dB NF CMOS low-noise amplifier", *IEEE J. of Solid-State Circuits*, vol. 37, no. 7, July 2002, pp. 852–856.

[29] X. Fan, H. Zhang, E. Snchez-Sinencio, "A noise reduction and linearity improvement technique for a differential cascode LNA", *IEEE J. of Solid-State Circuits*, vol. 43, no. 3, Mar. 2008, pp. 588–599.

[30] W. Redman-White and D. M. W. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers", *European Solid-state circuits conference(ESSCIRC'01)*, pp. 68–71, Villach Austria, 18-20 Sept. 2001.

[31] S. Chehrazi, R. Bagheri, and A. A. Abidi, "noise in passive FET mixers: A simple physical model", *IEEE Custom Integrated Circuits Conference (CICC'04)*, pp. 375–378, Orlando, FL, 3-6 Oct. 2004.

[32] S. Mahdavi, and A. A. Abidi, "Fully integrated 2.2-mW CMOS front end for a 900-MHz wireless receiver", *IEEE J. of Solid-State Circuits*, vol. 37, no. 5, May 2002, pp. 662–669.

[33] Y. Feng, G. Takemura, S. Kawaguchi, P. Kinget, Y. Feng, G. Takemura, S. Kawaguchi, P. Kinget, "Design of a high performance 2-GHz direct-conversion front-end with a single-ended RF input in 0.13 μm CMOS", *IEEE J. of Solid-State Circuits*, vol. 44, no. 5, May 2009, pp. 1380–1390.

[34] V. kopta, D. Barras, C.-C. Enz, "An Approximate Zero IF FM-UWB Receiver for High Density Wireless Sensor Networks", *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, Feb. 2017, pp. 374–385.

[35] K. Kivekas, A. Parssinen, and K. A. I. Halonen, "Characterization of IIP2 and dc offsets in transconductance mixers", *IEEE Trans. on Circuits and System-II: Anolog and Digital Signal Processing*, vol. 48, no. 11, Nov. 2001, pp. 1461–1473.

[36] R. Bagheri, A. Mirzaei, S. Chehrrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang and A. A. Abidi, "An 800-MHz-6-GHz software-defined wireless receiver in 90nm CMOS", *IEEE J. of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006, pp. 2860–2876.

[37] A. A. Abidi,G. J. Pottie, and W. J. Kaiser, "Power-conscious design of wireless circuits and systems," *Proceeding of the IEEE*, vol. 8, no. 10, Oct. 2000, pp. 1528–1545.

[38] B. gilbert, "A precise quadrant multiplier with subnanosecond response", *IEEE J. of Solid-State Circuits*, vol. SC-3, no. 4, Dec. 1968, pp. 365–373.

[39] J. Ryynanen, K. Kivekas, J. Jussila, L. Sumanen, A. Parssinen, and K. Halonen, "Single-chip multi-mode receiver for GSM900, DCS1800, PCS1900, and WCDMA", *IEEE J. of Solid-State Circuits*, vol. 38, no. 4, April 2003, pp. 594–602.

[40] S. Wu, and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications", *IEEE J. of Solid-State Circuits*, vol. 33, no. 12, Dec. 1998, pp. 2178–2185.

[41] Y-S. Hwang, S-F. Wang and I-J. Chen, "A differential multi-band CMOS low noise LNA+mixer", *IEEE Microwave Wireless Comon Lett*, vol. 19, no. 11 2009, pp. 755–757.

[42] C. Bryant and H. Sjoland, "A 2.45GHz ultra-low power quadrature front-end in 65nm CMOS", *RFIC Symp. Dig*, 2012, pp. 247–250.

[43] C. Lin and T. S. Kalkur. " A 2.4GHz Common-Gate LNA Using on-Chip Differential Inductors in a $0.18\hat{\text{I}}\frac{1}{4}$m CMOS Technology", *Electrical, Communications and Computers*, 2009. pp. 183–188.

[44] C. Choi, J. Choi and I. Nam,. " A low noise and highly linear 2.4-GHz RF front-end circuit for wireless sensor networks", *IEEE 9th International Conference on ASIC (ASICON)*, 2011.

[45] T. Taris, J. B. Begueret and Y. Deval.. "A 60 μW LNA for 2.4 GHz wireless sensors network applications", *in RFIC*, pp. 1–4, 2011.

[46] A. Hastings, *The Art of Analog Layout*, NJ, Englewood Cliffs: Prentice-Hall, 2001.