Available online at www.sciencedirect.com

ScienceDirect

Energy Procedia 124 (2017) 577–583

Energy Procedia

www.elsevier.com/locate/procedia

7th International Conference on Silicon Photovoltaics, SiliconPV 2017

Fabrication of Si tunnel diodes for c-Si based tandem solar cells using proximity rapid thermal diffusion

Alain Fave[a], Jean-François Lelièvre[b], Thibaut Gallet[a], Qiaoyu Su[a], Mustapha Lemiti[a]

[a] *Institut des Nanotechnologies de Lyon-INL, UMR CNRS 5270, INSA de Lyon, 7 av. Capelle, Villeurbanne 69621, France*
[b] *Procédés, Matériaux et Energie Solaire, PROMES - UPR CNRS 8521, Rambla de la Thermodynamique – Tecnosud, Perpignan 66100, France*

Abstract

Increasing competitiveness of photovoltaic (PV) devices is currently an important objective in technological research, especially with the development of tandem solar cells based on c-Si as the bottom cell. For a monolithical structure, a tunnel diode in between the top and bottom cells is necessary.
In this work we report on the development of the fabrication of Si tunnel junction using a combination of spin-on doping and proximity rapid thermal diffusion. A desirable attribute of this process is simplicity. Two different structures p^{++}/n^{++} or n^{++}/p^{++} were fabricated on (100) Si substrates. Carrier density profiles were measured by ECV to characterize the shallow doping profiles. Vertical tunnel diodes were fabricated and I(V) characteristics are presented. It is shown that device peak current densities up to 270 A/cm² are achieved using this technique, which is the best value reported with such simple technique.

Peer review by the scientific conference committee of SiliconPV 2017 under responsibility of PSE AG.

Keywords: tandem solar cell; silicon tunnel junction; proximity rapid thermal diffusion

1. Introduction

In the past 15 years, the photovoltaic (PV) industry has drastically reduced the fabrication cost of silicon solar cell modules reaching a very low 0.37US$/$W_p$ in 2016 [1]. It means that further cost reduction of PV modules mainly relies on better cell efficiency at low cost. However, the record efficiency of crystalline silicon (c-Si) single junction solar cell (26.3% [2]) is approaching the 29.4% maximum limit which is due to different physical loss mechanisms. Thermalization losses are reduced in multijunctions structures, which are fabricated using a combination of III-V alloys as upper cells and Ge substrate as bottom cell [3-4]. However, the use of expensive Ge substrates or wafer bonding techniques still restricts them to niche applications under concentration or in space. An obvious way to reduce the cost is to use Silicon substrates to realize the lower cell, which also brings the advantage of a well-

1876-6102
Peer review by the scientific conference committee of SiliconPV 2017 under responsibility of PSE AG.
10.1016/j.egypro.2017.09.281

established industry. To create a tandem cell with Si as bottom cell, the top cell should have a bandgap of 1.7 eV and efficiencies up to 41.9% are theoretically achievable [5]. Recent research efforts have been devoted to this structure and several materials can be used to fabricate the top cell including III-V alloys [6], perovskite [7-8]. Even higher efficiencies may be obtained with 3 junctions but with more complex schemes [9]. There are 2 ways to implement a tandem Si solar cell:

- 4-terminal tandem solar cell allows optimizing each sub-cell separately [6] but may generate extra costs with more metallic contacts.

- 2-terminal tandem solar cell consists in a monolithic integration of the top structure by epitaxy (or deposition) or by transfer and bonding on silicon. It requires an electrical coupling between the 2 sub-cells without preventing transmission of infrared light to the Silicon bottom sub-cell. Transparent conductive oxide (TCO) is an option [10] but suffers from parasitic absorption and limits the temperature of the subsequent process (elaboration of the top cell).

In this context, the contact between the two sub-cells is a key element of a monolithic 2-terminal tandem solar cell. A transparent conductive oxide (TCO) will limit the temperature process for the fabrication of the top cell. An alternative is a c-Si Esaki tunnel junction consisting of two highly doped and very thin n-type and p-type regions implemented on top of the Si bottom cell. In such a diode, the electrons move from the degenerated n-type region to the degenerated p-type region via tunneling process, enabling electrical coupling with minimal parasitic absorption. Molecular beam epitaxy (MBE) is an evident solution and already led to very efficient tunnel diode but its high cost is a serious bottleneck for PV applications [11-12]. We can also mention a PECVD doped a-Si deposition followed by recrystallization [8]. In this work we focus on a low-cost technique combining spin-on dopant (SOD) sources and rapid thermal annealing (RTA) to realize 2 successive diffusion of p and n type (or vice versa). Such technique is well adapted for the PV industry which widely uses belt furnace industrial processing. The main difficulty is to achieve very high doping concentrations with very sharp doping transitions considering the compensation of the two dopants inherent to this method. This explained the few works combining Si bottom cell with a tunnel diode realized by rapid thermal diffusion (RTD) [13-14].

In this paper we demonstrate, with a simple elaboration technique, the possibility to use either n^{++}/p^{++} or p^{++}/n^{++} c-Si tunnel diodes to give the path to select later either n- or p-type absorber (III-V or perovskite) for the top cell (Fig. 1).

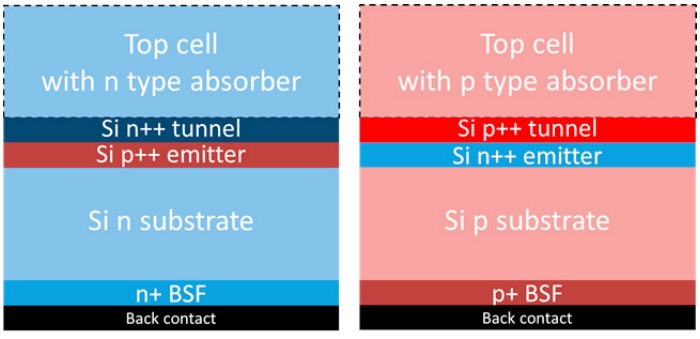

Fig. 1. Schematic of Si solar cell with integrated Si tunnel junction for tandem structure with a n-type absorber (left) or p-type absorber. Note that the top cell is not implemented in this work.

2. Proximity rapid thermal diffusion

2.1. Experiments

Rapid thermal annealing (RTA) is an established technique for ultra shallow junction fabrication. It can be combined with ion implantation, spin-on dopants (SOD), doped polysilicon, CVD deposited oxides, or planar solid sources [15]. We decided to combine SOD and RTA for their low thermal budget and their simplicity. Spin-on dopant can be deposited directly on silicon; however, especially in boron case, it can generate a residue layer of Boron Silicide at the wafer surface, which is difficult to etch as it is insoluble in HF. To avoid this problem, proximity rapid thermal diffusion (P-RTD) is an interesting technique [16]. The SOD is deposited on a Si wafer to be used as dopant source. This dopant source wafer is stacked in proximity to the Si target wafer separated by 300µm thick Si spacers, as shown on fig. 2. When heating in a N_2 ambient, the dopants go across the short space from the source wafer to the target wafer then diffuse through the silicon. This method allows also a better control of the junction depth.

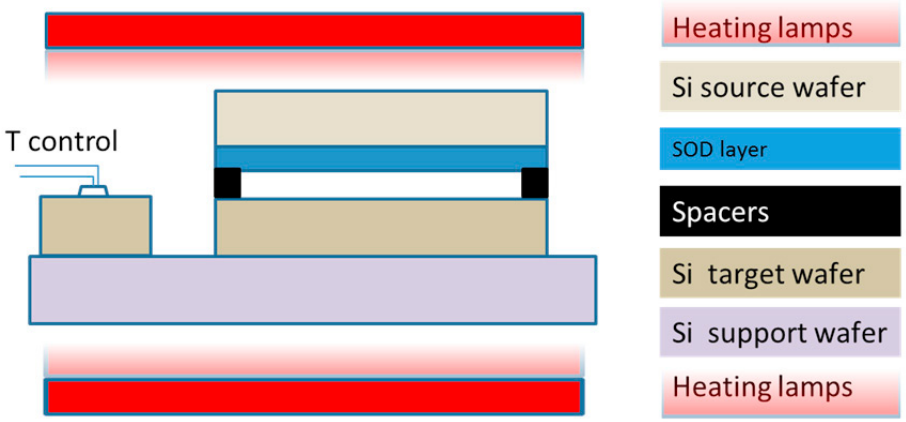

Fig. 2. Experimental set-up of the P-RTD

Source wafers were cleaned using 5% HF followed by a 15 min H_2SO_4/H_2O_2 solution to form a chemical oxide on the Si surface to improve the stability of the SOD which is deposited in the next step. Emulsitone Phosphorosilicafilm and Borofilm 100 were used as SOD sources for the n^{++} and p^{++} layers, respectively. The SOD is spun onto the source wafers at 3000 rpm during 30 s. The wafers were then baked at 200°C in air during 10 min. The P-RTD was performed under N_2 gas flow at atmospheric pressure in a ADDAX RTA furnace. The temperature peak was in the 900-1000°C range with a 50-100°C/s heating ramp.

2.2. Realization of the highly doped regions and characterization of free carrier density by ECV

The diffusion relies heavily on the temperature and the time of diffusion the wafer is undergoing at the peak temperature. If the temperature is too high or the time is too long, the concentration profile runs the risk of not being abrupt, therefore not leading to a shallow junction. If the temperature is too low, the concentration of dopants might not be high enough to have a good tunnel junction. Also, when combining two successive diffusions, the second dopant has to compensate the first one near the surface.

We measured the resulting doping profiles in the Si wafers by means of electrochemical capacitance-voltage (ECV - WEP-CVP21). Unlike SIMS measurements which give total concentration, the ECV profile represents the concentration of only electrically active dopants within Si and thus gives an accurate measurement of the junction depth [17-18]. During measurements, Si is slowly etched with a standard 0.1M Ammonium Bifluoride solution.

- n^{++}/p^{++} tunnel junctions on p^{+} (100) substrates

The first diffusion of boron was carried out at T = 980°C during 1 s with a heating rate of 90°C.s^{-1}. After this process, the sample was carefully cleaned using standard HF-H_2SO_4/H_2O-HF solutions in order to remove native oxide and contamination on the Si surface. During this step the first atomic layers of the Si substrate are removed. Phosphorus is then diffused at T= 950°C during 1 s with a heating rate of 79°C.s^{-1}.

The ECV profile (Fig. 3, a) shows that both n- and p- type regions are degenerated with active dopant concentrations above 10^{20} cm^{-3}, the concentration of phosphorus being 1.5 10^{20} cm^{-3} and that of boron being about 2 10^{20} cm^{-3}. Besides, the n-type region is very shallow (14nm) and a depletion region of only 3.4 nm is expected. This is suitable to form a high-quality tunnel junction.

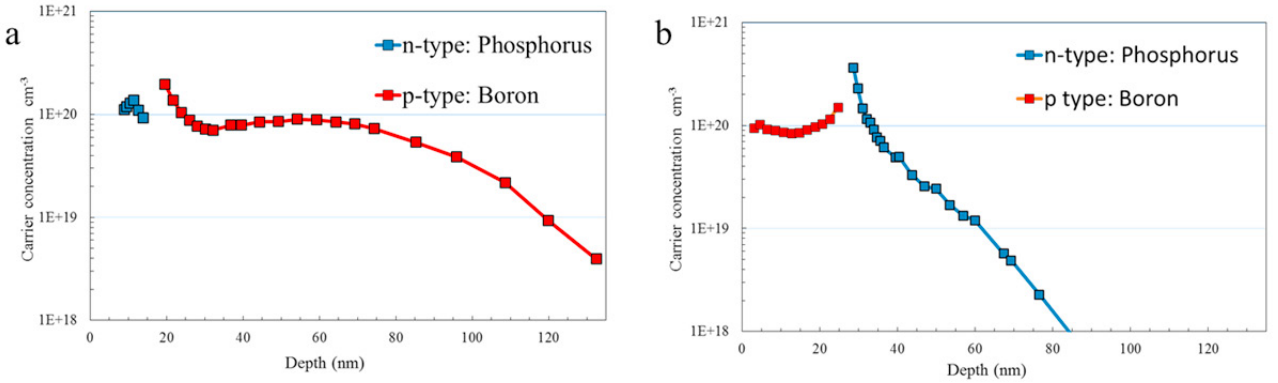

Fig. 3. ECV free carrier concentration versus depth (nm) for the 2 structures: (a) n^{++}/p^{++} ; and (b) p^{++}/n^{++}

- p^{++}/n^{++} tunnel junctions on n^{+} (100) substrates

The phosphorus diffusion was carried out at T = 980°C during 1 s with a heating rate of 90°C.s^{-1}. After this process, the sample was carefully cleaned using standard HF-H_2SO_4/H_2O-HF solution. For Boron diffusion, a 2 steps process with 2 successive P-RTD was applied, with a standard cleaning step in between. The first one is realized at 980°C (1s with a 65°C.s^{-1} heating ramp); the second one at 900°C (1s with a 65°C.s^{-1} heating ramp). With a single boron diffusion step, it was not possible to overpass the initial n-type level. Actually, as the boron solubility in Si is lower than that of phosphorus [19], after the first boron diffusion, there is a compensation of boron by phosphorus atoms and no p-type can be detected by ECV. One can note that finally, if the resulting carrier concentration is also higher than 10^{20} cm^{-3} for p- and n-type region, the p-type region is deeper than desired, with a 27 nm depth (Fig. 3, b).

3. Tunnel diode characterization

3.1. Tunnel diode fabrication

In order to evaluate the quality and the efficiency of our tunnel junctions, we fabricated vertical tunnel diodes on highly doped wafers to limit the contribution of the substrate to the series resistance. The diodes were processed on 2” wafers using photolithography and electron gun evaporation of Ti/Pd/Ag/Al (50-50-200-200 nm) for n type Si and Al (300 nm) for p type Si. Reactive ion etching (RIE) in SF6 and Ar, 5-20 sccm, 15 mTorr, 60W was used to form the device mesa, approximately 600 nm deep, leading to a diode diameter of 200 µm. Further annealing of the front contacts was realized at 350°C under N_2 during 30 s. The back contact was obtained using eutectic InGa. These test structures are sketched in Fig. 4 (b) and 5 (b).

3.2. Tunnel diode I(V) characterization

The room temperature current-voltage I(V) characteristics were measured with a Keithley 4200 semiconductor parameters analyzer. Two important figures of merits are the peak current density (PCD) and the peak-to-valley current ratio (PVCR). Both should be as high as possible to correspond to an ultra-low resistive contact.

- n^{++}/p^{++} tunnel junction on p^{+} (100) substrate

Fig. 4 (a) shows several tunnel diodes I(V) characteristics from the same substrate which provided the best results. One can clearly see the tunnel diode behavior. The highest PCD obtained is 270 A.cm^{-2} (85 mA for 0.314mm²) for a peak voltage of 0.6 V, with a PVCR of 2.1. The corresponding series resistance is 2 10^{-3} Ω.cm^2. Higher PVCR of 4.3 are obtained but with a lower PCD. Nevertheless, the low series resistance is similar for all diodes. Note that the last annealing step (350°C) has a strong influence on these parameters. Without annealing, the PCD didn't exceed 180 A.cm^{-2}. And the I(V) profiles after the peak voltage were not as smooth with a lot of background noise, which point out that the contacts have to be improved.

However, the 270 A.cm^{-2} is one of the best PCD value reported for P-RTD tunnel diodes. Better values were only obtained by MBE growth [11] which is a too costly technique for PV applications.

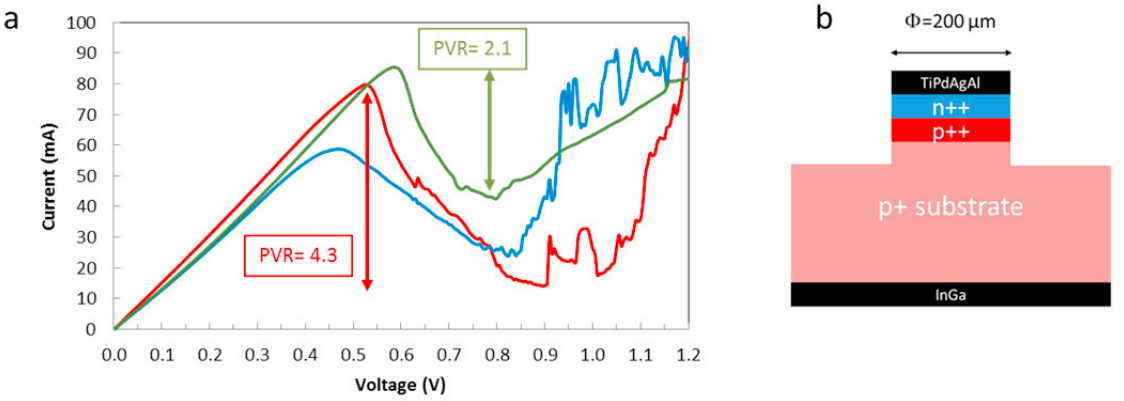

Fig. 4.(a) I(V) characteristics for n^{++}/p^{++} Si tunnel diodes on p^{+} (100) Si substrate at room temperature after a 30s annealing at 350°C. All the curves are from the same wafer; (b) scheme of the corresponding tunnel diode structure.

- p^{++}/n^{++} tunnel junctions on n^{+} (100) substrates

Fig. 5 (a) shows tunnel diodes I(V) characteristics of the p^{++}/n^{++} structure. It clearly shows that the tunnel behavior is not as marked as for the previous one. PCD of 150 A.cm^{-2} can be obtained but with a low PVR (~1.2). The resulting series resistance is also higher, between 3.4 10^{-3} and 8 10^{-3} Ω.cm^2. This is certainly related with the deeper boron diffused region (27 nm) we obtained (Fig.3 (b)). Actually, such p^{++}/n^{++} tunnel diode will be more challenging to implement, due to the lower solid solubility of B in Si which is about 4 times less than the one of P in Si [19].

The fabrication of such tunnel diodes should be followed by the deposition of the top cell structure. As perovskite is a very low temperature process, the doping profiles of the Si subcell will stay unchanged. When considering III-V monolithic integration, epitaxy temperature is in the 450-600°C range [20]. We tested shallow phosphorous and boron doped structures at 600°C during 30 min under ultra high vacuum. We didn't observe any modification of the

profiles except a slight decrease of phosphorous concentration near the surface probably due to exodiffusion. Nevertheless, this behavior can be taken into account by increasing slightly the temperature of phosphorus diffusion during tunnel junction fabrication.

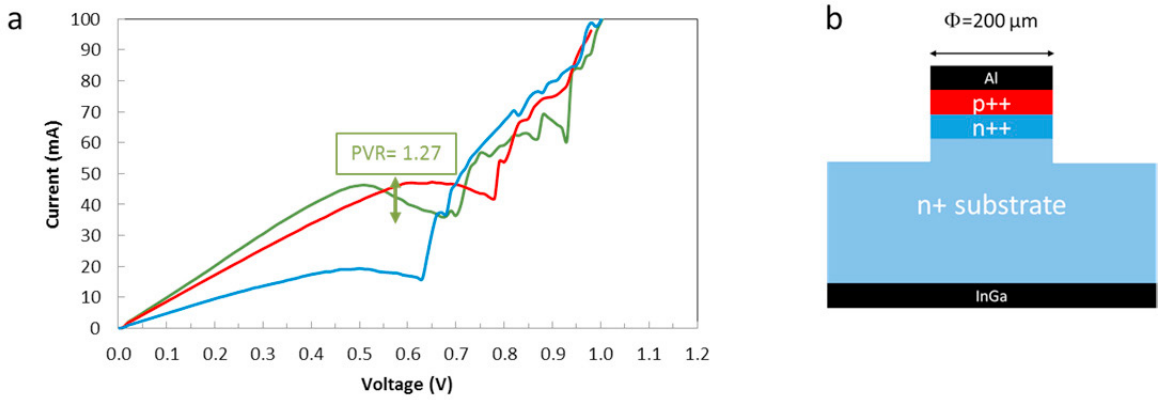

Fig. 5. (a) I(V) characteristics for p^{++}/n^{++} Si tunnel diodes on n^{+} (100) Si substrate after a 30s annealing at 350°C at room temperature. All the curves are from the same wafer; (b) scheme of the corresponding tunnel diode structure.

4. Conclusions

We successfully implemented a low thermal budget process to realize c-Si tunnel diodes using spin-on dopants and proximity rapid thermal diffusion. The control of the junction depth in the 10-20 nm range was realized by adjusting RTA temperature peak and heating ramp in the proximity configuration. Both n^{++}/p^{++} and p^{++}/n^{++} vertical tunnel diodes were fabricated, the last one showing a lower peak current density. Very high peak current densities were obtained, up to 270 $A.cm^{-2}$, with a peak-to-valley ratio in the 2.1-4.3 range. This record value for P-RTD is more than enough for standard tandem solar cell under 1 sun irradiation but also for high concentration applications. Further improvements can be achieved by a better control of the metallic contacts, an optimization of the temperature profile and by using dedicated furnaces for phosphorus and boron respectively. Nevertheless, these results demonstrate that high-quality Si tunnel diodes can be realized at low cost, which is a prerequesite for the development of competitive high efficiency c-Si based tandem solar cells.

Acknowledgements

We would like to thank Flore Boyer and Raj Kumar for their involvement in this project, the NANOLYON technological platform, especially Mr Khaled Ayadi, and Mr. Marco Vettori for MBE growth simulation. We are grateful to the French Agence Nationale de la Recherche for the financial support in the frame of the ANR projects NOVAGAINS, MENHIRS and HETONAN.

References

[1] ITRPV Working Group. (2016). International Technology Roadmap for Photovoltaic (ITRPV): 2016 Results.
[2] Green MA, Emery K, Hishikawa Y, Warta W, Dunlop ED, Levi DH, Ho-Baillie AWY, Solar cell efficiency tables (version 49), Progress in Photovoltaics: Research and Applications, 25, 2017; p 3–13
[3] Marti A and Araujo GL, “Limiting efficiencies for photovoltaic energy conversion in multigap systems,” Sol. Energy Mater. Sol. Cells, vol. 43, 1996, p. 203–222.
[4] Press release, Fraunhofer Institute for Solar Energy Systems, 1 December 2014 (accessed at http://www.ise. fraunhofer.de/en/press-and-media/press-releases/press-releases-2014/new-world-record-for-solar-cell-efficiency-at-46-percent on 7 December 2014).

[5] Connolly JP, Mencaraglia D, Renard C, Bouchier D, Designing III–V multijunction solar cells on silicon, Progress in Photovoltaics: Research and Applications, 22, 2014, p 810-820.
[6] Essig S, Steiner MA, Allebé C, Geisz JF, Paviet-Salomon B, Ward S, Descoeudres A, LaSalvia V, Barraud L, Badel N, Faes A, Levrat J, Despeisse M, Ballif C, Stradins P, Young DL, Realization of GaInP/Si dual junction solar cells with 29.8% 1-sun efficiency, IEEE Journal of Photovoltaics, 6 (4), 2016, p 1012–1019.
[7] Baillie CD, McGehee MD, High-efficiency tandem perovskite solar cells, MRS Bulletin, 40 (8), 2015, p 681-686.
[8] Mailoa, Jonathan P. et al. "A 2-Terminal Perovskite/silicon Multijunction Solar Cell Enabled by a Silicon Tunnel Junction." Applied Physics Letters 106.12 (2015)
[9] Cariou R, Benick, J, Beutel P, Razek N, Flötgen C, Hermle M, Lackner D, Glunz SW, Bett AW, Wimplinger M, Dimroth F, Monolithic 2-terminal III-V//Si triple junction solar cells with 30.2% efficiency under 1- sun AM1.5 g, IEEE Journal of Photovoltaics, 7 (1), 2017, p 367-373.
[10] Werner J, Wenig CH, Walter A, Fesquet L, Seif JP, De Wolf S, Niesen B, Ballif C, Efficient monolithic perovskite/silicon tandem solar cell with cell area >1 cm^2", Journal of Physical Chemistry Letters, 7 (1), 2016, p 161-166
[11] Oehme M, Hähnel D, Werner J, Kaschel M, Kirfel O, Kasper E, Schulze J, Si Esaki diodes with high peak to valley current ratios, Applied Physics Letters 95, 242109, 2009.
[12] Oehme M, Kirfel O, Werner J, Kaschel M, Kasper E, Schulze J, Antimony doped Si Esaki diodes without post growth annealing, Thin Solid Films 518, 2010, p S65–S67.
[13]Wang J, Wheeler D, Yan Y, Zhao J, Howard S, Seabaugh A, Silicon tunnel diodes formed by proximity rapid thermal annealing, IEEE Electron Device Letters, 24, 2, 2003, p 93-95.
[14] Yang J, Goguen J, KleimanR, Silicon solar cell with integrated tunnel junction for multijunction photovoltaic applications", IEEE Electron Device Letters, 33, 12, 2012, p1732-1734.
[15] Zagozdzon-Wosil W, Grabiec PB, Fabrication of submicron junctions - proximity rapid thermal diffusion of phosphorus, boron and arsenic, IEEE Transactions on Electron Devices, 41, 12, 1994, p 2281-2290.
[16] Nolan M, Perova T, Moore RA, Gamble HS, Boron diffusion from a spin-on source during rapid thermal Processing, Journal of Non-Crystalline Solids 254, 1999, p 89-93.
[17] Wu H, Ru G, Zhang Y, Jin C, Mizuno B, Jiang Y, Qu X, Li B, Electrochemical capacitance-voltage characterization of plasma-doped ultra-shallow junctions, Frontiers of Electrical and Electronic Engineering in China, 3(1), 2008, p 116–119.
[18] Bock R, Altermatt PP, Schmidt J, Accurate extraction of doping profiles from electrochemical capacitance voltage measurements, Proceedings of 23rd European Photovoltaic Solar Energy Conference, 1-5 September 2008, Valencia, Spain, p 1510-1513.
[19] Nobili D, Equilibrium carrier density and solubility of silicon dopants, in Semiconductor Silicon, 90, 1990, p 550-564.
[20] Da Silva M, Cornet C, Létoublon A, Levallois C, Rolland A, Even J, Pédesseau L, Wang YP, Wang S, Le Corre A, Boyer-Richard S, Rale P, Lombez L, Guillemoles JF, Mandorlo F, Lemiti M, Fave A, Ponchet A, Durand O, GaAsPN single and tandem solar cells on silicon, Montpellier, France, 18th International Conference on Molecular-Beam Epitaxy, 2016.