Handling of Unbalanced Faults in HVDC–Connected Wind Power Plants

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Abstract

High–voltage DC (HVDC) connections enable integration of wind power plants located very far from shore. The decoupled AC offshore grid comprises multiple wind turbine (WT) converters, and the voltage magnitude and frequency is primarily controlled by the offshore high–voltage DC voltage–source converter (VSC–HVDC). Faults in the offshore grid challenge the connected converters to provide an adequate response improving the overall fault behavior. Of special interest are asymmetrical faults due to the resulting unbalanced voltage conditions. This article addresses such conditions in the offshore grid and analyzes the impact on the offshore grid behavior for different converter contributions. Four fault ride–through strategies are studied for the WT converters. The effect of over–modulation of the converter voltages during such voltage conditions is highlighted. A test system is defined to analyze the fault and post–fault behavior. It is found that voltage support

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from the WT converters in both positive and negative sequence shows the best performance compared to controlled negative sequence current suppression. This scheme helps additionally the VSC–HVDC AC voltage control to return quickly to normal operation. To validate this statement simulations are performed for line–to–line (LL) and single line–to–ground (SLG) faults in immediate vicinity of the VSC–HVDC.
Keywords: Wind power plants, High voltage direct current (HVDC), Offshore grid control, Fault–ride through, Voltage–source converter

1. Introduction

Integration of renewable energy challenges current power systems in terms of reduced inertia, higher volatility, asymmetrical power flow and consequently a need for system reinforcement [1]. Offshore wind power plants (WPPs) usually require dedicated grid connections to connect to the main AC grids [2]. For very remote offshore WPPs, the high reactive power requirement due to the capacitance of submarine cables makes high–voltage AC (HVAC) unfeasible and motivates a high–voltage DC (HVDC) transmission. High–voltage DC voltage–source converter (VSC–HVDC) transmission with modular multi–level converters (MMCs) has been established as the state–of–the–art technology for such connections. It offers low transmission losses, small filter requirements resulting in less foot–print, black–start capability of the offshore grid and less raw material for the cables compared to AC [3]. In the future, interconnection between several HVDC connections might evolve into a meshed HVDC grid to integrate flawlessly offshore wind into the European grids [4, 5, 6].

In the usual configuration for this application the VSC–HVDC system is composed by two converter stations and a pair of DC submarine cables, the positive (pos.) and the negative (neg.) pole, respectively, resulting in a symmetrical monopole configuration. The offshore WPP is deployed as an AC system which is composed by the medium–voltage (MV) collection grid of e.g. 33 kV or 66 kV and the export grid at a higher voltage (e.g. 150 kV) [7]. WPP AC transformers boost the voltage between the collection and the export grid. The offshore VSC–HVDC sinks the generated power (active and reactive) of the WPPs through continuous control of voltage magnitude and system frequency of the offshore AC system, referred as controlled–frequency voltage–source converter (VSC) system [8]. The onshore VSC–HVDC controls the power flow over the DC link through DC voltage control and interfaces the main AC grid. The wind turbine (WT) converters, usually VSCs themselves, control their active and reactive power exchange with the offshore AC grid by means of current controllers and grid–synchronization through phase–locked loops (PLLs). Only power converters and no synchronous generators (SGs) are present in such a grid which challenges the traditional operation concepts. Specifically, there is a significant concern regarding the correct neg. sequence (seq.) behavior in VSC–HVDC–operated offshore AC grids from the WT converters and the VSC–HVDC [9].

In the literature, neg. seq. handling by WT converters is treated in [10, 11, 12, 13, 14, 15, 16, 17, 18] and in the light of VSC–HVDC–interfaced AC grids in [19, 20, 21, 22]. Converter control regarding neg. seq. is proposed and analyzed in [11, 17], focusing proportional–integral (PI) control in the synchronous reference frame and proportional–resonant (PR) control

in the stationary reference frame, as well as for MMCs in [23]. Ref. [14] highlights the importance of the neg. seq. voltage phase angle estimation and the impact of over–modulation (OM) limitation. The converter current references during unbalanced (or asymmetrical) faults are either focusing to improve the quality of the power exchange (avoid DC link ripple and constant active power injection) in [11, 13, 24] or to support the grid (voltage support) in [10, 12]. From a power system point of view, it was shown that such voltage support is beneficial for grids with many converter–connected generation and few conventional synchronous generators [10, 18]. Ref. [18] further highlights the impact of pos. and neg. seq. support by WTs and concludes that this approach might be considered in future grid codes (GCs). The studies regarding grid support are focused on AC grids without presence of VSC–HVDC (e.g. [11, 10, 18]) or interaction between the onshore VSC–HVDC and the main grid [12, 22]. In [12], unbalanced faults in the onshore grid were investigated and a injection of neg. seq. currents by the VSC–HVDC was seen as beneficial for the protection system in comparison to suppression thereof. Ref. [22] covers the neg. seq. suppression capability of AC–connected WPPs stressing their importance in a power grid with increased share of power converters.

Faults in a VSC–HVDC–operated offshore grid were investigated in [20, 21, 19, 25, 26]. Ref. [20] focuses on correct protection and isolation without any neg. seq. control by the converters. Refs. [19, 21] use pos. and neg. seq. control and the current references strategy focuses constant active power injection and reduction of DC link oscillation rather than voltage support. Ref. [25] presents a transient control strategy to provide more re-

active power during asymmetrical faults but lacks of a clear explanation of the offshore VSC–HVDC control. Moreover, it uses a PLL system which is not necessary in the real application [9]. Ref. [26] proposes a controlled AC voltage drop imposed by the offshore VSC–HVDC to activate a positive–sequence–voltage–drop–dependent active power reduction from the offshore WPP during onshore faults. Hence, onshore unbalanced faults might be ride through with a larger reactive current provision for grid support.

This paper investigates unbalanced faults of VSC–HVDC–operated offshore grids. Being pure power converter–based grids the fault ride through (FRT) response of each converter defines the dynamic behavior during such conditions. Four FRT strategies of the WT converters are analyzed: an OM–dependent active power reduction scheme, two different pos. seq. support scheme, respectively, and a pos. and neg. seq. voltage support scheme. Simulations are performed for a test system comprising three WPPs. The impact on the grid–forming VSC–HVDC, represented by the upper level controls and a regulated voltage source, as well as on the offshore grid system are emphasized. The consequences of harmonic oscillations due to OM are addressed as well as the fault and post–fault behavior of the system.

The paper is organized as follows: Section 2 highlights the system and controller configurations as well as the current reference calculation strategies under consideration. The parameters of the test system are given in Section 3. Section 4 presents the simulation results of two asymmetrical faults applied at the point of common coupling (PCC). Section 5 discusses the simulation results and its implication in the offshore grid operation. Finally, Section 6 concludes the research and highlights further work.

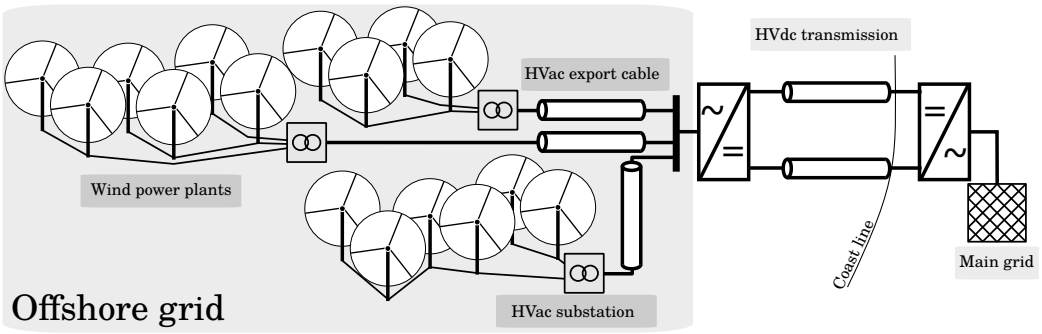


Figure 1: Common scheme of HVDC–connected WPPs.

2. System and controller structure

Multiple WPPs might be connected through an HVDC transmission link as shown in Fig. 1. The offshore grid is composed by passive components, such as transformers, cables and their shunt compensations, and the power converters interfacing the grid.

The nomenclature and matrices for Park, Clarke and Fortescue transformation used in this paper are outlined in the Appendix A.

2.1. WT converter control

The currents injected by the WT converters are classically controlled through PI controllers in the synchronous reference frame with dq–components. The system equations for the pos. and neg. seq. components of a VSC coupled through an inductive filter L with a parasitic resistance R to the grid

are shown in (1) and (2):

$$\begin{bmatrix} u^c_{1\mathrm{d}} \\ u^c_{1\mathrm{q}} \end{bmatrix} = \begin{bmatrix} u^g_{1\mathrm{d}} \\ u^g_{1\mathrm{q}} \end{bmatrix} - \begin{bmatrix} R & -\omega L \\ \omega L & R \end{bmatrix} \begin{bmatrix} i_{1\mathrm{d}} \\ i_{1\mathrm{q}} \end{bmatrix} - L\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{1\mathrm{d}} \\ i_{1\mathrm{q}} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} u^c_{2\mathrm{d}} \\ u^c_{2\mathrm{q}} \end{bmatrix} = \begin{bmatrix} u^g_{2\mathrm{d}} \\ u^g_{2\mathrm{q}} \end{bmatrix} - \begin{bmatrix} R & \omega L \\ -\omega L & R \end{bmatrix} \begin{bmatrix} i_{2\mathrm{d}} \\ i_{2\mathrm{q}} \end{bmatrix} - L\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{2\mathrm{d}} \\ i_{2\mathrm{q}} \end{bmatrix} \tag{2}$$

Where ω is the pos. seq. angular frequency. The subscripts 1 and 2 denote pos. and neg. seq. components, respectively. The superscript g defines a grid variable, whereas c stands for converter.

2.1.1. Grid synchronization

To control its phase current injection $\mathbf{i} = [i_a, i_b, i_c]^\top$ into the three–phase system the VSC synchronizes to the grid voltage. The voltage measurement might be passed through a PLL which locks to the phase angle of both pos. and neg. seq. components (magnitudes $|\mathbf{u^g_1}|$, $|\mathbf{u^g_2}|$ and phase angles θ^g_1, θ^g_2, respectively). In [11] a thorough analysis on PLLs is given concluding that for controllers in the synchronous reference frame (dq–components) the double decoupled synchronous reference frame PLL (DDSRF–PLL) provides a fast and accurate response during balanced and unbalanced grid conditions. The neg. seq. phase angle is aligned to the respective voltage vector which is challenging for very low magnitudes [14]. Therefore, for a magnitude smaller than 0.05 per unit (p.u.) the neg. seq. phase angle is set to $\theta^g_2 = -\theta^g_1$; otherwise the neg. seq. phase angle is locked by the mentioned PLL. A hysteresis control avoids toggling for the neg. seq. phase angle (upper boundary at 0.2 p.u.). The implementation of the DDSRF–PLL and the described modification for low neg. seq. magnitudes is sketched in Fig. 2. The nominal

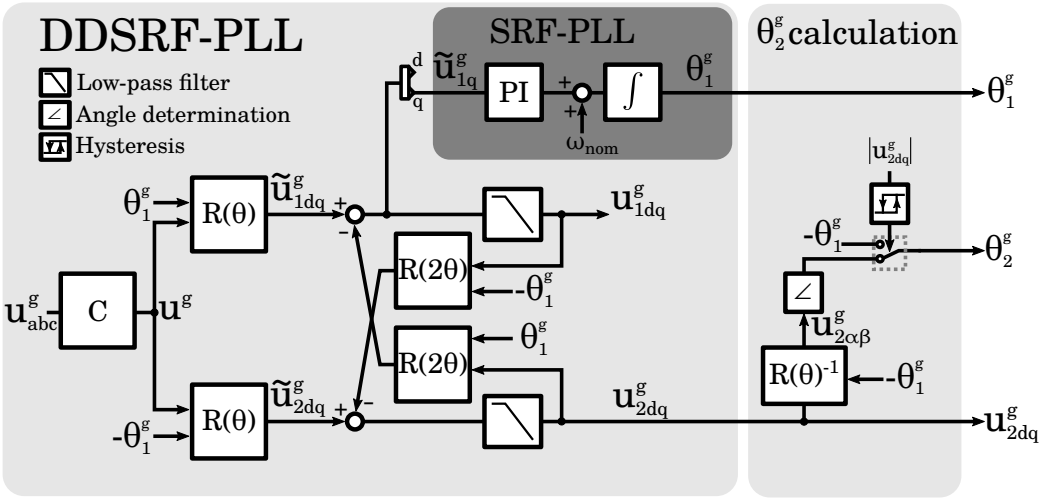


Figure 2: DDSRF–PLL implementation and neg. seq. phase angle determination. **C** is the Clarke–transformation, whereas $\mathbf{R}(\theta)$ rotates the input vector by θ. Both transformation matrices are described in the Appendix A.

frequency $f_{\text{nom}} = 50\,\text{Hz}$ is fed–forward through the angular frequency of $\omega_{\text{nom}} = 2\pi f_{\text{nom}}$ in the PLL.

2.1.2. Positive and negative sequence current control

The coupling between the sequences pronounces double fundamental frequency components. The main challenge is to filter these components for the current control avoiding the introduction of significant delays which might harm the controller performance. It is well known that the neg. seq. components appear as double fundamental frequency components in the pos. seq.

components and vice–versa [11]:

$$\mathbf{i_1} = \begin{bmatrix} i_{1\mathrm{d}} \\ i_{1\mathrm{q}} \end{bmatrix} = |\mathbf{i_1}| \begin{bmatrix} \cos(\phi_1) \\ \sin(\phi_1) \end{bmatrix} + |\mathbf{i_2}| \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\phi_2) \\ \sin(\phi_2) \end{bmatrix} \quad (3)$$

$$\mathbf{i_2} = \begin{bmatrix} i_{2\mathrm{d}} \\ i_{2\mathrm{q}} \end{bmatrix} = |\mathbf{i_2}| \begin{bmatrix} \cos(\phi_2) \\ \sin(\phi_2) \end{bmatrix} + |\mathbf{i_1}| \begin{bmatrix} \cos(2\omega t) & -\sin(2\omega t) \\ \sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos(\phi_1) \\ \sin(\phi_1) \end{bmatrix} \quad (4)$$

Where ϕ_1 and ϕ_2 are the pos. and neg. seq. angles, respectively.

Similarly to the decoupling principle in the DDSRF–PLL, the current controllers in the double synchronous reference frame aim to mitigate the double fundamental frequency terms through notch filtering, a decoupling network based on the measured signals, or a decoupling network based on the reference and error signals [11]. This work uses a decoupling network based on the reference and error signals for the WT converter current controllers, thus notch filtering is not required in the WT converter control. The seq. components of the grid voltage are fed–forward through a low–pass filter with a bandwidth of 40 rad/s to damp high–order oscillations.

2.1.3. Fault ride–through

Especially during fault events the correct tracking of the voltage magnitudes is of utmost importance to sense the voltage sag and trigger subsequent actions. One action might be dynamic voltage support as highlighted in the following.

Dynamic voltage support. Pos. seq. voltage support is demanded in most GCs [7, 27]. The principle demands converter–based generation (e.g. WTs) to support the grid voltage through reactive power injection. This might be

realized by injecting additional reactive current proportional to the respective voltage drop and is defined for pos. seq. in (5) and for neg. seq. in (6):

$$i_{1q} = k_1(|\mathbf{u}_{1,\text{pre-fault}}| - |\mathbf{u_1}|) \tag{5}$$

$$i_{2q} = k_2(|\mathbf{u}_{2,\text{pre-fault}}| - |\mathbf{u_2}|) \tag{6}$$

Where a pos. current flows from the grid to the converter. The pre–fault voltage $\mathbf{u}_{1,\text{pre-fault}}$ might be a one minute mean value prior to the fault. The proportional gain k_1 might take any pos. value, but the maximum additional reactive current is limited (to e.g. 1 p.u.).

A deadband for continuous operation voltages, e.g. 0.9 p.u. to 1.1 p.u., might avoid voltage support during normal steady–state conditions. In normal operation the grid voltages are balanced, thus the magnitude of the pre–fault neg. seq. voltage $|\mathbf{u}_{2,\text{pre-fault}}|$ is zero. During unbalanced voltage conditions, neg. seq. voltage arises and might be attenuated by dynamic voltage reduction by choosing $k_2 \neq 0$. The reduction of the neg. seq. voltage component leads to more balanced voltages. Ref. [27] demands such a scheme with default proportional gains $k_1 = k_2 = 2$ which will be used in the analysis. Furthermore, a voltage deadband of ± 0.1 p.u. in the neg. seq. controller is implemented to avoid neg. seq. current injection outside fault transients and/or under an erroneous phase angle as emphasized in [14] and Section 2.1.1.

Sag start and ending detection. To track the magnitudes of the three phase voltages, independent single–phase PLLs might be used. Nevertheless, the DDSRF–PLL is already implemented (see Section 2.1.1) for the phase angle tracking. In general, phase magnitudes $\mathbf{x} = [x_a, x_b, x_c]^\top$ can be calculated

from the seq. components $\mathbf{x_1}, \mathbf{x_2}$ and the respective angles ϕ_1, ϕ_2 through (7) to (9) using the inverse Clarke–transformation applied on the pos. and neg. seq. components in the stationary reference frame [28]:

$$|x_a| = \sqrt{|\mathbf{x_1}|^2 + |\mathbf{x_2}|^2 + 2|\mathbf{x_1}||\mathbf{x_2}| \cos \alpha} \tag{7}$$

$$|x_b| = \sqrt{|\mathbf{x_1}|^2 + |\mathbf{x_2}|^2 + 2|\mathbf{x_1}||\mathbf{x_2}| \cos \left(\alpha + \frac{4\pi}{3}\right)} \tag{8}$$

$$|x_c| = \sqrt{|\mathbf{x_1}|^2 + |\mathbf{x_2}|^2 + 2|\mathbf{x_1}||\mathbf{x_2}| \cos \left(\alpha - \frac{4\pi}{3}\right)} \tag{9}$$

Where α is defined by $\alpha = \phi_2 - \phi_1$. To calculate the phase voltage magnitudes $|\mathbf{u}|$, vector $\mathbf{x} = [x_a, x_b, x_c]^\top$ is replaced by $\mathbf{u} = [u_a, u_b, u_c]^\top$.

The full information of a sine wave is available in one quarter of a fundamental cycle. The waveforms change significantly at the respective start and end of a voltage event. The described time range of one quarter of a grid cycle is valid for the sensing of the fault start, whereas the end of the fault after isolation of the faulted system might be more challenging as the system is affected by the dynamics during the fault. The power converter controls might introduce a post–fault transient although the fault is physically cleared from the system. The use of the three to five grid cycles–long mean average filtered value of the measurement during the post–fault situation showed a good performance to avoid toggling of the sag detection signal.

Active power limitation and reduction. GCs, e.g. [27], might prioritize reactive currents during dynamic voltage support which could result active power limitation. Without immediate active power in–feed reduction by the WT, e.g. by torque or pitch control, an active power limitation of the grid–side

converter ultimately leads to a DC voltage increase. A dynamic braking resistor (DC chopper) in the DC link is a usual solution to dump the surplus energy. Contrary to active power limitation, active power reduction is referred to the desired operation of reducing active power fed to the grid (e.g. for the purpose of active power scheduling).

2.2. Offshore VSC–HVDC control

The offshore VSC–HVDC control is shown in Fig. 3. The measured grid voltage in the abc frame $u_{\mathrm{abc}}^{\mathrm{pcc}}$ is transformed into the synchronous reference frame through the decoupling network depicted in Fig. 4. The decoupling network cancels the double grid frequency oscillations on the signals similar to the DDSRF–PLL [11]. A PLL is not needed as the angular frequency is directly set through integration of ω_{nom} as depicted on the right hand side of Fig. 4.

A load–independent control strategy based on vector control in both sequences is implemented as described in [8] for the pos. seq. control. Refs. [9, 29, 30] mention a different control strategy based on direct control of the AC voltage. The lack of a dedicated fast current controller is compensated by limiting the voltage drop over the converter impedance to e.g. 0.1 p.u. [9]. This scheme provides only an indirect limitation of the converter current through voltage limitation. Ref. [29] considers this as a drawback during fault events. As a consequence the converter currents might exceed the limits [29]. Therefore, the vector control–based scheme is used in pos. and neg. seq.. The decoupling terms for the voltage controller use the impedance of the converter capacitor installed at the terminals. The setup considers a physical shunt capacitor to control the voltage independently from possible

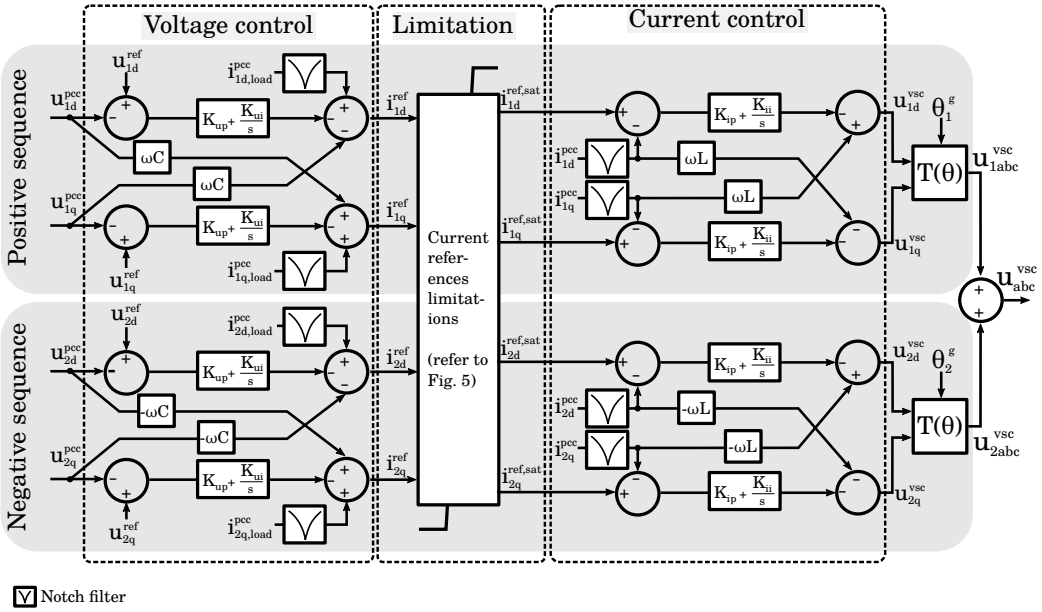


Figure 3: VSC–HVDC overall control scheme including voltage control, current control, and current references limitation in pos. and neg. seq..

offshore grid operations [31]. This allows to use the beneficial feed–forward of the load current in the voltage control [30]. The effective capacitance of the offshore grid in combination with gain scheduling might allow its avoidance [29] but is outside the scope of this study.

The current control is designed with notch–filter–based controllers (tuned to $f = 100\,\mathrm{Hz}$, damping factor $\zeta = 0.5$) to cancel out the double fundamental frequency terms. The notch filters are applied to the current measurements, whereas the voltage measurements are passed through the DDSRF–PLL. In case of an MMC, the effective coupling inductance L might be the converter arm and converter transformer windings, respectively.

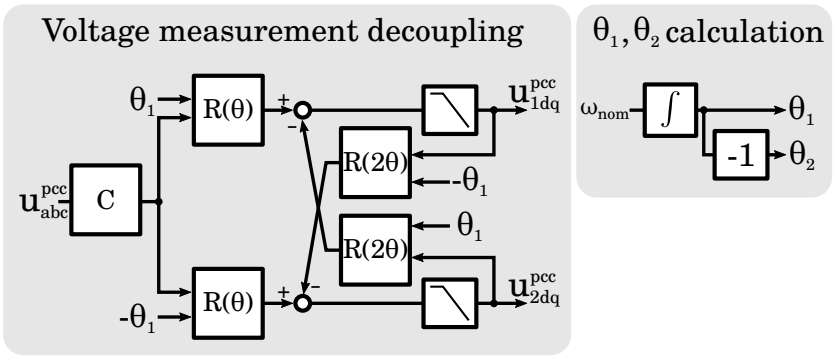


Figure 4: Voltage measurement decoupling and phase angle determination for the VSC–HVDC control.

2.2.1. Feed–forward implementation

The feed–forward scheme in Fig. 3 avoids large deviation during set–point changes. In the voltage controller, the load current is directly fed–forward through 100 Hz–tuned notch filters (damping factor $\zeta = 0.5$) on the pos. and neg. seq. components. No feed–forward is established for the current controller. Alternatively, the reference voltage could be fed–forward to improve the response of the current control on reference voltage changes [30].

2.3. Limitations and over–modulation (OM)

Mainly the semiconductor devices in combination with the operation strategy define the maximum current and voltage capability of a converter. Hence, the controller design and used reference calculation (RC) has to prevent over–currents and voltages to avoid the activation of internal converter protection inherently resulting in a shut–down.

2.3.1. Maximum phase current

If the neg. seq. component is zero the maximum current $i_{\max}$ can be limited straightforwardly:

$$\sqrt{{i_{1d}}^2 + {i_{1q}}^2} \leq i_{\max} \tag{10}$$

In case of unbalanced conditions, the simplest limitation is made for the pos. and neg. seq. components:

$$|\mathbf{i_1}| + |\mathbf{i_2}| \leq i_{\max} \tag{11}$$

Eq. (11) might be too strict in dependence of the seq. angle difference. Therefore, the full converter capability might be reached by calculating the phase current magnitudes expressed by (7) to (9) under a variable substitution of $\mathbf{x}$ by $\mathbf{i}$ and $\alpha = \phi_2 - \phi_1$ [32]. The saturation gets active when (7) to (9) exceeds the maximum current $i_{\max}$. The implementation is depicted in the block diagram in Fig. 5. The limitation of the phase currents results to an equal and linear scaling for the dq–components in both sequences by $\max\{|i_a|, |i_b|, |i_c|\}$ when $\max\{|i_a|, |i_b|, |i_c|\} \geq i_{\max}$.

2.3.2. OM and total harmonic distortion

The maximum applied voltage at the AC terminals of VSCs $|\mathbf{u}_{\mathrm{abc}}^{\mathrm{vsc}}|$ is limited as shown by (12) [33]:

$$|\mathbf{u}_{\mathrm{abc}}^{\mathrm{vsc}}| \leq m\frac{u_{\mathrm{DC}}}{2} \tag{12}$$

Where m is the modulation index. The linear region is defined for $m \leq 1$, whereas for $m > 1$ the fundamental voltage does not increase linearly and OM occurs. Third harmonic injection allows an increase of the modulation index

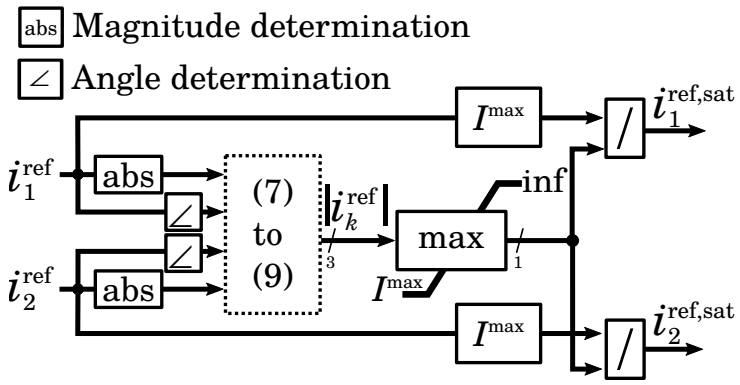


Figure 5: Current references saturation scheme based on sequence components. The current references are limited when the highest phase magnitude exceeds the maximum current.

barrier m_{bar} to $\frac{2}{\sqrt{3}} \approx 1.154$. An over–modulated applied voltage waveform contains harmonics of even order [33].

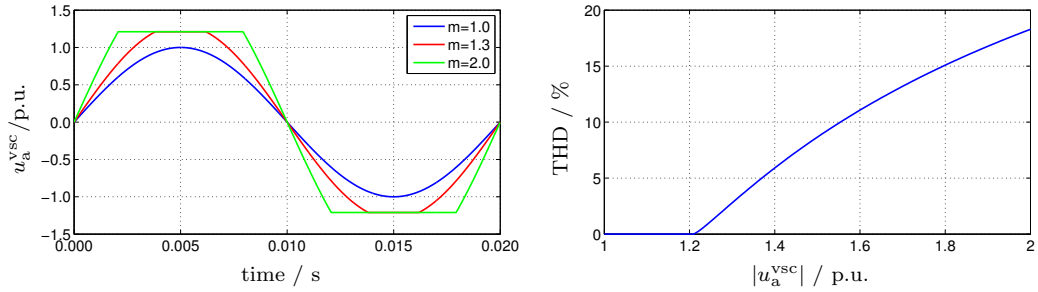
OM might also occur in an ideal MMC, whose basic equations relate converter AC, DC, and arm voltages by $u_c = \frac{u_{DC}}{2} - u_u = u_l - \frac{u_{DC}}{2}$ and $u_{DC} = u_l + u_u$ [3]. The upper and lower arm voltage are the sum of the inserted submodule voltages, $u_u = \sum u_u^{\text{SM}}$ and $u_l = \sum u_l^{\text{SM}}$, respectively. This implies that the DC voltage is defined by the voltages of the inserted sub–modules. Thus, AC voltage limitation as described in (12) might occur in an MMC similar to a conventional VSC.

The total harmonic distortion (THD) in % is defined for steady–state voltages and currents:

$$\text{THD} = \sqrt{\frac{1}{u_1^2} \sum_{n=2}^{N} u_{\text{n}}^2} \cdot 100 \tag{13}$$

Where u_{n} is the n–th harmonic voltage and N the highest order under consideration.

Fig. 6a shows the applied VSC phase voltage $u_{\mathrm{a}}^{\mathrm{vsc}}$ for $m = 1.0$, $m = 1.3$ and $m = 2.0$. Fig. 6b plots the evolution of the THD of over–modulated signals up to $m = 2$ (m_{bar} is set to 1.21 by extension of m through third harmonic injection and 5 % DC voltage increase). For $|u_{\mathrm{a}}^{\mathrm{vsc}}| \leq m_{\mathrm{bar}}$ the THD is zero, whereas larger values cause an over–modulated signal with non–zero THD values. The highest output voltage of the fundamental can be reached with a square–wave waveform leading to a magnitude of $4/\pi \approx 1.273$ [33]. Nevertheless, the converter currents are then uncontrolled.



(a) (b)

Figure 6: Characteristics of voltage limitation by converter OM on (a) applied voltage reference signals and (b) THD.

2.3.3. OM limitation

OM is undesired due to lost of controllability and waveform distortion. The avoidance of OM might be achieved through an appropriate converter design which allows an extensive continuous voltage range operation in the linear region. However, an over–specification of the converter voltage might increase the converter costs. To the authors' knowledge, the limitation of OM is not specified by actual GCs. Limited currents according to Section 2.3.1 do

not ensure that the applied voltages at the output of the current controllers are not affected by OM. Nevertheless, two possibilities arise to avoid/reduce OM in the given control scheme in symmetrical components: 1) limitation of the applied converter voltage seq. components $\mathbf{u}_1^{\mathbf{c}}$ and $\mathbf{u}_2^{\mathbf{c}}$ (post–controller) or 2) current reference reduction of $\mathbf{i}_1^{\mathrm{ref}}$ and $\mathbf{i}_2^{\mathrm{ref}}$ (pre–controller). It is obvious that the first option does not allow to track the original current references and leads to uncontrollability [according to (1) and (2)]. The second option reduces either the reactive or the active pos. seq. current reference to limit OM similar to [14]. As long as OM is detected, either the q– or the d–component of the current reference is reduced.

2.4. WT converter current references

Four WT converter current RCs are discussed in the following. Other strategies were disqualified prior to the study due to their poor performance, e.g. no voltage support without OM limitation or only pos. seq. control. Table 1 summarizes the characteristics of the selected strategies.

RC1 targets no voltage support and a pos. seq. reduction to limit OM. Hence, the converter avoids any additional reactive currents and OM limitation is active through reduction of pos. seq. d–axis component (active current). The short–term power reduction might be dissipated by the DC chopper. The neg. seq. current (both in d– and q–axis) is controlled to zero. **RC2** uses pos. seq. voltage support and controls the neg. seq. current to zero. Therefore, additional pos. seq. reactive current is applied according to (5). An OM limitation control is not applied. **RC3** uses pos. seq. voltage support such as RC2 but further applies OM limitation. The converter controls pos. and neg. seq., the latter to zero. OM limitation control is active

and reduces the dynamic voltage support up to zero in order to lower the magnitude of the applied voltage. Finally, **RC4** targets pos. and neg. seq. voltage support. The pos. and neg. seq. reactive current references, i_{1q} and i_{2q}, are altered by the additional references in (5) and (6), respectively. The objective is to reduce the voltage imbalance and simultaneously boost the pos. seq. voltage. OM limitation control is inactive for this strategy.

Table 1: Characteristics of current RCs.

RC	Pos. seq. ctrl	Neg. seq. ctrl	OM limitation
RC1	No support	Zero	Yes
RC2	Voltage support	Zero	No
RC3	Voltage support	Zero	Yes
RC4	Voltage support	Voltage support	No

3. Case study

The study is conducted in Matlab/Simscape Power Systems for an HVDC–connected offshore grid system of 1.2 GW as shown in Fig. 7. Three WPPs link under different distances to the VSC–HVDC station. WPP1 is rated to 498 MW in 25 km distance, WPP2 represents 450 MW in 15 km, and WPP3 injects 198 MW at full power, in a distance of 5 km. The WPPs are modeled with a respective aggregated WT converter average model (grid–side converter and wind–dependent power injection in the DC link), a lumped π–model of the collection grid cabling, the transformers, and the export cable system (distributed elements line model). The offshore VSC–HVDC station is modeled as a controlled three–phase voltage source with the control

scheme introduced in Section 2. The OM barriers are set to 1.21 for the WPP converters and to 1.3 for the offshore VSC–HVDC. The higher value for the VSC–HVDC was chosen to allow a increase the voltage margin of this grid–forming converter. Relevant system parameters are shown in Table 2 and further data is taken from [34].

Two temporary faults are considered for a duration of $t_\mathrm{f} = 250\,\mathrm{ms}$ each at fault location A (FA) which is the busbar to the cable connection of WPP1. A line–to–line (LL) fault with a fault resistance of $R_\mathrm{LL} = 2\,\mathrm{m\Omega}$ between phase a and b as well as a single line–to–ground (SLG) fault with a total fault resistance of $R_\mathrm{SLG} = 2\,\mathrm{m\Omega}$ between phase a and ground. Prior to the faults the system is operating at full power. A LL fault inside the export cable is not feasible due to the shielding around the conductors which is grounded on both sides [35].

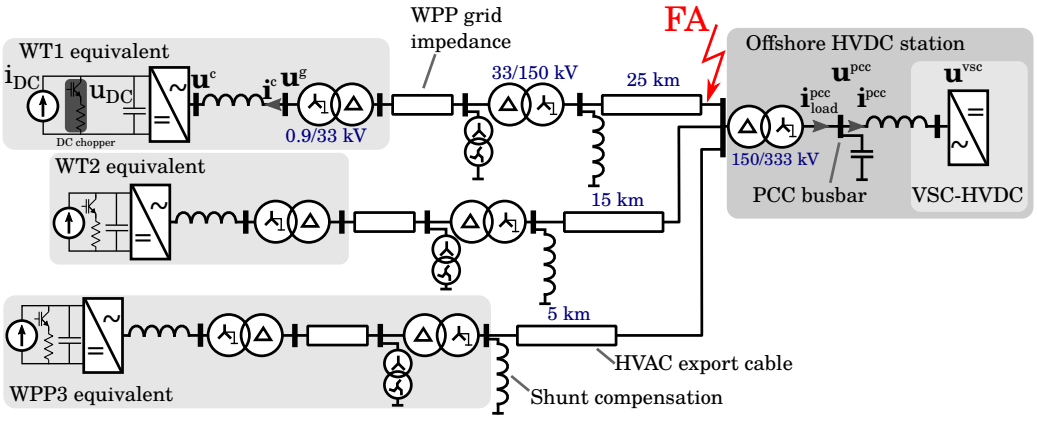


Figure 7: Electrical layout of the offshore grid system. The HVDC link to shore and onshore VSC–HVDC are neither shown nor modeled.

Table 2: Relevant parameters of the test system. Data partly extracted from [34, 36, 37]. Base power if stated $S_\mathrm{b} = 1000\,\mathrm{MVA}$, otherwise component power rating.

WPP and HVAC export grid	WPP1	WPP2	WPP3
Number of turbines	83	75	33
WT conv. rating (S/MVA, U_AC/kV)		6.7, 0.9	
OM limitation of $u_\mathrm{abc}^\mathrm{wpp}$ (m_bar/p.u.)		1.21	
WT conv. coupling impedance (z/p.u.)		$0.01 + \mathrm{j}0.05$	
WT transformer impedance (z/p.u.)		$0.01 + \mathrm{j}0.06$	
Collection grid voltage (U_AC/kV)		33	
Transformer impedance (z/p.u.)		$0.003 + \mathrm{j}0.15$	
WPP grid impedance (z/p.u.)[a]	$0.018 + \mathrm{j}0.035$	$0.014 + \mathrm{j}0.023$	$0.025 + \mathrm{j}0.041$
WPP grid shunt reactance (x/p.u.)[a]	0.011	0.009	0.003
Export grid voltage (U_AC/kV)		150	
Export cable compensation (Q_r/Mvar)	50.5	30.9	4.0
Export cables impedance (z/p.u.)[a]	$0.13 + \mathrm{j}0.40$	$0.08 + \mathrm{j}0.24$	$0.01 + \mathrm{j}0.03$
Export shunt reactance (x/p.u.)[a]	0.025	0.041	0.597
VSC–HVDC			
Rating (S/MVA, U_AC/kV, U_DC/kV)		1333.3, 320, ±320	
Transformer impedance (z/p.u.)		$0.003 + \mathrm{j}0.15$	
Coupling impedance (z/p.u.)		$0.010 + \mathrm{j}0.12$	
Shunt reactance (capacitance) (x/p.u.)		-10	
$u_\mathrm{ref,vsc}$ OM limitation (m_bar/p.u.)		1.3	
PI controllers			
WT conv. ($K_\mathrm{ip}, K_\mathrm{ii}$ / $\mathrm{V\,A^{-1}}$)		0.1, 3.3	
WT OM limitation ($K_\mathrm{OMp}, K_\mathrm{OMi}$)		2, 200	
VSC–HVDC VC ($K_\mathrm{up}, K_\mathrm{ui}$ / $\mathrm{A\,V^{-1}}$)		0.005, 1.34	
VSC–HVDC CC ($K_\mathrm{ip}, K_\mathrm{ii}$ / $\mathrm{V\,A^{-1}}$)		73.7, 1930.2	

[a] Base power S_b applies.

4. Results

The simulations were performed for the four RC strategies and the two different faults. Figs. 8 and 10 plot voltages and currents in the time window of interest (being around 100 ms before the fault inception and 350 ms after the fault end) for the LL and the SLG fault, respectively. Additionally, Figs. 9 and 11 depict detailed plots for the respective faults. The RC strategies are arranged column–wise, whereas each row shows a different variable.

First, the LL fault results are outlined Fig. 8. Row 1 shows the three–phase voltage profile at the PCC busbar (according to Fig. 7). The values are 1 p.u. during pre–fault conditions and return to this value after the fault. Due to the delta–star configuration of the converter transformer the PCC voltages have the shape of a SLG fault. The voltage magnitude differs: two phase voltages increase transiently up to 1.45 p.u. for RC2 and RC3, whereas it stays below 1.3 p.u. for RC1. The plot of strategy RC4 peaks below 1.3 p.u.. The post–fault recovery (starting from $t = 0.25$ s) indicates the fastest return to balanced voltages by RC1 and RC4 and slightly slower responses for RC2 and RC3. The applied voltages at the converter of WPP1 and the VSC–HVDC are illustrated in Row 2 and 3, respectively. These voltages are subject to their inherent converter limitations such as OM. The qualitative effect of OM might be analyzed by the zoomed plots in Fig. 9 (Row 1 and 2) detailing the shape of the applied voltage starting from $t = 200$ ms. For the WPP1 converter, OM occurs for RC2, RC3, and RC4, although the largest OM occurs for RC2 and RC3 (phase b and c are almost square waveforms). The VSC–HVDC is also subject to OM, especially for RC2, RC3, and RC4. No OM appears for RC1 (both converters).

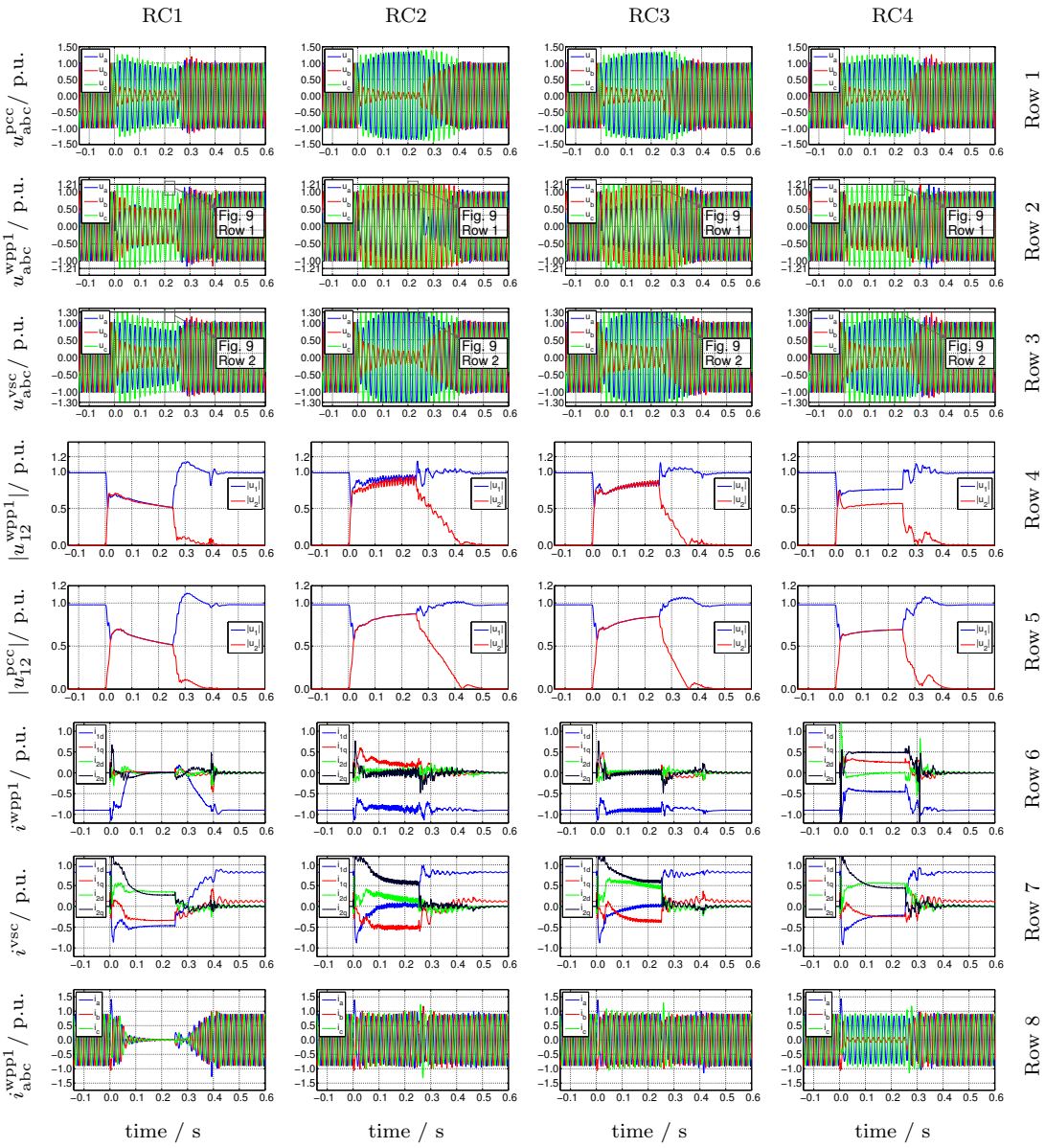


Figure 8: Results for LL fault. Column–wise order by strategy RC1 to RC4, and row–wise by voltage at PCC, applied voltage of WPP1 converter and of VSC–HVDC, seq. magnitudes for voltages at WPP1 and PCC, dq–components of currents injected by WPP1 and VSC–HVDC, and three–phase currents injected by WPP1, in the respective order.

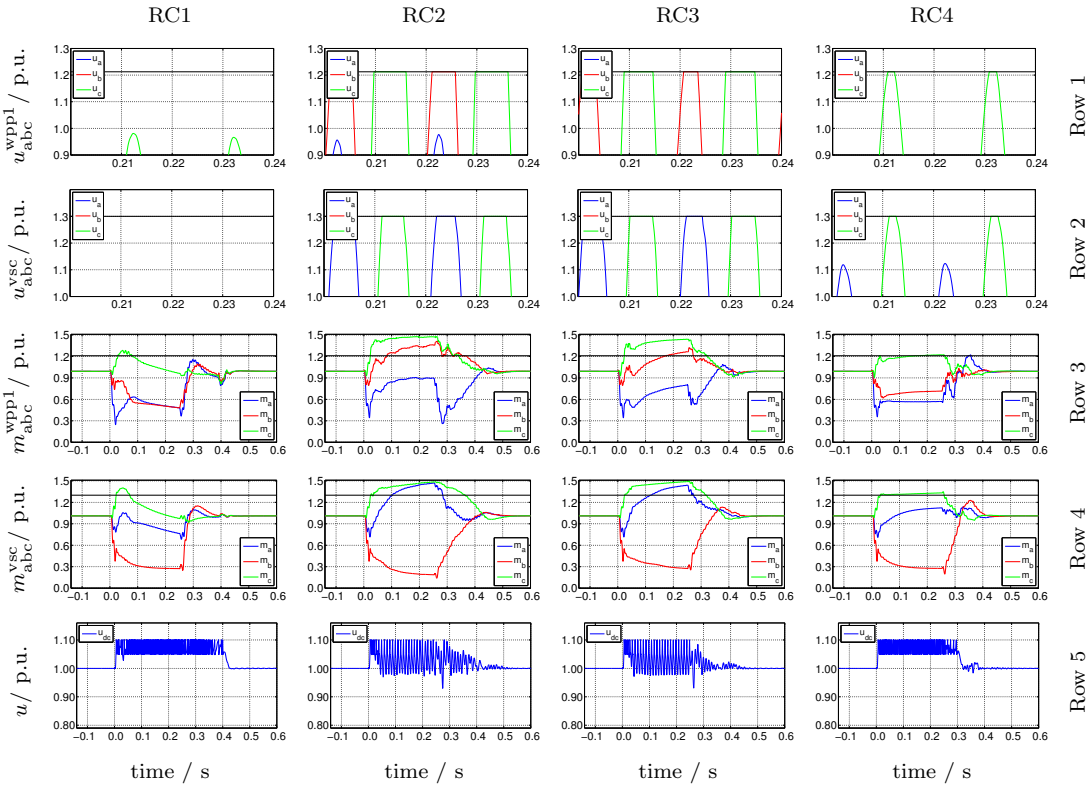


Figure 9: Zoomed results from Fig. 8, Row 2 and 3, and modulation indexes for the LL fault to visualize OM. Row 1 depicts the zoom on the applied voltage at WPP1 converter, Row 2 the zoom on the applied voltage of VSC–HVDC, and Row 3 and 4 the three–phase modulation indexes for the WPP1 converter and offshore VSC–HVDC, respectively. Row 5 plots the DC voltage of WPP1.

Row 4 and 5 of Fig. 8 depict the seq. magnitudes of the voltages at different locations, namely at the low–voltage (LV) terminals of WPP1 converter and at the PCC busbar. The voltage magnitudes for RC1 are lower during the fault than for the other strategies. Especially the WPP1 converter shows distortions for RC2 and RC3, inherently caused by OM. The OM limitation in RC3 results in a slight improvement. For RC4 the neg. seq. voltage magnitude at the WPP1 terminals is lowered through neg. seq. voltage support. Row 6 and 7 plot the dq–components of pos. and neg. seq. current measurements i_{1d}, i_{1q}, i_{2d}, and i_{2q} for WPP1 and VSC–HVDC, respectively. For RC1 and RC4 the active power injection (i_{1d}) demonstrates a significant reduction during the fault. For RC1 this is due to the OM limitation control, whereas for RC4 the q–components in both sequences have priority during the fault and force the limitation of active power. Row 8 which depicts the three–phase currents from the WPP1 converter. It underlines that the current injection differs significantly: for RC1 the current injection is reduced during the fault, whereas for RC2 and RC3 balanced currents are injected. For RC4 it might be seen that the neg. seq. voltage support leads to the injection of unbalanced currents. In Fig. 9, Rows 3 and 4, the three–phase modulation indexes of the WPP1 converter and the VSC–HVDC are depicted. Moreover, the modulation index barrier is sketched as a horizontal line at 1.21 for the WPP1 and 1.3 for the VSC–HVDC, respectively. It can be seen that the RCs relying on pos. seq. voltage support (RC2 and RC3) face higher modulation indexes and thus OM. The last row of Fig. 9 (Row 5) shows the WPP1 converter DC voltage. It is obvious that for all strategies the active current is limited leading to an increase in DC voltage and subse-

quent triggering of the DC chopper. The waveforms of RC2 and RC3 show the typical double fundamental frequency affected DC voltage ripple during the unbalanced faults. For RC1 and RC4 the active power limitation and subsequent permanent DC chopper activation revokes this oscillation.

Table 3 summarizes the mean THDs of applied converter voltages and currents at fault location which are calculated as average of the three phases over two grid cycles and 200 ms after the respective fault inception. The values are rather indicative as the concept of THD is usually applied to steady–state values and not evaluated during faults. The results related to the LL fault demonstrate low values for RC1 and RC4, as expected, higher values for RC3, and the highest for RC2. It should be mentioned that a distortion in the applied voltage obviously causes a distortion in the injected current.

In the following the SLG fault results are presented. Figs. 10 and 11 depicts the results in a similar manner as earlier for the LL fault. It can be noticed that the voltage waveforms at the PCC are similar for all RC strategies. The values of RC1 show the fastest post–fault recovery. The applied voltages (of the WPP1 converter and the VSC–HVDC) are not affected by OM for RC1 (Row 2 and 3 of Fig. 10 and Row 1 and 2 of Fig. 11). For RC2 and RC3 OM occurs in at least one phase voltage for both WPP1 converter and VSC–HVDC. The VSC–HVDC voltage corresponding to RC4 shows slight OM. The qualitative assessment can be complemented by the indicative THD values demonstrated in Table 3. The value during the faults for the WPP1 converter, for instance, is the highest for RC2 and RC3, RC4 and RC1 follow in the respective order. In the Row 4 and 5 the seq. mag-

nitudes of the voltages at the LV terminals of WPP1 and at the PCC are visualized. It can be highlighted that the seq. magnitudes are lowered the most for RC1. For RC2 and RC3, the magnitudes measured at the WPP1 face slight oscillations due to the converters operating in the area of OM. The neg. seq. magnitude reduction can be observed for RC4. Row 6 and 7 of Fig. 10 illustrate the pos. and neg. seq. current measurements for WPP1 and VSC–HVDC, respectively. For RC2 and RC3 the i_{1q} is 0.1 p.u. and zero, respectively. For the strategies RC1, RC2, and RC3 the WPP1 converter achieves the injection of almost balanced currents due to control of $\mathbf{i_2}$–components to zero. The reason is that the applied voltage is successfully adjusted without causing a (significant) OM. It can be noticed that the WPP1 converter absorbs neg. seq. currents of 0.5 p.u. for RC4 during the fault leading also to a reduction of the pos. seq. headroom. The VSC–HVDC injects i_{1q} during the fault for RC1 and RC2 (that means it absorbs reactive power generated by the WPPs and the collection grid). In contrast, the active power reduces below zero. The neg. seq. support is clearly visible by the non–zero components i_{2d} and i_{2q}. This indicates that the converter is injecting actively $\mathbf{i_2}$ components to balance the PCC voltage. Row 8 of Fig. 10 depicts the three–phase current injection by the WPP1 converter which underlines the balanced currents for RC1, RC2, and RC3 and the grid support by RC4 with unbalanced currents. To reiterate how the applied voltages are affected by OM, in Row 3 and 4 of Fig. 11, the modulation indexes of the WPP1 converter and VSC–HVDC are outlined. It can be concluded that significant OM occurs only for RC2 and RC3, whereas the results for RC4 demonstrate slight OM for the VSC–HVDC. Row 5 of Fig. 11 displays

the DC voltage of the WPP1 converter and draws similar results as during the LL fault.

Table 3: Indicative mean THDs of three–phase values: Applied voltages at the VSCs ($u_{\mathrm{abc}}^{\mathrm{wpp1}}, u_{\mathrm{abc}}^{\mathrm{vsc}}$) and of the fault currents ($i_{\mathrm{FA}}^{\mathrm{wpp1}}, i_{\mathrm{FA}}^{\mathrm{vsc}}$) for LL and SLG fault in %.

		LL				SLG			
Variable		RC1	RC2	RC3	RC4	RC1	RC2	RC3	RC4
$u_{\mathrm{abc}}^{\mathrm{vsc}}$	WPP1	1.2	22.7	17.5	1.2	1.2	8.4	9.1	4.5
	VSC	1.2	11.3	11.6	1.2	2.8	6.7	7.8	3.8
i_{FA}	WPP1	8.5	21.2	12.1	2.6	3.8	5.0	8.3	6.0
	VSC	2.8	6.7	7.8	3.8	1.8	3.5	8.5	5.8

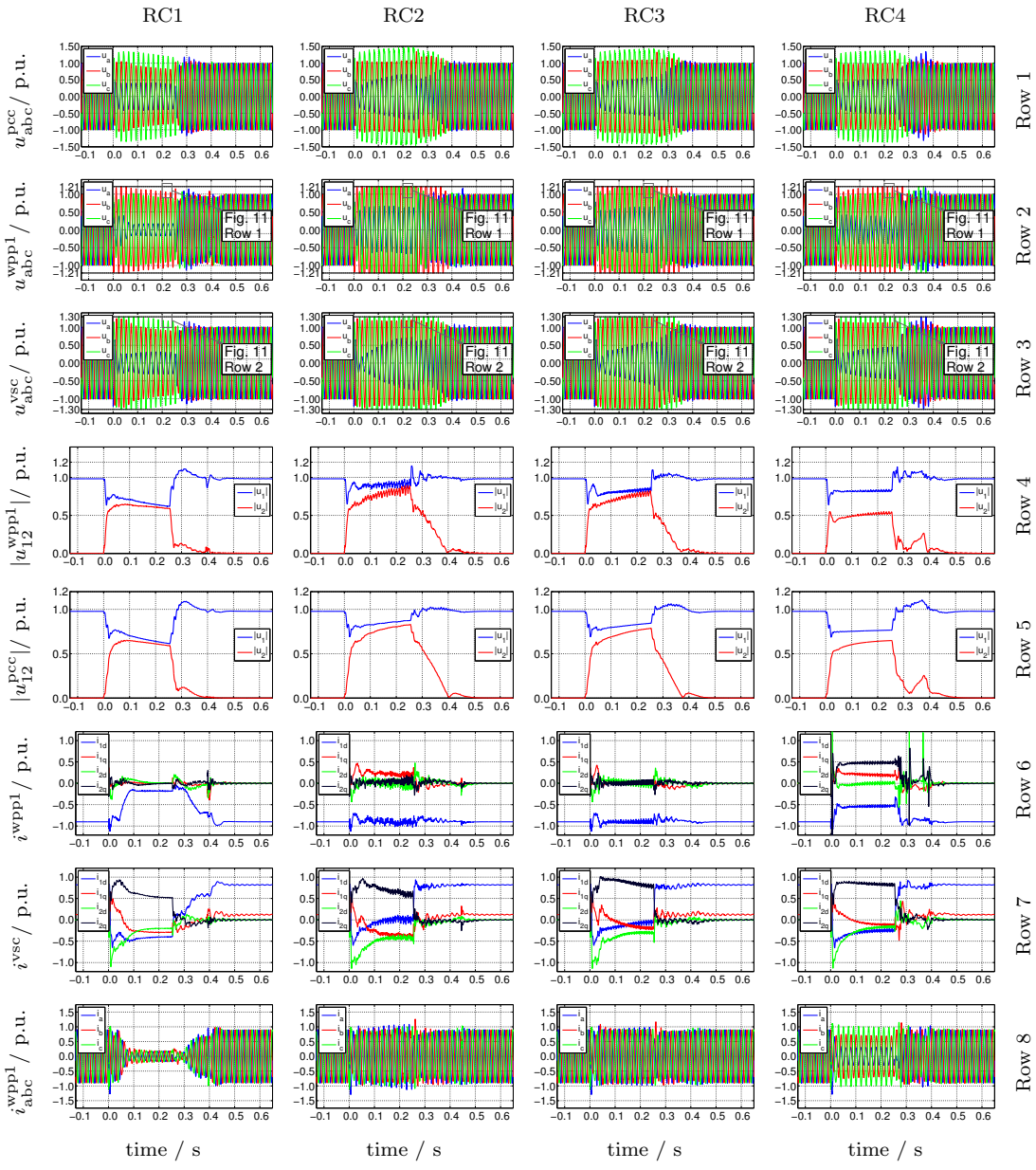


Figure 10: Results for SLG fault. Column–wise order by strategy RC1 to RC4, and row–wise by voltage at PCC, applied voltage at WPP1 converter, applied voltage at VSC–HVDC, seq. magnitudes for voltages at WPP1 and PCC, respectively, *dq*–components of currents injected by WPP1 and VSC–HVDC, and three–phase currents injected by WPP1, in the respective order.

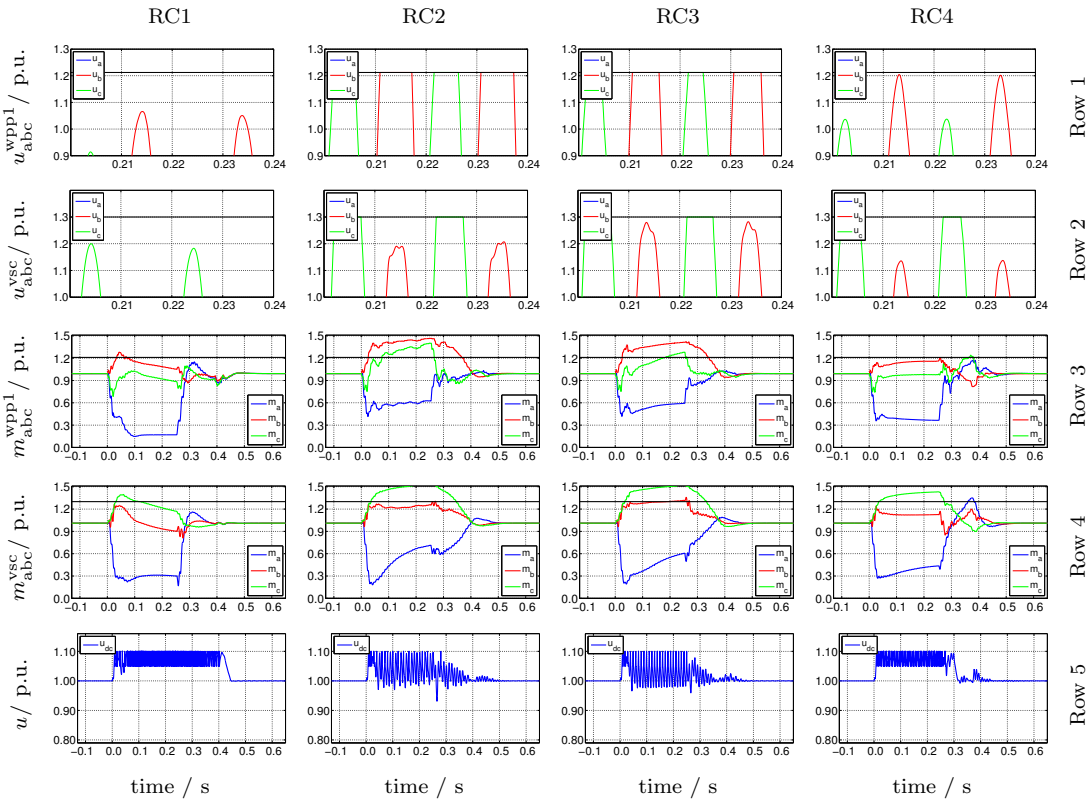


Figure 11: Zoomed results from Fig. 10, Row 2 and 3, and modulation indexes for SLG fault to visualize OM. Row 1 depicts the zoom on the applied voltage at WPP1 converter, Row 2 the zoom on the applied voltage at VSC–HVDC, and Row 3 and 4 the three–phase modulation indexes for the WPP1 converter and offshore VSC–HVDC, respectively. Row 5 plots the DC voltage of WPP1.

5. Discussion

The comparison of the strategies underlines an advantage from combined pos. and neg. seq. voltage control as well as simply no voltage support with OM limitation by reduction of active current. The faults occur in close vicinity of the VSC–HVDC which triggers fast control actions by this grid–forming converter. The results show that RC1 and RC4 are the most appropriate strategies to provide a good fault behavior as well as post–fault recovery of the system. However, when strategy RC1 is chosen there is a low short–circuit current flowing from the WPP side which might lead to problems for protection measures. The use of only pos. seq. support leads to more significant OM and consequently harmonic oscillations due to higher phase voltages even in healthy phases (RC2 and RC3). In summary, strategy RC4 provides a good system response and low OM effects for the applied voltages.

6. Conclusions

This paper has addressed the handling of unbalanced voltage conditions in VSC–HVDC–operated offshore grids. In these converter–based grids the fault contribution during unbalanced faults might be controlled by the converters and ranges from no support to pos. and neg. seq. dynamic voltage support. Unbalanced faults in vicinity of the VSC–HVDC present severe interruptions of the normal operation which have been addressed in this article. It was elaborated that OM is a challenging issue during such conditions and might be attenuated through strategies using OM limitation as well as dynamic voltage support of the neg. seq.. Furthermore, those strategies have

reduced the harmonic oscillations during the fault occurrence and supported the post–fault behavior of the system. Dynamic voltage support in both pos. and neg. seq. has represented the most appropriate solution to support both the offshore grid and the VSC–HVDC to ride–through the fault and continue to normal operation in a smooth manner.

It is recommended that offshore grid operators consider the definition of a dedicated GC for HVDC–connected offshore grids which address the specialty of those (no SGs, pure converter–based and VSC–controlled grid voltage). Future studies are targeting to use the lessons learned from the WT controls in the VSC–HVDC to enhance the most powerful converter in the system.

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Appendix A.

In this paper, vectors are denoted in **bold** and scalars in normal font, respectively. For the ease of understanding three transformation used in this paper are given: the Clarke–, Park–transformation, and the Fortescue–operator. The Clarke–transformation matrix $\mathbf{C}$ relates an $\alpha\beta 0$–vector $\mathbf{v}_{\alpha\beta\mathbf{0}}$

with the stationary reference *abc*–frame vector $\mathbf{v_{abc}}$:

$$\mathbf{v}_{\alpha\beta\mathbf{0}} = \mathbf{C}\,\mathbf{v_{abc}}; \qquad \mathbf{C} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 1 & 1 \end{bmatrix} \tag{A.1}$$

The relation between a vector in the stationary reference *abc*–frame $\mathbf{v_{abc}}$ and the synchronous reference frame $\mathbf{v_{dq0}}$ is made by the so–called Park–transformation $T(\theta)$ which results from the Clarke–transformation under rotation of angle θ using $R(\theta)$ [38]:

$$\mathbf{v_{dq0}} = \underbrace{\mathbf{C}\mathbf{R}(\theta)}_{T(\theta)}\,\mathbf{v_{abc}}; \qquad \mathbf{R}(\theta) = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{A.2}$$

Symmetrical components $\mathbf{v_{120}}$ might be transformed to the corresponding stationary frame *abc* vector $\mathbf{v_{abc}}$ by the Fortescue–operator $\mathbf{F}$ [39]:

$$\mathbf{v_{abc}} = \mathbf{F}\,\mathbf{v_{120}}; \qquad \mathbf{F} = \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{bmatrix} \tag{A.3}$$

Where multiplication with $\alpha = \exp(j2\pi/3)$ rotates a phase vector by 120°.

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