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Design of a CMOS power amplifier and built-in sensors for variability monitoring and compensation

Dissertation presented to apply for
MSc Electronic Engineering

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I think that when we know that we actually do live in uncertainty, then we ought to admit it; it is of great value to realize that we do not know the answers to different questions. This attitude of mind - this attitude of uncertainty - is vital to the scientist, and it is this attitude of mind which the student must first acquire.

Richard P. Feynman

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I would like to thank my family and Laura, for being always by my side and for their endless patience.

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Summary

This research thesis aims to develop a system composed by a a CMOS power amplifier and built-in sensors for variability monitoring and compensation.

The integration of monitoring systems with high frequency analog circuits is commonly used for performance optimization and control. In addition, built-in sensors are used in quality testing, improving the yield by detecting circuit faults during the fabrication of these.

Typically, most of the built-in sensors are electrically connected to a node of the circuit under test, affecting its performance. In tuned power amplifiers, for instance, a small load variation can cause a degradation of its output power and efficiency. Hence, the integration between the circuit under test and the monitoring block should be carefully designed. These loading effects can be avoided using non-invasive solutions such as temperature sensors.

An integrated circuit composed by a CMOS power amplifier, two amplitude detectors and a temperature sensor is implemented in this work. The degradation of the power amplifier performance due to variability effects is accelerated by increasing its supply voltage. A feedback loop is added to control and adjust the system operation, stress the amplifier and accelerate its degradation, monitor the amplifier performance using the sensors and compensate the observed degradation.

The design of each one of the main parts of the system is presented through this work, explaining their theoretical basis and validating their operation with simulations results. Finally, all the parts are integrated together, and a feedback loop with a control algorithm is proposed to monitor and compensate the DUT variability effects.

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CHAPTER 1

Introduction

During the last 40 years, the number of integrated transistors per die has been constantly increasing, making possible to improve the performance of integrated circuits [1](Fig. 1.1). This technology evolution implies a challenge for the designers that should face with new tradeoffs during the design process.

The channel length of transistors has been constantly reduced, increasing their switching frequency, and thus improving the operation speed of integrated circuits (IC). Nevertheless, higher operating frequencies suppose an increase in circuits power dissipation and, both the high transistors density and high switching frequency lead an increase in power density. Large power densities are translated into surface temperature increments, which have an impact on transistors reliability and electrical properties, affecting the overall circuit performance. As the channel length is scaled, high supply voltages can affect transistors properties and reliability. In addition, electric fields are increased due to the distance reduction between different potentials. As a solution to the stated issues, supply voltage has been scaled from 5V down to approximately 1V. Apart from temperature and voltage, manufacturing process variations must also be considered. In small channel length technologies, where supply voltage is scaled to approximately 1V, devices operate close to the threshold regime and therefore these are strongly sensitive to voltage, temperature and process variations. Therefore, it is necessary to pay attention to all these sources of unwanted errors during the design process of an integrated circuit.

Process, voltage and temperature variations together with ageing effects are typically called PVTA. Ageing effects and process variations mechanisms are described in detail in the following section. Also, some design techniques are proposed to reduce the impact of process variation effects. Finally, a brief description of temperature and voltage effects is given.

1.1 Process variations and design techniques

Process variations are those variations caused by IC manufacturing process. There are several sources of these: variations in film thickness depositions, variations due to the sub wavelength lithography, variations due to the chemical

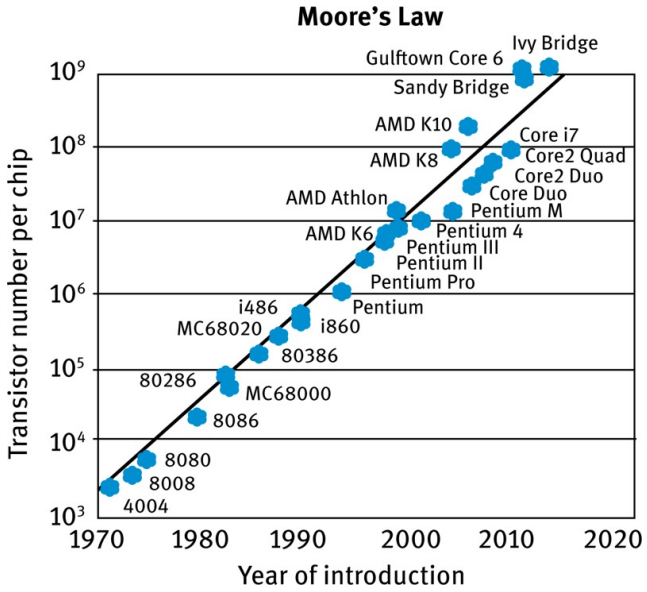

Figure 1.1: Moore's law. Evolution of the number of transistors per integrated circuit in Intel products [2]

mechanical polishing, variations on the dosage of implants, layout related issues, line edge roughness, interface roughness, random dopant fluctuations, etc. Nevertheless, the consequence in all the cases is the same: the electrical properties of one or more devices are affected and the obtained value differs from the nominal value specified during the design phase. These unwanted variations can change the expected behavior of a single device but are also source of mismatch errors that can be critical in circuits where two devices must be identical. There are, however, design techniques addressed to solve CMOS IC non-idealities, especially those related with process variability and mismatch between devices in nanoscale technologies.

Having an accurate circuit biasing is a commonly used technique. For this, there are several options. For instance, it is possible to have an accurate and temperature insensitive bias current using an on-chip bandgap voltage reference and an off-chip resistor with a very small tolerance. The obtained current is then distributed along the chip with mirroring techniques. An alternative to the off-chip resistor is to use an on-chip resistor, which will be less accurate but will still present a good matching with other on-chip resistors. Other solutions such as using a constant-gm current bias are also popular for obtaining a good biasing. The above-mentioned techniques have a big dependence on the resistors accuracy.

Another technique is the use of feedback. Feedback paths are used to track and compensate errors and inaccuracies. These are especially useful for digital IC where the clock generation is a critical part of the entire design. Using feedback it is possible to obtain a good reference clock and consequently accurate on-chip frequencies. Besides, the use of feedback technique allows us to precisely obtain a certain voltage reference (from a bandgap voltage source) or to have a good stabilization of an oscillator.

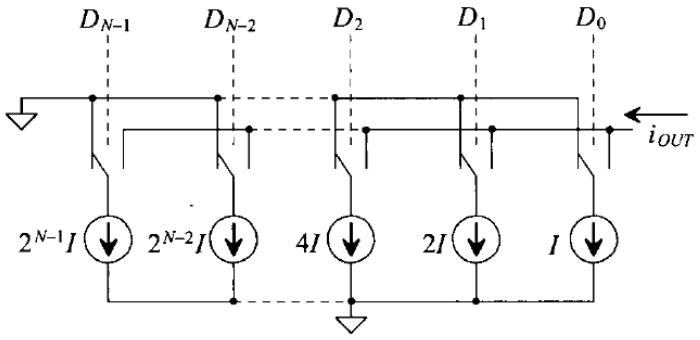

Figure 1.2: Binary-weighted current sources [5]

In addition to the mentioned analog solutions, the use of digital circuitry is usually considered as another solution, allowing the user to calibrate the IC once it has been designed and manufactured. Digitally programmable analog components such as resistors or capacitors are typically implemented [3]. Also, digitally controlled current sources are often used [4]. For instance, bandgap voltage reference with off-chip (or on-chip) resistors can be replaced by thermometer or binary weighted current sources controlled by a digital word (Figure 1.2).

An IC can be calibrated either when it is powered up or during the system operation. Calibration at the startup helps minimizing process and mismatch errors, but it will not fix system degradation due to aging effects (these will be described later). On the contrary, calibration during the system operation can compensate all kind of PVTA errors, since voltage-temperature-ageing errors will arise once the IC has been manufactured and it is already operating.

1.2 Ageing effects

Ageing effects depend on the operating conditions of a device: i.e. current levels, operating voltages and temperature. There are analytical models that can predict the degradation of MOSFET parameters as a function of applied voltages, time and temperature. However, these predictions are just approximations, and for this reason ageing effects are considered random and difficult to predict with accuracy. This section summarizes the main mechanisms source of ageing.

1.2.1 Hot Carrier Injection

Hot carrier injection (HCI) mechanisms occur when high electric fields are generated in a device. Carriers are accelerated in the presence of these electric fields, obtaining a very high kinetic energy and, in some cases, getting trapped into 'non-expected' regions. Trapped carriers modify the transistor characteristics such as the threshold voltage V_{th} and carriers mobility.

HCI effects should be taken into account specially for nowadays technologies. Although supply levels have been downscaled, circuits present high components density and distances between different voltages are reduced, generating large

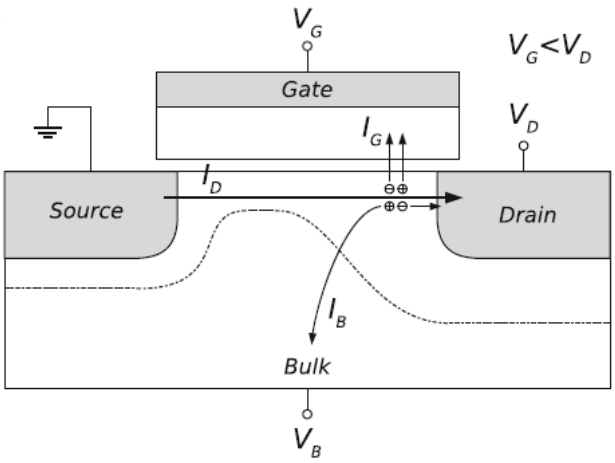

Figure 1.3: Drain avalanche hot carrier generation [6]

electric fields. Additionally, increasing the transistor bias voltage will increase the electric fields, accelerating the degradation process.

Hot carrier injection mechanisms can be classified depending on which region is affected by the large electric field (gate, bulk, drain...). Among all the mechanisms, drain avalanche hot carrier generation (DAHC) (Fig. 1.3) and channel hot electron injection (CHE) are considered the worst.

For instance, 0.35 um technology devices (e.g., AMS 0.35um technology) are strongly affected by DAHC mechanism. This effect can be observed when the device is biased with high drain voltages (or high supply voltages). On the other hand, smaller devices are more sensitive to CHE effects. These can be observed when the gate voltage is approximately equal to the drain voltage.

1.2.2 Time-Dependent Dielectric Breakdown

The correct operation of a MOS transistor relies on the insulating properties of the dielectric layer below the gate electrode of the transistor. The dielectric material, however, has a maximum electric field that can withstand, therefore it may breakdown when a high electric field is applied (Hard Breakdown effect HBD), or simply after some usage time (Time-dependent dielectric breakdown, TDDB).

The degradation of the dielectric is a gradual process caused by traps that are randomly generated inside the oxide. These traps induce leakage currents flowing through the interface, and the insulating properties of the dielectric are decreased. The process finishes when a high traps density is reached and the dielectric breaks down.

1.2.3 Bias Temperature Instability

Bias temperature instability (BTI) effects are observed when the gate of a MOSFET is biased with high voltage values. When MOS transistor is heavily biased for a long period of time, threshold voltage V_{th} and channel mobility are

modified. This parameters shift is caused by elevated temperature effects on the gate of the transistor. Consequently, the drain current and the transconductance are reduced, degrading the circuit performance.

BTI can affect both nMOS and pMOS devices, and can be distinguished in two main types: positive BTI (PBTI) and negative BTI (NBTI) depending on the sign of the gate bias voltage. Among the four possible permutations, pMOS-NBTI and nMOS-PBTI exhibit the worst effects, and therefore should be taken into account. It is important to remark that, contrary to the non-reversible HCI effects (carriers are trapped), BTI effects have transitory and permanent components, which means that the affected device is partially recovered after some time.

BTI and HCI mechanisms can be related, at least to some extent, given that both depend on device biasing. It may happen that, due to high gate voltage values, HCI mechanisms are triggered in addition to BTI (i.e. channel hot electron injection effects). For this reason, both effects can occur at the same time, and therefore it is important to avoid HCI effects in case we want to evaluate how BTI mechanism affects the device performance.

1.2.4 Electromigration

Finally, not only transistor devices but also other integrated circuits components such as interconnect wires and contacts are affected by ageing effects. The gradual movement of the ions in a conductor cause a transport of material, degrading the wire or contact physical properties. This effect is critical in applications that deal with high current densities.

1.3 Voltage and Temperature effects

Temperature variations are caused by both environmental factors and the power dissipation of the integrated transistors. The increase in power dissipation density due to high components density has aggravated thermal effects. Temperature changes affect transistors electrical parameters such as carriers mobility and V_{th}. Besides, reliability issues can arise (BTI), also affecting the threshold voltage V_{th} of the devices.

Voltage variations are a consequence of rapid switching of currents due to inductive components within an IC and resistive losses. These factors cause variability in the IC power distribution network and it may happen that two similar devices are supplied at slightly different voltages, affecting their performance.

1.4 Motivation

In the previous sections, the most relevant effects that push circuit performance and specifications such as ageing, process, voltage and temperature variations have been explained. Also, techniques for designing a robust and reliable circuit against process variations have been given. This is, however, not enough in most of the cases.

Due to the increasingly demand of high performance system-on-chips (SoC), it is necessary to check the correct operation of an integrated circuit before it is taken to the market. The quality testing is an important step in the product development, as well as the design and manufacturing phase. A good testing process can help improving the yield by detecting circuit faults during the early fabrication stages. When a fault is detected, it is possible to active a certain complementary circuitry or procedures to compensate it.

This need of fault detection has recently become more important with the growing interest in mixed-signals systems and the proliferation of wireless applications. RF circuits such as Low-noise amplifiers (LNA), voltage-controlled oscillators (VCO), mixers and power amplifiers (PA) are implemented in nowadays integrated circuits, and these must be tested to ensure the correct performance of the SoC wireless applications.

Tests can be done either analyzing the top-level performance parameters or accessing internal nodes and paths of the RF circuit. In the first case, performance parameters are obtained doing functional tests using equipment able to generate accurate signals in the bandwidths and resolution of the device. In most cases, the high cost of the necessary instrumentation can affect the final cost of the product.

Accessing internal nodes and paths is a useful method to characterize a specific block of the entire SoC. The figures of merit of each one of the composing blocks can be individually obtained monitoring their input and output nodes. For instance, the bandwidth, gain and linearity figures of a power amplifier can be obtained monitoring its input and output nodes. Analysing these figures of merit it is possible to detect if the PA is not operating as expected.

Besides, it is possible to analyze the temperature, voltage and process variation impact on each one of the blocks. Nevertheless, doing this can be almost impossible in current integrated circuits. As it was mentioned at the start of this chapter, the number of integrated transistors per die has been constantly increasing. This phenomena leads to a high increase in the complexity and components density of nowadays integrated circuits, complicating the monitoring of all the IC internal nodes during the debugging phase, thus decreasing the circuit observability. This loss of observability represents a problem when a certain faulty section of the SoC must be identified.

As a solution, the built-in test approach methodology is proposed. This approach is based on the use of on-chip sensors. The output signal of these on-chip sensors is sent to the exterior through IC package pins. Although adding extra circuitry in an IC will increase its area and cost, it will improve the accessibility and observability of internal nodes and paths, making easier to detect and identify possible faults, as well as reducing the need of high performance test equipment. In the case of RF circuitry, the design of on-chip sensors will have an added difficulty, considering the high operation frequencies and possible unwanted load effects.

1.5 Goal of this work

The objectives of this work are the following:

- To design an RF circuit that can be susceptible to ageing. This circuit will be the device under test (DUT).
- To be able to accelerate ageing effects modifying the bias of the DUT.
- To design a set of sensors that monitor several figures of merit of the DUT, in order to detect when ageing alters its performance.
- To include knobs in the circuit under test, that allow the implementation of a feedback mechanism that compensate performance degradation.
- To propose and evaluate a feedback mechanism for compensating DUT degradation.

For this, a system composed by an integrated circuit (IC) and a feedback loop will be designed. The IC will contain the device under test and monitoring circuit, while the feedback loop will contain the logic unit in charge of receiving and processing the signal coming from the monitoring block and actuating over the DUT if necessary.

To contemplate a real scenario, the chosen device under test is a power amplifier. RF communication circuitry is present in the vast majority of commercial devices due to the extensive use of wireless applications, and it is in charge of transmitting and receiving radio signals. To correctly establish communications and provide a good data transmission, the power amplifier must boost the power of the signals that are going to be sent. In order to transmit enough power, RF modules (and especially PA) typically work with higher supply voltages and currents than the rest of the circuit. The continuous use of high voltages and currents make power amplifiers prone to suffer from ageing effects, degrading their performance and deteriorating the radio communications of the commercial device.

To accelerate this degradation, ageing effects will be forced increasing the supply voltage of the device. This method is commonly known as 'stressing' the device. As a consequence, the electrical parameters of the PA will be modified, hence affecting the circuit performance.

The power amplifier will be characterised and monitored using on-chip sensors. Two different type of sensors will be implemented: temperature sensors and amplitude detectors. These will be in charge of tracking the PA input and output signals, in the case of the amplitude detector, and power dissipation in the case of the the temperature sensor. Finally, the sensors output signal will be sent to the feedback path through the IC package pins in order to analyse if the DUT has been affected by the forced ageing and temperature effects.

The main task of the feedback loop will be to check the data coming from the on-chip sensors and compare it with the one obtained before the PA is stressed (e.g, at the start of the measurement). Then, if the performance of the PA has changed (e.g, gain has decreased), its bias current will be increased, closing the system loop and compensating the measured degradation. Figure 1.4 illustrates a block diagram of the proposed system.

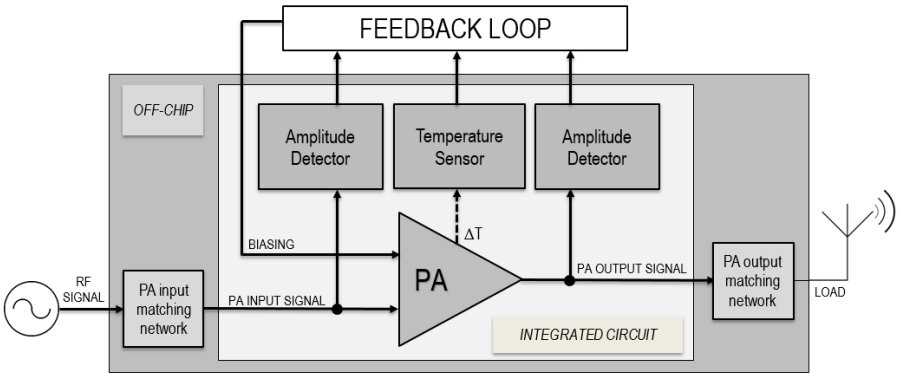

Figure 1.4: Block diagram of the proposed self-healing system

1.6 Document outline

This work is compiled in 7 chapters.

Chapter 1 gives a brief introduction to the most common IC variability effects and design techniques. Also, the motivation, objectives and document outline are presented.

Chapter 2 shows examples of digital and analog correction and calibration techniques. Among the presented analog approaches, special emphasize is put on temperature based measurements, and heterodyne and homodyne methods are analysed in detail.

Chapter 3 explains the design procedure of the PA. Firstly, a theoretical introduction is given. Then the design procedure is presented, describing in detail all the parts of the amplifier and design considerations. Simulation results are finally shown.

Chapter 4 corresponds to the design of the temperature sensor. It starts with a comparison between MOS and BJT transistors working as temperature transducers. Their thermal sensitivity is analysed and compared, showing the advantages and drawbacks of the use of each one depending on the targeted application. Then, an operational transconductance amplifier (OTA) is proposed as the conditioning circuit. Design keys and simulations are shown for both cases: using MOS and BJT transistors as transducers. The chapter concludes with a comparison of the obtained results.

The design of the amplitude detector is explained in *Chapter 5*. The operation principle of the chosen topology is explained. Following, the design decisions are detailed and the simulation results are shown.

Chapter 6 starts with a compilation of the previously designed modules. Their pinout an configuration is reviewed and a general view of the system is presented. Some possible measurements using the sensors are proposed, and the possible amplifier performance degradation scenarios are analysed. Finally, a system startup and ageing observation methodology are proposed.

Chapter 7 discuss the achieved goals. Also, next steps are proposed in order to continue with the research.

1.7 Methodology

- All the circuits have been designed with *AMS HITKIT 4.10 ISR* (Austria Microsystems High Performance Interface Tool Kit) environment, using AMS 0.35 µm components libraries.
- The schematics have been edited using *Virtuoso Analog Design Environment*, and simulated with *Spectre MMSIM* tools available in *Cadence*.
- The *Cadence* framework license has been provided by the Electronic Engineering Department (DEE) of the Universitat Politècnica de Catalunya (UPC).
- Finally, all the figures have been post-processed with *MATLAB*.

1.8 References

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CHAPTER 2

State of the Art

With the rapid progress of new technologies, integrated circuits (IC) have become smaller over the years. At the same time their complexity and functionality has increased, leading to, for instance, sophisticated mixed-signal chips. The design of nowadays IC represents a challenge and circuits should be designed in a way that their high-performance and reliability is not affected by sources of variability, mainly those associated to the manufacturing process.

Built-in test strategies allow to improve integrated circuits robustness and reliability against process variations. The use of on-chip sensors and tuning circuitry enable to precisely test and calibrate an individual part of a whole IC, increasing the product yield and lowering manufacturing costs.

The work presented in [1] contains several built-in test approaches for compensating process variation effects in IC. The main goal of all the compiled solutions is to provide circuits with tunability and controllability capacities, as well as propose digital calibration algorithms. Although these works are mainly focused on process variation related techniques, many of these solutions can be applied for compensating circuits performance degradation caused by other circumstances: i.e., to compensate degradation due to ageing effects.

In general, calibration, correction and tuning solutions can be classified in two big categories, depending on the nature of the implemented technique: digital correction and calibration methods, and analog measurement and tuning techniques. Also, it is possible to find solutions combining both analog and digital features. This section will provide a brief description of each type of technique, and some examples of state of the art works will be shown. Finally, especial emphasis will be placed on on-chip temperature sensors based solutions.

2.1 Digital solutions

Digital orrection and calibration techniques are based on measurements and compensation procedures carried out in the on-chip digital domain. For instance, the work in [2] proposes a digital solution for improving the performance of a low-IF receiver, while in [3] a digital technique is implemented to monitor failures and compensate center frequency drift of a digitally controlled oscillator.

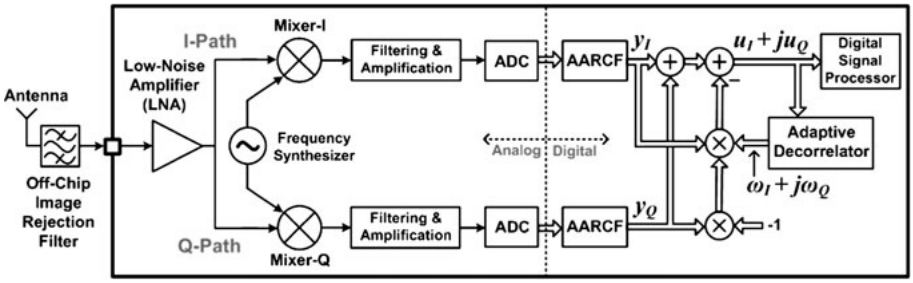

Figure 2.1: Low-IF receiver with digital IQ mismatch compensation [2]. Image taken from [1]

In both cases, the monitored circuits have on-chip analog-to-digital converters (ADC) and digital signal processor units (Fig. 2.1).

Digital methods offer a high precision solution since complex algorithms can be executed on-chip. However, the monitored system must have enough computational resources for digital signal processing tasks, as well as the necessary digital features.

2.2 Analog solutions

In circuits with few on-chip digital resources, analog solutions are typically used. Analog tuning and compensation circuits provide a faster correction than with digital approaches, because measurements do not need to be digitally processed (convergence of digital algorithms may be a time-consuming process). As a drawback, the design of analog circuitry is more challenging than with digital schemes, and it should be carefully designed to be robust and to avoid failures.

Analog approaches are used in many radio frequency (RF) front-end circuits where figures of merit such as input and output impedance matching, gain and linearity are prone to be affected by all type of process, voltage, temperature and ageing variations (PVTA). Digital techniques are normally discarded in RF applications because good signal digitization is not possible at high frequencies. The integration of analog built-in self-test (BIST) strategies permit to monitor all these figures of merit and therefore actuate over the device under test (DUT) if a performance variation or fault is detected. For example, [4] presents a low-cost RF BIST measurement for low-noise amplifiers (LNA). As it can be observed in Fig. 2.2, the proposed IC is formed by a LNA and an analog BIST block. The on-chip BIST block contains a signal amplifier and peak detectors, and is able to measure the most important LNA figures of merit without the need of integrating complex digital circuitry (i.e., digital signal processors [5]). In [6], a technique for self-calibration of input impedance matching in a low noise amplifier is exposed. On-chip analog sensing circuitry is used to achieve short calibration times. A peak detector is used to convert the signal coming from the sensing circuitry into a DC signal proportional to the input match of the LNA.

The use of power, envelope and rms detectors is considered as the classical solution for monitoring the circuit performance in RF built-in self-test mechanisms. The signal paths of RF circuits can be monitored by connecting

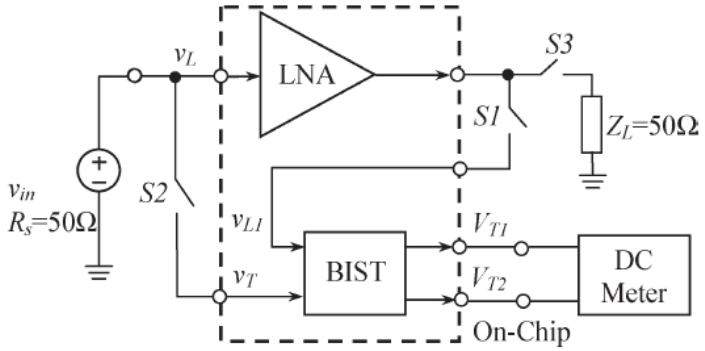

Figure 2.2: LNA test structure. Image taken from [4]

power or amplitude detectors to their nodes [7][8][6]. Figure 2.3 shows the system level illustration of the adaptive bias loop presented in [7]. A tunable envelope detector is connected to the output of a power amplifier (PA) in order to sense the power delivered to the load. The low frequency output voltage of the envelope detector is then used to dynamically adjust the bias current of the PA and improve its power added efficency. Connecting an envelope detector at the output of a RF circuit to dynamically control its bias is a technique widely used with mmWave amplifiers (60 - 90 GHz)[9][10][11].

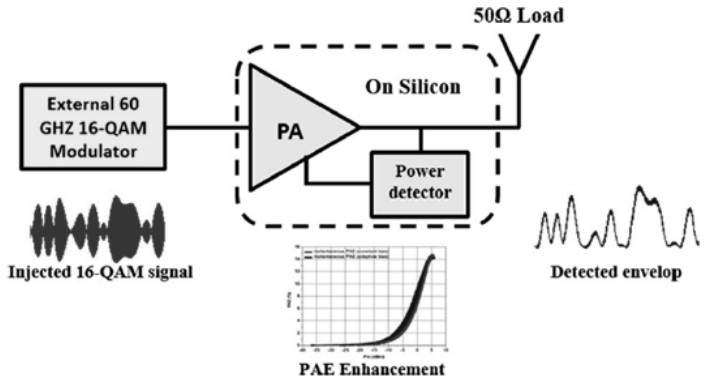

Figure 2.3: Adaptive bias loop system level illustration. Image taken from [7]

The main drawback of using power and amplitude detectors is that the monitored device is electrically loaded, therefore it may happen that the sensors themselves affect the DUT performance. Temperature sensors are proposed as a non-invasive solution for on-chip testing.

It has been already demonstrated that temperature sensors can be used for monitoring and characterizing circuits without electrically loading them. In the case of RF circuits, on-chip temperature sensors have been used, for instance, for monitoring circuit parameters such as the efficiency [12], center frequency and 3 dB bandwidth [13], 1 dB compression point [14] and gain [15] of an RF power amplifier, or the center frequency of a low noise amplifier [16].

Also, the silicon surface temperature as a function of the RF input signal of a power amplifier, and the structural integrity of a low noise amplifier have been measured with results in [17] and [18], respectively. Figure 2.4 shows the built-in test mechanism used in [19]. In this case, the system has no self-test capabilities but it is externally controlled with instrumentation: a circuit under test (CUT) is externally biased with a power supply. The CUT temperature is measured with a differential temperature sensor (DTS), and the output of the temperature sensor is sent to a digital multimeter.

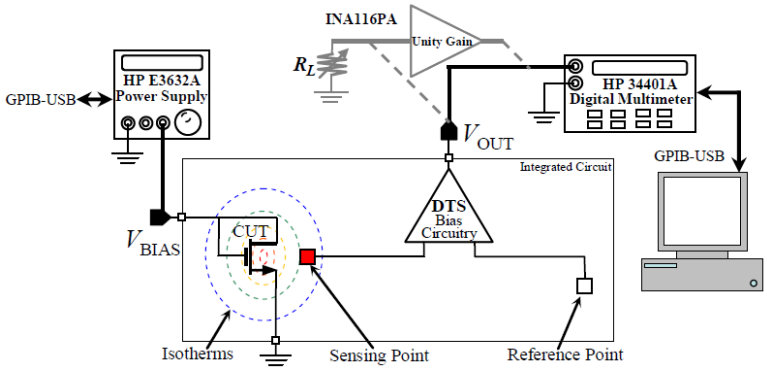

Figure 2.4: Test setup for DC measurements with a differential temperature sensor

In all the mentioned cases, the employed measurement technique is based on the same principle. Electrical dynamic operation at high frequencies is translated into low-frequency power dissipation. Due to the Joule effect, the power dissipation is converted into temperature, and propagated through the device under test (DUT) with a low-pass response. RF built-in testing mechanisms based on temperature observations exploit these electro-thermal properties, inducing temperature changes on DUT with RF signals, and monitoring the temperature variation at low frequencies (Fig. 2.5). Two main techniques are used: heterodyne [13] and homodyne [20]. A brief explanation of each technique basis is provided below.

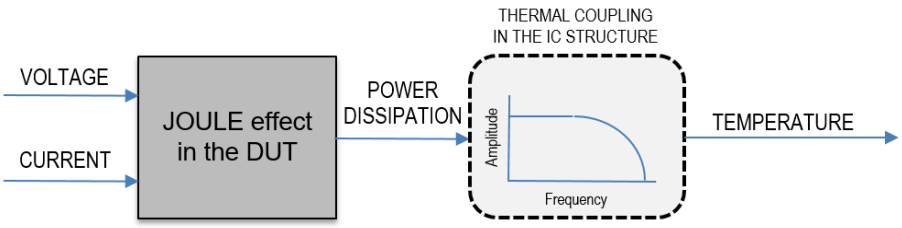

Figure 2.5: Thermal coupling model

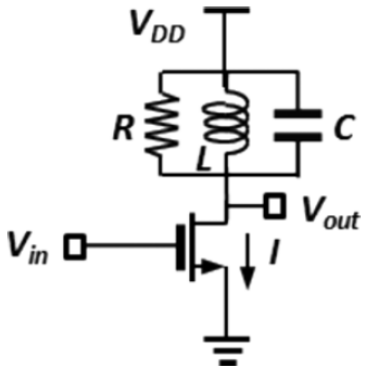

Figure 2.6: Tuned load common source amplifier. Image taken from [13]

2.3 Temperature sensing techniques

Heterodyne and homodyne techniques are both based on applying input tones to a circuit and observing variations on the device temperature. The measured temperature is related with the low frequency components of the device dissipated power (thermal coupling bandwidth), and therefore the DUT can be characterised if either the amplitude or phase of the dissipated power by the devices depends on the figure of merit to be observed, i.e., gain.

The main difference between heterodyne and homodyne technique is the number of tones applied at the input of the monitored device. Two input tones are applied using the heterodyne method, while a single tone is applied with homodyne.

2.3.1 Heterodyne technique

The heterodyne method is based on applying two input tones to the DUT. A tuned load common source amplifier has been chosen for the analysis (Fig. 2.6). The power dissipation of the MOS device is defined as:

$$P_{i_{MOS}} = V_{out} I_D = (V_{out_{DC}} + \Delta V_{out})(I_{bias} + \Delta I_D) \tag{2.1}$$

$$\Delta V_{out} = -g_m Z_L V_{in_{RF}} \tag{2.2}$$

$$V_{in} = V_{bias} + V_{in_{RF}} \tag{2.3}$$

$$V_{in_{RF}} = Acos(\omega_1 t) + Acos(\omega_2 t) \tag{2.4}$$

Where g_m is the MOSFET transconductance parameter, Z_L is the load impedance and A is the RF input signals amplitude. Manipulating expression (2.1), the power dissipation at the input tones frequency difference $\Delta\omega$ can be written as follows:

$$P_{i_{MOS}}(\Delta\omega) = \frac{-g_m^2 A^2 |Z_L|_{\omega_1}}{2} cos(\theta_{Z_{L_{\omega_1}}} - \Delta\omega) + \frac{-g_m^2 A^2 |Z_L|_{\omega_2}}{2} cos(\theta_{Z_{L_{\omega_2}}} + \Delta\omega) \tag{2.5}$$

$$P_{i_{MOS}}(\Delta\omega) \simeq -g_m^2 A^2 cos(\theta_{\omega_1,\omega_2}) cos(\Delta\omega t)|Z_L|_{\omega_1\omega 2} \tag{2.6}$$

The approximation of eq. 2.6 can be done by considering that both ω_1 and ω_2 are close enough to assume $\Delta\omega$ is smaller than the electrical bandwidth of the circuit. Also $\Delta\omega$ must be small enough to fall inside the thermal coupling bandwidth. Then, $|Z_L|_{\omega_1} \simeq |Z_L|_{\omega_2}$ and $\theta_1 = \theta_2$. Finally, the expression that relates the input tones with the power dissipation at $\Delta\omega$ is written as:

$$P_{i_{MOS}}(\Delta\omega) = -|A_v| g_m A^2 cos(\theta_{1,2}) cos(\Delta\omega t) \tag{2.7}$$

$$|A_v| = g_m |Z_L| \tag{2.8}$$

Where $|A_v|$ is the absolute value of the amplifier small signal gain.

As it can be seen in eq. 2.7, it is possible to characterize the DUT by sweeping the frequency of the two input tones frequency, keeping $\Delta\omega$ fixed. The dissipated power will depend on the stage gain A_v at the input tones frequency $\omega 1$ and $\omega 2$ (considering $\omega 1 \simeq \omega 2$). As a drawback, it is important to remark that it is difficult to generate two high-frequency tones with small and precise spacing between them, and a lock-in amplifier or signal processing is necessary in order to obtain the $\Delta\omega$ component of the temperature sensor output signal.

2.3.2 Homodyne technique

Homodyne method is similar to the heterodyne but only one input tone is used in this case. Again, a tuned load common source amplifier is used as a model for the theoretical analysis (Fig. 2.6). The dissipated power of the MOS transistor is expressed as:

$$P_{i_{MOS}} = V_{out} I_D \tag{2.9}$$

$$I_D = I_{bias} + g_m A cos(\omega_{in} t) \tag{2.10}$$

$$V_{out} = V_{out_{DC}} - g_m |Z_L|_{\omega_{in}} A cos(\omega_{in} t + \theta_{Z_{L_{w_{in}}}}) \tag{2.11}$$

Where A is the amplitude of the input signal, g_m is the MOS transconductance and Z_L is the equivalent load. Since device temperature is affected only by low frequency components, the expression of $P_{i_{MOS}}$ can be simplified to:

$$P_{i_{MOS}} = V_{out_{DC}} I_{bias} - \frac{g_m^2 A^2 |Z_L|_{\omega_{in}} cos(\theta_{Z_{L_{w_{in}}}})}{2} \tag{2.12}$$

As it can be observed, the DC component of P_{iMOS} is formed by two terms. The first term depends on the DC bias, while the second term depends on the RF input signal and the circuit load.

Similarly as with heterodyne technique, some conclusions can be obtained. The device under test can be characterised sweeping the RF input signal amplitude and frequency. Given that only one tone is needed, homodyne method is easier to implement than heterodyne. Besides, power dissipation measurements can be performed with a simple DC multimeter and therefore no complex equipment is necessary. Nevertheless, it is necessary to do a temperature measure with no RF input signal in order to calibrate the first term in eq. 2.12.

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CHAPTER 3

Power Amplifier

Power amplifier is a key part of an RF transceiver. It is usually the last stage in every RF transmitter front-end, and it is in charge of boosting the signal power so that it can be properly propagated, received and decoded by another transceiver. This chapter explains the design of the power amplifier used in this work. A theoretical introduction is first given in order to provide the basic insights about power amplifiers. It then moves to the design requirements and topology choice. Once the PA topology has been determined, its complete design is explained. Finally, simulation results are shown.

3.1 Introduction

There is a vast amount of literature about power amplifiers (PA) explaining their basic operation principles and fundamental metrics, classification, design workflows, stability and enhancement techniques [1][2][3][4]. However, the fundamental knowledge and aspects of power amplifiers are provided in this section. Basic notions of PA operation principle, classes and metrics are explained below.

3.1.1 Power amplifier operation principle

Figure 3.1 shows the generic PA topology, typically used to theoretically analyse and explain the basic PA operation. The NMOS transistor is commonly configured as a common-source stage with a large inductor connected between the output node and the supply source. The large inductor, also called RF choke inductor, feeds DC power to the drain, acting as a constant current source that can sustain both positive and negative voltage values. The PA drains power from the DC supply and converts it into an RF signal power. The output signal is controlled by the input signal and bias conditions of the transistor. Finally, input and output impedance matching networks are implemented in order to tune and maximise the power transfer from the input to the PA, and from the PA to the load (i.e., an antenna).

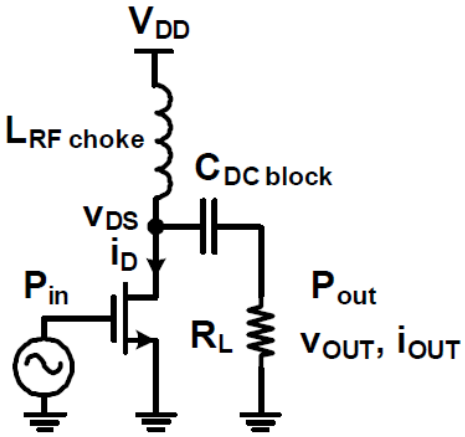

Figure 3.1: Basic power amplifier topology

3.1.2 Power amplifier classes

There are many PA operation modes and topologies, and these can be classified according to different criterias such as operation mode, number of stages, single ended or differential topology, etc. Nevertheless, power amplifiers are traditionally classified by their bias condition, labeled Class A, AB, B, C, D, E and F depending on the portion of the input signal cycle for which the transistor conducts (conduction angle).

Figure 3.2 illustrates the PA drain current I_D as a function of V_{GS}. As it can be observed, class A amplifiers are biased in a way that the transistor can conduct for the entire input signal range. Then, bias point is moved towards transistor threshold voltage V_{th}, and the PA only conducts during positive input signal cycles (Class AB and B). As long as the bias point is reduced (V_{GS} lower than V_{th}), the PA conducting time decreases (Class C). Finally, Class D and E amplifiers, also called switch-type PAs, use digital circuits and pulse width modulation (PWM) to constantly turn the transistor operation region from ohmic to cut-off.

Figure 3.3 shows the conduction angle and efficency of each PA class from A to E. As long as we move from class A to class F operation, the efficency of the PA is increased at expenses of linearity. Class A amplifiers are considered the most linear approach since the transistor is kept in the saturation region of operation almost all the time, but the drain efficency is poor because transistor is always conducting. On the contrary, class D and E power amplifiers exhibit high non-linearity figures due to their switching behavior, but these are more efficient solutions. Finally, class F PA is treated independently because it combines both current source amplifier and switching operation modes.

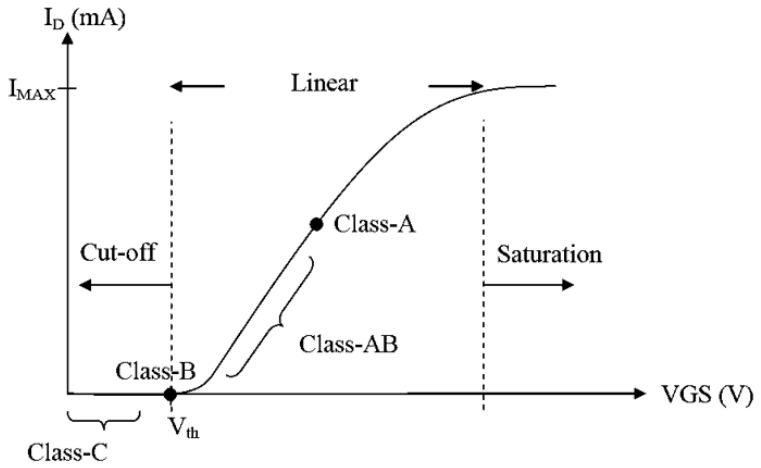

Figure 3.2: Comparison between PA classes operating point

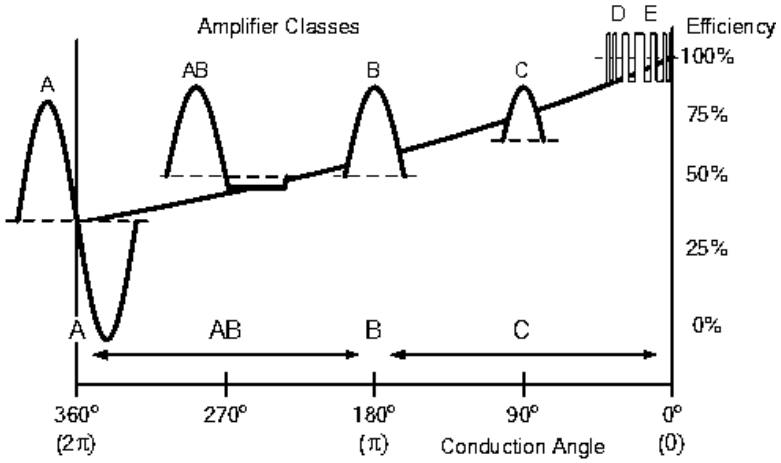

Figure 3.3: Comparison between PA classes efficiency and conduction angle. Image taken from [5]

3.1.3 Fundamental metrics

Power amplifiers are usually evaluated with a series of metrics that quantify their performance in terms of gain, linearity, efficiency, power capability, size, noise, etc. These metrics can also be used as a starting point for the design process. For instance, in applications where we need to deliver large power signals, the design is focused on power gain. While for applications where power consumption is a critical aspect, the PA design is focused on optimising its power efficiency. The most relevant PA metrics are listed below:

- *Saturated Power (P_{SAT})*: Saturated power indicates the maximum power that the power amplifier can deliver. Considering that PA is controlled by a sinusoidal signal, the maximum output power delivered to the load

can be expressed as:

$$P_{out} = \frac{V_{DD}^2}{2R_L} \tag{3.1}$$

- *Power Gain (G_P)*: Represents the ratio between the PA output power P_{OUT} and input power P_{IN}:

$$G_P = 10log(\frac{P_{OUT}}{P_{IN}}) \tag{3.2}$$

- *1 dB compression point (P_{1dB})*: Represents the output power at which the power gain G_P drops 1 dB from the linear value. It represents a practical limit between the linear and non-linear region (Figure 3.4).

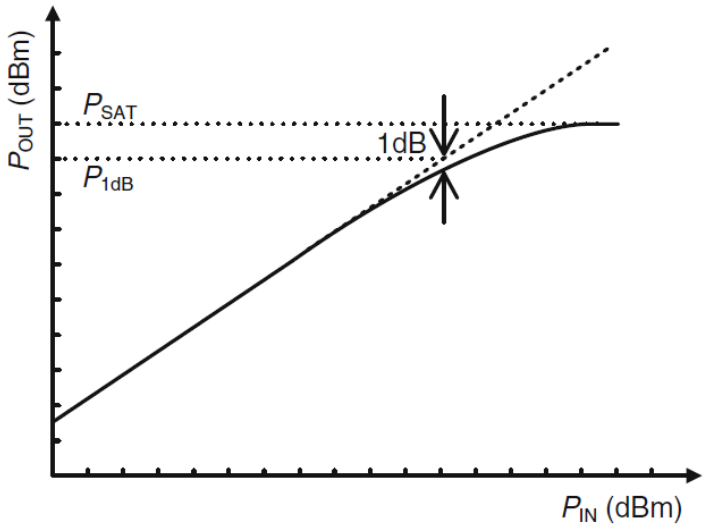

Figure 3.4: P_{1dB} representation in the P_{out}-P_{in} curve. Image taken from [4]

- *Third Order Interception Point ($ICP3$)*: The $ICP3$ represents the intersection between the fundamental tone at the output and the third order intermodulation products. Intermodulation products are generated when two tones close in frequency are applied to the PA input.
- *Drain efficiency (η_D)*: The drain efficiency represents the ratio between output power and DC power consumption.

$$\eta_D = 100\frac{P_{OUT}}{P_{DC}} \tag{3.3}$$

- *Power Added Efficiency (PAE)*: Similarly to Drain efficiency, Power Added Efficiency is represented as the ratio between the RF power consumption and the DC power consumption. The RF power consumption is calculated as the difference between P_{OUT} and P_{IN}:

$$PAE = 100\frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{3.4}$$

3.2 Power amplifier design

In this section the design of the power amplifier is explained. The PA chosen topology and technical specifications are presented. Then, the design of the PA is splitted into four parts: design for working under nominal conditions, stability considerations, stress and protection considerations, and simulation results.

3.2.1 Power amplifier topology

Choosing the right power amplifier topology strongly depends on the targeted application. Power output, gain, efficency and linearity requirements will determine which circuit topology is used in each situation. In this work, we want to stress a power amplifier and quantify its performance degradation. For this, the power amplifier must accomplish the following three requirements:

- **Controllable**: We must be able to modify its bias conditions, input signal power and supply voltage. Ageing effects will be accelerated increasing the PA supply voltage. Bias voltage will allow us to modify the PA operating point. Finally, RF input signal will allow us to characterise the PA behavior in terms of gain, bandwidth, linearity and efficiency.
- **Ageing sensitive**: The PA must be sensitive to ageing effects. Stressing the device should significantly affect its performance.
- **Observable**: We must have access to all the PA terminals to fully characterise and to monitor it. We want to externally measure each PA transistor. That means having acces to their gate, source and drain terminals.

Compared to single stage topologies, multistage power amplifiers provide higher gain, and increased power capabilities. Multistage topologies are commonly used in high power applications, or in systems where very weak signals must be boosted to usable levels such as radio receivers. Also, in mmWave amplifiers, where single stage configurations cannot provide the required gain values, multistage solutions are implemented. However, monitoring and controlling all the MOS devices is not feasible in terms of cost and sensing circuitry. Especially in RF circuits, adding too many sensing devices can affect the overall PA performance due to load effects. For this reason, multistage topologies are not considered as a possible PA configuration in this work.

Similarly to multistage, cascode configurations are typically used in power amplifiers. Cascode topologies improve the stability of the PA due to the isolation between input and output nodes. Nevertheless, these are neither a good solution since we cannot access to the drain node of the transconductor MOS. Besides, ageing effects are divided among two transistors, i.e. the PA is less sensitive to the applied stress.

Taking all into account, a single transistor PA topology has been chosen. It allows us to access to all the MOS terminals (gate, drain and source) and ageing effects can be precisely quantified since we only have to monitor one transistor.

Regarding the operation mode, class B to F power amplifiers are usually implemented in systems where linearity is not a major concern and power

efficiency is a requirement. These are however more complex to analyse than class A and AB because of their switching behavior. Instead, class A and AB power amplifiers are simplier to analyse. Provided that this work is a proof of concept, the PA should be easy to analyse and characterise to facilitate the study of the ageing effects over the PA performance. Moreover, power dissipation in Class A and AB power amplifiers is higher than in other operation modes, making it easier to monitor the device with temperature sensors. Therefore, the PA will be biased to work in between class A and AB operation modes.

In conclusion, a single-transistor, single-stage, common-source class A power amplifier has been the chosen topology for this work.

3.2.2 Technical specifications

The power amplifier has been designed to accomplish a series of basic requirements. Since it is a proof of concept, there are no imposed PA performance specifications. However, a few technical specifications have been determined in order to bound the design of the PA.

The PA topology itself will limit the maximum achievable PA power gain. Given that is is a single transistor amplifier, high gain values cannot be reached. Therefore, to set a realistic value, a power gain between 5 and 10 dB has been aimed.

As frequency band is concerned, the PA will be tuned at a widely used frequency: 2.45 GHz. This frequency corresponds to the center of a popular ISM band used in many communication protocols such as WiFi, Bluetooth, ZigBee, etc.

Regarding the maximum deliverable power. The PA should be able to provide a maximum power between 10 and 20 dBm to a $50\,\Omega$ load. Similar power values are defined in the already mentioned protocols specifications (i.e., Class 1 Bluetooth devices [6]).

Finally, there are no specifications about power efficiency and linearity. It is already assumed that, working in class A-AB operation modes, the PA will present a quite linear response and a power efficiency between 25 and 50%.

3.2.3 Design for nominal conditions

The saturated power equation (3.1) has been used to calculate the necessary peak current value to deliver a maximum output power of 20 dBm (assuming a sine is applied to the amplifier input). Considering that the load has an equivalent impedance of $50\,\Omega$ and $V_{DD} = 3.3\,\mathrm{V}$, a current peak value I_{peak} of 65 mA is necessary. The decoupling capacitor C_{DC} (Fig. 3.1) will remove the DC component of the current flowing through the load, therefore it can achieve both positive and negative values. To guarantee that negative values can reach the calculated I_{peak}, bias current should be, at least, equal to 65 mA.

The gain of the amplifier will be determined by its MOS transconductance parameter g_m, and consequently by its overdrive voltage V_{OD} and bias current I_{BIAS}. Regarding V_{OD}, it will depend both on I_{BIAS} and transistor aspect ratio $\frac{W}{L}$. An important trade-off must be considered in this situation:

- For a fixed I_{BIAS} value, large transistor aspect ratios would be translated into small overdrive voltages, increasing the PA power gain. However, as

higher the MOS dimensions, higher their parasitic capacitances. Large parasitic capacitors can lead to unstability problems, as well as complicate the PA tuning.

- For a fixed $\frac{W}{L}$ aspect ratio, increasing I_{BIAS} current (up to the already calculated limit I_{peak}) will be translated into a V_{OD} increment, also boosting the PA gain. On the contrary, lowering I_{BIAS} value will limit the negative amplitude of the current through the load, reducing the maximum delivered power and PA gain.
- The PA will be more sensitive to ageing effects if the MOS is working in weak or moderate inversion level than in strong inversion. Threshold voltage variations caused by ageing effects will produce a higher impact in V_{OD}, and consequently in the PA gain. Therefore, it will facilitate the observation of the PA performance degradation.

Thus, there is a compromise between the power amplifier gain and its sensitivity to ageing effects. In order to be able to externally adjust I_{BIAS}, the PA has been biased with a current mirror structure (Fig. 3.5) controlled with a voltage source. By default, this will be adjusted to drive a current of I_{BIAS} = 34 mA, delivering a theoretical maximum output power of 14.6 dBm and biasing the transistor with an overdrive voltage V_{OD} of approximately 400 mV. In the case that PA is too robust against ageing effects, it will be possible to decrease I_{BIAS} value, reducing the MOS overdrive voltage V_{OD} and increasing PA ageing sensitivity.

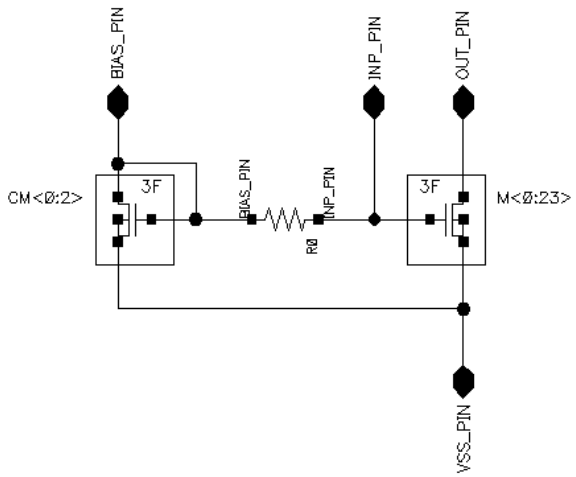

Figure 3.5: PA current mirror

Regarding the RF choke inductor, its purpose is to keep the current as constant as possible, acting as a DC current source. For this, the inductor must ideally behave as an open circuit at high frequencies, which means that $L_{RF_{choke}}$ equivalent impedance at high frequencies should be, at least, from 10 to 20 times larger than R_L. As it will be explained in further sections, choke inductor and impedance matching networks have been implemented off-chip.

By implementing the inductance externally, this can have a larger value than if it was implemented on-chip. Consequently, it is possible to use inductances able to withstand large current values. This is essential, since the PA drain current will increase during the stress. For this reason, $L_{RF_{choke}}$ has been set to 60 µH.

Regarding input and output impedance matching networks, these have been implemented with LC circuits (Figure 3.6). In the case of the output matching network, the RF choke inductor has been used as a part of the LC structure. Series resistors R_{in} and R_{out} have been added to enhance the PA stability (this will be explained in the following section). Table 3.1 summarizes the values of current mirror MOS transistors, choke inductor and both matching network components.

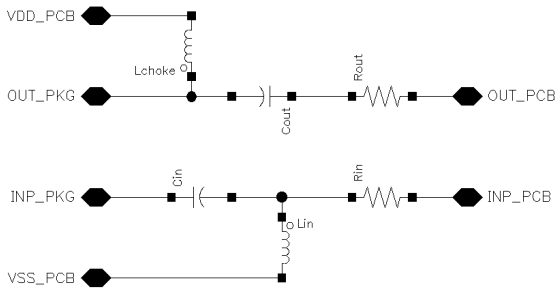

Figure 3.6: Externally implemented input and output impedance matching networks

Component	Value
CM_{mirror}	W = 124 µm, L = 0.35 µm
M_{mirror}	W = 1000 µm, L = 0.35 µm
L_{choke}	60 nH
C_{out}	1.1 pF
R_{out}	1 Ω
L_{in}	4 nH
C_{in}	0.75 pF
R_{in}	1 Ω

Table 3.1: Summary of PA components values

Finally, Figure 3.7 shows a hierarchical view of the designed power amplifier. PA_PCB block contains the input and output impedance matching networks, including the choke inductor. Bond wire connections between the integrated circuit package pins and the die pads are implemented within PA_PKG block and PA_XIP comprehends the power amplifier core.

PA_XIP is formed by the current mirror (PA_CORE), a decoupling capacitor connected between supply voltage and ground (PA_DECAP), PA_FBACK and PA_PAD blocks. These last two will be explained in the following sections.

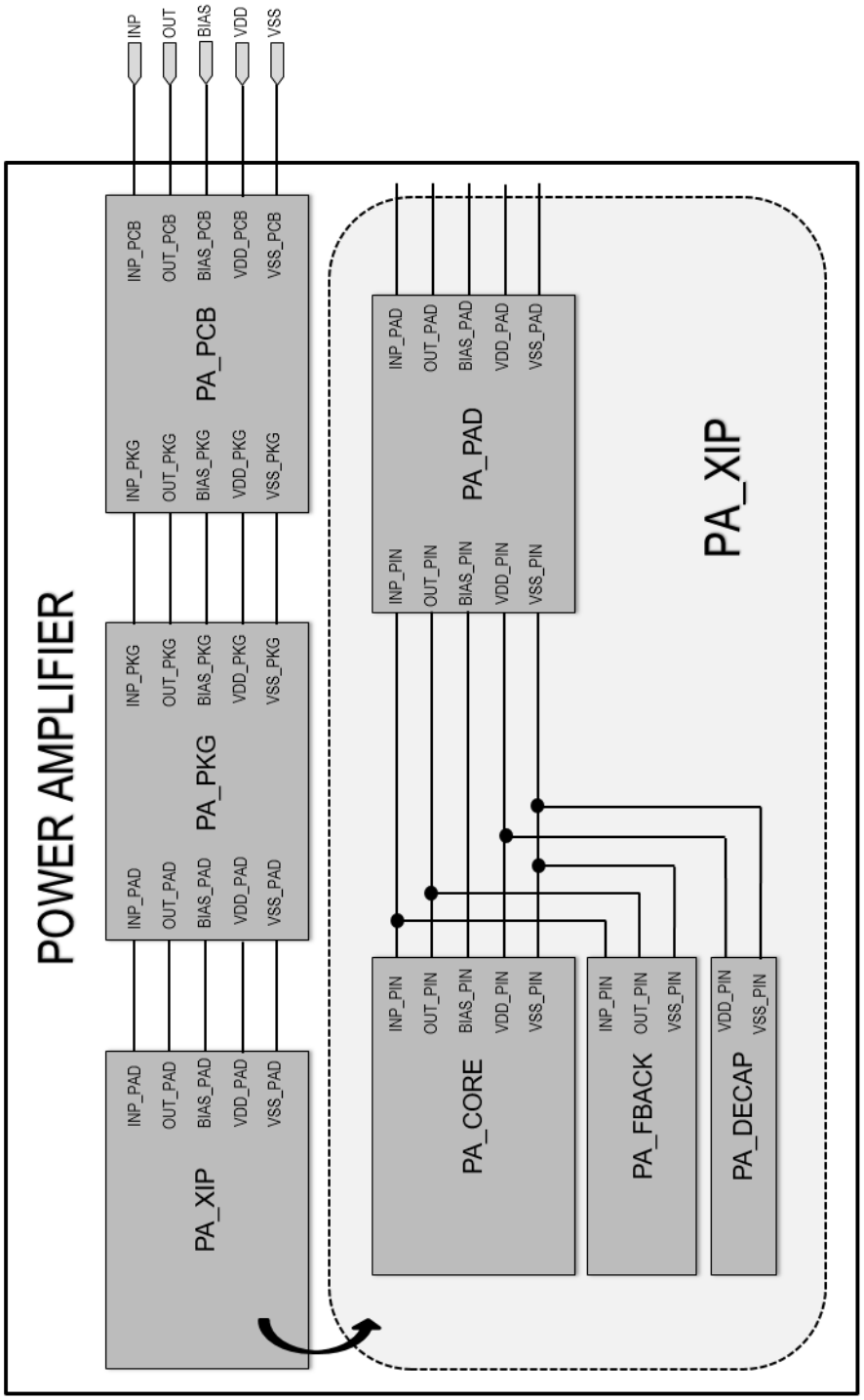

Figure 3.7: Power amplifier hierarchical view

3.2.4 Stability considerations

Stability is a major concern for any type of PA and microwave amplifier. It is normally defined with parameters K_f, also called Rollet factor, and B_{1f}:

$$K_f = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{21}||S_{12}|} \tag{3.5}$$

$$B_{1f} = 1 + |S_{11}|^2 - |S_{22}|^2 - |D|^2 \tag{3.6}$$

$$D = |S_{11}||S_{22}| - |S_{21}||S_{12}| \tag{3.7}$$

These expressions are based on the two-port equivalent S-parameters of the amplifier, and thus it is assumed that it has a linear behavior. Therefore this analysis has some limitations since the PA may work in non-linear conditions. Nevertheless, it provides a good approximation of the amplifier stability. The PA can be considered unconditionally stable when K_f factor has a value higher or equal to 1, and B_{1f} is higher than 0, as pointed out by [7]. Unconditional stability will make sure PA is stable over a wide enough frequency range, for every possible source and load termination.

Parasitic and bypass capacitors are a typical source of RF power amplifier instabilities. For instance, the loop formed by the gate-to-drain parasitic capacitor (C_{gd}) along with the drain choke inductor is a potential source of stability problems. Also, source degeneration caused by inductances in the ground path is usually taken into account when designing a PA. These inductances are introduced by the bondwires that connect integrated circuit (IC) pads with package pins.

Some solutions are commonly implemented to ensure the PA stability. For instance, cascode topologies isolate input and output terminals of the amplifier, reducing the effect of C_{gd} parasitic capacitor. Another solution is to add resistors to the loops that cause instability (e.g. connect a resistor between gate and drain terminals). Adding resistors will introduce power losses and the PA gain will be reduced, however, stability figure will improve. It is possible to limit the effect of the resistor to low or high frequencies adding a capacitor in parallel or series, respectively. Finally, in order to lessen the unwanted source degeneration caused by bondwire inductances, several pads can be connected to ground. Connecting several pads to ground reduces the total parasitic inductance value, minimising source degeneration and again, making the PA more stable.

In our case, the PA has a simple common-source single-transistor topology. Therefore, the effect of C_{gd} capacitor has a non-negligible impact on the PA stability performance and should be taken into account. Figure 3.8 (dashed line) shows K_f parameter in the frequency range 1.75 - 4 GHz. Stability factor K_f values are below 1, hence the PA is not unconditionally stable.

The lack of a cascode structure has been compensated implementing a feedback path between MOS gate and drain terminals (PA_FBACK, Fig. 3.7). This feedback path is formed by a resistor in series with a capacitor. The series resistance reduces the equivalent output resistance of the PA, which is translated into a gain reduction but at the same time the system stability is improved. Series capacitor limits the low resistance effect to high frequencies. The solid line of Figure 3.8 represents K_f parameter once the feedback has been added (R = 200 Ω, C = 20 pF). As it can be observed, K_f factor is higher than 1, and the PA is unconditionally stable for the analysed frequency range.

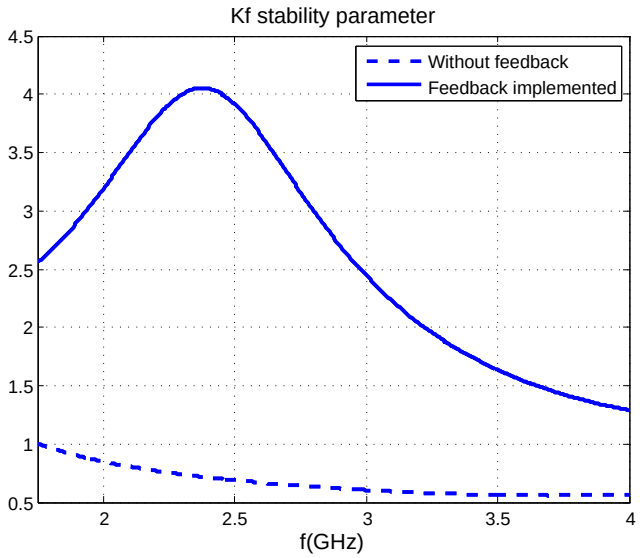

Figure 3.8: Effect of the feedback path on the PA stability

Also, small resistors have been connected in series with input and output impedance matching networks (PA_PCB, Fig. 3.7). These resistors introduce losses over the entire frequency range, improving PA stability. Figure 3.9 shows K_f factor for frequency values from 0.2 to 6 GHz. The stability enhancement effect of resistor losses can be clearly noticed , especially in the frequency ranges 0.2-1.5 GHz and 4-6 GHz.

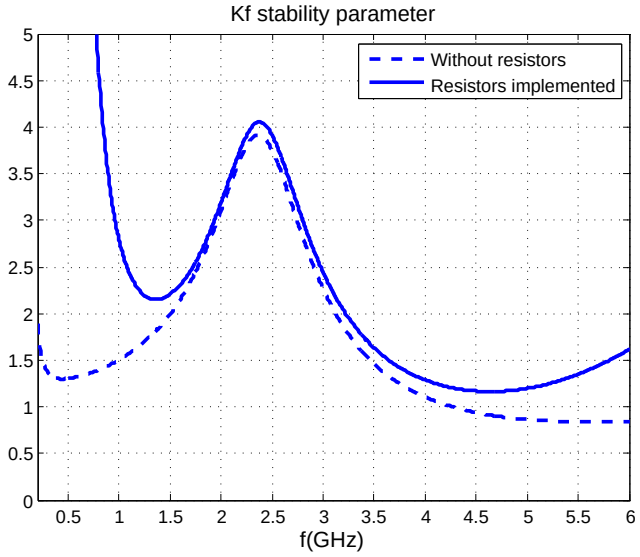

Figure 3.9: Effect of the resistor loses on the PA stability

Finally, up to five pads have been connected to ground in order to minimise

the source degradation introduced by the bondwire parasitic inductances (PA_PKG, Fig. 3.7).

3.2.5 Stress and protection

The designed PA will be stressed by increasing its supply voltage. Consequently, its bias current will increase. It is, however, impossible to predict the exact amount of current that will flow through the device, mainly because AMS 0.35 µm available MOS transistor models are not valid for drain voltage values higher than 3.6 V. Moreover, we found out that the MOS DC simulation results were different depending on which of the models provided by the foundry were used. There are two NMOS transistor models (nmos4 and nmosrf, which includes parasitic RF components) and two simulation models (BSIM3v3 and HiSIM2). Figure 3.10 shows the NMOS drain current I_D as a function of V_{DS} for each one of the combinations. As it can be observed, only HiSIM2-nmos4 and HiSIM2-nmosrf permutation are identical.

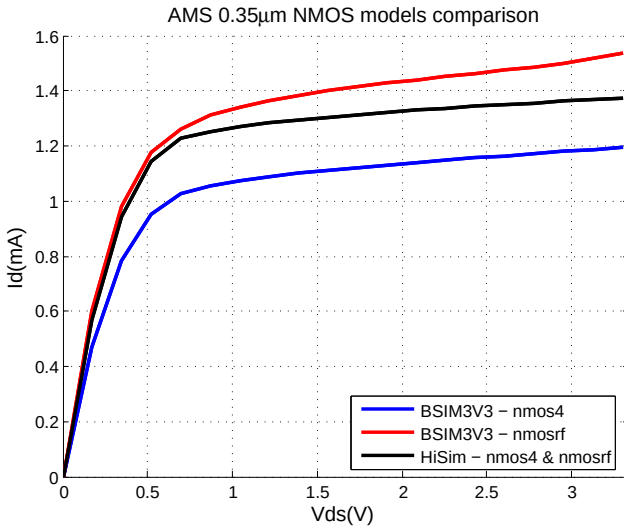

Figure 3.10: AMS 0.35 µm NMOS models comparison, $V_g = 1.5$ V, W = 10 µm, L = 0.35 µm

In any case, high current values are expected during stress mode. Drain current I_D will have a value of 34 mA with the PA operating at nominal conditions ($V_{DD} = 3.3$ V), but it could reach values of several hundreds of mA during the stress. Taking this into account, the design of the PA has been tailored to handle large current values, as it is explained below.

Inductance models provided by the foundry are not capable of withstanding I_D values of hundreds of mA and therefore cannot be used in this work. Designing our own inductance is neither a suitable solution in terms of layout area and cost. Instead, the choke inductor has been implemented off-chip. Also, input and output impedance matching networks have been externally implemented. Using off-chip inductors and capacitors permit us to use models that can resist large current values. It is also an advantage in terms of matching

and tuning, because these can be modified in case the measured PA performance differs from the expected due to process variations or components tolerances. Regarding the NMOS transistor, its layout has been designed focusing on maximising the current that can flow through the device.

The terminals of an IC are usually protected in order to improve circuit reliability and safety. Protection is achieved adding ESD (electrostatic discharges) diodes. There are pad cells in AMS 0.35 µm libraries that already include these type of diodes. For instance, Figure 3.11 shows the schematic of a pad (APRI0P cell). As it can be seen, pad input voltage (PAD pin) is limited to $V_{DD} + V_f$ and $-V_f$, where V_f is the diode forward voltage. In case the voltage at the PAD pin is higher or lower than the limits, diodes will start to conduct, preventing the circuit from being damaged. In this work, however, input and output supply voltage terminals have not been protected. The reason is that we must increase V_{DD} supply voltage to stress the PA, and also we need to be able to increase the RF input signal power. Protection pads are implemented in the PA_PAD block of Figure 3.7.

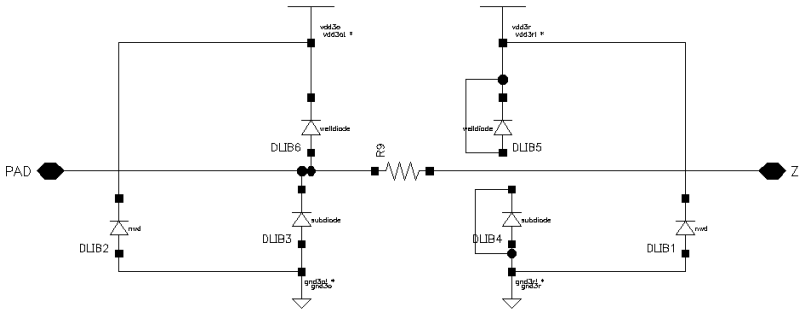

Figure 3.11: AMS 0.35 µm PAD with ESD protection model *APRIOP*

3.3 Simulation results

S-parameters are represented in figures 3.12 and 3.13. The power gain, represented by S_{21} (Fig. 3.13) reaches a maximum value of 6.9 dB at the working frequency 2.45 GHz. Input and output impedance matching represented by S_{11} and S_{22} (Fig. 3.12) are below -20 dB for the frequency range 2.3 GHz - 2.5 GHz, ensuring all the input signal power is transfered from the source to the PA, and from the PA to the load. Output to input isolation S_{12} values (Fig. 3.13) are below -20 dB over the entire frequency band.

The designed PA is unconditionally stable. Stability factors K_f and B_f are higher than 1 and 0, respectively, in the whole frequency range, as it is shown in Figure 3.14

Figure 3.15 represents the output power P_{OUT} as a function of the RF input signal power P_{IN}. Power gain is kept 6.9 dB for input power values lower than 13.55 dBm. Figure 3.16 shows the power gain figure as a function of input power P_{IN}. Again, the PA power gain starts decreasing for P_{IN} values above 13.55 dBm. From these two figures it can be concluded that the input referred 1 dB compression point (P_{1dB}) is 13.55 dBm.

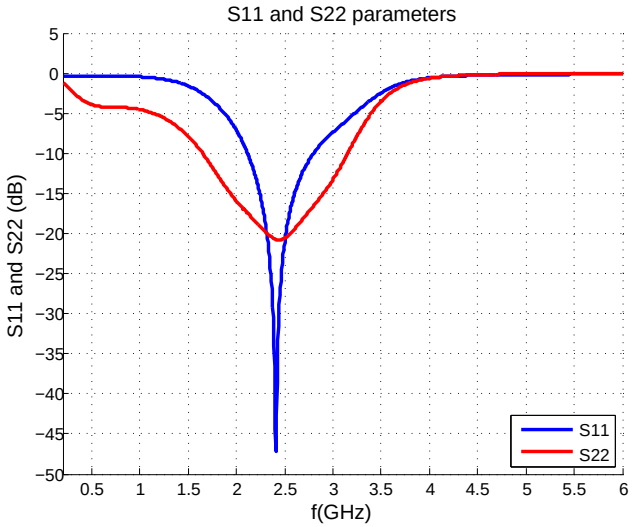

Figure 3.12: PA S11 and S22 parameters

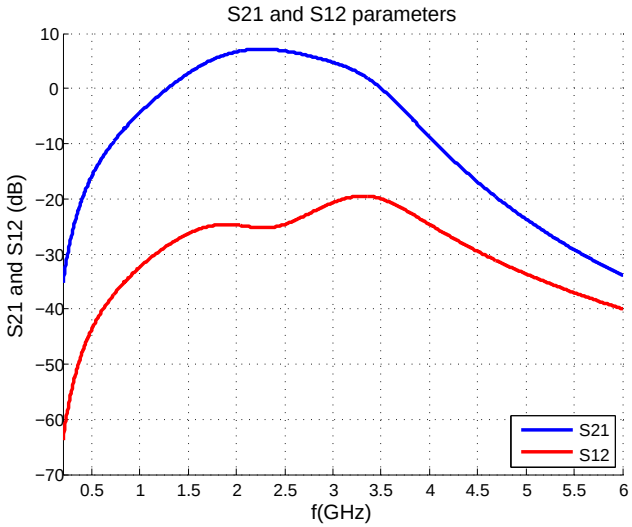

Figure 3.13: PA S21 and S12 parameters

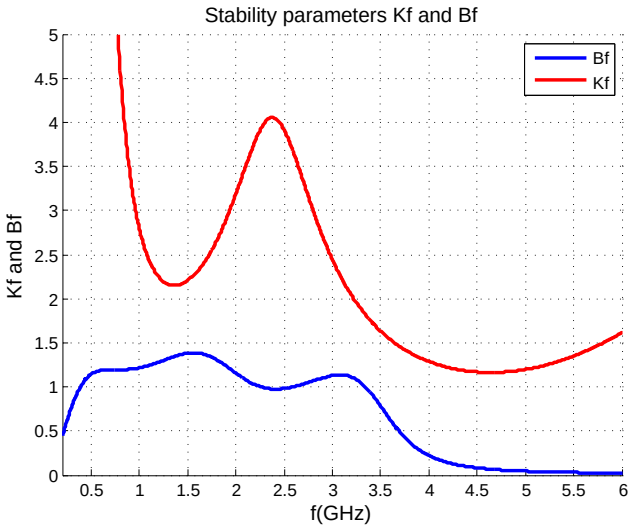

Figure 3.14: PA stability parameters K_f and B_f

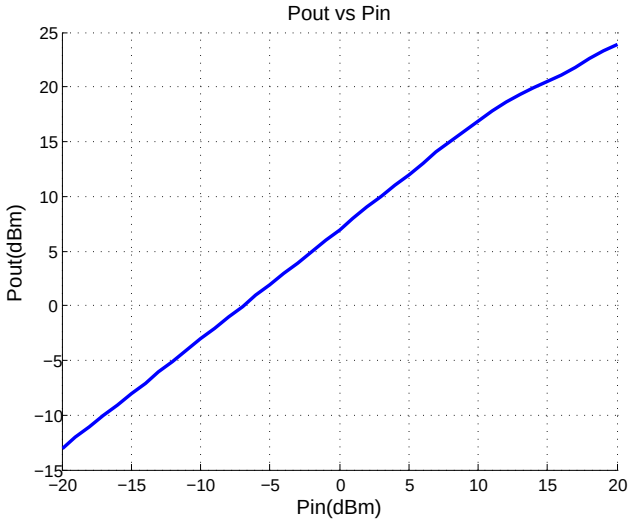

Figure 3.15: PA power output as a function of input power

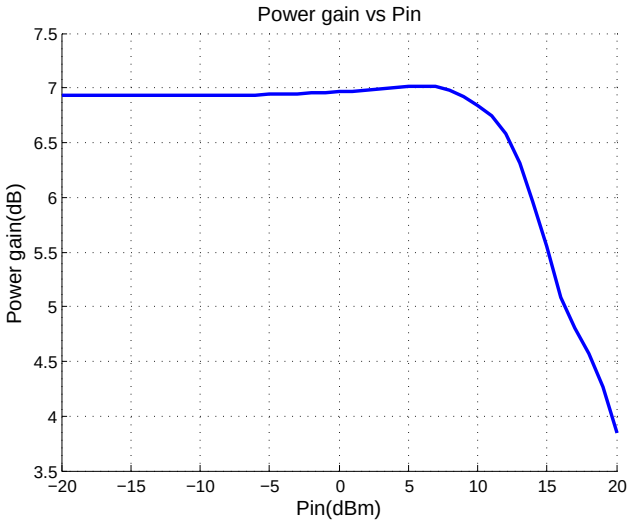

Figure 3.16: PA power gain as a function of input power

3.4 Conclusions

The design of the power amplifier stage has been explained in this chapter. Fundamental knowledges about power amplifiers have been given in the first section, comprehending PA operation principle and basic topology (Figure 3.1), operating classes (from class A to class F), comparison (Figures 3.2 and 3.3) and performance metrics.

Then, these theoretical fundaments have been used to justify the technical specifications and chosen topology of the PA. The design procedure has been divided in three parts and the PA nominal design has been complemented with stability and stress considerations: extra circuitry has been added in order to improve the stability of the amplifier (Figures 3.8 and 3.9), and impedance matching networks and choke inductor have been implemented off-chip to withstand the expected large current values during the PA stress (Figure 3.6).

Simulation results have been shown in section 3.3. The typical PA figures of merit such as input and output matching parameters S_{11} and S_{22}, gain and isolation S_{21} and S_{12}, power gain G_P and P_{1dB} have been reported for the chosen PA bias condition in figures from 3.12 to 3.16. The designed PA accomplishes with the required specifications, presenting a power gain of 6.9 dB at 2.45 GHz, and delivering a maximum output power of 14.6 dBm when biased with $I_{BIAS} = 34\,\text{mA}$.

3.5 References

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CHAPTER 4

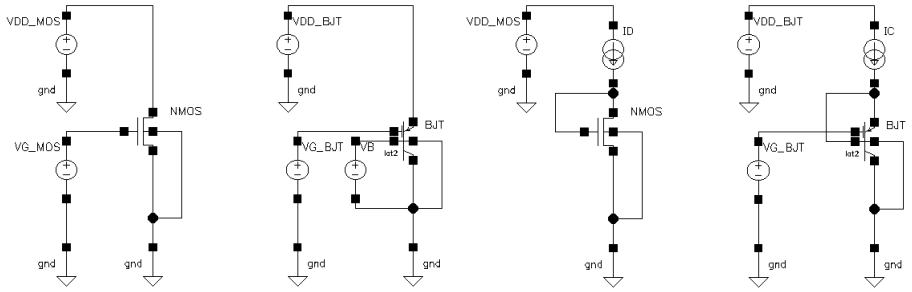
Temperature Sensors

Temperature sensors are specially used in microprocessors and other high performance digital integrated circuits (IC) where high heating values can be reached due to the components density and their power dissipation. By monitoring the temperature of an integrated circuit, it is possible to make a diagnose and protect it against potential overheating issues, for instance, switching it off, reducing its clock frequency or activating a cooling system. In RF front-ends, thermal sensors have been proposed to indirectly observe circuit characteristics such as gain [1], bandwidth and central frequency [2] or 1 dB compression point [3] without electrically loading any circuit node.

In relation to the goal of this work, the use of on-chip temperature sensors makes possible to detect temperature changes in the power amplifier. It has already been demonstrated that temperature changes in a PA are related with its power dissipation (chapter 2, section 2.3), and consequently can be related with the power gain. Taking this into account, it is possible to monitor and characterise the performance of the PA, since every variation on its power gain value will be translated into a variation in the output signal of the temperature sensor.

Designing integrated temperature sensors is a very mature art, and therefore it is possible to find a vast amount of information about different possible topologies. Even so, most of the temperature sensor structures can be splitted in two clearly distinguished parts no matter how complicated it is. On the one hand there is the transducer in charge of converting temperature variations into electrical signal variations, and in the other hand there is a conditioning circuit with the purpose of detecting and amplifying this electrical signal. While the conditioning circuit could be either very simple or extremely complex, the transducer block will be the same in both cases providing that we are using the same temperature-sensitive component. As a consequence, in case we want to compare two sensor topologies with the same conditioning circuit but different transducers, it would be only necessary to decide which transducer is better in terms of sensitivity.

In this chapter, two temperature sensor topologies are presented. Firstly, a comparison between the use of MOS transistors and BJT transistors as



(a) Schematic of MOS and BJT transistors configured as a current source

(b) Schematic of MOS and BJT transistors configured as diode

Figure 4.1: MOS and BJT temperature transducers configurations

transducers is presented with the aim of decide which one presents a better thermal sensitivity. Then a differential conditioning circuit is proposed to work with each one of them.

4.1 Comparison between MOS and BJT temperature transducers

Two configurations are typically used with MOS or bipolar transistors operating as temperature transducers.

The first one is a transistor used as a current source with a fixed V_{GS} or V_{BE} (Fig. 4.1.a). With this configuration current variations can be directly related to temperature changes and thus the transistor sensitivity is expressed as $S(nA/K)$. The second configuration consists on connecting the gate and drain (or base and emitter) of the transistor and bias it with a fixed current (Fig. 4.1.b). This diode structure permits to measure V_{GS} or V_{BE} voltage as an output and relate its variations with temperature. In this case, the transistor temperature sensitivity is expressed as $S(mV/K)$.

The following section presents an analysis in order to obtain both sensitivity expressions $S(nA/K)$ and $S(mV/K)$ for MOS and BJT transistors and determine which parameters determine them. The validity of these expressions is proved with simulation results.

4.1.1 MOS sensitivity S(nA/K) analysis

The starting point is the expression of the transistor current working in strong saturation, neglecting short-channel effects and body effect. Mobility and threshold voltage are expressed taking into account temperature effects. The approximated values of α and β are taken from [4] based on simulations using AMS 0.35 µm technology :

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{\alpha} \qquad V_T = V_{T0} + \beta(T - T_0) \tag{4.1}$$

$$\alpha = -1.8 \qquad \beta = -1.1\,\mathrm{mV/K} \tag{4.2}$$

Then, the expression (4.3) is derived with respect to temperature, and again, few assumptions (4.5) are made in order to have a more simplified result.

$$I_D = \frac{1}{2}\mu_0 \left(\frac{T}{T_0}\right)^{\alpha} C_{ox}\frac{W}{L}(V_{GS} - V_{T0} - \beta(T - T_0))^2 \tag{4.3}$$

$$\frac{\partial I_D}{\partial T} \simeq \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}[\frac{\alpha}{T_o}\left(\frac{T}{T_0}\right)^{\alpha-1}(V_{GS} - V_{T0} - \beta(T - T_0))^2 + \left(\frac{T}{T_0}\right)^{\alpha} 2(-\beta)(V_{GS} - V_{T0} - \beta(T - T_0))] \tag{4.4}$$

$$@T \approx T_0 \qquad \left(\frac{T}{T_0}\right)^{\alpha-1} \simeq \left(\frac{T}{T_0}\right)^{\alpha} \simeq 1$$

$$(V_{GS} - V_{T0} - \beta(T - T_0)) \simeq V_{GS} - V_{T0} = V_{OD} \tag{4.5}$$

$$\frac{\partial I_D}{\partial T} \simeq \frac{1}{2}\mu_0 C_{ox}\frac{W}{L}[\frac{\alpha}{T_o}V_{OD}^2 + 2(-\beta)V_{OD}] = I_D[\frac{\alpha}{T_o} - \frac{2\beta}{V_{OD}}] \tag{4.6}$$

Equation (4.6) allows us to compute the temperature sensitivity values of the transistor current. As it can be seen, the transistor temperature sensitivity strongly depends on $\frac{\alpha}{T_0}$ for high V_{OD} values, while for low V_{OD} it depends on $\frac{2\beta}{V_{OD}}$ and will take negative values. In the last case, however, the expression is not reliable given that MOS transistor is operating in moderate or weak inversion and the expression of its I_D current would not be accurate. Sensitivity sign varies when plotted as a function of V_{OD}, thus there is a certain V_{OD} value at which the transistor is temperature insensitive. Fig. 4.2 represents $S(nA/K)$ for several overdrive voltages and I_D currents.

In order to check the validity of the theoretical results, several simulations have been carried out configuring the transistor as a current source (Fig. 4.1.a). By changing V_{GS} voltage, V_{OD} value is swept, while I_D current is adjusted by modifying the transistor aspect ratio ($\frac{W}{L}$). Results for $I_D = 10\,\mu\mathrm{A}$ are summarized in Table 4.1 and graphically compared with the ones obtained with eq. (4.6) in Fig. 4.3. Figure 4.3 shows a desagrement lower than 10% for overdrive voltages higher than 300 mV (MOS working in strong inversion). However, for overdrives lower than 300 mV, the desagreement can reach values up to 62%, as it was expected.

Current mirror structures are commonly used for adjusting the sensitivity of a transistor just by changing its bias current. We have to take into account

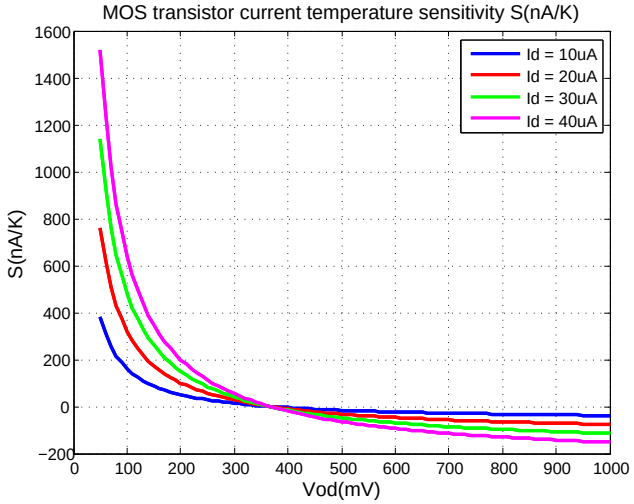


Figure 4.2: Sensitivity $S(nA/K)$ values obtained with theoretical expression (4.6) for different V_{OD} and I_D values

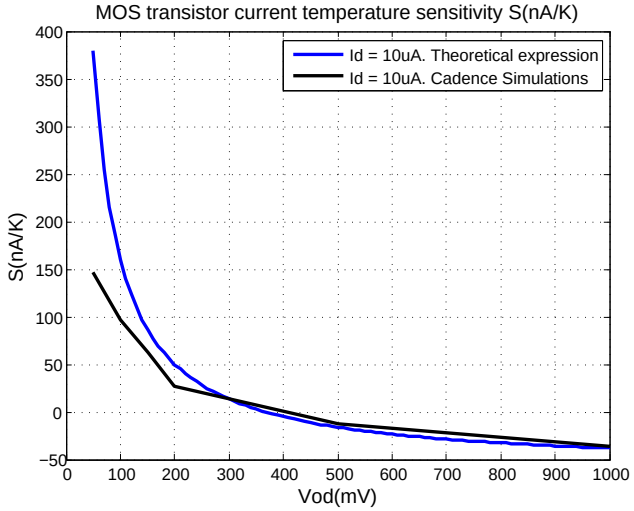


Figure 4.3: Comparison between $S(nA/K)$ values obtained with expression (4.6) and simulation results for $I_D = 10\,\mu A$

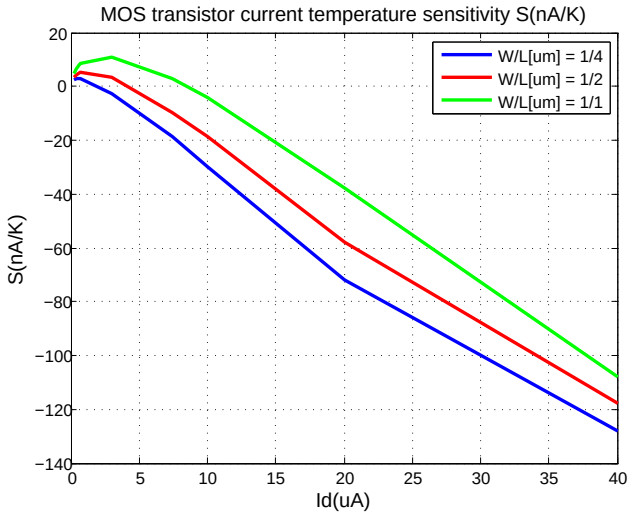


Figure 4.4: $S(nA/K)$ values obtained using a current mirror topology, I_D from 0 to 40 µA and three ($\frac{W}{L}$) aspect ratios

$I_D = 10\,\mu A$					
$V_{OD} = 50\,mV$		$V_{OD} = 100\,mV$		$V_{OD} = 150\,mV$	
Temp[K]	I_D[µA]	Temp[K]	I_D[µA]	Temp[K]	I_D[µA]
300	10	300	10	300	10
305	10.73	305	10.49	305	10.31
S[nA/K]	**147**	S[nA/K]	**97**	S[nA/K]	**62**
$I_D = 10\,\mu A$					
$V_{OD} = 200\,mV$		$V_{OD} = 500\,mV$		$V_{OD} = 1\,V$	
Temp[K]	I_D[µA]	Temp[K]	I_D[µA]	Temp[K]	I_D[µA]
300	10	300	10	300	10
305	10.13	305	9.93	305	9.82
S[nA/K]	**27**	S[nA/K]	**-13**	S[nA/K]	**-36**

Table 4.1: S(nA/K) sensitivity values obtained with Cadence simulations

though, that the transistor aspect ratio ($\frac{W}{L}$) is fixed so that I_D and V_{GS} cannot be changed independently according to eq. (4.3). An increase or decrease in I_D will be translated in a V_{OD} increase or reduction, respectively. Fig. 4.4 represents $S(nA/K)$ achievable values using a current mirror topology for three different transistor dimensions. Except for small I_D currents (lower than 5 µA), it is clear that under the same biasing scenario, wider transistors present a better temperature sensitivity since their V_{OD} is lower. In any case, the behavior of a MOS as a temperature transducer can be improved at expense of power consumption.

4.1.2 MOS sensitivity S(mV/K) analysis

A similar procedure as in section 4.1.1 is followed to find the sensitivity of V_{GS} with temperature, when the transistor is diode-connected as shown in Fig. 4.1.b. It can be obtained from (1.3) that:

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_0 \left(\frac{T}{T_0}\right)^{\alpha} C_{ox} \frac{W}{L}}} + V_{T0} + \beta(T - T_0) \tag{4.7}$$

$$V_{GS} = \sqrt{\frac{2I_D}{\mu_0 C_{ox} \frac{W}{L}}} (T_0)^{\frac{\alpha}{2}} (T)^{\frac{-\alpha}{2}} + V_{T0} + \beta(T - T_0) \tag{4.8}$$

Therefore, deriving the expression (4.8) with respect to the temperature and making some assumptions a simplified expression is obtained:

$$\frac{\partial V_{GS}}{\partial T} = \sqrt{\frac{2I_D}{\mu_0 C_{ox} \frac{W}{L}}} (T_0)^{\frac{\alpha}{2}} (-\frac{\alpha}{2}) (T)^{\frac{-\alpha}{2}-1} + \beta \tag{4.9}$$

$$\frac{\partial V_{GS}}{\partial T} = \sqrt{\frac{2I_D}{\mu_0 C_{ox} \frac{W}{L}}} (\frac{T_0}{T})^{\frac{\alpha}{2}} (-\frac{\alpha}{2}) (T)^{-1} + \beta \tag{4.10}$$

$$@T \approx T_0, \qquad (\frac{T_0}{T})^{\frac{\alpha}{2}} \approx 1 \tag{4.11}$$

$$\frac{\partial V_{GS}}{\partial T} \approx \sqrt{\frac{2I_D}{\mu_0 C_{ox} \frac{W}{L}}} (-\frac{\alpha}{2}) (T)^{-1} + \beta = \frac{-\alpha V_{OD}}{2T} + \beta \tag{4.12}$$

It is important to observe that the variation of V_{GS} with temperature only depends on the V_{OD}. This permits to easily measure temperature changes by using two diode-like MOS (Fig. 4.1.b), placing one of them near to a heat source and connecting its drain terminals to the inputs of a differential amplifier.

Again, the validity of the theoretical results has been checked with simulations. Fig. 4.5 shows a comparison between the simulation results and the values computed with expression (4.12). From it can be deduced that V_{GS} thermal sensitivity $S(mV/K)$ can be fitted to:

$$S = m \cdot V_{OD} + C \tag{4.13}$$

where $m = 0.345\,\mathrm{K}^{-1}$ and $C = 0.386\,\mathrm{mV/K}$. The dispersion of C between the simulated and theoretical data is due to the approximations done in equation (4.11).

Fig. 4.6 shows an example of the V_{OD} effect over the V_{GS} sensitivity $S(mV/K)$. The drain voltage (V_O) of a diode configured MOS with W = 1 µm and L = 16 µm has been observed for temperatures from 300 K to 353 K. Increasing the transistor current is translated into an overdrive voltage V_{OD} increase and, as it can be observed, its thermal sensitivity $S(mV/K)$ also increases. More concretely, the obtained values are 6.5 mV/K with $I_D = 20\,\mu\mathrm{A}$, 4 mV/K with $I_D = 10\,\mu\mathrm{A}$ and 2.4 mV/K with $I_D = 5\,\mu\mathrm{A}$. These results coincide with the ones of Fig. 4.5.

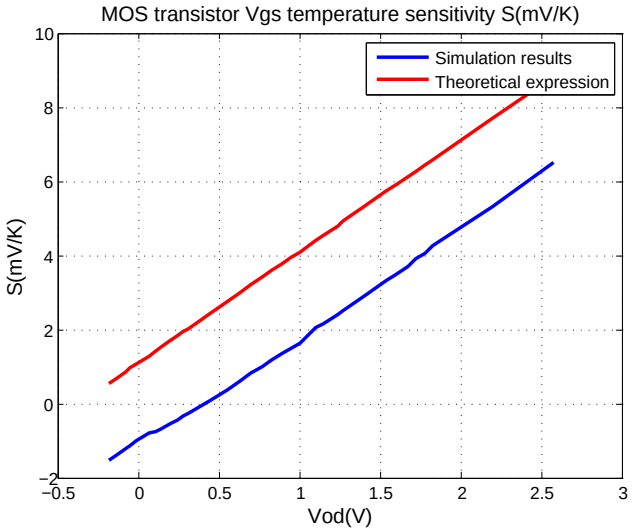


Figure 4.5: Comparison between $S(mV/K)$ values obtained with expression (1.12) and simulation results

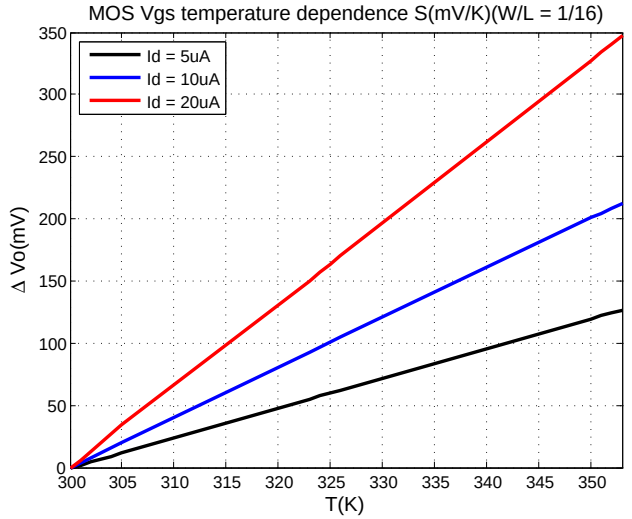


Figure 4.6: MOS transistor V_{GS} voltage for temperatures from 300 K to 353 K and three I_D current values (5 µA, 10 µA, 20 µA)

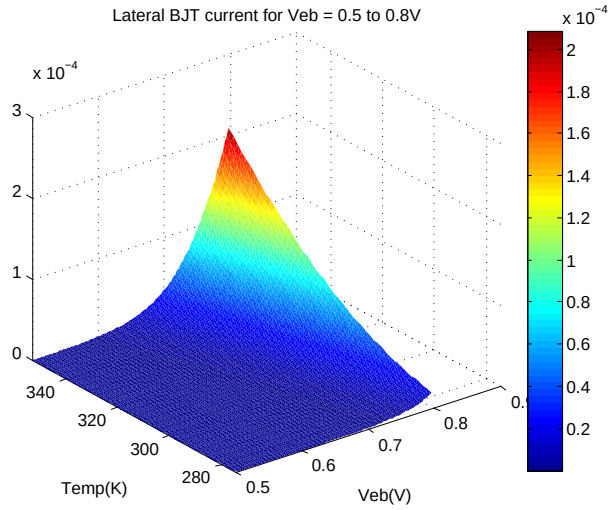


Figure 4.7: Lateral BJT I_C current values for V_{BE} values from 0.5 to 0.8 V and temperature from 273 K to 353 K

4.1.3 BJT sensitivity S(nA/K) analysis

The $S(nA/K)$ sensitivity of a bipolar transistor has been obtained configuring a lateral BJT (available in AMS 0.35 µm CMOS technology libraries) as a current source (Fig. 4.1.a) and sweeping its base-emitter V_{BE} voltage and temperature T. Note the dimensions of the BJT transistors cannot be changed now. As a result, the value of the BJT collector current I_C has been obtained for each (V_{BE}, T) point. Then, the current sensitivity $S(nA/K)$ for each V_{BE} value has been calculated deriving I_C with respect to T.

Fig. 4.7 represents the collector current I_C for V_{BE} voltage levels from 0.5 to 0.8 V and temperatures from 273 K to 353 K. while Fig. 4.8 represents the sensitivity $S(A/K)$ for the same range of V_{BE} and temperature. In this way we can associate each S(A/K) value to a temperature, V_{BE} and current consumption. Nevertheless, the simulation results lead to a set of I_C values which are not realistic (up to 200 µA) for our design, and thus no useful information can be obtained. In order to do a more precise analysis $I_C(V_{BE}, T)$ and S(V_{BE}, T) data has been limited to current consumption values from 0 to 20 µA. Then these data has been plotted using a heat map as shown in Fig. 4.9 and Fig. 4.10.

As it can be observed by comparing both figures, the current sensitivity $S(A/K)$ of the BJT transistor is constant for the whole temperature range and a fixed I_C current. This means that sensitivity only depends on the base-emitter voltage V_{BE} and by consequence, on the collector current. Taking this into account it is possible to represent the S(I_C) dependence (Fig. 4.11).

Sensitivity values go from 0 to 780 nA/K for current values from 0 to 20 µA, and the dependence of $S(nA/K)$ with I_C can be approximated by a straight line with a slope of 40 mK^{-1}. This result facilitates the use of the current source configured BJT transistor as a temperature sensing device since it only has

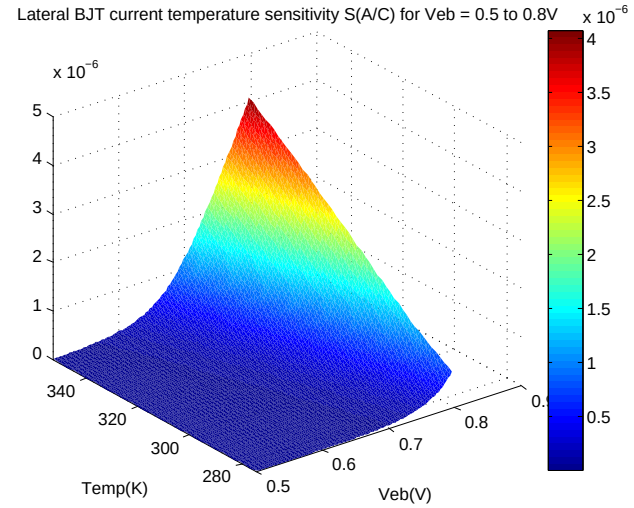


Figure 4.8: Lateral BJT I_C current thermal sensitivity values for V_{BE} values from 0.5 to 0.8 V and temperature from 273 K to 353 K

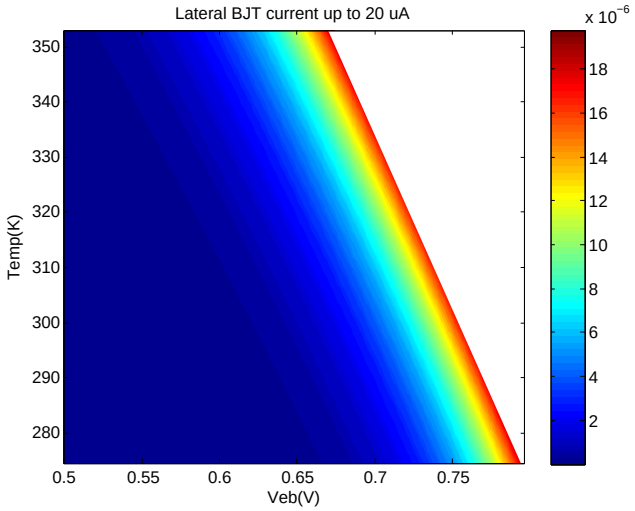


Figure 4.9: Lateral BJT I_C current for V_{BE} values from 0.5 to 0.8 V and temperature from 273 K to 353 K. I_C current limited to 20 µA

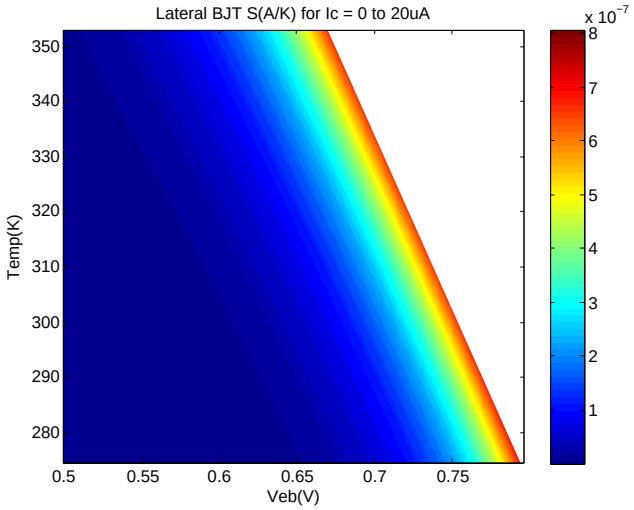


Figure 4.10: Lateral BJT I_C current thermal sensitivity values for V_{BE} values from 0.5 to 0.8 V and temperature from 273 K to 353 K.I_C current limited to 20 µA

one degree of freedom (V_{BE}) and thus it can be easily adjusted and controlled fixing its base-emitter voltage with, for exemple, a voltage source connected to its base.

4.1.4 BJT sensitivity S(mV/K) analysis

In order to analyse the base emitter voltage dependence with temperature $S(mV/K)$ a BJT transistor has been configured as a diode connecting its base terminal to the collector (Fig. 4.1.b). In this way, if the BJT emitter is tied to a known voltage i.e, to ground, its V_{BE} voltage can be directly measured at the collector terminal.

Using this topology it is possible to observe the variation of V_{BE} with temperature for a given I_C current. Simulation results have been obtained for three different I_C values (5 µA, 10 µA, 20 µA) and temperatures from 300 K to 353 K (Fig. 4.12). Results show a small variance in the sensitivity $S(mV/K)$ between different I_C currents. More concretely,the BJT presents a V_{BE} thermal sensitiviy of -1.72 mV/K when $I_C = 5$ µA, -1.67 mV/K when $I_C = 10$ µA and -1.62 mV/K when $I_C = 20$ µA. In this case, increasing the current, and thus the power consumption, will not provide a better thermal sensitivity.

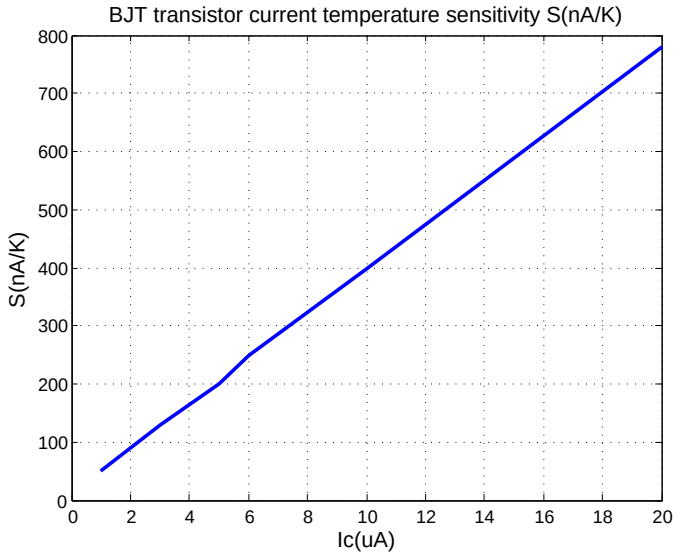


Figure 4.11: Lateral BJT transistor $S(nA/K)$ values for I_C currents from 0 to 20 µA

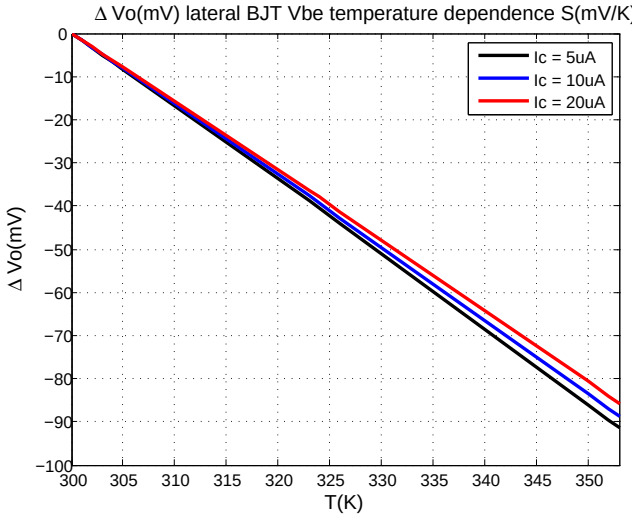


Figure 4.12: Lateral BJT transistor V_{BE} voltage for temperatures from 300 K to 353 K and three I_C current values (5 µA, 10 µA, 20 µA)

4.1.5 Conclusions

To point out which device is better in terms of thermal sensitivity is possible by comparing the obtained results. There are, however, two possible configurations to bias the transconductor, and thus two figures of merit that should be compared: $S(mV/K)$ and $S(nA/K)$, and it may happen that depending on the application one transistor is a better solution than the other.

In the case of voltage-mode biasing (output variable is current, sensitivity is $S(nA/K)$), the maximum achievable value using a MOS transistor in weak inversion is 150 nA/K for a current of $I_D = 10\,\mu A$ (Fig. 4.3) while using a lateral BJT a sensitivity of 400 nA/K is achieved with the same current consumption (Fig. 4.11). The lateral BJT is a better choice if we want to measure temperature changes by observing current variations.

Nevertheless, temperature changes can also be detected using a current-mode biased transistor and observing its collector (BJT) or drain (MOS) voltage. The lateral BJT available in AMS 0.35 µm technology libraries shows a V_{BE} thermal sensitivity among -1.72 mV/K and -1.67 mV/K (Fig. 4.12) for collector currents from 5 µA to 20 µA. In turn, using a MOS it is possible to easily achieve higher $S(mV/K)$ values since not only the current I_D can be adjusted but also its overdrive voltage V_{OD} by making it bigger or smaller. For example a sensitivity of S = 4 mV/K is obtained with $I_D = 10\,\mu A$, W = 1 µm and L = 16 µm (Fig. 4.6).

4.2 Design of the conditioning circuits

Two conditioning circuits have been designed in order to use MOS and BJT transistors as temperature transducers. Considering that a sensor is formed by a transducer (e.g. temperature to current) and a conditioning circuit, it will be possible then to compare two temperature sensors based in MOS and BJT sensing devices, respectively.

The proposed conditioning circuits are basically operational transconductance amplifiers (OTA)(Fig. 4.13 and Fig. 4.14) which are able to convert temperature changes into voltage variations. Their working principle is as follows:

The OTA differential pair is composed either by two identical lateral BJT transistors with common base terminals (T_1 - T_2) or by two identical MOS transistors with common gate terminals (T_3 - T_4). In both cases, BJT and MOS transducers are biased with the same operating point and the sum of current across them I_{BIAS} is fixed with a current source.

The current across temperature transducers is copied to the output node with current mirrors. M_1 - M_3, M_2 - M_4 and M_5 - M_6 in the case of BJT based topology. M_7 - M_9, M_8 - M_{10} and M_{11} - M_{12} in the case of MOSFET based topology.

When no temperature difference is presented between temperature transducers, their current is $I_{BIAS}/2$ and the voltage at the output node is fixed to a certain value. Whenever one of the transducers temperature increases or decreases, a current imbalance is generated and propagated to the output node with the above mentioned current mirrors. Finally, this current imbalance changes the output voltage value.

Considering current mirrors are perfectly matched, the variation in the output voltage ΔV_{out} is determined by the transducers current sensitivity $S(nA/K)$, the equivalent output resistance r_{out} at node V_{out}, and current mirrors aspect ratio 1:N as follows:

$$\Delta V_{out} = S(nA/K) \cdot r_{out} \cdot N \tag{4.14}$$

The DC value of V_{out} depends on the transistors dimensions and also on the current I_{BIAS}. More concretely, its value is fixed by $V_{DD} - V_{GS_{M_5}}$ (or $V_{GS_{M_{11}}}$, Fig. 4.14). However, given that V_{out} is a high impedance node, mismatch effects can produce large voltage variations. In order to compensate offset variations and adjust the V_{out} DC voltage value, two extra current sources I_N and I_P have been implemented. By changing its value, a certain amount of current is added or subtracted from the transducers branch, forcing a current imbalance and changing the DC value of V_{out}.

Finally, the bandwidth of the OTA is determined by the pole at the output node, and it is expressed as:

$$BW_{OTA} = \frac{1}{2\pi \cdot r_{out} \cdot C_{out}} \tag{4.15}$$

Where r_{out} is the equivalent output resistance and C_{out} is the sum of all the capacitances at the output node.

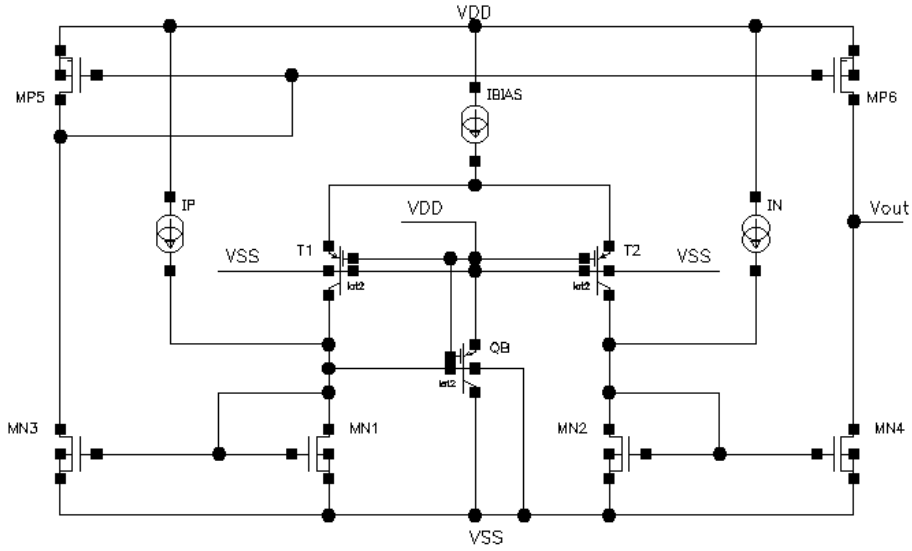


Figure 4.13: Conditioning circuit for BJT temperature transducers

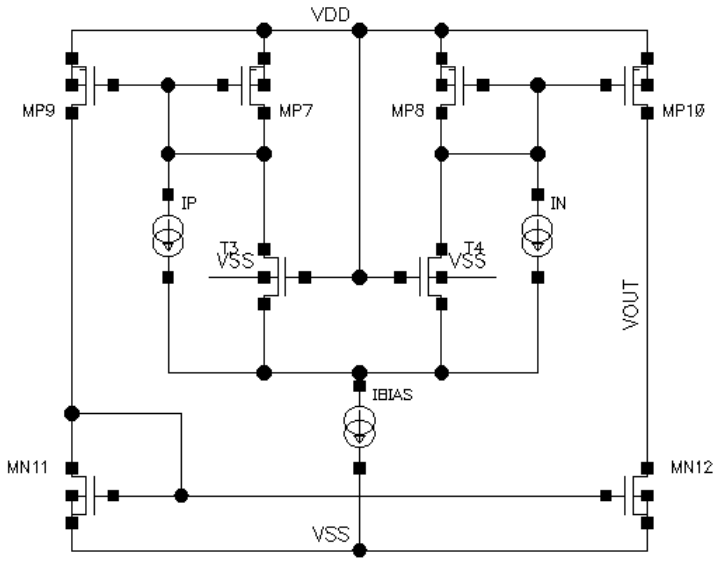


Figure 4.14: Conditioning circuit for MOS temperature transducers

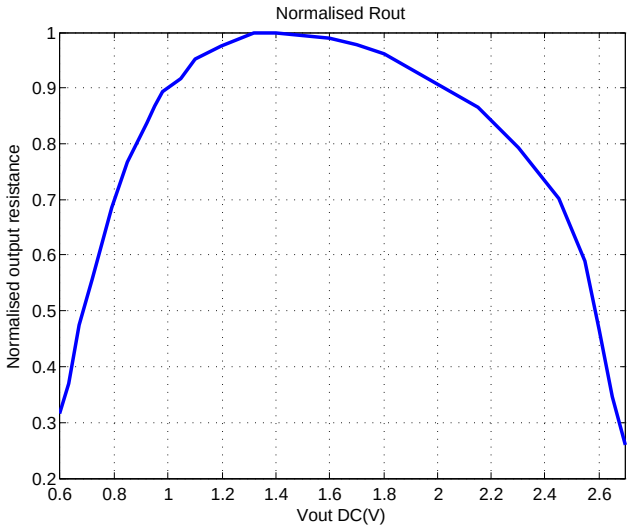


Figure 4.15: Normalised r_{out} output resistance as a function of V_{out}

4.2.1 Design of the BJT Differential conditioning circuit

The design of the BJT based differential topology has been aimed to obtain the maximum gain as possible in order to detect small temperature variations with an acceptable resolution. The following key issues arised during the design process.

The output ΔV_{out} slope is determined by the transducers sensitivity $S(nA/K)$ and the equivalent output resistance r_{out}. Transducers sensitivity depends on the bias current I_{BIAS}: the higher the BJT collector current the better its current thermal sensitivity.

At the same time, biasing current affects on opposite ways the sensor sensitivity. On the one hand, the term $S(nA/K) \cdot N$ of expression (4.14) increases with high current mirror ratio N values. On the other hand, the output resistence increases with small M_6 - M_4 I_{DS} current. For this reason, a current mirror ratio of 1:1 has been chosen for simplicity.

In order to simulate our circuit, we have used the lateral BJT transistor provided by the AMS 0.35 µm CMOS technology library (simulation models are provided for this transistor). In this device, all dimensions are already set. Nevertheless, the width and length of all the MOS transistors can be adjusted. Increasing the length of both NMOS and PMOS transistors implies a growth in r_{out} and thus in ΔV_{out} sensitivity. There is however, a trade-off between the sensor total area and the improvement in r_{out}. Taking this into account we have decided that the length of NMOS and PMOS is 40 µm and 25 µm, respectively.

Figure 4.15 shows the normalised output resistance of the circuit as a function of V_{out}. According to the results, higher r_{out} values are reached in the range of V_{out} from 1.2 V to 1.8 V. Taking this into account, maximum output sensitivity values will be achieved with V_{out} values around $V_{DD}/2$. Table 4.2 summarises the transistors dimensions of the sensor.

Component	Width (µm)	Length (µm)
M_1	2	40
M_2	2	40
M_3	2	40
M_4	2	40
M_5	2	25
M_6	2	25

Table 4.2: MOS transistors width and length values

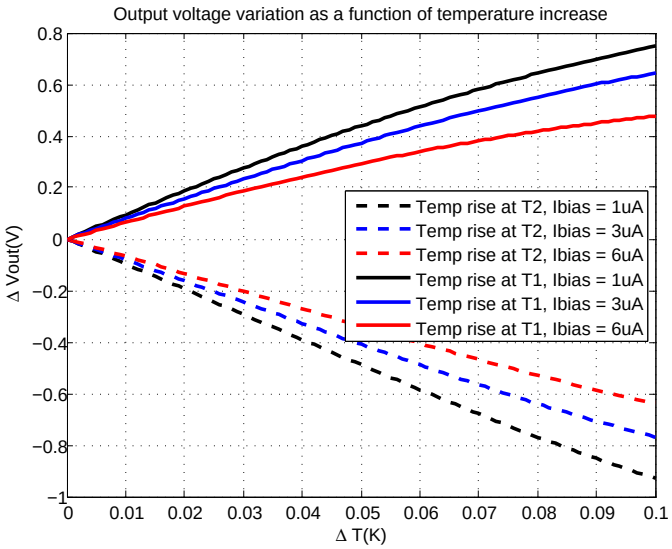


Figure 4.16: ΔV_{out} as a function of ΔT and current I_{BIAS} for temperature values from 300 K to 300.1 K. Temperature sensor with BJT transducers

4.2.2 Simulations of the BJT Differential conditioning circuit

By sweeping the *SPICE* parameter *TEMP*, it is possible to increase or decrease the absolute temperature value of one component while keeping the rest of the circuit at ambient temperature. Consequently, the output sensitivity of the sensor when one transducer is placed near the heating DUT can be simulated. The results of emulating a small temperature change $\Delta T = 0.1\,\mathrm{K}$ (from 300 K to 300.1 K) in the DUT are shown in Fig. 4.16. The response of the sensor has been analysed for three different bias currents: $I_{BIAS} = 1\,\mu\mathrm{A}$, $3\,\mu\mathrm{A}$ and $6\,\mu\mathrm{A}$.

An approximately symmetrical output dynamic margin is obtained fixing $V_{out_{DC}}$ to $V_{DD}/2$ with I_N and I_P current bleeding sources. Biasing the sensor with $I_{BIAS} = 1\,\mu\mathrm{A}$, the output signal V_{out} presents a sensitivity of $7.5\,\mathrm{V/K}$ when the temperature rises at T_1, and a sensitivity of $-9.5\,\mathrm{V/K}$ when temperature rises at T_2. V_{out} sensitivity values decrease when I_{BIAS} is increased. For instance, $I_{BIAS} = 3\,\mu\mathrm{A}$ provide sensitivity values of $6.5\,\mathrm{V/K}$ and $-7.8\,\mathrm{V/K}$, while using $I_{BIAS} = 6\,\mu\mathrm{A}$ these are $4.8\,\mathrm{V/K}$ and $-6.5\,\mathrm{V/K}$.

The presented topology is then a very suitable solution for detecting small

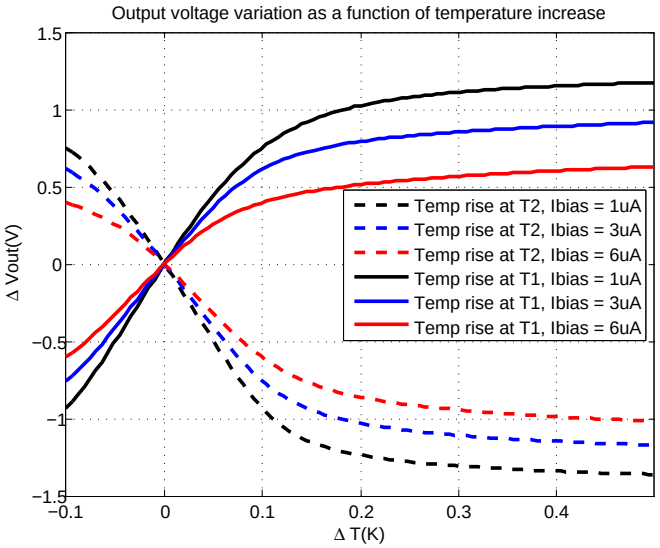


Figure 4.17: ΔV_{out} as a function of ΔT and current I_{BIAS} for temperature values from 299.9 K to 300.5 K. Temperature sensor with BJT transducers

temperature changes (0.1 K). Nevertheless, larger temperature variations cannot be properly detected since the OTA output would rapidly saturate. Fig, 4.17 illustrates the response of the OTA for temperature variations ΔT higher than 0.1 K. In this case, temperature has been swept from 299.9 K to 300.5 K, considering 300 K as the ambient temperature T_0 and, again, adjusting $V_{out_{DC}}$ to $V_{DD}/2$ for $I_{BIAS} = 1\,\mu A$, $3\,\mu A$ and $6\,\mu A$. Given that operating conditions are the same as in Fig. 4.16, results observed in the temperature range 300 K to 300.1 K are exactly the same. The sensor output voltage value decreases when T_2 BJT is heated, while output voltage value increases if T_1 BJT is close to the heat source. In Fig. 4.17 however, the output signal saturation can be observed.

When temperature in T_1 rises, the voltage at the drain of M_6 increases, drastically reducing r_{out} value and thus the output voltage sensitivity. The same happens when the temperature in T_2 increases. Output voltage quickly drops and the sensor output resistance decreases, reducing the sensitivity. Moreover, the sensor response enters in an undesired non-linear region since we want a linear relationship between the sensor output and the PA temperature.

Bandwidth and slew rate simulations have been done connecting a voltage source to the base of T_1 and T_2 BJT transducers. Bandwidth values have been obtained using a sinusoidal waveform while a voltage step has been applied for the slew-rate calculation. In both cases, the amplitude of the applied signal corresponded to a temperature variation around 0.0 K and 0.1 K according to the V_{BE} thermal sensitivity $S(mV/K)$ studied in section 4.1.4.

Simulations (Fig. 4.18) have been carried out adjusting $V_{out_{DC}}$ to $V_{DD}/2$ and biasing the sensor with $I_{BIAS} = 1\,\mu A$, $3\,\mu A$ and $6\,\mu A$. The sensor is working in open circuit, which means that no load is connected to its output node. The analysis of the results shows that the bandwidth of the conditioning circuit is inversely proportional to its response sensitivity. Decreasing I_{BIAS}

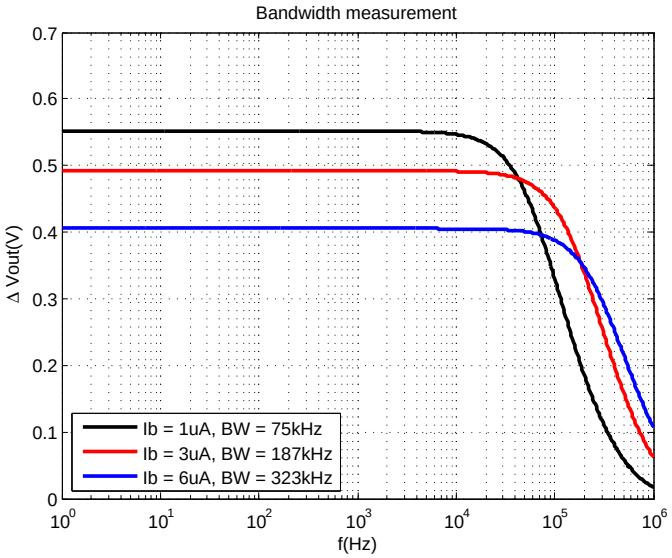


Figure 4.18: BJT temperature sensor bandwidth analysis. Sensor working in open circuit

Heated MOS	I_{BIAS} (µA)	SR (kV/s)	BW (kHz)	ΔV_{out} (V/K)
T_1	6	229.5	323	4.8
T_2		-226		-6.5
T_1	3	195	187	6.5
T_2		-198		-7.8
T_1	1	97.6	75	7.5
T_2		-95		-9.5

Table 4.3: BJT temperature sensor figures of merit summary

current provides a better V_{out} sensitivity as seen in Fig. 4.16, however, higher r_{out} values are translated into lower bandwidth values according to expression (4.15). Table 4.3 shows the calculated slew-rate values and summarises the characteristics of the sensor.

Small differences between devices can cause unexpected current imbalances, and consequently large variations in the output node voltage due to its high impedance nature. These variations, mainly caused by mismatch and process variations effects, are translated into temperature offsets. A solution to this problem is to calibrate the output level of the sensor ($Vout_{DC}$) to a known voltage with the help of I_N and I_P bleeding current sources.

To quantify the input-equivalent temperature offset ΔT introduced by mismatch and process variations, MonteCarlo simulations have been done taking the temperature at which $Vout_{DC}$ is equal to $V_{DD}/2$ under nominal conditions as the reference temperature value. The obtained statistical results are represented with normal distribution functions in Fig. 4.19, for $I_{BIAS} =$ 1 µA, 3 µA and 6 µA. Table 4.4 summarises the standard deviation represented as σ and $3 \cdot \sigma$.

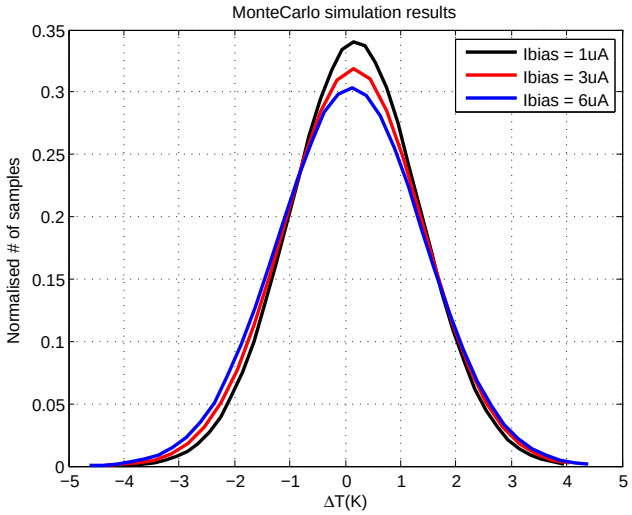


Figure 4.19: BJT Temperature sensor MonteCarlo analysis results. Input referred temperature offset distribution functions for I_{BIAS} = 1, 3 and 6 µA

I_{BIAS} (µm)	σ (K)	$3 \cdot \sigma$ (K)
1 µA	1.17	3.51
3 µA	1.25	3.75
6 µA	1.31	3.93

Table 4.4: BJT Temperature sensor MonteCarlo analysis results. Input referred temperature offset standard deviation values (σ and $3 \cdot \sigma$) obtained for I_{BIAS} = 1, 3 and 6 µA

4.2.3 Design of the MOS differential conditioning circuit

To be able to compare both sensors in terms of output sensitivity, the sizing of the transistors has been decided to be the same length as in the sensor with BJT transducers (T_1 and T_2). Hence, NMOS transistors length is L = 40 µm while the length of PMOS transistors is 25 µm.

The aspect ratio K = (W/L) of T_3 and T_4 MOS temperature transducers determine their V_{OD} voltage together with I_{BIAS}, and thus, their current thermal sensitivity $S(nA/K)$ (expression 4.6, Fig. 4.2). In order to maximise T_3 and T_4 sensitivity $S(nA/K)$, the performance of the sensor has been simulated with several K values. We have decided to use an aspect ratio of 50 (W = 50 µm, L = 1 µm) since there is almost no difference for K > 50. Moreover, smaller values of K lead to smaller layout areas.

The width of M_7 and M_8 determines the drain voltage of T_3 and T_4 MOS transducers. T_3 and T_4 must operate in saturation region, otherwise their current thermal sensitivity $S(nA/K)$ is almost negligible. For this purpose, the width of M_7 and M_8, and consequently the rest of the MOS transistors, has been seet to 40 µm. A summary of the transistors dimensions is shown in Table 4.5.

Component	Width (µm)	Length (µm)
T_3	50	1
T_4	50	1
M_7	40	25
M_8	40	25
M_9	40	25
M_{10}	40	25
M_{11}	40	40
M_{12}	40	40

Table 4.5: MOS temperature sensor transistors dimensions

4.2.4 Simulations of the MOS differential conditioning circuit

The same method as in section 4.2.2 has been used for simulating the sensor output sensitivity.

The response of the sensor for small temperature changes ($\Delta T = 0.1\,\mathrm{K}$) has been simulated fixing $V_{out_{DC}} = V_{DD}/2$, by adjusting the current bleeding sources (I_N and I_P). The results are shown in Fig. 4.20. Output sensitivity is $5.2\,\mathrm{V/K}$ when T_3 is heated, and $-5.8\,\mathrm{V/K}$ when T_4 is heated for $I_{BIAS} = 1\,\mu\mathrm{A}$. Lower sensitivities are reported for larger I_{BIAS}: $-5.1\,\mathrm{V/K}$ and $4.6\,\mathrm{V/K}$ for $I_{BIAS} = 3\,\mu\mathrm{A}$, and $-2.2\,\mathrm{V/K}$ and $2.1\,\mathrm{V/K}$ for $I_{BIAS} = 6\,\mu\mathrm{A}$.

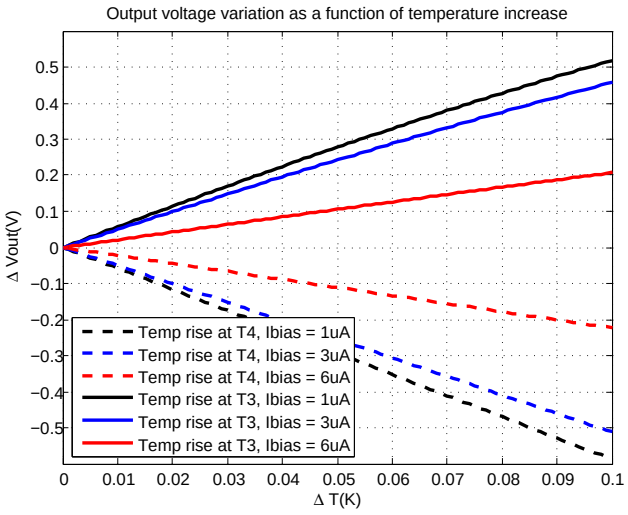


Figure 4.20: ΔV_{out} as a function of ΔT and current I_{BIAS} for temperature values from 300 K to 300.1 K. Temperature sensor with MOS transducers

Regarding the bandwidth and slew-rate measurements, these have been taken connecting a voltage source to the gate of T_3 and T_4 MOS transducers. Fig. 4.21 show the obtained bandwidth values of the sensor working in open circuit. Again, there is a trade-off between the sensor output sensitivity and its bandwidth. As higher the current I_{BIAS}, as higher the sensor bandwidth, but

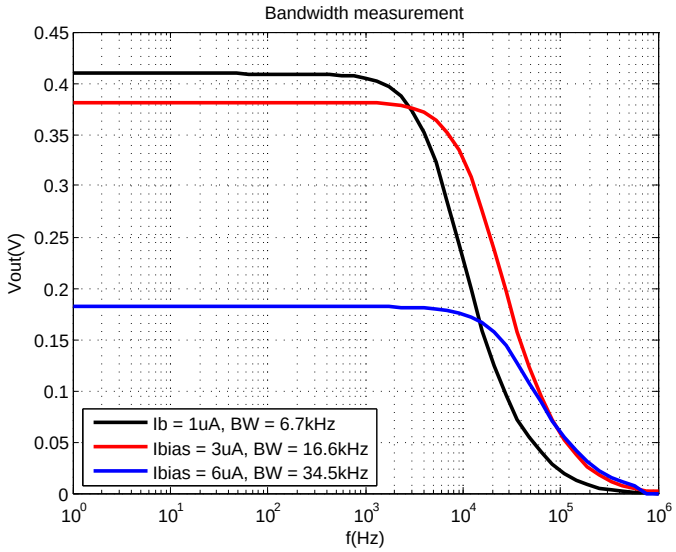


Figure 4.21: MOS temperature sensor bandwidth analysis. Sensor working in open circuit

at the same time as lower the ΔV_{out} slope. Table 4.6 contains the calculated slew-rate values as well as the already mentioned characteristics of the sensor.

Heated MOS	I_{BIAS} (µA)	SR (kV/s)	BW (kHz)	ΔV_{out} (V/K)
T_1	6	11.27	34.5	2.1
T_2		-11.4		-2.2
T_1	3	13.1	16.6	4.6
T_2		-13.47		-5.1
T_1	1	6.21	6.7	5.2
T_2		-6.26		-5.8

Table 4.6: MOS temperature sensor figures of merit summary

Finally, similarly to BJT Temperature sensor, input-equivalent temperature offset ΔT due to mismatch and process variations has been calculated doing MonteCarlo simulations. Results are illustrated in Fig. 4.22 and summarised in Table 4.7.

I_{BIAS} (µm)	σ (K)	$3 \cdot \sigma$ (K)
1 µA	1.00	3.00
3 µA	1.05	3.15
6 µA	1.18	3.54

Table 4.7: MOS Temperature sensor MonteCarlo analysis results. Input referred temperature offset standard deviation values (σ and $3 \cdot \sigma$) obtained for I_{BIAS} = 1, 3 and 6 µA

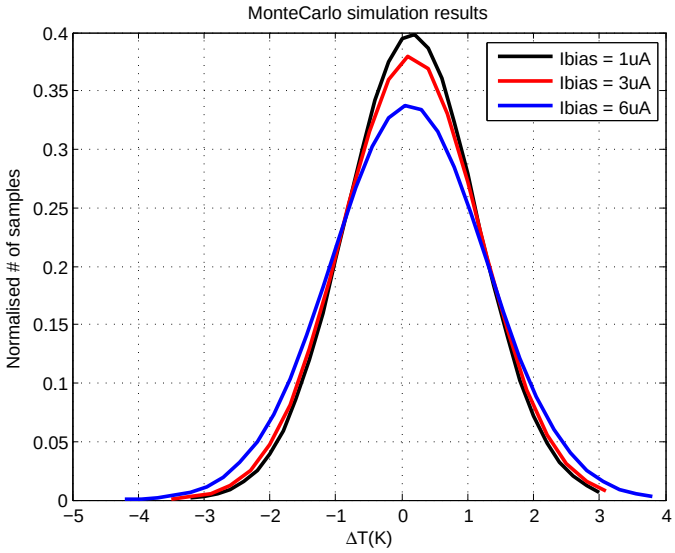


Figure 4.22: MOS Temperature sensor MonteCarlo analysis results. Input referred temperature offset distribution functions for I_{BIAS} = 1, 3 and 6 µA

4.3 Design of the bleeding current sources

The bleeding current sources I_N and I_P have been implemented as a digitally controlled series of binary weighted current sources. Each current source can be enabled or disabled by a switch. At the same time, switches are controlled by each one of the bits that form the digital word. Two main aspects have been considered for the design, the minimum current resolution and the maximum temperature offset ΔT that the sensor can present. Both aspects determine the necessary number of bits and the amount of current added or subtracted by current source associated to the the least significant bit (LSB).

First of all, simulations sweeping I_N and I_P ideal current sources have been carried out for calculating the amount of ΔT that can be compensated depending on how much bleeding current is added or subtracted. I_N and I_P current values have been swept from 0 to 25 % of I_{BIAS}. For instance, Fig. 4.23 shows the response of the sensor (V_{out}) as a function of the temperature for values from 0 to 250 nA (25 % of I_{BIAS} = 1 µA). As it can be observed a maximum of ±10 K temperature offset can be compensated. Using I_{BIAS} = 3 µA and I_{BIAS} = 6 µA it is possible to compensate up to 13 K and 16 K.

According to the MonteCarlo simulations in sections 4.4.2 and 4.2.4, mismatch and process variation effects can introduce temperature offsets of 3.93 K in the case of the BJT Temperature sensor and 3.54 K in the case of MOS Temperature sensor. In addition, the results reported in [1] indicate that the DUT biasing process also introduces a temperature offset in the sensor ranging from 7 to 10 K. Taking this into consideration, bleeding current sources must be able to compensate temperatures up to 14 K. This means that bleeding sources must provide a current value slightly higher than 25% of I_{BIAS}.

An offset ΔT of 0.1 K has been decided as the current associated to the LSB. This ΔT value corresponds to half the input temperature margin of the

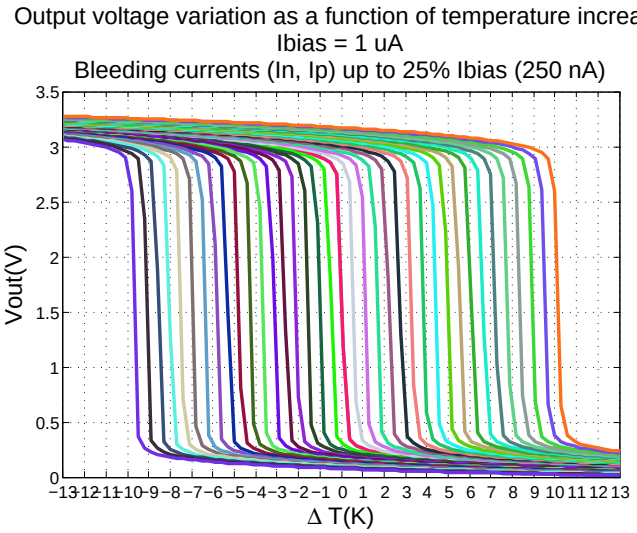


Figure 4.23: BJT Temperature sensor V_{out} variation as a function of temperature increase. Simulation sweeping I_N and I_P current sources values from 0 to 250 nA

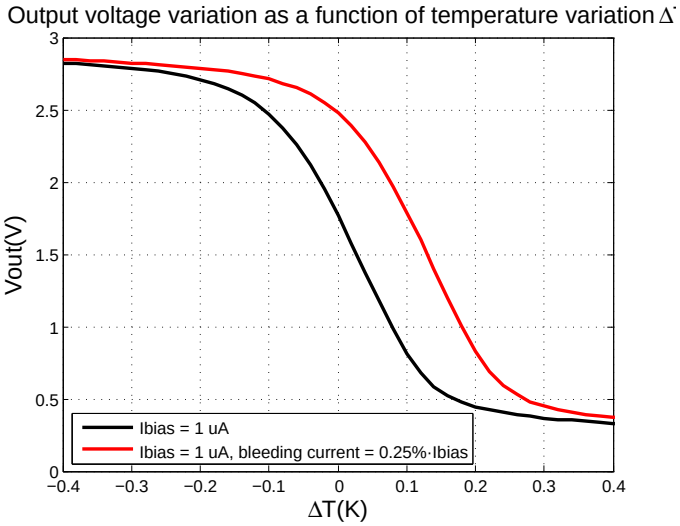


Figure 4.24: BJT Temperature sensor V_{out} as a function of temperature

	B_6	B_5	B_4	B_3	B_2	B_1	B_0	Total
% I_{BIAS}	16	8	4	2	1	0.5	0.25	31.75

Table 4.8: Bleeding current sources digital word structure

sensor with a maximum sensitivity value of $-9.5\,\mathrm{V/K}$. Fig. 4.24 shows that an offset of 0.1 K can be compensated by adding or subtracting the exact amount of 0.25 % $\cdot$ I_{BIAS}.

To make sure the noise of the circuit does not affect the chosen resolution, a *.noise* analysis has been done. Results report noise voltage levels of 70.13 mV (up to 100 kHz, Fig. 4.18, $I_{BIAS} = 1\,\mu\mathrm{A}$), 60.22 mV (up to 200 kHz, Fig. 4.18, $I_{BIAS} = 3\,\mu\mathrm{A}$) and 52.9 mV (up to 350 kHz, Fig. 4.18, $I_{BIAS} = 6\,\mu\mathrm{A}$). These noise levels are translated, in the worst case, into temperature offsets of 7 mK, 7.7 mK and 8.1 mK, respectively, given the BJT sensor output sensitivities (Table. 4.3, T_2 heated).

In order to decide if the offset ΔT introduced by the circuit noise should be taken into account, the worst case scenario have been analysed. As stated in section 4.2.2, the BJT Temperature sensor presents a maximum output sensitivity of $-9.5\,\mathrm{V/K}$ for $I_{BIAS} = 1\,\mu\mathrm{A}$ and $Vout_{DC} = V_{DD}/2$. Under these circumstances, temperature can variate approximately 0.2 K before the sensors output starts to saturate (Fig. 4.24). The temperature offset introduced by the circuit noise represents only a 4.05 % of the total temperature input margin (8.1 mK over 0.2 K), and therefore it can be neglected.

Given all that, 7 bits have been implemented in order to provide bleeding currents from 0.25 % $\cdot$ I_{BIAS} to 31.75 % $\cdot$ I_{BIAS} (Table 4.8). Working with percentage values make the offset compensation structure more versatile, given that in case I_{BIAS} value is increased, the bleeding current will also increase, and the compensated ΔT will remain approximately equal.

Figure 4.25 shows the schematic of the bleeding current sources and I_{BIAS} current source topology. As it can be observed, both I_{BIAS} and the bleeding current sources are generated from a reference current I_{REF}, controlled by an external voltage V_{EXT}. The current biasing the sensor, I_{BIAS}, is generated with a current mirror (M_{REF}-M_{BIAS}). The binary weighted current sources (from M_{B_6} to M_{B_0}, with their respective switches M_{BS_6} to M_{BS_0}) are also implemented with current mirrors and divided in three groups formed by M_{B_6}-M_{B_5}, M_{B_4}-M_{B_3} and M_{B_2}-M_{B_0}. Intermediate mirroring stages (M_{I_X}) have been added with the purpose of keeping a reasonable aspect ratio between the PMOS transistors associated to the MSB and LSB. MOS transistors M_{REF}, M_{BIAS}, M_{B_6} - M_{B_0} and intermediate stages transistors M_{I_X} have been dimensioned with L = 50 µm and width values multiples of 4 µm, being 4 µm the width of a gate finger. Finally, switch transistors M_{BS_6} - M_{BS_0} have been dimensioned with W = 1 µm and L = 1 µm.

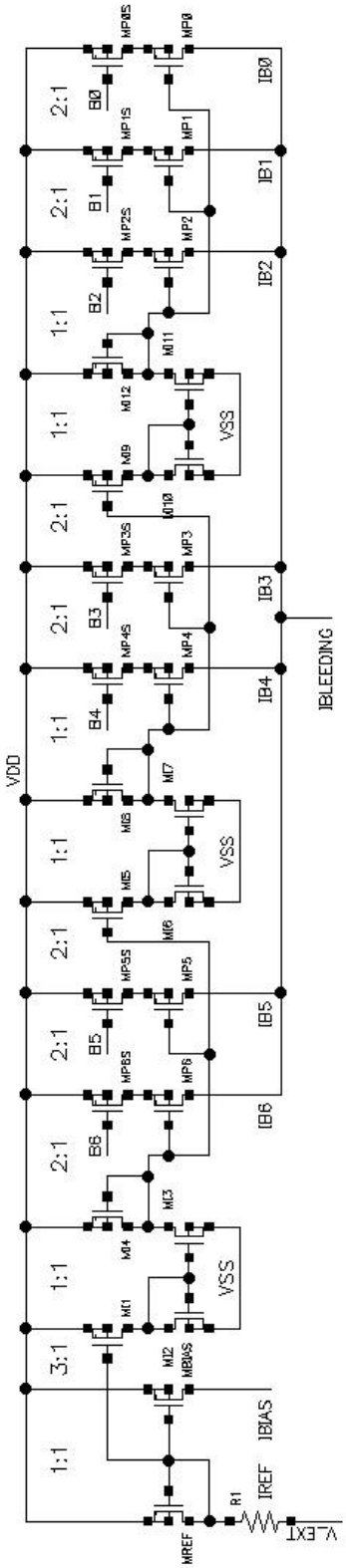


Figure 4.25: Bleeding current sources and I_{BIAS} schematic

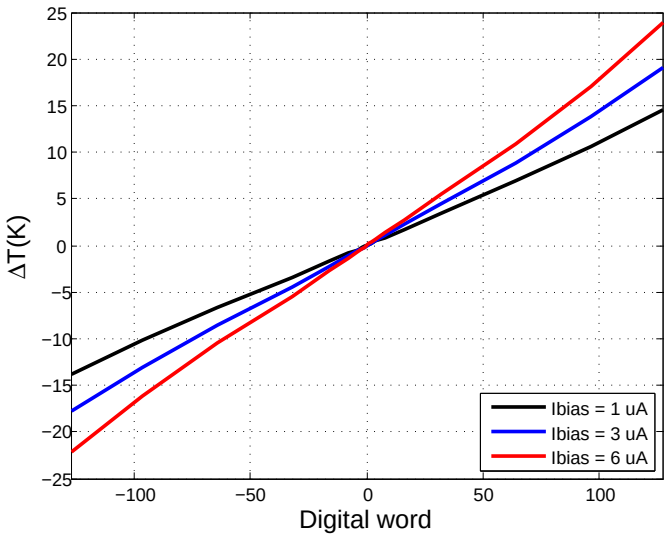


Figure 4.26: Compensable temperature offset as a function of I_{BIAS} and the digital word formed by A_6-A_0 and B_6-B_0

The designed structure has been integrated with the temperature sensor, replacing I_N and I_P ideal sources (Fig. 4.27; In this case, the BJT Temperature sensor is chosen for the integration). The digital word A_6-A_0 controls the bleeding current sources (formerly I_P) connected to the transducer T_1 branch, while the digital word formed by B_6-B_0 controls the bleeding current sources (formerly I_N) connected to the transducer T_2 branch. Figure 4.26 shows the amount of ΔT that can be compensated depending on the words B_6-B_0 and A_6-A_0, represented with their equivalent decimal value. Negative and positive values will correspond to B_6-B_0 or A_6-A_0 depending on which transducer is being heated. Figure 4.26 shows that it is possible to compensate ΔT of $\pm 14\,\mathrm{K}$, $18\,\mathrm{K}$ and $22\,\mathrm{K}$ with biasing currents $I_{BIAS} = 1\,\mu\mathrm{A}$, $3\,\mu\mathrm{A}$ and $6\,\mu\mathrm{A}$, thus accomplishing the design requirements.

To conclude, an operational amplifier has been used for the interface between the sensor and its corresponding IC pad. The use of an OpAmp does not affect the high impedance of the sensor output node, and therefore V_{out} sensitivity is not reduced. Nevertheless, the bandwidth and slew-rate values reported without loading the sensor (Table 4.3) are now lowered due to the input capacitance of the OpAmp. Table 4.9 shows the bandwidth and slew-rate of the sensor including the OpAmp. The implemented operational amplifier is the *OP0WB* wide-band model available in the AMS 0.35 µm Technology libraries and it is supplied with the *BBIAS* 11.4 µA current source model, also available in the libraries.

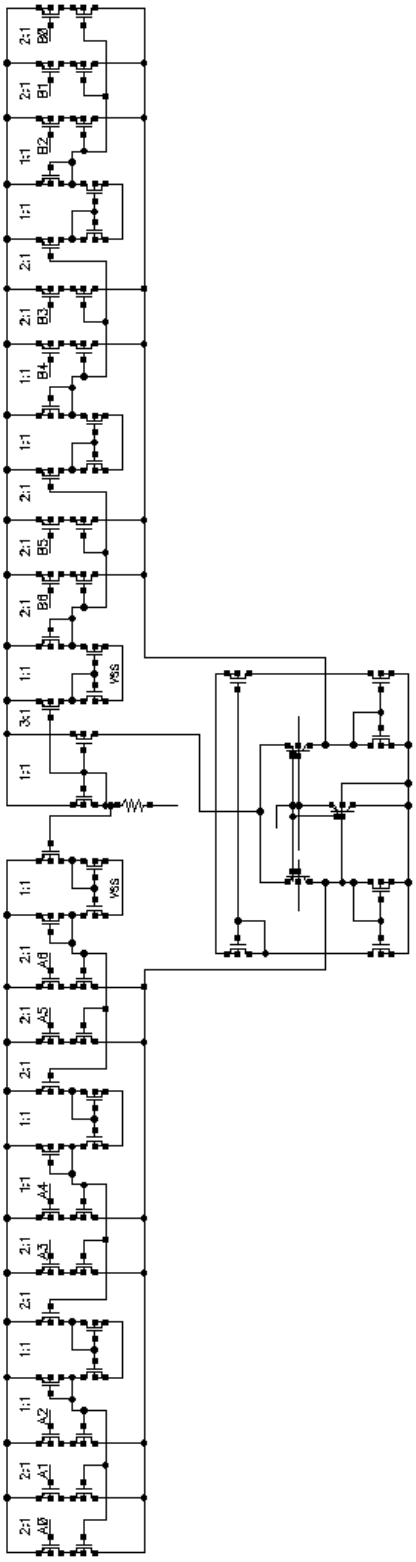


Figure 4.27: BJT Temperature sensor integrated with bleeding current sources and I_{BIAS} schematic

Heated MOS	I_{BIAS} (µA)	SR (kV/s)	BW (kHz)
T_1	6	45.8	46.12
T_2		-45.7	
T_1	3	31.99	25.99
T_2		-31.8	
T_1	1	11.3	11.5
T_2		-11	

Table 4.9: BJT Temperature sensor bandwidth and slew-rate values loading the sensor with an operational amplifier

4.4 Conclusions

Two temperature sensors have been presented in this chapter. Firstly, the behavior of MOS and BJT transistors as temperature transducers has been analysed and compared in section 4.1. Then, two conditioning circuits have been designed in section 4.2. The proposed topology is a differential-input single-ended output operational transimpedance amplifier. In this way, the sensors are able to convert temperature changes into current variations with MOS and BJT transducers, and to convert this current imbalances into an output voltage signal with the OTA conditioning circuits. Finally, both temperature sensors have been simulated and characterised in terms of output sensitivity (V/K), bandwidth and slew-rate.

As a first observation, the designed sensors present a high response sensitivity. This means that small temperature variations can be detected with a good output voltage resolution. Nevertheless, the sensitivity achieved with the BJT based temperature sensor is higher than the one obtained with the MOS based sensor. For instance, under the same biasing scenario ($I_{BIAS} = 1\,\mu A$), temperature sensor with BJT transducers offers an output sensitivity of $-9.5\,V/K$ (Fig. 4.16) while the MOS sensor has an output sensitivity of $-7.8\,V/K$ (Fig. 4.20).

In relation to bandwidth and slew-rate, BJT based sensor also provides a better performance than MOS sensor. Although both solutions have the same transistors length, the width of the MOS sensor transistors is bigger, increasing the output node capacitance and thus reducing its bandwidth and slew-rate features (Fig. 4.18 and 4.21).

Besides, an offset compensation structure has been designed in order to compensate possible temperature offsets ΔT and calibrate the sensor.

In terms of performance, the sensor with BJT temperature transducers is a better solution for on-chip thermal monitoring applications, where not only the sensor has to be capable of tracking small temperature variations but it also has to be able to provide a fast response. Even in terms of layout area, the BJT sensor can be easily integrated and placed near the heat source (e.g. a prower amplifier), while MOS sensor could be more problematic due to its wider transistors.

4.5 References

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CHAPTER 5

Amplitude detector

An amplitude detector has been designed and implemented in order to provide an observation of the power amplifier (PA) output power with a method alternative to the temperature sensor described in the former chapter. Amplitude detectors have been so far the classical way to monitor the performances of RF circuits with buit-in sensors. This amplitude sensor will provide a DC output proportional to the peak value of the power amplifier output signal. In this way, a decrease in the detector output can mean that the power amplifier properties have been degraded and its power gain has been reduced. In this chapter, the topology and design of the signal amplitude sensors is presented. The chapter covers only the design of the amplitude detector in charge of monitoring the PA output signal under the assumption that it can be reused for tracking the RF input signal of the PA.

5.1 Operation principle

Although there are many possible topologies [1][2], the detector described in [3] has been chosen because of its simplicity and its robustness against process variations. The chosen differential topology (Fig. 5.1) is formed by two MOS transistors in common-drain configuration (M_0 and M_1) and a low-pass filter in each output node. The static current of both common-drain structures is fixed by current sources implemented with NMOS transistors (M_2 and M_3).

Because of the non-linearities of a MOS transistor, the DC component of its current depends not only on the DC gate-source voltage but also on the RF signal applied to its gate.In this case, the DC component of M_1 current depends on the gate to source voltage $V_{GS}(M_1)$, while the DC component of M_0 current depends on $V_{GS}(M_0)$ but also on the RF signal V_{in} coming from the PA. Since M_2 and M_3 fix the DC component of M_0 and M_1 current and the DC gate voltage V_{bias} is the same in both transistors, every increase or decrease in V_{in} RF signal is translated into a Vx DC value variation in order to keep the same gate-source DC voltage in both transistors. Capacitors Cf_x and Cf_y are used to filter out high-frequency components and obtain only a DC signal output.

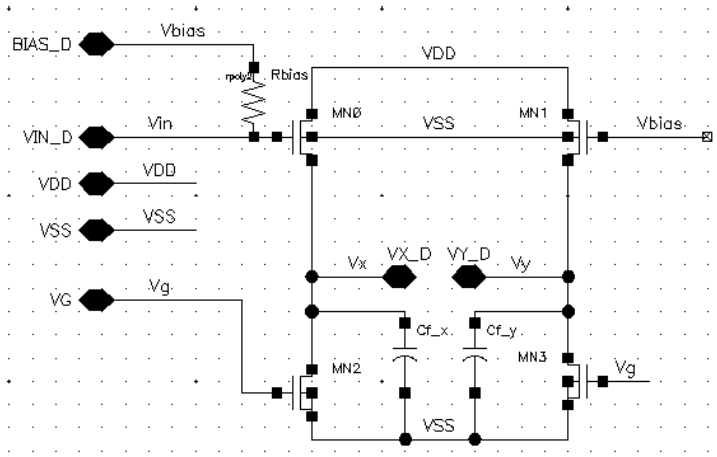

Figure 5.1: Schematic of the amplitude detector

	Saturation	
	All inputs	
Triple well	$(V_{GS}-V_{T2})-\sqrt{((V_{GS}-V_{T2})^2-\frac{A^2}{2})}$	
Body effect	$(V_{GS}-V_{T1})-\sqrt{((V_{GS}-V_{T2})^2-\frac{A^2}{2})}$	
	Subthreshold	
	Small inputs	*Large inputs*
Triple well	$\frac{A^2}{4nV_t}$	$A-\frac{nV_T}{2}\ln(\frac{2\pi A}{nV_T})$
Body effect	$\frac{A^2}{4n^2V_t}$	$\frac{A}{n}-\frac{V_T}{2}\ln(\frac{2\pi A}{nV_T})$

Table 5.1: RF-to-DC conversion equations for MOSFET [3]

The detector is able to operate with both transistors M_0 and M_1 working in saturated subthreshold and saturated strong inversion region since MOSFET I-V characteristic non-linearities appear in both situations. However, the sensor presents a better performance when working in subthreshold region. The theoretical expressions of the output voltage depending on the MOSFET operation region are summarized in [3] and presented in Table 5.1. As it can be observed, the response of the detector when working in subthreshold region is not affected by bias voltage, supply voltage or current variations. On the contrary, the detector response is susceptible to process and current variations when it is working in strong inversion region. Regarding the low-pass filter, its cut-off frequency is determined by the capacitor connected to the output node (Cf_x and Cf_y) and the equivalent output resistance of the current source (M_2 and M_3) and the common drain (M_0 and M_1). Finally, the common drain NMOS M_0 is biased using a resistor R_{bias} in series with a voltage source V_{bias}, and the input RF signal comes from the high-pass filtered power amplifier output.

At this point, it is convenient to analyze the characteristics of the signal at the detector input. First of all, we should recall that the power amplifier can work in two different situations:

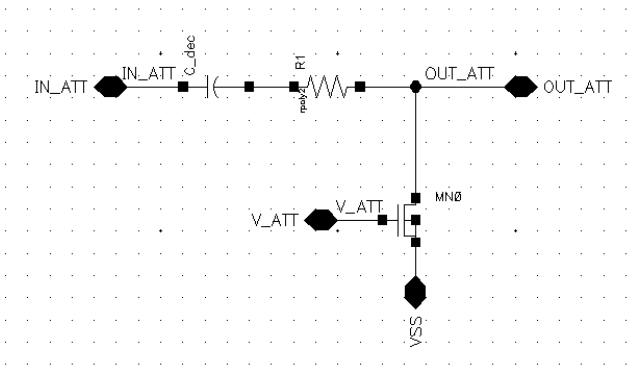

Figure 5.2: Schematic of the attenuator

- **Normal mode**: The power amplifier works under nominal conditions and thus its output signal can reach a maximum peak-peak value of $2{\cdot}V_{DD}$, where $V_{DD} = 3.3\,\mathrm{V}$. In this case, the maximum voltage at the gate of M_0 transistor would be $V_{bias} + 3.3\,\mathrm{V}$.
- **Stress mode**: The power amplifier is stressed in order to accelerate its aging by increasing its supply voltage well above 5 V. In this case, the voltage at the detectors input can be, for instance, as high as $V_{bias} + 5\,\mathrm{V}$. No measurements of the sensor output are taken during this operation mode.

Stress mode is induced only to the PA in order to accelerate its ageing and the PA performances are only measured during normal mode. However, during the stress mode, the high voltages can harm M_0 producing a gate oxide breakdown. In order to protect M_0, an attenuator has been introduced between the PA and the power detector with the purpose of reducing the maximum voltage levels at the gate of M_0. This attenuator must behave in the following way:

- **Normal mode**: The attenuator is disabled and it must attenuate as minimum as possible the signal coming from the power amplifier
- **Stress mode**: The attenuator is enabled and attenuates the signal coming from the power amplifier

The attenuator circuit (Fig. 5.2) has been implemented with a voltage divisor formed by a resistor and a voltage controlled MOSFET that acts as a switch.

Given that the block composed by the attenuator and the amplitude detector is electrically connected to the power amplifier output node, it is necessary to design the attenuator bearing in mind that the output impedance matching of the PA should not be modified in order to not affect its characteristics. Fig. 5.3 shows the integration of the attenuator and the amplitude detector with the power amplifier. Since it is an on-chip design, the attenuator is connected to the node between drain of the PA transistor (PA_CORE) and the output pads (PA_PAD).

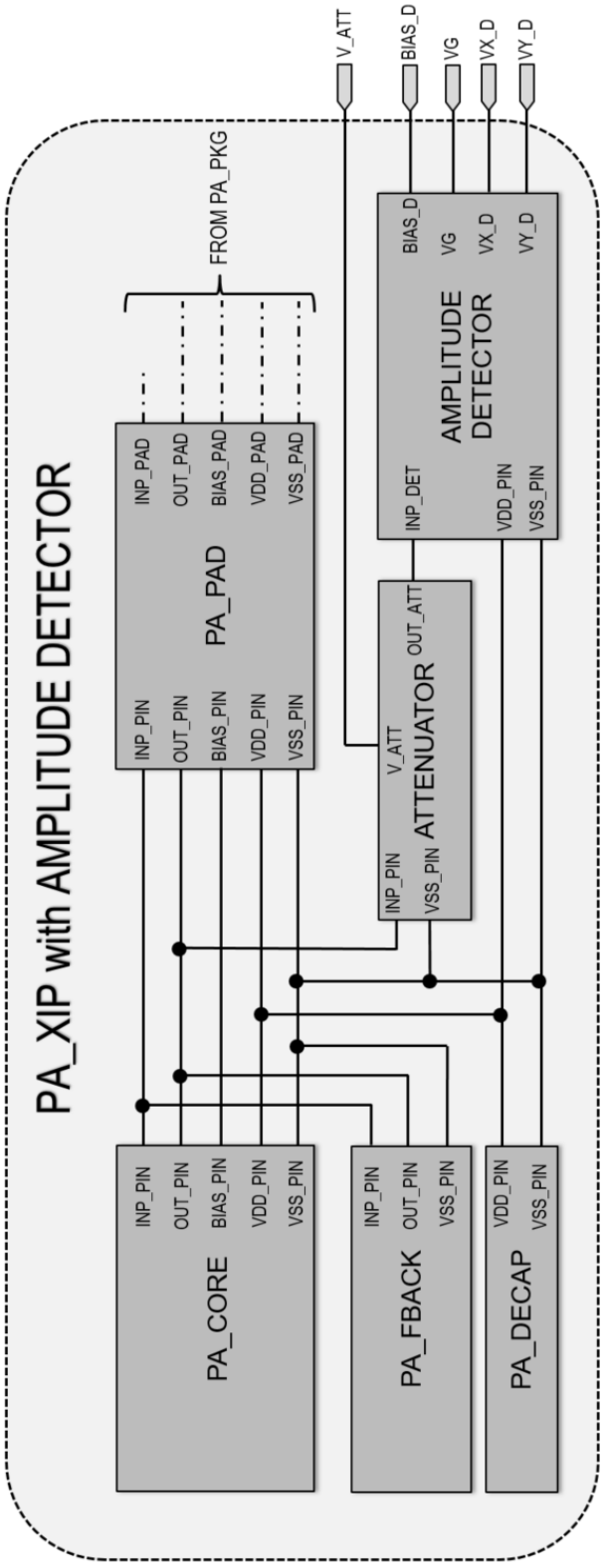

Figure 5.3: Hierarchical view of the attenuator and amplitude detector integrated with the power amplifier

Component	Design value
M_0, M_1	W = 1 µm L = 0.35 µm
Cf_x, Cf_y	1 pF
R_{bias}	10 kΩ
V_{bias}	1.5 V

Table 5.2: Design values of the amplitude detector components

5.2 Amplitude detector design

Table 5.2 summarizes the value of each one of the components used in the detector (Fig. 5.1). The MOS transistors M_0 and M_1 have been sized as small as possible in order to make its input impedance as high as possible. Their dimensions are W = 1 µm and L = 0.35 µm. The DC current must be set lower than 0.6 µA in order to keep M_0 and M_1 working in subthreshold region. The value of V_{bias} determines the DC voltage level at the output V_x and V_y. In this case a value of $V_{bias} = 1.5$ V has been chosen so that the DC voltage at the output node is enough for keeping M_2 and M_3 current sources working in saturation.

The biasing resistor R_{bias} should be high enough to affect neither the attenuator nor the output impedance matching of the power amplifier. The value selected is 10 kΩ (see justification in next section "Attenuator design"). Finally, we should take into account the following trade-off: the bigger the output capacitor (Cf_x and Cf_y), the lower the cut-off frequency, but at the same time, the larger the settling time. Moreover, as capacitors have a big impact in terms of layout area, it is preferable to have a smaller capacitor as long as the low-pass filter cutoff frequency is enough for our purposes. Taking all this into account, a capacitor of 1 pF has been used and the cut-off frequency is approximately 1.8 MHz.

Figures from 5.4 to 5.7 show the simulated results of the detector behavior working in subthreshold region. Fig. 5.4 compares the prediction of theoretical equation (Table 5.1, equation for subthreshold region operation taking into account the body effect) with simulated results using accurate MOS transistor models. The robustness of the sensor response against strong variations is demonstrated forcing current variations (Fig. 5.5), bias voltage V_{bias} variations (Fig. 5.6) and variations in the width of M_0 and M_1 (Fig. 5.7). As it can be observed, the sensitivity of the sensor is not affected by any of the above mentioned variations and only the DC level of V_x is slightly shifted causing an offset in the output V_{out} (defined as $V_x - V_y$). Since it is a differential topology, a mismatch between both branches would also cause an offset in V_{out}. In any case, it is not a major problem since variations in the PA performance are quantified with the increase or decrease ΔV_{out} and not with its absolute value.

Finally, Fig. 5.8 shows the DC output of the sensor for different PA input power values. In this case the attenuator block has not been included. The sensor presents a non-linear response because its operation is based on the MOS I-V non-linearities. Also, It is important to remark that the detector has a bigger sensitivity for PA input power values higher than 0 dBm than for low

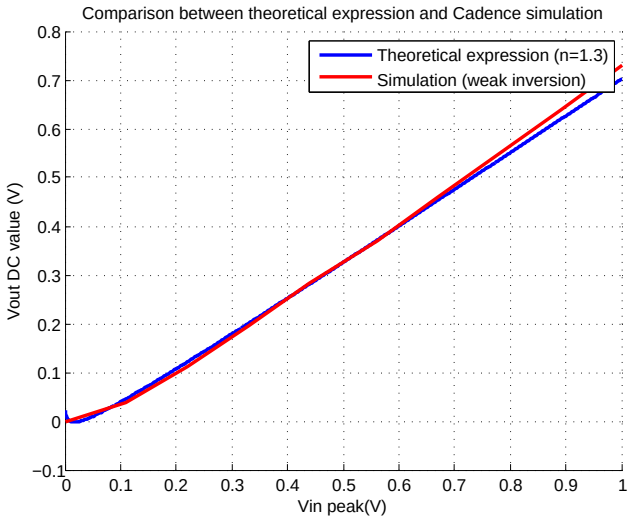

Figure 5.4: Comparison between the theoretical expression of the detector response with M_0 and M_1 working in subthreshold region and the simulated results

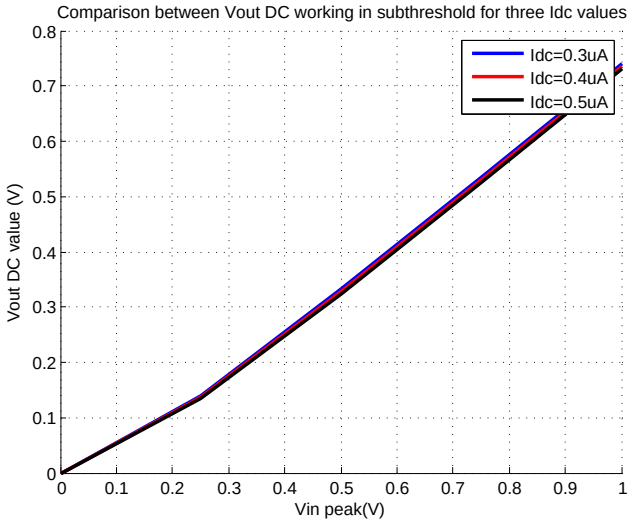

Figure 5.5: Comparison of the detector output signal for different I_{DC} current values

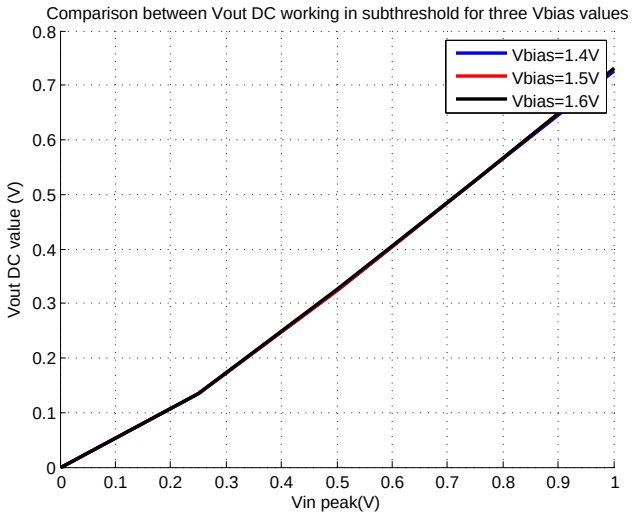

Figure 5.6: Comparison of the detector output signal for different V_{bias} voltage values

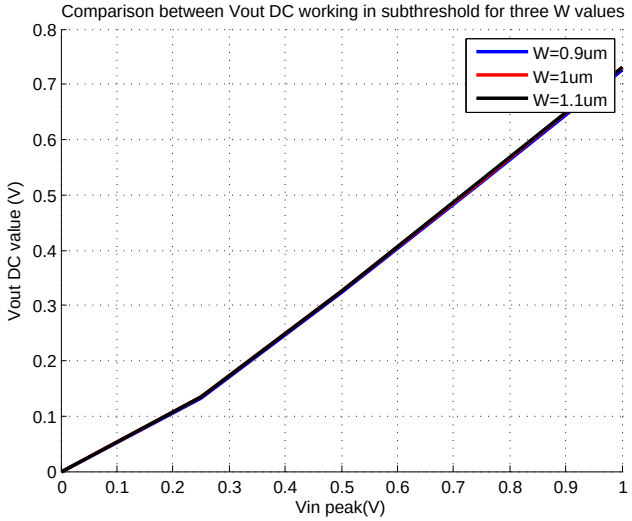

Figure 5.7: Comparison of the detector output signal for different M_0 and M_1 width value

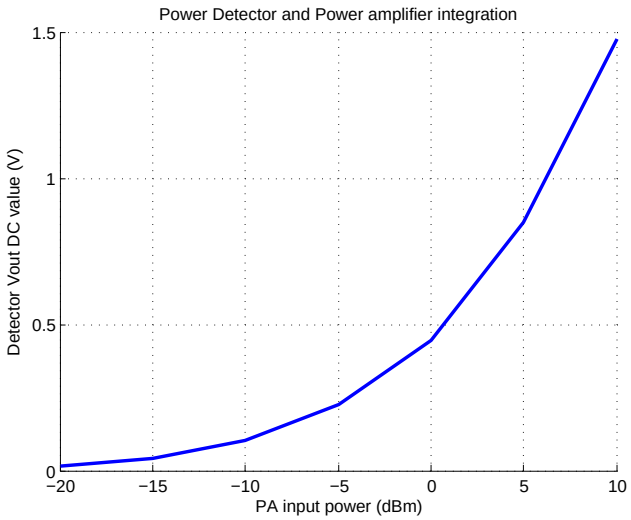

Figure 5.8: Output signal of the amplitude detector for different PA input power values

power signals. More concretely, the sensor presents sensitivity of 58.5 mV/dB for PA input power values from 0 to 10 dBm. This is an advantageous fact because, as it is reported in chapter 3, the amplifier stage will operate with signals within that range of power levels.

5.3 Attenuator design

The behavior of the attenuator can be analyzed as follows:

$$V_{InputDetector} = \frac{R_{switch}}{R_1 + R_{switch} + X_{Cdec}} V_{outputPA} \tag{5.1}$$

$$V_{InputDetector} = \frac{R_{in_{detector}} // R_{bias_{detector}}}{R_1 + X_{Cdec} + R_{in_{detector}} // R_{bias_{detector}}} V_{outputPA} \tag{5.2}$$

Eq. (5.1) is the attenuator transfer function when it is enabled, and eq. (5.2) when it is disabled. When the attenuator is disabled ($V_{ATT} = 0\,\text{V}$), the drain to source MOS equivalent resistance R_{switch} is very high, however eq. (5.2) shows that the attenuator still reduces the signal coming from the power amplifier due to the voltage divider formed by R_1, the impedance $X_{C_{dec}}$ of the decoupling capacitor C_{dec} and the parallel between R_{bias} and the detector equivalent input resistance. For this reason, in order to reduce these losses, the input transistors of the detector are made as small as possible, R_{bias} is set 10 kΩ and the resistor $R1$ is selected to be ten times smaller than R_{bias}. Taking all this into account, the signal coming from the PA is attenuated by 1 dB (attenuation factor = 0.9).

When the attenuator is enabled ($V_{ATT} = 3.3\,\text{V}$) the voltage divider is formed by R_1 and the ON resistance of the MOS (R_{switch} in eq.(5.1)). The value of this resistance can be reduced by increasing the width of the MOS transistor as shown in Fig. 5.9. A MOS with W = 40 µm, L = 0.35 µm has been chosen in

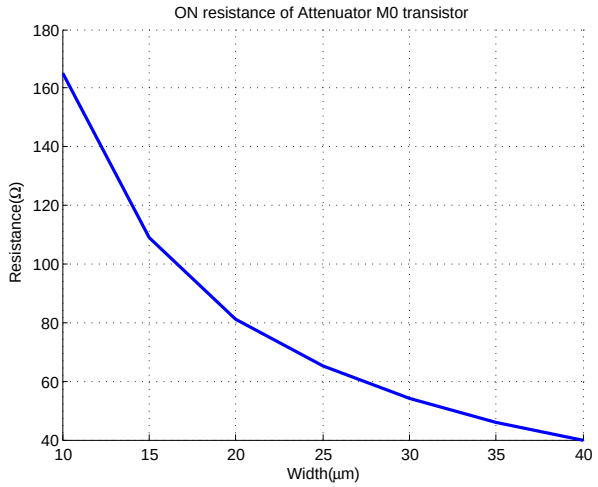

Figure 5.9: Drain to source MOS equivalent resistance for W values from 10 to 40 µm (L = 0.35 µm, V_{ATT} = 3.3 V)

order to have a small ON resistance. In this case, it has an equivalent resistance of 40 Ω when a voltage V_{ATT} of 3.3 V is applied to the gate. With the R_1 value selected before, and according to expression (5.1) the signal coming from the PA should be attenuated by a factor of 0.03. Nevertheless, there are inductances in the path to ground (due to the wire bonding) that contribute with a certain impedance in series with the MOS transistor and thus reduce the attenuation factor to 0.2. Fig. 5.10 shows the voltage at the input of the amplitude detector for different PA input power values in three different situations: without the attenuator, with the attenuator disabled (attenuation factor 0.9) and with the attenuator enabled (attenuation factor 0.2). The power amplifier has a power gain of 6.9 dB according to the bias conditions explained in chapter 3. Vertical axis is in logarithmic scale in order to easily compare the three signals. As can be observed, the signal in red (attenuator disabled) is attenuated by 0.9 respect to the blue signal (without attenuator), and the signal in green (attenuator enabled) is attenuated by a factor of 0.2 respect to the blue signal.

This means that when the PA is working in "stress mode" i.e., when the output of the PA can reach, for instance, values of $2{\cdot}V_{DD}$ = 10 V, the maximum voltage at the input of the amplitude detector transistor M_0 will be 1 V + V_{bias} if the attenuator is enabled, and therefore its gate will not be damaged according to [4].

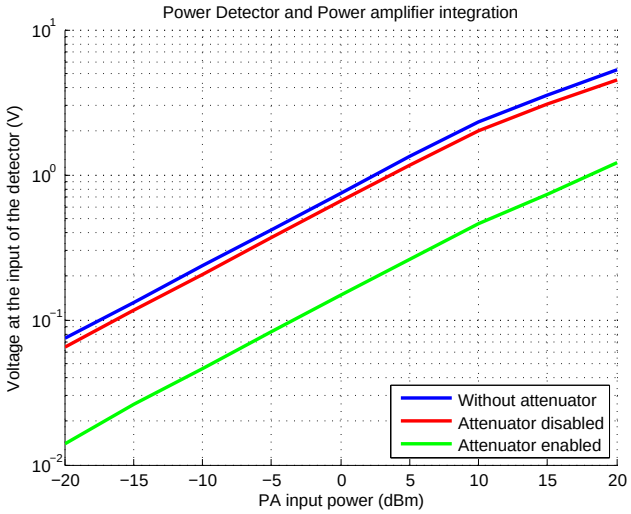

Figure 5.10: Input of the amplitude detector for different PA input power values

Lastly, the unavoidable losses of the attenuator with $V_{ATT} = 0\,\mathrm{V}$ reduce the output sensitivity of the amplitude detector. This can be observed in Fig. 5.11, where the signal in red belongs to the case where the attenuator is disabled, and the signal in blue belongs to the case where there is no attenuator stage between the power amplifier and the sensor. The sensor has an output sensitivity of approximately 44.7 mV/dB for PA input power values from 0 to 10 dBm with the attenuator, while it presents a sensitivity of 58.5 mV/dB when the attenuator is not included in the design.

Figure 5.11: Output signal of the amplitude detector for different PA input power values

5.4 Conclusions

In this chapter the design of the amplitude detector has been explained. Firstly, the circuit topology has been presented (Fig. 5.1) and its behavior has been analysed (Table 5.1). Also, the robustness of the chosen topology has been proved with simulations (Fig. 5.4 to 5.7).

The sensor has been integrated with the PA (Fig. 5.3) along with an attenuator stage for protection purposes. An attenuator has been included in order to protect the amplitude detector (Fig. 5.2) from high voltage values during the stress operation mode.

As it has been observed (Fig. 5.8), the detector output is not linear and two regions can be identified depending on the input signal level. An output sensitivity of 58.5 mV/dB has been reported for input power values from 0 to 10 dBm. This sensitivity value is decreased due to the attenuator losses (eq. 5.2) as it is shown in Figure 5.10. Sensitivity is reduced from 58.5 mV/dB to 44.7 mV/dB. Finally, the circuit has an output bandwidth of 1.8 MHz (fixed by capacitors Cf_x and Cf_y), which is enough for removing high frequency components and obtain a DC output signal.

5.5 References

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CHAPTER 6

Closing the loop

In the previous chapters, we have described the design of all the individual components in the proposed system: the power amplifier (PA), the temperature sensor and the amplitude sensor. As it has already been explained, the system has been designed to accelerate ageing effects in a device under test (DUT), embed circuitry able to monitor and measure the DUT behavior after ageing, and demonstrate the possibility to compensate performance degradations.

The temperature sensor will measure the temperature of the PA. This temperature can be directly related with the device power dissipation, and consequently with the delivered power. With the amplitude sensor we will be able to track the amplitude of the input and output PA signals. In this way, the PA response can be monitored and quantified. Finally, ageing effects will be accelerated by increasing the supply voltage of the PA.

In this chapter the observation and compensation methodology is presented. First, a review of the designed sensors and amplifier is given, remarking their control and adjustment signals. Then, the designed blocks are integrated and a general view of the system is given. A startup sequence is proposed in order to power up and calibrate each module separately. Some PA measurements using the sensors are presented, as well as the feedback loop basic requirements and the possible ageing scenarios. Finally, once the system has been started and prepared, a procedure for stressing the PA and compensating ageing effects is suggested. This chapter does not pretend to give a detailed description and quantitative design of the feedback, but to give a qualitative view of the system integration, possible measurements and compensation procedure.

6.1 Possible configurations

This section pretends to compile basic information and provide a clear view of the operation and pinout of each block. The two sensors and the power amplifier will have a different behavior depending on their configuration and therefore it is important to know their related signals in order to correctly adjust and operate them. Following, a review of the input and output signals of each block

will be given. Also, the relation between these signals and the block operation will be reviewed.

6.1.1 Temperature sensor

The temperature sensor has the following input and output signals:

- V_{EXT}: *Analog input signal.* Used to adjust $I_{BIAS_{Temp}}$.
- $A_0 - A_6$ and $B_0 - B_6$: *Digital input signals.* Adjust the offset of the sensor output voltage.
- $V_{OUT_{Temp}}$: *Analog output signal.* Response of the sensor.

The sensor will provide output voltage value depending on the sensed PA temperature. The increase of $V_{OUT_{temp}}$ respect to a temperature variation is determined by the sensitivity figure S(V/K). Signal V_{EXT} allows us to adjust the current consumption $I_{BIAS_{Temp}}$ of the sensor, affecting its response sensitivity S(V/K). The relation between $I_{BIAS_{Temp}}$ and S(V/K) is inversely proportional, thus we can increase the sensitivity of the sensor by reducing V_{EXT}. Current $I_{BIAS_{Temp}}$ should be adjusted depending on the expected PA ΔT (input dynamic margin), providing the maximum sensitivity S(V/K) as possible, while avoiding the sensor response from being saturated.

Finally, digital words $A_0 - A_6$ and $B_0 - B_6$ allow us to precisely set the offset of the sensor output voltage by injecting or extracting current from each branch of the differential structure.

Figure 6.1 shows a diagram that summarizes the temperature sensor pinout and configuration signals of the temperature sensor.

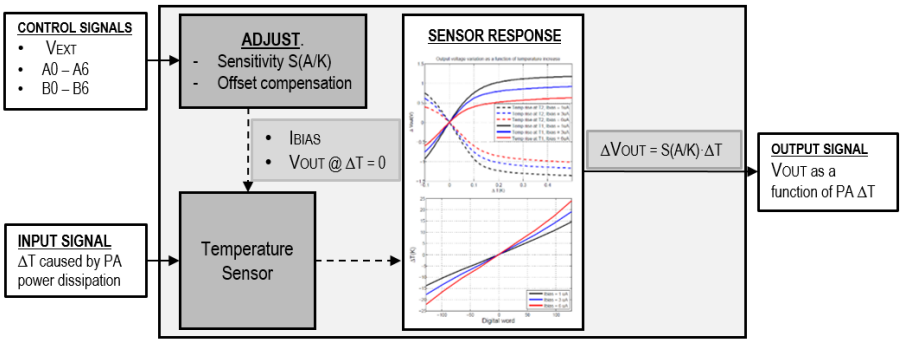

Figure 6.1: Temperature sensor summary diagram

6.1.2 Amplitude detector

The amplitude detector has the following input and output signals:

- V_{ATT}: *Digital input signal.* Enable or disable the attenuator.
- P_{IN}: *Analog input signal.* Signal to be sensed, it can be either the input signal of the PA or the PA output.
- $V_{X_{Det}}$ and $V_{Y_{Det}}$: *Analog output signals.* Response of the sensor. $V_{OUT_{Det}}$ is calculated as the difference between $V_{X_{Det}}$ and $V_{Y_{Det}}$ in differential mode.
- $BIAS_{Det}$ and $V_{G_{Det}}$: *Analog input signal.* Bias the common drain transistors by adjusting the gate DC voltage and current consumption, respectively.

The amplitude sensor will provide an output voltage depending of the amplitude of its input signal. As it was seen in chapter 5, the response sensitivity of the sensor depends on the input power value P_{IN}. The sensor presents a bigger sensitivity S(V/dB) for input power values above approximately 10 dBm than for power values lower than 10 dBm.

The system will contain two amplitude detectors. In the case of the amplitude detector connected to the PA input, its response will not be modified as long as the system RF input signal is kept constant. On the other hand, the amplitude detector connected to the PA output will provide an output value depending on the PA delivered power, hence it will provide us the necessary information to calculate the PA gain

Regarding the control signal V_{ATT}, it can enable or disable ($V_{ATT} = 3.3\,\text{V}$ and $V_{ATT} = 0\,\text{V}$, respectively) the attenuator block to prevent the sensor from being damaged due to large input voltage values. The attenuator will be enabled during the stress mode, and disabled with the PA operating in nominal conditions.

Figure 6.2 shows a diagram that summarizes the amplitude detector input and output signals.

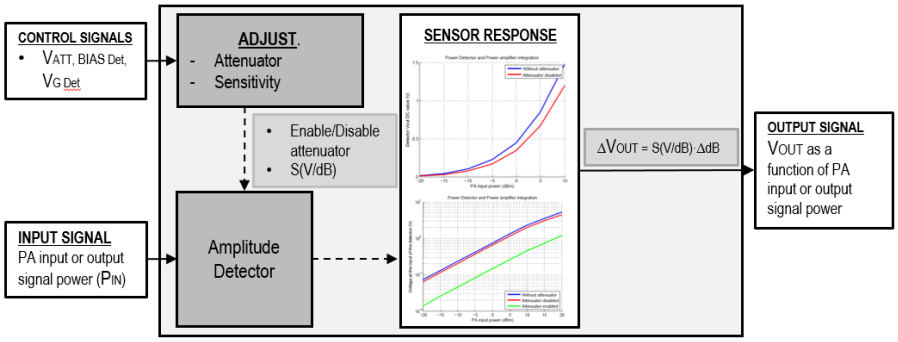

Figure 6.2: Amplitude detector summary diagram

6.1.3 Power amplifier

The power amplifier has the following input and output signals:

- *BIAS*: *Analog input signal.* Adjust the bias current of the PA.
- *PA INPUT SIGNAL*: *Analog input signal.* RF signal that will be amplified.
- *PA OUTPUT SIGNAL*: *Analog output signal.* Amplified signal delivered by the PA to the load.

The power amplifier is biased with a current mirror. This current mirror is externally controlled by the signal $BIAS$, and therefore the PA current I_{BIAS} can be increased or decreased by changing $BIAS$ value.

The PA figures of merit will be directly affected by any current variation. For instance: by decreasing I_{BIAS} we will reduce the amplifier power gain (G_P, or S_{21} if PA is fully matched), its maximum output power (saturated power P_{SAT}) and 1 dB compression point (P_{1dB}). Also, the MOS transistor overdrive voltage V_{OD} will decrease, making PA more prone to be affected by ageing effects.

The system will compensate PA ageing effects with $BIAS$ signal, i.e., power gain drops will be compensated increasing I_{BIAS} current. Thus, it is necessary to know the relation between I_{BIAS} and PA power gain G_P.

Figure 6.3 shows a diagram that summarizes the power amplifier input and output signals.

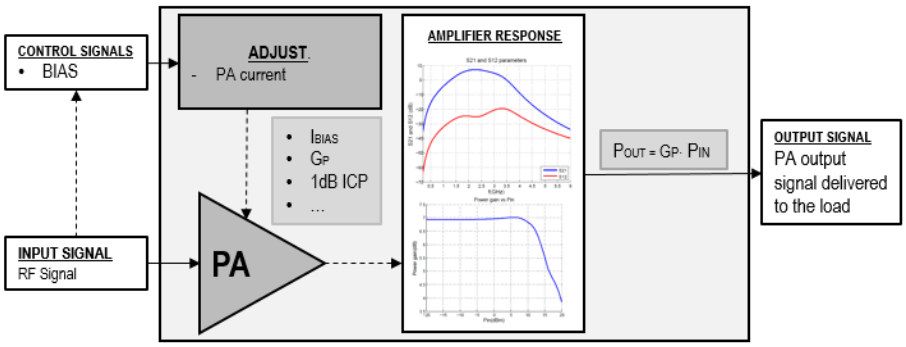

Figure 6.3: Power amplifier summary diagram

Finally, figure 6.4 shows a complete system diagram. This diagram contains all the explained blocks with their respective signals, and pretends to be a completed version of the Figure 1.4 presented in chapter 1. As it can be observed, a control algorithm has been proposed as the feedback loop. The control algorithm will be in charge of preparing and calibrating the system at its startup, stressing the power amplifier and monitoring its performance, and compensating ageing effects by modifying the $BIAS$ signal. The feedback loop will also have a memory unit to store configuration and sensor data. A complete initialization sequence of the sensors and the power will be explained in the following section.

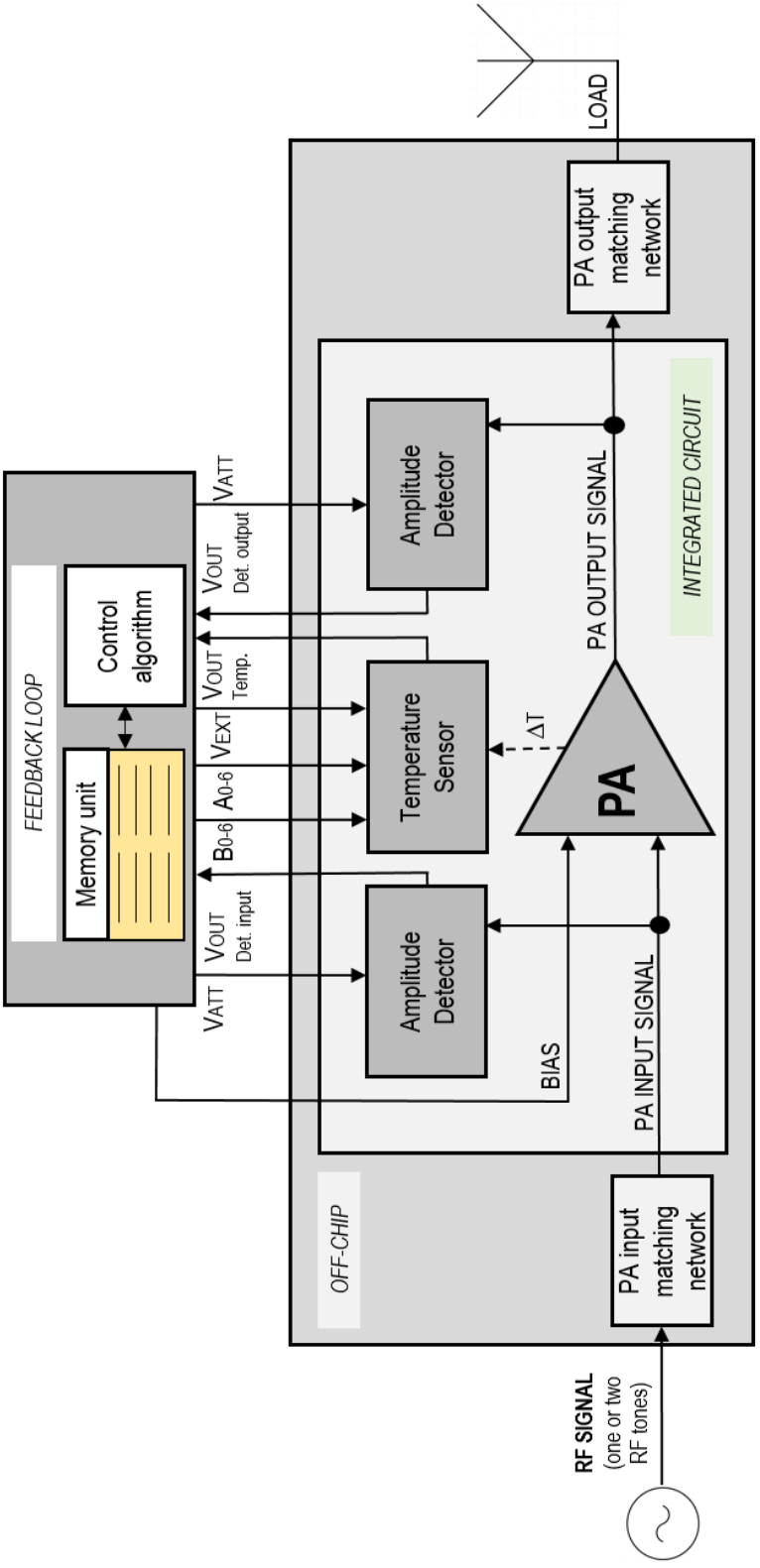

Figure 6.4: Complete system block diagram

6.2 Startup sequence

Startup calibration is typically used for minimizing process and mismatch errors. In this case, calibrating the system when it is powered up will prepare it for further measurements. The following steps are proposed to initiate each block of the system:

- **Power amplifier**: The amplifier is supplied with $V_{DD} = 3.3$V (nominal conditions). Then, its current consumption is adjusted with BIAS signal. For instance, the PA current can be set to 34 mA with BIAS = 2.74 V. With this bias current, the amplifier presents a power gain of 6.9 dB and 1 dB compression point of 14 dBm. In case we modify BIAS value, the PA performance will also be modified.

- **Temperature sensor**: Bias current $I_{BIAS_{Temp}}$ is adjusted with V_{EXT} according to the expected PA temperature variations. Once I_{BIAS} has been set, the temperature of the PA can be measured. This measurement will be done with the PA operating in nominal conditions and no RF signal applied to the PA. With the obtained reading we will know the offset voltage of the sensor response, and adjust it with $A_0 - A_6$ and $B_0 - B_6$ digital signals. Finally, the PA temperature will be measured again, but now with known an RF signal applied to the PA input. The difference between the measured offset voltage and the current measurement will determine the PA temperature ΔT, hence we will be able to calculate the gain figure of the amplifier and consider that the temperature sensor has been properly calibrated and setup.

- **Amplitude detectors**: Bias voltages $BIAS_{Det}$ and $V_{G_{Det}}$ are set to 1.5 V and 1 V, respectively. Then, since these will not be used until we stress the amplifier, attenuators are disabled with $V_{ATT} = 0$ V. To characterise the sensor, we can sweep the RF signal of the system and store the readings of the amplitude detector connected to the PA input. Once the sensor has been characterised, we can calculate the gain of the PA for a given input RF signal by comparing the readings of the detector connected to the PA input and the detector connected to the PA output. Therefore, both amplitude detectors are already prepared for further measurements.

Figure 6.5 illustrates the startup sequence of the three blocks.

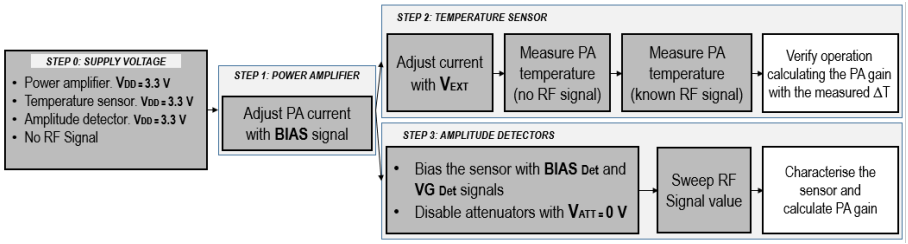

Figure 6.5: Proposed system startup sequence

6.3 Possible measurements

After biasing the power amplifier, calibrating the sensors and calculating the PA gain, the system is able to stress the PA and detect every variation of its performance. There are, however, a series of optional measurements that could be carried out in order to fully characterise the PA and obtain figures of merit such as its 1 dB compression point and bandwidth. A few of these measurements are listed below.

Measurements with amplitude sensors

- The bandwidth of the power amplifier can be measured by sweeping the frequency of the RF signal and reading the response of the detector connected to the output of the PA. Since we characterised the sensor during its startup, we can relate every output voltage with the PA output power, and therefore we will just need to observe when the PA output power has dropped 3 dB.
- Similarly, the 1 dB compression point of the PA can be measured. In this case, the frequency of the RF signal will be constant, and the RF signal power will be swept. The P_{1dB} figure will be observed when the PA output power has dropped 1 dB.

Measurements with the temperature sensor

- Measurements with temperature sensor can be done either with homodyne or heterodyne technique. PA bandwidth and 1 dB compression point can be calculated in both cases using the same methodology as with the amplitude detector, i.e, sweeping the RF signal frequency in the case of bandwidth measurements, and the RF signal power in the case of P_{1dB}.

6.4 Feedback loop requirements and implementation

The feedback loop must be able to manage with all the digital and analog signals of the system, i.e, it must be able to read the output of the sensors as well as to modify the value of their input signals. In other words, it should contain the required number of analog-to-digital converters ($V_{OUT_{Temp}}$, $V_{OUT_{Det}}$), digital-to-analog converters ($BIAS$, V_{EXT},...) and general purpose input-output pins. Also, it should be able to communicate with the supply source of the PA in order to automate the process of switching its supply voltage from nominal to stress values. Besides, it must have a memory unit to store all the necessary data such as the P_{IN}- $V_{OUT_{Det}}$ transfer curve of the amplitude detectors.

With regards to all these considerations, using a Field Programmable Gate Array (FPGA) or a microcontroller could be a suitable solution. In any case, the implemented solution must have all the mentioned requirements in addition to enough computational resources.

6.5 Scenarios

The system must be able to stress the PA and compensate performance variations of this. However, it is very difficult to predict and quantify the expected degradation of the power amplifier.

Mobility and threshold voltage parameters of the MOS transistor will be modified due to ageing effects, and consequently the PA current will change, affecting the amplifier figures of merit. Ageing effects will be forced by stressing the PA, increasing its supply voltage. Nevertheless, the impact of the forced stress on MOS parameters depends on several factors such as the time of application, fabrication technology and bias conditions.

For instance, the work presented in [1] shows measurements of ageing effects in transistors of a 0.35 µm CMOS technology. The work reports reports DC current degradations of about 10% when an NMOS is stressed with $V_{DS} = 4.4\,\mathrm{V}$ during 15 minutes. On the other hand, current variations of 30% were observed with a 65 nm power amplifier [2] suffering combined V_{DD} and RF stress.

Taking this into account, two possible current reduction scenarios have been considered: moderate degradation scenario with a current reduction of 10%, and strong degradation scenario with a current reduction of 25%. Tables 6.1 and 6.2 contain a total of eight examples combining the two proposed scenarios, two different RF signal power values (0 dBm and 10 dBm) and two PA bias current values (34 mA and 12 mA).

The values of amplifier power gain G_P and P_{1dB} and the output of the amplitude sensor (connected to the output of the amplifier) are analysed for each one of the examples. The PA current reduction due to ageing effects have been simulated by decreasing the $BIAS$ value. Three important conclusions can be obtained from the results.

As it was explained in chapter 5, the amplitude sensor has a bigger sensitivity for PA input power values above 0 dBm. It is confirmed by simply comparing $\Delta V_{OUT_{Det}}$ with $P_{RF} = 0\,\mathrm{dBm}$ and $P_{RF} = 10\,\mathrm{dBm}$. Therefore, it will be easier to detect PA degradation if this operates with input power values close to the 1 dB compression point.

The simulated ageing effects (translated into 10% and 25% current reduction) will have a bigger impact on the PA performance for low V_{OD} values as it was stated in chapter 3. For example, in the strong degradation scenario, the gain of the PA would be reduced in 0.296 dB with $I_{BIAS} = 34\,\mathrm{mA}$ ($V_{OD} = 400\,\mathrm{mV}$), while it will be reduced in 0.52 dB with $I_{BIAS} = 12\,\mathrm{mA}$ ($V_{OD} = 211\,\mathrm{mV}$). Hence, it will be possible to increase the effect of stressing the amplifier by reducing its bias current at expenses of gain.

Finally, it will be desirable that the PA suffers the worst degradation as possible to obtain large sensor output variations $\Delta V_{OUT_{Det}}$. Large $V_{OUT_{Det}}$ variations will be more precisely read by the sensors and the monitoring of PA performance will be more accurate.

			Before stress			*After stress*		
Scenario	**PA I_{BIAS}(mA)**	P_{RF}**(dBm)**	G_P**(dB)**	P_{1dB}**(dBm)**	$V_{OUT_{Det}}$**(mV)**	G_P**(dB)**	P_{1dB}**(dBm)**	$V_{OUT_{Det}}$**(mV)**
10%	34	0	6.9	13.55	343.6	6.785	13.56	336.9
		10	6.9	13.55	1196	6.785	13.56	1144
	12	0	5.6	15.74	250	5.43	16.46	238.8
		10	5.6	15.74	849.1	5.43	16.46	830.3
25%	34	0	6.9	13.55	343.6	6.604	13.6	324.6
		10	6.9	13.55	1196	6.604	13.6	1068
	12	0	5.6	15.74	250	5.08	18.32	217.8
		10	5.6	15.74	849.1	5.08	18.32	792

Table 6.1: Simulated PA degradation scenarios

			Increment		
Scenario	**PA current (mA)**	P_{RF}**(dBm)**	ΔG_P**(dB)**	$\Delta V_{OUT_{Det}}$**(mV)**	ΔP_{1dB}**(dB)**
10%	34	0	-0.115	6.7	0.01
		10	-0.115	52	0.01
	12	0	-0.17	11.2	0.72
		10	-0.17	18.8	0.72
25%	34	0	-0.296	19	0.05
		10	-0.296	128	0.05
	12	0	-0.52	32.2	2.58
		10	-0.52	57.1	2.58

Table 6.2: Simulated PA degradation scenarios

6.6 Ageing effects compensation methodology

To conclude this chapter, a compensation methodology is proposed, thus closing the entire operation sequence: startup and calibration, possible measurements using the available sensors, PA stress and performance degradation compensation. The suggested methodology is based on an iterative process. The value of $BIAS$ signal is slowly increased, and the gain of the amplifier is calculated with the sensors readings. This process is repeated until the calculated G_P has reached its initial value, i.e. the value measured before stressing the PA.

- Measure the current state of the PA. Read the outputs from both amplitude detectors and the temperature sensor and calculate the PA gain. Then, check that the obtained values correspond to the expected ones, taking into account the used $BIAS$ value.
- Enable the attenuators of amplitude detectors with $V_{ATT} = 3.3\,\mathrm{V}$ and increase the supply voltage of the power amplifier during a period of time (for exemple, from 15 to 20 minutes). No measurements will be taken during this mode.
- Decrease the PA supply voltage down to 3.3 V and disable the attenuators with $V_{ATT} = 0\,\mathrm{V}$. Read the output of the sensors and calculate the new amplifier power gain. Mobility and threshold voltage of the PA transistor will have changed due to induced ageing effects, reducing the amplifier current. To compensate this current reduction and recover the initial PA G_P value, it will be necessary to increase the value fo $BIAS$ signal.
- Gradually increase $BIAS$ value and measure the PA gain until the initial G_P gain is achieved. The initial power gain value will have been recovered at expenses of increasing the PA current consumption.

  Figure 6.6 illustrates the above mentioned procedure.

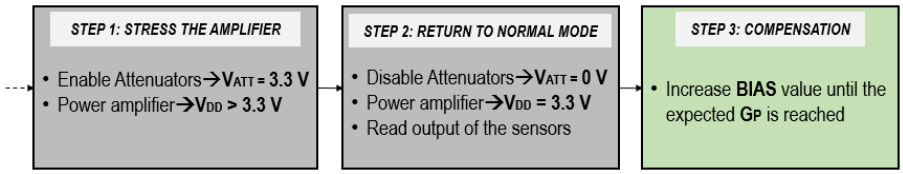

Figure 6.6: Proposed compensation methodology

6.7 References

[1] P. Habas et al. “Characterization of hot-carrier aging of a 0.35 mu;m fully overlapped-LDD CMOS technology”. In: *Proceedings of International Conference on Microelectronics*. Vol. 1. Sept. 1995, 197–202 vol.1.

[2] A. Crespo-Yepes et al. “MOSFET degradation dependence on input signal power in a RF power amplifier”. In: *Microelectronic Engineering* 178.Supplement C (2017). Special issue of Insulating Films on Semiconductors (INFOS 2017), pp. 289–292. ISSN: 0167-9317. URL: http://www.sciencedirect.com/science/article/pii/S0167931717302186.

CHAPTER 7

Conclusions

7.1 Conclusions

A self-healing system composed by a CMOS RF power amplifier, built-in sensors and a feedback loop for variability monitoring and compensation has been presented in this work. The following points provide a summarised view of what has been done, verifying that the goals stated in Chapter 1.5 have been accomplished.

- An RF power amplifier (PA) has been chosen to be the device under test (DUT) of the system. A single-transistor common-source Class A power amplifier has been designed. This presents a power gain of 6.9 dB tuned at 2.45 GHz, with a current consumption of 34 mA. All the PA signals can be externally controlled and observed: input and output RF signals, bias current and supply voltage, providing the system a full control over the DUT and meeting the following goals: to be able to compensate DUT performance degradation using externally controlled knobs, and to be able to accelerate ageing effects modifying the bias of the DUT.

- Two amplitude detectors have been designed and connected to the input and output PA terminals. These sensors allow us to fully monitor and track the PA input and output signals power with a sensitivity of 44.7 mV/dB and a current consumption of 1.2 µA. An attenuator has been connected to the detector input terminals to protect them against large voltage values. This attenuator can be externally enabled or disabled depending on the PA operation condition (nominal or stress mode).

- Furthermore, a temperature sensor has been implemented to monitor the PA temperature. A comparison between MOS and BJT transducers has been first done to characterise their behavior as thermal sensing devices. Then a conditioning circuit has been analysed, designed and validated with simulations. The designed temperature sensor is able to detect small PA temperature variations with a large response sensitivity of 9.5 V/K and a current consumption of 1 µA. The sensor output offset voltage can

be adjusted with digitally controlled current sources. Besides, sensitivity can be externally adjusted modifying the sensor bias current.

The development of these sensors has made it possible to accomplish the goal of monitoring several DUT figures of merit in order to detect if ageing effects have altered its performance, combining both the classical method using power amplifiers and thermal sensing.

- Finally, A feedback loop has been evaluated and proposed to compensate DUT degradation. A system startup sequence has been proposed to configure and calibrate the entire system at its power up, and a compensation algorithm has been suggested to stress the DUT, monitor the possible performance variations and compensate them with the implemented knobs.

7.2 Future work

As it can be observed, all the objectives have been accomplished in the framework of this master thesis. However, some tasks are still pending in order to complete the system:

- Finish with the circuit layout and prepare it for the manufacturing phase.
- To analyse in detail the technical requirements of the feedback loop and compare between all the possible solutions.
- To choose the most suitable solution and implement the control algorithm.
- To validate the manufactured IC performance in open loop configuration: check the correct amplifier and sensors operation.
- To close the loop by adding the feedback solution and validate the system operation in closed loop configuration: stress the amplifier, observe the PA performance degradation and compensate it.