Modulation Techniques applied to Medium Voltage Modular Multilevel Converters for Renewable Energy Integration: A review

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Abstract

Modular multilevel converters (MMC) inherent features are gaining more attention for dc voltage transmission systems. One of the main research paths regarding the converter performance deals with its voltage modulation. Specifically for medium voltage applications with relatively small number of submodules, the voltage modulation techniques impact on the MMC performance needs to be studied.

This work provides an extensive review of the carrier-based pulse with modulation (CB-PWM) techniques proposed to be applied on previous multilevel inverter versions. The CB-PWM methods were adapted to be compatible with an additional cell ranking and selection algorithm to ensure equal energy distribution on the arm cells. The state-of-the-art of zero sequence signals (ZSS) applied on three-phase inverters is also reviewed. The alliance between the ZSS with the CB-PWM, as well as the nearest level modulation (NLM), has an important impact on the MMC harmonic content, efficiency and voltage ripple of its cells capacitors. A 15 MW 28-cell-based MMC is used to investigate each particular combination between the modulation method and the common mode ZSS.

Keywords

≪ MMC ≫, ≪ Pulse Width modulation (PWM) ≫, ≪ Losses ≫, ≪ Power Quality ≫

1 Introduction

The modular multilevel converter (MMC) is a reasonably young inverter technology with a promising future in medium voltage DC (MVdc) systems, such as large wind turbines in the DC collection grids, large PV integration, large marine current and wave energy integration [1–4]. Modularity, redundancy and high quality voltage waveforms make the MMC a viable solution for dc transmission applications [5–8]. However, the arms voltage management evokes several concerns on its performance.

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Over time, several modulation techniques have been proposed to compile the required ac voltage at the output of the multilevel-based voltage source converters [8–15]. Most of the proposals were carrier-based PWM (CB-PWM) and depending on the nature of the corresponding carrier, different pulse patterns are applied to the converter's switches. Hence, different voltage profiles and performances were conceived for the VSC's.

This work presents a review of the CB-PWM techniques proposed for the previous multilevel VSC generations. Then, the relating strategies were considered to shape the voltage generated on the MMC's arms in combination with an additional capacitor's energy balancing algorithm. Additionally, the performance of the presented modulation strategies was complemented with the impact analysis of the zero sequence signals (ZSS) injection into the MMC arms modulation. A medium voltage-based MMC model with 15 MW/ 28 submodules is embraced to analyze the impact of several arm voltage modulation strategies on the converter performance, namely, on its efficiency, capacitors ripple and quality of its waveforms.

This paper is organized as follows: Section 2 presents and discusses several modulation strategies and zero sequence signals proposed in the literature that can be used to improve the operation of the inverters. The methodology followed to assess the performance of the MMC is discussed in Section 3. The impact of the modulation strategies on the converter performance is then argued in Section 4. The final remarks are presented in Section 5.

2 Multilevel modulation techniques

Several modulation strategies have been introduced to drive multilevel converters, namely for Neutral Point Clamped (NPC) [16], Flying Capacitor (FC) [17] and Cascaded H-Bridge (CHB) [18–22] and, more recently, modular multilevel converters [23, 24]. The first three VSC structures require proper PWM-controlled strategies to balance the energy storage of their dc-bus capacitors, without the use of additional hardware [25, 26]. Once the control scheme of these converters determines the require voltage target for their output u_j^*, it is normalized in accordance with the maximum voltage amplitude achievable at the VSC's output, particularly, the dc-bus voltage U_{dc} as:

$$m_j^* = u_j^*/U_{dc} \tag{1}$$

The correspondent modulation index m_j^* of a M-level converter is then compared with (M-1) carriers, resulting then in 2(M-1) logical signals to drive the correspondent switches of each converter leg. The intrinsic features of each CB-PWM techniques and their redundant voltage vectors are responsible for balancing the dc capacitors voltages [21].

In terms of the MMC, as presented in Figure 1, the energy is no longer stored on its dc side bus but instead in the capacitors placed inside the submodules (SM). Due to the converter nature, the grid currents flow directly on the SM's capacitors and this situation establishes a great voltage

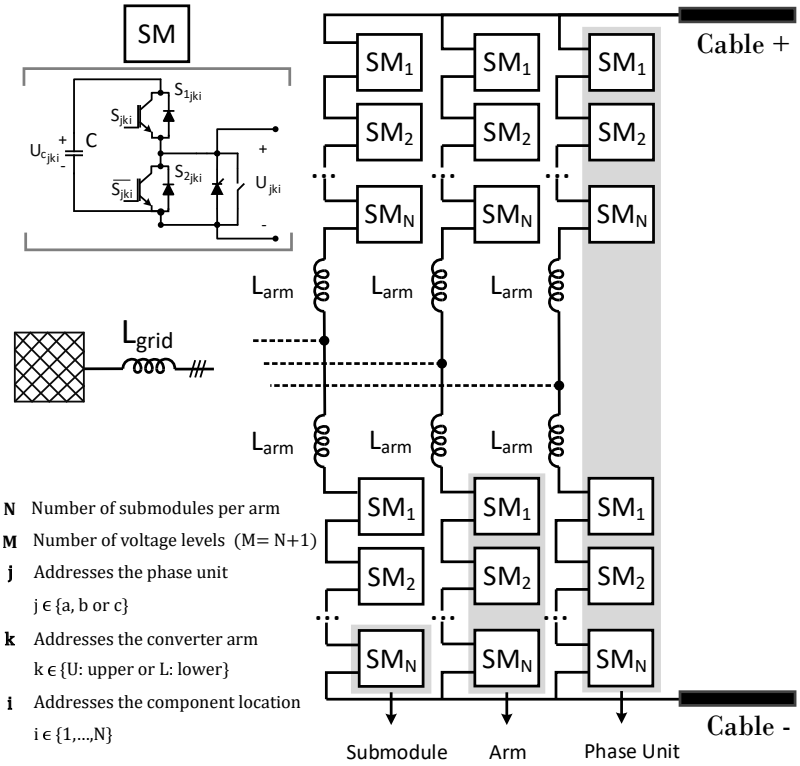


Figure 1: Three-phase circuit of the modular multilevel converter.

ripple variation. As a result, the energy stored in the capacitors tends to diverge over the time, which emerges the need for balancing their energy to achieve a proper converter operation [27,28]. This goal is addressed by selecting the proper redundant voltage vectors on the MMC arms, but this stage is done by means of a selective control of the cells.

So, if in the NPC, FC and CHB solutions, the CB-PWM techniques are used to shape their output voltages and to balance the energy storage of their floating capacitors [29], regarding the MMC this is done in more stages. The consequent stage of defining the required voltage to be synthesized across the converter arms u^*_{jk} is the determination of the arm modulation index target m^*_{jk}(2). Later on, the suitable number of on-state cells are determined by means of the multilevel modulation schemes. Thereupon, the cell selection methods are required to ensure controlled energy distribution between the capacitors within the same stack [27,30]. The flexibility allowed by sorting and selecting the MMC capacitor's to be inserted, besides the knowledge of their individual voltages, also permits a decision on which capacitors are inserted in the chain depending on the SM's semiconductors temperatures [31].

$$m^*_{jk} = \frac{u^*_{jk}}{U^{\Sigma}_{jk}} \tag{2}$$

The arm voltage modulation stages applied in the MMC are depicted in Figure 2. The stage 1 is defined by the admittance of zero sequence signals injection into the converter modulation, which is discussed in Section 2.1. The second stage consists in defining the suitable number of capacitors that should be inserted on the converter arms. Several techniques can be embraced and

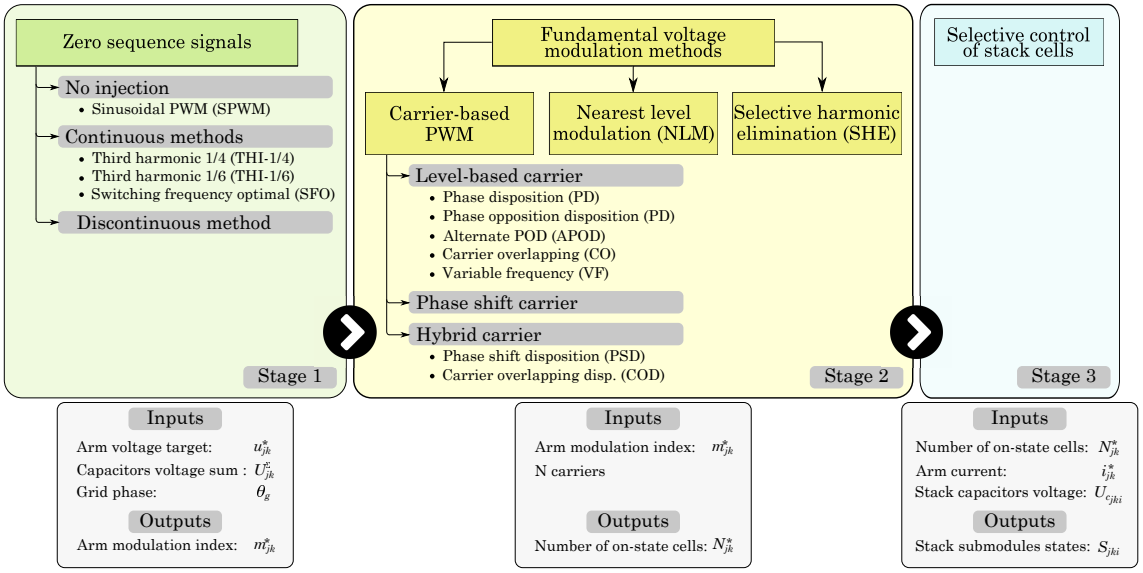


Figure 2: Overall voltage modulation stages of modular multilevel converters.

further analysis is presented in Section 2.2. In Section 2.3 the selective control scheme of the MMC cells is explained.

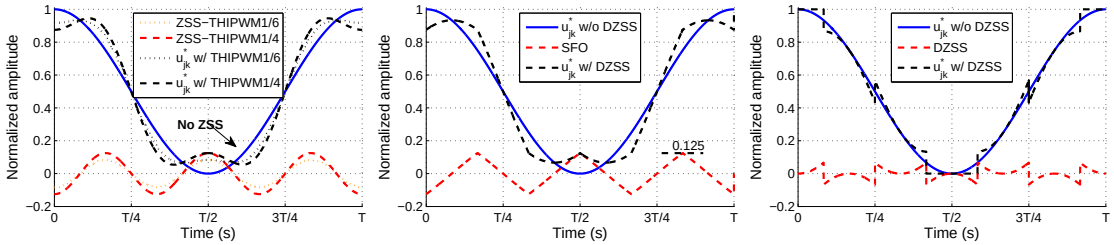
2.1 Zero sequence signals (ZSS)

Zero sequence signals (ZSS) are triple order harmonics that can be added to the modulation signals of the three-phase-based power converters to improve their performance. The injection of third harmonic odd-multiple signals (H_3,H_9, H_{15},...) into the modulation of the three-phase converters, these harmonics will be canceled on the line-to-line output voltages. The ZSS are used to address some goals such as harmonic spectrum reduction of the ac grid currents, increase the converter efficiency and to increase the linear range of the converter's modulation indexes [7,32–40].

If no ZSS is considered, it is designated in this work as sinusoidal PWM (SPWM). Otherwise, depending if they are derivable in the time domain, as illustrated in Figure 2, the ZSS signals are classified in this work as continuous or discontinuous.

2.1.1 Third Harmonic (THI)

The third harmonic-based ZSS (THI-ZSS) is a continuous common mode signal that is injected into the voltage modulation of the VSCs, mainly used to maximize the usage of their dc-bus. The THI-ZSS is illustrated in Figure 3(a). On two level inverters the amplitude of the THI-ZSS influences the performance of the converters differently. If a third harmonic ZSS with (1/6) of the converter's *emf* magnitude is considered, the linear range of the VSC is extended by ≈15.5 % in comparison with the SPWM, which is the maximum achievable on the VSCs [32,34]. Therefore is the typical ZSS solution accepted [7,32,34,41]. On the other hand, the injection of a third harmonic common mode signal with (1/4) of the converter's output voltage target into its modulation, the harmonic spectrum on the output voltages are minimized [32].



(a) (b) (c)

Figure 3: The ZSS injected on the MMC's arm voltage modulation: (a) a third harmonic, (b) switching frequency optimal (SFO) and a discontinuous-ZSS.

2.1.2 Switching frequency optimal (SFO)

This technique is also called naturally sampled space vector modulation (SVM) [10,37,42]. This ZSS technique is commonly used in ac drives applications [33] and it is illustrated in Figure 3(b). The ZSS-SFO curve is identical with a triangular curve, but in reality it is achieved by means of trigonometric functions [43].

The amplitude of the triangular waveform is equal to (1/4) of the output voltage magnitude desired for the converter and, conjointly with the THI (1/6), the linear range of the VSC's voltage modulation is extended by 15 % in comparison with the SPWM [44, 45].

Several combinations between the CB-PWM techniques with the SFO-ZSS were studied [12,37, 46]. Particulatly on a GTO-tyristor inverter, the aggregation of the APOD, PD and CO methods with the SFO-ZSS reduces the distortion factor of the grid currents, when compared to the CB-PWM techniques on their own [46]. Moreover, the SFO can slightly reduce the total harmonic distortion (THD) in the line-neutral voltages for particular modulation indexes when combined with PD or CO [12, 37].

2.1.3 Discontinuous ZSS (D-ZSS)

In the discontinuous ZSS an offset is added to the modulation index target in such a way that voltage generated at the VSC's output is clamped to a particular voltage level. In the literature it is shown that its possible to clamp the converter voltages over 30, 60, and 120 degrees intervals [33,34,47], and during those intervals the switching events are avoided [48,49]. Figure 3(c) shows an equivalent VSC's voltage reference when it is clamped on its top over 60 degrees. This particular case is commonly referred in the literature as the flat top D-ZSS. In this work, the MMC arm voltages were clamped over the 60 degrees intervals, particularly when the arm currents reach their positive and negative uppermost values [49].

The impact of the combination between the modulation techniques and the ZSS presented on the modular multilevel converter performance was also analyzed and presented in Section 4.

2.2 Fundamental voltage modulation methods

The modulation methods analyzed in this work are classified as carrier-based PWM (CB-PWM), nearest level modulation (NLM) and selective harmonic elimination (SHE) methods and

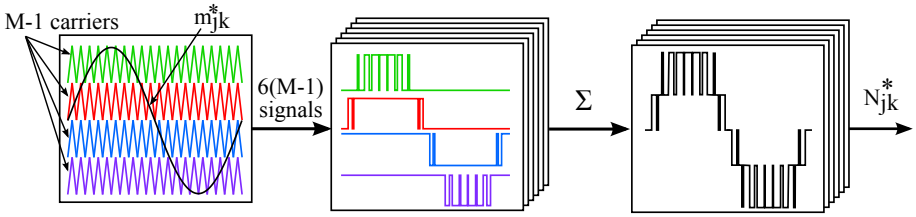


Figure 4: CB-PWM techniques applied in MMC applications.

they are presented in the sections 2.2.1, 2.2.2 and 2.2.3 respectively.

2.2.1 Carrier-based PWM

In a carrier-based PWM applied to a M level inverter, (M-1) carriers are used with particular technicalities as their frequency, amplitude, phase and dc offset. Combining different specifications on those signals entails different modulation strategies, which denote a different behavior of the converter. On the first modulation stage, (M-1) carriers are compared to the MMC arms modulation indexes m_{jk} (3), resulting 6(M-1) modulation patterns. To be compatible with the 'sort and select' algorithm, the six groups of (M-1) firing pulses are added and the target number of inserted capacitors N^*_{jk} (one per arm) is created, as Figure 4 illustrates [50].

$$m_{jk} = u^*_j / U^{\Sigma}_{jk} \tag{3}$$

In this work, the CB-PWM techniques are classified into: level-shifted PWM (LS-PWM), phase shift-carriers PWM-based (PSC-PWM) and hybrid PWM (H-PWM). The LS-PWM is characterized by placing (M-1) carriers in adjacent vertical bands. The PSC-PWM is characterized by having (M-1) carriers with the same amplitude and frequency however, shifted in phase angles. Lastly, the hybrid PWM (H-PWM) merges some characteristics of the LS-PWM and PSC-PWM strategies. The individual details are presented in the next sections.

Level-Shifted PWM

The LS-PWM strategies were mainly proposed to be applied on the multilevel NPC and FC converters [51,52]. The LS-PWM are not a suitable option for CHB converters since they produce an unequal power distribution among the H-Bridge-cells which pollutes the harmonic spectrum of the grid current[1] [52]. However, at the MMC scenario and as mentioned earlier, the CB-PWM (stage 2) are aggregated with the selective control of the submodules (stage 3) to overcome this issue. The individual LS-PWM techniques are briefly described in the following sections.

Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD) and Phase Opposition Disposition (POD): the carriers have the same amplitude and frequency, but

[1]This fact is also extended to the MMC, by the reason of the MMC also being a cascaded-connected-based cell converter.

placed in different levels (offsets) [15]. The carriers on the PD method have the same phase angle, as presented in Figure 5(a). In POD, the carriers above the zero line voltage reference are in phase opposition to those below, as shown in Figure 5(b). In the APOD method, all the carriers are alternatively in phase opposition, as presented in Figure 5(c).

The analytical and experimental comparison of the voltage harmonic spectrum generated by a three-phase/ five-level NPC (5L-NPC) inverter driven by APOD, POD and PD modulation methods was performed in [15, 53]. It was demonstrated that the PD has superior harmonic performance, as long as the carrier frequency is an odd triple multiple of the fundamental frequency, due to the fact that it concentrates significant harmonic energy at the carrier's frequency and it is canceled on the VSC's line to line voltage. Furthermore, if a third harmonic is injected into the output voltage modulation, the PD continues to retrieve better results than the APOD and POD methods in the same conditions [54, 55].

The APOD, POD and PD strategies were also applied to a five-arm-level MMC without any energy balance strategy [56]. In those conditions, a substantial amount of harmonics on the arm voltages and currents was generated due to the fact of the non-controlled and unequal voltage across the capacitors. These CB-PWM techniques, under the refereed conditions, are not suitable for MMC applications [56]. An intermediate mapping between the PD modulation and the firing pulses of the MMC's switches was investigated in [57].

Carrier Overlapping (CO): the carriers share the same frequency and phase, despite the amplitude and offset are designed to overlap the adjacent bands as shown in Figure 5(d) [12]. The overlapping distance between the adjacent carriers is half the value of their amplitude.

This method was compared to the phase disposition methods for a 3-level NPC (3L-NPC) converter [12, 37]. For modulation indexes lower than 0.7, the CO retrieves far less harmonic distortion on the line voltages than the PD methods because the reference intercepts more times the carriers due to the overlapping. On high modulation indexes (m_j >0.8), the harmonics distortion of such methods are similar.

The authors did not find any publications of this strategy applied on the MMC.

Variable Frequency (VF): it is an evolution of the PD method and it was created to equalize the power loss distribution along the NPC levels [10,12]. Whenever the NPC phases are modulated by the phase disposition method, the switches placed on the top/bottom layers commute more often than the ones placed on the intermediate levels. To adjust the transition asymmetry, a carrier with higher frequency was implanted on the intermediate levels as Figure 5(e) illustrates.

In opposition, in terms of the MMC, as the arm current reaches its peak values the voltage of the capacitors trend to drift, which motivates the need for rotating the inserted capacitors more often. Hence, higher frequencies on the top levels were considered to change more often the active

SM reference N_{jk}^{*} as shown in Figure 5(f) [58]. The reference [58] studied the variable-frequency strategy to be applied on the MMC, but with a crescent carrier frequency as the level increases. However, in the case of having unequal and unrelated carrier frequencies in each particular level, the harmonic spectrum is increased on the converter's line voltages. Hence, to avoid this issue, only two frequencies were considered, specifically for the intermediate and top layers.

Phase-Shift Carrier PWM

The phase shifting technique was the first multi-carrier-based PWM strategy presented in the literature. It was used to interleave n two-level converters that were connected in parallel [9]. All the carriers have the same amplitude, frequency and offset, but phase-shifted by $(2\pi/n)$ as shown in Figure 6. This method reduced the voltage ripple on the dc-link capacitors and eliminated certain groups of grid current harmonics [9].

The PSC overcame the asymmetric power distribution among the floating capacitors on the CHB and FC converters [51, 52, 59]. A M-level inverter driven by the PSC-PWM with carrier frequency f_c, significant harmonic content will be seen in the converter line-neutral voltages around $(M-1)f_c$ [55, 59]. Adjusting the frequency of the carriers in the PSC-PWM method, the correspondent voltage harmonic spectrum becomes equal to the APOD method [7, 53, 60].

This modulation mechanism can be used in MMC applications, however with limited bounds because it is not sensitive to the capacitor voltages drifts [61–63]. The reference [50, 64, 65] adapts the PSC-PWM to operate associated with an additional ranking and selection of cells approach.

Hybrid Carrier PWM

The denomination of hybrid-carrier is due to the fact that uses multiple CB-PWM techniques. According their features, can only be applied to converters with odd number of levels.

Phase-Shift Disposition (PSD): it is a combination of the PSC and PD modulation methods [11, 13, 55]. It is used to drive a M-level inverter and it consists of placing two groups of (M-1)/2 carriers waves with the PSC disposition in two adjacent bands in anti-phase as illustrated in Figure 7. This modulation method is characterized by placing significant harmonic content on the phase voltage around $f_c(M-1)/2$ [55]. Which can be adjusted, as well as the PSC, to retrieve similar results as the APOD method [53].

The efficiency of the PSD was analyzed for a 5L-NPC and compared to the previously presented CB-PWM techniques in [13]. The study reveals that, whenever the converter is operating with higher modulation indexes than 0.7, the PSD retrieves fewer switching losses than PD, POD, APOD, CO, PSC and COD, as long as the same carrier frequency is considered on all the correspondent methods [13].

The authors did not find any publications of this PWM strategy applied to the MMC.

Carrier Overlapping Disposition (COD): it is a combination of the CO with other LS-PWM strategies. In a M-level inverter, two groups of (M-1)/2 overlapped carriers are placed in two contiguous bands as Figure 9 shows. The combination of different phase angles for the adjacent carriers formulates different modulations schemes, as the CO-PD, CO-POD and CO-APOD which are formerly introduced in the next sections [66].

The authors did not find any publications of this COD modulation strategy applied to the MMC.

Carrier Overlapping- Phase Disposition (CO-PD): In this strategy the (M-1) carriers share the same phase as Figure 9(a) shows. This modulation technique was compared to PD, APOD, POD, PSC, CO and PSD for a 5L-NPC over the linear and over-modulation ranges [13]. The CO-PD retrieves similar results as the CO, being slightly more efficient for particular low modulation indexes.

Carrier Overlapping- Phase Opposition Disposition (CO-POD): this strategy imposes that the carriers placed on the upper and lower bands have their phase angle rotated by 180 degrees as shown in Figure 9(b).

Carrier Overlap.- Alternate Phase Opposition Disposition (CO-APOD): this method settles that two consecutive carriers are placed in antiphase as Figure 9(c) clarifies. The CO-APOD was proposed to be applied in a 5L-NPC, labeled as SPD in [11].

2.2.2 Nearest level modulation (NLM)

The NLM is a non-carrier method and suitable for MMC-HVdc-based applications [41]. In contrast to the CB-PWM methods, where the individual pulse patterns are added to create the N_{jk}^{*} target, on the NLM this set-point is obtained directly from the arm modulation index m_{jk}^{*} as:

$$N_{jk}^{*} = \text{round}\left(Nm_{jk}^{*}\right) \tag{4}$$

where N is the number of SMs available on the MMC stacks.

In this strategy, the modulator (Nm_{jk}^{*}) is discretized by rounding it to the closest integer number of SMs attainable, as shown in Figure 8. The greater number of levels is, the more accurate the output waveform becomes.

The NLM was proposed to drive a 4 asymmetric-CHB cells (81 level converter) in conjunction to the DTC scheme applied to an induction machine [14]. When compared to a PWM-based modulation, as the number of voltage levels is higher, the NLM shows a clear reduction of the number of switching events [14, 51].

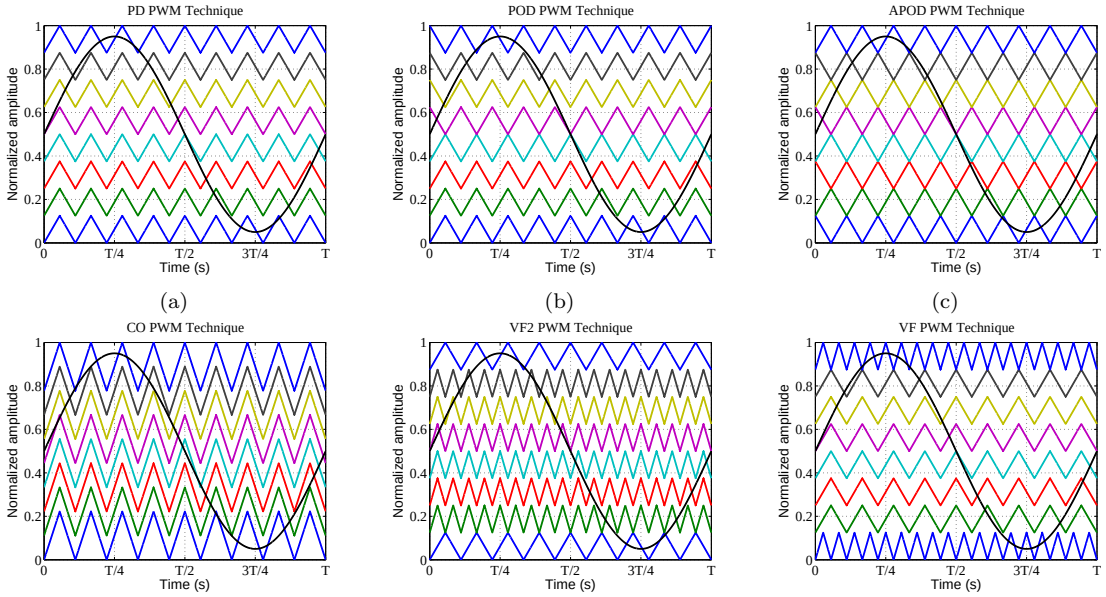


Figure 5: Level-Shifted PWM strategies:(a) Phase Disposition, (b) Phase Opposition Disposition, (c) Alternate Phase Opposition Disposition, (d) Carrier Overlapping and (e) Variable Frequency - original approach, (f) Variable Frequency - MMC-based approach.

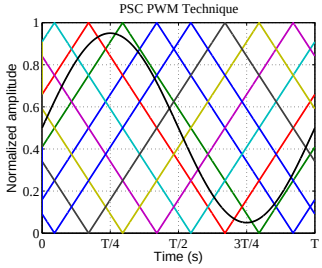


Figure 6: PSC-PWM strategy.

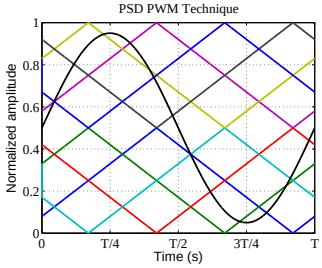


Figure 7: PSD-PWM strategy.

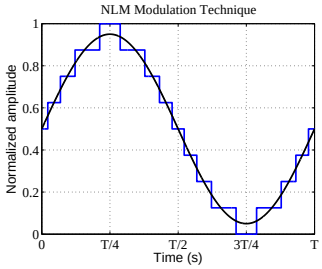


Figure 8: NLM strategy.

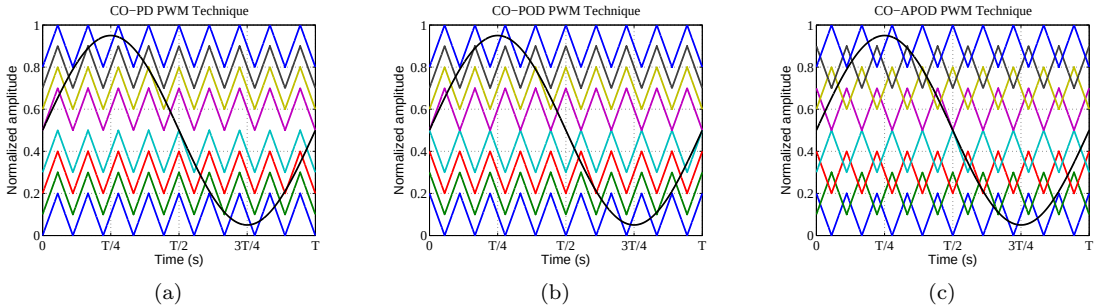


Figure 9: Carrier Overlapping disposition strategies: (a) Carrier Overlapping with Phase Disposition, (b) Carrier Overlapping with Phase Opposition Disposition and (c) Carrier Overlapping with Alternate Phase Opposition Disposition.

The NLM was first applied in MMC applications in 2010 [67], and since then, has been widely used to drive this converter structure in HVdc applications [6, 41, 61, 68].

2.2.3 Selective harmonic elimination (SHE)

The SHE is also called programmed harmonic elimination method. This modulation method consists of an optimization technique that, in accordance with the desired objective function, provides the firing pulses that should be applied on the semiconductors [69–74]. It can be applied either in real-time or in an offline mode, and is commonly adopted on power converters to minimize the switching losses, torque pulsations and/or elimination of particular low-order harmonics [75,76].

On multilevel converters composed of an high number of voltage steps, they can synthesize low-harmonic content-based voltage waveforms and, therefore, this modulation strategy becomes unsuitable [6,30,61]. The author could not find the SHE for MMC applications with more than 20 levels. Therefore, due to the relatively high number of levels of the MMC-based case study, this method was not considered in this study.

2.3 Selective control of the submodules

The consequent step of determining the target N_{jk}^{*} is the generation of the individual firing signals for the converter switches, in such a way that balances the energy storage of the individual capacitors. The schematic of the 'sort & select' algorithm is illustrated in Figure 10. The sorting algorithm (1) ranks the converter capacitors by their voltage $U_{c_{jki}}$. Then, depending on the arm current flow direction i_{jk}, the first or the last N_{jk}^{*} capacitors of the ranked list are selected in (2). As long as the target N_{jk}^{*} is not changed, the capacitors that are inserted on the stacks are not rotated.

As mentioned, this is accomplished by generating a firing pulse with a value 1 or 0 in $S_{jki}(t)$, to respectively insert or bypass the capacitor placed in the jki position. The cell selection algorithm embraced in this work to analyze the arm modulation impact on the converter perfornace is named as classic cell selection method and further details are provided in [24]. The referred strategy is capable of ensuring a symmetrical energy distribution among the capacitors assembled in the same stack [77]. Due to the high rotation of the inserted capacitors motivated by the sorting method adopted, the voltage differences across the capacitors are negligible. Hence, from the harmonic generation perceptive, the classic method for sorting the capacitors has an almost residual impact on the harmonic content of the converter.

3 Methodology followed to assess the converter performance

The impact of the presented modulation techniques and the corresponding aggregation with the ZSS were analyzed at steady-state conditions in terms of the semiconductor's power losses,

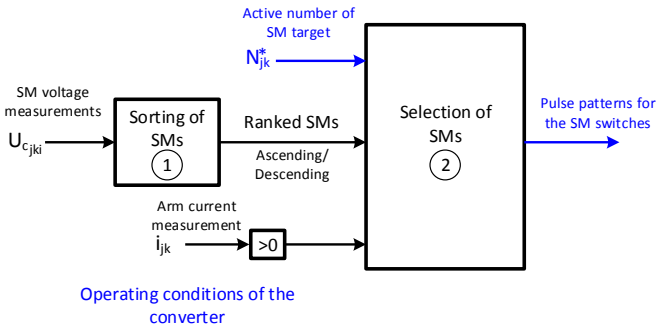


Figure 10: Overall scheme of the classic selection method.

harmonic distortion factors of the grid currents and arm voltages, and finally, the voltage ripple of the SM capacitors. This study was based on the point-to-point dc transmission scheme of Figure 11. The MMC1, which was modeled as a current source, injects a constant power at the transmission link, whereas MMC2 is responsible for managing the pole-to-pole voltage at the dc bus. The converter 2 are characterized by the parameters shown in the Table 1. The modulation strategies presented have been implemented on the MMC2, whose performance is being studied in this work.

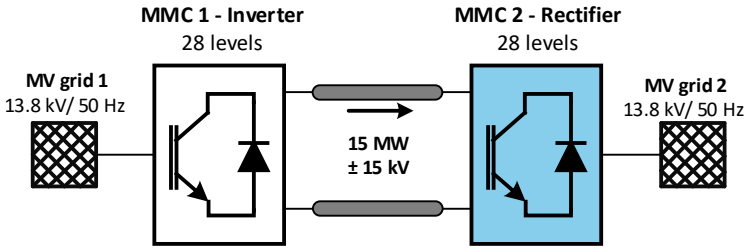


Figure 11: MMC-MVdc transmission system analyzed.

The methodology used to operate and control the MMC2 is presented in Section 3.1. The quantification of the semiconductor's power losses is explained in Section 3.2. The semiconductor's power losses and the harmonic content retrieved by the CB-PWM techniques greatly depend on the frequency that is adopted for the correspondent carriers. Therefore Section 3.3 presents the reasoning adopted in the carrier's frequency design.

Table 1: Circuit Parameters used for simulation

Parameters	Notation	Value
Number of submodules/arm	N	28
Rated active power	P	15 MW
Power factor	$\cos\phi$	1
Line voltage	U_{LL}	13.8 kV
Grid frequency	f_{grid}	50 Hz
dc-bus voltage	U_{dc}	$\pm$ 15 kV
Cell capacitance (35 kJ/MW)	C	4.5 mF
Nominal submodule voltage	$\bar{U}_{c_{jki}}$	1200 V
Arm inductance	L_{arm}	20 mH
Grid Inductance	L_{grid}	5 mH
Parasitic resistance of the inductors	R	0.1 Ω

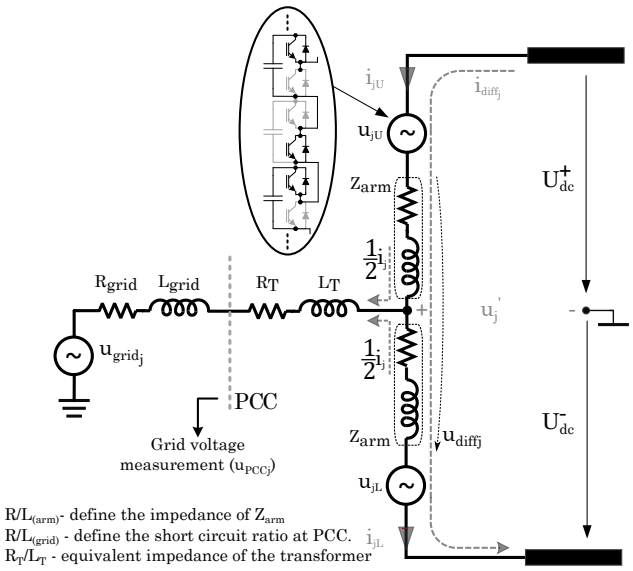


Figure 12: MMC equivalent circuit of one phase unit.

3.1 MMC operation and control

To provide a mathematical description of the dynamic behavior of MMC2, the progressive change of the inserted number of low-voltage-based capacitors can be approximated by a voltage source u_{jk}, as shown in Figure 12. Depending on the voltages that are synthesized at the arms, the converter electromotive force (*emf*) e_j and the voltage drop across the series-connected arm impedances u_{diff_j} are respectively managed as (5) and (6) [78].

$$e_j(t) = \frac{u_{jL}(t) - u_{jU}(t)}{2} \tag{5}$$

$$u_{diff_j}(t) = U_{DC}(t) - (u_{jU}(t) + u_{jL}(t)) \tag{6}$$

Admitting that the *emf* dynamics (5) and inner voltage drop dynamics (6) are independently managed, these variables are responsible to handle the electrical current injection into ac grid i_j (7) and the inner current flow (8), respectively [78].

$$e_j = u'_j(t) + \frac{R_{arm}}{2} i_j(t) + \frac{L_{arm}}{2} \frac{\mathrm{d}i_j(t)}{\mathrm{d}t} \tag{7}$$

$$u_{diff_j}(t) = 2\left(R_{arm} i_{diff}(t) + L_{arm} \frac{\mathrm{d}i_{diff}(t)}{\mathrm{d}t}\right) \tag{8}$$

Therefore, these variables are used to manage the MMC energy storage. As a consequence of its decentralized approach to store energy, any current flow difference between the MMC arms (9)

lead to the uneven energy storage condition between its six stacks.

$$\begin{cases} i_{jU}(t) = i_{diff_j}(t) + \dfrac{i_j(t)}{2} \\ i_{jL}(t) = i_{diff_j}(t) - \dfrac{i_j(t)}{2} \end{cases} \tag{9}$$

When the MMC energy balancing topic comes to discussion three types of energy control are identified. The vertical balancing between the upper and lower stacks of the MMC, which enables the establishment of similar voltage ranges across them. The parallel connection between the converter legs may lead to inrush currents flowing between them, which motivate the need for balancing their energy storage (horizontal balancing). The vertical and horizontal energy distribution can be controlled by imposing the proper harmonic frequencies on the inner current flow i_{diff_j} [78, 79]. The third energy balancing procedure refers to the energy distribution between the capacitors assembled on the same stack, which is achieved by a selective control of the submodules states [61, 80].

Aligned with what was mentioned, the block diagram with the overall control scheme of the MMC is depicted in Figure 13. From the voltage measurement of the 6 groups of N capacitors that build each stack, the energy stored at each particular stack E_{jk} (10) is determined in stage (1). Moreover, this stage also determines the global energy storage E_T (11). Consequently, Figure 13 presents two main control directions for this converter, namely its inner dynamics (blocks 2 to 5) and interactions with the ac grid (block 6 to 8).

$$E_{jk}(t) = \sum_{i=1}^{N} E_{jki}(t) = \sum_{i=1}^{N} \left(\frac{1}{2} C U_{c_{jki}}^2 \right) \tag{10}$$

$$E_T(t) = \sum_{\substack{j \in \{a,b,c\} \\ k \in \{U,L\}}} E_{jk}(t) \tag{11}$$

Regarding the inner dynamics, the energy storage deviation between the converter legs E_{jj}^{Δ} (12) and upper/ lower stacks E_j^{Δ} (13) are calculated in stage (2).

$$E_{jj}^{\Delta}(t) = \begin{bmatrix} E_{ab}^{\Delta} \\ E_{bc}^{\Delta} \\ E_{ca}^{\Delta} \end{bmatrix} = \begin{bmatrix} (E_{aU} + E_{aL}) - (E_{bU} + E_{bL}) \\ (E_{bU} + E_{bL}) - (E_{cU} + E_{cL}) \\ (E_{cU} + E_{cL}) - (E_{aU} + E_{aL}) \end{bmatrix} \tag{12}$$

$$E_j^{\Delta}(t) = \begin{bmatrix} (E_{aU} - E_{aL}) \\ (E_{bU} - E_{bL}) \\ (E_{cU} - E_{cL}) \end{bmatrix} \tag{13}$$

In order to accomplish identical energy distribution among the six stacks, the energy deviation targets for its legs and arms, respectively modeled as $E_{jj}^{\Delta *}$ and $E_j^{\Delta *}$, were set to zero. To address

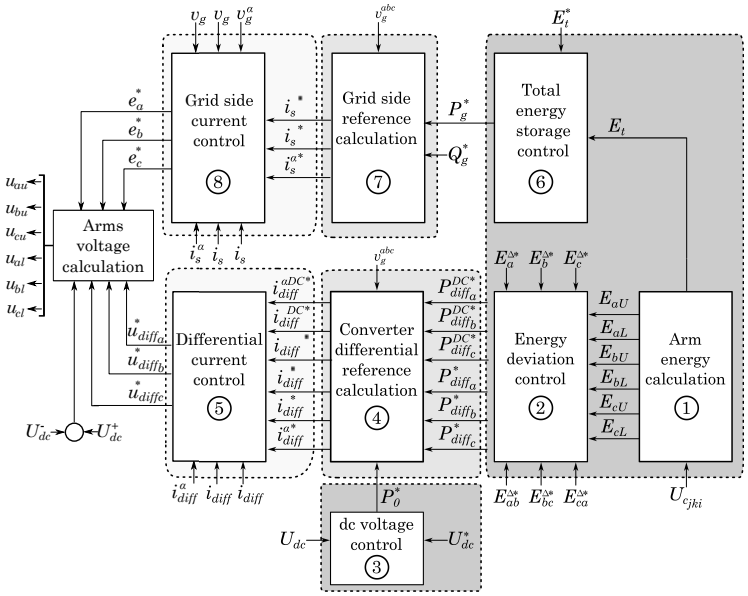


Figure 13: Control scheme used to manage the MMC in the HVdc applications.

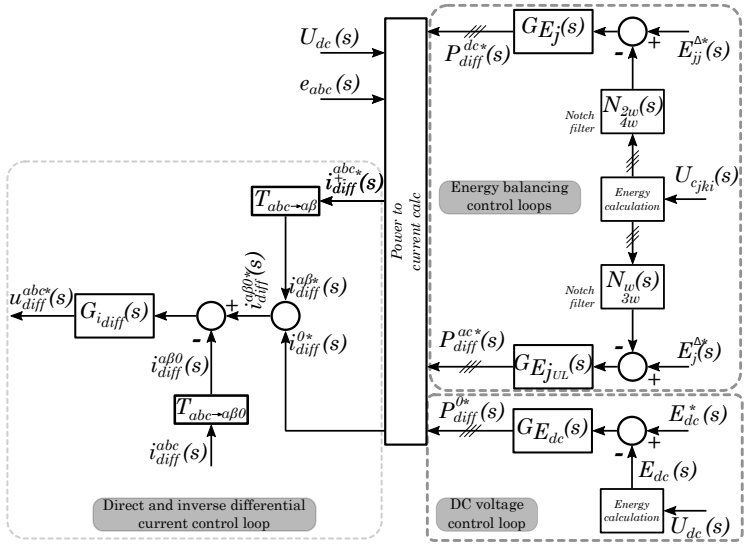


Figure 14: Energy balancing and differential current flow control loops.

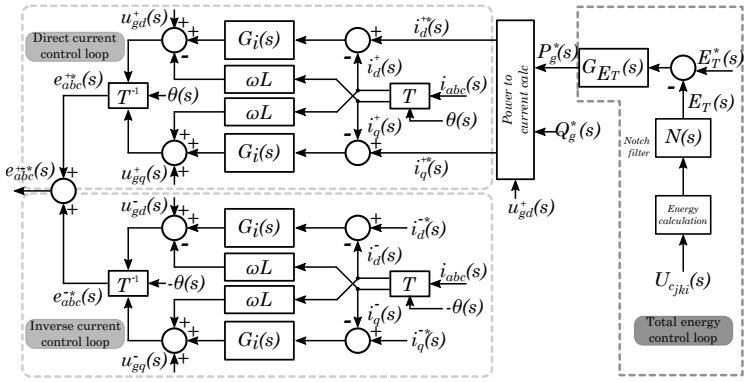


Figure 15: Total energy storage and interaction with ac network control loops.

these set-points, the required power values for the ac and dc power components that should internally flow in the converter legs are computed in stage (2), respectively modeled as $P_{diff_j}^{AC*}$ and $P_{diff_j}^{DC*}$ [78, 79]. In addition, in order to locally manage the pole-to-pole voltage across the dc terminals, the stage (3) imposes the homopolar power component that gets into the converter from its dc side. Once the power targets are defined, they are translated to inner current targets on the stage (4), which are managed in (5) by means of the inner voltage drop u_{diff_j}. The MMC energy balancing control loops are detailed in Figure 14. The control loops of the energy storage deviation between legs adjusts the dc power flow component between the converter phase units $P_{diff_j}^{DC*}$ to achieve a symmetric energy distribution between them $(E_{jU} + E_{jL}) = (1/3)E_T$. Furthermore, a sinusoidal current component with frequency ω is imposed to flow between the converter phase units to transmit the $P_{diff_j}^{ac*}$ power between the upper and lower stacks to harmonize their energy storage $(E_{jU} = E_{jL})$ [78, 79]. In addition, the homopolar component of the power flow on the converter legs $P_{diff_j}^{0*}$ is used to manage the pole-to-pole dc voltage. Finally, the unbalanced differential current targets $i_{diff_j}^{*}$ are managed in the $\alpha\beta 0$ domain by controlling u_{diff_j}.

In terms of interactions with the ac grid, the stage (6) manages the active power injection target into the grid to address the total energy storage set-point E_T^*. In accordance with the active P_g^* and reactive Q_g^* power flow targets, the block (7) sets the target values for the electrical current injection into the network. The grid side current control block (8) is responsible to manage magnitude and phase angle of the *emf* generated by the converter e_j^{+-} to inject balanced electrical currents into the ac grid. The total energy storage and interaction with ac network control loops are detailed in Figure 15. The total energy storage of the MMC and reactive power targets are managed by means of a balanced and direct current sequence control scheme i_{dq}^{+}. The inverse current sequence target i_{dq}^{-*} is set to zero to result a balanced grid current flow between the MMC and ac network.

Depending on the output values of the converter control, particularly the inner voltage drop $u_{diff_j}^{*}$ (see Figure 14) and the converter *emf* e_j^* (see Figure 15), the target values for the voltages across the arms u_{jk}^* are defined as (14). Moreover, these arm voltage targets are used to feed the modulation stage 1 (see Figure 2).

$$\begin{cases} u_{jU}^*(t) = \dfrac{U_{DC}(t)}{2} - \dfrac{u_{diff_j}^*(t)}{2} - e_j^*(t) \\ u_{jL}^*(t) = \dfrac{U_{DC}(t)}{2} - \dfrac{u_{diff_j}^*(t)}{2} + e_j^*(t) \end{cases} \tag{14}$$

3.2 Converter modeling and semiconductor losses estimation

Several MMC models with different levels of detail have been presented in the literature. In order to study the modular multilevel converter efficiency, the DEM was implemented but characterized by ideal switches (zero or $\infty\ \Omega$). Then, the semiconductor's power losses were estimated according to methodology presented in [81]. As the author described, to estimate the power losses

generated by the switches, besides the knowledge of its features (voltage drop and energy loss vs. driven current), the operating characteristics should be recorded during the on-state mode (guided current) and during the switching events (SM capacitor voltage and guided current). Hence, it was necessary to record the referred electrical signals for the 6N submodules, and, in addition, the firing pulses S_{jki} were also recorded to acknowledge the states of each particular switch.

In accordance with the operating conditions presented in the Table 1, the nominal voltage of the capacitors and the electrical current flow on the stacks of the converter, the ABB device 5SNA 1500E250300 seems to be a possible option [82]. The details of this semiconductor device and the methodology followed to estimate the power losses produced in this application are further detailed in the next sections.

3.2.1 On-state losses

The conducting losses of the semiconductors are affected by several phenomenons such as: the device's junction temperature (T_j), the voltage drop at the devices terminals (IGBTs: $U_{CE_{sat}}$/ diodes U_F), the operating currents (IGBTs: i_{CE} / diodes i_F) and, in case of IGBTs, the driver circuitry voltage (U_g). The average on-state losses of a single SM IGBT ($P_{T1}^{con}/P_{T2}^{con}$) and the diodes ($P_{D1}^{con}/P_{D2}^{con}$) over a grid period ($[t_s, T_s]$) are given by (15) and (16) respectively [81].

$$P_{T\lambda}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{CE}(t)\ U_{CE}^{[U_g,T_j]}\left(i_{CE}(t)\right) dt \tag{15}$$

where λ, in this context addresses the upper ($\lambda = 1$) or the lower upper ($\lambda = 2$) switch of the cell.

$$P_{D\lambda}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_F(t)\ U_F^{[T_j]}\left(i_F(t)\right) dt \tag{16}$$

Particularizing (15) and (16) to the specific IGBTs and diodes of the jki SM, as well as, the operating state S_{jki} of the SM[2], it respectively leads to:

$$P_{T\lambda_{jki}}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{jk}(t)\ U_{CE}^{[U_g,T_j]}\left(i_{jk}(t)\right) S_{T\lambda jki}(t) dt \tag{17}$$

$$P_{D\lambda_{jki}}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{jk}(t)\ U_F^{[T_j]}\left(i_{jk}(t)\right) S_{D\lambda jki}(t) dt \tag{18}$$

By applying the previous equations through all the γjki switches, the total on-state power dissipated on the semiconductors P_{cond} as:

$$P_{cond} = \sum_{\lambda jki} (P_{T_{\lambda jki}}^{con} + P_{D_{\lambda jki}}^{con}) \tag{19}$$

[2]From the SM state S_{jki} and the arm current direction, it is deduced whether the upper or lower switches, namely the diodes or the IGBTs, are the devices that are conducting. Then, a correlation between the SM state and the state of the correspondent semiconductor should be made $S_{T\lambda jki}/S_{D\lambda jki}$. The $S_{T\lambda jki} = 1/\ S_{T\lambda jki} = 0$ means that the IGBT $T\lambda$ is closed/open. The $S_{D\lambda jki} = 1/\ S_{D\lambda jki} = 0$ means that the diode $D\lambda$ is closed/open.

The oscillation of the junction temperature over the different operating conditions, as the voltage amplitude variation on the gating circuitry were not considered ($T_j \approx 125\ ^oC$/ U_g= 15 V). The non-linear relation between IGBT's saturation voltage and the diode's forward voltage with the corresponding flowing currents were fitted from the manufacturer component data (20), and they are illustrated in Figure 16.

$$U(i) = a + b\ i^c \Rightarrow \begin{cases} U_{CE_{sat}}(i_{CE}) = 0.654 + 0.007889(i_{CE})^{0.7483} \\ U_F(i_F) = 0.4715 + 0.03069(i_F)^{0.5314} \end{cases} (V) \tag{20}$$

3.2.2 Switching losses

The required time that a semiconductors need to commute has a nonlinear relation with the electrical current that is flowing on the correspondent instant. Therefore, due to the non-zero time interval of a switching event, some energy is dissipated. For the presented IGBT device, the switching energy loss was obtained from the component's data-sheet and described as a cubic relation in respect to the switched current as (21), and illustrated in Figure 17.

$$E(i) = a + b\ i + c\ i^2 + d\ i^3 \Rightarrow \begin{cases} E_{on}^{U_{CE}=1250V}(i_{CE}) = (4.988\text{e-}11)i_{CE}^3 \\ \qquad\qquad + (3.697\text{e-}8)i_{CE}^2 \\ \qquad\qquad + (7.264\text{e-}4)i_{CE} \\ \qquad\qquad + 0.0868 \\ E_{off}^{U_{CE}=1250V}(i_{CE}) = (1.371\text{e-}10)i_{CE}^3 \\ \qquad\qquad - (6.740\text{e-}7)i_{CE}^2 \\ \qquad\qquad + (2.038\text{e-}3)i_{CE} \\ \qquad\qquad + 0.21 \\ E_{rec}^{U_F=1250V}(i_F) = (5.29\text{e-}11)i_F^3 \\ \qquad\qquad - (4.016\text{e-}7)i_F^2 \\ \qquad\qquad + (1.109\text{e-}3)i_F \\ \qquad\qquad + 0.1229 \end{cases} \tag{21}$$

where (i_{CE}, i_F) pair is the collector-emitter current of the IGBT and diode at the moment of the commutation. ($E_{on}^{1250\text{V}}$, $E_{off}^{1250\text{V}}$) pair is the energy dissipated on the turn-on and turn-off event of a IGBT which has a capacitor with 1250V across its terminals. $E_{rec}^{1250\text{V}}$ is the energy dissipated on a turn-off event of a diode which has 1250 V across its terminals.

Afterwards, the energy estimation loss (21) was linearly adjusted to the switched voltage value

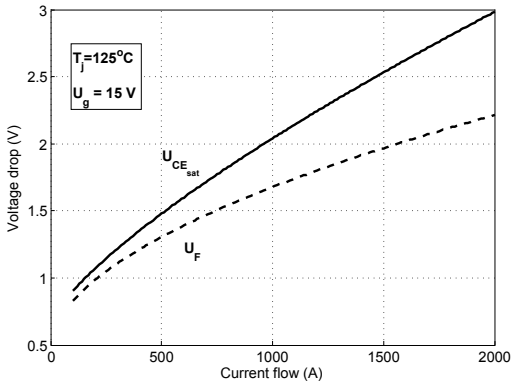


Figure 16: Estimated V-I characteristics of the embraced semiconductor.

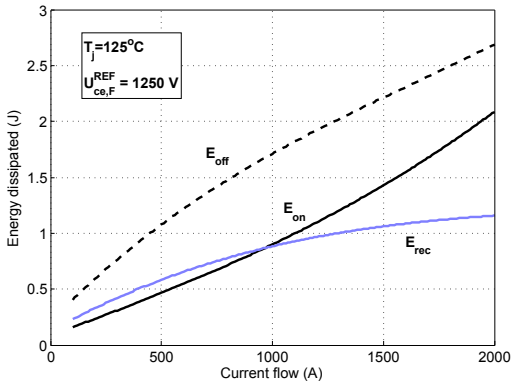


Figure 17: Estimated energy lost characteristics of the semiconductor.

present at the device's terminals during the switching event as (22) [81].

$$\begin{aligned} P_{on_{T\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\beta} \left(\frac{U_{c_{jki}}(t_\beta)}{U_{CE}^{REF}} \right) E_{on_T}^{[T_j]} \left(i_{jk}(t_\beta) \right) \\ P_{off_{T\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\gamma} \left(\frac{U_{c_{jki}}(t_\gamma)}{U_{CE}^{REF}} \right) E_{off_T}^{[T_j]} \left(i_{jk}(t_\gamma) \right) \\ P_{rec_{D\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\kappa} \left(\frac{U_{c_{jki}}(t_\kappa)}{U_{F}^{REF}} \right) E_{rec_D}^{[T_j]} \left(i_{jk}(t_\kappa) \right) \end{aligned} \tag{22}$$

where the $i_{CE}(t_\beta)/\ i_{CE}(t_\gamma)$ are the switched currents and $U_{CE}(t_\beta)/\ U_{CE}(t_\gamma)$ are the voltages at the IGBT terminals at the $\beta/\ \gamma$ triggering/ blocking events.

By applying the previous equations through all the jki switches, the total power dissipated on the commutation of the semiconductors P_{sw} is given by:

$$P_{sw} = \sum_{jki} (P_{onT_{jki}} + P_{offT_{jki}} + P_{recD_{jki}}) \tag{23}$$

3.3 Carriers frequency in the CB-PWM methods

In order to achieve a fair comparison between all the modulation strategies presented, a set of operating conditions was considered on the frequency design of the carriers used.

As mentioned, each particular carrier-based method introduces a significant harmonic content centered on a specific harmonic frequency of the MMC's line-neutral voltages spectrum. This frequency is designated in this work as the carrier central frequency f_{cc}. The intrinsic nature of the carrier's disposition endorses a particular harmonic spectrum of the arm voltages. Then, in order to achieve a fair harmonic distortion comparison between all the modulation techniques, the central frequency should be the same for all the CB-PWM methods.

To reach an equivalent total harmonic distortion over the three *emf* voltages of the converter, the central frequency of the carriers should be equal to an odd multiple of three of the fundamental grid frequency (24) [32].

$$f_{cc} = 3(2n-1)f_{grid} \qquad n=1,2\ ...\infty \tag{24}$$

Table 2: Selected values for the carriers frequencies.

CB-PWM method		f_{cc} [Hz]		
		150	450	750
APOD, POD, PD, CO CO-PD, CO-POD, CO-APOD	f_{c1}	150	450	750
VF	f_{c1}/f_{c2}	150/ $3f_{c1}$	450/ $3f_{c1}$	750/ $3f_{c1}$
PSC	f_{c1}	$\frac{150}{N}$	$\frac{450}{N}$	$\frac{750}{N}$
PSD	f_{c1}	$2\frac{150}{N}$	$2\frac{450}{N}$	$2\frac{750}{N}$

In accordance with what has been mentioned, the central frequencies selected for the carriers were the lowest three-values of n in (24), namely 150 Hz, 450 Hz and 750 Hz. The individual frequency of each particular CB-PWM carrier is shown in the Table 2.

In the LS-PWM techniques, the frequency of the individual carriers is equal to the central frequency, because those techniques add significant harmonic content in the arm voltages, particularly around the carrier's frequency. On the VF technique, the carrier levels that cross the top and bottom part of the arm voltage targets have three times the frequency of the inner layers due to symmetry issues over the three-phase system, as has already been pointed out. Finally, as the phase-shift-based strategies add their harmonic content as a dependence on the number of cells and the individual carrier's frequency, the last factor was designed in such a way that the harmonic content injected in the converter arm voltages would be centered around the LS-PWM techniques.

If the carriers are designed in accordance with the Table 2, in terms of the APOD, PSC and PSD techniques, they will look as depicted in Figure 18. The figure illustrates an example of the disposition of the APOD, PSC and PSD carriers for a 8-cell-based MMC. Focusing on the disposition of the APOD carriers, their frequency is 9 times higher than the voltage reference (450 Hz for T= 20 ms). On the other hand, if the PSC and PSD carrier methods were designed in accordance with Table 2 (N=8 and f_{cc}= 450 Hz), f_{c1} would be 56.25 Hz and 112.5 Hz respectively, as depicted in Figure 18(b) and Figure 18(c). Thus, if the resultant disposition of the carriers for the APOD, PSC and PSD methods are investigated, the arm voltage targets will cross a particular carrier precisely at the same instant across the APOD, PSC and PSD methods. As a result, the set-points for the number of inserted capacitors N_{jk}^{*} retrieved by the APOD, PSC and PSD methods will be the same. Therefore, the results obtained for the APOD, PSC and PSD techniques match together.

4 Impact of the modulation techniques on the MMC-MVDC performance

The CB-PWM and NLM methods in conjunction with each particular ZSS strategy were used to modulate the arm voltages of the MMC in the Matlab/ Simulink environment. Then, the

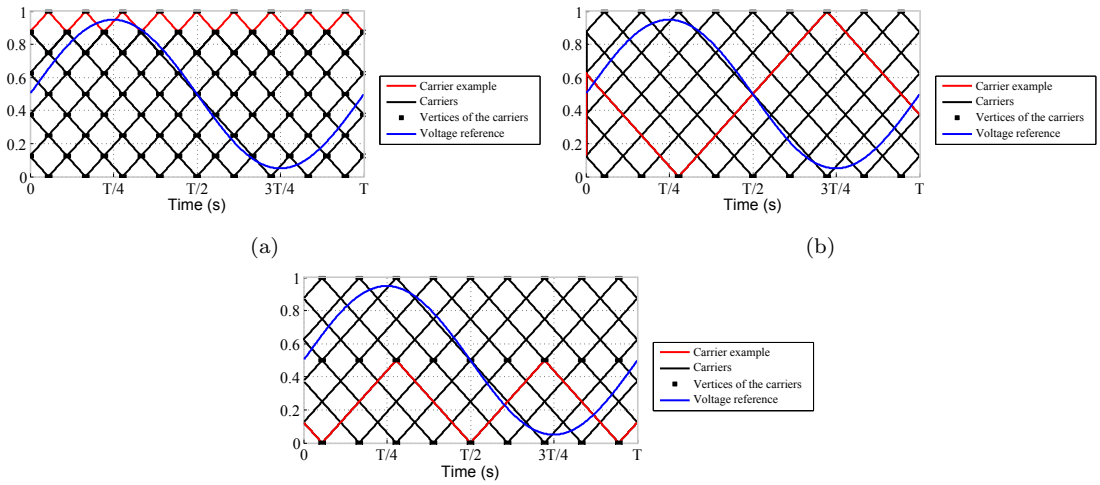


Figure 18: Similarity between the disposition of the carriers for the: (a) APOD,(b) PSC and (c) PSD methods.

steady-state performance of the presented methods were assessed. The total harmonic distortion generated by each modulation technique is presented in the subsection 4.1. On the other hand, the generated losses by the converter are shown in the subsection 4.2. Finally, the voltage ripple of the capacitors is shown in Section 4.3.

4.1 Power quality

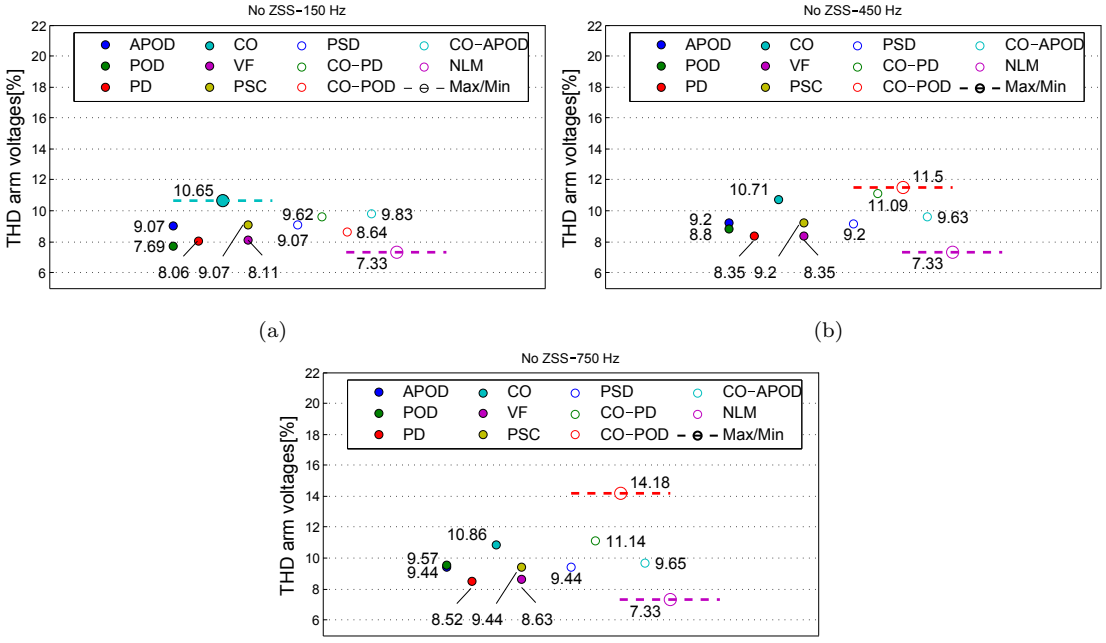
To inspect the impact of the CB-based techniques on the THD generated on the arm voltages, they were first implemented with the central frequency of 150 Hz, 450 Hz and 750 Hz without the presence of the ZSS. Moreover, the non-carrier-based NLM technique was also implemented to compare its impact on the MMC arms voltage THD. The results are summarized in Table 3. Focusing at the non-ZSS injection into the arms modulation results, which are emphasized in gray in Table 3 and illustrated in Figure 19, besides the THD factor being kept equal for the three f_{cc} scenarios, since it is not a frequency dependent technique, the arm voltages THD are also minimized. In terms of the CB-based techniques, as the central frequency is increased, the THD factor of the arm voltages becomes higher. Particularly, the CO-POD is the technique that is most affected with the increase of f_{cc}, its THD is 8.6 %, 11.5 % and 14.2 % for the f_{cc} respectively equal to 150 Hz, 450 Hz and 750 Hz. This occurs because the harmonics generated around the central frequency become more dominant as the frequency of the carriers are incremented, as Figure 20 suggests.

Table 3: Modulation methods impact on the MMC's arms voltage THD.

	No ZSS			THI 1/6			THI 1/4			SFO			D-ZSS		
Methods	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
APOD	9.03	9.20	9.46	20.30	20.31	20.25	28.24	28.35	28.41	24.10	24.06	24.20	55.70	55.87	55.96
POD	7.69	8.80	9.57	19.63	19.96	20.16	27.83	28.25	28.30	23.57	23.87	24.32	55.37	55.80	55.60
PD	8.06	8.35	8.52	21.73	19.54	19.60	30.25	27.53	27.96	25.61	23.43	23.74	55.69	55.34	56.16
CO	10.65	10.71	10.86	24.25	20.76	20.85	32.83	28.95	28.86	28.46	24.17	24.70	56.05	55.27	57.05
VF	8.10	8.35	8.63	21.3	19.54	19.86	30.28	27.53	28.38	25.79	23.43	24.02	55.75	55.34	56.29
PSC	9.03	9.20	9.46	20.30	20.31	20.25	28.24	28.35	28.41	24.10	24.06	24.20	55.70	55.87	55.96
PSD	9.03	9.20	9.46	20.30	20.31	20.25	28.24	28.35	28.41	24.10	24.06	24.20	55.70	55.87	55.96
CO-PD	9.62	11.09	11.14	23.77	20.15	20.49	32.78	28.94	28.93	28.24	23.84	24.63	56.17	55.39	57.2
CO-POD	8.64	11.50	14.18	19.28	20.71	22.32	28.02	29.11	30.39	23.67	24.83	26.26	55.60	56.08	56.51
CO-APOD	9.83	9.63	9.65	19.73	19.77	19.67	28.53	28.53	28.43	23.86	23.90	24.12	55.79	55.92	55.96
NLM		7.33			19.49			27.82			23.53			55.29	

*A,B,C are the f_{cc} values correspondent to 150 Hz, 450 Hz and 750 Hz respectively.

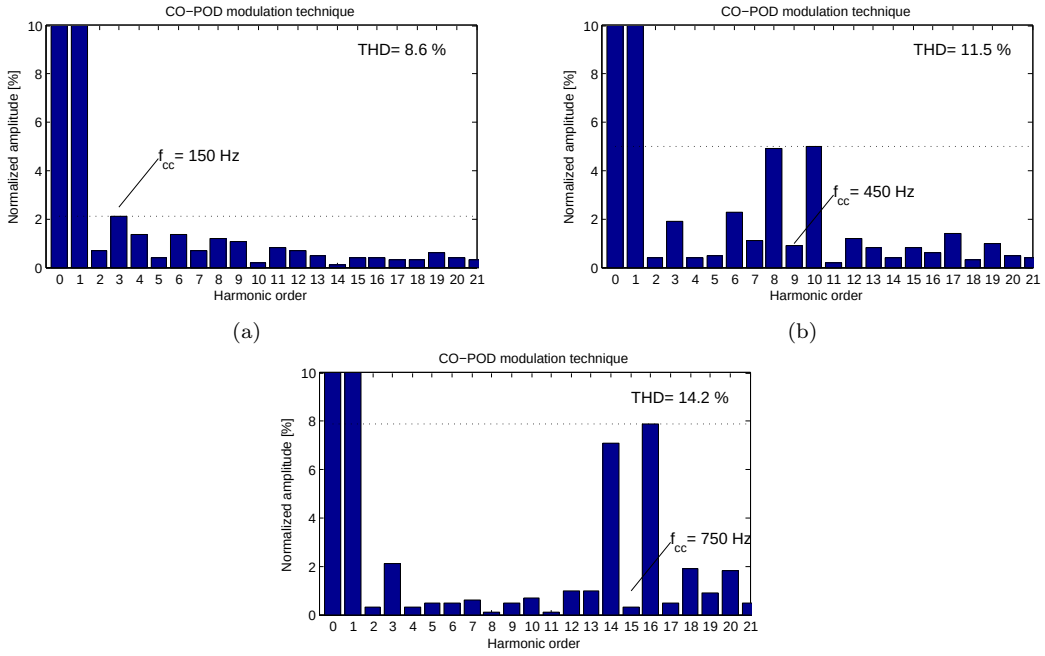
**The THD values are given in [%].



(a) (b)

(c)

Figure 19: Impact of the modulation techniques on the arms voltages THD: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

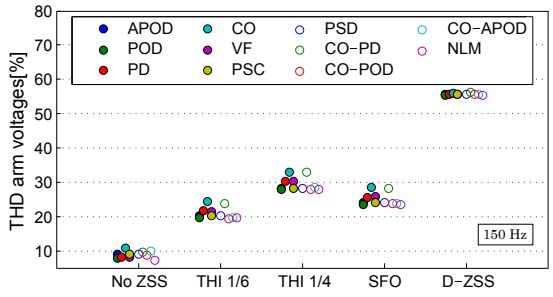


(a) (b)

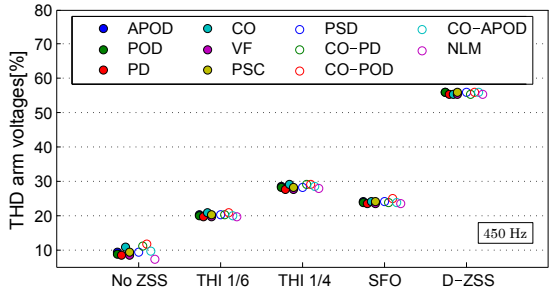
(c)

Figure 20: Impact of the carrier's frequency on the arm's voltage spectrum: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

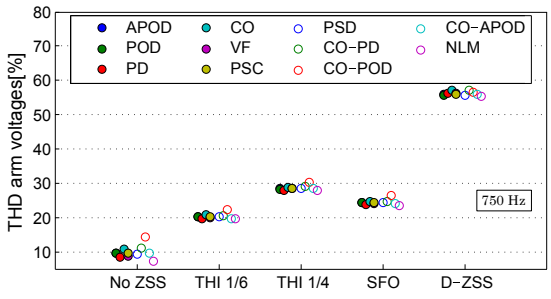
On the other hand, in case of zero sequence signals injection being considered on the MMC arm's voltage modulation, more harmonic frequencies are included, magnifying the arm voltages THD factors, as depicted in Figure 21 and detailed in Table 3. In the no-ZSS-based scenario, the arm voltages present less harmonic content and, logically, the lowest THD factor is retrieved regardless of the frequency considered for the modulation techniques. By including a third harmonic with (1/6) of the *emf*'s magnitude of the converter into its modulation, the second-lowest THD-based cluster solution is achieved. In contrast, if it included a third-harmonic with (1/4) of the converter's magnitude, it originates higher THD factors than for the (1/6) condition and slightly higher than the THD factors retrieved by the SFO. As the discontinuous-ZSS is composed of several third-order-based harmonics, it severely impacts on the arm voltages THD factors.



(a)



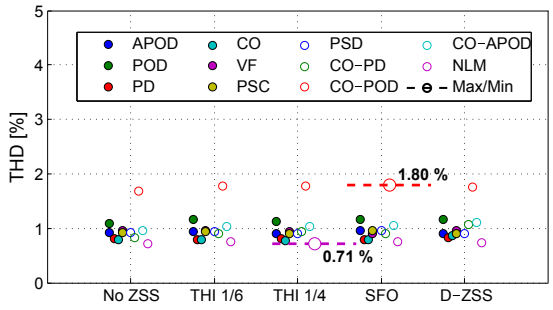
(b)



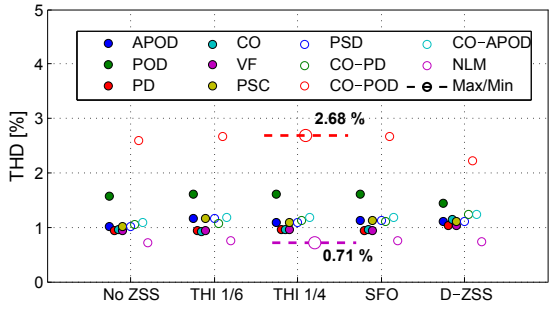
(c)

Figure 21: Impact of the ZSS on the arm's voltage THD: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

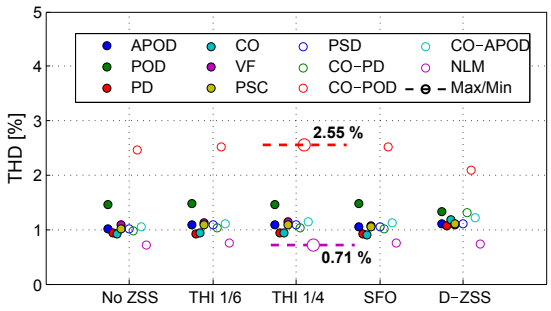
Regarding the harmonic contento of the grid currents, the results retrieved by the combination of the modulation techniques studied are displayed in Figure 22 and detailed in Table 4. It should be reinforced that the MMC operation is characterized by a notably low harmonic distortion of its grid currents, which is an accurate indicator of the power quality of its waveforms. The presented



(a)



(b)



(c)

Figure 22: Modulation methods impact on the total harmonic distortion of the MMC's line currents for: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

Table 4: Modulation methods impact on the MMC's line currents THD.

	No ZSS			THI 1/6			THI 1/4			SFO			D-ZSS		
Methods	A	B	C	A	B	C	A	B	C	A	B	C	A	B	C
APOD	0.92	1.01	1.01	0.94	1.17	1.09	0.91	1.08	1.08	0.96	1.13	1.06	0.9	1.10	1.10
POD	1.09	1.56	1.47	1.16	1.62	1.48	1.13	1.61	1.46	1.17	1.60	1.47	1.17	1.44	1.33
PD	0.80	0.94	0.94	0.79	0.94	0.93	0.82	0.97	0.94	0.78	0.94	0.93	0.83	1.02	1.07
CO	0.79	0.96	0.92	0.79	0.92	0.93	0.78	0.95	0.93	0.79	0.95	0.91	0.86	1.15	1.18
VF	0.96	0.94	1.09	0.96	0.94	1.12	0.94	0.97	1.14	0.90	0.94	1.07	0.95	1.02	1.09
PSC	0.92	1.01	1.01	0.94	1.17	1.09	0.91	1.08	1.08	0.96	1.13	1.06	0.9	1.10	1.10
PSD	0.92	1.01	1.01	0.94	1.17	1.09	0.91	1.08	1.08	0.96	1.13	1.06	0.9	1.10	1.10
CO-PD	0.83	1.05	0.97	0.9	1.08	1.04	0.95	1.12	1.04	0.90	1.11	1.02	1.07	1.24	1.32
CO-POD	1.68	2.59	2.47	1.78	2.67	2.52	1.78	2.68	2.55	1.80	2.67	2.52	1.76	2.22	2.09
CO-APOD	0.97	1.08	1.05	1.03	1.18	1.12	1.04	1.17	1.15	1.04	1.18	1.12	1.10	1.24	1.22
NLM	0.72			0.75			0.71			0.75			0.74		

*A,B,C are the f_{cc} values correspondent to 150 Hz, 450 Hz and 750 Hz respectively.

**The THD values are given in [%].

arm voltage modulations retrieve the remarkable values for THD between 0.71 % and 2.55 %. The POD and CO-POD techniques are the solutions that more harmonics inject into the grid currents (regardless the carrier's frequency and ZSS scenario). In opposition, the NLM is the technique that most reduces the ac currents THD. Furthermore, the remaining strategies retrieve alike results in terms of the current THD. In terms of the zero sequence signals, their impact on the grid-line currents' THD is also indistinguishable, as they got canceled at the line-to-line voltage converter's

output. The central frequency examined of 150 Hz marginally reduces the THD factors of the ac grid currents in comparison with higher f_{cc} scenarios and specifically to CB-PWM techniques.

4.2 Converter efficiency

This section presents the average power losses produced by the MMC semiconductors. Once the results were extracted from the Matlab/ Simulink model, the methodology presented in Section 3.2 was followed to estimate the power losses. As mentioned, the power losses were categorized as conducting P_{cond}, for the intervals that the semiconductors were closed and hence guiding the arm currents, or as switching losses P_{sw}, for the events that the semiconductors changed their state. For each combination between the modulation techniques, carrier's central frequency (if applied) and the ZSSs presented, the conducting and switching power losses generated were quantified, which are depicted in Figure 23 and Figure 24 respectively.

As the converter nature requires the arm current to be continuously flowing, there is always one semiconductor per submodule that is closed and carrying the arm current. Then, according to the converter model (Table 1), there are always 28 semiconductors (IGBTs and/ or diodes) conducting on the converter stacks. The fact that the converter is operating with the same power flow conditions in all the modulation techniques presented, the number of inserted capacitors in each leg is roughly equal. Thus, all the modulation techniques intrinsically enforce that the number and the nature of the closed switches are approximately the same. For this reason it is reinforced that regardless of the strategy adopted to modulate the arm voltages, the average conducting losses of the MMC are identical. Therefore, under those conditions, as the vertical bar graph of Figure 23 illustrates, the conducting power losses are approximately equal for the three f_{cc} scenarios studied, and their variance is practically nonexistent.

In terms of the semiconductor's power losses during the commutation events, as revealed in Figure 24, they are attached to the modulation strategy used. In the interest of the carrier's central frequency, as it increases, the target for inserting the number of cells N_{jk}^{*} is more often varied. Therefore, according to the classic cell selection method used, if N_{jk}^{*} has more pulses, the MMC cells are more often rotated. This issue directly increases the semiconductor's switching frequency and, as a result, they will dissipate more power. Moreover, the fact of increasing the f_{cc} factor, as the vertical bar graph of Figure 24 presents, the switching losses variance becomes more expanded.

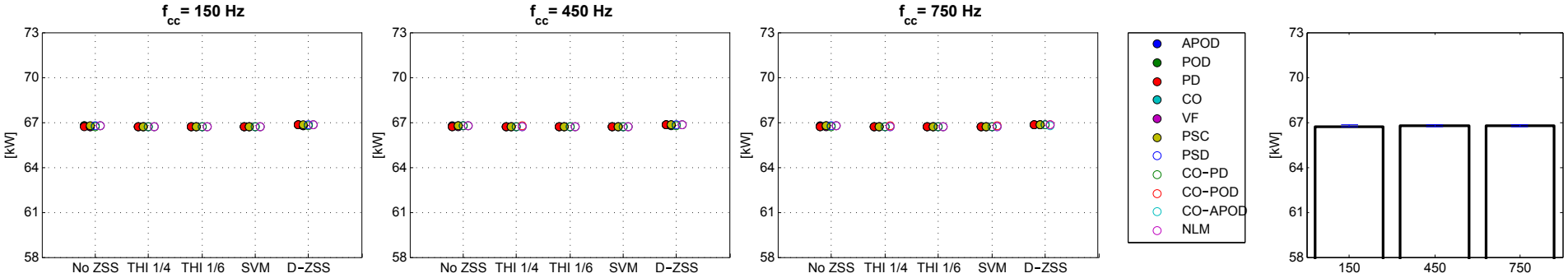


Figure 23: Summary of semiconductor's conducting losses retrieved by the presented modulation techniques.

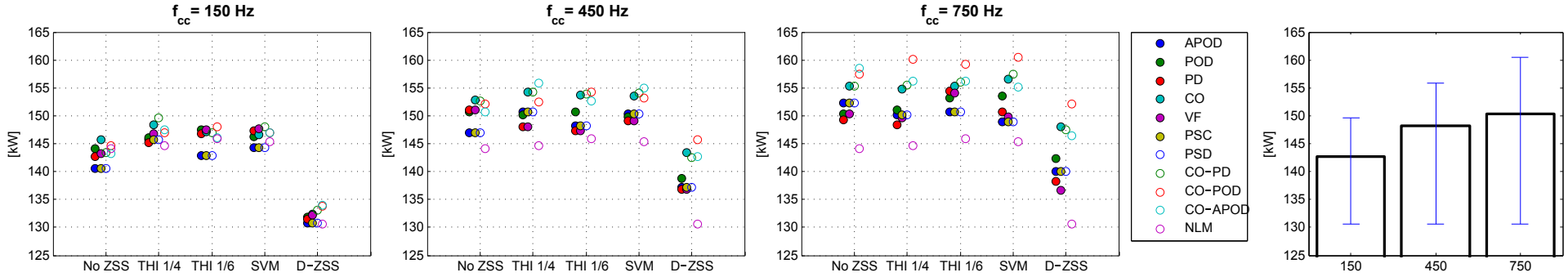


Figure 24: Summary of semiconductor's switching losses retrieved by the presented modulation techniques.

Another important aspect for this study is the performance of the discontinuous zero sequence signal that is injected into the arms voltage modulation. Independently of the methodology followed to synthesize the arm voltages, if a discontinuous zero sequence signal is used to bypass the capacitors on the most stressful intervals of the semiconductors, according to the selective control of the cells adopted, it certainly reduces the power losses (switching). For the modulation scenarios studied, the aggregation between the NLM modulation with the DZSS minimizes the switching power losses and the aggregation makes the usage of the CB-PWM techniques pointless from the converter efficiency perspective.

If the continuous-based ZSS are used instead, the converter performance should be evaluated individually to the modulation strategy considered. This happens because it is not a straightforward correlation between the continuous-based ZSS features with the disposition and frequency of the carriers. However, the APOD/ PSC/ PSD tend to be the CB-based techniques that most reduces the switching losses (f_{cc}=150 Hz). As the increase of the f_{cc} factor leads to a further increase of the power dissipation on the CB-based scenarios, on the f_{cc}= 450 Hz and f_{cc}= 750 Hz circumstances, all the CB techniques exceed the power dissipation retrieved by the NLM. In contrast, due to the nature of the carrier-overlapping-based techniques, for the same f_{cc} factor as the other CB-PWM solutions, the modulation indexes m_{jk} intercepts the carriers more times, which imposes more pulses in N^*_{jk}. Therefore, the CO-based techniques tend to compute higher switching events and power losses as the central frequency factor is enlarged.

From an efficiency point of view, it is more advantageous to use either the APOD/ PSC/ PSD (f_{cc}=150 Hz without ZSS) or the NLM (with the DZSS) due to their reduced generation of the power losses. In fact, even for the DZSS injection scenario, both solutions are very close. Hence, the decision to move forward to either solutions may depend on the intrinsic hardware implementation difficulty that each one requires. Finally, the total power losses produced can vary from 167 kW/≈1.1% (67 kW + 130 kW) to 207 kW/≈1.4% (67 kW + 140 kW), depending if the NLM with the DZSS is adopted or the referred CB-based techniques without the ZSS, respectively. Either ways, the power losses of the semiconductor's is roughly equal to 1 % of the MMC rated value, which corroborates the previous analysis done in the MMC's efficiency analysis [83, 84].

The power losses produced by the MMC is greatly dependent on the cell selection method adopted. Due to the high rotation of the cells imposed by the classic cell selection method embraced, the commutation losses can be further reduced by implementing another strategy. However, since the focus of this work is to analyze impact of the arm voltage modulation schemes on the converter performance, this fact is considered to be out of the scope.

4.3 Capacitor's voltage ripple

The combination between the modulation techniques with the ZSS incites further changes on the MMC performance, namely in the capacitor's voltage ripple. The mean voltage ripple is characterized by the range of $(U_{jk}^{\Sigma}/\mathrm{N})$ and was normalized in respect to the SPWM. The impact of the presented modulation strategies on the mean voltage ripple of the MMC's capacitors are shown in the Figures 25 and 26 respectively.

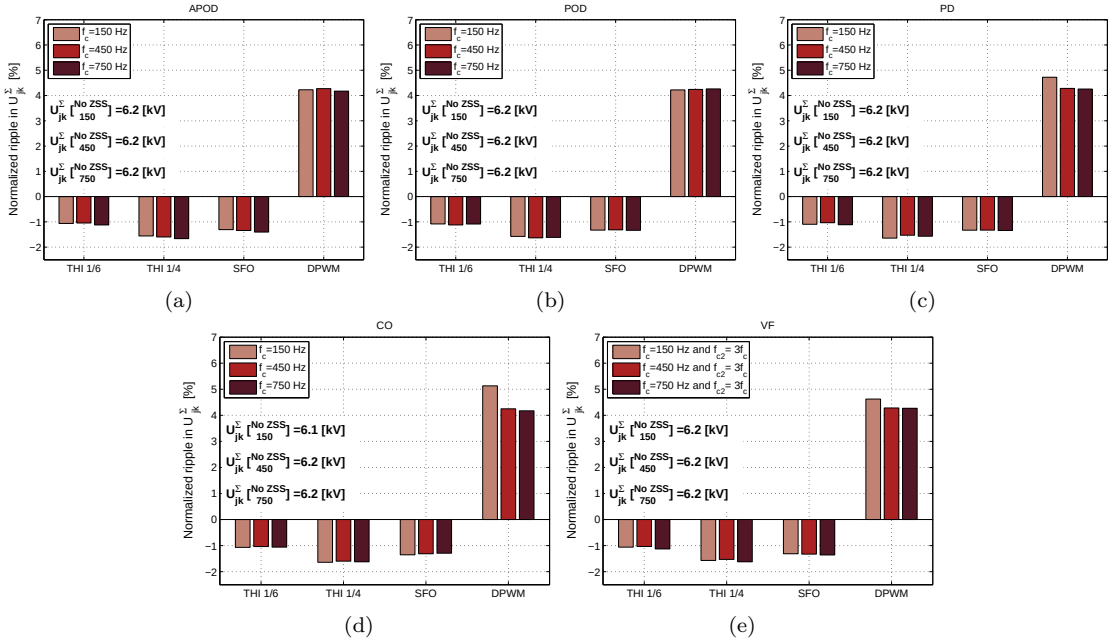


Figure 25: Impact of the LS modulation strategies on the capacitor's voltage ripple: (a) APOD/ PSC/PSD, (b) POD, (c) PD, (d) CO and (e) VF.

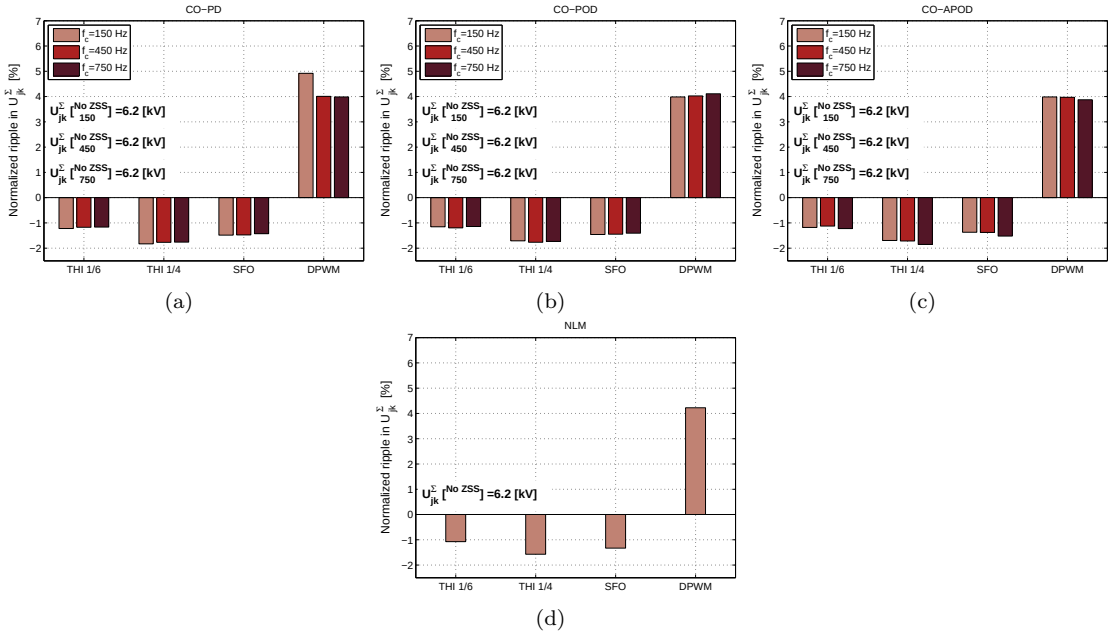


Figure 26: Impact of the CO-hybrid and NLM modulation strategies on the capacitor's voltage ripple: (a) CO-PD, (b) CO-POD, (c) CO-APOD, (d) NLM.

Again, the nature of the ZSS entails relevant consequences for converter performance. Regardless of the modulation itself, if the THI (1/4) is injected on the MMC arms voltage modulation,

the capacitor's ripple is minimized among the selected ZSSs analyzed. This occurs because the *emf* voltage component of the arms is practically aligned with the line currents. Then, as the THI (1/4) is the technique that most reduces the amplitude of the arm voltages when the current reaches its peak, it intrinsically reduces the voltage amplitude across the converter stacks. This fact leads to a reduction of the number of capacitors that are inserted during the peak current instant, which contributes to the minimization of the capacitor's voltage ripple.

On the other hand, as the DZSS forces the capacitors to go longer without being rotated in comparison with the other ZSS techniques. Under these circumstances, the voltage ripple across the capacitors is increased to higher values than the ones obtained without the presence of any ZSS.

The most evident fact is that the inclusion of the third harmonic or the SFO into the voltage modulation, it has an higher impact on the capacitors mean voltage ripple than the predisposition of the carriers and their central frequency f_{cc}. For those ZSS techniques, the impact of the disposition of the carriers on the capacitor's voltage ripple is below 0.3 %, which corroborates their light impact on this factor.

The fact of the carrier-overlapping-based techniques inflicting more pulses on N_{jk}^{*} than the other CB techniques, inherently contributes to a higher rotation of the converter capacitors. Thus, the CO-based schemes contributes to the capacitor's average voltage ripple reduction. Finally, the minimum voltage ripples achieved for the converter capacitors were:

- -1.83 %: for CO-PD with THI 1/4 f_{cc}= 150 Hz;
- -1.77 %: for CO-PD with THI 1/4 for f_{cc}= 450 Hz;
- -1.85 %: for CO-APOD with THI 1/4 for f_{cc}= 750 Hz;

For the reasons already pointed out, the aggregation between the CO-based techniques and the injection of the third harmonic (THI 1/4) component into the arms voltage modulation leads to the minimization of the capacitors' voltage ripple.

5 Conclusions

The modular multilevel converter (MMC) has very interesting features and it is being pointed as one possible key-point breakthrough in dc power transmission field. The importance of improving converter performance plays a tremendous role on its efficiency, reliability and economic benefits. A transversal research topic to these aspects is the voltage modulation employed at this converter scheme. This paper has provided a comparative review of multilevel modulation techniques and their impact on the converter harmonic pollution, efficiency and voltage ripple synthesized across its capacitors.

Once the target values for the MMC arms are determined by proper control algorithms, their voltage modulation is divided into three distinct stages. At the first stage, literature zero-sequence signals (ZSS) may be added to the voltage targets and are consequently normalized in respect to the maximum voltage vector achievable across the correspondent arms. On the following stage, different multilevel strategies that have been introduced in the literature for modulating the several power converter structures and ergo reviewed in this paper, are used to modulate the required voltage target values. Finally, the third and last stage deals with a selective control of the cells to assure a symmetrical energy distribution between the capacitors assembled in the same stack.

The comparative study shows that the alliance between the intrinsic nature of the ZSS considered (stage 1) and the voltage modulation method followed (stage 2) can be embraced to improve the MMC performance in terms of power quality, higher efficiency or the reduction of the capacitor's voltage ripple. By including ZSS into the sinusoidal arm voltage targets, besides increasing their harmonic pollution from roughly 15% to 57%, different performance factors are affected.

In respect to the carrier-based multilevel methodologies studied, due to the relatively high number of submodules available on the converter model, in accordance with their displacement and for the frequency values analyzed, their characteristics led to the diminished harmonic distortion factors of the line currents between 0.78% to 2.55%. These exceptional values were only surpassed by the nearest level modulation method which computed the lowermost harmonic distortion factor of 0.71%.

Focusing on the multilevel modulation impact on the converter efficiency, it is demonstrated that for the same operating conditions, they do not affect the on-state losses of the semiconductors, but on the power losses generated during the switching events. Depending the modulation strategy adopted the semiconductors power losses vary from 1.1% to 1.4%. The combination between the alternate phase opposition disposition (APOD) or the nearest level modulation strategies with the discontinuous-based ZSS are the solutions that most reduces the semiconductor's power losses for the conditions studied. Moreover, in case of the arm voltages being modulated by carrier-overlapping-based techniques, a higher rotation of the capacitors is imposed which reduces their voltage ripple. Additionally, the lowermost voltage ripple achieved occurred with the presence of the ZSS with the third harmonic 1/4 nature on the arm voltage modulation.

Finally, by inspecting the different arm voltage modulation scenarios studied, it is concluded that the selection of the modulation strategy embraced greatly depends on the factor that needing further optimization. Generally, the nearest level modulation is responsible for generating low harmonic content on the grid currents as well as, it generates less power losses. On the other hand, regarding the ZSS, the third harmonic with (1/4) reduces the voltage ripple of the capacitors, the third harmonic with (1/6) conjointly with the SFO maximizes the linear range of the modulation and, finally, the discontinuous-ZSS reduces the switching events and the corresponding losses of the semiconductors.

Acknowledgments

The author Abel A. Ferreira gratefully acknowledge for the financial support from the People Programme (Marie Curie Actions) of the European Unions Seventh Framework Programme FP7/2007-2013/ (grant agreement no. 317221), project title MEDOW.

The author Oriol Gomis-Bellmunt would like to express his gratitude to the Spanish Ministry of Economy and Competitiveness under the project ENE2015-67048-C4-1-R and the European Regional Development Fund (ERDF) for financial support.

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