Background Digital Calibration of Comparator Offsets in Pipeline ADCs

A. J. Ginés, E. J. Peralías, A. Rueda

***Abstract*— This paper presents a low-cost digital technique for background calibration of comparator offsets in Pipeline ADCs. Thanks to calibration, comparator offset errors above half the stage least-significant bit (LSB) margin in a unitary redundancy scheme are admissible, thus relaxing comparator design requirements and allowing their optimization for low-power high-speed applications and low input capacitance. The technique also makes it possible to relax design requirements of stage amplifiers within the Pipeline queue, since output swing and driving capability are significantly lower. In this brief, the proposal is validated using realistic hardware-behavioral models.**

***Index Terms*— Comparator Offset, Digital Blind Estimation, Background Calibration, Flash and Pipeline ADCs.**

I. Introduction

The Flash subADC inside each Pipeline ADC stage provides a coarse estimation of the stage analog input and resolves part of the final resolution in the complete Pipeline queue. In a design with unitary redundancy [1], the maximum offset in subADC comparators is limited to half the stage LSB (least-significant bit). This accuracy requirement limits the resolution of Pipeline stages to 2-3 bits (and rarely, 4 bits) in most practical cases. The reasons for the reduced set of resolutions can be found [2] in: a) the existing trade-off between resolution and conversion-speed/power-consumption in comparators, b) the increment of stage op-amp driving requirements with accuracy due the subADC comparator capacitive load, and c) the direct relationship between comparator offset and stage op-amp output swing.

The trade-offs between speed and accuracy are clearly analyzed in stand-alone dynamic latches comparators (SA-DLC) with no preamplifier and no resistor ladder [3], since this topology provides the faster response and lower power consumption due to positive feedback at the expense of accuracy (this topology is high sensitive to environmental conditions and mismatches [4], displaying offset above 200mV). Actually, the huge variability of SA-DLCs limits their use to low-resolution stages, typically of 1.5 bits. Practical stage implementations with higher resolution consider comparator topologies based on a front-end preamplifier [5], they rely on relatively complex correction techniques in the analog domain [6] and/or they add extra clock phases [7]. In these solutions, the power optimization of the complete Pipeline ADC needs to consider significant constrains between accuracy, speed, and power consumption, affected also by the comparator selection. The stage amplifier requirements are highly dependent on comparator input capacitances and offsets. Actually, the smaller the comparator offset, the lower the output swing in stage amplifiers and the higher the comparator's parasitic input capacitances.

As an alternative to the traditional methods, we propose using calibration as an extra design variable for dealing with comparator offset in Pipeline ADCs, with the target of simplifying comparator design and relaxing the output swing and driving requirements of MDAC op-amps. The proposed method accurately estimates and corrects offsets with very fast convergence and low-cost digital resources. It can use existing ADC input as calibration stimulus, and it does not therefore affect to the input conversion (background mode). An additional and relevant advantage of the method is that it contributes to relax power consumption and input parasitic capacitances since smaller devices can be used.

The paper is organized as follows. Section II introduces the Pipeline ADC topology and looks at the effects of the comparator offsets on converter non-linear errors. Section III presents the proposed calibration method. Section IV shows the simulation results. Finally, conclusions are drawn in Section V.

II. Comparator Offset Effects in Pipeline ADCs

Fig. 1 shows a simplified block diagram of an (L-1)-stage Pipeline ADC, with a last quantizer (LQ). Each stage, STG_i with $i \in [\ 1,\ L\text{-}1\ ]$, comprises: a) a $subADC_i$ which performs a coarse quantization k_i of its analog input x_i with N_i-bit resolution; and b) an $MDAC_i$ which generates the amplified residue x_{i+1} to be processed by the following stages. In this topology, the roll of $C_{i,j}$ will become relevant for calibration purpose (see Sect. III). The digital representation X_1^H of the converter input $x \approx x_1$ is finally obtained, by the TAL (Time Alignment & Arithmetic Logic), as a simple binary weighted function of the synchronized codes $\{k_i\}$ with $i = 1, \ldots, L$.

The $subADC_i$ architecture is classically based on a Flash ADC made up of a bank of M comparators, a resistor ladder for the threshold voltage generation, called transition t_j, and a thermometer-to-binary encoder which codifies the analog input signal, $x \in [\text{-}R,R\ ]$, into the N-bit output code, $k \in [0,M\ ]$. The relationship between x, the set of transitions $\{t_j\}$, the output code k and the comparator offset are given by,

$$k = \text{subADC}(x) \quad \Leftrightarrow \quad x \in [\ t_k,\ t_{k+1}\ ) \tag{1}$$

$$off_j = t_j - t_j^* \quad , \quad j \in [\ 1,\ M\ ] \tag{2}$$

where sub-index j specifies a particular comparator within the i-th subADC and t_j* defines its ideal value.

In a Pipeline ADC with unitary redundancy [1], the accuracy resolution of the i-th subADC is theoretically bounded by the stage resolution, that is $|off_j| < Q/2 = R/2^N$, where N is the stage resolution and Q is the stage LSB. However, even when this condition is satisfied, the amount of offset has a non-negligible impact on the linearity of the amplified residue x_{i+1},

Manuscript received July 18, 2013. This work was supported in part by the Andalusian Government project P09-TIC-5386 and the Spanish Government project TEC2011-28302, both of them cofounded by the European FEDER program.

Authors are with the Instituto de Microelectrónica de Sevilla (IMSE-CNM-CSIC) and the Universidad de Sevilla, Edificio IMSE-CNM, Av. Americo Vespucio, s/n 41092, Sevilla, Spain (phone: +34 954 466 666 ; fax: +34 954 466 600; e-mails: {gines, peralias, rueda}@ imse-cnm.csic.es).

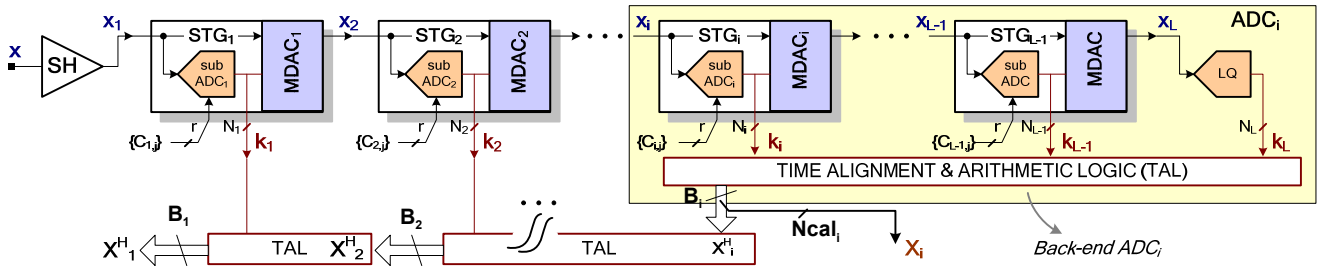

Fig. 1 Simplified block diagram of an L-stage Pipeline ADC with details of stage topology and time alignment and arithmetic logic (TAL).

since a large output swing (OS) in the MDAC is needed. Fig. 2 illustrates this effect in a 3-bit stage example with low and high comparator offsets. When the offset is high, the amplifier's non-linear region could affect residue generation. These limitations are usually addressed by: a) incrementing the accuracy of the comparator at the expense of higher power consumption and extra input capacitance, and/or b) increasing the output swing capability of the MDAC amplifier (op-amp), which also has a negative impact on power consumption. As an alternative, this work proposes the use of calibration as a mean of overcoming this power overhead. This is done in the digital domain.

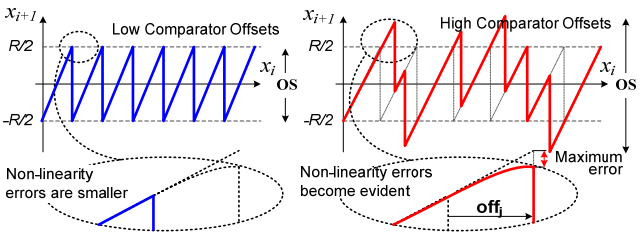

Fig. 2 Contribution of redundancy-compatible comparator offsets to stage non-linearity errors.

III. Proposed Background Calibration Technique

The adaptive calibration technique we propose performs two different tasks. First, it obtains a measurement of the comparator offset based on [8], thanks to the equivalence between (2) and the subADC *Integral Non-Linearity* (*INL*). This information is used in a second process to generate a set of calibration codes, the role of which is to act on the comparator's transitions for effective offset cancellation. Both processes are performed in the digital domain and we will see display fast robust convergence to the stationary situation. Fig. 3 shows the conceptual scheme of the proposed calibration techniques for the *i-th* subADC. The *Comparator Offset Calibration Logic* (*COCL*) comprises the *Offset Adaptive Estimation* (*OAE*) block and the *Calibration Code Generator* (*CCG*) block. Both logic units can work simultaneously.

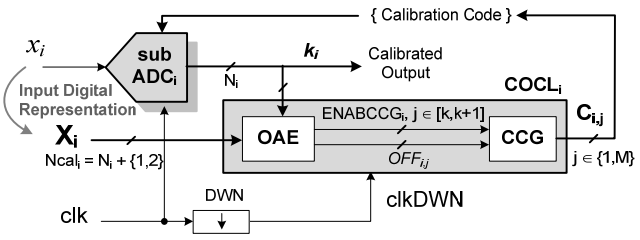

Fig. 3 Block diagram of the comparator offset calibration technique.

A. Offset Estimation

The task of the OAE block is to obtain a digital estimation $\{OFF_j\}$ of the comparator offset $\{off_j\}$ in (2) through an adaptive algorithm which forces implication (1) to be fulfilled in the digital domain. That is,

$$\text{if } \; k[n] = \text{subADC}(\, x[n]\,) \;\Rightarrow\; X[n] \in [\, T_k[n],\, T_{k+1}[n]\,) \qquad (3)$$

where n is an updating timing index, $T_k[n]$ is a digital code associated with the actual transition t_k, and $X[n]$ is a digital representation of the sampled analog input $x[n]$, both with resolution N_{cal} ($>N$). In other words, if $k[n]$ is the subADC output at time index n, the corresponding ADC input $x[n]$ must be located within the interval $[t_k,t_{k+1})$, and therefore, its digital counterpart should fulfill $X[n]\in[T_k[n],\ T_{k+1}[n])$. If this relationship is not satisfied, the OAE will change the transition estimations $\{T_k[n],\ T_{k+1}[n]\}$ until it is verified.

Taking into account these estimations, equation (2) can be evaluated in the digital domain as,

$$OFF_j = T_j - T_j^{*} \quad , \quad j \in [\,1,\, M\,] \qquad (4)$$

where T_k^{*} is a digital code associated with the ideal transition t_k^{*} of the subADC, and it is always known a priori. In a shifted binary code, it is given by $T_k^{*} = k\ 2^{(\text{Ncal-N})}$.

Combining (3) and (4) in a single expression to manifest the dependence on the offset estimation OFF_j, we finally arrive at the following updating criterion, where for the sake of simplicity the updating index n has been omitted,

$$\text{if } k = \text{subADC}(x) \;\Rightarrow\; X \in [\, T_k^{*} + OFF_k,\ T_{k+1}^{*} + OFF_{k+1}\,] \qquad (5)$$

The technique continuously verifies whether (5) is satisfied. When it is not, the offset estimation OFF_j is updated. A simple adaptive algorithm for this procedure is given by,

$$\begin{aligned} &\text{Being } k[n] \text{ the output code at the } n \text{ updating index,} \\ &\text{if } X[n] > OFF_{k+1}[n] + T_{k+1}^{*} \rightarrow \begin{cases} OFF_{k+1}[n+1] = OFF_{k+1}[n] + \mu \\ ENABCCG = 1 \;\text{ in }\; j = k+1 \end{cases} \\ &\text{if } X[n] < OFF_k[n] + T_k^{*} \;\;\rightarrow \begin{cases} OFF_k[n+1] = OFF_k[n] - \mu \\ ENABCCG = 1 \;\text{ in }\; j = k \end{cases} \\ &\text{otherwise, } OFF_k[n] \text{ does not change and ENABCCG = 0.} \end{aligned} \qquad (6)$$

where $\mu = 2^{-m}$ (with m integer) is the adaptive constant step in the example, ENABCCG is a control signal which enables (logical value '1') or disables (logical value '0') the next CCG

operation, and j is the updating pointer which determines the specific calibration code C_j that must be updated. If k reaches an extreme value, 0 or M, only one decision of (6) applies.

B. Input Digital Representation

With regard to the digital representation $X_i[n]$ of the analog input $x_i[n]$ for the different subADCs, it should be pointed out that due to the iterative structure of the Pipeline ADC, this information is already available in the output code, $X_i^H = \mathrm{ADC}_i(x_i)$ of the back-end stages from STG_i to LQ. These back-end stages form an analog-to-digital converter labeled ADC_i in Fig. 1. To reduce the calibration logic requirements, as well as, to improve immunity against comparator thermal noise and ADC_i second order effects (such as amplifier thermal noise, capacitor mismatch or amplifier finite gain), we consider a truncated version X_i of X_i^H,

$$X_i = \left\lfloor X_i^H / 2^{B_i - Ncal_i} \right\rfloor \quad ; \quad N_i < Ncal_i \le B_i \tag{7}$$

where B_i is the number of bits of the back-end ADC_i, and $Ncal_i$ is the resolution of X_i exceeding N_i.

C. Calibration Code Generation

The role of calibration codes $\{C_{i,j}\}$ is to control comparator transitions in such a way as to compensate for their offsets. Let us again implicitly assume the stage index "i" for the sake of clarity. Signal C_j then represents the code performing the t_j modification of the j-th comparator ($Comp_j$) within a specific subADC_i. If a sign (r+1)-bit binary encoding signal is selected for the calibration code C_j, the transition location t_j becomes,

$$t_j = t_j[0] - \delta \cdot C_j \quad ; \quad \delta = off_{\max} / 2^r \tag{8}$$

where $t_j[0]$ is the uncalibrated transition, off_{max} is the wanted maximum correctable offset, δ is the adaptation step and r defines the C_j resolution.

The task of calibration block *CCG* is to determine the value of C_j. The generation of C_j is performed straightforward in the digital domain using the offset estimation OFF_j derived in (6). Starting from an initial value of zero, C_j is modified to ensure that OFF_j remains low enough. The adaptation criterion maintains the offset error OFF_j within an interval of amplitude Δ,

$$|OFF_j| < \Delta \quad ; \quad \Delta = \left\lfloor \delta / Q_{cal} \right\rfloor = \left\lfloor \delta \ (2^{Ncal} / 2R) \right\rfloor \tag{9}$$

where $\lfloor \bullet \rfloor$ is the floor operator, Δ is the digital representation of the comparator step δ in (8) and Q_{cal} is the quantum associated to the input estimation $X[n]$, i.e. $Q_{cal} = 2R/2^{\mathrm{Ncal}}$.

The procedure is only enabled, ENABCCG = 1, when OFF_j is updated, with the index pointer $j \in \{k, k+1\}$ provided by the OAE in Fig. 3, according to subADC output k . In this case, if $OFF_j > \Delta$, the calibration code C_j is increased and the offset is consequently reduced in accordance with (8). If $OFF_j < -\Delta$, C_j is decreased and the offset is therefore again reduced. This procedure can be implemented by the following algorithm,

$$\begin{aligned} &\text{Being } j \text{ the transition pointer at time index } n, \\ &\text{if ENABCCG=1 \& } OFF_j[n] > \Delta \ \rightarrow C_j[n] = C_j[n-1] + 1 \\ &\text{if ENABCCG=1 \& } OFF_j[n] < -\Delta \rightarrow C_j[n] = C_j[n-1] - 1 \\ &\text{otherwise,} \quad C_j[n] \text{ does not change} \end{aligned} \tag{10}$$

where $|C_j| \le 2^r$ and r is the resolution. Obviously, amplitude Δ, or equivalently δ, establishes a boundary on the offset compensation performance. The smaller these values are, the greater the accuracy, but, according to (8), the higher the resolution r for a given maximum correctable offset off_{max}. In practical terms, r values in the order of 2-3 bits are enough to keep the residual post-calibrated offset well below half the LSB, at the same time reducing the calibrated comparator complexity.

Fig. 4b shows a simplified block diagram of the digital implementation of the calibration code generator (CCG) for the algorithm in (10). The CCG comprises a comparison block (C-CB), a single 1-bit input incrementer/decrementer (C-ADD) and a register bank (C-RB) for storing the C_j values. When the ENABCCG signal takes the logical value 1, the C-CB receives the offset code OFF_j according to the OAE updating pointer $j[n]$. Taking into account the relationship between $OFF_j[n]$ and Δ, the C-CB block defines the C-ADD enable (EN) and sign (Sgn) for $C_j[n\text{-}1]$ updating. The resulting code word $C_j[n]$ is stored in the C-RB using the same j[n] as the read/writer pointer. Note that C-RB is a low resolution bank of registers with M by (r+1) different memory locations.

D. Comparator Offset Compensation

The procedure for compensating the comparator offset by modifying the effective transition location t_j according to calibration code C_j depends on the specific comparator's topology. In the case of a CMOS SA-DL comparator, it can be practically introduced using two programmable banks which generate a differential imbalance in some of the SA-DL's

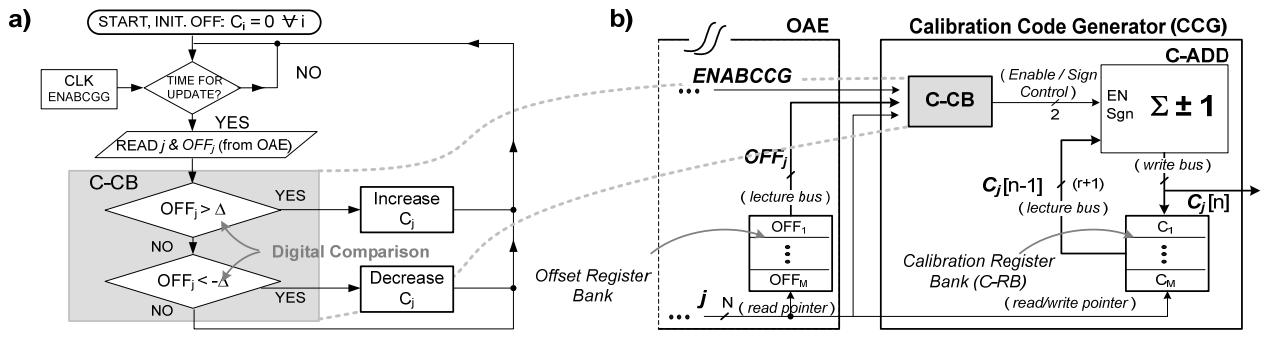

Fig. 4 a) Flow diagram of the CCG for comparator offset calibration in Flash ADCs; b) details of digital hardware resources using a single accumulator.

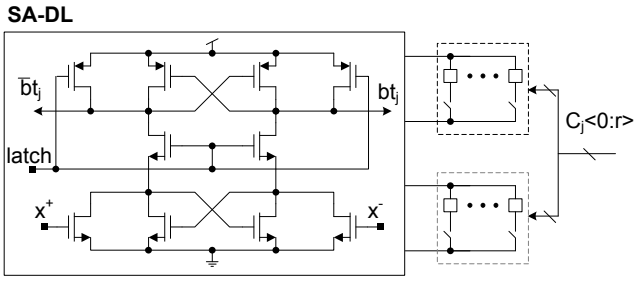

Fig. 5 Comparator block diagram with systematic programmable imbalance for offset compensation (conceptual implementation in a SA-DL).

internal nodes, as conceptually depicted in Fig. 5. Alternative actuations schemes, as one in [3], are also suitable.

IV. Simulation Results

To verify the proposed calibration, extensive behavioral and electrical simulations have been carried out. In this section, and due to space limitations, we will focus on the behavioral simulation results. As a case of study in MATLAB™, a 14-bit 100Msps Pipeline ADC with 1V reference is presented to clearly show the calibration advantages independently on the comparator architecture and target technology. The architecture was made up of two most significant stages of 3 bits followed by nine stages of 1.5 bits (including the LQ). In a first case of study, we focused exclusively on the comparator offset to isolate the impact of subADC errors inside each stage. Non-linear errors in these blocks were modeled by introducing random invariant offsets in comparators with a maximum dispersion of 230mV and zero mean value. Comparator uncertainly due to thermal noise and metastability was taken into account considering a time-variant random additive term with Gaussian distribution and 5mV standard deviation. The high offset values made it necessary to calibrate the first two stages, because they exceeded the half the LSB limit [1]: that is, off_{max} = 230mV > Q/2=125mV.

Comparator errors in the subADCs of STG_1 and STG_2, were calibrated concurrently without interrupting analogue input conversion using the developed method. The comparators in $STG_{1\text{-}2}$ used the same topology with a (3+1)-bit programmable bank, r = 3 in (8), and maximum correctable offset off_{max} of 300mV. A 10% error term depending on the calibration code was also considered to model calibration bank mismatch. Two offset logics, COCL in Fig. 3, were used for $subADC_1$ and $subADC_2$. The two estimation blocks, OAE_1 and OAE_2, operated concurrently and were based on the implementation presented in [8], considering a fixed-point description. They used constant adaptive steps, $\mu_1 = 2^0 = 1$ and $\mu_2 = 2^0 = 1$. The *Ncal* resolutions of X_1 and X_2 were 8 bits (discarding the less significant 6 and 4 bits of X_1^H and X_2^H, respectively). This approach provided sufficient margin for noise immunity while at the same time reducing the code-word lengths of the registers and accumulators. As with the offset estimation logic, two calibration code blocks, CCG_1 and CCG_2, were considered. The hardware models of these blocks were implemented by an incrementer/decrementer-by-one and a bank of registers.

Fig. 6a and Fig. 6b show the transient evolution of the adaptive calibration measurements for $subADC_1$ and $subADC_2$, respectively. A full-scale sinusoidal signal is considered as input stimulus. In each case the offset values associated with transitions $t_{1,1}$ and $t_{2,4}$ are depicted for the sake of conciseness (the right hand axes show their equivalent digital codes). The results include the actual location of offset in (8) (dotted curves $off_{1,1}$ and $off_{2,4}$) and the corresponding calibration code C_j. They also depict the initial uncalibrated offset $off_{i,j}[0]$ (lines with square markers) and the adaptive measurement ($OFF_{1,1}$ and $OFF_{2,4}$), evaluated from (6). Notice that the proposed technique has a very fast response even when two stages are calibrated simultaneously. In fact, less than one thousand samples are required to achieve convergence. In this situation the huge initial comparator offsets are compensated according to (9) below a safety interval around the ideal zero location with amplitude δ_i = 37.5mV (or Δ_i = 4 in its digital counterpart). The technique allows the correct operation of the $subADC_i$ even if the initial errors are located, as in this case, far from the half the LSB limit in a design with unitary redundancy. The ranges of digital correction (± Q/2) are represented in the figures limited by shadowed areas. Offset values inside the light areas satisfy the digital correction requirements [1], while offsets in the shaded regions, such as for $off_{1,1}[0]$ and $off_{2,4}[0]$ will violate this condition causing stage overranging.

The overranging phenomenon and the effect of calibration are illustrated in Fig. 7a-b. These figures show $subADC_1$ and STG_1 input-output characteristics before and after calibration (dotted red curve and continuous blue curves, respectively). In

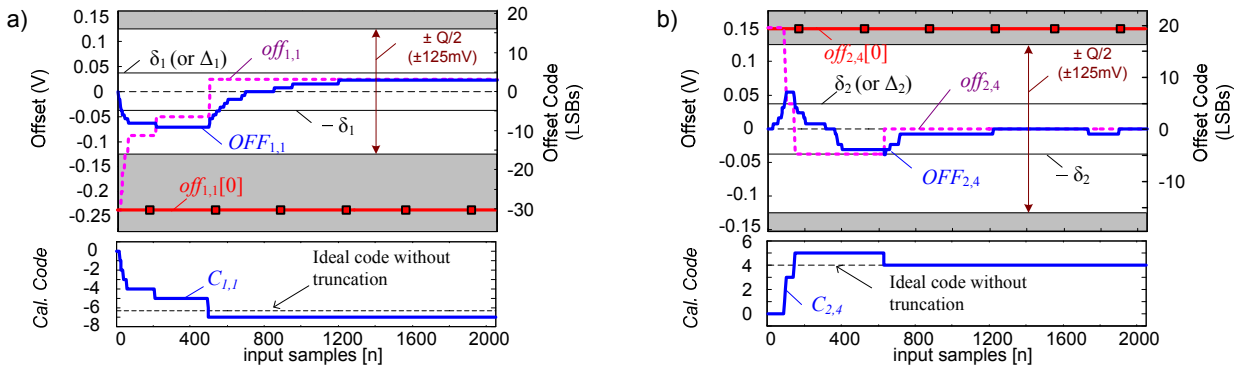

Fig. 6 Transient evolution of adaptive calibration measurements for: a) $subADC_1$, and b) $subADC_2$ (sensing references $t_{1,1}$ and $t_{2,4}$, respectively).

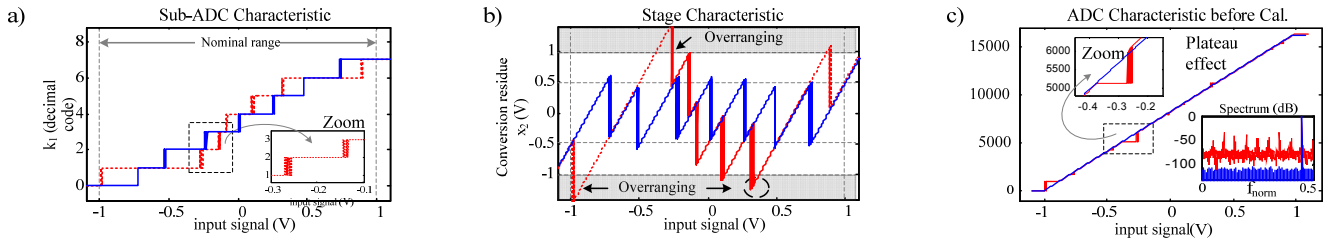

Fig. 7 First stage input-output characteristics of: a) the subADC and b) MDAC and c) the complete Pipeline ADC response before and after calibration

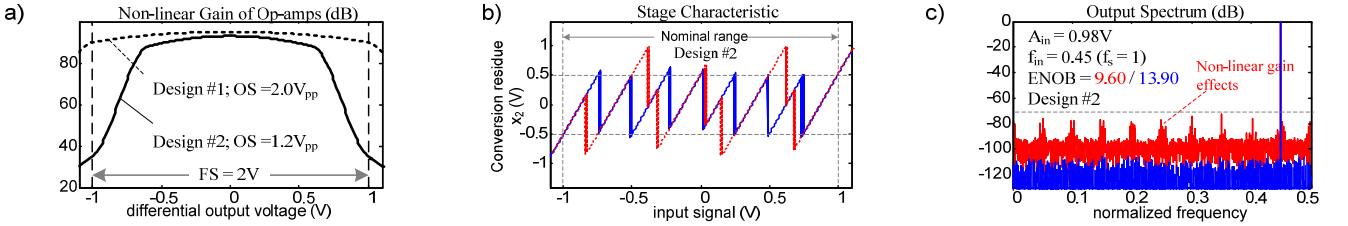

Fig. 8 a) Output swing requirement of $MDAC_1$ op-amp for 13.9 effective bits: without calibration (Design #1), and with calibration (Design #2); b input-output characteristics of STG_1 and c) output spectrum for the complete 14-bit Pipeline ADC before, and after calibration (Design #2).

each case the response of the complete 14-bit Pipeline ADC is also shown in Fig. 7c. Note that prior to calibration the amplified residue x_2 exceeds the converter reference R=1V, and some plateaus are produced in the final ADC output code X_I^H, limiting the *effective number of bits* (ENOB) to 4.4 bits. After offset compensation, this non-linear behavior completely disappears, almost achieving the 14.0-bit value expected in ideal MDACs. The maximum x_2 excursions is maintained close to half the reference *R*. Although omitted in the figure, the same behavior is observed for $subADC_2$ and $MDAC_2$.

Offset calibration improves the performance not only of comparators in low voltage applications, but also of MDAC amplifiers since their output swing requirements are significantly relaxed. This additional advantage becomes evident even if overranging is not present in the design. To illustrate this, let us consider a second case of study with maximum comparator offsets of 100mV and non-linear gain errors in the operational amplifiers (op-amp). A realistic shape-preserving model for op-amp gain was considered. Fig. 8a depicts a comparison of op-amp gain requirements in STG_1 for 13.9 effective bits without (design #1) and with (design #2) offset calibration. Note that the output swing can be reduced from approximately $2V_{pp}$ to $1.2V_{pp}$ (dashed and bold curves, respectively). Fig. 8b and Fig. 8c show the simulation results for the case of study based on design #2 with an output swing of 1.2Vpp. In both cases, the STG_1 input-output characteristic and the ADC output spectrum are shown before and after offset calibration, respectively. As the maximum comparator offsets was 100mV, overranging is avoided, and hence, only the op-amp impact is shown. Thanks to the reduction of amplified residue excursion after calibration, non-linear gain errors are also compensated. The simulation results show an ENOB improvement of 4.3 bits.

V. Conclusions

This paper presents a robust adaptive digital technique for comparator offset calibration in Pipeline ADCs. The proposed measurement-actuation procedure uses low-cost logic resources: basically a comparison block, an accumulator, an incrementer/decrementer and a small size register for storing the offset and correction codes. No extra analogue hardware is required since the comparator offsets are evaluated using the ADC's own back-end stages as a measurement instrument.

Thanks to calibration, comparator offset errors above half the stage least-significant bit (LSB) margin in a unitary redundancy scheme are admissible, thus relaxing comparator design requirements and allowing their optimization for low-power high-speed applications and low input capacitance. The technique also makes it possible to relax design requirements of stage amplifiers within the Pipeline queue, since output swing and driving capability are significantly lower (from 2Vpp to 1.2Vpp in a 14-bit Pipeline ADC case of study).

References

[1] S. Lewis et al., "A 10-b 20-Msample/s Analog-to-Digital Converter,'' *IEEE J. of Solid-State Circuits*, vol. 27, no. 3, pp. 351-358, Mar. 1992.

[2] J. Goes, J. C. Vital and J. Franca, "Systematic Design for Optimisation of Pipelined ADCs," *Kluwer Academic Publisher* (ISBN 0792372913), 2001.

[3] D. C. Daly, A. P. Chandrakasan, "A 6b 0.2-to-0.9V Highly-Digital Flash ADC with Comparator Redundancy", *IEEE Inter. Solid-State Circuits Conference*, *ISSCC*, pp. 554-555, Feb. 2008.

[4] J. He et al., "A simple and accurate method to predict offset voltage in dynamic comparators," *IEEE Inter. Symp. on Cir. and Systems*, ISCAS, pp.1934-1937, May 2008.

[5] Razavi, "Design of Analog CMOS Integrated Circuits," McGraw-Hill, 2000.

[6] Y.-Z. Lin, C.-W. Lin, and S.-J. Chang, "A 5-bit 3.2-GS/s Flash ADC With a Digital Offset Calibration Scheme," *IEEE Trans. on VLSI Systems*, vol. 18, no. 3, pp. 509–513, 2010.

[7] J. Hu, N. Dolev, B. Murmann, "A 9.4-bit, 50-MS/s, 1.44-mW Pipelined ADC Using Dynamic Source Follower Residue Amplification", *IEEE J. of Solid-State Circuits*, vol.44, no.4, pp.1057,1066, April 2009.

[8] A.J. Ginés, E. J. Peralias, A. Rueda, "Blind Adaptive Estimation of Integral Nonlinear Errors in ADCs Using Arbitrary Input Stimulus," *IEEE Trans. on Inst. and Meas.*, vol.60, no.2, pp.452-461, Feb. 2011.

[9] A. N. Karanicolas, Hae-Seung Lee and K. L. Barcrania, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. of Solid-State Circuits*, vol. 28, Dec. 1993, pp. 1207-1215.