MULTI-INPUT VOLTAGE AND CURRENT-MODE MIN/MAX CIRCUITS

I. Baturone, A. Barriga, J. L. Huertas

Instituto de Microelectrónica de Sevilla - Centro Nacional de Microelectrónica
Avda. Reina Mercedes s/n, (Edif. CICA)
E-41012, Sevilla, Spain

Multi-input Voltage and Current-mode Min/Max Circuits

I. Baturone, A. Barriga, J. L. Huertas

Dept. de Electrónica y Electromagnetismo
Facultad de Física Universidad de Sevilla, SPAIN

Abstract.-- This paper presents briefly a review of the different algorithms and hardware implementations for multi-input min/max operators. This allow us to show how a clever utilization of MOS devices leads to very simple current and voltage-mode min/max circuits.

I. INTRODUCTION

Minimum and maximum operators are typically employed to define the sentence connectives in any kind of fuzzy controller. In a Mamdani's controller they also define the fuzzy implication and aggregation mechanism. Before the development of fuzzy hardware, minimum/maximum circuits were already required in signal analysis (to perform operations such as median or normalization). Artificial neural networks that are trained with unsupervised learning also utilize them. In these applications it is not necessary to know the activity level of the dominating neuron but only to identify it.

In general, multiple minimum or maximum operations have to be realized. When only two-input operators are available, they are placed serially or in a binary tree, thus resulting in accumulative errors and time delays. This is why much work has been dedicated to the development of multiple-input operators.

Minimum and maximum circuits are discussed jointly in this paper because their implementations are usually complement or one of them can be obtained from the other by means of the De Morgan relation:

$$\text{Min}(x_i) = \overline{\text{Max}}(\overline{x}_i)$$

where - represents the complement operator.

II. ALGORITHMS FOR MAX OPERATORS

The different algorithms which have been proposed for multiple-input max operators have been the following:

$$x_o = \Sigma_i (x_i \Theta (x_o - \xi_i)) \text{ with } \xi_i = x_i \Theta \Sigma_{j \neq i} \xi_j \qquad (1)$$
$$x_o = A \Sigma_i (x_i \Theta x_o) \qquad (2)$$
$$x_o = \Sigma_i x_i H (x_i \Theta x_o) \qquad (3)$$

where x_i are the inputs, x_o is the output, A is a big number, Θ is the bounded-difference operator and H is Heaviside function. These are defined as:

$$a \Theta b = \begin{cases} a - b & \text{if } a > b \\ 0 & \text{otherwise} \end{cases}$$

and:

$$H(x) = \begin{cases} 1 & \text{if } x > 0 \\ 0 & \text{otherwise} \end{cases}$$

The first algorithm is analysed in [1], and a current-mode realization is proposed. The structure reminds those massively parallel neural nets in which neurons are fully interconnected. In this sense, each input current is replicated to inhibit all other inputs. The result is an $O(n^2)$ structure with the consequent large area occupation and slow operation due to many parasitic capacitors.

In the other two algorithms the inhibition signal for each input is represented by the mean value of those inputs which have not been zeroed out. The idea is based on a theorem by Hardy et al., which states that in a set of nonnegative numbers, x_i, minimum $(x_i) <$ mean $(x_i) <$ maximum (x_i). That is why the minimum is obtained by a very similar expression ($x_o = \Sigma_i x_i H (x_o \Theta x_i)$). The inhibition signals are then simple to generate as they do not involve internal variables, like ξ_i in the first case. Then, structures of O(n) complexity are possible.

The second algorithms is proposed in [2], while the third one is described in [3]. The latter provides more precision, because equation (3) can be also expressed as $\Sigma_i (x_i \Theta x_o) = 0$, which is obtained from (2) when A tends to infinity. From a hardware point of view, the precision of a max circuit is evaluated by the needed difference between inputs to obtain a single dominating one and by the observed error at the output when all the inputs have an equal value. A high gain value of A means that the former errors are proportionally reduced. This translates in using feedback schemes with high gain blocks.

The problems arise because of the cost to pay for this high gain. Several solutions lead to a large area (if resorting to the use of operational amplifiers [4] or large current mirror ratios [5]). Besides, they operate at a low speed due to a required dominant pole which achieves stability (if several gain stages are cascaded [2-5-6]). The current-mode max circuit which is described in [7] avoids those drawbacks because only two transistors take part in the feedback loop. For n inputs this circuit consists in 5n+1 transistors.

The authors have recently proposed a modification to the previous structure which reduces the required transistors to 3n+1, yet achieving the same precision [8]. Its quite simple structure, which is shown in Fig. 1a, leads to low area and power consumption and to high frecuency performance. This reduction is possible because all the potentialities of MOS transistors are
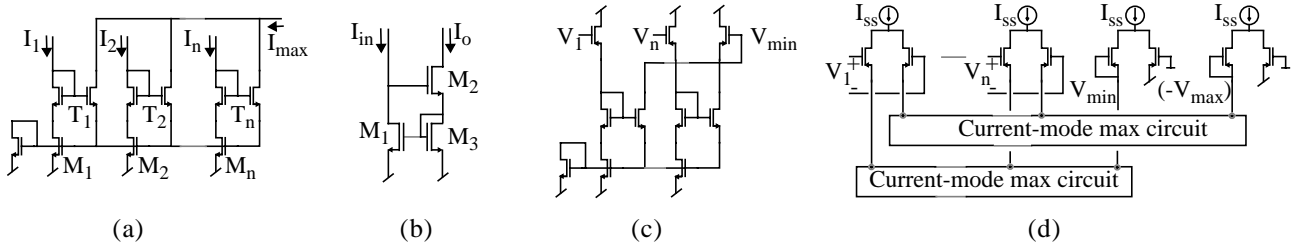
Fig. 1.- (a) Proposed current-mode max circuit. (b) Wilson current mirror. (c) Proposed voltage-mode minimum circuit. (d) Proposed voltage-mode differential min/max circuit.

exploited. To show this, let us compare it with the typical voltage-mode circuit which consists in diodes and operational amplifiers acting as voltage followers [4]. The output voltage is shared and fed back to all the amplifiers. The actions of the diodes make that only a single operational amplifier receives the proper output voltage to perform a voltage following, the others being saturated. For a resembling current-mode design, current-followers are needed. Among them, the Wilson current mirror works with a very similar structure to that of a voltage follower. The transistor level schematic is illustrated in Fig. 1b, where the dashed line represents the feedback wire. According to this figure, an small signal analysis leads to $v_{g2}=i_{in}r_{ds1}$ and $i_o=g_{m2}v_{g2}=g_{m2}r_{ds1}i_{in}$. The feedback is realized by connecting the gates of M_1 and M_3. Thus, the expression for I_o in the feedback configuration is the following:

$$I_o = g_{m2}r_{ds1}\left(I_{in} - \frac{g_{m1}}{g_{m3}}I_o\right)$$

The gain value A is, then, equal to $g_{m2}r_{ds1}$. Similar to the voltage case, in the structure of Fig. 1a the feedback voltage is shared by all the cells. This voltage is fixed to the value needed by a MOS transistor to be in saturation conducting the maximum input current I_{max}. There is no need for diodes in the feedback path because transistors T_i already act as diodes: if $I(M_x) < I(M_y)$, M_x enters ohmic region, so that $V_g(T_x)$ decreases and T_x goes off; if $I(M_x) > I(M_y)$, M_x enters saturation region and T_x, acting as a voltage follower, closes the feedback loop which makes $I(M_x) = I(T_x)$.

III. VOLTAGE-MODE MIN/MAX CIRCUITS

In this section we propose voltage-mode min/max operators which are based on a double conversion V-I/I-V. The idea resembles that of a current mirror. In the latter, an input current is non-linearly converted to a voltage. The same voltage arrives to a matched transistor which realizes the inverse operation. In the single or differential-input min/max circuits of Fig. 1c,d the input voltages are non-linearly converted to currents. The current-mode max circuit replicates the maximum current to a matched transistor. This technique is extremely sensitive to the precision with which the current is transferred. In this sense, the high output impedance of the current-mode max circuit is a very appealing feature. This is a novelty of our max circuit because transistors T_i are not only employed as voltage followers but also as devices which convey the current from a low impedance to a high impedance node, thus avoiding additional cascode or regulated output stages. While current-mode circuits employ De Morgan's law to obtain min/max operators, voltage-mode circuits exploit the dual behaviour of pmos and nmos transistors. This means that a voltage-input maximum circuit is obtained from the minimum one in Fig. 1c by changing the pmos by nmos transconductors (and employing a current-mode max circuit with pmos transistors).

REFERENCES

[1] M. Sasaki, T. Inoue, Y. Shirai and F. Ueno, "*Fuzzy multiple-input maximum and minimum circuits in current mode and their analysis using bounded difference equations*", IEEE Trans. on Computer, Vol. 39 (6), June 1990, pp. 764-774.

[2] T. Inoue, F. Ueno and T. Motomura, "*Analysis and Design of Analog CMOS Building Blocks for Integrated Fuzzy Inference Circuits*", Proc. ISCAS, Singapore 1991, pp. 2024-2027.

[3] B. W. Suter and M. Kabrisky, "*On a Magnitude Preserving Iterative MAXnet Algorithm*", Neural Computation, Vol. 4, pp. 224-233, 1992.

[4] J. G. Graeme, "*Designing with Operational Amplifiers*", Mc Graw Hill, 1977.

[5] K. Tsukano, T. Inoue and F. Ueno, "*A design of current-mode analog circuits for fuzzy inference hardware systems*", Proc. ISCAS, May 1993, pp. 1385-1388.

[6] J. L. Huertas, S. Sánchez-Solano, I. Baturone and A. Barriga, "*Building Blocks for Current-Mode Implementation of VLSI Fuzzy Microcontrollers*", Proc. IFSA, Seul 1993, pp. 929-932.

[7] M. Sasaki, N. Ishikawa, F. Ueno and T. Inoue, "*Current Mode Analog Fuzzy Hardware with Voltage Input Interface and Normalization Locked Loop*". IEICE Trans. Fundamentals, Vol. E75-A (6), June 1992, pp. 650-654.

[8] I. Baturone, J. L. Huertas, A. Barriga and S. Sánchez-Solano, "*Current-Mode Multiple-Input Maximum Circuit*", Electronics Letters, Vol. 30 (9), April 1994, pp. 678-680.

$$(2)$$