ANALYTICAL MODELING OF NANOSCALE 4H-SiC MOSFETs FOR HIGH POWER APPLICATIONS

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May 29, 2016

Supervisor's Certificate

This is to certify that the work presented in this dissertation entitled *Analytical Modeling of Nanoscale 4H-SiC MOSFETs for High Power Application* by *Manoj Kumar Yadav*, Roll Number 214EE1223, is a record of original research carried out by him under my supervision and guidance in partial fulfillment of the requirements of the degree of *Master of Technology* in *Electrical Engineering*. Neither this dissertation nor any part of it has been submitted for any degree or diploma to any institute or university in India or abroad.

Supervisor's Signature

Dedicated

to

The Dreams and Sacrifices of
My Loving Parents,
And
my Dear Ones who Love me a Lot.

Declaration of Originality

I, Manoj Kumar Yadav, Roll Number 214EE1223 hereby declare that this dissertation entitled *Analytical Modeling of Nanoscale 4H-SiC MOSFETs for High Power Applications* represents my original work carried out as a postgraduate student of NIT Rourkela and, to the best of my knowledge, it contains no material previously published or written by another person, nor any material presented for the award of any other degree or diploma of NIT Rourkela or any other institution. Any contribution made to this research by others, with whom I have worked at NIT Rourkela or elsewhere, is explicitly acknowledged in the dissertation. Works of other authors cited in this dissertation have been duly acknowledged under the section Bibliography. I have also submitted my original research records to the scrutiny committee for evaluation of my dissertation.

I am fully aware that in case of any non-compliance detected in future, the Senate of NIT Rourkela may withdraw the degree awarded to me on the basis of the present dissertation.

May 29, 2016
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Manoj Kumar Yadav

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Abstract

Threshold voltage instability was investigated for 4H-SiC MOSFETs with SiO_2, Si_3N_4 and HFO_2 gate oxides. Threshold voltage changes observed in the drain current Vs. gate voltage (I_D-V_G) characteristics was determined using various gate voltage sweeps at room temperature. Three types of MOSFETs show different instability characteristics. Depending on gate voltage, many difficulties come up with 4H-SiC MOSFETs, such as low mobility and poor reliability.

The characteristics like channel potential, field distribution and the threshold voltage of the proposed models of MOSFETs, 4H-SiC and SOI-4H-SiC were compared with simulator results to validate the models. Short channel effects (SCEs) were also investigated and compared with the existing nanoscale silicon MOSFETs The surface potential model is calculated by using the two-dimensional Poisson equation. The specifications of the model are examined by several MOSFET parameters such as body doping concentration, metal gate work function, silicon carbide layer thickness, thickness of metal gate oxide layer, buried oxide thickness, drain to source voltage, and gate to source voltage. The outcomes of modeling and simulation of 4H-SiC MOSFETs model show that the proposed models can reduce short channel effects more than the Silicon MOSFETs. Proposed models highly reduces the drain-induced-barrier-lowering (DIBL) to meet the performance fulfillment in Nano electronic applications when compared to silicon MOSFETs. Establishing the results, we have noticed that this model can be utilized as a useful tool for the characterization and design of high-efficiency 4H-SiC nanoscale MOSFETs. By matching the two-dimensional device simulation results with analytical modeling, the validity of the recommended models are proven.

0.1 Keywords

4H-SiC; MOSFET; Short channel effects (SCEs); 2-D modelling; Threshold Voltage Instability; SOI; TCAD.

List of Acronyms

Acronym	Description
FET	Field Effect Transistor
JFET	Junction Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon On Insulator
SCEs	Short channel Effects
DIBL	Drain-Induced-Barrier-Lowering
CLM	Channel Length Modulation
EBD	Energy Band Diagram
TC	Transfer characteristic
OC	Output Characteristic
SM	Semiconductor Material
FD	Fully Depleted
S-SOI	Strained-Silicon-On-Insulator
VS	Velocity Saturation
HCE	Hot Carrier Effect
2-D	Two-Dimensional
VLSI	Very Large Scale Integration
WBG	Wide Band-Gap
NBG	Narrow Band-Gap
LPA	Low Power application
HPA	High Power Application
RDC	Relative Dielectric Constant
ITD	Interface Trap Density
PFC	Power Factor Correction
MDI	Motor Driver Inverter
BC	Buck Converter
HCM	High Channel Mobility
CB	Conduction Band
VB	Valance Band
FG	Forbidden Gap
H	Hexagonal
C	Cubic
CSIR	Council of Scientific & Industrial Research
BV	Blocking Voltage
ECB	Electronic Contribution

continued on the next page

List of Acronyms (*continued*)

Acronym	Description
ICB	Ionic Contribution
OCB	Orientation Contribution
CBO	Conduction Band Offset
TCE	Trichloro Ethyleen
CAD	Computer Added Design

List of Symbols

Symbol	Description
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
Si_3N_4	Silicon Nitride
HFO_2	Hydrogen Floro Dioxide
G_aN	Gallium Nitride
G_aA_s	Gallium Arsenide
Si	Silicon
μ	Mobility
λ	Constant
α	Constant
β	Constant
Γ	Constant
σ	Constant
T	Temperature in Kelvin
V_d	Drift Velocity
m	Material Constant
NO	Nitric Oxide
C	Diamond
G_e	Germanium
ε_r	Relative permitivity
ε_0	Absolute Permitivity
L	Channel Length
K	Boltzmann constant

continued on the next page

List of Symbols (*continued*)

Symbol	Description
$E_{g,SiC}$	Energy bandgap of SiC
V_T	Thermal voltage
$E_{g,Si}$	Energy bandgap of Silicon
q	Electron charge
ϕ_M	Metal gate work function
N_A	Channel doping concentration
N	Source and Drain doping
N_b	Substrate concentration
n_{Si}	Intrinsic concentration in Silicon
n_{4H-SiC}	Intrinsic concentration in 4H-SiC
ε_{Si}	Dielectric material constant of silicon
ε_{Si}	Dielectric material constant of SiC
t_{Si}	Silicon film thickness
t_{SiC}	SiC thin film thickness
t_{ox}	Thickness of gate oxide layer
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
V_{sub}	The substrate bias
X_{4H-SiC}	Electron affinity of Silicon carbide
$\phi_s(X)$	Surface potential
V_{th}	Threshold voltage
I_D	Drain Current
C_{ox}	Oxide capacitance

continued on the next page

List of Symbols (*continued*)

Symbol	Description
C_{SiC}	Capacitance of SiC thin layer
C_{Si}	Capacitance of Silicon thin layer

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Chapter 1

Prologue

MOSFET stands for "Metal oxide semiconductor field effect transistor" [1]. MOSFET is a four-terminal semiconductor device i.e. gate, source, drain, and substrate. MOSFET is a semiconductor device thus it can conduct current better than an insulator. MOSFETs can be used for low power applications as well as high power applications [2]. MOSFET is a Voltage controlled and dominant VLSI device. From last many years, silicon is most preferable semiconductor material used for MOSFETs. But there are some limitations of silicon material e.g. silicon can be used only for low power applications [2], it can not be used for high power applications. The band-gap of the silicon material is 1.1 eV [3]. Hence, it breakdown voltage is very low. Silicon semiconductor material is more sensitive to temperature [4] so it can not be operated at the higher temperature. Therefore, due to these limitations of silicon material, one new semiconductor material Silicon carbide [5] comes into the picture. Silicon carbide material is used for a variety of applications. .

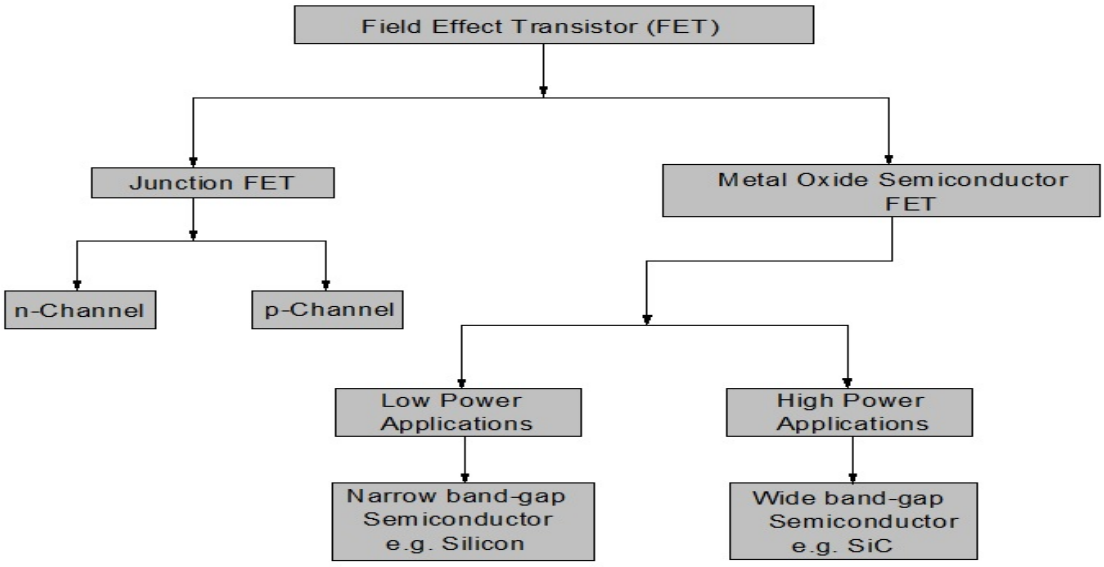


Figure 1.1: Classifications of field effect transistor.

1.1 Overview of SiC

Silicon carbide (SiC) was incidentally discovered in 1890 [6] by Edward G. Acheson, an assistant to Thomas Edison. SiC is a compound semiconductor and is a mixture of silicon and carbon with chemical formula SiC [6] as shown in figure 1.2 [10]. Silicon is covalently bonded with carbon [6]. Silicon carbide is a wide band-gap semiconductor material [7]. SiC exists in a kind of polymorphic crystalline buildings known as poly types, e.g., 3C-SiC, 4H-SiC, 6H-SiC [8]. According to the Ramsdell classification scheme the number indicates the layer and the letter indicate the Bravais lattice [8], like H, indicates hexagonal, C indicates cubic [8].

Presently 4H-SiC is usually preferred in power device manufacturing. In 4H-SiC, there are four layers in structure and it is hexagonal. Thats mean in 4H-SiC structure, four hexagonal layers of silicon carbide are present [9] as shown in figure 1.3 [12]. SiC is a wider bandgap (Eg) material with $Eg = 3.3eV$ [9] as compared to silicon that has band-gap of ($Eg = 1.1eV$). Hence, SiC has a bandgap three times higher than silicon. Due to its large bandgap, it has higher blocking voltage [7]. SiC is the most advancing substrates for power devices due to its higher blocking voltage, elevated operating temperature, and admirable thermal conductivity [7].

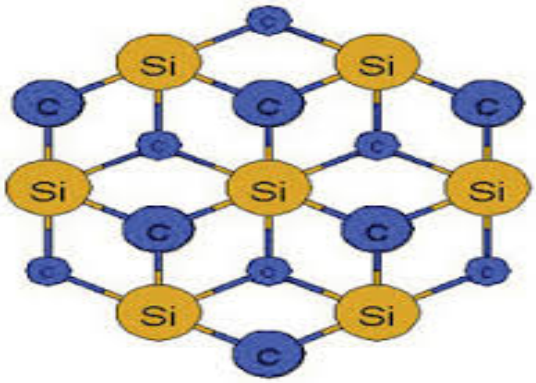


Figure 1.2: Crystal structure of SiC.

4H-SiC MOSFETs are the power MOSFETs devices that have low switching losses and that can deliver low conduction with high breakdown voltages [11]. At present, SiC power MOSFETs with breakdown voltages from 500 to 1500V [7] are readily available. SiC devices can also be made to have much thinner drift layer, and greater doping concentration, i.e., breakdown area for SiC is 2.4MV/cm [7] compare to silicon that has breakdown discipline of 0.25MV/cm [3]. That means breakdown field for Silicon is ten times lesser than Silicon carbide. Electron mobility (μ) for SiC is 950 cm2/V.s [11] compare to Silicon, μ = 1400 cm2/V.s. This analogy shows electron mobility for Silicon carbide is quite less as compared to silicon. The continuous shrinkage of the device may require for attaining excessive packing density and higher efficiency.

The concept 4H-SiC came into the picture due to some limitations of silicon semiconductor material. Now-days both p-type 4H-SiC and n-type 4H-SiC [13] can be formed that are necessary for semiconductor materials for fashion device design issues.

1.1.1 Properties of SiC material

SiC is a wide bandgap semiconductor material. It has some specific properties. This section contains the properties of 4H-SiC material [14] and comparison with the properties of another material is shown in Table 1.1.

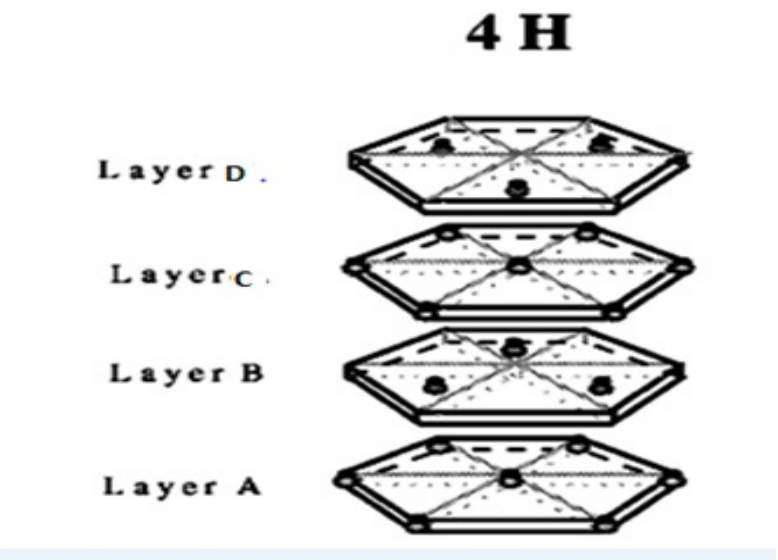


Figure 1.3: Crystal structure of 4H-SiC.

1.1.2 Advantages and drawbacks of 4H-SiC semiconductor material

The popular advantages and drawbacks of 4H-SiC semiconductor material are:

- The bandgap of 4H-SiC Material is large due to this its breakdown voltage is high it means 4H-SiC can be operated at high voltages.
- The Breakdown field and carrier concentration of 4H-SiC are high thus taking the advantage of the properties it can meet all the three characteristics of the power switch, i.e., low on-resistance, high voltage and fast switching speed [15].
- The larger bandgap of SiC means devices can operate at higher temperatures. Presently SiC devices guaranteed operated from 150℃- 200℃. It means SiC semiconductor is less sensitive to temperature [16] than silicon material.
- Thermal conductivity and saturation velocity [17] of 4H-SiC semiconductor material is high it means the current caring capacity of 4H-SiC MOSFET is high than the Silicon MOSFET.
- The mobility of 4H-SiC semiconductor material [9] is less comparable with silicon material so to improve the mobility of 4H-SiC MOSFET types of research are going on.
- Threshold voltage instability [18] is also a big problem for 4H-SiC MOSFET. Threshold voltage instability is due to the presence of trap charges at the semiconductor/gate oxide interface in 4H-SiC MOSFETs.

Table 1.1: Properties of 4H-SiC material

Properties	**Silicon**	**4H-SiC**	**GaN**	**GaAs**
Crystal structure	Diamond	Hexagonal	Hexagonal	Zincblende
Band-gap (eV)	1.11	3.25	3.5	1.43
Electron Mobility ($cm^2/V.s.$)	1400	900	1250	8500
Breakdown Field (MV/cm)	0.25	2.5	2.5	0.4
Thermal Conductivity (W/cmK)	1.5	4.9	1.3	0.5
Saturation Velocity $(cm/s)X10^7$	1	2.6	2.6	2
Relative Dielectric Constant	11.8	9.7	9.5	12.8

1.1.3 Application of 4H-SiC semiconductor material

4H-SiC semiconductor material has high power applications [16]. There are many applications of 4H-SiC. The most popular applications are:

- Solar inverters
- DC to DC converters
- Bi-directional converters
- Inverters for induction heating equipment
- Motor drive inverters
- Buck converters
- Power factor correction (PFC) circuits

1.1.4 Challenges of 4H-SiC MOSFETs

The performance of the 4H-SiC MOSFETs heavily depends on the conditions under which it is evaluated. Under restricted conditions, the system can attain high performance. There are some difficulties with 4H-SiC MOSFETs.

- **Threshold voltage instability**:Threshold voltage instability [7] in 4H-SiC MOSFETs is due to presence of many types of trap charges [1] at the interface of semiconductor/gate oxide interface. There is always some charges located in the gate oxide layer and some charges at the

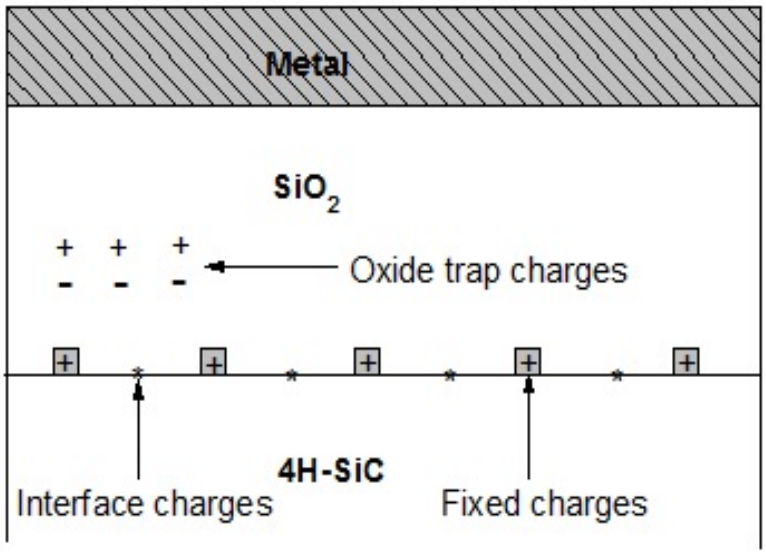


Figure 1.4: different types of trap charges.

semiconductor/oxide interface. Due to the presence of these charge in the gate oxide, there will require a shift in the gate voltage to reach the threshold voltage condition. Oxide quality identifies by the charges presented in the oxide. There are various types of charges [1]. There are non-ideality present at the interface called interfaced trapped charges.
These interface trapped charged may come about because of some various thing as shown in figure 1.4. It can be because of some mechanical damages already present in the wafer. It can be because of breaking 4H-SiC bonds. These oxide charges are mostly always only positive charges and these come out because of incomplete oxidation. If applied gate voltage is positive then all mobile ions get pushed to the interfaced [7] and if we applied negative gate voltage all mobile ions would move up towards the surface. This check whether the mobile ions are present or not. It can be done very simply by doing a proper C-V analysis

- **Poor Mobility** Mobility denotes how much fast the charge carriers are moving from one place to another place. Electron mobility is always greater than hole mobility [19] i.e. electron can travel more quickly and also contributes more current than a hole. The mobility of charge carriers always dependent on the temperature [20]. As temperature increases, the atoms in the material will vibrate and give to the thermal vibrations. The mobility of charge carrier decreases with temperature [20].

$$\mu \propto \mathrm{T}^{-m} \tag{1.1}$$

Where m is constant and different for material to material

As from the equations

$$\mu = \frac{V_d}{E} \; and \; V_T = \frac{T}{11600} \tag{1.2}$$

For a large variation in the temperature (0-300°K) there will be a small change in threshold voltage (0-26mV) so it means up to 300°K [21], thermal voltage increases slowly, means electrical field intensity E will be low therefore if the field is small then mobility will be high [22]. An electric field always depends on the permittivity of the dielectrics. So by setting the value of dielectric can be improved the mobility of the 4H-SiC MOSFETs.

1.2 Motivation of the Work

4H-SiC MOSFET is an emerging device for high power application in the field of semiconductor technology that has a lot of real-world applications. A depth organization of science and relevancy is essential. There are many techniques have been developed to enhance the performance of semiconductor devices. Unluckily, despite this success of the 4H-SiC MOSFETs over the last decades for high power applications. The performance of this device degrades where the high mobility is required. This phenomenon is important where the high blocking voltage is required. 4H-SiC MOSFET device gives high drain current comparable to Silicon MOSFET devices. this device can also be operated at a higher temperature.
The focus of the 4H-SiC MOSFET research in the last few years has intensified on the reduction of instability in threshold voltage and improvement in the mobility. Many years ago, conventional MOSFETs used for the research had dimensions in micrometers, but nowadays dimensions scale down to nanometers [23]. Nanoscale MOSFETs improves the performance of the device comparable to conventional MOSFETs. but one big problem with nanoscale MOSFETs is shorts channel effects(SCEs) [24]. without reducing the short channel effects, MOSFETs can not give the good performance. Thus, there is a need to reduce the SCEs for better performance. This dissertation aims to extend the research on short channel effects and develop new methods by which performance can be enhanced in nanoscale MOSFETs.

1.3 Literature Survey

Considering the last few year, 4H-SiC MOSFETs turns into a standard research matter in the field of semiconductor devices. Various types of investigations have been taken by the many researchers in 4H-SiC MOSFETs. Few number of these research idea enhance my awareness to implement into the research of 4H-SiC

MOSFETs. Right here is the concise description of literature survey undertaken in this research work. This research work mainly has four sections such as characteristics of the 4H-SiC MOSFETs, threshold voltage instability in 4H-SiC MOSFETs using various type of dielectrics, short channel effects in nanoscale 4H-SiC MOSFET and short channel effects in nanoscale 4H-SiC MOSFETs. Literature survey is classified as follows:

1.3.1 Instability in threshold Voltage

Threshold voltage instability [7] in 4H-SiC MOSFETs is due to the presence of many types of trap charges at the interface of Semiconductor/gate oxide interface [13]. There is always some charges located in the gate oxide layer and some charges at the semiconductor/oxide interface. Due to the presence of these charge in the gate oxide, there will require a shift in the gate voltage to reach the threshold voltage condition. So it is a big problem in 4H-SiC MOSFET devices.
In *February* 2015, *Dr. Hiroshi Yano* and *Dr. Natsuko kanafuji* [7] proposed a technique to reduce the instability in 4H-SiC MOSFET. They were taken nitride and phosphorus doped gate oxides. They verified the shift in threshold voltage in the both direction of drain current vs. gate voltage characteristics. It was observed by using several gate voltage sweeps at room temperature and above room temperature up to 200. The shift in the threshold was also evaluating using negative bias and positive bias temperature stress. There are two types of MOSFETs one with $POCl_3$ gate oxide and another one is NO gate oxide [7]. And they have different-different instability characteristics. It is seen that there are oxide trap charges present in phosphorus doped oxide operation and interface trap charges are found in the process with nitride oxides
Thus, the threshold voltage instability studied have been done using $POCl_3$ oxide and NO oxides in the bidirectional $I_D - V_G$ characteristics at various elevated temperatures [7]. In the positive gate bias means on state, gate voltage depends on threshold voltage and a stable threshold voltage was evaluated in phosphorus doped gate oxide. And in the reverse bias means when negative threshold voltage is applied then there is a shift in threshold voltage due to the presence of trap charges in the oxide injected by F-N tunneling [7]. On the other side, when the positive voltage is applied means in forward bias, there was a large variation in the threshold voltage even at VGS = 10 V due to the trap charges located near the oxide/4H-SiC interface. And in the off-state gate voltage depends on the threshold voltage, a small shift in the V_{th} was found for both NO and $POCl_3$ at elevated temperature.
Thus, the use of $POCl_3$ is more suitable than the NO oxide because it has high channel mobility. But stable threshold voltage can be observed under small oxide

field [7].

1.3.2 Performance of fully depleted strained-SOI MOSFETs regarding SCEs

The purpose of this literature was, to propose a model of 4H-SiC MOSFET for the surface potential and threshold voltage to estimate the short channel effects (SCEs). It was done by solving the two-dimensional Poisson equation in the thin film of strained-silicon. And verify the behavior of the surface potential and threshold voltage on several device parameters such as channel length, strain, strained-silicon film thickness, gate metal work function, supply voltages and doping concentrations.

In *October* 2006, *Dr. M.Jagadesh Kumar* and *Dr. Vivek Venkataraman* [25]first time proposed an accurate and simple analytical solution for surface potential of nanoscale fully depleted stained SOI MOSFET by using the two-dimensional Poisson equation. The authors have considered various types of parameters: 1) effects of strain, 2) thin film doping of strained silicon, 3) thickness of strain silicon thin film, 4) metal gate work function, 5) short channel effects, 6) supply voltages and other various parameters. By matching the outcomes from the developed analytical model and 2D simulation outcomes obtained using MEDICI tolls the accuracy has been verified. It has been clear that the proposed model is correct, and the threshold voltage decreases with the decrease in channel length [25] and also there is a decrement in threshold voltage with increasing strain [25]. It is also seen that the height of the potential barrier is small at the source side so the electrons can easily move from source to drain resign.

The two-dimensional Poisson equation [3] has been solved by using four boundary conditions in the strained-silicon region. The threshold voltage values calculated from the proposed model match well with the results carried from the simulation. And it is concluded that there is a minute drop in the threshold voltage with decreasing channel length and increasing strain in the thin film as compared to the without using strain in the silicon film. Therefore the performance of the silicon MOSFET enhanced by using strain in the thin layer of silicon

1.4 Objectives of the Work

The general aims of the thesis are:-

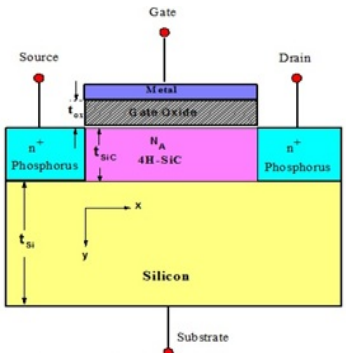
- To study the characteristics of Silicon and 4H-SiC MOSFETs with various types of dielectrics and compare them.

- To study the Threshold voltage instability in 4H-SiC MOSFET with SiO_2, Si_3N_4 and HFO_2 dielectrics [1].
- To develop a technique to improved the mobility of the 4H-SiC MOSFETs
- To propose a new technique to reduce the threshold voltage instability in 4H-SiC MOSFETs.
- To Study of the short channel effects in Silicon and 4H-SiC MOSFETs.
- To develop a technique to reduce the short channel effects for 4H-SiC MOSFETs.
- To propose a model of CMOS for 4H-SiC MOSFETs.

1.5 Organization of the Thesis

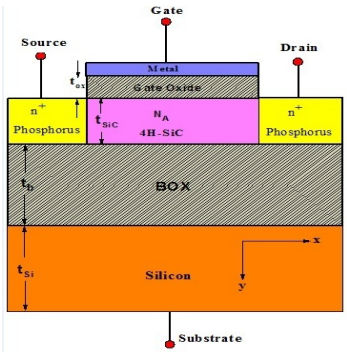
This thesis work proposes a systematic investigation of characteristics and short channel effects to enhance the performance of the 4H-SiC MOSFETs. The work is presented in a sequential way to demonstrate the trade-off between feature dimension and performance. After evaluating the performance of the 4H-SiC MOSFET, it is extended to reduce the short channel effect with nanoscale SOI 4H-SiC MOSFET model. This thesis is organized into five chapters starting with Prologue of the thesis.The remaining of the thesis is organized as follows: -

Chapter 2: (Fundamental study of the 4H-SiC MOSFET) it covers the basics of wide band gap semiconductors, the study of various types of dielectrics, characteristics of the conventional 4H-SiC MOSFET, comparison of characteristics between silicon and 4H-SiC MOSFETs, threshold voltage instability in 4H-SiC MOSFETs with different kinds of dielectrics. It is enough to understand the basic concept of the 4H-SiC MOSFET and propped new techniques to improve the performance of the 4H-SiC MOSFET. This chapter also covers the overview of databases used in this work.



Chapter 3: (Analytical Model of 4H-SIC MOSFET in Nanoscale) This chapter belongs to the shorts channel (SCEs) effects in 4H-SiC MOSFETs. This chapter includes the basic study of the short channel effects, types of short channel effects, a simple two-dimensional analytical modeling of surface potential, threshold voltage and electric field distribution with various device parameters such as metal gate function, SiC thin film thickness, gate oxide film thickness, doping concentration and other parameters, to reduce the short channel effects in nanoscale 4H-SiC MOSFET devices. Simulation of 4H-SiC MOSFETs and then to verify the validity of the model matched the results

from analytical modeling with the results obtained from the simulation.



Chapter 4: (Nanoscale SOI-4H-SiC MOSFETs Analytical Model) This chapter is the modified version of the chapter 3 to improve the performance of 4H-SiC MOSFET in respect of short channel effects. This chapter includes the basic building of silicon-on-insulator 4H-SiC MOSFET, mathematical 2D solution for threshold voltage, surface potential and field distribution in 4H-SiC MOSFET to reduce the short channel effects. Simulation of SOI-4H-SiC MOSFETs and then matched the outcomes obtained from the analytical modeling and outcome obtained from simulation to verify the validity of the model.

Chapter 5: (Conclusion and Future Scope) Summarizes the work presented in the thesis, scope of the work in future that need move investigation.

1.6 Summary

This chapter deals with introduction and history of silicon carbide semiconductor material. The objectives and motivation of this research are also considered. The objective of this research is to reduce the short channel effects, threshold voltage instability in 4H-SiC MOSFET and improve the performance of the MOSFET devices. This chapter also deals with the structure design issues, characteristics and applications of SiC MOSFETs. Finally, a brief plan of work is discussed.

Chapter 2

Fundamental study of 4H-SiC MOSFET

2.1 Introduction

SiC is a compound semiconductor and is a mixture of silicon and carbon with chemical formula SiC. Silicon is covalently bonded to carbon. Silicon carbide is a wide band-gap semiconductor material [15]. SiC exists in a kind of polymorphic crystalline buildings known as polytypes, e.g., 3C-SiC, 4H-SiC, 6H-SiC. According to the Ramsdell classification [8] scheme, the number indicates the layer and the letter indicate the Bravais lattice, like H, indicates hexagonal, C indicates cubic. Presently 4H-SiC is usually preferred in power device manufacturing. In 4H-SiC, there are four layers in structure, and it is hexagonal. That mean in 4H-SiC structure four hexagonal layers of silicon carbide are present. 4H-SiC is a wider bandgap (Eg) material with $Eg = 3.3eV$ as compared to silicon that has a bandgap of ($Eg = 1.1eV$). Hence, SiC has a band-gap three times higher than silicon.

Bandgap = energy required by an electron to moves freely inside the

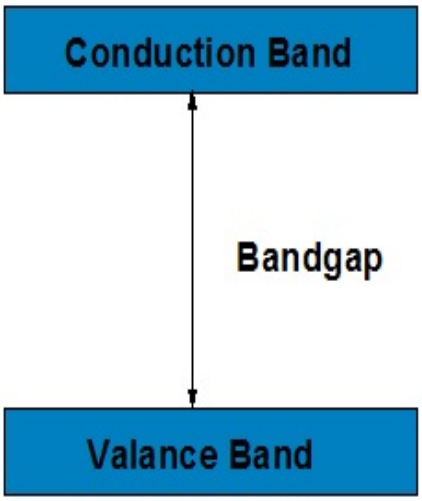


Figure 2.1: Energy Band diagram.

semiconductor. For metal valance band and conduction band are overlapped. Means energy difference between top of the valence band and bottom of the conduction band is very low compared to semiconductors.
Higher breakdown field so that material can block higher voltage at higher temperatures with lower leakage current.
The highest filled band is known as the valence band, or the highest energy band is valance band.
The lowest filled band is conduction band.
So to have a semiconductor is not like metal where free electrons are, neither it is like an insulator where no current flow. It needs to have the resistance of the semiconductor depends on how much electrons have in the conduction band.

So the bandgap is the property to find the conductivity of the semiconductor.

Table 2.1: Energy Bandgaps of various semiconductors

Materials	**Chemical symbol**	**Bandgap energy (eV)**
Germanium	Ge	0.7
Silicon	Si	1.1
Gallium Arsenide	GaAs	1.4
Silicon Carbide	SiC	3.3
Gallium Nitride	GaN	3.4
Diamond	C	5.5

Therefore, due to its large bandgap, it has higher blocking voltage [5]. SiC is the most rising substrates for power devices due to its higher blocking voltage, elevated operating temperature, and admirable thermal conductivity. 4H-SiC MOSFETs are the power MOSFETs devices that have low switching losses and that can deliver low conduction with high breakdown voltages.

2.2 Conventional 4H-SiC MOSFET Structure

The structure of the conventional 4H-SiC MOSFET is shown in figure: 2.2. The dimensions of the structure are taken in micrometers. This structure of 4H-SiC MOSFET consists of a silicon substrate of 80 μm in length and 50 μm in width, 4H-SiC thin layer thickness of 4 μm and gate oxide thickness of 20 nm. In this device SiO_2 is used as a gate oxide. In this structure a 4H-SiC p-type epilayer grown on n-type substrate
The epilayer is doped with boron concentration of $7 \times (10^{15})$ cm^{-3} [7]
Source and Drain regions are doped with phosphorus concentration of $2 \times (10^{21})$ cm^{-3} [7]
Aluminum ions are implemented for body contact regions.
Channel length = 50 μm
oxide thickness = 45 nm
Metal thickness = 20 nm

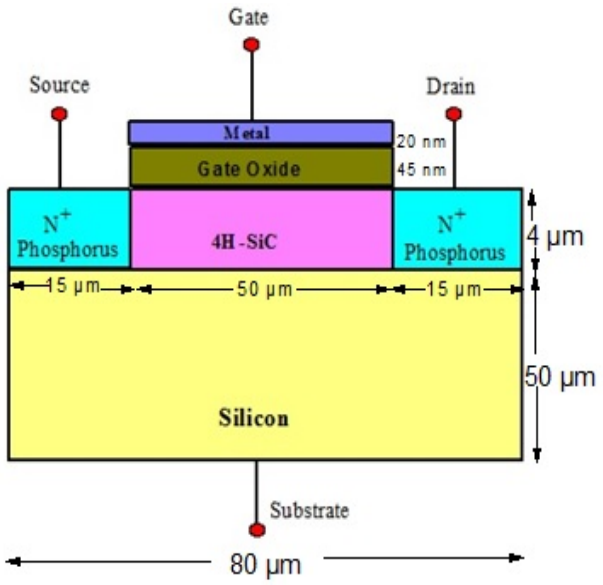


Figure 2.2: Structure of conventional 4H-SiC MOSFET .

2.3 Dielectrics

Dielectric is a quantity measuring the ability of a substance to store electrical energy in an electric field. The relative permittivity of material is its dielectric permittivity expressed as a ratio about the permittivity of vacuum [1]. Relative permittivity is typically denoted as ε_r or K is defined as $\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}$ where ε is the absolute permittivity of the material and ε_0 is the vacuum permittivity with value $\varepsilon_0 = 8.85 \times 10^{-12}$

2.3.1 Dielectric contributions

Dielectric constant has three types of contributions namely electronics, ionic contribution, and Orientation contribution.

Electronic contribution

This contribution of the electrons under an applied field and it is related to the number of bonds per unit volume. So electronic contribution is directly proportional to the density of the material.

Ionic contribution

The ionic contribution is dependent on the type of the atoms (Si, H, C, N, I) present in the material.

Orientation contribution

Orientation contribution is related to the structure of the material.
if these three contributions are high for any dielectric material it means that dielectrically is good.

2.3.2 Dielectric properties

Each dielectric has three main properties-
1) Permittivity
2) Bandgap
3) Conduction band offset
Permittivity is an ability of how much electric field lines will pass through it. And the bandgap is related to the how much current will be passed through it. If bandgap of the material is high, then small current will be flowing, and if bandgap is narrow, then high current will be flowing.
There are some dielectric materials which act as insulator shown in Table:2.2

Table 2.2: Properties of dielectric materials

Insulator	**Bandgap(eV)**	**Relative permittivity**	**Conduction band offset**
SiO_2	9	3.9	3.15
Si_3N_4	5.3	7.9	2.4
HFO_2	4.5	22	1.5

Table 2.2 shows the values of bandgap, relative permittivity, and conduction band offset properties for the insulators SiO_2, Si_3N_4, HFO_2 [1]. It can be seen from Table 2.2, that the bandgap and relative permittivity for HFO_2 dielectric is high comparable to SiO_2, Si_3N_4, thus if HFO_2 used as dielectric then there will be a large flow of current and small electric field in the channel. Therefore, among three HFO_2 is best dielectric so it can be used as a gate oxide.

2.4 Simulation Methodology

The two-dimensional device simulations are carried out by Sentaurus TCAD [**?**] to estimate the perspective benefits of the conventional 4H-SiC MOSFETs. The current-voltage Characteristics for each electrode are calculated after every step of bias ramp through quasi-stationary manner.

2.5 Characteristics of conventional 4H-SiC MOSFET

Characteristic is nothing but the plot of current vs. voltage. There are two types of characteristics in MOSFETs. The first one is transfer characteristics, and another one is output characteristics. In this section, we have studied about the transfer characteristics and output characteristics of the 4H-SiC MOSFET with three types of dielectrics such as SiO_2, Si_3N_4 and HFO_2 and compare these characteristics. The simulation of three 4H-SiC MOSFETs done by using three different dielectrics used as gate oxides. These characteristics are following-

2.5.1 Transfer characteristics

transfer characteristic is a plot of drain current vs. gate voltage for various values of drain voltage.

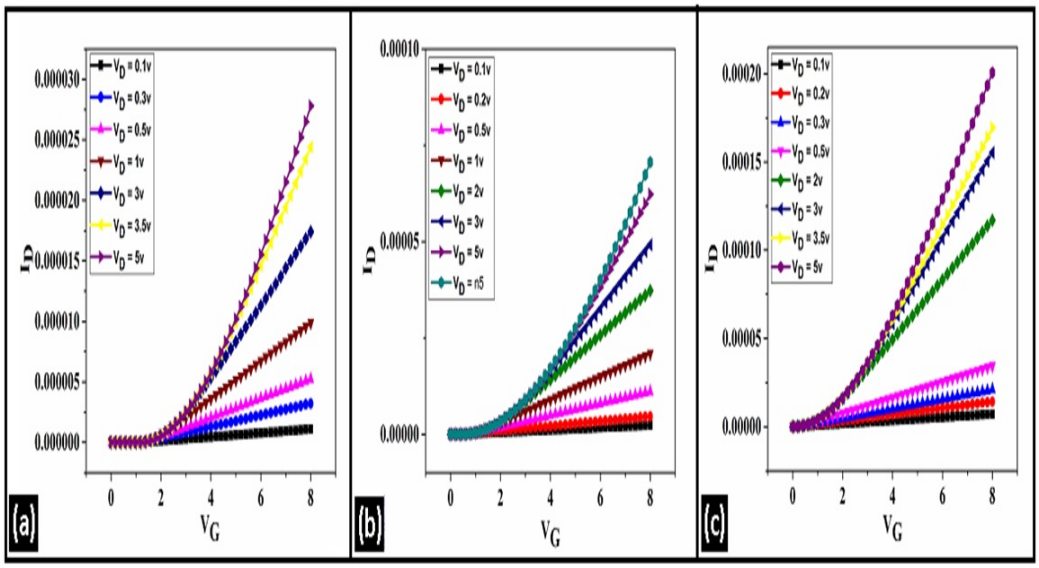


Figure 2.3: I_D Vs V_G characteristics at different V_D(a) SiO_2 (b) Si_3N_4 (c) HFO_2.

Figure 2.3 shows the I_D - V_G characteristics for the SiO_2, Si_3N_4 and HFO_2.

- Figure 2.3(a) shows the I_D vs. V_G characteristics for various value of V_D. Here we are taking SiO_2 as a gate oxide in 4H-SiC MOSFET. The drain voltage varies from 0.1 V to 5 V. Thus, for each value of V_D we get different values of drain current. In this plot at $V_D = 0.1V$ there is a negligible flow of drain current, at $V_D = 3V$ the value of drain current is $0.0018mA$, and for $V_D = 5V$ drain current is approximate $0.030mA$. Therefore, if the value of drain voltages increases then the value drain current is also increasing.
- Figure 2.3(b) shows the I_D vs. V_G characteristics for various value of V_D. Here we are taking Si_3N_4 as a gate oxide in 4H-SiC MOSFET. The drain

voltage varies from 0.1 V to 5 V. Thus for each value of V_D we get different values of drain current. In this plot at $V_D = 0.1V$ there is a negligible flow of drain current, at $V_D = 3V$ the value of drain current is $0.05mA$, and for $V_D = 5V$ the value of drain current is approximate $0.080mA$. Therefore, if the value of drain voltages increases then the value drain current is also increasing. Thus, Si_3N_4 dielectric material is better than SiO_2 to improve the performance of the 4H-SiC MOSFET in term of drain current.

- Figure 2.3(c) shows the I_D vs. V_G characteristics for various value of V_D. Here we are taking HFO_2 as a gate oxide in 4H-SiC MOSFET. The drain voltage varies from 0.1 V to 5 V. Thus for each value of V_D we get different values of drain current. In this plot at $V_D = 0.1V$ there is a negligible flow of drain current, at $V_D = 3V$ the value of drain current is $0.15mA$, and for $V_D = 5V$ the value of drain current is approximate $0.20mA$. Thus, HFO_2 dielectric material is better than other two SiO_2 and Si_3N_4 to enhance the performance of the 4H-SiC MOSFET in term of drain current.

2.5.2 Output characteristics

Output characteristics is a plot of drain current vs. drain voltage for various values of gate voltages. Figure 2.4 shows the I_D - V_D characteristics for the SiO_2, Si_3N_4

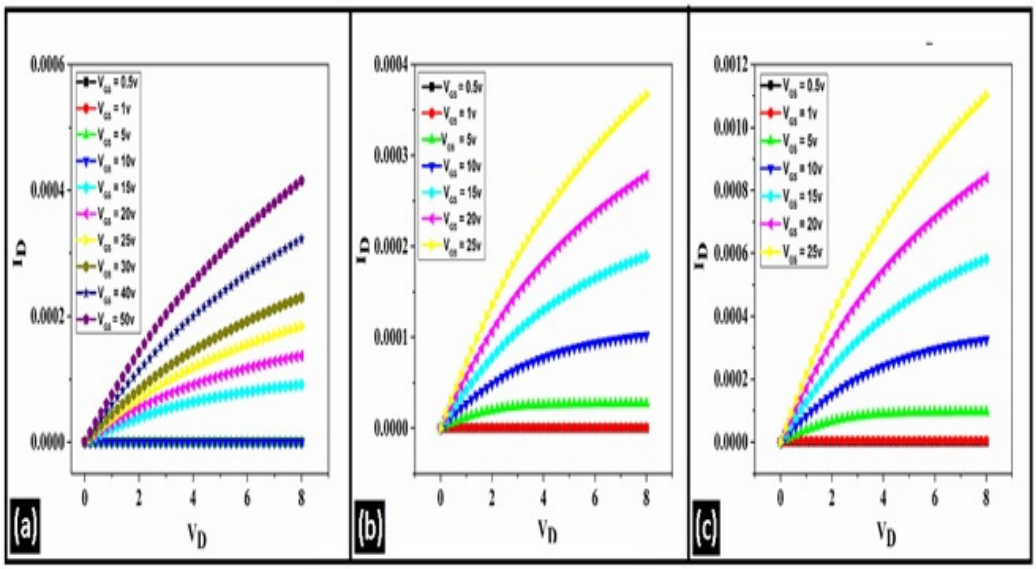


Figure 2.4: I_D Vs V_D characteristics at different V_{GS} (a) SiO_2 (b) Si_3N_4 (c) HFO_2.

and HFO_2 dielectric materials taken as gate oxides.

- Figure 2.4(a) shows the I_D vs. V_D characteristics for various value of V_{GS}. Here we are taking SiO_2 as a gate oxide in 4H-SiC MOSFET. The gate voltage varies from 0.5 V to 50 V. Thus for each value of V_{GS} we get

different values of drain current. In this plot up to $V_{GS} = 10V$ there are negligible drain current flows, and after $V_{GS} = 10V$ the value of drain current increasing. And at $V_{GS} = 25V$ drain current is approximate $0.2mA$. And for $V_{GS} = 25V$ drain current is increased to $0.4mA$.

- Figure 2.4(b) shows the I_D vs. V_D characteristics for various value of V_{GS}. Here we are taking Si_3N_4 as a gate oxide in 4H-SiC MOSFET. The gate voltage varies from 0.5 V to 25 V. Thus for each value of V_{GS} we get different values of drain current. In this plot up to $V_{GS} = 3V$ there is negligible drain current flows, and after $V_{GS} = 3V$ the value of drain current increasing. And at $V_{GS} = 25V$ drain current is approximate $0.4mA$. Therefore, compare to SiO_2, at $V_{GS} = 25V$ two times current flows in the 4H-SiC MOSFET by using Si_3N_4 dielectric material.

- Figure 2.4(c) shows the I_D vs. V_D characteristics for various value of V_{GS}. Here we are taking HFO_2 as a gate oxide in 4H-SiC MOSFET. The gate voltage varies from 0.5 V to 25 V. Thus, for each value of V_{GS} we get different values of drain current. In this plot up to $V_{GS} = 2V$ there is negligible drain current flows, and after $V_{GS} = 2V$ the value of drain current increasing. And at $V_{GS} = 25V$ drain current is approximate $1.1mA$. Therefore, compare to SiO_2 and Si_3N_4, HFO_2 provides better output characteristics in 4H-SiC MOSFET.

2.6 Threshold voltage instability in 4H-SiC MOSFET

Threshold voltage instability in 4H-SiC MOSFETs is due to the presence of many types of trap charges at the interface of Semiconductor/gate oxide interface [18]. There is always some charges located in the gate oxide layer and some charges at the semiconductor/oxide interface. Due to the presence of these charge in the gate oxide, there will require a shift in the gate voltage to reach the threshold voltage condition. So it is a big problem in 4H-SiC MOSFET devices. In this section, We will prove that there is instability in threshold voltage for various types of dielectrics.

Figure 2.5, 2.6 and 2.7 shows the threshold voltage instability in the 4H-SiC MOSFET with different dielectric, here we discussed three dielectrics SiO_2, Si_3N_4, and HFO_2. Threshold voltage shift investigated using V_{th} Vs V_{GS} characteristics evaluated for various gate voltage series at room temperature. Among these three, HFO_2 has least threshold voltage instability for V_D= 0.1V and 2.0 V. Here voltage instability is discussed for only forward sweep voltage. So for forward sweep voltage

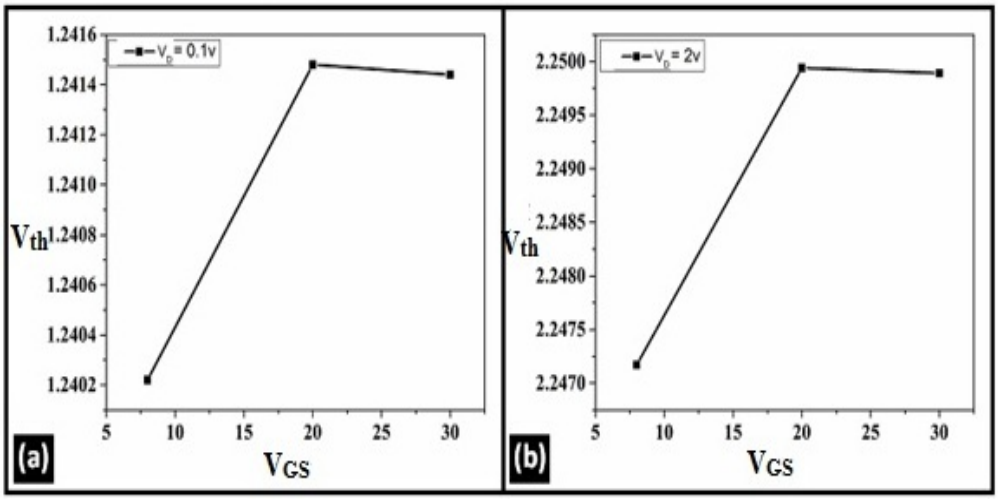


Figure 2.5: V_{th} Vs V_{GS} characteristics for SiO_2 dielectric (a) plot for $V_D = 0.1V$ (b) plot for $V_D = 2V$.

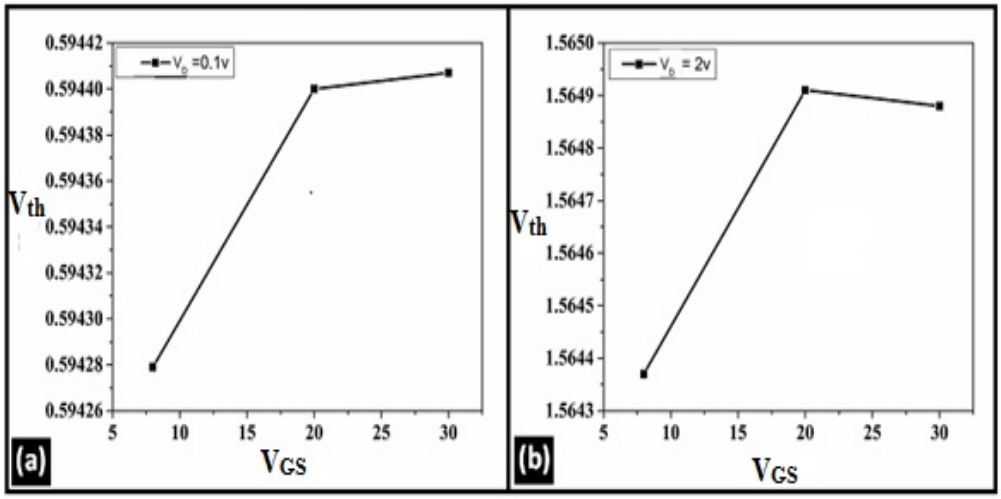


Figure 2.6: V_{th} Vs V_{GS} characteristics for Si_3N_4 dielectric (a) plot for $V_D = 0.1V$ (b) plot for $V_D = 2V$.

there is not much variation in the threshold voltage while using HFO_2 dielectric material as a gate oxide in 4H-SiC MOSFET.

2.7 Solution for threshold voltage instability in 4H-SiC MOSFET

Chlorine oxidation

It uses the small quantity of chlorine. This chlorine may be in the form of Cl_2 gas or it can be in the form of HCl, but science both these are potential material to deal with trichloroethylene (TCE).

Oxidation of silicon is taking place at the interface because the oxidation species are moving inside as the oxidation process goes on the oxidizing species move

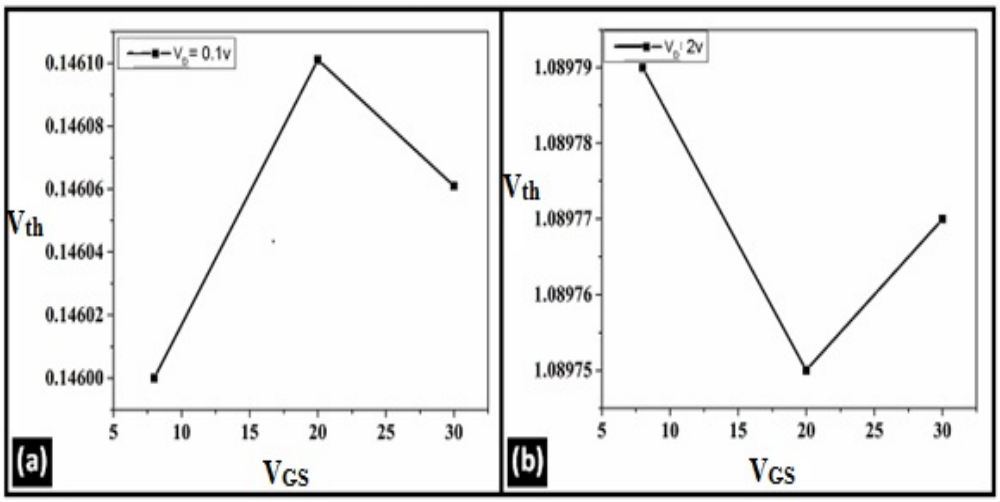


Figure 2.7: V_{th} Vs V_{GS} characteristics for HFO_2 dielectric (a) plot for $V_D = 0.1V$ (b) plot for $V_D = 2V$.

inside and the oxide is formed. Therefore, the oxidation reaction takes place at the interface. There are many Si-Si bonds it is part of silicon crystal lattice. Now the Si-Si bond breaks and new bonds are forming between silicon and oxygen. Therefore, these silicon atoms can move into the interstitial side, so after oxidation, it is found that there is a large number of silicon interstitial. There are some defects in the bar of silicon crystal. And these interstitial atoms move on to the defects and act as the nucleation side for the formation.

Now, chlorine oxidation can help in a very interesting way. The presence of chlorine in the oxidation ambient is going to create a lot of silicon vacancies at the surface. So these interstitial moves towards the defects side and preserve the silicon crystal So it is found that small quantity of chlorine during oxidation, helps not only in fixing the mobile ions but also reduces the oxidation induced stacking. Chlorine oxidation is also important to improve the lifetime of carriers.

2.8 Summary

This chapter reveals the concept of conventional 4H-SiC MOSFET and its unique advantages over conventional Silicon MOSFETs. This chapter illustrates the impact of considering three different dielectric material as a gate oxide in 4H-SiC MOSFETs platform. Nonetheless, the proposed device architecture shows an improvement in I_D, and around instability of threshold voltage in 4H-SiC MOSFET. We have performed and evaluated the characteristics of 4H-SiC MOSFET for three types of dielectric materials at room temperature. From the conferred results, the existence of the characteristics has been identified, which will help to enhance the performance of the device. Finally, the proposed one will show excellent performance regarding I_D and the threshold

voltage instability.

Chapter 3

Analytical Model of 4H-SiC MOSFET in Nanoscale

3.1 Introduction

THe continuously shrinkage of the device [26] may require for attaining excessive packing density and higher efficiency. However, the devaluation of the device dimensions in all forms decreases the performance that rising high short channel effects. Compressing the bulk MOSFET into nanometer MOSFET, compelling challenges and difficulties came ahead as the control of short channel effects. The controllability of the gate terminal on channel region reduces due to the short channel effects which lead to increases in the drain current and decrement of the sub-threshold slope. The use of shallow source-drain junction and thin layer of gate oxide are the simple solutions of preventing SCEs.
The short channel effects occur when the channel length is decreased in the same order as the depth of the channel [3]. When the length of the channel decreases, then the threshold voltage drops because the controllability of gate terminal on the channel region reduced due to the sharing of charges increased from source-drain junction [25]. According to our knowledge of concern, till now there is not any compress analytical model on hand within the literature for the threshold voltage and surface potential of nanoscale 4H-SiC MOSFET. The model presents the threshold voltage and surface potential of nanoscale 4H-SiC MOSFET using the 2-D Poisson equation [27]. The two-dimensional Poisson equation may be solved by using four boundary condition in silicon carbide region. And analyze the behavior of threshold voltage, surface potential, and electric field with varying device parameters like gate oxide thickness (tox), 4H-SiC thin layer thickness (t_{4H-SiC}), the channel length (L), and body doping (N_A). The intention is to study a physics-centered two-dimensional model for a 4H-SiC MOSFET with the aid of solving the 2-D Poisson equation. Established on results, now we have noticeable that this model can be utilized as a useful tool for the characterization and design of high-efficiency 4H-SiC nanoscale MOSFETs together with the short channel results by varying various physical parameters. The validity of the model checked with the aid of matching the model results with the two-dimensional simulation outcomes gathered utilizing T-CAD.

3.2 Short channel effects

Short channel effects (SCEs) can also be explained with the drain induced barrier lowering (DIBL) [28]. Threshold voltage drop falls when the channel length decreases. Hence, the effect on threshold voltage due to the channel length is called Short channel effect. SCE is also depended on the thickness of thin film, doping concentration, substrate biasing metal gate work function and

processing technology [28]. The main types of short channel effects are following-

3.2.1 Drain-induced-barrier-lowering

For long channel devices (means $L >> d_{max}$) the gate is completely responsible for depleting the semiconductor but in very short channel devices, part of the depletion region also dependent on the source and drain bias voltage. Science low gate voltage is required to depleted the semiconductor, threshold voltage reduced as channel length decreases. Similarly, if drain voltage increases then the depletion region of the semiconductor more increases by drain bias and hence, threshold voltage reduced.

If the channel length becomes too short, the depletion region from the drain can reach the source side and lowered the barrier for electron injection: this is known as punch through. DIBl results in an increase in the drain current at a given gate voltage [29]. Therefore, the threshold voltage decreases as channel length decreases.

3.2.2 Velocity saturation

The phenomenon of velocity saturation is associated with drift currents And as such it will be discussed in the context of strong inversion where such currents are dominant [17]. Let E_x be the value of the longitudinal component of the electric field in the semiconductor. That is the component parallel to the semiconductor-insulator interface. We have assumed that at all points in the inversion layer E_x is small enough so that the magnitude of the carrier velocity V_d is proportional to E_x.

$$E = \frac{V_d}{\mu} \tag{3.1}$$

The velocity of the carriers in the inversion layer tends to saturate at high E_x values. Effects due to the lack of proportionality between V_d and E_x on device characteristics are known as velocity saturation effects [17].

3.2.3 Hot carrier effect

The presence of a high electric field in the channel region, electrons with high energy moves towards the gate oxide. These hot electrons inside the oxide and semiconductor/oxide interface are called trap charges. Hence, the transfer of electrons from channel to oxide layer is known as hot carrier effect [24]. These trap charges change the threshold voltage of the device. Hot electron effect [13] can be reduced by reducing the electric field.it can also be reduced by reducing source and drain doping concentrations So that the junction fields are smaller.

3.2.4 Impact ionization

When there is a high electric field in the channel region of the MOSFET, then electrons gains higher energy and with higher velocity they impacted SiC atoms and ionized them. Then electron-hole pairs can generate. Due to this phenomenon [30] the electrons with high electric field moves towards the substrate, while trying to depart from the drain. Hence, It can also affect the other devices on the chip.

3.3 Two-dimensional structure of nanoscale 4H-SiC MOSFET

The structure of 4H-SiC MOSFET is shown in Figure 3.1 When compared to silicon MOSFET; 4H-SiC MOSFET structure is especially helpful for device scaling. In this structure a 4H-SiC epilayer grown on a silicon substrate.

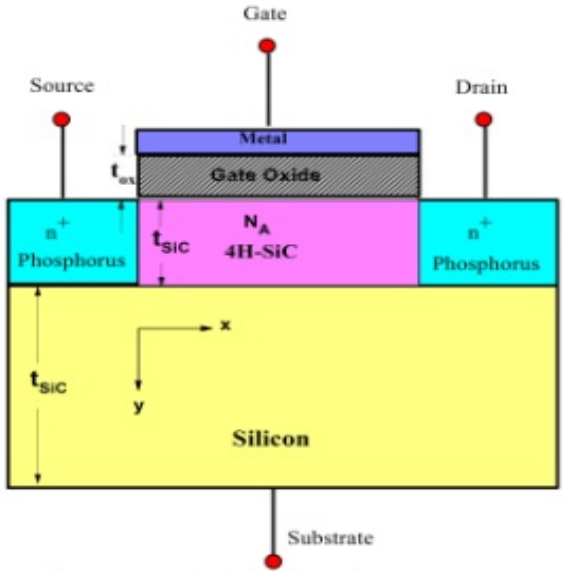


Figure 3.1: Cross-sectional view of nanoscale 4H-SiC MOSFET.

The epilayer has doped with the boron concentration of $1 \times (10^{17})\ cm^{-3}$ [25]. The phosphorus concentration of $2 \times (10^{20})\ cm^{-3}$ [25] is used for source and drain region doping. Silicon dioxide layer is maintained between the gate metal and the 4H-SiC layer, and the thickness of gate oxide layer is tox. All the device design parameters with specific values are tabulated in Table 3.1. The compact model will be used for the characterization and design of high-efficiency nanoscale 4H-SiC MOSFETs.

3.4 Methodology

The model for surface potential is solved by using two-dimensional Poisson equation. There are four boundaries condition [31] used to solve the Poisson

Table 3.1: Parameters considered for simulation of nanoscale 4H-SiC MOSFET

Symbol	Confession	Numeric Value
L	Channel length	100 nm
$E_{g,SiC}$	Energy band gap of SiC	3.25 eV
K	Boltzmann constant	1.38×10^{-23}
V_T	The thermal voltage	0.026 mV
$E_{g,Si}$	Band gap in Silicon	1.1 eV
ϕ_M	Metal gate work function	4.35 eV
q	Electron charge	$1.6 \times 10^{-19}\ cm^{-3}$
N_A	Channel doping concentration	$1 \times (10^{17})\ cm^{-3}$
N	Source and Drain doping	$2 \times (10^{20})\ cm^{-3}$
N_b	Substrate concentration	$1 \times (10^{15})\ cm^{-3}$
n_{Si}	Intrinsic concentration in Silicon	$1.45 \times (10^{10})\ cm^{-3}$
ε_{Si}	Dielectric material constant of silicon	11.7
ε_{SiC}	Dielectric constant of SiC	9.7
t_{Si}	Silicon film thickness	100 nm
t_{SiC}	SiC thin film thickness	30 nm
$\phi_s(X)$	surface potential in thin film	unknown
ε_{ox}	Gate oxide dielectric constant	20
t_{ox}	Thickness of gate oxide layer	5 nm
V_{GS}	Gate to source voltage	0.1 V
V_{sub}	The substrate bias	0.0 V
T	Temperature in Kelvin	300 K

equation. Then threshold voltage model is obtained by using maximal-minima theorem. And the model for an electrical field is solved by using differentiation properties. Extensive 2-D simulations are carried out by Sentaurus TCAD [32] [33] [34] to match the results came from the analytical modeling. Thus, the validity of the model is proven by matching the results came from analytical modeling and 2D simulation.

3.5 Surface Potential Model

Before access of inversion, the two-dimensional Poisson equation in the SiC film of a 4H-SiC MOSFET, appearance in Figure 3.1, may also be written as follows [35] [25]

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = \frac{qN_A}{\varepsilon_{SiC}}, for 0 \leqslant x \leqslant L, and 0 \leqslant y \leqslant t_{SiC} \tag{3.2}$$

The surface potential profile in the SiC film will also be approximated by a parabolic function, as carried out in [35] [25]

$$\phi\left(x,y\right) = \phi_S\left(x\right) + b_1\left(x\right)y + b_2\left(x\right)y^2 \tag{3.3}$$

Where $b_1(x)$ and $b_2(x)$ are the coefficients, and are functions of variable x. Equation (3.2) may be calculated by using the following boundary conditions-
I. At the source side the surface potential is

$$\phi(0,0) = \phi_s(0) = V_{bi,SiC} \tag{3.4}$$

$$V_{bi,SiC} = \frac{E_{g,SiC}}{2q} + \phi_{F,SiC} \tag{3.5}$$

Where $\phi_{_{F,SiC}}$ is the Fermi potential in SiC.
II. At the drain side the surface potential is

$$\phi(L,0) = \phi_s(L) = V_{bi,SiC} + V_{DS} \tag{3.6}$$

III. Electric field at the interface of gate oxide and SiC film is continuous, i.e.,

$$\left[\frac{d\phi(x,y)}{dy}\right]_{y=0} = \frac{\in_{ox}}{\in_{SiC}}\left(\frac{\phi_s(x) - \mathrm{V}_{GS}}{t_{ox}}\right) \tag{3.7}$$

IV. Electric field at the interface of SiC and the Silicon substrate is

$$\left[\frac{d\phi(x,y)}{dy}\right]_{y=t_{SiC}} = \frac{\in_{Si}}{\in_{SiC}}\left(\frac{V_{sub} - \phi(x,t_{SiC})}{t_{Si}}\right) \tag{3.8}$$

By using the boundary conditions (III) and (IV), we can obtain the coefficients $b_1(x)$ and $b_2(x)$. And then by placing these coefficients in to the expression for $\phi(x,y)$ and setting $y = 0$, we obtain

$$\frac{d^2\phi_S\left(x\right)}{dx^2} - \alpha\phi_S\left(x\right) = \beta \tag{3.9}$$

Where,

$$\alpha = \frac{2\left(1 + \frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{SiC}}\right)}{t_{SiC}^2\left(1 + 2\frac{C_{SiC}}{C_{Si}}\right)} \tag{3.10}$$

$$\beta = \frac{q \times N_A}{\varepsilon_{SiC}} - \frac{2 \times V_{GS}\left(\frac{C_{ox}}{C_{Si}} + \frac{C_{ox}}{C_{SiC}}\right)}{t_{SiC}^2\left(1 + 2\frac{C_{SiC}}{C_{Si}}\right)} - \frac{2 \times V_{svb}}{t_{SiC}^2\left(1 + 2\frac{C_{SiC}}{C_{Si}}\right)} \tag{3.11}$$

Where C_{ox}, C_{Si} and C_{SiC} are the capacitances per unit area for gate oxide layer, silicon layer and 4H-SiC film respectively.

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$, and $C_{SiC} = \frac{\varepsilon_{SiC}}{t_{SiC}}$
Solving equation (3.10) with boundary conditions

$$\phi_s(o) = \phi_{bi,SiC} \tag{3.12}$$

$$\phi_s(L) = \phi_{bi,SiC} + V_{DS} \tag{3.13}$$

Let $\lambda = \sqrt{\alpha}$ and $\sigma = \frac{\beta}{\alpha}$
The solution of equation (3.9) which is a second order non homogeneous differential equation with constant coefficient.

$$\phi_S(x) = Ae^{\lambda x} + Be^{-\lambda x} - \sigma \tag{3.14}$$

$$A = \left\{ \frac{(V_{bi,SiC} + \sigma + V_{DS}) - (V_{bi,SiC} + \sigma)e^{-\lambda L}}{1 - e^{-2\lambda L}} \right\} \times e^{-\lambda L} \tag{3.15}$$

$$B = \left\{ \frac{(V_{bi,SiC} + \sigma) - (V_{bi,SiC} + \sigma + V_{DS})e^{-\lambda L}}{1 - e^{-2\lambda L}} \right\} \tag{3.16}$$

3.6 Electric Field Model

We know that the rate of change of potential is called electric field, so by differentiating eq. (3.14) we can get the electric field.

$$E = \frac{d\phi_s(x)}{dx} = A\lambda e^{\lambda x} - B\lambda e^{-\lambda x} \tag{3.17}$$

3.7 Threshold Voltage Model

Threshold voltage model can be obtained by taking the minima of the surface potential from equation (3.14) is given as-

$$\phi_S(x) = Ae^{\lambda x} + Be^{-\lambda x} - \sigma \tag{3.18}$$

For minima condition, substituting equation (3.18) equal to zero

$$\frac{d\phi_s(x)}{dx} = 0 \tag{3.19}$$

$$A\lambda \exp(\lambda x) - B\lambda \exp(-\lambda x) = 0$$

$$\lambda(A \exp(\lambda x) - B \exp(-\lambda x)) = 0$$

$$A \exp(\lambda x) = B \exp(-\lambda x)$$

$$\exp(2\lambda x) = \left({}^{B}/_{A}\right)$$

$$x = \frac{1}{2\lambda} \ln \left({}^{B}/_{A}\right) \tag{3.20}$$

x is positive; it means there is a minimum at

$$x = \frac{1}{2\lambda} \ln \left({}^{B}/_{A}\right)$$

Now place this value of x in equation (3.18)

$$\phi_{s,\min} = A\exp\left(\ln\left(\sqrt{B/A}\right)\right) + B\exp\left(-\ln\left(\sqrt{B/A}\right)\right) - \sigma$$
$$= A\left(\sqrt{B/A}\right) + B\left(\sqrt{A/B}\right) - \sigma$$

$$\phi_{S_{\min}} = 2\sqrt{AB} - \sigma \tag{3.21}$$

The V_{th} voltage is the minimum price of gate to source voltage (V_{GS}) at which a channel is brought about under the gate oxide at the floor of 4H-SiC MOSFET. Thus, in a 4H-SiC MOSFET, the V_{th} voltage is taken to be that value of (V_{GS}) for which the channel surface advantage is the same as the twice of the difference between the intrinsic and extrinsic Fermi level [36] i.e.

$$\phi_{S,\min} = 2\phi_{F,SiC}$$

where $\phi_{_{F,SiC}}$ is the difference between the intrinsic and the extrinsic Fermi level. For the 4H-SiC MOSFET, the situation for threshold voltage under the gate is adjusted.

$$\phi_{S,\min} = 2\phi_{F,SiC} = \phi_{th} \tag{3.22}$$

And ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density within the 4H-SiC device is equal as doping attention [37]. Thus, the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential is equal. Therefore, accordingly, we will be able to determine the value of threshold voltage with the aid of putting equation (3.21) into (3.22) and solving for V_{GS}. The threshold voltage can be calculated by substituting equation (18) in equation (3.22) and solving for equation (3.21) by putting the expressions of α, β, λ, σ, A, and B.

$$V_{th} = \frac{-K_2 + \sqrt{K_2^2 - 4K_1K_3}}{2K_1} \tag{3.23}$$

Where,

$$K_1 = b^2[4(N - N^2) - 1] \tag{3.24}$$

$$K_2 = b\left\{4\left(NV_{bi,SiC} + M - 2MN\right) - \phi_{th}\right\} + 2ab\left\{4\left(N - N^2\right) - 1\right\} \tag{3.25}$$

$$K_3 = a\left\{4\left(NV_{bi,SiC} + M - 2MN\right) - \phi_{th}\right\} - \phi_{th}^2 - 4\left(M^2 - MV_{bi,Si_C}\right) + a^2\left\{4\left(N - N^2\right) - 1\right\} \tag{3.26}$$

$$M = \left\{\frac{\left(1 - \exp\left(-\lambda L\right)\right)V_{bi,SiC} + V_{DS}}{2\sinh(\lambda L)}\right\} \tag{3.27}$$

$$N = \left\{\frac{1 - \exp\left(-\lambda L\right)}{2\sinh(\lambda L)}\right\} \tag{3.28}$$

$$a = \frac{1}{\alpha}\left[\begin{array}{l}\dfrac{qN_A}{\varepsilon_{SiC}} - \left\{\dfrac{C_{Si}}{t_{SiC}\varepsilon_{SiC}} + \dfrac{C_{Si}^2}{(2C_{SiC}+C_{Si})\,t_{SiC}\varepsilon_{SiC}}\right\}V_{sub} \\ + \left\{\dfrac{C_{Si}C_{ox}}{t_{SiC}\varepsilon_{SiC}\,(2C_{SiC}+C_{Si})} + \dfrac{C_{ox}}{t_{SiC}\varepsilon_{SiC}}\right\}\end{array}\right] \tag{3.29}$$

$$b = -\frac{1}{\alpha}\left[\frac{C_{Si}C_{ox}}{t_{SiC}\varepsilon_{SiC}\,(2C_{SiC}+C_{Si})} + \frac{C_{ox}}{t_{SiC}\varepsilon_{SiC}}\right] \tag{3.30}$$

Where K_1, K_2, K_3, M, N, a, and b are constants and the expressions are as mentioned above and L being the channel length of the device.

3.8 Results and Discussion

3.8.1 Surface Potential

To validate the suggested analytical model, the 2D device simulator T-CAD [34] is used for the simulation of the surface potential distribution within the SiC layer and the threshold voltage (V_{th}) variation and the results are compared with the analytical model.

Figure 3.2 shows the surface potential variation along the channel length for distinct values of drain voltages. It is understood from figure 3.2 that there is no powerful change in the potential at the source side and an infinitesimal change at the drain side. As a final result, (V_{DS}) has a slight effect on (I_D) after saturation and it is visible from the figure that there is a negligible shift within the factor of the minimum surface potential regardless of the applied drain bias voltage. For this reason, drain-induced barrier lowering is substantially reduced for the 4H-SiC comparable to silicon. The model results and the simulation results are correlated with each other to prove the accuracy of our suggested analytical model.

Figure 3.3 shows the surface potential variation along the channel for various values of oxide thickness. When the gate oxide thickness increased, the electric field decreased. Therefore, because the decrement of electric field impact ionization also reduced, the rate of the generation of Carriers were small. So, the controllability of the gate over the channel potential increases, and it is less prominent to SCEs. Therefore, oxide thickness cannot be scaled right down to very small values because the results of tunneling via the thin oxide and hot-carrier end up prominent.

Figure 3.4 shows the surface potential variation along the channel for various values of gate voltages. It may be observed from the figure that as the gate voltage increases, there is quite an increment in the height of the barrier at the source side and drain side. Therefore the surface potential increases in the

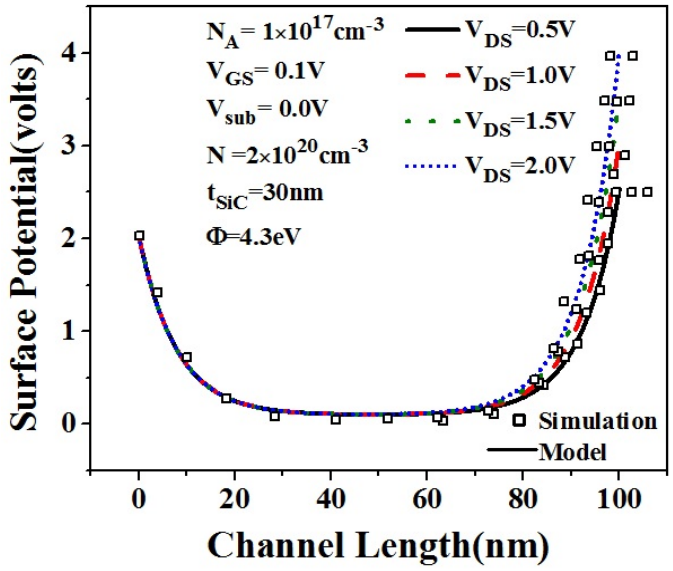


Figure 3.2: Graph for surface potential versus channel length for V_{DS} = 0.5 V, V_{DS} = 1.0 V, V_{DS} = 1.5 V and V_{DS} = 2.0 V. The device parameters are used as follows: V_{sub} = 0 V, V_{GS} = 0.1 V, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, t_{ox} = 5 nm, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

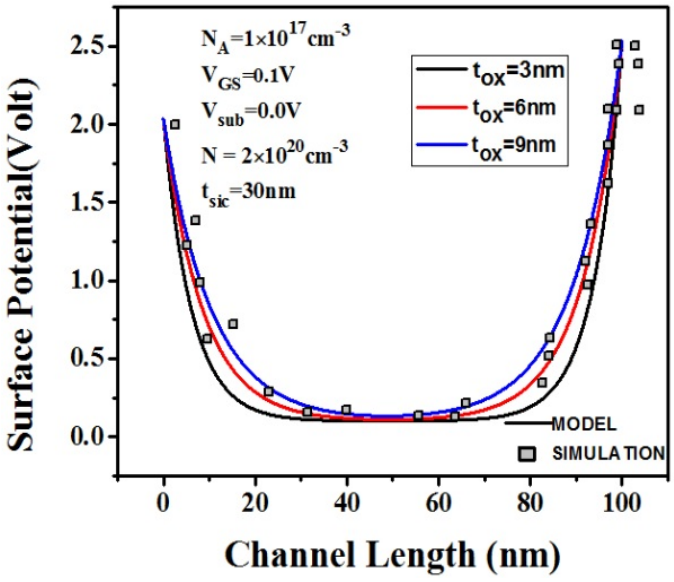


Figure 3.3: Graph for surface potential versus channel length for t_{ox} = 3 nm, t_{ox} = 6 nm, t_{ox} = 9 nm. The device parameters are used as follows: V_{sub} = 0 V, V_{GS} = 0.1 V, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, V_{DS} = 0.5 V, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

channel region. Consequently, DIBL decreases and the immunity to manage the SCEs is enhanced.

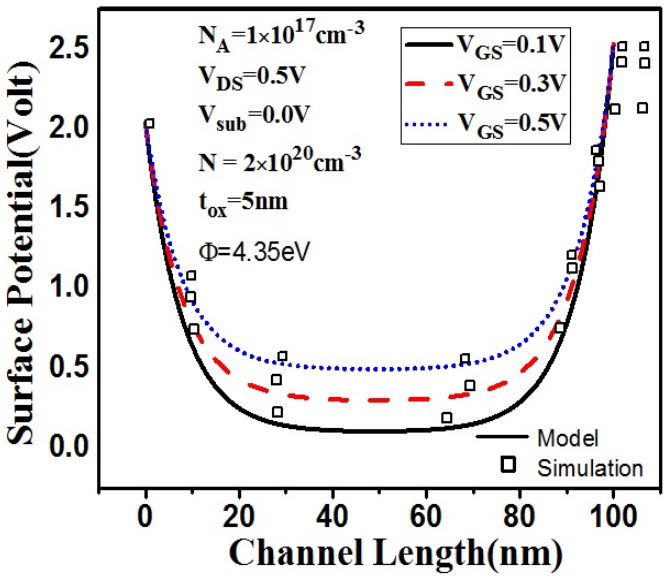


Figure 3.4: Graph for surface potential versus channel length for V_{GS} = 0.1 V, V_{GS} = 0.3 V,V_{GS} = 0.5 V The device parameters are used as follows: V_{sub} = 0 V, t_{ox} = 5 nm, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, V_{DS} = 0.5 V, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

3.8.2 Electric field

Figure 3.5 shows the electric field distribution variation along the channel for distinct values of gate oxide thickness. It may be observed from the figure that at the drain side, with an increase in the gate oxide value, the electric field substantially reduces. Hence, the reduction of the electric field experienced by the carriers in the channel may be understood because of the reduction of the hot-carrier effect.

3.8.3 Threshold voltage

Figure 3.6 shows the variation of the threshold voltage along the channel for distinct doping concentration. As proven within the figure, the threshold voltage increases with improved body doping concentration. Hence, the scaling of the device can go to a further extent without any further increase in SCEs by increasing the body doping concentration. The threshold voltage obtained from the model correlates very well with the simulation result.

Figure 3.7 shows the threshold voltage variation alongside the channel for distinct values of gate oxide thickness. When the gate oxide thickness is diminished, the threshold voltage can also be decreased which is the requirement for a faster device. Therefore, continuous scaling down of the gate oxide thickness offers a rise to faster devices. However, oxide thickness cannot be scaled all the way down to very small values because tunneling via the thin oxide

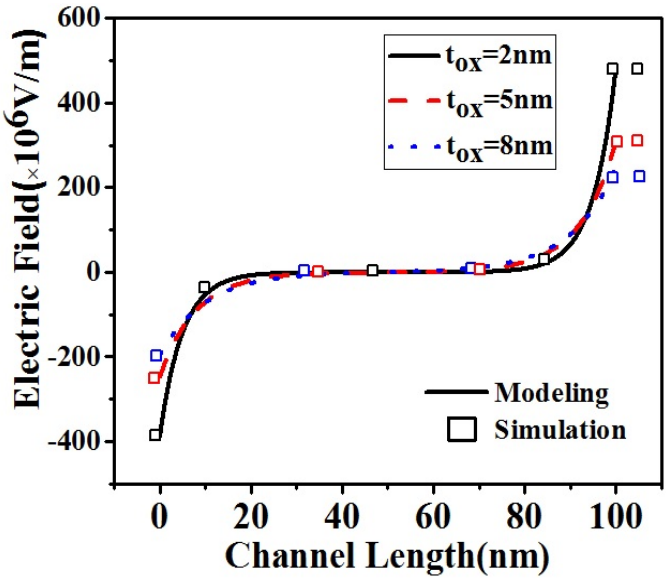


Figure 3.5: Graph for electric field versus channel length for t_{ox} = 2 nm, t_{ox} = 5 nm, t_{ox} = 8 nm. The device parameters are used as follows: V_{sub} = 0 V, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, V_{DS} = 0.5 V, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

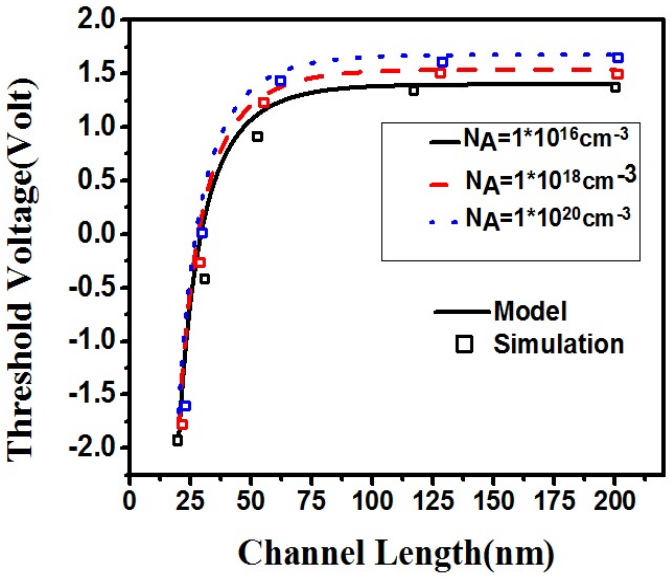


Figure 3.6: The graph for threshold voltage versus channel length for various values of NA. The device parameters are used as follows: V_{sub} = 0 V, t_{ox} = 5 nm, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, V_{DS} = 0.5 V, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

layer and hot carrier effects become prominent. It is clear that there is a close match between the analytical outcome and the 2D simulation outcome.

3.9 Summary

Analytical modeling of the electric field, surface potential and threshold voltage for a 4H-SiC MOSFET is developed based on the 2D physical model. The

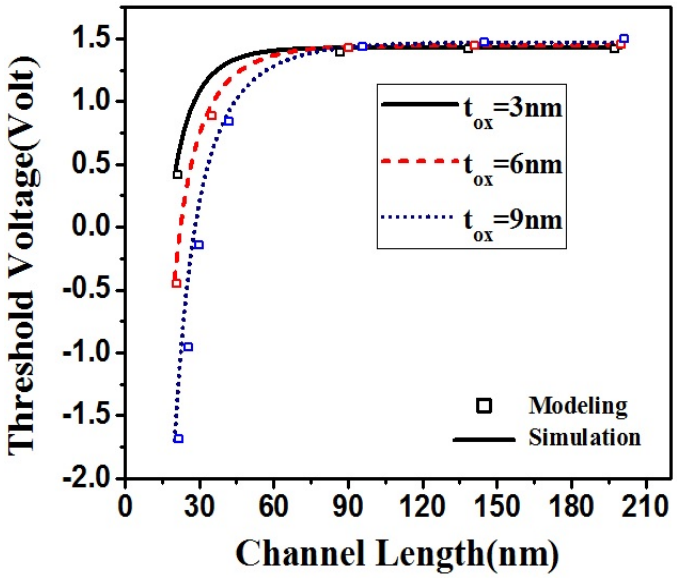


Figure 3.7: Graph for threshold voltage versus channel length for t_{ox} = 3 nm, t_{ox} = 6 nm, t_{ox} = 9 nm. The device parameters are used as follows: V_{sub} = 0 V, $N = 2 \times 10^{20}\ cm^{-3}$, t_{SiC} = 30 nm, V_{DS} = 0.5 V, t_{Si} = 100 nm and ϕ_M = 4.35 eV.

influence of quite a lot of device parameters likes gate length scaling, body doping, SiC thickness, gate oxide thickness on the electric field, the surface potential, and the threshold voltage are analyzed. The results envisioned by the model are compared with the 2D simulations performed by using a commercially available device simulator Sentaurus TM. There is a large drop in the threshold voltage with the decrease in channel length. The use of 4H-SiC material instead of silicon increases the device performance regarding reduced short channel effects. The compact model adequately predicts the threshold voltage over a huge variety of device parameters and can also be conveniently used to characterize and design the nanoscale 4HSiC MOSFETs with the desired performance

Chapter 4

Nanoscale SOI-4H-SiC MOSFETs Analytical Model

4.1 Introduction

This chapter is the modified version of Chapter 3 to improve the performance of 4H-SiC MOSFET in respect of short channel effects. This section includes the necessary building of silicon-on-insulator 4H-SiC MOSFET, 2D mathematical solution for threshold voltage, surface potential and field distribution in 4H-SiC MOSFET to reduce the short channel effects. Simulation of SOI-4H-SiC MOSFETs and then matched the outcomes obtained from the analytical modeling and outcome obtained from simulation to verify the validity of the model.

Silicon on insulator technology refers to a thin layer of 4H-SiC isolated from a silicon substrate by a relatively thick layer of SiO_2. SOI technology offers superior MOSFET devices with excellent radiation hardness and high device density. It provides very small leakage current in CMOS. SOI technology is more suitable for scaling down devices.

From many years silicon science is leading the IC market. However, primary problem of silicon is the consequences happening because of the devaluation of the dimensions. The regular scaling of the semiconductor device is required to attain high packing density and higher performance. The decline of the device dimensions in all features degrades the efficiency and the ensuing short channel effects (SCEs) heavily have an impact on the device. SOI engineering is brought into the picture has real suppressing SCEs when compared to bulk MOSFETs . At the same time scaling the bulk MOSFET into nanometer regime, tremendous challenges are observed just like highly sensitive towards SCEs. Consequently, more than a few new models with various engineering ideas had been suggested to shrink the SCEs in SOI platform [38].

Silicon -On-Insulator-4H-SiC is one of the best device structures to reduce the SCEs as compared to SOI-silicon structure. Drain-Induced-Barrier-Lowering (DIBL) can palpably define the SCEs, and it reduces the threshold voltage as channel length decreases. DIBL effects [28] present if barrier height of the surface potential at the source side reduces due to change of field at drain side when drain voltage increases. Therefore, some charge carriers injected into the channel increases which increases the drain off current. But in SOI devices, SCEs are also changed by body doping concentration, 4H-SiC thin film thickness, drain and gate biasing buried oxide layer thickness and metal gate work function. SOI-4H-SiC MOSFETs are engaging semiconductor devices for high-power, high-speed applications because of small parasitic capacitance. In this work, by using two-dimensional Poisson equation, the model for surface potential is solved using the boundary conditions for a SOI-4H-SiC MOSFET

The behavior of surface potential, threshold voltage, and electric field are systematically analyzed with varying device parameters like metal gate work function (ϕ_M), gate oxide thickness (t_{ox}), 4H-SiC thin layer thickness (t_{4H-SiC}), buried oxide thickness (t_b)), body doping (N_A) and supply voltages along the channel length. The intention is to study a physics based two-dimensional model for SOI-4H-SiC MOSFETs with the aid of solving the 2-D Poisson equation. The validity of the model checked with the aid of matching the model results with the 2-D simulation results gathered utilizing Sentaurus TCAD.

4.1.1 Two-Dimensional structure of SOI-4H-SiC MOSFET

The 2-D structure of SOI- 4H-SiC MOSFET is shown in Figure 4.1 When compared to silicon MOSFET and conventional 4H-SiC MOSFET; SOI-4H-SiC MOSFET device structure is much useful for device scaling down. This structure consists of one 4H-SiC thin film layer, silicon substrate layer and one buried oxide layer. 4H-SiC layer is grown on BOX layer. Boron concentration of $1 \times 10^{17}\ cm^{-3}$ [31] is used for doping of 4H-SiC epilayer. Source and drain regions are doped with the phosphorus concentration of $2 \times 10^{20}\ cm^{-3}$. Silicon semiconductor is used as substrate material. The thickness of silicon layer is 100nm. Silicon dioxide layer is placed between the gate metal and the 4H-SiC layer, and the thickness of gate oxide layer is tox. All the device design parameters with specific values are tabulated in Table 4.1. The compact model will be used for the characterization and design of high-efficiency nanoscale 4H-SiC MOSFET.

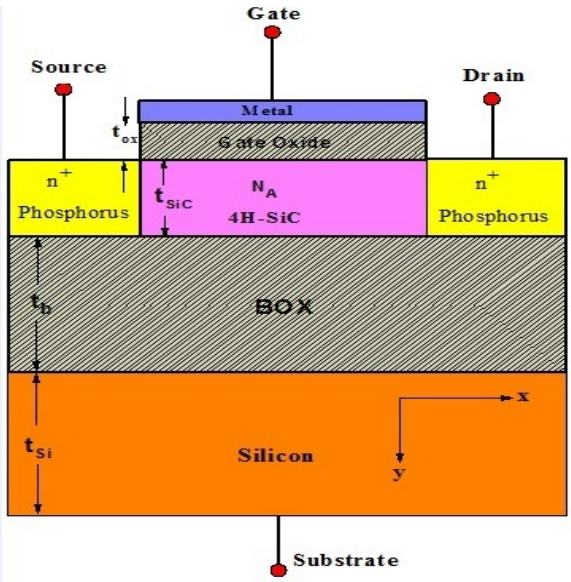


Figure 4.1: Cross-sectional view of nanoscale SOI-4H-SiC MOSFET.

Table 4.1: Parameters considered for simulation of nanoscale SOI-4H-SiC MOSFET

Symbol	**Confession**	**Numeric Value**
L	Channel length	100 nm
$E_{g,4H-SiC}$	Energy band gap of 4H-SiC	3.25 eV
K	Boltzmann constant	1.38×10^{-23}
V_T	The thermal voltage	0.026 mV
$E_{g,si}$	Band gap in Silicon	1.1 eV
ϕ_M	Metal gate work function	4.35 eV
X_{4H-SiC}	Electron affinity of Silicon carbide	3.1
q	Electron charge	$1.6 \times 10^{-19}\ cm^{-3}$
N_A	Channel doping concentration	$1 \times (10^{17})\ cm^{-3}$
N	Source and Drain doping	$2 \times (10^{20})\ cm^{-3}$
N_b	Substrate concentration	$1 \times (10^{15})\ cm^{-3}$
n_{4H-SiC}	Intrinsic concentration in 4H-SiC	$5 \times (10^{-9})\ cm^{-3}$
ε_{Si}	Dielectric material constant of silicon	11.7
ε_{4H-SiC}	Dielectric constant of 4H-SiC	9.7
t_{Si}	Silicon substrate thickness	100 nm
t_{4H-SiC}	4H-SiC thin film thickness	30 nm
t_b	BOX thickness	100 nm
t_{ox}	Thickness of gate oxide layer	5 nm
$\phi_s(X)$	surface potential in thin film	unknown
ε_{ox}	Gate oxide dielectric constant	20
V_{GS}	Gate to source voltage	0.1 V
V_{sub}	The substrate bias	0.0 V
T	Temperature in Kelvin	300 K

4.2 Methodology

The model for surface potential is solved by using two-dimensional Poisson equation. there are four boundaries condition used to solve the Poisson equation. then threshold voltage model is obtained by using maximal-minima theorem. And the model for electrical field is solved by using differentiation properties. Extensive 2-D simulations are carried out by Sentaurus TCAD [33] to match the results came from the analytical modeling. thus, the validity of the model is proven by matching the results came from from analytical modeling and 2D simulation.

4.3 Surface Potential Model

Before accomplishment of strong inversion, the 2-D Poisson equation in the Silicon carbide thin film of a 4H-SiC MOSFET, present in Figure 4.1, may also be written as follows [35]

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{4H-SiC}}, for 0\leqslant x\leqslant L, and 0\leqslant y\leqslant t_{4H-SiC} \tag{4.1}$$

In 4H-SiC thin film, the surface potential will be approximated by a parabolic function, as implement in,

$$\phi(x,y)=\phi_S(x)+q_1(x)\,y+q_2(x)\,y^2 \tag{4.2}$$

Where $q_1(x)$ and $q_2(x)$ are the coefficients, and are functions of variable x. there are four boundary conditions exist to solve the model for surface potential. Hence, by using these boundary conditions, equation (1) can be solved.

I. Surface potential at the source side

$$\phi(0,0)=\phi_s(0)=V_{bi,4H-SiC} \tag{4.3}$$

$$V_{bi,4H-SiC}=\frac{E_{g,4H-SiC}}{2q}+\phi_{F,4H-SiC}$$

Where $\phi_{F,4H-SiC}$ is the Fermi potential in 4H-SiC thin film.

$$\phi_{F,4H-SiC}=V_T\ln\left(\frac{N_A}{\eta_{i,4H-SiC}}\right)$$

Where $n_{i,4H-SiC}$ is intrinsic carrier concentration of 4H-SiC.

II. Surface potential at the drain side

$$\phi(L,0)=\phi_s(L)=V_{bi,4H-SiC}+V_{DS} \tag{4.4}$$

III. Electric field at the gate oxide/4H-SiC interface is continuous, i.e.

$$\left[\frac{d\phi(x,y)}{dy}\right]_{y=0}=\frac{\in_{ox}}{\in_{4H-SiC}}\left(\frac{\phi_s(x)-\mathrm{V}_{GS_1}}{t_{ox}}\right) \tag{4.5}$$

Where

$$\mathrm{V}_{GS1} = \mathrm{V}_{GS} - (\mathrm{V}_{FB,f})_{4H-SiC} \tag{4.6}$$

And,

$$(\mathrm{V}_{FB,f})_{4H-SiC} = \phi_M - \phi_{4H-SiC} \tag{4.7}$$

$$\phi_{4H-SiC} = \frac{\chi_{4H-SiC}}{q} + \frac{E_{g,4H-SiC}}{2q} + \phi_{F,4H-SiC} \tag{4.8}$$

Where ϕ_{4H-SiC} is work function of 4H-SiC.

IV. Electric field at BOX/4H-SiC interface is

$$\left[\frac{d\phi(x,y)}{dy}\right]_{y=t_{4H-SiC}} = \frac{\in_{ox}}{\in_{4H-SiC}}\left(\frac{V_{sub1} - \phi_b(x)}{t_b}\right) \tag{4.9}$$

Where,

$$\mathrm{V}_{sub1} = \mathrm{V}_{sub} - (\mathrm{V}_{FB,b})_{4H-SiC}$$

And

$$(\mathrm{V}_{FB,b})_{4H-SiC} = \phi_{sub} - \phi_{4H-SiC}$$

By solving equation (4.5) and (4.9) we can calculate the coefficients $q_1(x)$ and $q_2(x)$. And then putting the value of these coefficientâĂŹs in equation (4.1) and by placing y=0 we obtain

$$\frac{d^2\phi_S(x)}{dx^2} - \alpha\phi_S(x) = \beta \tag{4.10}$$

If we consider that the back channel oxide capacitance C_b is much smaller than the both front-channel capacitance C_{ox} and the 4H-SiC film capacitance C_{4H-SiC}. Then the values of α and β will be approximately

$$\alpha = \frac{2\left(1 + \frac{C_{ox}}{C_{4H-SiC}} + \frac{C_{ox}}{C_b}\right)}{t^2_{4H-SiC}\left(1 + 2\frac{C_{4H-SiC}}{C_b}\right)} \tag{4.11}$$

$$\alpha \approx \frac{\varepsilon_{ox}}{\varepsilon_{4H-SiC}} \times \frac{1}{t_{4H-SiC} \times t_{ox}} \tag{4.12}$$

And,

$$\beta = \frac{q \times N_A}{\varepsilon_{4H-SiC}} - \frac{2 \times V_{GS1}\left(\frac{C_{ox}}{C_{4H-SiC}} + \frac{C_{ox}}{C_b}\right)}{t^2_{4H-SiC}\left(1 + 2\frac{C_{4H-SiC}}{C_b}\right)} - \frac{2 \times V_{sub1}}{t^2_{4H-SiC}\left(1 + 2\frac{C_{4H-SiC}}{C_b}\right)} \tag{4.13}$$

$$\beta \approx \frac{q \times N_A}{\varepsilon_{4H-SiC}} - \frac{\varepsilon_{ox} \times V_{GS1}}{\varepsilon_{4H-SiC} \times t_{4H-SiC} \times t_{ox}} - \frac{\varepsilon_{ox} \times V_{sub1}}{\varepsilon_{4H-SiC} \times t_{4H-SiC} \times t_b} \tag{4.14}$$

Now we can solved the equation (4.10) by using the following boundary conditions-

$$\phi_s(0) = V_{bi,4H-SiC} \tag{4.15}$$

$$\phi_s(L) = V_{bi,4H-SiC} + V_{DS} \tag{4.16}$$

Let us consider

$$\gamma = \sqrt{\alpha}$$

And

$$\Gamma = \frac{\beta}{\alpha}$$

The solution of equation (4.10) is non-homogeneous differential equation of second order with constant coefficient.

$$\phi_S(x) = D_1 e^{\gamma x} + D_2 e^{-\gamma x} - \Gamma \tag{4.17}$$

Where,

$$D_1 = \left\{ \frac{(V_{bi,4H-SiC} + \Gamma + V_{DS}) - (V_{bi,4H-SiC} + \Gamma)e^{-\gamma L}}{1 - e^{-2\gamma L}} \right\} \times e^{-\gamma L} \tag{4.18}$$

And,

$$D_2 = \left\{ \frac{(V_{bi,4H-SiC} + \Gamma) - (V_{bi,4H-SiC} + \Gamma + V_{DS})e^{-\gamma L}}{1 - e^{-2\gamma L}} \right\} \tag{4.19}$$

Hence, equation (4.17) is the surface potential equation, so by simulating these equations in MATLAB Tool, we can get results for surface potential

4.4 Electric field model

Electric field is determined as the rate of change of potential i.e.

$$E = \frac{d\phi_s(x)}{dx} \tag{4.20}$$

And from equation (4.17),

$$\phi_S(x) = D_1 e^{\gamma x} + D_2 e^{-\gamma x} - \Gamma \tag{4.21}$$

So by taking differentiation of equation (4.17) we can get the electric field.

$$E = \frac{d\phi_s(x)}{dx} = D_1 \gamma e^{\gamma x} - D_2 \gamma e^{-\gamma x} \tag{4.22}$$

4.5 Threshold voltage model

The minimum value of the surface potential is called the threshold voltage. Hence, by taking minima of equation (4.17) we can get threshold voltage model equation.

$$\phi_S(x) = D_1 e^{\gamma x} + D_2 e^{-\gamma x} - \Gamma \tag{4.23}$$

To obtain minima of equation (4.23), we need to take differentiation of equation (4.23) and then put equal to zero.

$$\frac{d\phi_s(x)}{dx} = 0 \tag{4.24}$$

Then we get,

$$x = \frac{1}{2\gamma} \ln \left({}^{D_1}\!/_{D_2} \right) \tag{4.25}$$

The value of x is positive means there is a minima point at

$$x = \frac{1}{2\gamma} \ln \left({}^{D_1}\!/_{D_2} \right)$$

Now putting this value of x in equation (4.23) to obtain minimum surface potential

$$\begin{aligned}\phi_{s,\min}(x) = D_1 \exp\left(\ln\left(\sqrt{D_2/D_1}\right)\right) x + \\ D_2 \exp\left(-\ln\left(\sqrt{D_2/D_1}\right)\right) x - \Gamma\end{aligned} \tag{4.26}$$

$$\phi_{S_{\min}} = 2\sqrt{D_1 D_2} - \Gamma \tag{4.27}$$

Threshold voltage is the minimum value of gate to supply voltage at which a channel is set up through the gate oxide at the surface of SOI-4H-SIC MOSFET. Accordingly, in a SOI-4H-SiC MOSFET, the threshold voltage is taken to be that value of V_{GS} for which the surface potential is equal to the twice of the difference between the intrinsic and extrinsic Fermi level.

$$\phi_{S,\min} = 2\phi_{F,Si}$$

where $\phi_{F,4H-SiC}$ is the difference between the intrinsic and the extrinsic Fermi level.

$$\phi_{S,\min} = 2\phi_{F,4H-SiC} = \phi_{th} \tag{4.28}$$

And ϕ_{th} is the value of surface potential at which the inversion electron charge density in the SOI-4H-SiC device is equal to body doping concentration.
Hence, we will examine the value of threshold voltage through making use of placing equation (4.27) into (4.28) and solving for V_{GS}.

$$V_{th} = \frac{-K_2 + \sqrt{K_2^2 - 4K_1K_3}}{2K_1} \tag{4.29}$$

Where,

$$K_1 = b^2[4(N - N^2) - 1] \tag{4.30}$$

$$K_2 = b\left\{4\left(NV_{bi,4H-SiC} + M - 2MN\right) - 2\phi_{F,4H-SiC}\right\} + 2ab\left\{4\left(N - N^2\right) - 1\right\} \tag{4.31}$$

$$\begin{aligned}K_3 = a\left\{4\left(NV_{bi,4H-SiC} + M - 2MN\right) - 2\phi_{F,4H-SiC}\right\} \\ -\phi_{F,4H-SiC}^2 - 4\left(M^2 - MV_{bi,4H-Si_C}\right) + a^2\left\{4\left(N - N^2\right) - 1\right\}\end{aligned} \tag{4.32}$$

$$M = \frac{\left\{1 - \exp\left(-\gamma L\right) V_{bi,4H-SiC} + V_{DS}\right\}}{2\sinh\gamma L} \tag{4.33}$$

$$N = \frac{1 - \exp\left(-\gamma L\right)}{2\sinh\gamma L} \tag{4.34}$$

$$a = \frac{1}{\alpha}\left[\begin{array}{l} \frac{qN_A}{\varepsilon_{4H-SiC}} - \left\{\frac{C_b}{t_{4H-SiC}\varepsilon_{4H-SiC}} + \frac{C_b^2}{(2C_{4H-SiC}+C_b)t_{4H-SiC}\varepsilon_{4H-SiC}}\right\}V_{sub1}+ \\ \left\{\frac{C_bC_{ox}}{t_{4H-SiC}\varepsilon_{4H-SiC}(2C_{4H-SiC}+C_b)} + \frac{C_{ox}}{t_{4H-SiC}\varepsilon_{4H-SiC}}\right\}(\mathrm{V}_{FB,b})_{4H-SiC} \end{array}\right] \tag{4.35}$$

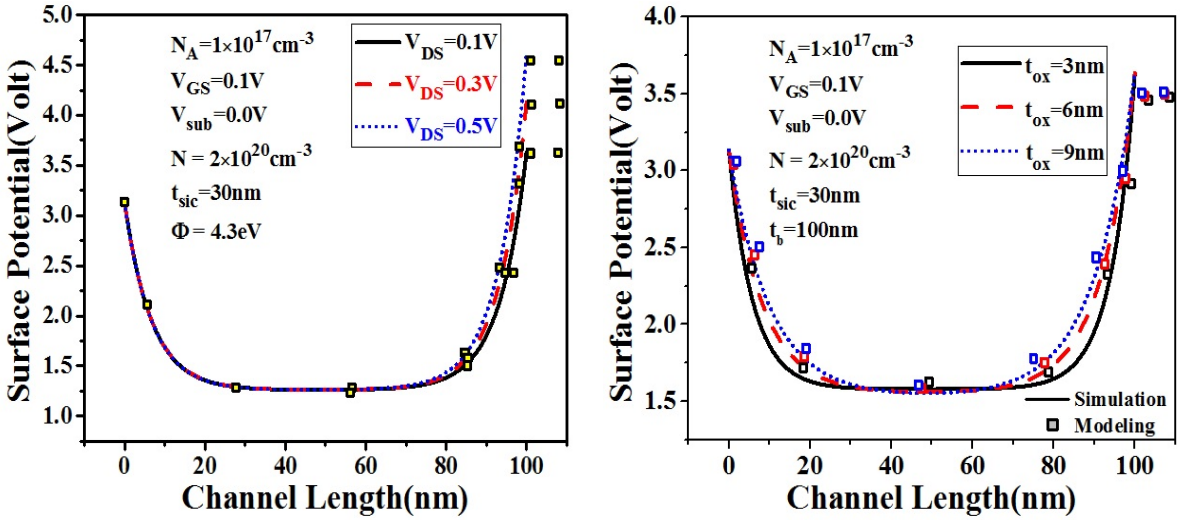
$$b = -\frac{1}{\alpha}\left[\frac{C_bC_{ox}}{t_{4H-SiC}\varepsilon_{4H-SiC}\left(2C_{4H-SiC}+C_b\right)} + \frac{C_{ox}}{t_{4H-SiC}\varepsilon_{4H-SiC}}\right] \tag{4.36}$$

4.6 Results and Discussion

4.6.1 Surface Potential

The surface potential model has been determined mathematically. Now to verify the proposed model results, the 2-D device simulator TCAD is used. TCAD tool is used to simulate the surface potential in the 4H-SiC layer, electric field distribution and the threshold voltage variations and the outcomes are correlated with the mathematical model done by MATLAB Tool.

Fig. 4.2(a) shows variations of surface potential towards the channel for drain



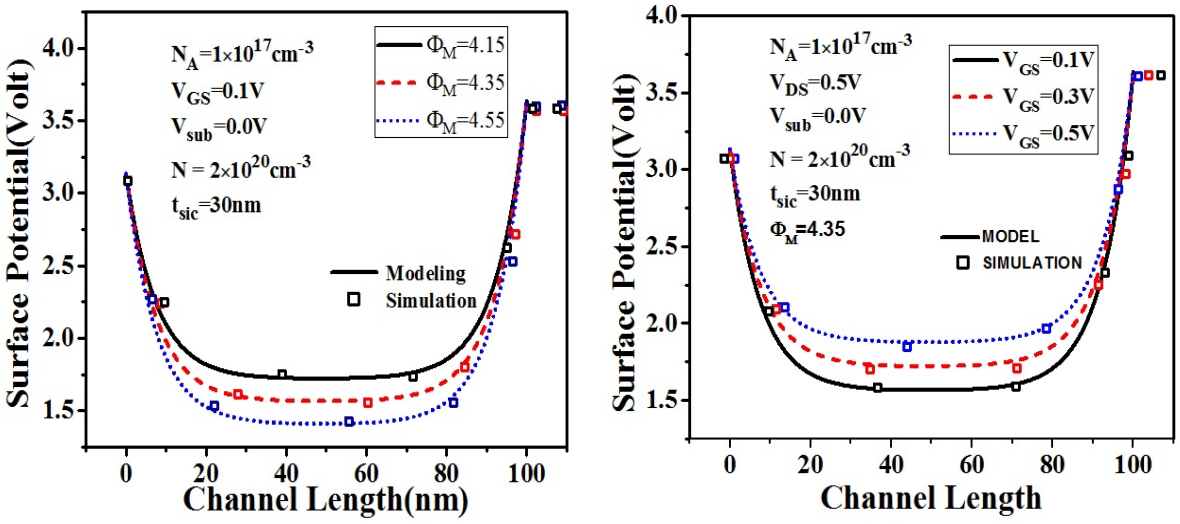
(a) (b)

Figure 4.2: Graph for surface potential vs. channel length for (a) $V_{DS} = 0.1$ V, $V_{DS} = 0.3$ V, and $V_{DS} = 0.5$ V. (b) $t_{ox} = 3$nm, $t_{ox} = 6$nm and $t_{ox} = 9$nm.

voltages $V_{DS} = 0.1$ V, $V_{DS} = 0.3$ V, and $V_{DS} = 0.5$ V. It is understood from Figure 2 that there is no more changes in the potential height at the source side and an infinitesimal shifts in the surface potential at the drain end. As a final result, V_{DS} has handiest a minuscule effect on I_D after saturation, and it's visible from the figure that there's a negligible shift within the factor of minimum surface potential regardless of the applied drain bias voltage. For this reason, the DIBL effect is substantially reduced for the SOI-4H-SiC comparable to

conventional 4H-SiC and silicon MOSFETs. For proving accuracy, simulation result and analytical modeling results have been mapped.
Figure 4.2(b) shows the surface potential variations onward the channel for three values of oxide thickness. There will be a decrement in the electric field with the increase in gate oxide thickness. Therefore due to the decrement of the electric field, impact ionization also reduced, means the rate of generation of carriers has been low. Thus, the controllability of the gate over the surface potential increases, and it is less dominant to SCEs. Consequently, Oxide thickness can't be scaled down to very small values when you consider that tunneling through the thin oxide and hot carrier outcome emerge as prominent.

Figure 4.3(a) shows the surface potential variations along the channel length for metal gate work function values of $\phi_M = 4.15$eV, $\phi_M = 4.35$eV, $\phi_M = 4.55$ev. As it can be noticeable from equation (4.7), if metal gate work function increases then front channel flat band voltage in 4H-SiC region also increases. Due to this from equation (4.6), $V_{GS,1}$ decreases, now we can see from the equation (4.5) surface potential depends on $V_{GS,1}$, therefore, surface potential increases in the channel region by increasing metal gate work function. Also, we can see from figure when work function value increases from 4.15eV to 4.55eV then there is an increment of surface potential in the channel region. Thus by choosing a higher value of gate metal work function leads to a greater manage of the surface potential.



(a) (b)

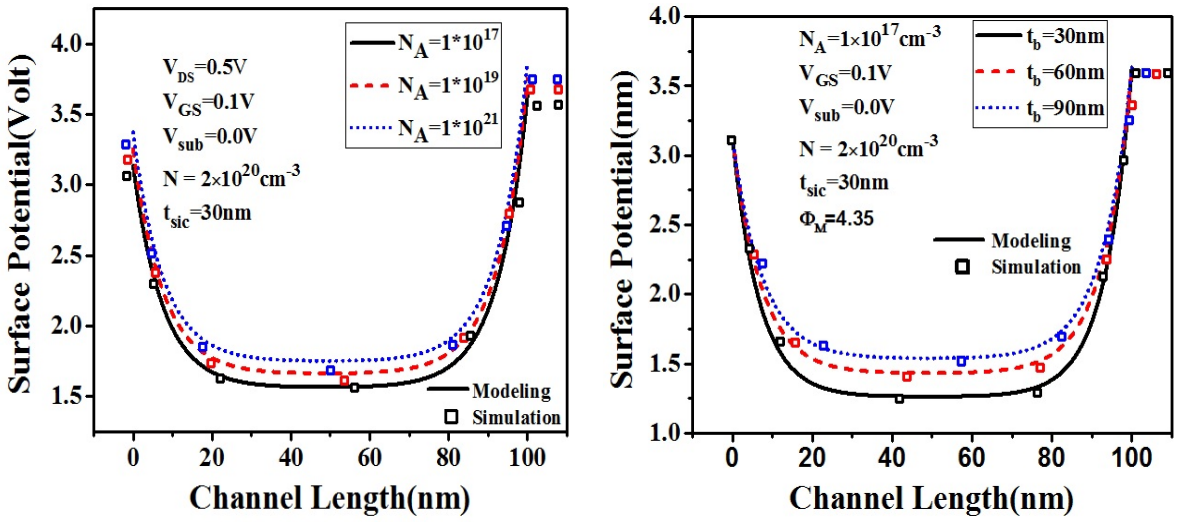
Figure 4.3: Graph for surface potential vs. channel length for (a)$\phi_M = 4.15$ eV, $\phi_M = 4.35$ eV, and $\phi_M = 4.55$ eV. (b) $V_{GS} = 0.1$ V, $V_{GS} = 0.3$ V, $V_{GS} = 0.5$ V.

Figure. 4.3(b) shows the surface potential variation onward the channel length for three values of gate voltage $V_{GS} = 0.1$V, 0.3V and 0.5V. It may be observed

from the figure that as the increases in the gate voltage, there is quite increment in the height of the barrier at the source end and drain end. The surface potential increases in the channel region. Thus, an increment of gate to source voltage will give better control on barrier height. Consequently, DIBL decreases and the immunity to manage the SCEs are multiplied.

Figure. 4.4(a) shows the surface potential variations towards the channel length for three values of channel doping concentration $N_A = 1 \times 10^{17}$, $N_A = 1 \times 10^{19}$ and for $N_A = 1 \times 10^{21}$. If doping concentration increases in the channel, then there is need of high gate voltage to control the device. As shown in figure, the surface potential increases at source and drain end when doping concentration increases from 1×10^{17} to 1×10^{21}. Thus chosen of high doping concentration will give the better results and reduce the SCEs in SOI-4H-SiC MOSFETs.

Figure. 4.4(b) shows the surface potential variations towards the channel length



(a) (b)

Figure 4.4: Graph for surface potential vs. channel length for (a)$N_A = 1 \times 10^{17}$, $N_A = 1 \times 10^{19}$, and $N_A = 1 \times 10^{21}$. (b) t_b = 30nm, 60nm,and 90nm.

for three values of buried oxide thickness t_b = 30nm, 60nm, and 90nm. From the figure, as the thickness of buried oxide increases from 30nm to 90nm the surface potential also increases in the channel region. But if the high value of tb is considered then there will be a decrement in the height of the potential barrier which will increase SCEs. Thus, we must choose a proper value of buried oxide thickness by which short channel effects could not increase.

Figure. 4.5 shows the surface potential variations towards the channel length for three values of 4H-SiC thickness t_{4H-SiC} = 20nm, 30nm, and 40nm. From equation (4.12), as the value of α decreases, the thickness of 4H-SiC film increases so the value of Γ increases, thus from equation (4.17) surface potential decreases

in the channel region. From figure 8, the value of surface potential decreases in the channel region with an increase in 4H-SiC film thickness. To verify the validity of the model, results from the analytical modeling have been correlated with simulation results.

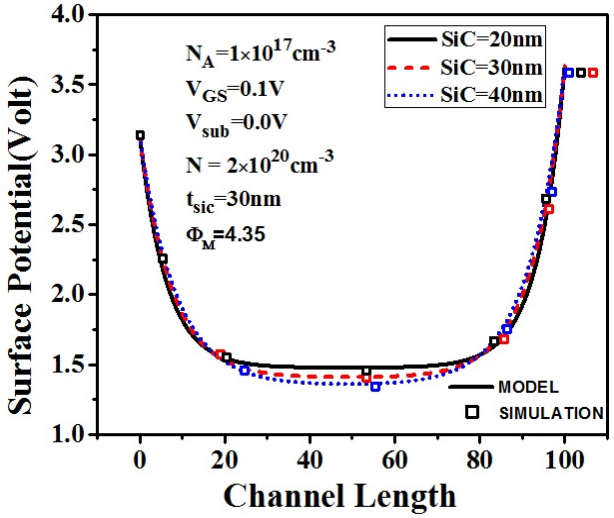


Figure 4.5: Graph for surface potential vs channel length for t_{4H-SiC} = 20nm, 30nm, and 40nm.

4.6.2 Electric Field

Figure. 4.6 shows the variations of electric field towards the channel length for three values of gate oxide thickness t_{ox} = 2nm, 5nm, and 8nm. It may be observed from the figure that at the drain end, with an increase in t_{ox} value, the electric field substantially reduces.

Because electric field depends on the permittivity of the dielectric material in the oxide layer. Thus, the high value of gate oxide thickness decreases the electric field. Hence, carriers experience low energy due to the reduction in the electric field. Therefore, Charge carriers could not cross the 4 H-SiC/SiO_2 interfaces, so there is the reduction in hot-carrier effect.

4.6.3 Threshold Voltage

Figure. 4.7(a) shows the variations of threshold voltage alongside the channel length for three values of gate oxide thickness t_{ox} = 3nm, 5nm, and 7nm. When the gate oxide thickness is decreased from 7nm to 3nm, then threshold voltage is improving comparable to 5nm and 7nm. Thus, continuous scaling in thickness of the gate oxide rise to faster device but, gate oxide thickness cannot be scaled right down to very small values because if thickness is very less then there will be very high field in the channel region then there will be tunneling via the thin oxide layer and then there will be hot-carrier effects. It is clear that there is a close matching

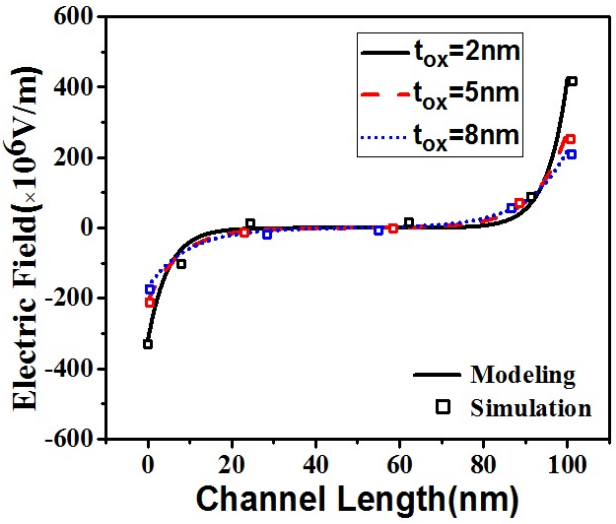
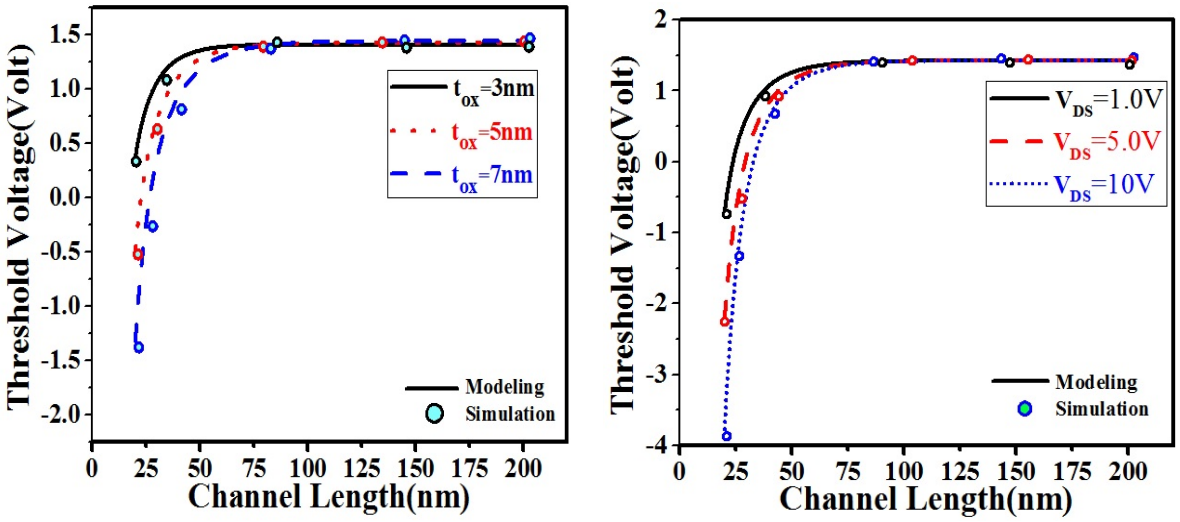


Figure 4.6: Graph for Electric field vs channel length for t_{ox} = 2nm, for t_{ox} = 5nm, for t_{ox} = 8nm.

between the analytical outcome and the two-dimensional simulation outcome.

Figure. 4.7(b) shows variations of the threshold voltage along the channel for



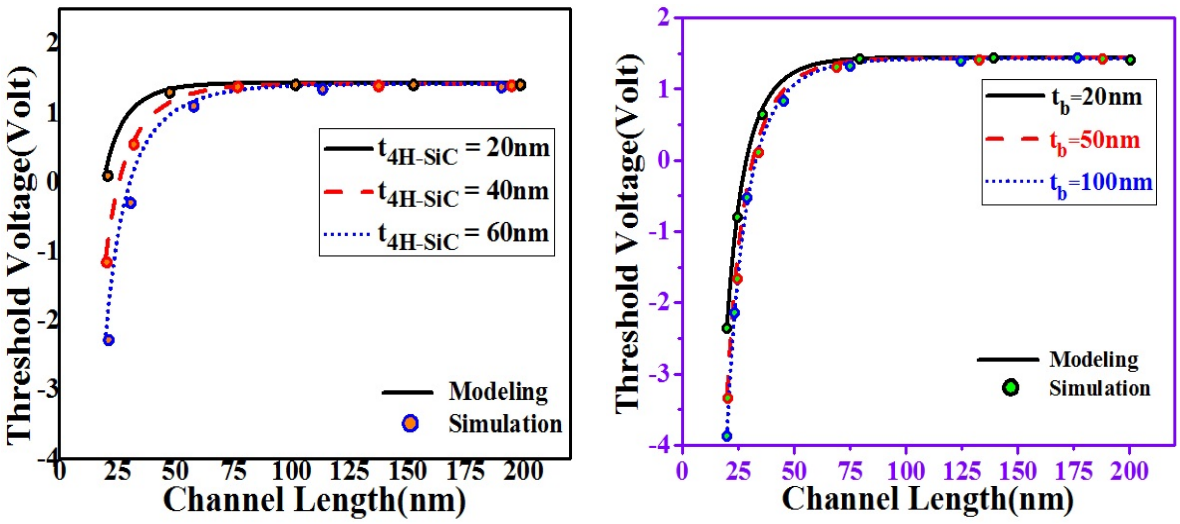
(a) (b)

Figure 4.7: Graph for threshold voltage vs channel length for (a)t_{ox} = 3nm, t_{ox} = 5nm, and t_{ox} = 7nm. (b) V_{DS} = 1 V, V_{DS} = 5 V, and V_{DS} = 10 V.

drain voltages V_{DS} = 1 V, V_{DS} = 5 V, and V_{DS} = 10 V. It is understood from the figure as V_{DS} values increases from 1V to 10V the threshold voltage also decreases that is undesirable. Hence, short channel effects increases in SOI-4H-SiC MOSFET for the high drain to source voltage. For proving accuracy, simulation result and analytical modeling results have been mapped.

Figure. 4.8(a) shows the variations of threshold voltage towards the channel length for three different values of 4H-SiC thickness t_{4H-SiC} = 20nm, 40nm, and 60nm. From equation (4.12), if the thickness of 4H-SiC film increases then the value

of α decreases so the value of Γ increases, thus from the equation (4.23) the minimum surface potential decreases in the channel region. From the figure, the value of threshold voltage for t_{4H-SiC} = 60nm falls earlier comparable to t_{4H-SiC} = 40nm and t_{4H-SiC} = 20nm. To verify the validity of the model, results from the analytical modeling have been mapped with simulation results. Figure. 4.8(b)



(a) (b)

Figure 4.8: Graph for threshold voltage vs channel length for (a)t_{4H-SiC} = 20nm, 40nm, and 60nm. (b) t_b = 20nm, 50nm, and 100nm.

shows the variations of threshold voltage towards the channel length for three different values of buried oxide thickness t_b = 20nm, 50nm, and 100nm. From the figure, as the thickness of buried oxide increases from 20nm to 100nm the threshold voltage decreases continuously. But if for the high value of t_b there will be no change in the threshold voltage. Thus, a proper value of buried oxide thickness must be chosen for which short channel effects could not increase.

4.7 Summary

An analytical modeling of the electric field, surface potential and threshold voltage for SOI-4H-SiC MOSFET is developed based on the two-dimensional physical model. The influence of quite a lot of device parameters like gate length scaling, metal gate work function, body doping, silicon carbide thickness, buried oxide thickness, gate oxide thickness on the electric field, the surface potential, and the threshold voltage are analyzed. The results envisioned by the model are when put next with 2-D simulations performed by using commercially available device simulator Sentaurus TCAD. The threshold voltage decreases with channel length but less comparable to conventional 4H-SiC MOSFET and SOI-Si MOSFETs. The use of SOI-4H-SiC instead of 4H-SiC is to increases the device performance regarding reduced short channel effects. The compressed model

adequately conclude the threshold voltage over a huge variety of parameters and can also be conveniently used to characterize and design the nanoscale SOI-4H-SiC MOSFETs with the desired device performance.

Chapter 5

Conclusion And Future Work

5.1 Conclusion

The use of 4H-SiC semiconductor material enhances the performance of the MOSFET device. Thermal conductivity and saturation velocity [17] of 4H-SiC semiconductor material is high it means the current caring capacity of 4H-SiC MOSFET is high than the Silicon MOSFET. 4H-SiC MOSFET has the significant threshold voltage and can operate at higher voltage and higher temperature comparable to Silicon devices. And in the output characteristic, it gives much greater drain current than the drain current flows in the silicon MOSFETs. Therefore in the characteristics point of view 4H-SiC MOSFET provides the better result than silicon devices. The drawback of the 4H-SiC MOSFET is threshold voltage instability. So in term of instability in threshold voltage, it is concluded that the instability in threshold voltage of 4H-SiC MOSFETs is due to the presence of many types of trap charges at the interface of Semiconductor/gate oxide interface. There is always some charges located inside the oxide layer and some charges at the semiconductor/oxide interface. Due to the presence of these charge in an oxide layer, there will require a shift in the gate voltage to reach the threshold voltage condition. After all, it is concluded that the instability in the threshold voltage can be reduced by using chlorine oxidation. It uses the small quantity of chlorine. This chlorine may be in the form of Cl_2 gas or it can be in the form of HCl, but science both these are potential material to deal with trichloroethylene (TCE). The presence of chlorine in the oxidation ambient is going to create a lot of silicon vacancies at the surface. So these interstitial moves towards the defects side and preserve the silicon crystal. So it is found that small quantity of chlorine during oxidation, helps not only in fixing the mobile ions but also reduces the oxidation induced stacking.

There is a regular scaling in the dimensions of the MOSFET device which decreases the performance in term of short channel effect and leakage. But now, 4H-SiC semiconductor material used in the nanoscale MOSFET can help in a much interesting way. In nanoscale 4H-SiC MOSFET when channel length decreases from 100nm to 60nm then there is no change in the threshold voltage. Means, threshold voltage remains same up to 60 nm and drops when channel length go below 60nm. But it much better results than silicon MOSFET regarding SCES. The drain-induced barrier lowering for nanoscale 4H-SiC MOSFET is decreasing because the value of barrier height of the channel potential is near about 2 V. Which is more than two times higher than the nanoscale silicon MOSFET. NOW nanoscale SOI 4H-SiC MOSFET came into the picture to enhance the performance of the nanoscale 4H-SiC MOSFET

regarding short-channel effects and leakage current. There are huge changes in the threshold voltage and surface potential model of SOI-4H-SiC MOSFET. It gives the surface potential value is approximately 3.4 V which is much higher than the nanoscale Silicon MOSFET and 4H-SiC MOSFET. Due to the large height of the potential barrier, there is a great reduction in the value of DIBL. Therefore, 4H-SiC MOSFET is much batter than the silicon MOSFET in term of transfer and output characteristics, operating limitations and short channel effects.

5.2 Comparison among the performances of Silicon, 4H-SiC and SOI-4H-SiC MOSFETs

- The height of the potential barrier for nanoscale silicon MOSFET is approximate 0.9 V.
  The height of the potential barrier for nanoscale 4H-SiC MOSFET is approximate 2 V.
  The height of the potential barrier for nanoscale SOI-4H-SiC MOSFET is approximate 3.5 V.

- Drain induced barrier lowering (DIBL) is high because it depends on the height of the potential barrier.
  The value of DIBL is low comparable to silicon and high as comparable to SOI-4H-SiC MOSFET.
  DIBL is very low as compare to Silicon and 4H-SiC MOSFET.

- Hot carrier effect is high because more number of charge carriers penetrate the S_i/S_iO_2 interface and moves inside the oxide due to presence of high electric field even when oxide thickness increases.
  The value of electric field decreases with increases in the gate oxide thickness.
  Thus, the hot carrier effect is low as comparable to silicon MOSFETs.
  Hot carrier effect is very low as compared to silicon and 4H-SiC.

- The value of threshold voltage is approximate 0.4 V for channel length $L = 100nm$. And threshold voltage drops continuously when channel length reduces.
  The value of threshold voltage is approximate 1.3 V for channel length $L = 100nm$. And threshold voltage decreases when channel length goes below 65 nm.
  The value of threshold voltage is approximate 1.5 V for channel length $L =$

100nm. And threshold voltage decreases when channel length goes below to 50 nm.

5.3 Future Work

In this thesis, the research work enhances the performance of the MOSFET devices regarding transfer and output characteristics, threshold voltage instability and short channel effects by choosing appropriate device parameters and device dimensions. There is the need for a lot of investigations for future. Some future work is the following-

- Develop various types of structure for 4H-SiC MOSFET to reduce short channel effects.
- Improve the threshold voltage stability using chlorine oxidation.
- Enhance the performance of the 4H-SiC MOSFET by improving the mobility.
- Proposed a model for 4H-SiC CMOS by using 4H-SiC NMOS and PMOS techniques.

Dissemination

Journals

- M K Yadav, K P Pradhan and P K Sahu 2016 A complete analytical potential based solution for a 4H-SiC MOSFET in nanoscale IOP Science Adv. Nat. Sci.: Nanosci. Nanotechnol. 7 (2016) 025011 (6pp).
- M K Yadav, K P Pradhan and P K Sahu Two-Dimensional Simulation and Analytical Solution for SCEs in Nano-scale SOI-4H-SiC MOSFETs communicated to Elsevier Journal.

Conference

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