EXTERNAL QUANTUM EFFICIENCY MODELING OF GaAs SOLAR CELLS GROWN ON Si: A METHOD TO ASSESS THE THREADING DISLOCATION DENSITY

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ABSTRACT: A method is reported in order to determine an upper bound for the Threading Dislocation (TD) density in experimental GaAs solar cells grown lattice-mismatched on Si. The method is based on the modeling of the devices' External Quantum Efficiency (EQE), using the classic drift-diffusion model, or Hovel model. The model is fitted to experimental EQE measurements, using the diffusion length of minority carriers as the sole fitting parameter. Assuming low surface recombination velocities at both interfaces, a lower bound for the diffusion length of minority carriers is determined. Considering non-radiative recombinations on TDs as the dominant recombination pathway, this lower bound for the diffusion length of minority carriers can be converted to an upper bound for the TD density, using the NTT model. This method is then used to assess the TD density in GaAs solar cells grown on Si by Molecular Beam Epitaxy, using Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs) coupled with Thermal Cycle Annealing (TCA) steps in order to reduce the TD density in the active region of the devices. Upper bounds for the TD densities in the low $10^7 cm^{-2}$ are thus extracted from the devices' experimental EQE measurements.
Keywords: Dislocation, Modeling, III-V Semiconductors, c-Si, Epitaxy

1 INTRODUCTION

Direct monolithic integration of III-V materials on silicon in a multijunction architecture, where high-efficiency high-bandgap III-V top cells are epitaxially grown on a crystalline silicon (c-Si) wafer acting as a bottom cell, is an elegant pathway toward the development of silicon-based devices exceeding the ≈29 % theoretical efficiency limit of single junction c-Si solar cells [1]. The main challenge of this approach lies in the difference of lattice parameters between the c-Si substrate and III-V materials of interest, as there is no nitrogen-free III-V material lattice-matched to Si with the required bandgap for a dual junction or triple junction device. As a result of this lattice-mismatch, Threading Dislocations (TDs) nucleate at the III-V/Si interface and propagate upward toward the active region of the device. There, TDs act as non-radiative recombination centers, reducing the minority carriers' diffusion length and lifetime. Hence, the performances of the upper III-V cells are impaired. Demonstration of top cells with a low Threading Dislocation Density (TDD) is thus of paramount importance for the success of the technology.

Rapid and accurate characterization of the TDD in experimental III-V solar cell devices grown on Si is therefore needed. Common characterization methods include Electron Beam Induced Current (EBIC), Cathodoluminescence (CL), Electron Channeling Contrast Imaging (ECCI), Planar-View Transmission Electron Microscopy (PV-TEM), Cross-Sectional Transmission Electron Microscopy (CS-TEM) and Defect Selective Etching (DSE). A review of the pros and cons of each technique has been presented by Yaung *et. al*. [2-3]. Although the best techniques can provide an excellent accuracy in the range of TDDs under investigation (10^4-10^8 cm^{-2}) [2-3], they require advanced microscopy equipment – such as a scanning electron microscopy system (EBIC, CL and ECCI) or a transmission electron microscopy system (PV-TEM and CS-TEM) – and/or advanced sample preparation, leading to the destruction of the portion of sample characterized (PV-TEM, CS-TEM and DSE).

In this contribution, we present an optoelectronic technique in order to calculate an upper bound for the TDD in fully fabricated GaAs solar cells epitaxially grown on Si. Knowing the wavelength-dependent refractive indexes $n(\lambda)$ and absorption coefficients $\alpha(\lambda)$ of the different materials used in the structure, the architecture of the device and its External Quantum Efficiency (EQE) are the only inputs needed to assess the TDD. With further information on the Surface Recombination Velocities (SRVs) of the emitter/window and of the base/back surface field interfaces, the TDD calculation can be refined and an absolute value can be extracted.

We apply this method to experimental p-on-n GaAs solar cells grown on Si using Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs), with and without Thermal Cycle Annealing (TCA) steps performed during growth. Lower bounds of 930 nm and 720 nm are extracted for the diffusion lengths of holes in devices grown with and without TCA steps, corresponding to TDDs of 1.5×10^7 cm^{-2} and 2.5×10^7 cm^{-2}, respectively. For the reference sample grown lattice-matched on GaAs, a lower bound of 2760 nm has been extracted for the hole diffusion length.

2 THEORETICAL MODEL

Simulation of the GaAs solar cells' EQE has been carried out using a combination of the minority carrier drift-diffusion model from Hovel and Woodall [4] and the diffusion length model in the presence of TDs developed by Yamaguchi and Amano [5]. A similar model has been developed by McClure *et. al*., with a good accuracy, to simulate III-V devices grown on polycrystalline substrates [6].

The equations for the contributions of the depletion zone and of the quasi-neutral regions to the photocurrent, as a function of the wavelength, can be found in the extension of the Hovel model presented in Ref. [7]. Reflection at the back of the device – at the interface between the base and the back surface field – has been neglected. The simpler version model from Ref. [7], without back reflection, has consequently been used. In

order to calculate a lower bound for the minority carriers' diffusion length, low Surface Recombination Velocities (SRVs) at the emitter/window interface and at the base/back surface field interface have been assumed, with values of 1×10^3 cm.s^{-1} for both interfaces. Reflection on the front surface of the device and absorption in the window and contacting layer have been calculated using OPAL 2 software [8].

Using the diffusion length as the sole fitting parameter, this modeled EQE is matched to experimental measurements. A lower limit for the diffusion length of minority carriers $L_{tot,min}$ – holes in the case of the n-on-p experimental devices presented hereafter – can thus be extracted. According to the NTT model [5], the diffusion length of minority carriers L_{tot} is then given by:

$$\frac{1}{L_{tot}^2} = \frac{1}{L_0^2} + \frac{1}{L_{TD}^2} \quad (1)$$

where L_0 is the diffusion length in the absence of dislocations and L_{TD} is the diffusion length associated with non-radiative Shockley-Read-Hall recombinations on TDs, given by:

$$\frac{1}{L_{TD}^2} = \frac{\pi^3 TDD}{4} \quad (2)$$

Assuming that the diffusion length in the absence of TDs L_0 is much larger than the diffusion length associated with SRH recombinations on TDs L_{TD} ($L_0 >> L_{TD}$), the contribution to the diffusion length from recombination on TDs dominate and $L_{TD} \approx L_{tot}$. In any case, $L_{TD} \geq L_{tot}$ is assured. An upper limit to the TDD can hence be calculated:

$$TDD \leq TDD_{max} = \frac{4}{\pi^3 L_{tot,min}^2} \quad (3)$$

Knowing the total diffusion length in the absence of TDs L_0, for example from comparison with an identical reference cell grown lattice-matched of GaAs, the calculation can be refined and a better assessment of this upper limit of the TDD can be calculated.

3 EXPERIMENTAL METHODS

3.1 Samples growth

Three samples were grown by solid-source Molecular Beam Epitaxy (MBE): two samples were grown lattice-mismatched on Si, with and without TCA steps; a third sample was grown lattice-matched on GaAs, as a reference. Details of the structure grown on Si are presented in FIGURE 1. The buffer consist of an AlGaAs nucleation layer followed by an AlAs/GaAs superlattice in order to flatten out the growth front and to achieve a smooth growth surface before growth of the four Strained Layer Superlattice (SLS) Dislocation Filter Layers (DFLs). Each DFL consists of a stack of ten alternating InGaAs compression layer and GaAs tension layers; inserted between two thicker GaAs spacer layers. Each DFL is less than 450nm-thick, leading to a total buffer thickness – including the nucleation layer and the AlAs/GaAs superlattice – of less than 3µm. This buffer is replaced with a 200nm-thick n$^+$-GaAs buffer for the sample grown lattice-matched on GaAs.

A standard cell structure has been used for both absorber materials, including a 30nm-thick n$^+$-$Al_{0.35}Ga_{0.65}As$ back surface field, a 2000nm-thick n-GaAs base, a 200nm-thick p$^+$-GaAs emitter, a 30nm-thick p$^+$-$Al_{0.75}Ga_{0.25}As$ window layer and a 50nm-thick p$^+$-GaAs contacting and capping layer.

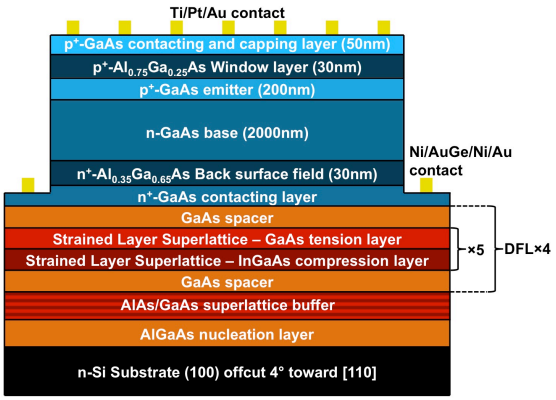

Figure 1: Details of the structure grown on Si. The red/orange layers represent the SLS DFL buffer; the blue layers represent the active layers of the cell. For the sample grown lattice-matched on GaAs, the SLS DFL buffer in orange/red is replaced with a 200nm-thick GaAs buffer.

3.2 Devices fabrication and characterization

Device fabrication was carried out using standard photolithography techniques. The samples were first etched in a H_2SO_4:H_2O_2:H_2O (1:10:80) solution, in order to define and isolate the mesa devices and to access the bottom n$^+$-type contacting layer. For the contact to the n-type region, a Ni/AuGe/Ni/Au contact structure was thermally evaporated and subsequently annealed at 390°C for 60s. The Ti/Pt/Au contact to the p-type region was then sputtered.

It is to be noted that, in order to avoid oxidation of the underlying Al-rich layers, the top GaAs capping layer has not been etched between the contact pads, leading to a non-negligible absorption in this lower bandgap layer. Moreover, no Anti-Reflection Coating (ARC) has been applied on top of the cells, leading to further reflection losses. Using OPAL 2 software [8], the losses through reflection are evaluated at 12.5mA.cm^{-2} and the losses through absorption in the contacting and window layers are evaluated at 5.0mA.cm^{-2}.

External Quantum Efficiencies (EQEs) were acquired using a ReRa SpeQuest quantum efficiency system, without bias. Absolute EQEs have been extracted by adjusting the measured EQEs to match the cells short-circuit current, measured at room-temperature under AM1.5G illumination from an LOT solar simulator.

4 RESULTS AND DISCUSSION

4.1 TDD extraction from EQE modeling

The experimental (circles) and simulated (solid lines) EQE data are presented in FIGURE 2. From the fitting of the simulated EQEs to the experimental data, lower bounds on the diffusion length of holes $L_{tot,min}$ of 720nm, 930nm and 2760nm have been extracted for the samples grown on Si without TCA steps (blue), grown on Si with TCA steps (red) and grown on GaAs as a reference (black), respectively.

As previously demonstrated with $Al_{0.2}Ga_{0.8}As$ solar cells [9], the use of TCA steps reduces the TDD by improving the mobility of dislocations, thus increasing the probability of dislocations encountering each other and self-annihilating or merging [10]. As a result, the diffusion length of minority carriers is increased, leading

to an improvement of the carrier collection efficiency, especially at the back of the cell where lower energy photons are absorbed. This improvement is visible on FIGURE 2, with an enhancement of the EQE at longer wavelengths using TCA steps.

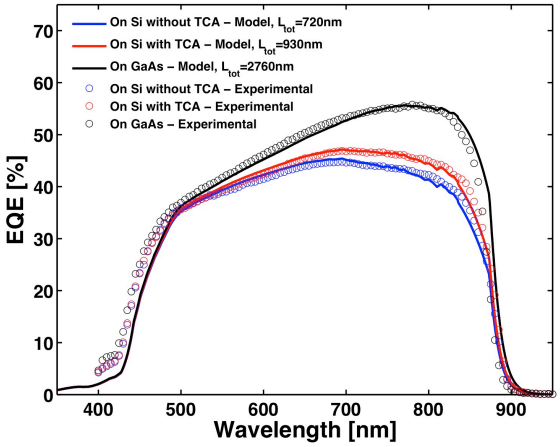

Figure 2: Fitting of the simulated EQE curves (solid lines) on the experimental data (circles). The three samples grown on Si without TCA steps (blue), on Si with TCA steps (red) and on GaAs as a reference (black) are displayed.

Assuming that the diffusion length is strongly dominated by the contribution from SRH recombinations on TDs ($L_{TD} \approx L_{tot}$), upper bounds for the TDD of 1.5×10^7 cm^{-2} and 2.5×10^7 cm^{-2} have been calculated for the samples grown with TCA steps (red) and without TCA steps (blue), respectively. Considering a similar contribution from non-TD-related recombinations for all samples (i.e. L_0=2760nm for the three samples), upper bounds for the TDD of 1.3×10^7 cm^{-2} and 2.3×10^7 cm^{-2} are obtained. The underlying assumptions behind these refined results are that the cell grown lattice-matched on GaAs presents a negligible TDD, that the TD-related and non-TD-related recombination pathways are independent and that, independently of the presence of TDs, the intrinsic material qualities of the three samples are similar.

These results compare with TDDs in the high 10^6 cm^{-2}, extracted from CS-TEM images, previously reported in $Al_{0.2}Ga_{0.8}As$ and GaAs devices grown lattice-mismatched on Si using SLS DFL buffers [9,11]. As expected, the upper bound for the TDD – calculated from EQE modeling – is higher than the CS-TEM measurements. The results are thus consistent. On top of the likely under-evaluation of the diffusion length – related to the assumptions of low SRVs and of independence of the SRH recombination pathways – inhomogeneities in the distribution of the TDD across the grown wafer can also explain the difference between the two calculations.

4.2 Limits of the method

Although a reasonable evaluation of the TDD can be achieved through the reported method, a certain number of hypotheses are necessary. A good confidence in the structure of the cell, especially regarding the thicknesses of the upper layers, is needed to accurately model the spectrum transmitted to the absorber region of the devices. The assumption of negligible reflection on the Back Surface Field appears to be justified, as the difference of refractive index between GaAs and $Al_{0.35}Ga_{0.65}As$ is limited over the range of wavelengths considered [12]. For structures where such a hypothesis would not be justified, implementation of the full model from Ref. [7], including reflection at the rear interface of the cell, would be needed.

The assumption of low SRVs at both interfaces leads to an underestimation of the diffusion lengths. Measurement of the SRV for experimental devices, in the presence and in the absence of TDs, could strongly improve the accuracy of the model. Similarly, assumptions on the contribution L_0 to the diffusion length from non-TD-related recombination pathways, for example from comparison with a reference device grown lattice-matched on GaAs, can increase the precision of the calculation. However, an additional strong hypothesis is then required: that the TD-related and non-TD-related recombination pathways are independent.

Finally, when recombination on TDs is not the dominant recombination pathway – such as in the $Al_{0.2}Ga_{0.8}As$ devices presented in Ref. [11] – our method presents limited interest, as the EQEs of devices grown lattice-matched and lattice-mismatched can be highly similar even though they exhibit a strong difference in TDDs.

5 CONCLUSION

We present an optoelectronic method to calculate an upper bound for the Threading Dislocation Density (TDD) in GaAs solar cells grown lattice-mismatched on Si. The method is based on the fitting of the External Quantum Efficiencies (EQEs) of experimental devices with the drift-diffusion model from Hovel *et. al*. [4]. Assuming low Surface Recombination Velocities (SRVs), a lower bound for the diffusion length of minority carriers is extracted. Using the NTT model [5], an upper bound for the TDD is then calculated. Applied to experimental n-on-p GaAs devices grown on Si using Dislocation Filter Layers (DFLs), a TDD below 1.5×10^7 cm^{-2} has been calculated for the sample grown using Thermal Cycle Annealing (TCA) steps. For the sample grown without such TCA steps, a TDD below 2.5×10^7 cm^{-2} has been extracted.

6 ACKNOLEWDGEMENTS

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