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Valley current characterization of high current density resonant tunnelling diodes for terahertz-wave applications

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We report valley current characterisation of high current density InGaAs/AlAs/InP resonant tunnelling diodes (RTDs) grown by metal-organic vapour phase epitaxy (MOVPE) for THz emission, with a view to investigate the origin of the valley current and optimize device performance. By applying a dual-pass fabrication technique, we are able to measure the RTD I-V characteristic for different perimeter/area ratios, which uniquely allows us to investigate the contribution of leakage current to the valley current and its effect on the PVCR from a single device. Temperature dependent (20 – 300 K) characteristics for a device are critically analysed and the effect of temperature on the maximum extractable power (P_{MAX}) and the negative differential conductance (NDC) of the device is investigated. By performing theoretical modelling, we are able to explore the effect of typical variations in structural composition during the growth process on the tunnelling properties of the device, and hence the device performance. https://doi.org/10.1063/1.4997664

INTRODUCTION

The frequency band between microwave and infrared radiation, also known as the terahertz (THz) frequency band (100 GHz - 10 THz), has recently gained significant research interest due to emerging applications in communications and sensing.[1–3] Requirements for practical devices operating in this spectral band are high output power and efficiency, as well as room temperature operation. Unlike many electronic and optical devices, the high current density resonant tunnelling diode (RTD) has been able to operate in this spectral region as the speed of operation of this electronic device is not limited by a conventional carrier transit-time or a band-to-band transition process[4] but by quantum mechanical tunneling.[5] First demonstration of a resonant tunnelling device was in 1972 by Chang et al.[6] After several years of research, room temperature operation has been demonstrated at a fundamental frequency of 1.92 THz[7] through minimization of conduction losses, highlighting the need for high output powers from these high current density (J), small area RTDs. The maximum theoretically output power, P_{MAX}, that can be extracted from a tunnel diode is given by Eq. 1.

$$P_{MAX} = \frac{3}{16}\Delta V \Delta I \tag{1}$$

where ΔV is defined as the span between the valley and peak voltage and ΔI the span between the peak and valley current of the negative conductance region.[8] The peak and valley points of the NDC

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region are defined by the extend of the region where the first derivative of the current with respect to the voltage is negative.

Eq. 1 clearly indicates that large voltage spans (ΔV) and current spans (ΔI) are required in the RTD's NDC region to obtain a high output power. The peak-to-valley current ratio (PVCR), which is defined as the on-and off-resonant current ratio, is an important figure of merit of the RTD as it provides a measure of the quality of the QW.[9] As the characteristic curve of the RTD is sensitive to parameter variations such as: barrier and well thickness, material composition[10] and doping,[11] accurate control over the quantum well (QW) interface perfection, compositional uniformity, and doping uniformity, is crucial to enable low-cost volume manufacture.

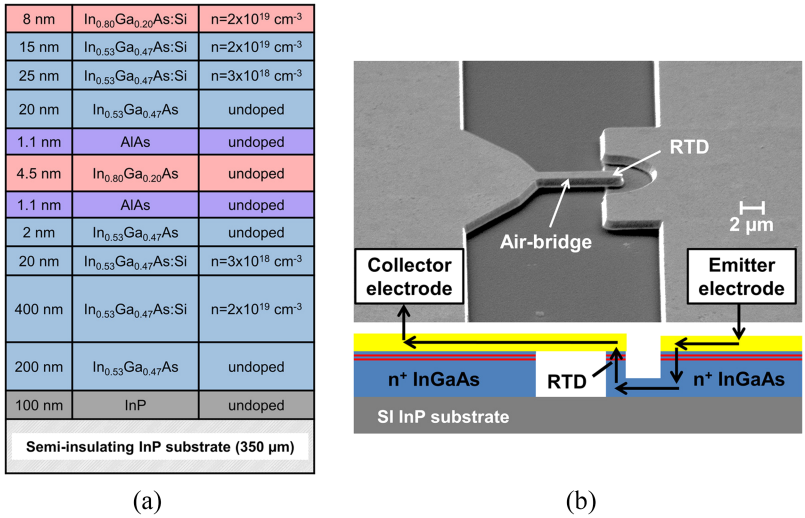
To solve the problems associated with the low-cost volume manufacture of this device, new characterization methodologies are required to support the epitaxial process. We recently reported how low temperature photoluminescence (LTPL) can be applied as a powerful characterisation technique for high J RTDs to non-destructive map important structural parameters of the RTD such as: doping concentrations, alloy compositional uniformity, average well-width and the monitoring of the structural perfection of the double barrier heterostructure with regard to interface roughness and alloy disorder.[12,13] We have also shown that by incorporating a 'dummy' RTD in the InGaAs buffer layer we can extract important information on the structural composition and electronic properties of the device, including the relative position of the first electron resonant energy level.[14] While LTPL allows monitoring of key RTD parameters that determine the overall I-V characteristic of the device, and hence the valley current, the technique does not provide information on the parasitic leakage current of the actual device and thermally activated transport mechanisms that contribute to the valley current. These mechanisms have previously been investigated both theoretically and experimentally for Si/SiGe, AlGaAs/GaAs, and AlSb-InAs RTDs,[15,16] but no detailed experimental analysis has been reported yet for high current density InGaAs/AlAs/InP RTDs.[17,18]

In this paper, we report an experimental analysis on the valley current of a high current density double barrier InGaAs/AlAs/InP RTDs grown by metal-organic vapour phase epitaxy (MOVPE), with a view to maximize P_{MAX} at THz frequencies, and hence the maximum operating frequency. We propose and demonstrate a methodology to investigate the origin of the valley current of a high J RTD by measuring the surface leakage current of the device and the temperature dependence of the valley current. By applying a dual-pass fabrication scheme, we have been able to investigate for the first time the leakage current of a *single* device with different perimeter/area ratios and investigate the effect on the PVCR. We note that the dual-pass fabrication scheme does not only enable the leakage current of the device to be investigated in detail, but the scheme also reduces the device fabrication complexity. We investigate the temperature dependent (20 – 300 K) electrical characteristics of our device to quantify the thermally and non-thermally activated valley current, and we discuss the origin of it through device simulation.

EXPERIMENTAL PROCEDURE

The RTD structure was grown on a semi-insulating InP:Fe substrate in a close-coupled shower head MOVPE reactor from Thomas Swan. Details about the epitaxial process are reported elsewhere.[12] Fig. 1(a) shows a schematic of the RTD layer structure with a 4.5 nm $In_{0.80}Ga_{0.20}As$ QW formed between two thin AlAs barriers and lattice matched InGaAs collector and emitter layers. Highly n-doped InGaAs ($2x10^{19}$ cm^{-3} Si) is used for the emitter and collector contact layers to enable the formation of low resistance ohmic contacts.

Fig. 1(b) shows a scanning electron microscopy (SEM) image of the fabricated dual-pass RTD and a circuit diagram illustrating the current path in this device.[19] Forming the emitter and collector electrodes *before* the RTD mesa uniquely allows us investigate the I-V performance from a *single* device with different perimeter/area ratios by measuring the I-V characteristic of the RTD during the etch process. To investigate the thermal performance of the device, I-V characterization was carried out in a closed-cycle helium (He) cryostat over a temperature range from 20 K to 300 K. The device temperature for these measurements was controlled with a PID temperature controller and a resistive heater element attached to the cold finger of the cryostat. Good thermal contact



(a) (b)

FIG. 1. (a) Schematic of the RTD layer structure (b) SEM and cross-sectioned schematic illustrating the current path in a dual-pass RTD.

between the device and the cold finger was established by bonding the device with indium to an aluminium oxide carrier tile. A Keithley 2400 source-measure unit (SMU) was used as a voltage source for the I-V characterisation and a two wire measurement scheme was adopted for the measurement.

RESULTS & DISCUSSION

Fig. 2(a) shows a series of room temperature I-V characteristics for a single etched device measured during the etch process. Resonant tunnelling is confirmed in this device as the NDC characteristic is clearly observed in the I-V curve. In addition, the "plateau-like" feature in the NDC region of the device indicates the oscillating nature of the measurement circuit when the RTD is biased within the unstable region.[20] The reducing peak current from etch A to G is attributed to a reduction in RTD mesa area due to the undercutting action of the etch. For a RTD peak current density of ~700kA/cm^2 in third-quadrant (i.e. negative bias is applied on the collector contact), we find that the device area reduces from ~7.8 µm^2 to ~3.8 µm^2 during the etch process. We were able to extract the peak current density for this material from a device fabricated using a different process as the wet etch undercut in this process prevents an accurate measurement of the mesa area. We note that the I-V characterization was carried out in third quadrant to minimize device self-heating and thereby inhibiting catastrophic failure as the initial device size is relatively large. The tunnelling current density in third quadrant operation is less than in first quadrant operation due to the asymmetric spacer layers.

We find that our devices are performing in-line with the literature for a measured PVCR of 1.6 in third quadrant, as the empirical fit of the peak current density against PVCR in literature from Sugiyama *et al.*[21] provides a PVCR of ~2.5 for a device with a similar peak current density operated in the first quadrant, and a ~1.66 increase in PVCR is expected for such devices between first and third quadrant operation.

While the PVCR provides an important measure of the QW resonator quality, we note that the ratio between the peak and valley currents also provides an important measure of the leakage current as we have been able to measure the I-V of a *single* device with different perimeter/area ratios. Fig. 2(b) shows the measured RTD peak current and valley current as a function of mesa radius as extracted from the I-V curves shown in Fig. 2(a). The inset shows the corresponding PVCR of the same device for etch A-G, with the device cross section (mesa area) shown on the horizontal axis. The blue and green solid lines represent the calculated trend for a peak and valley current scaling

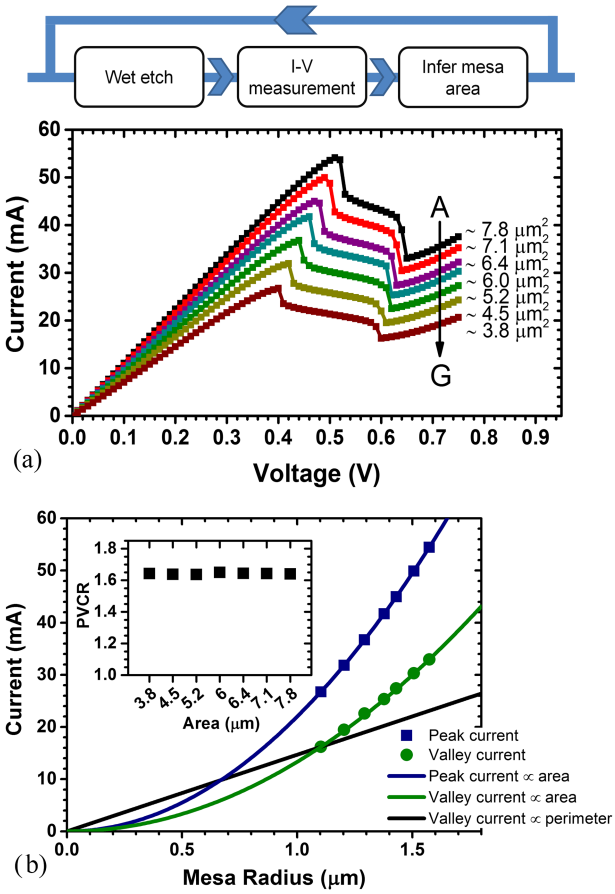


FIG. 2. (a) I-V characteristics from a single etched RTD measured in-line with the fabrication process. The device area for etches A-G represents the total RTD area and is calculated from the peak current density of the material (b) Experimental and theoretical RTD peak and valley current as a function of mesa radius. The inset shows the measured PVCR for mesa etch A-G.

to the area of the mesa, whilst the black solid line represents the expected trend for a valley current scaling to the device perimeter.

For a constant PVCR of 1.6 on a single etched device with different perimeter/area ratios, we can confirm that the valley current of the RTD can be associated to the tunnelling area of the mesa, not to leakage surface current through defects around the perimeter of the mesa. We highlight that by using a wet-etch process, we are able to effectively avoid the ion-induced sidewall damage that is known to occur with dry-etch processes. The introduction of energetic ions in a dry-etch process can induce traps and point defects in the mesa sidewall which can severely degrade the device performance. While the effect may not be of significant importance for large devices, it is of importance for micron and sub-micron scale RTDs as the damaged region, which can be up to 100 nm deep,[22] starts to become comparable to the device size. Furthermore, our results also indicate that no significant improvement in device performance (with regard to the leakage current) can be expected by passivating the mesa-sidewall.

Having confirmed there is essentially no sidewall leakage, temperature dependent I-V measurements were carried out to investigate the temperature dependence of the valley current, its effect on the PVCR, and device performance. Fig. 3(a) shows the I-V characteristics of a single RTD (n.b. different RTD as shown in Fig.2) from 20-300 K for voltage sweeps up to 0.85 V. Fig.3(b) plots the measured peak and valley currents and PVCR of the RTD (from Fig. 3(a)) as a function of temperature.

As shown in Fig.3(a), with increasing temperature we observe; an essentially constant peak current, an increasing peak voltage, an increasing valley current and an increasing valley voltage.

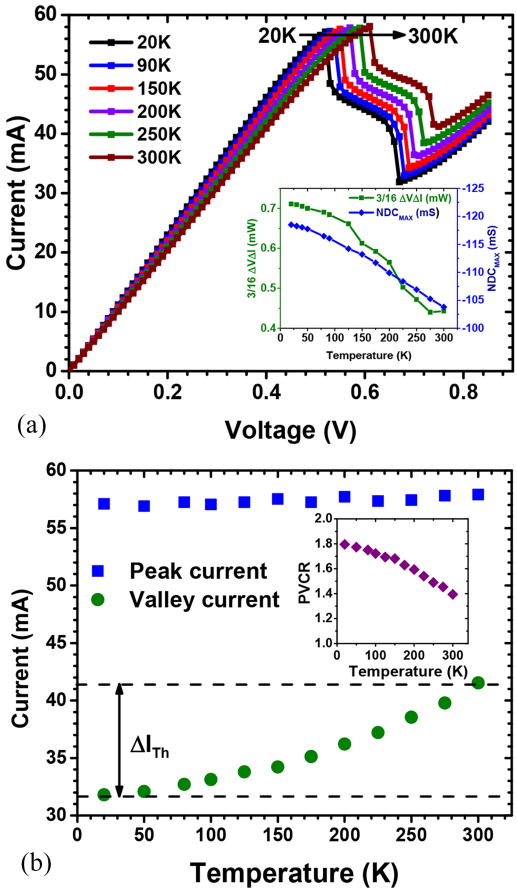


FIG. 3. (a) RTD I-V characteristics measured from 20 to 300 K. The inset shows the approximate maximum extractable power from the RTD and maximum NDC as a function of temperature (b) RTD peak and valley current as a function of temperature. ΔI_{Th} is defined as the thermally activated tunnelling current. The inset shows the PVCR as a function of temperature.

Fig.3(b) shows a 22% decrease in PVCR from 1.8 to 1.4. This reduction is associated to the increasing valley current with temperature. With regard to peak and valley voltage, a shift of 90 mV is observed, of which ~24mV (26%) is attributed to the thermal voltage across the active area. The remainder is attributed to the temperature-dependent series resistance of the external circuit, on which a similar observation was reported by Li *et al.* on GaN RTDs.[23]

Following Eq.1, it is clear that a thermally sensitive valley current has a direct impact on the maximum extractable power (P_{MAX}) and NDC_{MAX} of the device, thereby affecting the overall device performance. The inset of Fig. 3(a) shows the temperature dependence of P_{MAX} and NDC_{MAX} (maximum is typically observed on the onset of NDC[24]). When the device temperature is increased from 20-300 K, a 40 % decrease in P_{MAX} is observed from 0.72 mW to 0.43 mW.

Aside maximum output power, a temperature stable NDC is also important with regard to optimum device performance. A temperature unstable NDC will inevitably cause impedance mismatching and consequently reducing power transfer between the RTD and the load (e.g. antenna). From our measurements, a relatively small 15 mS (14%) increase in NDC_{MAX} is measured from 20-300 K. We note that quantitatively, the calculated NDC_{MAX} is an inaccurate value, as this is a DC-unstable region, though it provides important qualitative results, as opposed to using an arbitrary middle point or median of this NDC region.

Furthermore, as shown in Fig.3(b), on increasing the operating temperature from 20-300K, we observe that the valley current increases by 30 % from 31.8 to 41.5mA, whilst the peak current remains essentially unchanged as the Fermi level lies within the conduction band.[25] By extrapolating the peak and valley currents to higher temperatures, we predict that our RTD will fail to exhibit NDC

at ~500 K, which is still above the typical extended limit rating for conventional opto-electronic packaging. Extrapolating the valley current to the limit of 0 K shows that 72 % of the valley current tends to be not thermally activated, but is most likely rather related to other elastic and inelastic electron scattering processes, such as interface roughness, alloy, and impurity scattering.[26–28] This result suggests that the thermally-activated tunnelling is not as significant in these InGaAs/AlAs/InP RTDs as previously thought.[29] It is important to note, however, that several material characteristics change with temperature, such as conduction band energy, accumulated stress, saturation velocity, and the incoherent scattering rate.[30]

Whereas thermally activated tunnelling through higher electronic states can be reduced by optimising the energy interval between the resonant energy levels of the RTD, structural perfection of the epitaxial growth is expected to reduce the non-thermal component of the valley current. To explore the sensitivity of the structural parameters on the valley current, we have carried out a structural parameter sensitivity analysis by numerically modelling of effect of typical variations in structure and composition during the growth process, using the transmission probability of the RTD as an indicator. The impact of barrier thickness fluctuations, well thickness fluctuations and variations in alloy composition in the well on the electron tunnelling probability was investigated. Fig. 4 shows the effect of (a) monolayer (ML) barrier-width fluctuations (b) ML well-width fluctuations, and (c) indium composition fluctuations of the QW on the tunnelling probability of the structure. Fig. 4 shows that ML barrier-width fluctuations have a large impact on the tunnelling probability off-resonance, whereas ML well-width fluctuations mainly cause broadening of the second resonant energy level. From analysing the low temperature PL emission linewidth from lattice-matched InGaAs on InP, our measured linewidth of 6 meV corresponds to < 0.5 % variations in alloy composition over the exciton volume. QW alloy compositional fluctuations of 1% (n.b. an over estimate) are considered in Fig. 4(c). Binary compounds are expected to offer good performance figures by eliminating the alloy scattering in ternary materials. Smet *et al.* demonstrated a PVCR of 50 at 300 K for an InGaAs/AlAs/InAs structure with AlAs barriers of 9 ML for a peak current density of 6 kA/cm^2.[31] Even though alloy

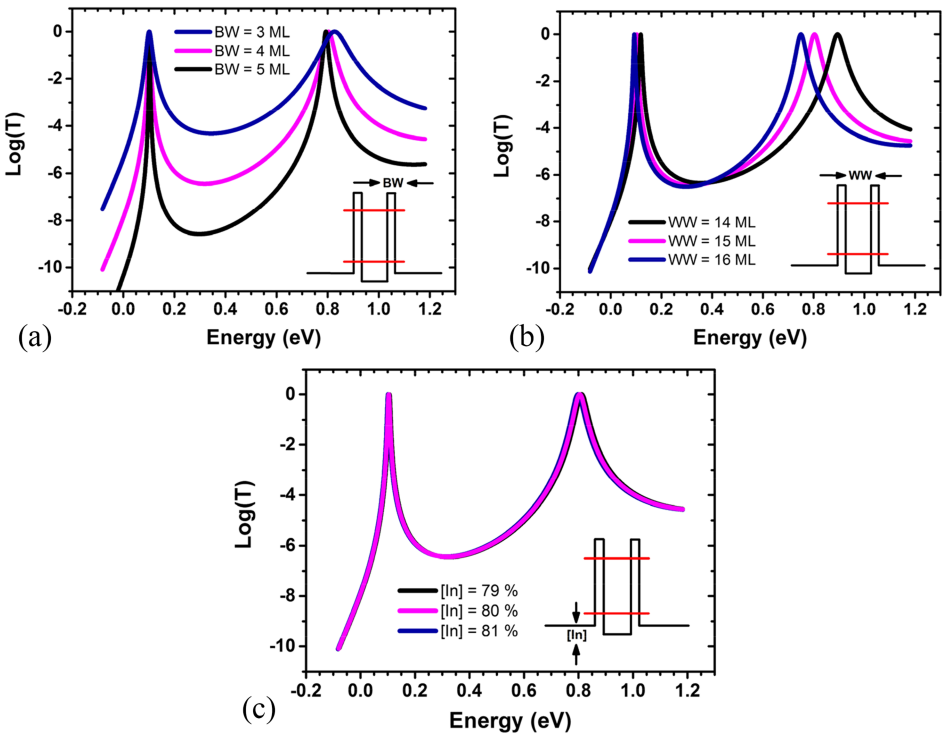


FIG. 4. Impact of (a) monolayer (ML) barrier-width fluctuations (b) ML well-width fluctuations, and (c) indium composition fluctuations of the QW on the tunnelling probability of the structure shown in Fig. 1(a).

compositional fluctuations are considered important, our modelling results show that the structural perfection of the potential barriers is a key parameter which defines the PVCR of these high current density RTDs, as the potential barriers of the high current density RTD are thin and have a large confining potential. Higher PVCR ratios are expected in future by optimising the epitaxial growth to minimise structural imperfections of the QW.

CONCLUSIONS

In summary, we reported on valley current characterisation of high current density InGaAs/AlAs/InP RTDs with a view to investigate the origin of the valley current and optimize device performance. By applying a dual-pass fabrication technique we were able to confirm that essentially no surface leakage current flows arounds the perimeter of the device by measuring the I-V characteristic during the etch process from a *single* device for different perimeter/area ratios with no change observed in PVCR. From temperature dependent I-V characterisation, we observed; a 22 % reduction in PVCR (1.8 to 1.6), a 40 % decrease in P_{MAX} (0.72 mW to 0.43 mW), and a 14% increase in NDC_{MAX} (103mS to 117 mS) from 20-300 K. We also find that only 28 % of the valley current is thermally activated, a lower contribution than previously reported. These thermal measurements show that not only good thermal heatsinking is required to minimize self-heating for optimum device performance, but practical devices might also benefit in future from active temperature control to obtain a stable performance. Our modelling results show that most of the valley current originates from structural imperfections of the QW, with AlAs barrier width fluctuations being highlighted as the primary candidate for optimisation.

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