A 32x32 ISFET chemical sensing array with integrated trapped charge and gain compensation

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***Abstract*—This paper presents a CMOS based 32×32 ISFET System-on-Chip for real-time ion-imaging. Fabricated in an unmodified 0.35μm CMOS technology, the ISFET sensor array is based on a pixel topology which uses capacitive feedback to improve signal attenuation due to passivation capacitance and a low-leakage floating-gate reset followed by a digital correlated double-sampling (CDS) to robustly remove unwanted trapped charge induced DC offset. An automatic gain calibration (AGC) is used to perform real-time calibration and guarantee all sensors have the same gain with a 99% accuracy and combining all these mechanisms guarantees an average pixel voltage variation of 14.3mV after gain is applied when measured over multiple dies. The full array is experimentally shown to be capable of real-time ion-imaging of pH, with an intrinsic sensitivity of 39.6mV/pH and a scan rate of 9.3 frames/sec when running the AGC, with a total power consumption of 10.2mW.**

I. Introduction

Ion-Sensitive Field-Effect Transistors (ISFETs) have shown significant promise in recent years for the design of fully integrated chemical sensing systems in CMOS, enabling the development of large-scale sensing arrays with integrated instrumentation and on-chip processing. Furthermore, fabrication of ISFETs in CMOS leverages on the economies of scale of the semiconductor industry and Moore's law to create high density systems at low cost. This has benefited specific applications including semiconductor-based DNA sequencing [1] and point-of-care diagnostics [2], which rely on label-free detection of H^+ ions, eliminating the need for fluorescent labels or optics required in conventional detection methods.

Fabrication of ISFETs in CMOS is enabled by extending the gate of a standard MOSFET to the top metal of the process [3], which is then in contact with an insulator sensitive to H^+ ions, typically SiO_2 or Si_3N_4. The structure of the device is shown in Fig. 1, along with its equivalent macromodel, where V_{chem} is the equivalent pH dependent voltage generated across the double layer Gouy-Chapman and Helmholtz capacitance, V_{tc} the trapped charge in passivation and C_{pass} the passivation capacitance which exists as a result of the Si_3N_4/SiO_2 top insulating layer.

However, ISFETs fabricated in unmodified CMOS experience similar challenges to regular floating-gate MOSFETs, both suffering from the trapped charge inducing DC offset and the attenuation of the sensed potential due to capacitive division. A threshold voltage spread of $-1.32V$ due to trapped charge and a loss of half transconductance efficiency

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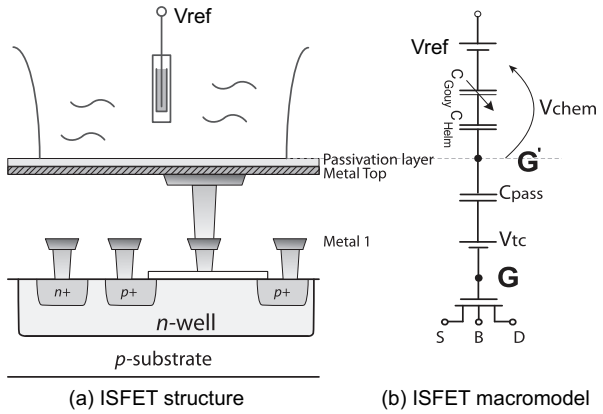


Fig. 1: Structure of the ISFET in unmodified CMOS technology and its equivalent macro-model [4].

(g_m/I_D) have been reported [3], both of which can provide severe constraints on the output dynamic range of the sensor. Additionally, regular ISFETs suffer from severe drift [5] due to the non-ideal nature of the passivation layer, which also degrades the sensor performance [6].

Efforts to design ISFET arrays have thus far focused on compensating for these non-idealities to reduce pixel-to-pixel variation in the array and improve sensor robustness and performance [7]. Some approaches reported in the literature have focused on post-processing of the CMOS die, such as [8] where trapped charge was removed using external UV radiation. On the other hand, some have attempted at circuit level compensation, including [9] where a programmable gate was used to bias all the ISFET sensors at the required operating mode. Inclusion of the programmable gate however leads to attenuation of the chemical signal.

In [4], the original concept of capacitive feedback was introduced for ISFET sensors, setting the floating gate voltage and hence compensating for trapped charge. The feedback circuit was implemented with a low leakage switch to create a robust front end and limit the inherent electrical drift at the floating gate. Additionally, in [10], it was shown how this feedback capacitor could be directly integrated as part of the ISFET sensor by taking advantage of the parasitics capacitance of the device. Such topology led to a voltage mode pixel with inherent gain and no capacitive attenuation at the expense of variable gain due to capacitor mismatch.

In this paper, we combine these two concepts to propose a novel, compact and low-power ISFET sensing array which is capable of compensating for issues including trapped charge,

pixel offset voltage and capacitive division of the input signal through direct capacitive feedback. We simplify the previous pixel [4] by reducing the number of transistors required to establish the floating gate voltage using the ISFET as a common source amplifier. The pixel allows trapped charge compensation through the use of a low leakage switch and integrates a physical capacitor in the feedback path to reduce pixel gain variation. The new pixel also includes an output buffer with a power down mechanism to allow the output to drive a line capacitance, as is expected in a larger array and keep the pixel power low to for scaling to larger arrays. An additional novelty is that we have included the generation of a local reference voltage which serves to further minimise the leakage current of the switch. A fabricated 32×32 sensor array is demonstrated which also includes an Automatic Gain Calibration (AGC) system to compensate for variation in pixel gain as a result of capacitor mismatch in the array, and a Correlated Double Sampling (CDS) mechanism to reduce the mismatch between pixels, in addition to an on-chip ADC and SPI for readout. This is the first demonstration of a complete System-on-Chip ISFET array using these methods with SPI readout for real-time pH imaging.

The paper is organised as follows: Section II presents the top-level system architecture, followed in Section III by a detailed description of the circuits implemented and in Section IV by an illustration of the system operation. Section V presents the fabricated system including the experimental platform, and the measured results are presented in Section VI. Lastly, we provide a conclusion in Section VII where we discuss the system performance.

II. System Architecture

The top-level system architecture of the ISFET System-on-Chip is shown in Fig. 2. The sensor array is composed of 32×32 pixels, which are addressed through multiplexing, similarly to the mechanism used in memory arrays. This is shown in Fig. 3 whereby each pixel comprises of the ISFET sensor and instrumentation. Pixels are firstly selected by row through an address decoder, whose outputs are then read by a column header. The current mirrors in every pixel are biased

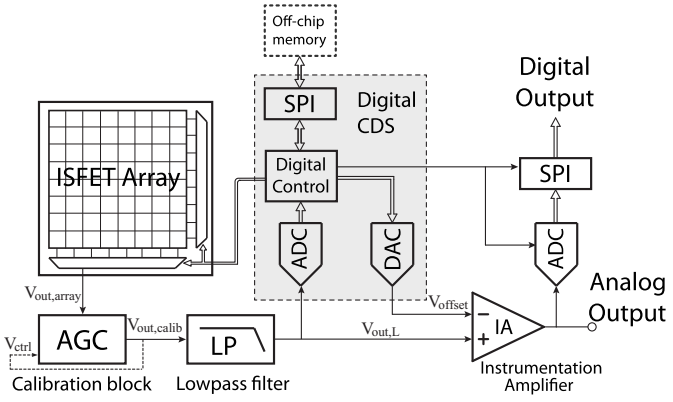


Fig. 2: Top level system architecture of the ISFET System-on-Chip.

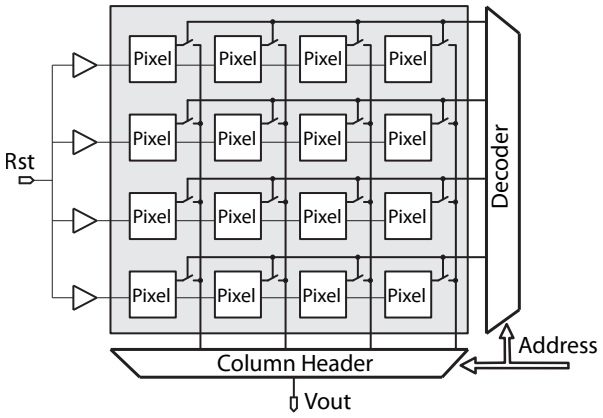


Fig. 3: Pixel array readout architecture. The pixel address is decoded into a one-hot signal. Pixels are selected by row and the column header multiplexes the active output.

by a global voltage V_{bp}, although the reset signal is buffered and driven only to single rows to guarantee a fast slew rate, which is critical to minimise charge injection effects. The output of each pixel is then calibrated in real-time using an Automatic Gain Calibration system to provide approximately 99% gain accuracy for the output signal. The AGC will be described in more detail in the next section. It is followed by a low-pass filter to remove high-frequency signals which are used to perform the AGC.

A digital Correlated Double Sampling (CDS) scheme is then applied to cancel out pixel offset. Digital CDS is used with offset values stored in off-chip memory as the system has been designed for measuring reactions lasting several seconds before the floating gate voltage is reset. The sampling scheme is designed to compensate for a CDS offset voltage of 200 mV using a resistive 8-bit DAC, and the output voltage is then subtracted with an instrumentation amplifier (IA). The resulting voltage containing the compensated chemical information is digitised with a sensing 8-bit ADC, operating at a range of 2V to capture a dynamic range of 10 pH. The ADC is implemented using a standard SAR approach. The bottleneck of the system in terms of speed is at the calibration phase of the AGC, and therefore the ADC is not optimised for bandwidth but adequately achieves 125k conversion rate to be able to measure the output of the array in real-time.

All the digital signals are controlled by a synthesised control block. The SPI block is used for serial communication of the output of the array to an external processing unit

III. System Implementation

We now present the design of each block described previously and highlight the design decisions.

A. ISFET pixel architecture

The pixel architecture used in the ISFET array is shown in Fig. 4. It is an improvement on the previously proposed front-end [4], which combines a low leakage reset of the floating gate, in addition to capacitive amplification through the ratio of

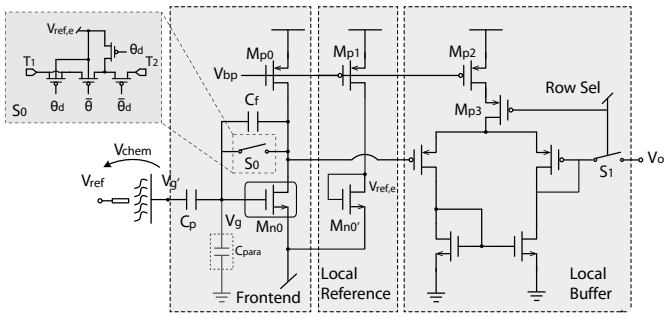


Fig. 4: The pixel architecture contains the sensing frontend based on a capacitive feedback configuration. The low-leakage switch requires a reference voltage generated by the local reference. The output is buffered locally to drive the line capacitance.

a gate-to-drain connected capacitance C_f and the passivation capacitance C_p of the ISFET.

A low leakage switch S_0 [11] allows the pixel to operate with two phases, a reset phase and a sensing phase. The reset phase cancels non-ideal DC offsets found in the ISFET such as trapped charge and drift, whereas the sensing phase tracks any chemical activity sensed by the sensor surface.

The gain of this front-end is determined by the ratio of the passivation capacitance C_p to the feedback capacitor C_f, to give an output response as [12]:

$$\Delta V_{out} = \frac{C_p}{C_f}\frac{2.3\alpha kT}{q}\Delta pH \tag{1}$$

where α is a scaling factor ranging from 0 to 1, describing the reduction of sensitivity from the ideal Nernstian response.

When using the pixel to create a large array, line capacitance becomes a main bottleneck which restricts the bandwidth of the design. In our circuit, we use a reference high-frequency sine wave for the AGC as shall be described in the next section and therefore need the circuit to operate with sufficient bandwidth. For this reason, a local buffer is added for the output of the pixel, with a power-down to disconnect it when the pixel is not being addressed. Additionally, a local reference circuit is included to generate a reference voltage $V_{ref,e}$ for the switch S_0. Although this is done at the expense of two additional transistors, keeping the difference between the stored and reference voltages minimal is essential to achieving extremely low leakage for the switch [11].

B. Automatic Gain Calibration

In order to compensate for capacitor mismatch between the passivation capacitance and feedback capacitor in Eq. 1 and guarantee that all pixels within the sensing array have exactly the same gain and therefore output response for a change in pH, an AGC circuit designed in [13] is used which continuously adapts the gain to reduce variation in sensor performance between pixels. The concept of gain calibration is illustrated in Fig. 5. Since the chemical reactions are generally very low frequency (e.g.$<$ 0.2Hz), the high frequency spectrum can be used to examine the gain variation between pixels. To achieve this, a high frequency (100 Hz) and small amplitude sinusoidal wave is applied through the reference electrode and superimposed on the sensed chemical signal. We thus generate a combined signal consisting of low-frequency sensed chemical information and a high-frequency sine wave carrying information about the sensors' local gain. The latter is then filtered out using a rectifier and a peak detector such that the output is compared to a fixed reference and any deviation is used to tune the bias current of a variable gain amplifier consisting of an OTA. This specifically designed AGC has been demonstrated to achieve 1.2% accuracy (1.2%peak-to-peak control fluctuation) with about 70μs settling time and a linear operating range of *800mV* which is adequate for our sensing array [13].

C. Low-pass Filter

Since the output signal from the AGC shown in Fig. 5 consists of both low frequency chemical and high frequency sine wave signals, it is necessary to filter out the sine wave component while still guaranteeing a fast response from the system. For this purpose, six 1st-order low-pass gm-C filters with 50kHz cut-off frequency are connected in series. Each g_m stage exhibits a transconductance of $290nA/V$ and load capacitance of around $900fF$. With these values, we yield an attenuation of 125 at 100kHz.

D. Instrumentation Amplifier

The offset signal is retrieved and converted back to the analogue domain using a DAC. To subtract it from the pixel readout, a conventional instrumentation amplifier is implemented whose output presents the final analogue output and can also be further digitalized.

Considering the linear range of the AGC output is around *800mV*, we add further amplification to use all the dynamic range of the system. According to the implementation shown in Fig. 6, the gain of the amplifier is defined as:

$$G = \frac{R_4}{R_3}\left(1 + \frac{2R_1}{R_2}\right) \tag{2}$$

By setting all the resistor values to $200k\Omega$, we tune the gain of this stage to 3. The output of the amplifier is then the final analogue output with all non-ideal offsets and pixel gain variations compensated for.

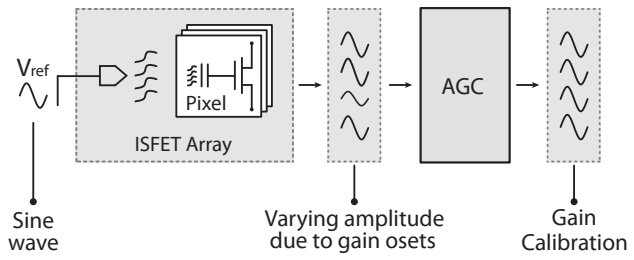


Fig. 5: The Automatic Gain Calibration System.

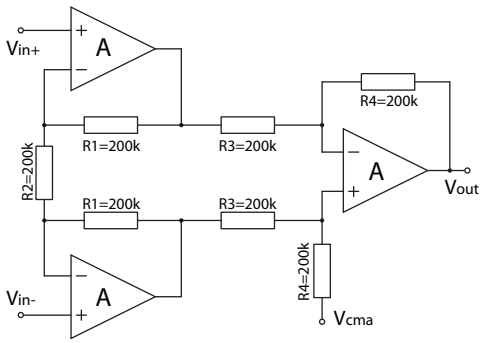


Fig. 6: Circuit topology of the instrumentation amplifier.

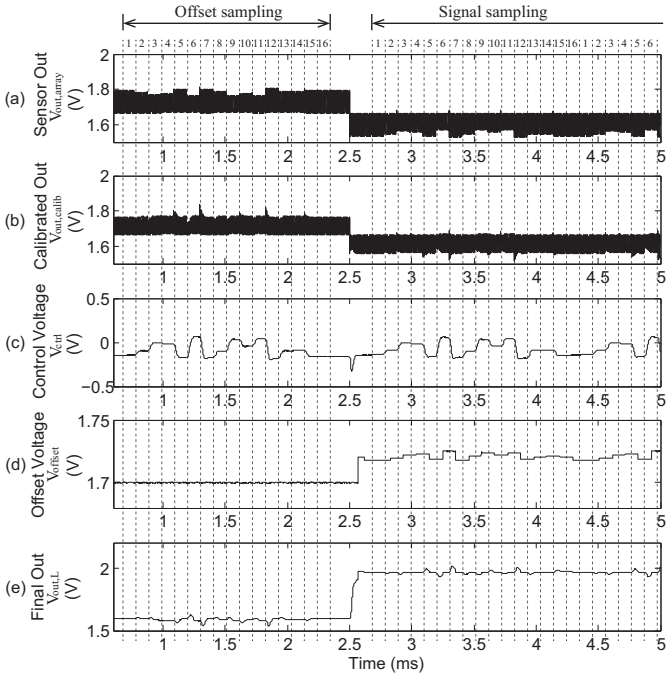


Fig. 7: Timing chart for the full system operation.

IV. System operation

In order to illustrate the system operation, we provide post-layout simulation results for a 4x4 ISFET array in Fig. 7. The passivation capacitances of these pixels are randomly allocated between 77fF and 107fF to simulate the mismatch while a feedback capacitor (C_f) of 72fF is chosen for our ISFET pixel. The clock frequency is set at 100kHz.

The system operation involves two phases as shown in Fig.7. The process starts with an *offset sampling* phase, whereby switch S_0 shown in Fig. 4 is closed and each of the 16 pixels is sampled by the digital CDS in 16 cycles to capture and store the offset. This is followed by a *signal sampling* phase to measure the chemical response of each pixel. During this phase, the switch S_0 is released to allow the ISFET to reliably sense the pH activity on its surface. Simultaneously, the AGC system to sets the pixel gain and the IA amplifier subtracts the offsets saved in the offset sampling phase. In the simulation shown in Fig.7, we emulate a chemical change by varying the gate voltage of the ISFETs by 100mV at 2.5ms, which is equivalent to a 2.5 pH change.

The depicted signals a-e shown in Fig. 7 are annotated in Fig. 2 and illustrate the chemical sensing operation of the system. Fig. 7(a) shows the multiplexed output signal from the ISFET array ($V_{out,array}$) containing a superimposed high frequency sine wave. Fig. 7(b) illustrates the signal ($V_{out,calib}$) after gain calibration using the AGC. Every time a new pixel is selected, the control voltage V_{ctrl} (Fig. 7(c)) is adjusted and settles quickly to calibrate the gain deviation. The sampled offsets which were saved in the first 16 cycles (V_{offset}) are shown in Fig. 7(d) to yield the final output ($V_{out,f}$) of Fig. 7(e).The distribution of the final output voltage of the 16 pixels is shown Fig. 8. The simulation results demonstrate that the added compensation reduces significantly the spread in output voltage to 2.4%, compared to a 39 % deviation which was the case before calibration. This shows that the system can reliably achieve in simulation good matching of pixel response with reduced offset.

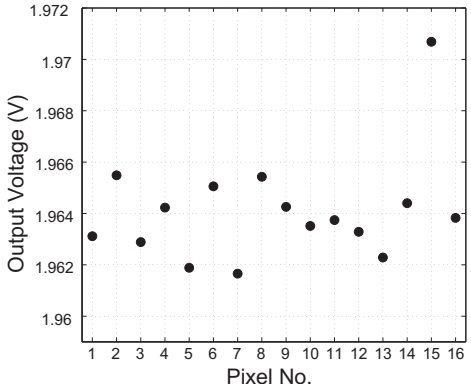


Fig. 8: Final output values of the 16 pixels. The calibration procedure allows a reduction in the standard deviation from 39% to 2.4%.

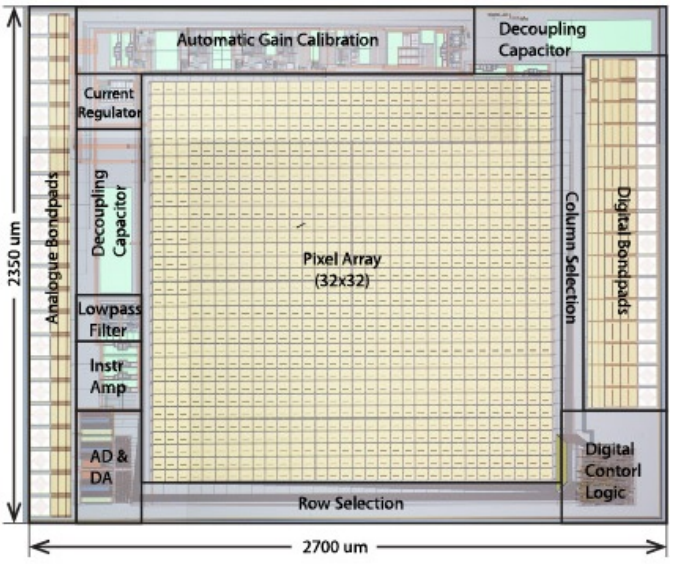


Fig. 9: Micro-photograph and floorplan of the fabricated chip.

V. Fabricated System

The full system was designed and fabricated in AMS 0.35μm CMOS technology. The fabricated chip is shown in Fig. 9, annotated with the floorplan. It consists of 1024 ISFET sensors with a chemical sensing area of 50μm x 50μm per ISFET and peripheral circuits to perform the operations described in Sections II & III. Due to the requirements of encapsulation using glob-top which isolates the aluminium pads and the wire-bonding from the solution, the ISFET array is located at the centre of the chip and a $200\mu m$ gap is left from each edge. The analogue and digital pads are separated at opposite sides of the chip and two on-chip decoupling capacitors are added to improve noise performance.

The SPI is integrated in the digital control block at the corner of the chip.

A. Experimental Platform

The platform designed to test the system is shown in Fig. 10. The bare CMOS dies are wire-bonded and epoxy encapsulated on a small PCB cartridge which is then plugged into a PCB motherboard. The motherboard PCB comprises of various components, including voltage regulators, variable resistors and analogue buffers to provide clean power supply and reference voltages to the chip. There are connection headers on each side of the motherboard, one for the SPI digital output connection to an FPGA, and the other for monitoring analogue signals at test points on the chip for debugging using SMB ports.

A microfluidic flow cell is clamped on top of the PCB cartridge forming a sealed chamber except for the inlet and outlet. The whole chip is immersed in solution whose flow is controlled by a syringe connected with the inlet of the chamber. An Ag/AgCl reference electrode is placed in the centre of the chamber to bias the ISFET devices. Since the chamber is fully sealed, new solution coming from the inlet will expel any previous solution rather than reacting with it, which is also guaranteed by the large volume of solution involved inside the chamber. As a result, the pH concentration sensed by the chip is the same as the one kept in the syringe when the chamber is flushed. Tricine 1M KCl pH buffers were used for the subsequent experimental tests.

The off-chip memory is implemented on a DE0 FPGA board, which is also responsible for sending the data to a computer, processing the output values in real-time. Due to clock synchronisation requirements, the clock used in the chip is generated from the FPGA. The connection between the FPGA and the computer is based on the UART protocol.

VI. Measured results (Fabricated chip)

In this section, we provide measured results from the integrated platform with the fabricated chip in order to validate the system operation. Four dies were prepared and measured.

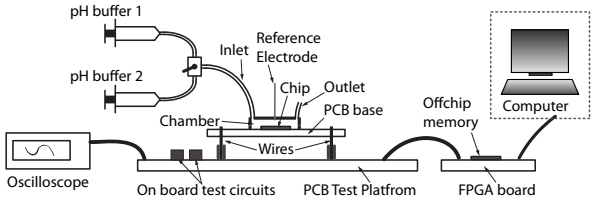
A. Pixel DC offsets

The first objective of the full system is to cancel the DC offset of the 1024 ISFET sensors using the digital CDS. The sampled offset values stored in the off-chip memory are represented in Fig. 11 for four dies, and are shown to follow a gaussian distribution.

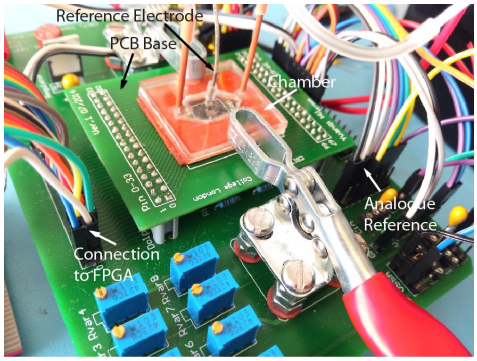
TABLE I: Standard deviation of offset voltages over 4 chips

	Chip 1	Chip 2	Chip 3	Chip 4
Std	13.9mV	14.2mV	14.0mV	15.2mV

An average standard deviation of *14.3mV* is obtained which indicates that the cancellation of trapped charge was successful. The mean value is less important since it is tunable via

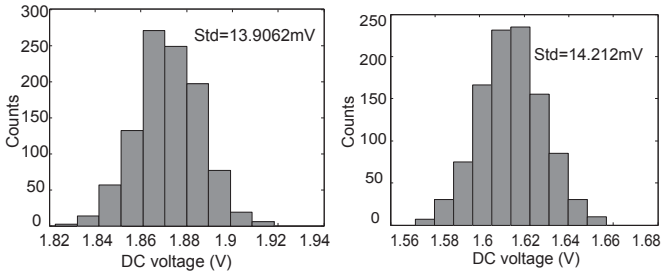


(a) Experimental platform test setup

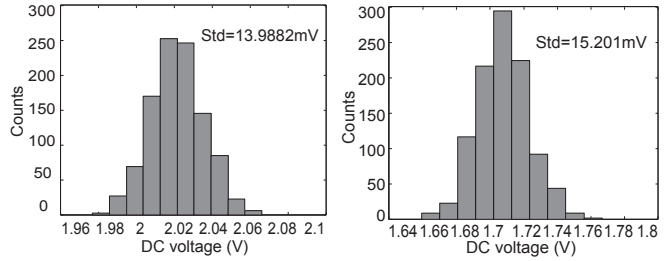


(b) Photograph of the experimental platform

Fig. 10: Experimental platform used to test the ISFET array.



(a) Chip 1 (b) Chip 2



(c) Chip 3 (d) Chip 4

Fig. 11: Distribution of the DC voltages over 4 chips.

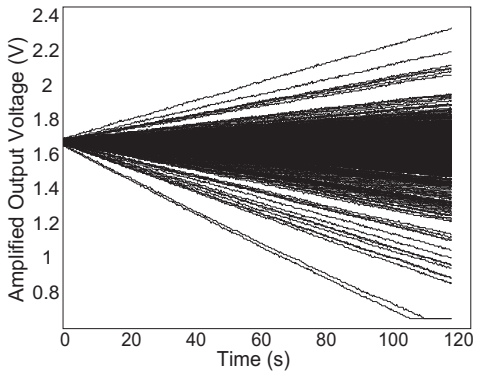


Fig. 12: Output drifts due to switch S_0 for the whole array. The amplified output voltage slowly varies in time due to leakage.

the source voltage of all the pixels. It can then be seen in Fig. 12 that after this offset cancellation step, the readout for all the pixels starts from the same voltage level.

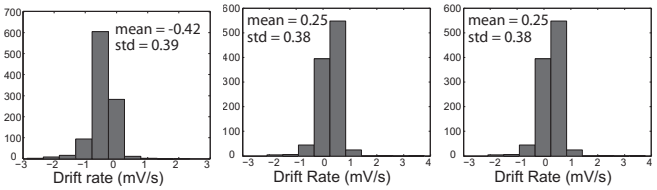
B. Drift due to switch leakage

As discussed in [4], the main concern of the two-phase sensing mechanism is the leakage due to the switch. The pixels inside the array can suffer from different drift rates which can also be positive or negative depending on the on the initial amount of trapped charge in each ISFET. Fig. 12 shows this effect for the output of the whole array, where amplitudes shown are after the gain of 3 applied by the the instrumentation amplifier. The internal reference voltage for the switch is set to 1.7V.

By investigating the leakage of each pixels in different dies, we found that its pattern still follows a Gaussian distribution, with mean value approximately equal to zero. The drift rate is shown in Fig. 13. It is important to note that through the reset switch S_0 drift compensation can be achieved as detailed in [4] by periodically resetting the floating gate of the ISFET.

C. In-pixel gain test

To test the effect of the AGC system electrically, the input signal is emulated as a change of the reference voltage instead of a variation of chemical solution. When increasing the reference voltage by 200mV, the output voltage of the array rises as shown in Fig. 14. The original and calibrated output signals are compared over 4 chips, and the measured distribution between all pixels is shown in Fig. 15.



(a) Chip 1 (b) Chip 2 (c) Chip 3

Fig. 13: Distribution of drift rates due to switch leakage for each chip.

The achieved standard deviation in output voltage for each chip before and after calibration is shown in Table II. It is important to note that the original gain distribution was much better than expected in this fabrication run, and hence we observe only a slight improvement in performance after the AGC. However, this indicates that our results will yield a lower spread in output, and will never result in a larger spread, even in the case where the array exhibits worse performance due to fabrication. In addition to this, the chip-to-chip variation in DC gain shown can also be always tuned by changing the external reference voltage of the AGC.

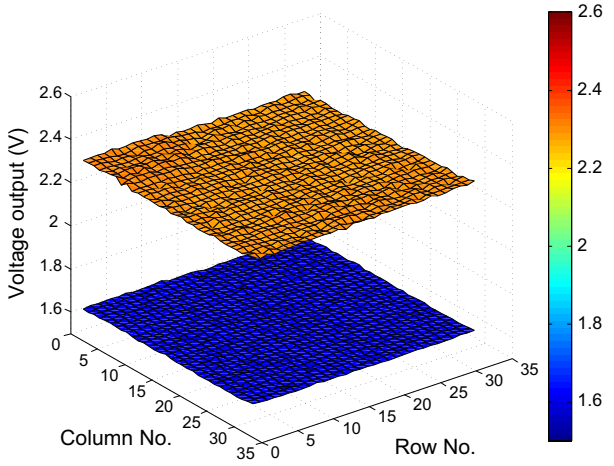
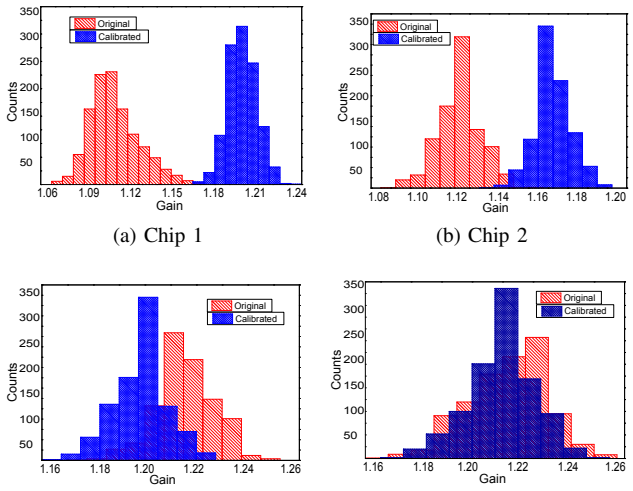


Fig. 14: In-pixel amplification over the whole array for a change of 200 mV in the reference electrode voltage.



(a) Chip 1 (b) Chip 2

(c) Chip 3 (d) Chip 4

Fig. 15: Distribution of the gain measured over 4 chips.

TABLE II: Standard deviation of the pixel gains over chips.

	Original	Calibrated
Chip 1	17m	9.8m
Chip 2	10.9m	9.1m
Chip 3	11.3m	10.2m
Chip 4	12.5m	10.8m

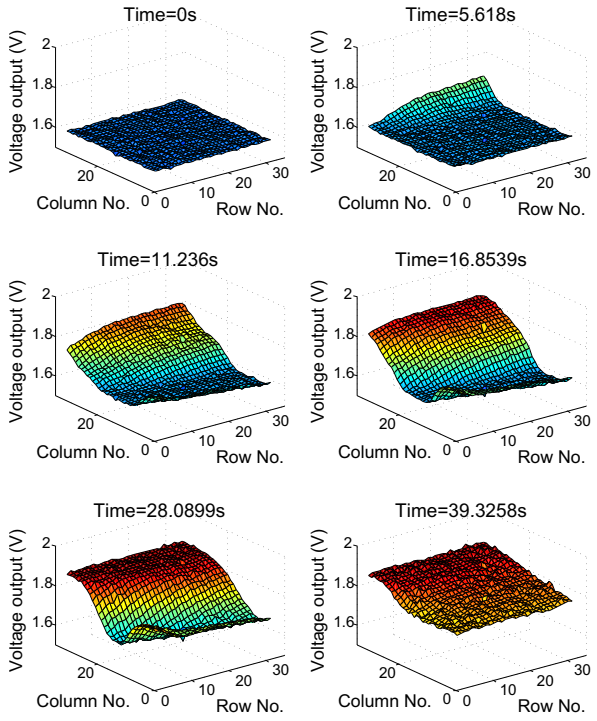


Fig. 16: The system output varies progressively in time for a change in pH from 7 to 9. The array illustrates the diffusion of the liquid at the surface of the sensors.

D. Ion-imaging

Lastly, we demonstrate the chemical imaging capabilities of the array.

1) Dynamic pH changes: The first experiment involves imaging the pH reaction at the surface of the array when flushing a pH 9 buffer solution into the chamber to replace the existing pH 7 buffer. Fig. 16 shows a 3D snapshot of the output of the array. It can bee seen that as the pH 7 solution is replaced by pH 9, the output response progressively varies to reflect the pH variation providing an image of the chemical change on the surface of the array.

The statistical data of this pH change as measured from the output of the chip is shown in Fig. 17. Considering the in-pixel amplification of 1.26 and a gain of 3 in the instrumentation amplifier, the intrinsic sensitivity of the sensor is approximately 39.6mV/pH which agrees with previously published ISFET sensitivites in unmodified CMOS [4].

The pH resolution is determined by the noise floor of the analogue front-end. We have measured the average noise floor for a pixel at 1Hz as 2.6mV, which corresponds to a pH resolution of 0.066 pH. We also characterise the absolute accuracy of the chip as

$$\begin{aligned}\text{Accuracy} = \text{pH sensitivity} \times \text{Gain error} \\ + \text{Voltage range} \times \text{Offset error} + \text{Noise}\end{aligned}$$

where the gain error is the measured standard deviation of the gain ($9.98m$) normalised with respect to the gain 3.78, the offset error is the measured standard deviation of the error ($14.3mV$) normalised with respect to the common mode

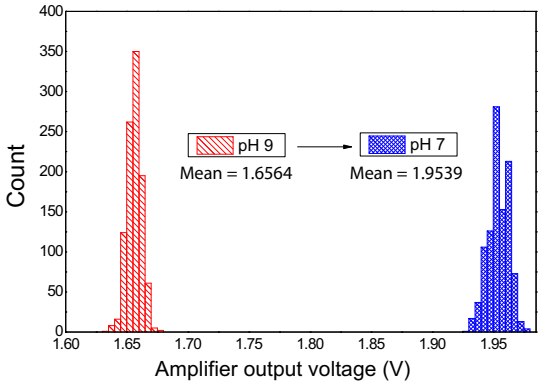


Fig. 17: Spread in voltage output of the array before and after the change in pH.

voltage and the noise is the noise floor of 2.6mV. This yields an absolute accuracy of 17.3 mV, or 0.116pH.

2) Sensor inhibition: In order to further demonstrate the spatio-temporal chemical imaging capabilities of the ISFET array, we cover a cluster of pixels inside the array with a polymer membrane which is pipetted to the surface and reduces the pH sensitivity of the sensors. The chip is shown under the microscope in Fig. 18a, clearly identifying the position of the polymer material. The membrane is then left to dry for 24 hours.

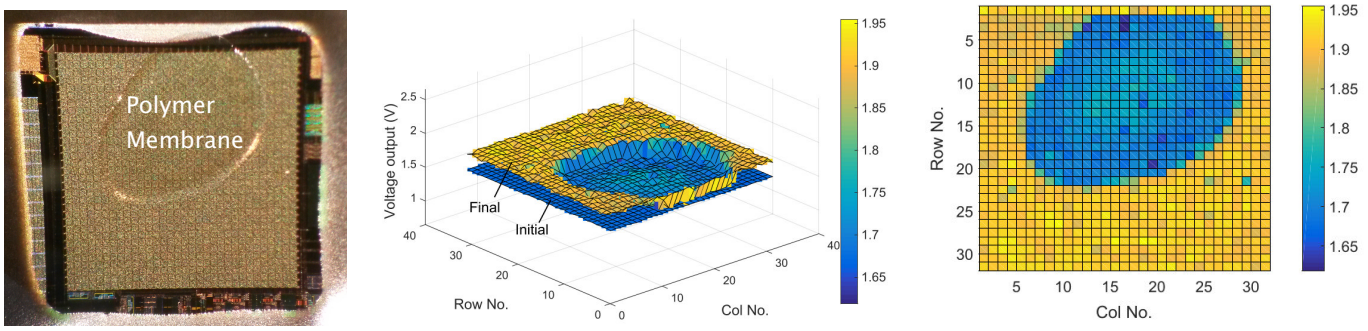
We now repeat the experiment described in 1) with a pH variation of 7 to 5. Fig. 18b shows the voltage across the array before and after the pH flush. The results demonstrate that the output of the covered pixels is maintained at the initial calibrated value, and Fig. 18c showing the array from the top successfully identifies the pixel covered by the polymer membrane. This confirms functionality of the system as a chemical sensing imager.

VII. Conclusion

In this paper, we have presented a robust 32x32 ISFET System-on-Chip for pH monitoring which combines for the first time a capacitive feedback readout for reduced chemical attenuation, reset of the floating gate for in-pixel offset calibration, and automatic gain calibration as well as digital CDS for pixel mismatch compensation. The system includes an SPI readout for real-time chemical image visualisation in addition to off-chip offset storage.

Measured results demonstrate the trapped-charge offset cancellation capabilities of the system, achieved by introducing the reset phase before sensing, with the remaining electrical offset exhibiting a low average standard deviation of 14.3mV over 4 chips. The digital CDS fixes the initial DC output voltage for all the sensors, with a resolution determined by the CDS and sensing ADCs. This allows to cancel any DC mismatch between the pixels, hence guaranteeing improved accuracy of readout and limiting the range of quantisation.

The achieved system specifications are listed in Table III including a detailed power consumption for each block. The complete system is capable of reading reliably pH images at 9 frames/second with an average pixel variation of 14.3mV at the output and a total system power consumption of 10.12mW.



(a) Chip photograph as seen under the microscope.

(b) Array output before and after injection of pH 5.

(c) 2D array output.

Fig. 18: Chemical imaging of the array for pH 7 - 5 with deposition of an ion-insensitive polymer membrane, before (initial) and after (final) the pH variation.

We have demonstrated that the complete 32x32 array has good performance for measuring pH with an average sensitivity of 39.6mV/pH.

Compared with our previously published programmable gate approach in [9], the new pixel architecture solves three main issues. (a) It avoids signal attenuation as a result of the programmable gate (improved intrinsic sensitivity of 39.6mV/pH in this work compared to 5.7mV/pH). (b) It minimises gain variation as a result of variance over all the pixels. (c) It reduces pixel variation in terms of offset cancellation and pH sensitivity ([9] achieves 9mV standard deviation with a total sensitivity 57mV/pH with a gain of 10, and our current work achieves 14.3mV standard deviation with a total sensitivity 149.7mV/pH with a gain of 3.78).

In Table IV, we compare our work with existing large ISFET arrays which were fabricated in unmodified CMOS technology. We show that our work is the first to compensate on-chip for trapped charge, sensitivity loss due to capacitive attenuation and pixel gain variation in ISFET arrays.

The platform undeniably represents a robust and efficient solution for chemical reaction imaging. Target applications can include diagnostics based on DNA detection, but we have also demonstrated its use in the context of ion-imaging. Thanks to the possibilities for H^+ ion detection, this system will provide great opportunities in the field of chemical sensing and Lab-on-Chip design.

TABLE III: Specifications for the full system.

Technology	AMS 0.35μm 2P4M CMOS
Supply Voltage	3.3V
Die dimension	2.7mm × 2.35mm
Array Size	32 × 32
Power Consumption	2.66mW (Array) (1.98μW/pixel)
	0.52mW (Digital logic @ 1MHz clock)
	4.65mW (AGC)
	2.29mW (Others)
	10.12mW (Total)
Sensing frame	9.3 frames/sec (105μs/pixel)
Trapped charge cancellation	$\sigma = 14.3mV$
Gain Calibration	$\sigma = 9.98m$
Intrinsic sensitivity	39.6mV/pH
Pixel sensitivity	149.7mV/pH with a gain of 3.78
Resolution	0.066 pH
Accuracy	0.116 pH

TABLE IV: Comparison of ISFET sensor arrays.

Ref.	[14]	[9]	[15]	This work
Technology	0.18μm	0.35μm	0.35μm	0.35μm
Pixel Size	20μm× 2μm	150μm× 150μm	10.2μm× 10.2 μm	50μm× 50μm
Array Size	8×8	8×8	64×64	32×32
Trapped charge compensation	Yes	Yes	No	Yes
Sensitivity loss compensation	No	No	No	Yes
Pixel Gain calibration	No	No	No	Yes
pH sensitivity [mV/pH]	37	57 (gain of 10)	20	149.7 (gain of 3.78)

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