Modular Integrated SiC MOSFET Matrix Converter

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Abstract— **This paper presents the assembly and characterization of an integrated all SiC 3-to-1 phases matrix converter, of typical application in domains requiring harsh environment withstand capability with high reliability and availability levels (e.g., renewable energies, solid-state transformation, smart grids, electric transport). Commercially available silicon-carbide (SiC) power MOSFETs are procured in bare-die form to develop custom-packaged bi-directional switches, with an advanced approach aiming to optimize the electro-thermal and electro-magnetic performance at switch level. Advanced cooling and packaging solutions at system level enable modularity with reduced impact of single component failure on the overall system, contributing to significantly reduced maintenance and repair costs.**

Keywords— Wide Band-Gap power Devices; SiC Power MOSFETs; Matrix converters, Integration.

I. INTRODUCTION

Efficiency, power density and reliability are main drivers of power electronics technology evolution. The conjunct improvement of these figures-of-merit is a challenging undertaking, due to the conflicting technological requirements underlying the optimization of each of them. The advent of wide-band-gap (WBG) semiconductors (e.g., silicon carbide SiC; gallium nitride, GaN) is enabling significant steps towards that aim. The use of SiC enables operation at higher frequencies and increased efficiencies. Hence, for a given power rating, the use of SiC devices can result in a reduction of the filter elements volume and weight. Higher efficiency also allows reduced heat sink size and typically weight. The use of SiC transistors in the matrix converter has been already addressed in recent studies, including a focus on the achievement of higher power densities and operation at higher temperatures [1]-[6]. Those investigations centerd mainly around the use of discretely packaged SiC transistors in a direct matrix converter. Nevertheless, bespoke packaging and integration solutions are crucial to ensure that the superior features of the device technology can be taken full advantage of. Building upon previous work done on silicon transistors (IGBTs) and diodes [7], this contribution delivers an innovative solution tailored to the characteristics of SiC MOSFETs: in view of substantially different functional and structural features between the two device types, an original design is presented to maximize the benefit that can be drawn from the integration exercise. The design is validated and optimized in terms of materials selection, geometry, sizes and cooling solutions by means of computer aided analysis. A prototype of the integrated bi-directional switch is presented, along with results of extraction of parasitic inductance in the device structure.

II. INTEGRATED BI-DIRECTIONAL SIC MOSFET SWITCHES

AC-to-AC power conversion requires switches that enable bi-directional (BD) current flow between the power source and the load, while blocking voltage of either polarity. If MOSFETs are used, then a typical BD switch (BDS) is as shown in Fig. 1: the drain terminal of each transistor (D1 and D2) is the only power terminal to the outside world, with current flowing in and out of it during operation, whereas the gates (G1 and G2) and common source (S) terminals are to be made externally accessible for driving purposes only. The common source connection simplifies gate-driver design and operation. If required by the switching scheme, current flow can also rely on the MOSFET intrinsic body-diode during some operational instants.

In view of its intended operation, an optimum integration

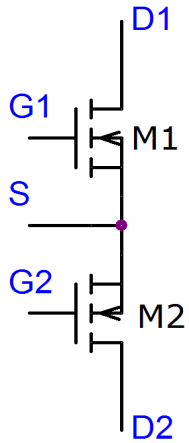


Fig. 1. Schematic of a bi-directional power switch using MOSFETs in common *source* connection. D_1 and D_2 are power terminals; $G_{1,2}$ and S are only used for driving purposes.

solution for this architecture is illustrated with the help of Fig. 2: the two transistor chips are mounted backside down (drain terminal) onto two separate, but identical direct bonded copper (DBC) substrates (Fig. 2 a)); one substrate is flip-mounted on top of the other by means of soldered copper (Cu) bumps (Fig. 2 b)); smaller bumps are used on the SiC chips top-side to implement the current conducting interconnection of the source terminals for between the two transistors (Fig. 2 b) and c)); a dedicated additional DBC substrate partly sandwiched between the other two substrates is used to implement the power terminals D1 and D2, whereas, for simplicity, bond-wires and external leads are still used for the gate-drive interconnection here (Fig. 2 c) and d). Fig. 3 shows a cross-sectional view of the integrated BDS with details of the power and drive interconnects. For reference, the devices used in this study are 1200 V – 80 mΩ MOSFETs, with dimensions of 3.1 x 3.6 mm^2 and about 200 µm thickness [8].

It is worth pointing out that the devised assembly solution is compatible with an automated process, which could run, for instance, according to the sequence:

- dies soldered on substrates (use of solder foil and masks)
- wirebonding;
- all bumps and gate-source drive terminals soldered on one substrate (use of solder paste);
- die carrying substrates and intermediate power terminals substrate soldered;
- insulation (gel filling) and terminals interconnections.

Also, the center power terminal carrier does not need to be a ceramic substrate and could instead be some kind of printed circuit board (PCB) of suitable thickness and material, able to withstand the temperature values involved in the assembly process. The switch and cooler design were optimized on the basis of extensive electro-thermal analysis [9].

The mechanical framework is implemented by the liquid cooler, constructed from a polymer in such a way as to enable easy thermal interconnection of multiple switches to form a system. The idea is illustrated in Fig. 4 for a single switch. Three such bricks can be easily interconnected by means of gaskets and screws and two additional plastic pieces (detailed in the next section) to build up a liquid cooled 3-to-1 phase matrix converter module

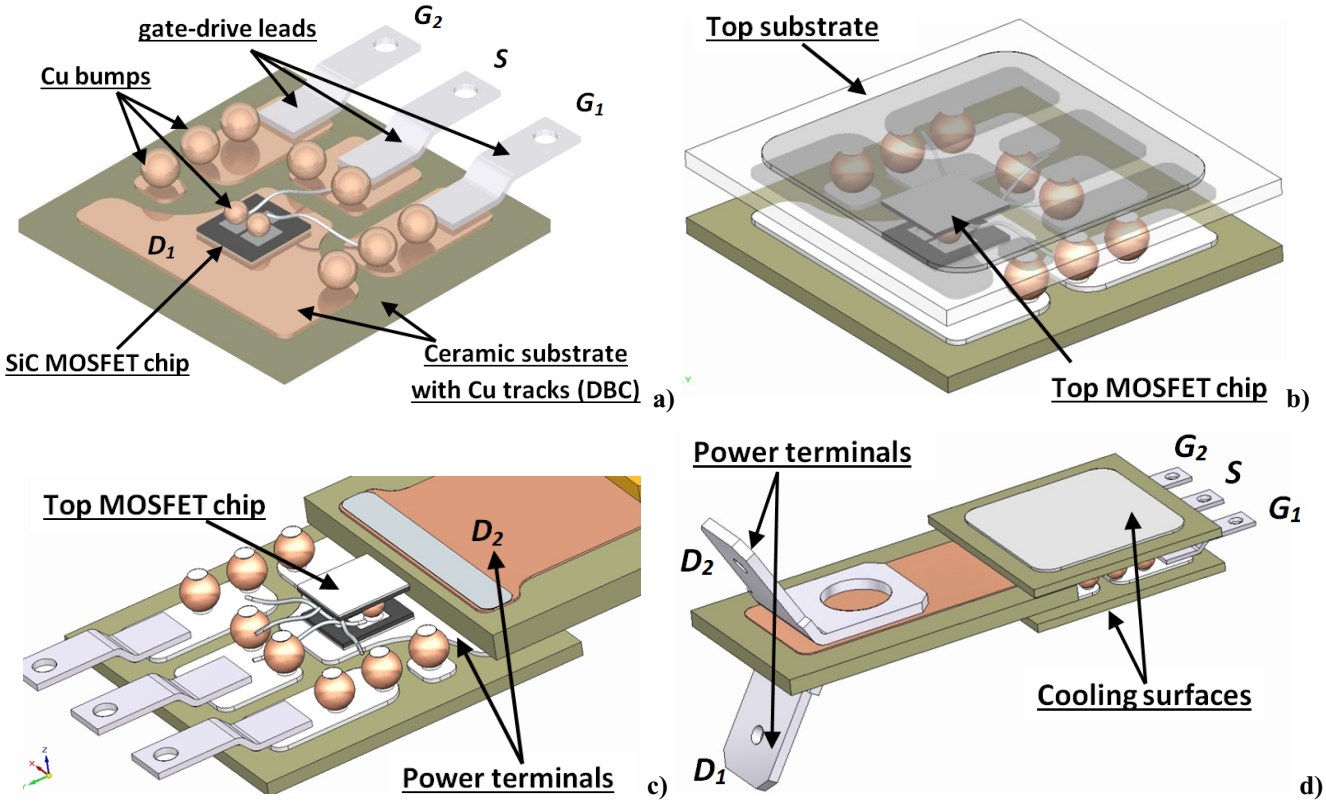


Fig. 2. In a), SiC MOSFET chip M_1 mounted on ceramic substrate. The chip side dimensions are 3.10 x 3.36 mm; the substrate is 15 x 15 mm; in b), mounting of top-side substrate and SiC MOSFET chip M2; in c), interconnection of third intermediate substrate for power terminals; in d), fully assembled power switch design.

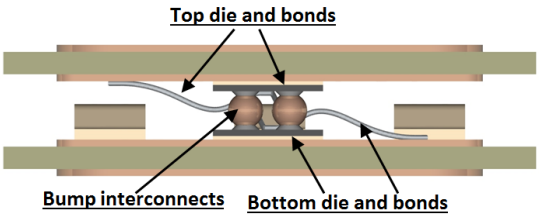


Fig. 3. Cross-sectional view of the BDS assembly

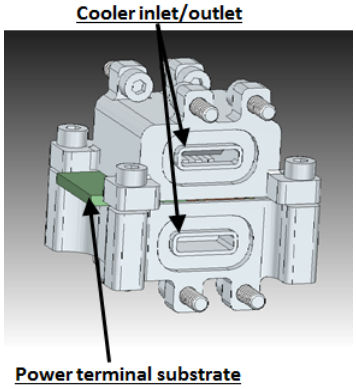
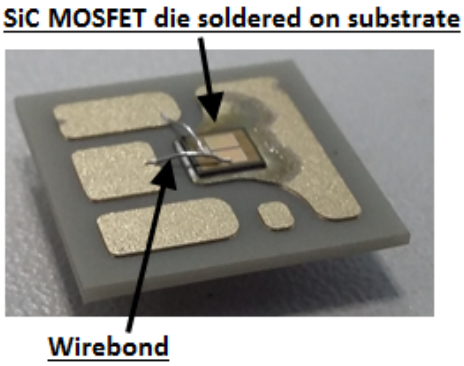
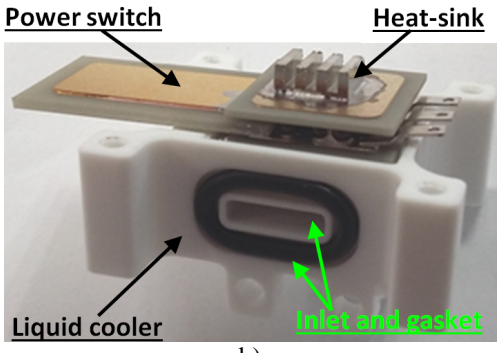


Fig. 4. Cooler design for a single switch



a)



b)

Fig. 5. In a), SiC MOSFET chip soldered onto ceramic substrate, with gate and source wire-bonded; in b), fully assembled power switch sitting on half of liquid cooler.

III. HARDWARE PROTOTYPE

Fig. 5 shows some parts of the hardware prototype, described in the caption to the figure. **The switches are insulated with dielectric gel. A gasket enables modular and re-openable system assembly simply via additional joining elements.**

The cooler design is also modular, so that assembly of a matrix converter block is achieved by combining a given number of elementary bricks. All elements of the structure are shown in Fig. 6: one joining element enables interconnection of two basic bricks as per Fig. 5; a second joining element, featuring a threaded cavity for mounting of the liquid fluid circulating pipes, enables connection to the temperature regulating unit. The final system level assembly is shown in Fig. 7: The phases are later terminated with soldered pins and interconnected by a dedicated bus-bar PCB, where the input filter passive components can also be mounted. The structure can be easily dismounted to replace a single brick in case of failure.

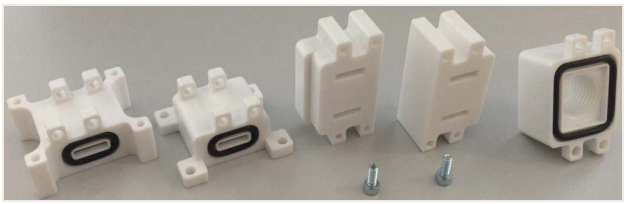


Fig. 6. Components of the liquid cooler unit.

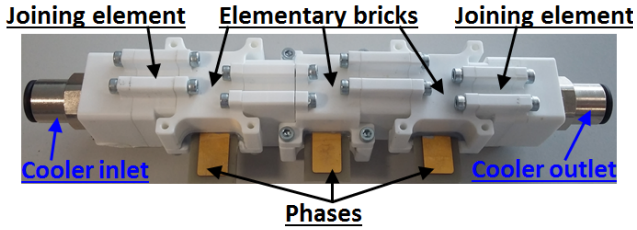


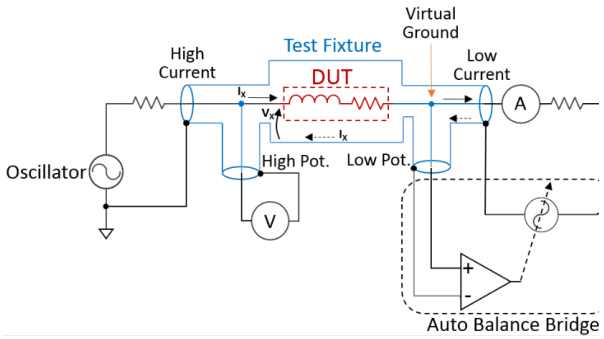
Fig. 7. Modular converter assembly (3-to-1 phases).

IV. PARASITIC INDUCTANCE EXTRACTION

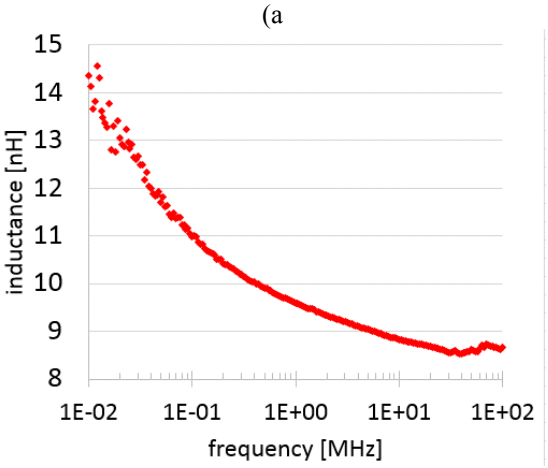
The final fully assembled bi-directional switch was characterized in terms of their parasitic inductance in the commutation loop identified by terminals D_1 and D_2 (see Fig. 2 a)). The characterization was done using a Keysight E4990A meter with the 16047E fixture to carry on measurements at higher frequencies. The procedure is illustrated in Fig. 8 a) and corresponds to the methodology put forward in [10, 11]: in black the parts of the impedance analyzer, in blue the test fixture and in red the device under test. The LCR meters used here are not traditional Maxwell-Wien or Kelvin/Thomson measurement bridges. Rather, when connecting a test object, the impedance $|Z|$ and the corresponding phase angle Θ (phase between current and voltage) are determined due to the Auto Balance Bridge. These measurement values are frequency dependent and are determined by means of a variable AC test signal (Oscillator). In this work the DUTs can be represented

by series R-L components. The extracted values of equivalent parasitic inductance are shown in Fig. 8 b) and indicate values fall within the range of a few nH.

The parasitic inductances in the commutation loop of the bi-directional switch can be measured connecting the terminals D_1 and D_2 to an LCR meter as shown in Fig. 9. Both MOSFETs are turned on with the same V_{GS} (17 V in this case). Fig. 10 shows the small-signal equivalent circuit of the device under test.



(a)



(b)

Fig. 8. a) Schematic diagram of the measurement setup based on the four terminal pair principle; b) Extracted overall parasitic inductance

The test fixture can be compensated directly by the LCR meter. The thus extracted values of equivalent parasitic inductance are shown in Fig. 8 b) and indicate values fall within the range of less than 15 nH. These values include the terminals used to connect the test device to the test fixture. Hence, there is a need to de-embed the inductance of the terminals used to connect the switch to the test fixture, because their minimum length which allows for connection is 2.5 mm (the inductance of the terminals is of the order of few nH as will be shown). The de-embedding technique applied here, was inspired by the TLM (Transmission Line Method) used for the measurement of the contact resistance across a metal-semiconductor interface [12]. Considering that the inductance of the wires results in series with the stray inductance of the bi-directional switch, some measurements were carried out by varying the length of the terminals of the test device from the test fixture and recording the inductance. This gives the relationship of the inductance of the terminal with length.

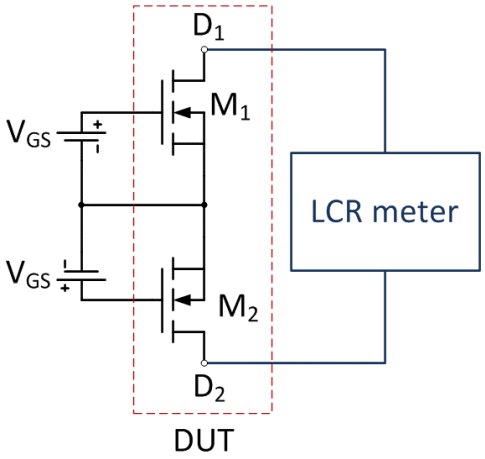


Fig. 9. Parasitic inductance measurement schematic.

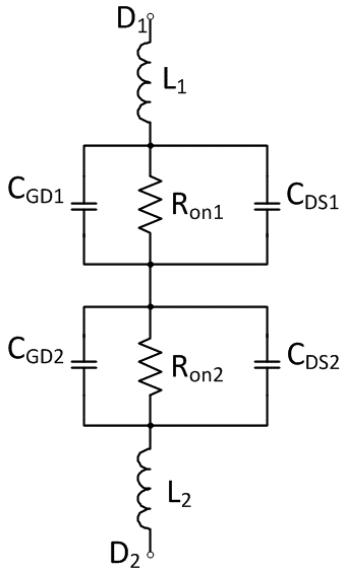


Fig. 10. Small-signal circuit model of the bi-directional switch biased as in Fig. 9.

Due to the fact that certain parts of the terminals are soldered to the test device and their respective lengths can't be altered at those points, a graph is derived that relates the inductance to the length of the terminals from the previous measurements. The inductance of the terminals is then extrapolated to a zero length, and deducted from the overall parasitic inductance. The resulting stay inductance L_s is shown in Fig. 11 at each frequency of the considered span (10 kHz – 100 MHz).The inductance of the shortest connecting wires is around 1.6 nH, not negligible if compared to the whole parasitic inductance of the bi-directional switch. The measured

R_s (Fig. 12), confirms that the R_{on} of the MOSFET is around 80 mΩ..

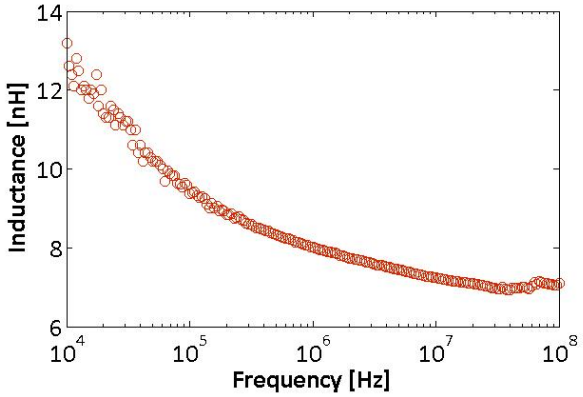


Fig.11. Parasitic inductance evaluated compensating the wires used to connect the bi-directional switch to the test fixture.

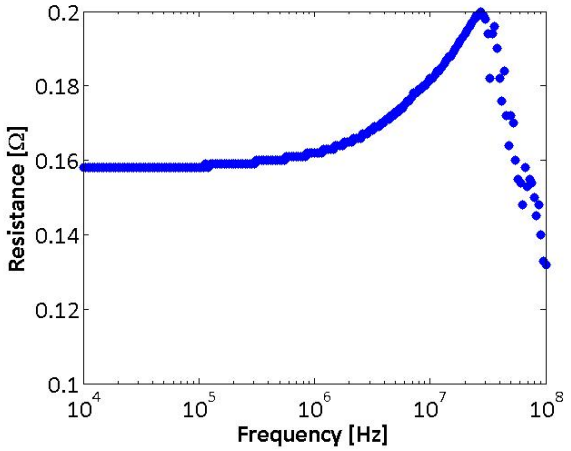


Fig. 12. Measurement result of the R_s resulting by the series of the MOSFETs in the bi-directional switch, both turned on.

V. CONCLUSION

This paper has presented assembly and characterisation of SiC power MOSFETs to create highly integrated bidirectional power switches, used to assemble a 3-to-1 phase matrix converter cell. The approach aims to improve state-of-the-art in power converter design and construction, by improving power density (including both volume and weight), performance and reliability, at the same time bringing along modularity for improved system level availability and reduced impact of failure on maintenance repairing costs and availability. The proposed assembly approach is compatible with automated processes.

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