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Characterisation of a Novel Reverse-Biased PPD CMOS Image Sensor

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ABSTRACT: A new pinned photodiode (PPD) CMOS image sensor (CIS) has been developed and characterised. The sensor can be fully depleted by means of reverse bias applied to the substrate, and the principle of operation is applicable to very thick sensitive volumes. Additional n-type implants under the pixel p-wells, called Deep Depletion Extension (DDE), have been added in order to eliminate the large parasitic substrate current that would otherwise be present in a normal device. The first prototype has been manufactured on a 18 µm thick, 1000 Ω.cm epitaxial silicon wafers using 180 nm PPD image sensor process at TowerJazz Semiconductor. The chip contains arrays of 10 µm and 5.4 µm pixels, with variations of the shape, size and the depth of the DDE implant. Back-side illuminated (BSI) devices were manufactured in collaboration with Teledyne e2v, and characterised together with the front-side illuminated (FSI) variants. The presented results show that the devices could be reverse-biased without parasitic leakage currents, in good agreement with simulations. The new 10 µm pixels in both BSI and FSI variants exhibit nearly identical photo response to the reference non-modified pixels, as characterised with the photon transfer curve. Different techniques were used to measure the depletion depth in FSI and BSI chips, and the results are consistent with the expected full depletion.

KEYWORDS: CMOS image sensor; Pinned photodiode (PPD); Depletion depth; Reverse bias.

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1. Introduction

Many scientific imaging applications are increasingly transitioning from CCDs to CMOS image sensors (CIS), particularly when high speed readout, low power dissipation or radiation hardness are required. Modern CIS routinely achieve sub-electron readout noise levels, something that is challenging for CCDs, and have very low dark current. These features are ideal for scientific imaging, however the quantum efficiency (QE) of monolithic CIS is usually much lower at near-infrared and soft X-ray wavelengths due to the relatively thin active semiconductor volumes.

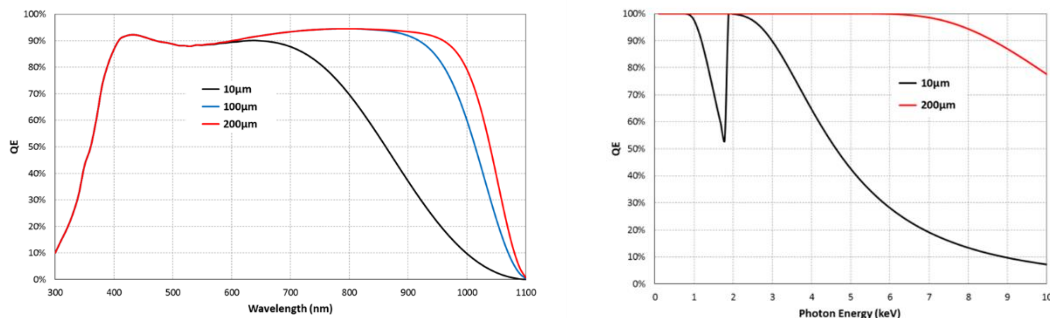

Figure 1 – Calculated QE for silicon image sensors with different photosensitive thicknesses. For visible and NIR light the sensor has broadband anti-reflective coating.

For a high QE at NIR and soft X-ray (<10 keV) bands, the active sensor volume should be tens or even hundreds of micrometres thick due to the large absorption length of silicon, as shown in Figure 1. To prevent deterioration of the modulation transfer function (MTF) this volume should be fully depleted and even over-depleted in order to increase the carrier drift velocity and to minimize the charge diffusion during collection [1].

Devices targeting high QE are normally back-side illuminated and made on high resistivity (>1 kΩ.cm) bulk silicon, however in CIS the normal operating voltages are not sufficient to achieve full depletion beyond approximately 10 µm. Applying a separate reverse bias is the usual way to overcome the low voltage limitation, but in monolithic CIS this leads to parasitic substrate currents. As shown in Figure 2, the front side p-wells in a p-type active silicon create a conductive path to the backside, which would cause large leakage current if the reverse voltage V_{BSB} is applied.

Preventing this current while preserving the properties of the pixel would open up the possibility of monolithic CIS with high QE, competitive to CCDs and hybrid sensors. In particular, developing a method applicable to pinned photodiode (PPD) CIS [2], which are widely used in mass market and high performance imaging would be extremely advantageous. In PPD sensors the collecting diode is a floating n-type implant topped with a shallow, heavily doped p^+ layer as shown in Figure 2. The p^+ implant is connected to the substrate via the pixel p-wells and maintains the top side of the PPD fixed (i.e. "pinned") to substrate potential. By driving the transfer gate (TG) high, charge is transferred out of the PPD to the sense node, which can be reset to an appropriate higher potential by the reset gate (RG). After charge transfer the PPD is fully depleted and the peak potential V_{pin} (the pinning voltage) resides few hundred nanometres below the Si-SiO_2 interface.

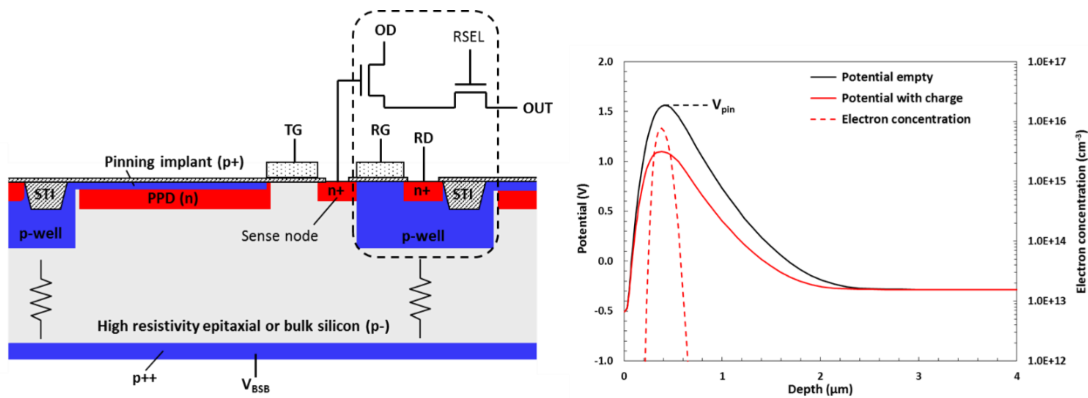

Figure 2 – Cross section of a typical (4T) pinned photodiode pixel (left); and its potential profile in depth through the centre of the PPD (right). All transistors are physically located in the pixel p-well, shown with a dashed line (left).

This paper describes a novel PPD pixel structure which successfully suppresses the leakage current and allows reverse voltage to be applied across the substrate to achieve full depletion of thick semiconductor volumes and high QE.

2. Operating principles

The conductive path under the p-wells has to be pinched off in order to supress the substrate current. This is illustrated in Figure 3(a) by the equivalent p-channel JFET created in the substrate, with the adjacent photodiodes serving as gates. The pinch-off condition does not occur naturally in PPD CIS due to the depth of the p-wells and the relatively low pinning voltage V_{pin}. To help achieve it, the new pixel design implements a deep, lightly doped n-type implant under the pixel

p-wells, as shown in Figure 3(b). This implant, called “deep depletion extension” (DDE) is floating and does not connect to the PPDs.

As described in [3][4], in normal operation the DDE acquires its potential from the adjacent PPDs and becomes depleted. By choosing the appropriate doping profile and size of the implant, its potential can be made lower than the peak diode voltage (the pinning voltage V_{pin}), but still high enough to create a potential barrier in the vertical direction. The DDE region acts as a bridge extending the depletions from the PPDs underneath the p-wells, creating a pinch-off and a potential barrier of sufficient height to prevent undesired substrate currents.

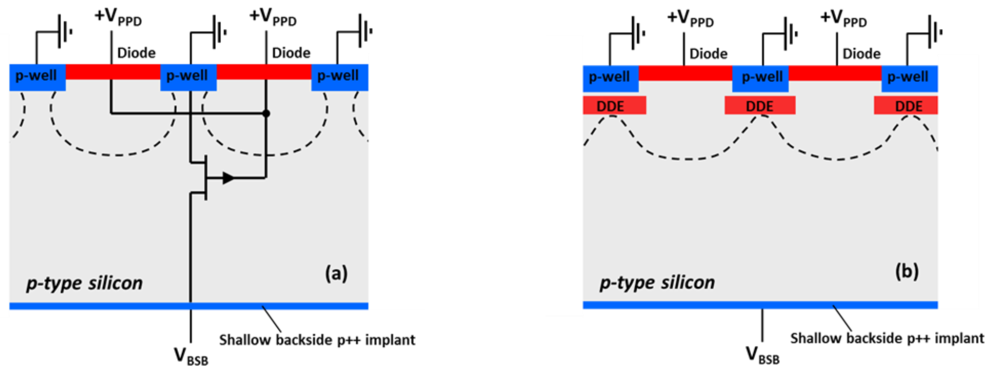

Figure 3 – P-channel JFET as an equivalent circuit of a reverse biased sensor (a), and the change of the potential distribution by the DDE implant resulting in a pinch-off (b).

3. Design

Based on the DDE concept, an image sensor was designed at the Centre for Electronic Imaging at The Open University and manufactured by TowerJazz Semiconductor in a 180 nm PPD CIS process. The sensor was made on 1000 Ω.cm, 18 μm thick epitaxial silicon and contains arrays with 10 μm and 5.4 μm square pixels, with each array implementing different shape and size of the DDE implant. The shape of the implant generally follows the shape of the pixel p-well and overlaps it, and the size of the overlap changes between the pixel variants.

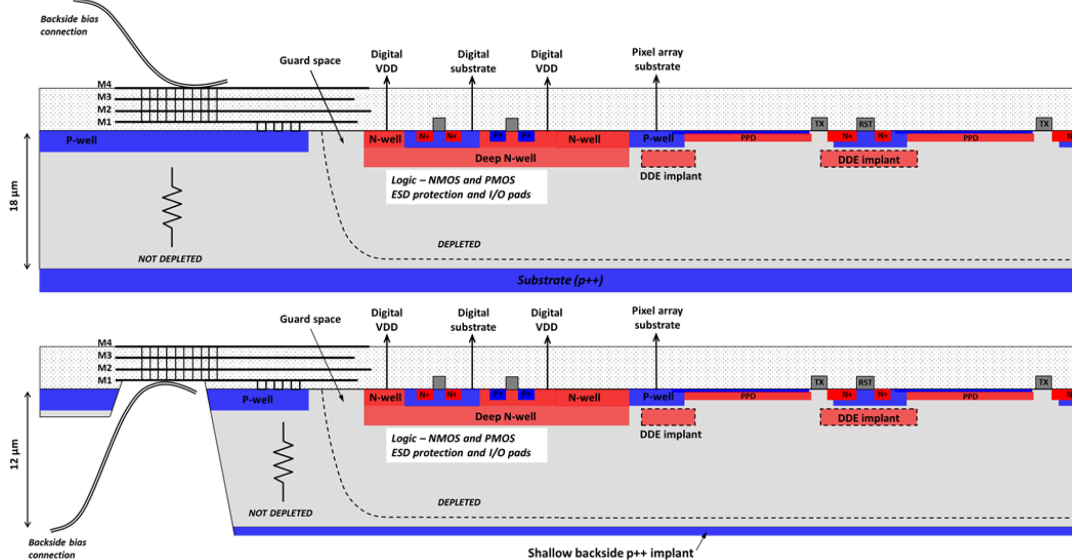

Figure 4 – Simplified cross sections of a FSI (top) and BSI sensor (bottom).

The cross sections of the sensor in both front-side (FSI) and back-side illuminated (BSI) variants are shown in Figure 4. BSI processing was carried out by Teledyne e2v, which produced a sensor thinned to 12 µm, with the backside implanted with a shallow p^{++} dopant for electrical conductivity and passivation.

The new pixel design is intended to minimize the disruption to the PPD doping profiles, bias and operation, and implements only one additional manufacturing step. Reverse bias is applied to the back through the conductive periphery of the chip, which is left intentionally undepleted as shown in Figure 4 and described in more detail in [3].

Three process variants with different depth of the DDE were manufactured – shallow, medium and deep, in combination with two different pinning voltages – 1.5 V (low V_{pin}) and 1.7 V (high V_{pin}). Simulations show that the peak of the DDE doping profiles ranges from 1.0 µm to 1.5 µm below the surface for the three depth variants, but significant dopant concentration is present down to 3 µm due to the high energy implantation.

One wafer type with high V_{pin} did not receive the DDE implant and was used as a reference, as the pixels on it did not receive any modifications. A variant with low V_{pin} and shallow DDE was not manufactured. Figure 5 shows a photograph of the FSI chip variant.

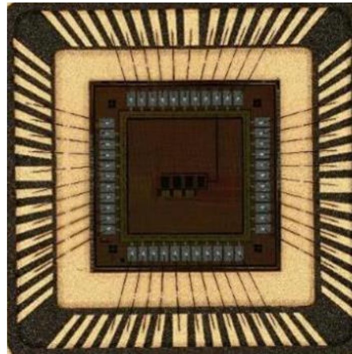

Figure 5 – Photograph of the FSI chip variant. The chip size is 5 mm × 5 mm.

4. Experimental results

A number of measurements were conducted on all devices in order to characterise their reverse current and photo response, and estimate their depletion depth.

4.1 Substrate leakage current

The substrate leakage current under reverse bias V_{BSB} was measured for all chip variants at room temperature, and the results are shown in Figure 6. In the reference design the reverse current is very large as expected, due to the resistive path through the substrate as illustrated in Figure 2.

In contrast, in all 5 DDE variants the substrate leakage current is suppressed up to a threshold voltage, above which it increases exponentially. This is consistent with the expected behaviour of thermionic emission [5] of holes over the potential barrier created by the DDE. The simulations in Figure 7 show that the barrier under the p-wells is lowered approximately linearly as V_{BSB} increases in absolute value. This potential modulation is typical for floating depleted volumes and is similar to the way the potential of a buried channel CCD is affected by the gate voltage [6].

The reverse substrate current I_{BSB} is described well by the thermionic emission equation with the addition of a leakage current outside the pixel area I_0:

$$I_{BSB} = I_0 + AT^2 S \frac{m_h^*}{m_0} \exp\left(-\frac{V_{PW} + \beta V_{BSB}}{kT/q}\right), \tag{1}$$

where A is the Richardson's constant for free electrons, S is the total area of the pixel p-well, m_0 is the free electron mass, m_h^* is the effective hole mass in p-type silicon ([5], p. 257), V_{PW} is the potential barrier height under the p-well at zero reverse bias, and β is a proportionality coefficient describing the change of the barrier height with increasing reverse bias V_{BSB}. Good estimates for V_{PW} and β are obtained from the potential simulations by fitting a straight line to the data in Figure 7(b). The threshold voltage can be expressed from (1) at the point when the thermionic current equals I_0 and gives

$$V_{thr} = \frac{1}{\beta}\left[\frac{kT}{q} \ln\left(\frac{AT^2 S}{I_0} \frac{m_h^*}{m_0}\right) - V_{PW}\right]. \tag{2}$$

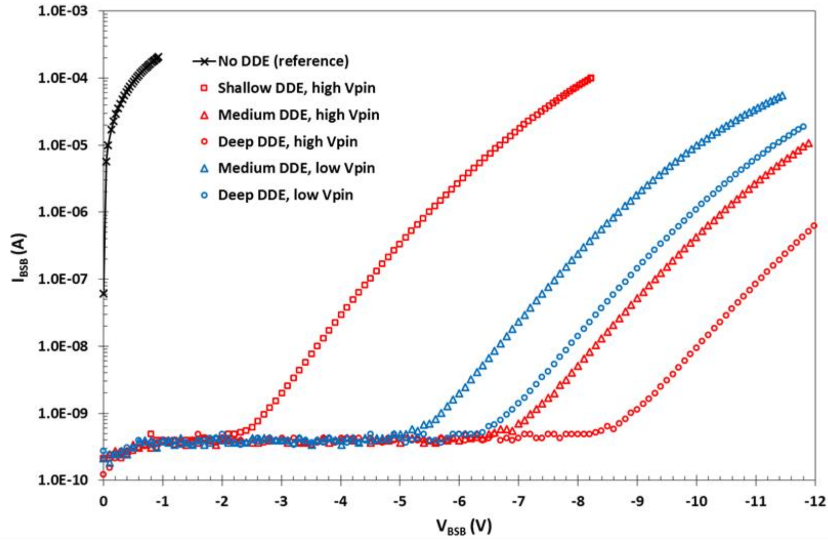

Figure 6 – Measured reverse currents in all 5 FSI chip variants, including the reference device.

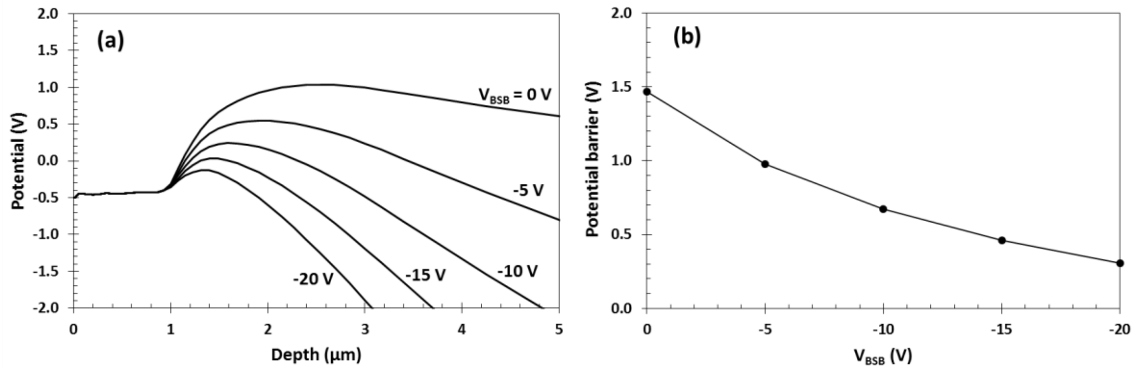

Figure 7 – Simulated potential profiles in depth under the p-well for medium DDE implant (a), and decrease of the potential barrier as a function of V_{BSB} (b).

For the chosen device resistivity and epitaxial thickness the calculated full depletion voltage is V_{BSB} = -4V. This implies that all chips with medium and deep DDE can be over-depleted.

Most of the applied reverse voltage drops across the depleted epitaxial silicon, and begins to significantly affect the potentials at the front of the device once full depletion is exceeded. As the

thickness of the sensor increases, the reverse voltage threshold V_{thr} at which the DDE barrier is lowered sufficiently to allow leakage current increases too. Since $V_{thr} \gg V_{PW}$, the voltage V_{thr} is expected to be proportional to the thickness of the active semiconductor, and device simulations confirm it. Measurements on devices with the same DDE but different thicknesses are in good agreement with these considerations. Figure 8 shows the measured reverse current in the FSI and the BSI variant of the same device. The ratio of the threshold voltages (measured at 1 nA reverse current) is approximately 7.2 V/5.0 V = 1.44, close to the thickness ratio of 18 µm/12 µm = 1.5.

Provided that there are no breakdown mechanisms outside the pixel area which can limit the applied reverse voltage, the principle of operation allows devices with very large active thicknesses to be realized. If over-depletion is required, the height of the DDE barrier can be made larger in order to accommodate it.

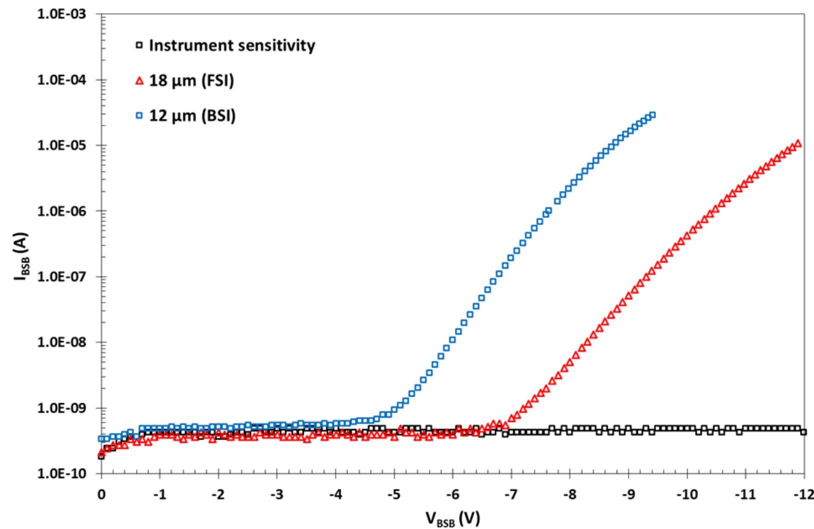

Figure 8 – Reverse currents in a medium DDE, high V_{pin} device in both FSI and BSI variants.

4.2 Photo response

The response of the sensor to visible light was obtained from the photon transfer curves (PTC) [7], which are generated by plotting the mean output signal and its variance from a group of uniformly illuminated pixels, for increasing levels of illumination. The PTC is sensitive to subtle aspects of charge collection and transfer, such as charge partitioning under the transfer gate and charge redistribution between adjacent gates in CCDs, manifesting as dips in the signal variance [8].

Figure 9 shows the measured PTCs of the same 10 µm DDE pixel variant in both FSI and BSI sensors, together with the reference which was made only in FSI variant. There are no significant differences between the PTCs, and no change is observed under reverse bias. The conversion gain of the sensors, which can be obtained from the slope of the variance at low signals, also did not change.

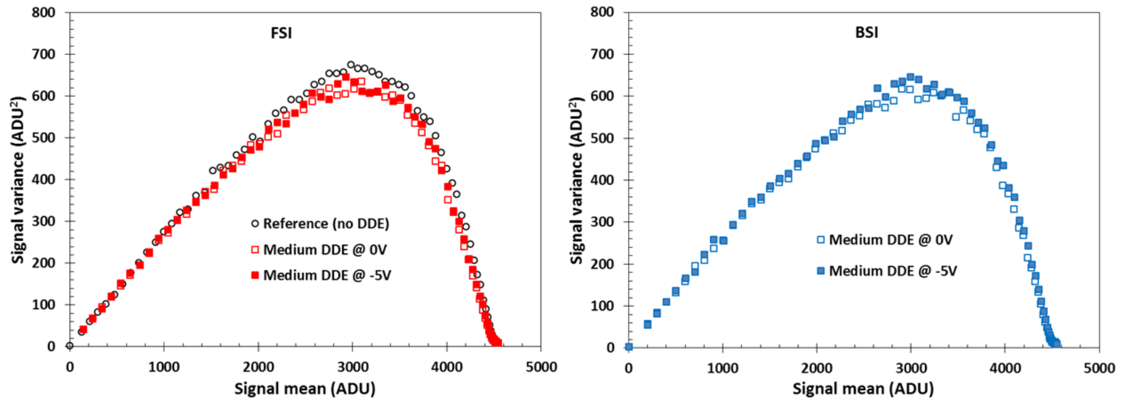

Figure 9 – Photon transfer curves of a 10 µm pixel in FSI and BSI chip variants at zero and -5V reverse substrate bias, obtained using frame differencing. The illumination is with a red LED with dominant wavelength of 624 nm.

The PTC data indicates that the DDE implant has no adverse effect on signal collection, as may have been anticipated from its proximity to the sense node and the PPD. Electro-optically most of the new 10 µm pixel designs are nearly identical to the reference, with the exception that full depletion is achieved via the application of reverse bias.

Measurements at high signal levels well beyond full well capacity show that the reduction of the pinning potential due to the accumulated charge does not cause sudden collapse of the potential barrier under the p-well [4].

4.3 Measurements of the depletion depth

The lack of substrate leakage current up to and beyond the estimated reverse voltage for full depletion is a strong indicator that this is indeed achieved. The device structure shown in Figure 4 ensures very good conductivity between the front side p-well contact and the backside, despite the high resistance of the epitaxial layer, due to the large area occupied by the peripheral p-well. Nevertheless, additional measurements were conducted to investigate the depth of depletion.

In FSI chips the dark current is dominated by the bulk silicon because the surface states are almost fully suppressed by the pinning implant [9], and the dark current increase is proportional to the depletion depth as shown in the diagram in Figure 10. Increasing the reverse bias beyond full depletion does not lead to further increase of the dark current, and the measurements in Figure 10 [4] confirm this.

In BSI devices the dark current is substantially larger, most likely due to the imperfect passivation of the back surface, and the method used for the FSI devices is not feasible. Instead, spot illumination at different wavelengths using a precision pinhole placed on the back surface of the device was used. The size of the image spot is affected by charge diffusion and can be used as an indicator of the extent of the field-free region in the device, as shown in Figure 11.

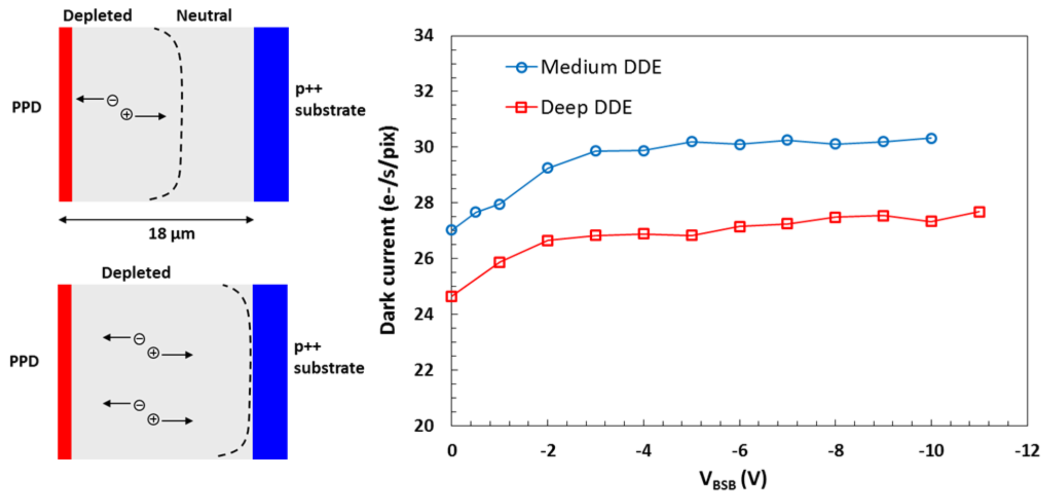

Figure 10 – Depletion depth measurement using dark current modulation.

Short wavelengths (for example 470 nm, 0.6 µm absorption length in silicon) are absorbed near the backside, and if there is no electric field in that region the charge will undergo some diffusion before collection. However, if the depletion reaches the back of the device there will be less diffusion, and the projected spot will appear sharper. Much longer wavelengths (for example 940 nm, 54 µm absorption length) are absorbed throughout the thickness of the device and the charge spread is much less sensitive to the extent of depletion, in particular in our relatively thin 12 µm BSI devices. From these considerations we expect the spot size to be less sensitive to the depletion depth (and by proxy on the reverse bias) as the illumination wavelength increases from 470 nm to 940 nm.

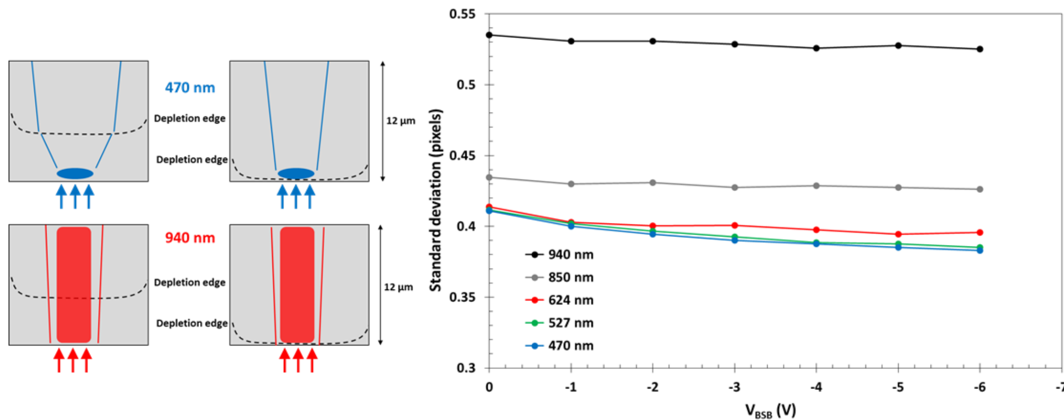

Figure 11 – Measurement diagram (left) and spot illumination size versus reverse bias in a BSI sensor with 10 µm pixels for different light wavelengths (right). The pinhole diameter is 10 µm.

Figure 11 shows the measured spot sizes at 5 different wavelengths as a function of the reverse bias for a sensor with 10 µm pixels and medium DDE. The cross section of the spot image in the horizontal direction was fitted with a Gaussian curve and the standard deviation plotted.

The data is consistent with an increase of the depletion depth with the applied reverse bias V_{BSB}. The size of the image spot decreases and levels off as the depletion edge reaches the back surface for red, green and blue wavelengths, for which this method is most sensitive. The change

of the spot size is less prominent for the longer wavelengths, as expected and discussed above. The larger initial sizes for 850 nm and 940 nm are most likely due to reflections from the metal layers on the active side of the device because near-IR light reaches them without much attenuation.

5. Conclusions

The characterisation results from the newly developed, reverse-biased PPD CMOS image sensor show successful operation. The additional DDE implants suppress the parasitic leakage current through the substrate, which is present in standard, non-modified pixels. This allows sufficient reverse bias to be applied to reach and exceed full depletion of the active semiconductor material. The photo response of the new pixel designs is nearly identical to the reference non-modified pixel. Full depletion of the sensor has been demonstrated in both FSI and BSI chips using two different methods. The first prototype has been made on 18 μm thick epitaxial silicon for direct comparison with other CIS, however the principle of operation is not limited to a particular thickness.

This development has the potential to greatly increase the quantum efficiency of scientific PPD CIS at near-infrared and soft X-ray wavelengths, due to the ability to realise sensors with sensitive thickness in excess of 100 μm. Likely applications are in sensors for astronomy, Earth observation, hyperspectral imaging, high speed imaging, spectroscopy, microscopy and surveillance, as well as for soft X-ray (<10 keV) imaging at synchrotron light sources and free electron lasers.

Future work will include design and manufacture of a second generation sensor on a much thicker, high resistivity bulk silicon.

Acknowledgments

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