Universitat Autònoma de Barcelona

Inkjet-Configurable Gate Arrays. Towards Application Specific Printed Electronic Circuits

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"An expert is a person who has made all the mistakes that can be made in a very narrow field"

Niels Bohr

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Abstract

Over the last decades, Organic Electronics has been emerging as a multidisciplinary and innovative way to generate electronic devices and systems. It is intended to provide a platform for low-cost, large-area, and low-frequency Printable Electronics on a variety of substrates, including flexible plastic substrates. Just as the first information revolution caused by integrated silicon circuits, PE is expected to cause another revolution characterized by the distribution of information systems in all aspects of life.

Although the integrated circuits, based on Organic Thin Film Transistors (OTFT), are not meant to compete with the silicon-based high-end industry, their performance have already reached to a level enabling the use of organic technology to an ever-increasing number of emerging applications, such as flexible optical displays, sensors, and low-end microelectronics.

Currently, most of the digital integrated circuits are yet designed by specifying the layout of each individual transistor and their interconnections. Full-custom design is extremely labor-intensive, time consuming for complex circuits and it requires advanced computer software in the design process, and several expensive mask sets in the fabrication process. Besides, taking the soft and hard faults at transistor level into account, the yield at system level is expected to be very low, since failure of one transistor causes the entire circuit to fail. This is more important for technologies based in non crystalline materials (such as silicon) in which deposition and layer formation is more irregular. On the other side, organic electronics is more complex than Printed Circuit Boards (PCB) in the sense that these do not include active devices and do not reach high integration level. Furthermore, similar to any new-born technology, the performance of organic electronic circuits is degraded due to some limitations in technological and materials sides. That being said, the question arises as to whether circuit design techniques can be employed to compensate these bottlenecks so as to meet yield and performance requirements.

The work presented in this thesis contributes to overcome the above-mentioned issues by proposing the novel concept of Inkjet-configurable Gate Array (IGA) as a design-manufacturing method for the direct mapping of digital functions on top of new prefabricated structures. IGA brings together the advantages of semi-custom gate array methodology, field-configurability, and fault-tolernace, and adopt it to Application Specific Printed Electronic Circuit (ASPEC), which is the equivalent term to Application Specific Integrated Circuit (ASIC), but for PE.

This alternative has two main advantages. Firstly, it allows implementing individual circuit personalization at a very low cost through the best use of additive mask-less digital printing techniques (i.e. Inkjet, Superfine Jet, and etc.) "in the field", thus avoiding the need for One Time Programmable ROM-like (or E2PROM) devices. Secondly, fault tolerance technique allows the adoption of a failure map to use only working transistors for circuit implementation, thus, it helps to obtain high yield circuits out of mid-yield foils.

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Chapter 1

INTRODUCTION

The semiconductor industry's ability to follow Moore's Law [1] has been the engine of an efficient and effective cycle: through transistor scaling, one can obtain a better performance-to-cost ratio of products while enabling the production of more complex circuits on a single semiconductor substrate. This induced an exponential growth of the semiconductor market and allowed further investments in new technologies, which will fuel further scaling.

From a technology perspective, the continuous increase in the integration density has been possible through a dimensional scaling, whose benefits in performance can also be explored. According to Dennard *et al.* [2], by downscaling the critical dimensions on a given technology node while keeping the electrical field constant, one can obtain, at the same time, a higher speed and a reduced power consumption of a digital MOS circuit. These two parameters, along with the integration density, became driving forces of the microelectronics industry and the related disruptive changes in different application fields such as the digital economy, the smartphones, the automotive industry, and etc.

It is predicted that the trend towards miniaturization and its associated benefits in performance will continue, while performance can always be traded against power depending on every application domain although the fabrication costs strongly increase (and the number of technology investors is being limited). This direction for further progress is labeled as More Moore. Anyway, we are now in a point in which it seems that we are at the soft landing of this empirical law and thus there is a search for new technologies able to continue promoting disruptive changes and the economy growth.

A novel perspective arises for functional diversification of semiconductor-based devices to complement the integrated systems. Heterogeneous functionalities, which do not necessarily scale according to Moore's Law, but provide additional value in different ways, tend to migrate from the system board-level into the package or onto

the chip. Consequently, in view of added functionality, this trend is being designated More-than-Moore.

More-than-Moore technologies do not constitute an alternative or even competitor to the digital trend as described by Moore's Law. In fact, it is the heterogeneous integration of digital and non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields. The main focus of this thesis is on Printed Electronics (PE) as a comprehensive More-than-Moore technology, exploring the possibility of hybrid fabrication processes, such as conventional clean-room approaches, together with the benefits of digital printing techniques.

This chapter introduces the concepts regarding PE, from devices to systems, then places PE compared to conventional silicon-based electronics. High-throughput Roll-to-Roll (R2R) technologies, clean-room processes, and digital printing technology are discussed later, and the applications and challenges concerning PE are presented. Finally, the objectives and organization of this thesis are introduced.

1.1 Printed electronics: from devices to systems

Monolithic, heterogeneous integration of non-digital components into one coherent chip is both difficult and expensive, as is even with different silicon technologies (digital, analog, power, MEMS, SRAM, DRAM, NAND flash, NOR flash). The difficulty arises from the incompatibilities of the functional materials and of the various fabrication processes required to optimize each type of device in the most efficient way. In addition, while many new molecular and nanoscale components are under investigation, their homogeneous and heterogeneous integration into higher-order two- and three-dimensional structures and devices will not be straightforward with the current standard fabrication (photolithographic) processes.

As the device sizes shrink and as the functionality of heterogeneous integration (bringing many devices of different origins together on a substrate or packaging) gains importance, high-throughput pick-and-place techniques at low temperature compared with current technologies, capable of handling many components, will become critical. Thus, the need for economically viable technologies, which provide heterogeneous integration of individual components on a host substrate with required accuracies and yields, is inevitable. Furthermore, current trends are that those substrate should be thin (and even flexible).

Besides, for applications that require the electronics to be distributed over a large area and/or flexible substrates (i.e. biosensors, wearables, future automotive, and etc.),

the current scaled high-performance silicon technologies are not very applicable. This is because of the high cost per unit area for processing and manufacturing, as well as the high cost of single-crystal wafer substrates.

Therefore, the trend towards highly cost-efficient electronics for low-end products, which are simultaneously available in great numbers, ultimately leads to a new functional diversification technology which is mass-printed on flexible surfaces by using organic materials. For example, Radio Frequency Identification (RFID) tags or flexible Organic Light Emitting Diode (OLED) displays, which compete with barcode or Liquid Crystal Display (LCD), might be easier to adopt if their cost or functionalities were appealing to the end user.

Printed electronics (PE), also known as "Organic Electronics (OE)", "Flexible Electronics", "Plastic Electronics", "Large Area Electronics", supposed to be a new concept in electronic technology. It is based on the combination of a new class of materials, substrates, and large area deposition and patterning techniques to enable new applications not possible or not affordable with silicon-based electronics. In general, PE refers to electronics that are based on materials that can be deposited onto a surface using printing techniques, extending functionalities to both flexibility (due to non-cristallinity) and low-temperature materials. The basic elements of PE can be summarized as printing engine, materials or inks for printing, and substrates to be printed on.

Comparing to conventional electronics, PE has an entirely different feature set that will make it applicable to a novel range of uses that is quite distinct from the range of silicon applications. Its applications are demonstrated in flexible displays and lighting [3]–[7], energy harvesting [8]–[12], sensors [13]–[16], Internet of Things (IoT) applications [17], [18], and healthcare applications [19]–[22]. The main goal of PE is to create new mass markets for low-cost, flexible and large area electronics, without attempting to compete with silicon-based electronics that is a hopeless endeavor.

1.2 Printing technologies: throughput vs. resolution

Printing technology taking its heritage from the graphic arts and newspaper industry can be adapted in principle to the production of large-volume organic electronics. A broad range of deposition and patterning techniques can be considered for printing of functional materials, same as in the printing industry. The existing technologies range from batch, clean-room processes to high-throughput mass printing processes. All of them differ strongly with regard to resolution, feature size, substrate, physical and

chemical properties of functional materials, deposition techniques, and Non-Recurring Engineering (NRE) costs.

According to the specific requirements of a particular system, PE applications may be better addressed by one of the existing technologies, in which manufacturing costs is appealing to the end user. Each process has its own strengths, e.g. screen printing [23] is excellent for stacking multiple thick films, while gravure [24] combines high throughput with robust printing forms and can deliver homogeneous thin films. Offset [25] combines high throughput with small feature size, but formulating suitable functional inks has proven to be a major challenge. Figure 1.1 represents the throughput versus resolution for obtaining premium quality production processes (Source: [26]).

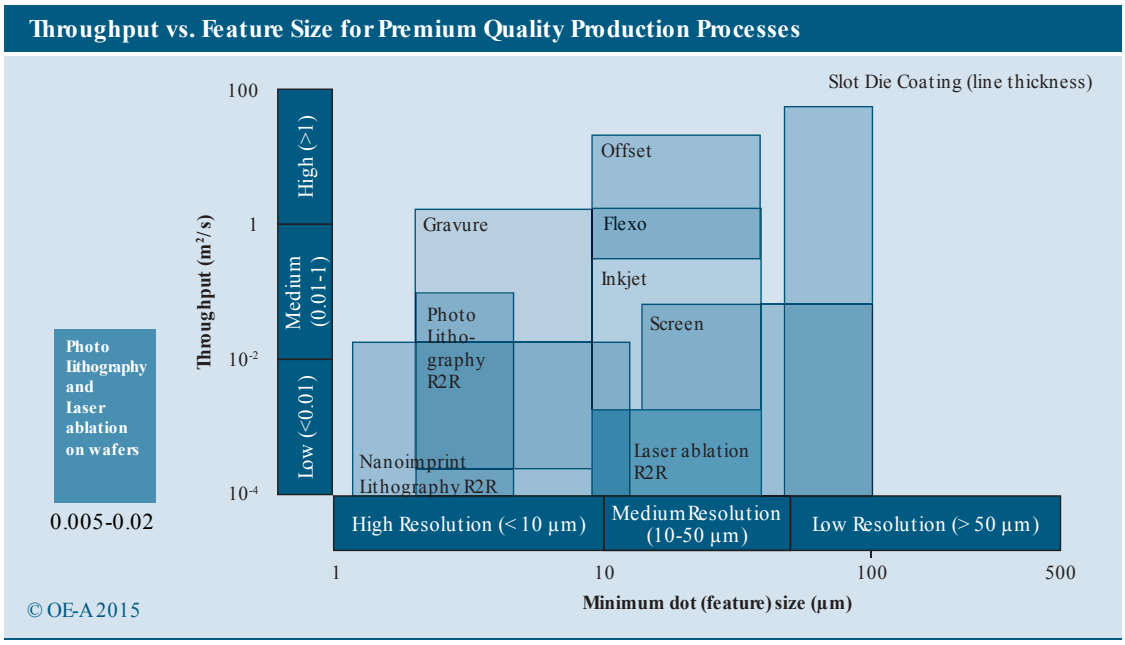


Fig. 1.1 Resolution and throughput for highest quality levels of common deposition and patterning technologies

For high-end applications, where performance and miniaturization play important roles, clean-room processes with high lateral resolution (smallest feature that can be printed) are the best candidates. Vacuum, evaporation, and photolithography are further deposition and patterning techniques. Despite a relatively high production cost, high resolution can be achieved by vacuum deposition and/or spin coating followed by photolithography and wet or dry etching.

In contrast, for low-end applications, where large-area, flexibility and low costs are important, conventional mass-printing technologies, such as flexographic, gravure,

offset, and screen printing can be used. These fully-printed technologies comprise continuous, automated mass-production compatible printing and coating techniques on flexible substrates. Also, they are compatible for conversion to in-line Roll-to-Roll (R2R) processes, which enables high throughput by depositing square meters of substrates per second.

The choice between clean room and printing technologies is not always an either-or decision. Hybridization, which is the combination of high resolution clean-room processes with high-throughput large-area printing techniques, appears to be one of the most promising approaches for further market penetration as it has been for Printed Circuit Boards (PCB). This allows combining with some amount of silicon for specific functions in order to use the strength of each technology and bring the flexibility feature to the high performance silicon-based electronics that instead of PCBs, can include sensing feature and/or devices (active and passive). This has become an attractive topic over the few years and promises to be a platform for new products in the near term. Thus, depending on the requirements of PE applications, the key factor in system hybridization is to find the best relative portion for each process and materials, driven by the application requirements.

1.3 Digital printing technology

Digital printing, which refers to the process in which computer-controlled printers are used to deposit a given material onto a substrate, has been used as reliable research tool for organic electronics. In contrast to mask-based analog printing, in which screens and plates are used for patterning the desired structures, digital printing is a mask-less process, making it cost-efficient, faster, and more accessible than its counterpart.

Regarding PE, the desired printing patterns are defined through EDA tools allowing rapid prototyping of several geometries. It also enables variable printing (modification of the pattern used for each impression) since no mask or plate is needed, and can thus correct in-line for distortion, leading to short turnaround time. Figure 1.2 compares digital and analog printing process flows.

As an additive manufacturing process, which is based on layer-to-layer registration, material loss is minimal and no functional materials have to be removed as in conventional subtractive processes. This is also opening up new possibilities for conformal electronic circuits and systems embedded in advanced 3D structures. Additionally, it allows the use of highly conductive nano-particle inks, which provide more precise and higher resolution.

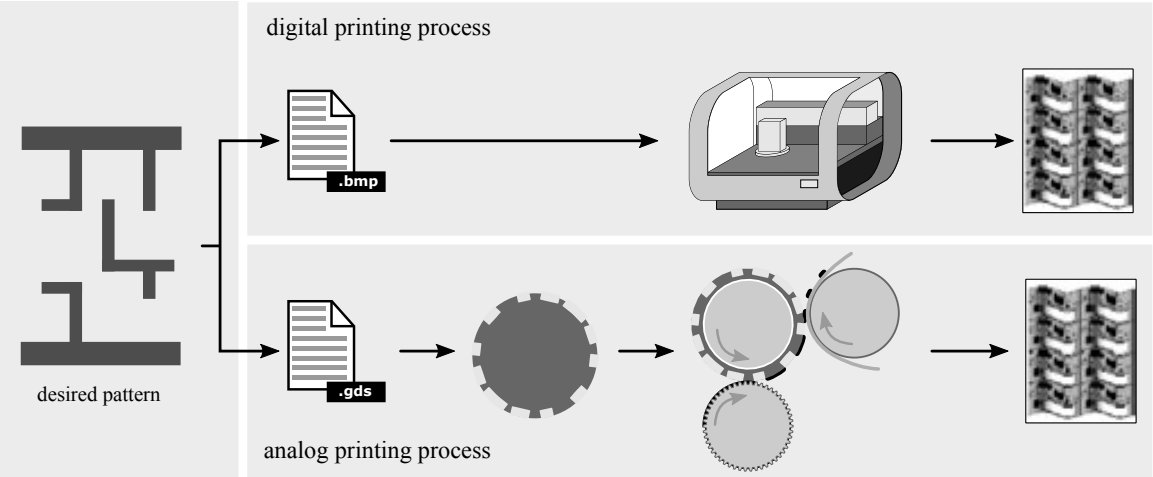


Fig. 1.2 Digital printing flowchart

Progress in increasing the resolution and registration is a critical step to dimensional scaling of organic electronic circuits, which could be of similar importance to the scaling of photolithography processes for silicon electronics. The equipment developers continued providing thinner print heads, which are starting to enable features in the order of few microns, and throughput is improving with the development of reliable multi-head printers. Also, surface energy patterning can be a key factor for obtaining high quality small features. As a counterpart, digital printing depends on jetting material, what means that the printing cannot be done for a given material in a single step (as in Photolithography). Anyway, industrial inkjet is a main trend in newspaper industry and multiple drops can issue materials in parallel.

That being said, a number of features have made digital printing the best candidate for individual personalization of electronic circuits: it is mask-less and computer-controllable; and there is a trend towards down-scaling printing features. The capability of building individual circuits with technological steps simpler than clean-room photolithographic ones is opening a concept similar to field-configurability for PE circuit design – personalizing a pre-fabricated device in the field without disassembling it or returning it for its manufacturer. Digital printing could be used for wiring new metallic layers on top of the circuits to build PLA-like circuits [27], [28], or program One Time Programmable memories (OTP-ROM) [29]. This examples are all subjected to the current low resolution of digital printing technology and improvement of this property is key in this thesis.

1.4 Business models

Printed, flexible and organic electronics market has gained remarkable increase in the demand at present. It is making up around $26.5 billion currently and its value is estimated to reach $40.2 and $69 billion by 2020 and 2026 respectively, the majority of that being OLED display and lighting [30], [31].

As More-than-More products with integration of heterogeneous functionalities start rolling out, two different business models have emerged, which are vertical and horizontal. In the vertical business model, the commercialization of an application, its design and fabrication are all provided and controlled by one single company. The main advantage of this approach is that the industry can optimize the fabrication process to the market application, although this tends to be narrow and thus, related technology, is difficult to apply or reuse for other application domains.

However, since vertical business model is application oriented and the entire system is designed and manufactured for a particular application by a particular vendor, the user is entirely dependent on the vendor for improvements, enhancements, or upgrades of the devices and systems. The major drawbacks to the vertical approach will only have an effect over time, as users seek to update or enhance their systems. But limitations in how quickly a vertical business model can embrace new opportunities may also limit how quickly the market grows as a whole.

Printed electronics currently has a fab-based application-oriented vertical business market, in which there are several printing technologies providing different printers, inks, and substrates, while there is a limited application domain. Although there are different levels of accesses such as design kits, CAD tools, and etc., they are all restricted to internal use of the technology provider.

On the other hand, there is a motivation behind a horizontal model to foster growth and innovation in the industry by allowing multiple providers to work with a common framework. The idea is that by making the gateway and cloud resources something that can be assumed to be in place and have known and open functionality, innovators can concentrate their efforts on creating products and services. These products and services can more easily share information and resources, if they work on a common framework. The horizontal approach makes innovation easier and allows rapid proliferation of new applications and businesses, but it needs to gain considerable traction before it can pay off on its promises.

In silicon-based microelectronics industry, as one of the best examples of horizontal business model, there is a clear design and fabrication methodology, large market, clear providers, and good value chain. Therefore, going from a concept to application

implementation is something predictable, hence there is a large domain of ideas and applications in different markets. The number of fabs/foundries is limited and reducing every day, and the reason is that the most portion of the IC fabrication is in the hand of the big players in Taiwan or United States, with huge facilities and expensive investments. But, the number of chip vendors is high and increasing, which means that the chip vendors are not the foundries, but they just order chips according to their application specific product.

That being said, we expect the evolution of fab-based printed electronics with its application-oriented vertical business model towards the advantages of the microelectronic industry horizontal business model, so that the application enablers meet the technology providers, for better interaction and widening the application domain, hence the technology success.

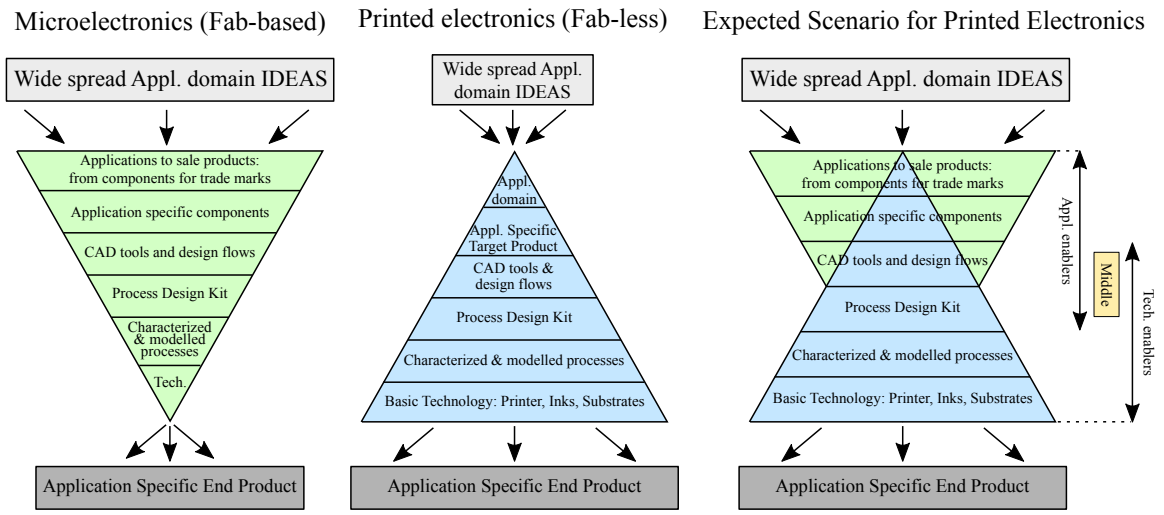


Fig. 1.3 Microelectronics vs. Printed electronics: ideas to end products

1.5 Applications and Challenges

There are several reasons why PE is gaining considerable attention. The environmentally friendly printing processes can be applied to many different kinds of substrates, and also three-dimensional printing is possible. This enables the changing of the whole system of producing electronic devices, including the design and manufacturing phases, material selection, and device structure and architecture. Besides, printing process is potentially cost-effective and much faster than wafer-based fabrication in silicon electronics (partly because it uses a reduced number of layers). Complete system

integration can be realized as a part of other means by printing them on the printer, which enables the integration of devices with multiple functionalities (logic, memory, battery, display, sensors, etc.). This also allows printing electronics on large surfaces not restricted to the wafer size. The capital investment cost for PE is some orders of magnitude lower than current conventional silicon fabrication.

The applications of OE have been grouped into five main clusters: (i) Flexible and OLED displays; (ii) Organic Photovoltaic (OPV); (iii) OLED lighting; (iv) Electronics and components (including printed memories, RFID tags, batteries, passive and active devices and logics); and (v) Integrated Smart Systems (ISS) like smart objects, sensors and smart textiles. Figure 1.4 shows the 6th edition applications roadmap, which is published by organic electronic association OE-A (Source: [26]). In the following, each of these clusters is slightly detailed, with special attention to electronics and components, the main focus of the thesis.

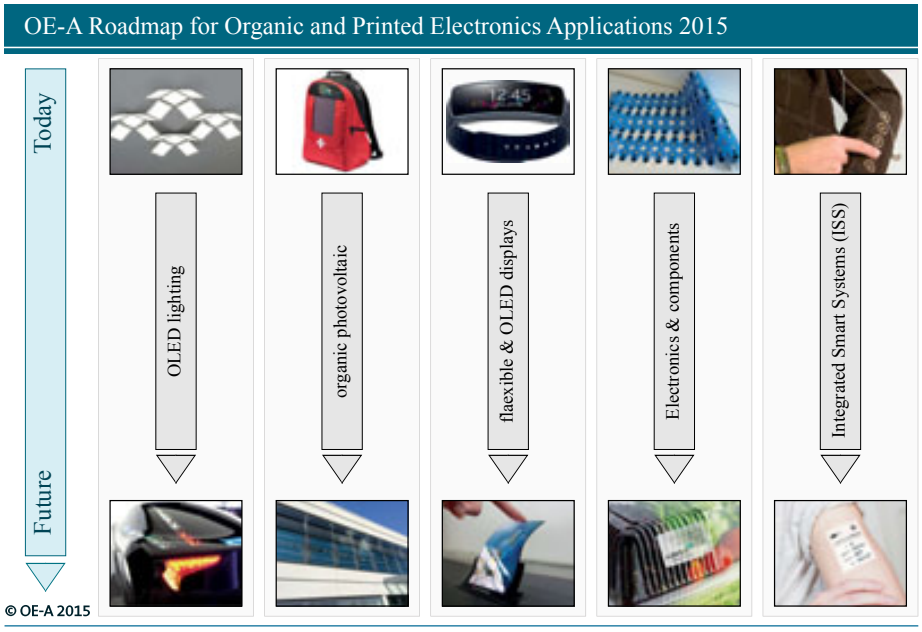


Fig. 1.4 Overview of the 6th edition of OE-A roadmap for OE/PE applications

1. Flexible displays can dispense with some key limitations of current flat displays, such as the presence of breakable and heavy glass and inability to be bent, rolled or used with other than flat form factor. Additional opportunities are expected in the future, when transparent OLED displays become commercially available, e.g. for mounting in windows or glasses. All of the OLED displays have in common the use of an Active Matrix array of Thin Film Transistors (AMTFT), which acts as a backplane to control each pixel individually [32].

2. OPV is an emerging, clean energy technology enabling a wide application range such as lightweight, flexible and conformable power sources suitable for wearable and mobile devices. OPV devices typically comprise a substrate, semi-transparent, and photo-absorbing organic layers.

3. OLED lighting is seen as the most promising approach for future lighting due to superior energy efficiency, absence of hazardous materials, flexible form factor, and high durability. The OLED products offer novel features such as being large-area, flexible and very thin, high efficiency and variable color. Beside white emitting OLED for general lighting, monochrome OLED lamps (for automotive or signage applications) are growing in importance.

4. Electronics and components have a set of different driving forces in Internet of Things (IoT) era for PE. This requires seamless integration of relatively simple electronics, both for digital and analog ICs. Organic active devices, such as Organic Thin Film Transistors (OTFT), diodes, and logic circuits, containing an organic semiconductor are essential part of smart objects and integrated systems. The coupling of printed sensors, batteries, displays and memories – with printed transistors to drive the logic – is probably the most important trigger for many future applications of printed electronics.

   In a detailed perspective for digital circuits, that are capable of processing digital information, transponder circuits for RFID tags are one of the targeted applications. In this case, Boolean information from a memory is read out and prepared for radio frequency transmission to a base station. Furthermore, the rows of active-matrix displays are addressed one-by-one at a constant speed, resulting in the refresh rate of the display. The row-driver chip is a digital circuit that sequentially addresses a row line and comprises of shift register and decoders, which are implementable by PE circuitry.

   Concerning analog circuits, they are typically used for conditioning, filtering, and amplifying analog signals, or for converting them into a stream of Boolean digits. For example, the output signal of a sensor has typically low voltage range. Then, it must be amplified into a large swing signal through a front-end amplifier. Afterwards, the amplified version of the signal needs to be processed and stored by a digital processing unit. Therefore, an Analog-to-Digital Converter (ADC) needs to be employed in the next step to convert the continuous signal into a set of discrete values.

Another key element that can enable complex printed circuits is memory. Data storage is essential in many devices designed for mobile use, such as in sensors and actuators, and in wireless communication devices. The use of non-volatile memory would reduce the power consumption. Combining logic and memory can enhance the capability of printed electronics. [33], [34]

5. ISS bring together multicore functionalities to perform complex, automated tasks without the need for external electronic hardware. Integration of sensors, transistors, memories and batteries onto the same substrate is realized by functional printing. The importance of sensors in organic and printed electronics is growing due to the fact that they will increase the range of functionalities of products and also because they can use other previously developed printed devices such as OLEDs and photodiodes. Printed sensors are starting to replace conventionally manufactured sensors and being truly a class of smart objects. By taking advantages of flexible electronics, significant advances are being made in smart textiles; hence functionality is already being embedded into clothing.

A common feature of all future generations of PE products is that the complexity and oversize of logic circuits is increasing. In certain cases, future applications include millions of transistors and will need to operate at frequencies suitable for RF communication. Also, there are high performance devices that should fit into small and smaller areas, being integrated together with several electronic devices. In this case, clean-room processes, like photolithography, are required to satisfy the need for high density and high frequency features, while the NRE cost would be an obstacle for fabricating many individual chips.

Some other products will combine various digital and non-digital functionalities and electronic devices like circuitry, power supply, sensors, displays and switches. Furthermore, some high performance components will have to be placed precisely over large areas, up to few square meters. In this case, wafer-level processing will not be a commercially viable approach, and hybridization technologies should be adapted to pick-and-place the high-performance devices and circuits onto a large-area printed substrates.

However, there are several limitations and challenges for developing high performance organic devices and circuits, which are related to either material or technological processes. Electronic performance of organic electronic devices is limited by the intrinsic semiconductor properties. Another big challenge arises when making materials that combine high uniformity with high mobility, capable of industrial quantities with

reliable quality. Low charge carrier mobility of existing organic materials (polymers and small molecules), especially for n-type organic semiconductors, is also a limitation for implementing organic transistors and complex circuits.

On the fabrication side, resolution, uniformity, reliability and yield are still key challenges in mass production of robust and scalable systems. For instance, low resolution and registration in high-throughput processes is a big barrier to achieve the expected down-scaling of devices in similar way to that observed in silicon. Furthermore, due to the process variation in these technologies, the overall yield and reproducibility is low. Adopting silicon-based circuit design methodologies to PE is also challenging when considering technology limitations, material evolution and printing processes. Thus, the link between materials, printing processes, and design methodologies is crucial for the technology to succeed.

Due to the above-mentioned limitations, PE devices and circuits are suffering from some drawbacks, such as low performance, both in device and system levels, high process variability and low or mid-yield. Here, the question arises as to whether circuit techniques can be employed to compensate these bottlenecks so as to meet yield and performance requirements.

1.6 Thesis objective

The main objective of this thesis is to provide a new circuit implementation technology (with its related methodology) that brings together two well-established concepts from ASIC industry: (1) gate array, which separates master slice fabrication from functional personalization steps; and (2) field-configurability feature, through the use of digital printing techniques to personalize individual circuits.

Gate arrays are prefabricated master chips with no particular function, in which the personalization is accomplished by adding the final metal layer(s) late in the manufacturing process (in a second phase of production). Besides, field configurability allows the designer to customize pre-fabricated devices in the field (at home) without disassembling or returning it to its manufacturer.

In the way to combine the gate array design methodology with field-configurability concepts for PE, a hybrid approach is proposed to merge the benefits of clean-room and digital printing processes. For that, master chips can take advantages of high-yield clean-room processes to enable pre-fabrication of high-performance basic devices (transistors). Following that phase, mask-less digital printing techniques, such as inkjet

printing can be employed in the metallization step (second fabrication phase). This brings the idea of Inkjet-configurable Gate Arrays (IGA).

The first advantage of this method is increasing functional capabilities by using digital Drop-on-Demand (DoD) printing to customize every individual fabricated master slice (master foil) to its unique functionality. ASIC-oriented field-configurable devices are commonly personalized by means of fuses and antifuses, Static Random Access Memory (SRAM), Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM), and flash memories [35], while gate arrays and Sea-of-Gates (SoG) adopt mask-based, photolithography techniques. The use of additive mask-less printing techniques enables quick and accurate placement of wires and interconnects at a very low cost, thus avoiding the need for EEPROM devices or a new mask for functionality personalization.

However, this combined mask-based and mask-less hybrid approach intrinsically turn their different printing resolutions into a big challenge. Clean-room processes, such as photolithography, are able to follow miniaturization trends with much higher pace than digital printing techniques. This leads to printed structures with very different minimum features, possibly an order of magnitude.

A demand addressed in this work is to study circuit design methodologies and fabrication technologies to make them compatible in respect to their resolution when bringing them together onto the same substrate. For that, several interconnection strategies were explored, in order to achieve such compatibility while optimizing circuit density, material usage, and electrical properties.

Printed electronics is also suffering from low/mid yield at device level, which means that a failure in one single transistor will lead the complete circuit to fail. There are a number of ways to address this issue from either organic materials perspective or technology side. The PE community is already going into that direction by improving the quality and electrical properties of organic materials, as well as by evolving the fabrication processes.

The second advantage of the proposed methodology is obtaining high yield at system-level out of mid yield foils at device-level. For that, we are adding fault tolerance technique to the concept of inkjet-configurable gate array. Fault tolerant technique allows the adoption of a failure map to use only working transistors when personalizing the system to a desired functionality.

1.7 Thesis organization

The organization of this thesis is as follows,

Chapter 2 reviews all basic and established knowledge about integrated circuit design methodologies and full-custom and semi-custom level that is needed to understand the concepts presented in this work. Please, consider skipping this chapter if you are familiar with ASIC-based circuit design methodologies.

Chapter 3 presents in a bottom-up approach an evolutionary line over the main PE state-of-the-art concepts. For that, some previous and recent works are summarized concerning technology and materials, organic transistors and digital cell design.

Chapter 4 addresses the interaction between design and technology and the necessary information for a seamless bridge. This chapter highlights three main contributions; firstly, some critical technology information is automatically extracted by using a parameterized approach. Secondly, different layout design styles for OTFTs are proposed and compared according to their electrical properties and variability. Finally, some elementary logic gates are developed for a photolithography process.

Chapter 5 introduces Inkjet-configurable Gate Array (IGA) concept as the main contribution of this thesis. The generation of the IGA bulk is explained as the first step, and then I present the Drop-on-Demand configurable methodologies for metallization of IGAs, as the second step. Then I introduce IGAs for different purposes (yield and/or functionality personalization), as well as presenting some fabricated samples, and finally, some implemented circuits on IGA bulks are provided.

Chapter 6 provides the main conclusions, summarizes the contributions of this work and presents the intended future works.

Chapter 2

BACKGROUND: ASIC DESIGN METHODOLOGIES

Integrated Circuit (IC) is a set of electronic devices on a die, made from semiconductor material, normally silicon wafer, each of them holding hundreds of dies. Circuits are built up in many overlapping layers of materials like polysilicon, aluminum, and silicon dioxide, each defined by photolithography. Patterns must be etched into the material to create transistors and interconnections on the surface of the wafer. Etching creates microscopic patterns on the wafer's surface, and is the true magic of IC technology because it delineates fine geometries using an optical process, forming very small features.

Application Specific Integrated Circuit (ASIC) is a subset of Integrated Circuits (ICs) that are designed and customized for a particular function specified by the owner of the ASIC for its sole use, rather than intended for general-purpose (microprocessors, memories, and etc.) use. ASIC can be software programmable to perform a wide variety of different tasks, while being a digital circuit built up with successive mask layers to meet specifications set by a specific function.

IC design (organic/inorganic) is an interactive process with given trade-offs between die area (highly related to cost), complexity, performance (speed, power, etc.), yield, energy efficiency and design time. Considering the trend toward steadily miniaturization and enhanced complexity as predicted by Moore's law, the target for the development of ASIC is to optimize the involved fabrication processes regarding to the above-mentioned criteria what leads also to technology specialization.

There are several types of existing ASIC design methodologies, either of which is prone to some cost functions. In this chapter, an overview of ASIC design methodologies with their advantages and disadvantages is presented. Figure 2.1 shows the evolution of

microelectronics circuit design methodologies from technology-dependent full-custom and cell-based design, to technology-independent re-usable design, during its evolution years. It also indicated the complexity of final prototype in respect to the transistor counts [36].

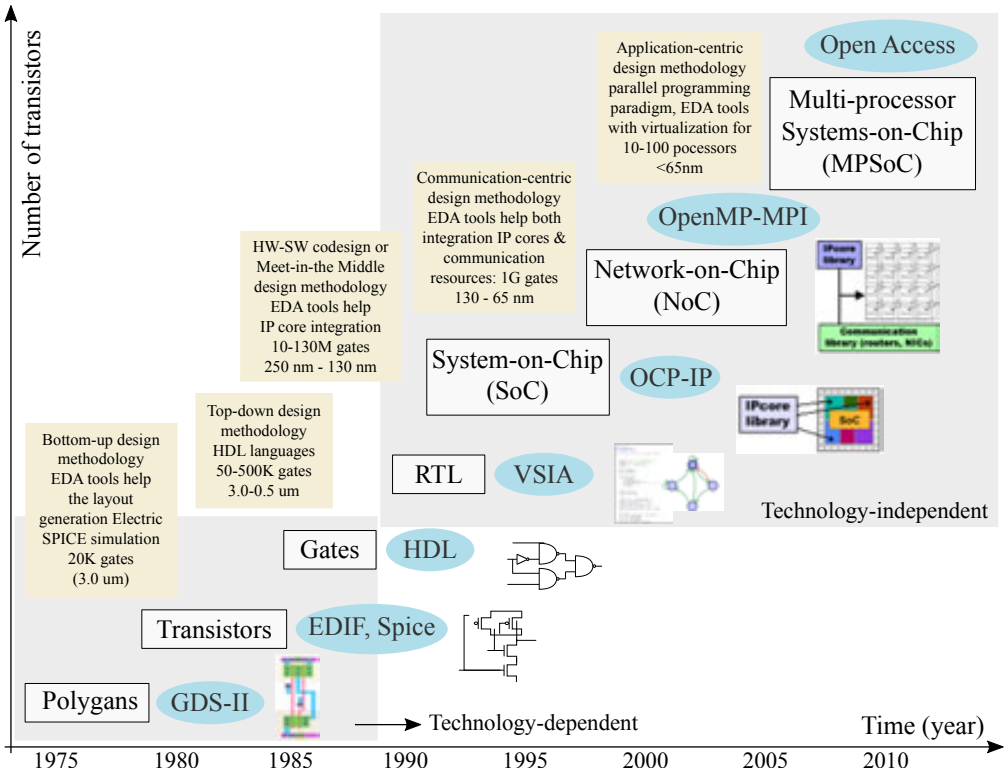


Fig. 2.1 Microelectronic evolution: from geometries to systems

2.1 Full-custom

The oldest and most traditional circuit design technique is termed full-custom, in which a designer sits in front of a graphics display running an interactive editor and pieces designs together at the geometry level one rectangle at a time. This work is sometimes called polygon pushing and the variation of custom mask design is called symbolic layout. In this methodology, the layout of each transistor and the interconnections between them is specified.

Full-custom design is the lowest abstraction level from design point of view, which uses the basic set of information (electrical parameters and models, geometrical design rules, and technology layers) to design, simulate and draw circuit. Rather than dealing

with rectangles and polygons on various mask levels, the primitives such as transistors, contacts, wires, and ports (points of connection) can be used in custom design.

Custom design is worthwhile pedagogically because it completes the link between technology and design: from technology layout transistors, cells, and systems. Its main advantage is maximized performance and minimized area of the chip, but it is extremely labor-intensive and risky to implement and several mask sets are required in order to transfer the circuit designs onto the wafer. Due to area and performance optimization in custom design, the scope of the methodology covers the key design domains of analog and RF, custom digital, and cell libraries for standard cell libraries.

2.2 Cell-based

Cell-based design methodology is a semi-custom method of designing ASICs with digital logic cells. The basic building blocks of a chip are pre-designed and pre-characterized (standard cells) or pre-fabricated (gate arrays). This is an example of design abstraction, where a low-level integration is encapsulated into abstract logic representation. The cells are placed in appropriate positions, then their interconnections are routed. Foundries and library vendors supply cells with a wide range of functionalities such as:

1. Small-scale integration (SSI) digital logic (NAND, NOR, XOR, AOI, OAI, inverters, buffers, registers) and analog cells (current mirrors, opamps, ADC & DAC, and etc.)

2. Memories (RAM, ROM, CAM, register files), usually built out of compilers for structures of elementary cells.

3. System level modules such as processors, protocol processors, serial interfaces, and bus interfaces, known as IPs and built out of two previous elements.

4. Possibility of mixed-signal and RF modules

A typical standard cell library contains two main components:

1. Library database that consists of a number of views including layout, schematic, symbol, abstract, and other simulation views (behavioral, electrical, adn etc.). They can be provided through various information means including the Cadence LEF format, and Synopsys Milkway format. LEF file contains reduced information about the cell layouts, sufficient to run automated "place and route" tools.

2. Timing abstract, which is typically in liberty format, to provide functional definitions, timing, power, and noise information for each cell.

Standard cells are fixed-height, variable-width with power and ground routed respectively at the top and bottom of the cells. This allows the cells to be abutted end to end and to have the supply rails connect, easing the process of automated digital layout. The cells are typically optimized full-custom, in order to minimize the delays and area. This design methodology can deliver small, fast, and low-power chips to produce the custom mask set. Therefore, it is only economical for high volume parts or when the performance commands a lucrative sales price. As compared to full-custom design that required even higher costs (and thus usually volume), it offers much higher productivity because it uses pre-designed cells with layouts.

2.3 Gate arrays and sea-of-gates

Designers typically strive to keep the NRE cost as low as possible. The Gate Array (GA) design alternative is a semi-custom prefabricated silicon chip, containing a common base array of transistors or logic gates with no function. These logic blocks are placed at regular predefined positions, surrounded by interconnect resources, and are kept unconnected. Later on, creation of a circuit with specific functionality is accomplished by altering the metallization (metal and via masks) layers that is placed on top of the arrays.

The key feature in GA design methodology is that the master slices are usually prefabricated and stockpiled in large quantities regardless of the customer orders. The design and fabrication according to end-user application is realized by using a reduced metallization step(s), which alleviates the often prohibitive time and expense of multiple mask set designs in cell-based and full-custom design. In this way, the costs of the shared masks are spread over all applications and only the cost of the final customization mask is additional.

A particular subclass of GAs is known as a Sea-of-Gates (SoG) chip (channel-less gate array), in which rows of nMOS and pMOS transistors are arrayed in the chip. Each logic row consists of an n-row and p-row. Personalization of SoG structure commences at contact and metal1 masks, and can continue up for all metal layers available in the process. Figure 2.2 depicts a sea of gates manufacturing steps.

There are two basic limitations of gate arrays: firstly, the designer or user cannot customize the chip in-the-field and the customization is performed during chip fabrication by specifying the metal interconnect. Secondly, the gate arrays are One-Time Programmable (OTP) devices, which means once the chip is customized to its function, it is not possible to erase that functionality and re-configure it.

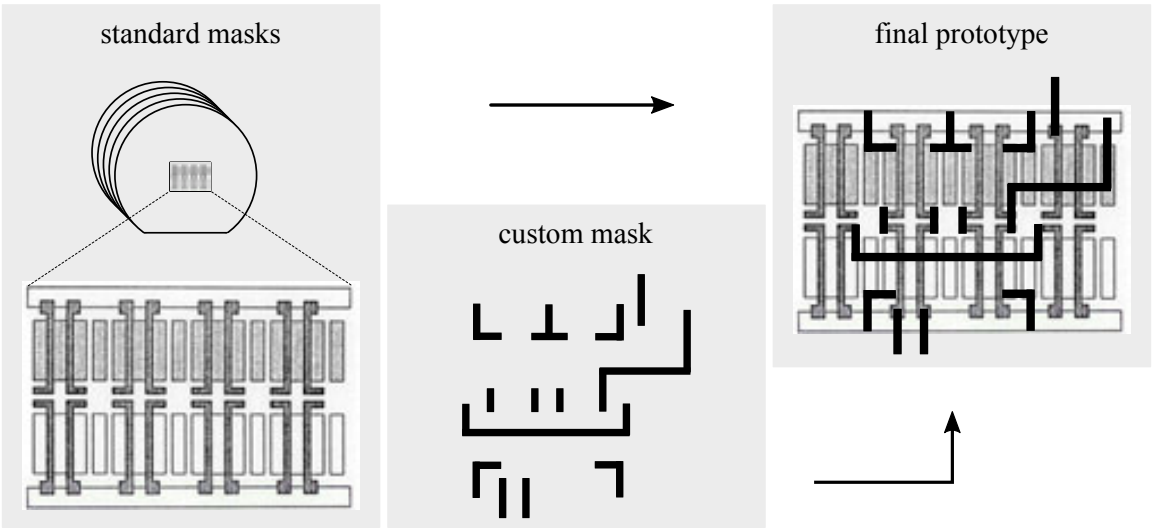


Fig. 2.2 Manufacturing steps of a sea of gates chip

2.4 Field-programmable devices

Field-Programmable Device (FPD), also known as field-configurable device, or Programmable Logic Device (PLD), refers to any type integrated circuit used for implementing digital hardware, where the chip can be configured by the end user in-the-field to realize different designs. Programming of such a device often involves placing the chip into a special programming or configured "in-system" using standard means (USB, JTAG, etc.). The most compelling advantages of FPDs are instant manufacturing turnaround, low start-up costs, low financial risk (since programming is done by the end user) and ease of design.

Field-Programmable Gate Array (FPGA) is an FPD, which consists of an array of logic cells surrounded by configurable routing resources similar to gate arrays, but the configuration is generally specified using a Hardware Description Language (HDL) or composing IP blocks. They use the high circuit densities in modern processes featuring a general structure that allows very high logic capacity. There are two basic versions of FPGAs in respect to programming method.

The first uses a special process option such as a fuse or antifuse to permanently program interconnect and personalize logic, addressed as OTP. As an example, devices manufactured by Actel embed an array of logic modules within an interconnect matrix that is formed on the top metal layers [37]. These successive routing channels run vertically or horizontally, and an antifuse OTP contacts are placed at the intersection of routing traces. Figure 2.3 shows the antifuse that consists of three sandwiched

layers (conductor-insulator-conductor) and is located between two interconnect wires. It normally has high resistance (effectively open circuit), and by applying a special programming voltage across the contact, the resistance permanently drops to a few ohms. Actel´s antifuses uses Poly-Si and n^+ diffusion as conductor and ONO [37], while other antifuses rely on metal for conductors, with amorphous silicon as the middle layer [38].

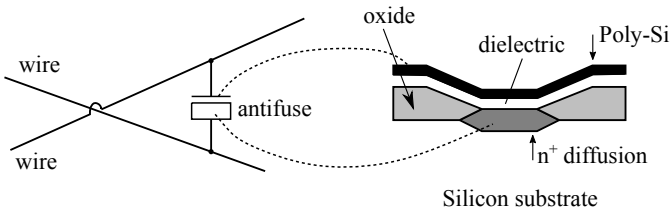


Fig. 2.3 Actel antifuse structure

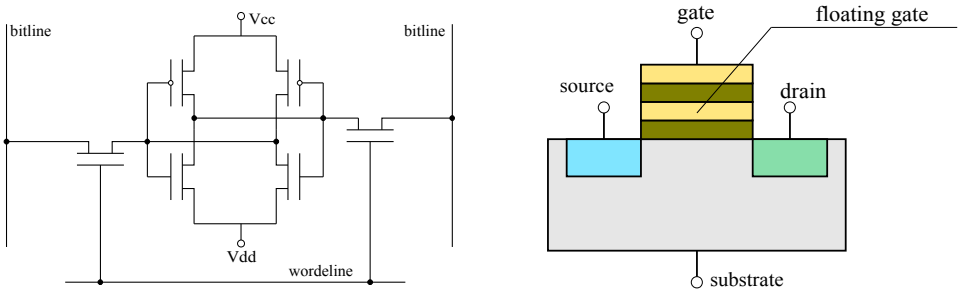
The advantage of this type of routing is that the size of the programmable interconnect is tiny enabling higher overall density. The disadvantage is that the interconnect is not re-programmable, so once a chip is programmed, its function is fixed to the extent that the interconnect has been personalized [39].

The second type of FPGAs uses Static Random Access Memory (SRAM) or flash memory to configure routing and logic functions. The key advantage that this type of configuration offers is the re-programmability feature, which allows the end user to reuse the chip for different applications.

SRAM-based FPGAs store logic cells configuration data in the static memory (organized as an array of latches). SRAM is volatile and cannot keep data without power supply, therefore, the FPGA must be configured upon start. While it may seem inefficient (in terms of area, speed and power) to use a RAM cell to perform logic, specially designed single-data line RAMs are small and fast in current processes, and resources such as the routing tend to dominate modern designs from a density and speed viewpoint. Currently, Xilinx Virtex [40], and Spartan families [41], and Altera Stratix [42] and Cyclone [43] devices use SRAMs for programming. Figure 2.4 (a) shows an SRAM memory cell.

Flash-based FPGAs uses flash as a primary resource for configuration storage. Flash memories require more complex process than SRAM. This technology has an advantage of being less power consumptive, and more tolerant to radiation effects. Furthermore, this type of FPGAs has a non-volatile memory cell to hold the configuration pattern right on the chip, and even if power is removed the contents of the flash cells stay intact. FPGA families, such as Actel LGLOO and ProASIC3 use this configuration technique.

Figure 2.4 (b) shows a floating-gate transistor used in flash memory. Traditionally, due to challenges of shrinking the flash memory cell, flash-based FPGAs used to suffer from lower density and performance than SRAMs. However, advances in process technology now allow the FPGA designers to shrink the flash configuration cells and integrate them into advanced logic processes, enabling high-performance flash-based FPGAs to deliver features and functions comparable to or even better than SRAM-based FPGAs.



(a) SRAM memory cell

(b) Floating-gate transistor used in flash memory

Fig. 2.4 Re-programmable configuration techniques

2.5 Altera HardCopy

Traditionally, ASICs have been the ideal solution for system architects designing high-volume, high-performance applications. However, designing complex ASICs requires expensive design tools, results in high development costs, and involves significant overall risk when bringing products to market in a timely manner. In contrast, FPGAs offer design flexibility and automation by using software to estimate performance and power consumption, and maximize system throughput. Moreover, FPGAs reduce the risk, time-to-market, and cost. However, comparing with high-density ASIC, they consume more power with lower performance. They are also not very common and cost-efficient for volume production.

As a mid-point solution, Altera [44] introduced new devices known as Altera´s HardCopy devices, that offer system solution by providing flexibility of FPGAs at the low power and cost of ASICs for volume production. One example is Altera´s HardCopy Stratix^{TM} series [45] that preserve their Stratix FPGA counterpart´s architecture [42], but the configuration and programmable routing resources are removed and replaced with direct metal interconnects (same concept as metallization step in SoGs). This

results in considerable die size reduction and ensuing cost savings. The user can obtain an average of 50% higher performance and up to 40% lower power consumption than can be achieved in the corresponding Stratix FPGAs. However, once the device is manufactured, the functionality of the device is fixed and no re-programming is possible.

HardCopy Stratix devices consist of base arrays that are common to all designs for a particular device density and design-specific customization is done within the top metal layer(s). The base arrays use an area-efficient Sea-Of-Logic-Elements (SOLE) core and extend the flexibility of high-density Stratix FPGAs to a cost-effective, high volume production solution. With a seamless migration process, functionality-verified Stratix FPGA designs can be migrated to fixed-function HardCopy Stratix devices with minimal risk and guaranteed first-time success. Another family of Altera´s HardCopy devices is APEX^{TM} [46] manufactured using an 0.18 um CMOS six-layer-metal process technology, which enables high-density APEX 20KE device technology [47] to be used in high-volume applications.

To ensure the device functionality and performance, designers should thoroughly test the original FPGA-based design for satisfactory results before committing the design for migration to a HardCopy device. For that, Altera has developed a "design once" flow for both HardCopy ASICs and their prototyping FPGAs. At the front end, before design hand-off, user can have one design, one IP set, one methodology, and one tool to create two device implementations. First, the user can get his system ready for production with an FPGA prototype, and guarantee a functional equivalent and pin-/footprint-compatible HardCopy ASIC as a drop-in replacement for volume production (Figure 2.5).

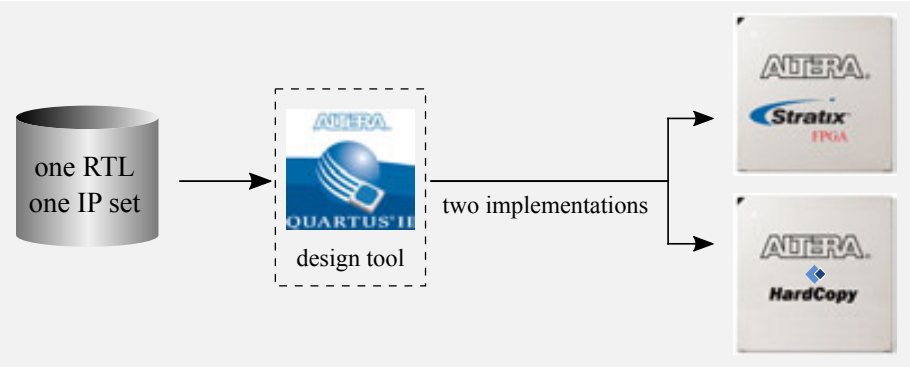


Fig. 2.5 One design, one RTL, one IP set, two implementations

Once the system is ready, one can perform market testing and initial low-volume production with FPGA devices. Following that, if the client requires low-power, high-

performance, volume production of the same system, then HardCopy ASICs can be employed to obtain a fully-tested and production-quality sample in less than two weeks and the large-volume production in twelve weeks.

Software, such as, Quartus II provides a complete set of inexpensive and easy-to-use tools for designing HardCopy devices in a manner similar to the traditional ASIC design flow. Combination of FPGAs for prototyping and design verification, HardCopy devices for high-volume production, and the design software provide a comprehensive and powerful alternative to conventional ASIC.

2.6 Summary

Several ICs, as well as their pros and cons were explained in this chapter. The main factor in choosing a class of IC is the quantity of parts you will need in mass production, because selling a larger volume of parts drives the need for a lower unit cost and provides profits to pay back a large NRE. High volume ICs need a low unit price but can tolerate a high NRE, so full custom ICs are the best fit. Low volume ICs can tolerate a high unit cost but need a low NRE, so FPGAs are the best choice. Semi-custom ASICs (standard cells and gate arrays) provide a balance of reasonable unit cost and moderate NRE, so they fit in the middle ground where production volumes are moderate. Table 2.1 indicates the proper design methodology in respect to annual production volume (Source: [48]).

Table 2.1 Selecting an integrated circuit class

Annual production	Critical factors	IC class
High	Low unit cost	Full-custom
Medium	reasonable unit cost and NRE	Semi-custom (SC and GA)
Low	Low NRE and quick time to develop	FPGA

Another important factor in choosing a class of IC is the time it takes to develop the chip. Development time may be a few months for FPGAs, a year or so for standard cells and gate arrays, and few years for full custom ICs. Some design methodologies take advantage of the best features of all three classes of ICs by prototyping with FPGAs, beginning low volume production with ASICs, and converting the design to full custom if the product is successful in the market and the volumes ramp up to millions. Table 2.2 summarizes the characteristics of classes (Source: [48]).

Due to a lack of circuit components, cell libraries, and an automated design flow, the advantages of a cell-based and array-based semi-custom design methodology are

Table 2.2 Characteristics of integrated circuit classes

Characteristic	Full-custom IC	Semi-custom IC	FPGA
Masks customized	All	A few	None
NRE	$300,000 to $millions	$50,000 to $150,000	Less than $50,000
Die size	Small	medium	Large
Time to develop	2 to 5 years	About 1 year	A week to a few months
Unit cost (10M/year)	Small	Medium	Large
Unit cost (100K/year)	Not feasible	Medium	Large
Unit cost (1K/year)	Not feasible	Not feasible	Large

not yet explored when considering digital design for organic electronics. In this thesis, we use the above-mentioned well-established benefits of ASIC industry and map it to Application Specific Printed Electronic Circuits (ASPEC) by adopting array-based design methodology.

Chapter 3

STATE OF THE ART

In this chapter, a brief introduction about the state of the art in respect to different aspects of printed electronics is provided. The goal of this chapter is to set the ground for ongoing investigations about development of organic devices and circuits.

In organic electronics, there are some physical features in transistor level that enables circuit techniques, different from standard CMOS technology. Circuit design in organic electronics is different from conventional silicon-based electronics, and needs some specific background on materials and technologies with related working principles, advantages, and challenges. Therefore, in this section a closer look on functional materials, substrates, and technology processes is given.

3.1 Functional materials

During the last decades, there has been a lot of effort for progressively replacing the inorganic semiconductors (silicon, gallium arsenide, etc.), silicon oxide insulator and the metals (aluminum and cooper) with environmentally friendly organic materials that can be fabricated with low cost techniques. The effort has been focused to improve the electrical properties and stability of organic materials.

Electrical characteristics of the basic devices, such as organic transistors, play an important role in improving the performance of electronic circuits. For instance, a large current modulation ratio (I_{on}/I_{off} ratio) is essential, since most electronic applications require the transistor to behave as a switch, with a large drain current in the "on" state, and a negligible drain current in the "off" state. This combination of requirements is best met with a semiconductor that is characterized by a large intrinsic resistivity and a large carrier mobility.

3.1.1 Organic Semiconductor

Organic Semiconductor (OSC) is a molecular solid built from conjugated molecules showing an alternation of single and double bonds between carbon atoms. The electronic structure for hole and electron is referred to as the Highest Occupied Molecular Orbital (HOMO) and the Lowest Unoccupied Molecular Orbital (LUMO), which play similar roles as the valence band and the conduction band on the molecular level, respectively [49]. These two bands are separated by an energy gap. The larger the conjugated network is on a molecule, the smaller the HOMO-LUMO gap will be because of the increased extends of the potential well.

Many amorphous or polycrystalline organic semiconductors exclusively support positive or negative charge carriers, but not both. In crystalline semiconductor technologies, n-type and p-type refer to the type of dopant, and therefore majority carrier, in a semiconductor, and both holes and electrons can usually be transported. In contrast, organic semiconductors only support one type of charge carrier and are more properly referred to as hole –designated as p-type– or electron –designated as n-type– transporting. Organic semiconductors are traditionally classified as polymers or small molecules.

Polymers have the advantage of being amenable to specific deposition techniques, such as solution processing with good uniformity, that have been developed for long for conventional polymers [50], [51]. The charge mobility and performance of these materials is still lower than small molecule semiconductors. The performance critically depends on the chemical and structural ordering of the chains at the insulator-polymer interface [52]. It has been demonstrated that the mobility can be slightly increased if the film is applied by dip-coating instead of spin-coating [53].

Small molecules are light and can usually be purified and deposited through thermal evaporation process in vacuum. They exhibit high charge mobility and performance but poor uniformity [54], [55]. Only a few of small molecule semiconductors are soluble and thus can be solution-processed. The highest reported mobility is up to 6 cm^2/Vs for pentacene-based OTFTs [56]. Pentacene ($C_{22}H_{14}$) is the most common example in this category and is usually used for only p-type transistors and circuits. In practice it is considered as a unipolar semiconductor. $F_{16}CuPc$ [57], and fullerenes such as C_{60} [58] are the examples of evaporated n-type OSCs.

Meanwhile, precursors, such as TIPS-pentacene, can be solution-processed and then converted by annealing to small molecule [59]. Thus, they take the advantages of easy processing for polymers and high mobility and performance of small molecule. This successful combination can also be obtained with polymer-small molecule blends

such as diF-TESADT:PTAA achieving charge mobilities over 2 cm^2/Vs with good uniformity [60], [61].

Besides low mobility, another key limitation of organic semiconductors is their poor stability against oxidation and reduction reactions, enumerated by De Leeuw [62]. However, by engineering the electron energy levels of organic semiconductors, it is possible to set the HOMO and LUMO levels so that the equilibrium potential at no bias sits in a region which is thermodynamically stable against these redox reactions. Providing n-type stability is synthetically more difficult than p-type ones [63], [64].

There exist both p-type and n-type semiconductors, and also ambipolar semiconductors showing both behaviors, but still, the most common organic semiconductor used is p-type due to its higher performance and ambient stability. However, currently n-type semiconductors are approaching their mobility and stability to p-type ones allowing the use of complementary logic with higher stability and power-efficiency.

3.1.2 Insulators

When selecting the process and material for gate dielectric, a number of considerations, such as, leakage, patterning convenience and compatibility, semiconductor compatibility, achievable capacitance, surface tunability, and hysteresis, typically should be taken into account.

The deposition of inorganic gate dielectrics with sufficient quality typically requires process temperatures near or above 250°, and such temperatures are often incompatible with low-cost, flexible, polymeric substrates, which typically have glass transition temperature below 200°. In contrast, polymer gate dielectrics can be solution-processed (spin-coated, spray-coated, and printing) for fabrication of OTFTs on flexible polymeric substrates. They offer great process throughput, low fabrication costs, and a lower thermal budget compared with inorganic dielectrics. Since OTFTs are targeting inexpensive applications, throughput and low-cost processes are of particular concern, thus making the high-quality, solution-processed polymer gate dielectrics the best candidate in fabrication of OTFTs and integrated circuits.

In 1998, Duray *et al.* reported the first organic integrated circuits with solution-processed polyvinyl phenol as the polymer gate dielectric [65]. Later in 2000, solution-processed photoresist (Olin Hunt Model SC100) was employed as the gate dielectric layer in OTFTs and fairly complex integrated circuit [66]. The main disadvantage of solution-processed polymer gate dielectrics is the minimum thickness of such films. While, the high-temperature, vacuum-deposited inorganic gate dielectrics can offer

scalable thickness with relative ease, solution-processing of polymers typically results in relatively thick films with thickness of greater than 100nm.

Insulating, organic, Self-Assembled Monolayers (SAMs) is a complementary technique to improve polymer dielectric characteristics and also to decrease the thickness, enabling the fabrication of fast integrated circuits with lower power consumption. With a thickness of between 2nm and 3nm, they can provide leakage currents similar to or even smaller than those typically obtained with high-quality silicon oxide films [67]. In 2002, OTFTs with SAM gate dielectric layer were demonstrated. For a TFT with channel length greater than 200nm, gate leakage on the order of 10^{-6} A/cm^2, threshold voltage of -1.3 (V), and a current modulation ratio of 10^4 were extracted [68].

3.1.3 Conductor materials

Gate, source, and drain electrodes are often prepared using inorganic metals. Non-noble metals, such as aluminum or chromium, are suitable for the gate electrodes in the inverted device structures, since these metals have excellent adhesion on glass and plastic substrates. Noble metals, most notably gold, are a popular choice for the source and drain contacts, since they tend to provide better contact performance than other metals, at least for most p-channel TFTs, but also for many n-channel TFTs.

The metals are conveniently deposited by thermal evaporation in vacuum and patterned either by photolithography in combination with lift-off or wet-chemical etching. The key parameter for the patterning of the source and drain contacts is the minimum achievable feature size, which ideally should be as small as possible.

An alternative to inorganic metals are conducting polymers, such as polyaniline (PANI) and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS). These are chemically doped conjugated polymers that have electrical conductance in the range between 0.1 and $1000 S.cm^{-1}$. Conducting polymers can be processed from organic solutions (PANI) or from aqueous dispersions (PEDOT:PSS), so the gate electrodes and the source and drain contacts of organic TFTs can be conveniently prepared by spin-coating and photolithography, or by direct inkjet-printing.

Work function difference between the semiconductor and the energy levels in semiconductor is another consideration in selection of source and drain electrodes. Gold is a popular choice for p-type organic transistors, since its large work function provides reasonable access to the HOMO level of many materials.

3.2 Substrates

Most of the PE devices target the use of potentially low cost and flexible substrates to enable large area products with higher freedom of design. Glass and metal (stainless steel, alumina or titanium foil) with high and reliable barrier properties are used in many applications such as sensors, OLED lighting and displays, Organic Photovoltaic (OPV) and flexible dye-sensitized solar cells [69]–[72]. Flexible, lightweight plastic and polyesters (PET, PEN) substrates have also attracted much attention in large-area roll-to-roll production [73]–[78]. Paper, a material made from renewable resource, has turned out to be one of the best candidates for cheap green electronics applications [79], [80].

3.3 Technological processes

Printability of the circuit is one of the most important arguments in favor of printed electronics. The low thermal budget and the high degree of mechanical flexibility have opened new opportunities to produce soft, lightweight, and flexible thin films for electronic applications over small (sheet-to-sheet manufacturing) or large area (roll-to-roll manufacturing). Typically, the aim is to fabricate (semi-) transparent, bendable and even rollable flexible electronic devices such as OLED-based displays, RFID tags, and organic solar cells.

However, flexible electronics face new challenges, not necessarily originating from the small dimensions of the device, but from the deformations and dimensional instability of the substrate. For example, low temperature processing becomes necessary as the substrates, such as plastic or glass, may deform in high temperatures, causing distortion of the printed device.

Electrically functional devices can be printed by using the same technologies in graphics art industry, and almost all of the industrial printing methods (flexography, screen, offset, lithography, inkjet, and etc.) can be used for PE. Manufacturing approach is also similar to conventional printing, because devices and circuits are fabricated on a layer-by-layer basis, depositing them on top of each other. However, the maximum desired resolution for electronic devices especially short-channel transistors, whose lower dimensions mostly imply higher performance, is higher than conventional printing.

The organic electronic device structures appear relatively straightforward and their production process has lower degree of complexity than standard CMOS production process (mostly due to the different integration scale). However, its implementation and

fabrication is challenging. Although device materials and structures may be identical in design, device performances can differ significantly according to the processing method [81].

Deposition of the organic semiconductor is one of the most critical steps in this process. Charge carriers move through the semiconducting layer near the dielectric layer. Therefore, the semiconductor-dielectric interface characteristics and the molecular ordering of the semiconductor must be optimized to achieve a high performance [82], [83]. The level of ordering in the pentacene crystals, as well as, the grain size and the presence of lattice defects, all have an influence on the transistor parameters, such as mobility and turn-on voltage.

The deposition of other layers such as insulators and metal contacts can play an important role in device performance. Dielectric must be uniformly deposited to reduce the gate leakage current. The source and drain electrodes formation and structure can also influence the properties of the transistor channel itself. Crystal growth nucleated on the source and drain and the process used to pattern the electrodes can have a significant effect on overall device performance.

In this section, different existing technological processes for building organic devices with the focus on progress in thermal budget, maximum achievable resolution, process complexity, and deposition techniques, are presented.

3.3.1 Clean room

According to the International Organization for Standardization (ISO) standard 14644-1 [84], clean-room is defined as a room in which the concentration of airborne particles is controlled, and which is constructed and used in a manner to minimize the introduction, generation, and retention of particles inside the room and in which other relevant parameters, e.g. temperature, humidity, and pressure, are controlled as necessary.

The most well-known and widely spread clean-room patterning technique in semiconductor industry is optical lithography (i.e. photolithography). It proved to be far more capable of reducing the minimal feature dimensions to fulfill Moore's law than one could have imagined. Photolithography in an strategy for layer definition, in which a radiation sensitive material is exposed to a structured radiation pattern (UV through a high optical density mask) and developed. This template is then used as a mask or lift-off vehicle for other materials which are not themselves light sensitive. Photolithography can be directly applied to all of the layers of the organic semiconductor stack.

The resolution limit of optical lithography has been continuously improved by reducing the exposure wavelength and increase of the numerical aperture. High-end optical lithographic patterning techniques such as deep- and extreme UV [85], X-ray [86], and immersion lithography [87], [88] have pushed the resolution limit into the sub-micrometer and tens of nanometers regime on Si substrates.

The main difficulty when using this technique is associated with removing photoresist after the etching process is complete, because device performance can easily be affected by even slight surface residues. Therefore, cleaning steps after lithography need to be engineered to insure optimal surface cleanliness.

Many organic semiconductor materials are also not tolerant to solvent or developer exposure, and this limits the applicability of standard resist systems on semiconductor materials. The solution to that is to protect the semiconductor from materials it is not compatible with, such as, organic solvent and water. Some approaches were proposed in the state of the art: using water soluble resists [89], encapsulating the transistors using parylene before photolithography and patterning [90], and using fluorinated or super-critical CO_2-based resist materials [91].

On flexible substrates, photolithography is often used to pattern large micrometer features such as a gate or source drain terminals [88], [92], but also the semiconductor is regularly patterned by photolithography [93]. Photolithography defined OTFT devices were fabricated using two layers of pentacene deposited at different substrate temperatures as the active material [94]. TFTs with low-voltage high-mobility organic semiconductors for flexible display applications patterned by photolithography technique were also reported in [95].

In typical photolithographic processes, the substrates and organic electronic materials are exposed to corrosive etchants, high-energy radiation, and relatively high temperatures during processing. The high investment and operation costs of this process at the resolution limit, are feasible as long as high yields and volumes are targeted.

An economically more feasible route to high-resolution electronic devices is envisioned by one of the next-generation lithography techniques (e.g., Nanoimprint lithography) on low-cost, polymeric foils. These alternative, high-resolution patterning techniques can be operated at lower costs to obtain the same or an improved resolution compared to the high-end photolithography systems. The integration in high-throughput patterning facilities such as a R2R line, would allow the fabrication of low-cost, large-area, flexible and lightweight devices. However, the transfer of processes from Si to polymeric foils is challenging and not straightforward.

Photolithography has been used for fabricating some of the OTFTs in this work. Further explanation of different alternative methods towards high-resolution patterning (such as soft lithography, nanoimprint, etc.) is out of the scope of this thesis.

3.3.2 Conventional analog printing processes

Analog printing refers to the process in which manually prepared screens or plates are used for printing the desired pattern. These techniques apply pressure to the substrate during ink transfer. The stages involved in analog printing are given as follows: Files for each and every material used in printing are created separately. Then the screens or plates for every file are generated with respect to their functional material. Afterwards, every single material is printed through its own screen or plate.

Four conventional analog techniques exist, named after the type of master used for printing: relief printing (flexographic), intaglio printing (gravure), planographic printing (offset), and print through (screen printing). The cost and complexity of producing a master range from relatively low cost in the case of screen printing to medium cost for flexographic printing and very high cost for gravure printing [96].

I. Flexographic printing

Flexographic printing is a reliable technique, similar to the traditional rubber-stamp technique, which has been in use for hundreds of years. In flexographic printing, the desired pattern is printed from protruding elements on a plate cylinder to almost any type of substrate (paper, plastic, metal foil, and etc.). The elastic printing plate is made by exposure of a light-sensitive polymer, by computer-guided laser engraving, or through a molding process from a metallic plate creating a 3D relief in a rubber or polymer material. Figure 3.1 shows the schematic of flexographic printing.

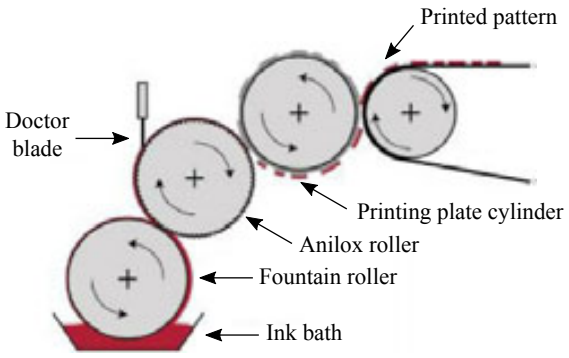


Fig. 3.1 Schematic of flexographic printing techniques

Ink is transferred from the ink or fountain roll to an anilox roll, the textures of which hold a specific amount of ink. From the anilox roll, a controlled amount of ink with a uniform thickness is evenly and quickly transferred to the printing plate. The reliefs on the printing cylinder pick out ink from the anilox roll, where after the ink is finally printed by pressing the web substrate against an impression cylinder. The pressure of the impression cylinder helps transfer the ink from the printing plate and the image on to the printing substrate. The quality of the image is related to the applied pressure between plate cylinder and substrate materials and to the geometry of the anilox roll cells, depth, and volume. The thickness of the printed film can be controlled with the rotating speed, the type of anilox roller and plate cylinder, and the pressure applied to printing substrate [97].

Flexography method has several advantages and disadvantages in electronic manufacturing. The thickness of the film can be controlled especially over large areas. Next to the wide variety of substrates, a wide range of inks that can be printed: solvent-based inks, water-based inks, electron-beam curing inks, UV curing inks and two-part chemically-curing inks. The spreading of the ink can be controlled by using a hard polymer cover or components and the pressure-sensitivity of the operation.

With flexography, continuous conductive grids of Ag ink have been reported on indium tin oxide (ITO)-coated poly(ethylene terephthalate) (PET) foil with a minimal line width of 75um [98]. The typical resolution limit of 50–100 um [99] for flexography can be reduced to around 20um by controlled edge dewetting and film breakup of inks, transferring for example Ag ink from a poly(dimethyl siloxane) (PDMS) mold to SU8-coated substrates [100].

Flexography has been used addressing several application in printed electronics, such as, volume printing of large-area OLED lighting and conducting tracks for packaging.

II. Gravure Printing

Gravure printing is the reverse of flexographic printing in terms of wetting the ink on the printing plate (called the rotogravure plate). In gravure printing, an engraved cylinder, on which the pattern has been etched by laser or photolithography, is rolled over a moving substrate, typically paper or plastic [24]. Excess ink is removed from the protruded elements of the cylinder by a doctor blade before the relatively low-viscosity ink is transferred from the cells to the substrate. Typical cell densities are between 220 and 400 cells per inch, with a groove or cell depth around 40um and width $<$100um [101]. Figure 3.2 shows the schematic of gravure printing.

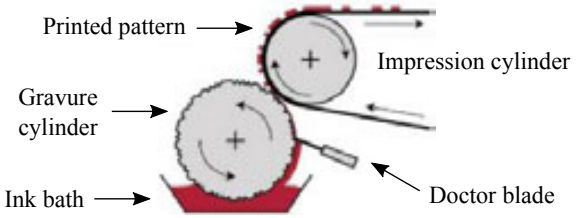


Fig. 3.2 Schematic of gravure printing techniques

Different amounts of materials can be deposited in different locations according to the depth of the grooves. For successful printing, the surface of the substrate must be smooth enough for proper contact with the engraved grooves. Otherwise, inadequate contact occurs with the substrate, leading to reduced mechanical and electrical performance on the printed structure.

Gravure printing is a high speed process using low-viscosity materials. The system is costly, because of the expensive printing rolls compared to rubber-made rolls in flexography. On the other hand, it is very durable, and the printing rolls can well withstand various solvents. For a low-viscosity ink for high printing speeds, solvents such as toluene, xylene, and alcohols are often used purely or together with water. Adequate viscosity can be achieved by thinning polymers into the above solvents. However, fast evaporation of the solvent and cross-linking of polymers pose a challenge in high-speed printing.

The quality of the printing patterns depends on the properties of the substrate, such as smoothness, compressibility, porosity, ink receptivity, and wettability and on the chemistry, and drying. Gravure printing has been used to manufacture Ultra-High-Frequency (UHF) RFID antenna and shown to be practical in manufacturing OLEDs.

III. Offset printing

In offset lithography, introduced at the end of the 18th century by Alois Senefelder [25] images are formed by the physicochemical difference between pleo phobic and oleophilic areas on the printing master, thus not requiring a pattern relief. The main carrier is ole ophobic and often made of aluminum, while the color is taken up mostly by an oleophilic grease layer. Thin film plates holding the actual printing image are placed on the surface of the anilox roller. Figure 3.3 shows the schematic of offset printing.

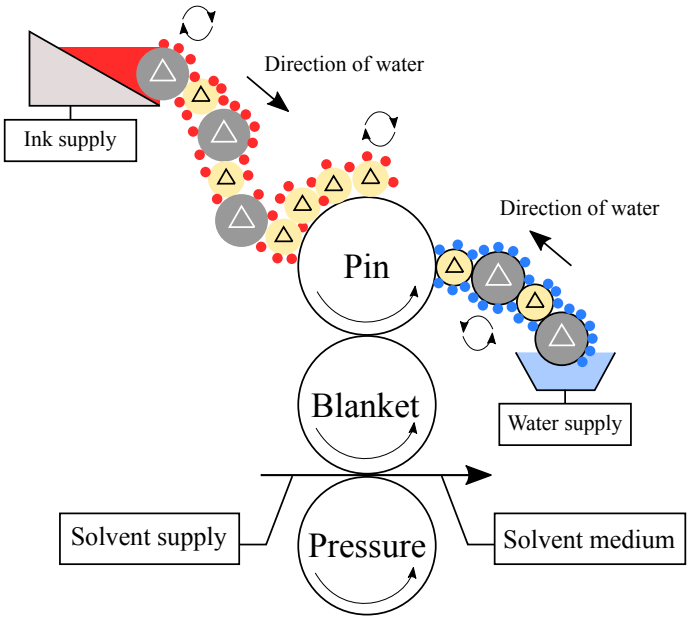


Fig. 3.3 Schematic of offset printing techniques

However, wetting the printing plate is very complex. Successful printing of an image on the substrate requires precise calibration of the anilox roller and the surface energy of the offset plate. In the graphic industry, offset is one of the most popular printing techniques, and it is also used in electronic manufacturing. This technique boasts excellent control, fast high-volume production, and high resolution in printing electronic circuits.

Offset printed features have typically a resolution in the range of 20um and a layer thickness below 1um [102], allowing micro-structuring up to 200,000m^2/h. Offset-printed source and drain electrodes of top gate TFTs and a seven-stage ring oscillator have been reported on PET foil, showing a gap width in the range of 50um and a line width down to 100um. The dry layer thickness obtained for printed PEDOT was 600nm [102]. In a modified offset printing technique [103], developed by LG Display Co., thin and uniform layers of etch resist were printed to form fine patterns of 10um width and 6um spacing as short channels of a TFT on Si.

IV. Screen printing

In screen printing [104], ink is pressed with a squeegee through a screen onto the substrate. The screen is typically made of a porous mesh, from materials such as a porous fabric or stainless steel. The image to be replicated, the stencil, can be

photochemically or manually defined on the mesh. Figure 3.4 shows the schematic of screen printing.

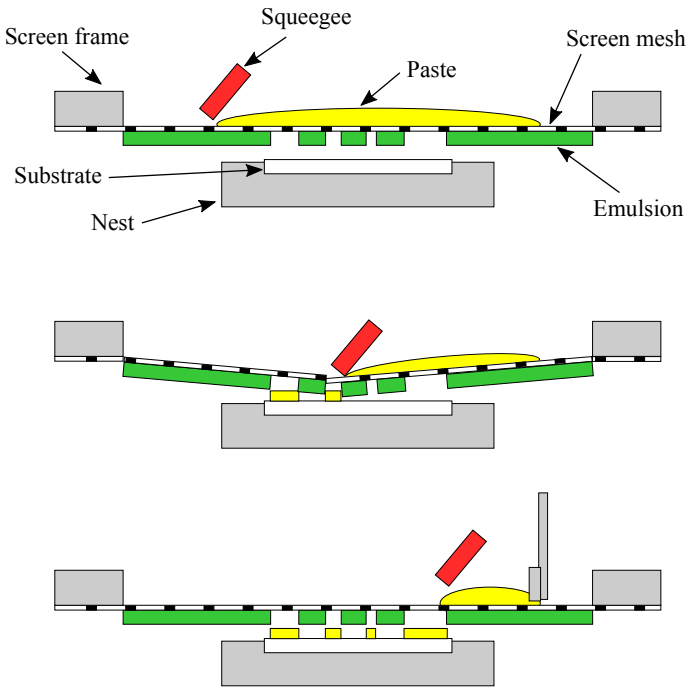


Fig. 3.4 Schematic of screen printing techniques

Due to the simplicity of the process, a wide variety of substrates and inks can be used, allowing a high layer thickness which is typical for screen printing. Screen printing is rather inexpensive and highly flexible for manufacturing electronics. It consumes small amounts of material with little waste and produce dry thick print layers.

However, it has limited resolution, limited throughput compared to gravure, offset, or flexography. From the three types of screen printing, rotary screen printing has the highest throughput, edge definition/resolution and achievable wet thickness [105].

In industrial processes, screen-printed films usually have a thickness larger than 0.5um [106]. Thin and homogeneous layers are not easily obtained by screen printing. As an example, the inhomogeneous 100nm hole transport layer of an OLED has been reported [107]. Nevertheless, also a 40nm thin active layer of a bulk hetero-junction photovoltaic device with an RMS value of 2.6nm has been reported [106]. Both devices have been fabricated on glass substrates. Silk screen-printed polymer solar cells have been reported on PET foil by Krebs *et al* [108].

Flexible pentacene transistors have been demonstrated [109] with room temperature, silk screen printed silver resist, forming the top contact source-drain electrodes on

poly (phthalate carbonate) foil. The channel length was varied from 40 to 200um at a fixed channel width of 1.5mm. CMOS devices on PEN foil have been fabricated by laser ablation of a 30nm gold source-drain layer and screen printing [110]. The p- and n-type semiconductor, a 800-nm-thick dielectric fluoropolymer and a gate layer of silver paste were subsequently screen printed, showing a process alignment of ±25um for all printed materials. With the printed inverters, a voltage-controlled oscillator and two differential organic amplifiers were presented. A solely screen-printed device, a flexible thin film supercapacitor on polyester (PE) foil, has been reported in [111].

3.3.3 Digital printing processes

Digital printing refers to the process in which the desired printing patterns are defined through computer-based EDA tools. Despite analog printing, no mask or plate is required for patterning the structures, thus allowing rapid prototyping of several geometries. As a direct-write and non-contact printing technique, the ink is dropped from a nozzle onto the substrate according to a digital image. Thereby, no pressure is applied to the substrate, which makes them non-impact techniques.

Digital printing is also named as additive manufacturing due to the fact that materials are deposited layer-to-layer after each other. From an engineering and design standpoint, additive manufacturing technologies are becoming more accurate with features ranging from micron-sized to building sized. However, the minimum feature size and resolution in digital printing techniques is low comparing to clean room processes, such as photolithography.

The absence of a printing master makes digital printing more customizable and results in less waste with respect to chemicals and the target material. Utilization of a digital master has the considerable advantage of reduced cost, since the cost and complexity of producing a master range from relatively low cost in the case of screen printing to medium cost for flexographic printing and very high cost for gravure printing. Direct write attribute of digital printing allows for deposition of versatile thin films, the designs of which can be changed with ease from batch to batch.

The combination of 3D micro-scale structures and additive printed electronics is expected to produce a significant impact on the functionality and component design, manufacturing processes, and business models. Highly complex components can also be fabricated faster while consuming less material and using less energy.

Several applications addressing organic devices and circuits by using digital printing have been reported [112]–[115]. However, the main focus of this thesis is to take the main advantages of this technique such as cost-efficiency, rapid prototyping, and

low-complexity (mask-less), and adopt it for metallization of the semi-custom circuits, which will be presented later in chapter 5.

There is a variety of digital printing techniques, according to their operating principle and complexity. Here, I introduce some of the most dominant conventional and modern techniques, which have been used during this thesis, and compare them in respect to their key features such as resolution, throughput, complexity, and etc.

I. Inkjet printing

Inkjet Printing (IJP), the most conventional digital printing technique, is an additive non-contact method that encompasses a wide variety of different techniques to generate droplets. It uses several inks jetted repeatedly from the printhead to form small droplets that can be directed accurately on to the substrate. It has forced its way from being just a graphic arts printing tool (very popular these days) to the paradigm of micro/nano manufacturing and has also been successfully used for the direct 3-D fabrication of micro/nano structures.

There have been an increasing research developing processes and devices using this technology [116]–[119], and hybrid approaches [120], [121]. Applications such as light-emitting diodes [122], metallization of solar cells [123], [124], thin film transistors [121], [125], encapsulated electronic packages [126], bio-sensors [127], and programmable memories [128]–[130] have been reported using inkjet printing technology.

As a digital printing technique, IJP has a number of attributes for its evaluation and subsequent development: Precise quantities of a wide range of materials can be deposited in the form of conducting lines or single droplets on various substrates. It is a versatile, low-cost and rapid patterning technique with a large potential to manufacture electronic circuits, enabling large-scale and large-area applications.

Drawbacks of this technique are the necessary adjustment of the ink viscosity, concentration and solvent system to the nozzle (to prevent clogging) and the substrate material. Spreading of the ink and wanted or unwanted merging of dispensed droplets needs to be controlled. Further solvent, concentration and viscosity fine-tuning is required to control the shape, thickness and morphology of the dried droplet.

Typically, the serial printing characteristics of the inkjet system limits the throughput of the deposition. To overcome this issue, industrial inkjet printheads utilize hundreds to thousands of nozzles to realize throughput enhancement via parallelization [131].

Inkjet is not a single process but a diverse, versatile and multi-length scale group of process technologies, and a variety of mechanisms and energy modes are used to

create material transfer to produce features from nanometer to micrometer range. It can mainly be classified based on printhead types and the ejection of the ink into Continuous-mode (CIJ) and Drop-on-Demand (DoD). The main difference between those techniques is that in CIJ process, the continuously generated flow of ink drops is directed onto substrate in accordance to the image data. In contrast, in DoD processes, the droplets are generated and ejected from the nozzle orifice as and when required. CIJ method is not the in the scope of this thesis, thus, no further elaboration is provided here. Some interesting publications about this method exist in the state of the art literature [132]–[134].

DoD works simply by ejecting droplets only at the chosen moments, and it happens either through piezoelectric (PIJ) or thermal (TIJ), (almost discarded in PE), actuator inside the ink chamber. The chamber is connected to ink reservoir by a large channel called the throttle and to environment with a smaller channel called the nozzle. A pressure pulse will be generated inside the chamber by voltage controlled expansion of a piezoelectric element or a thermal bubble generated by a voltage controlled resistor. The pressure pulse will drive the ink out of the nozzle since the volume, and the mass, of the liquid inside the nozzle is significantly smaller than the mass of the liquid inside the large throttle. Figure 3.5 shows the schematic and operating principle of CIJ and DoD printing, as well as desktop printer machinery.

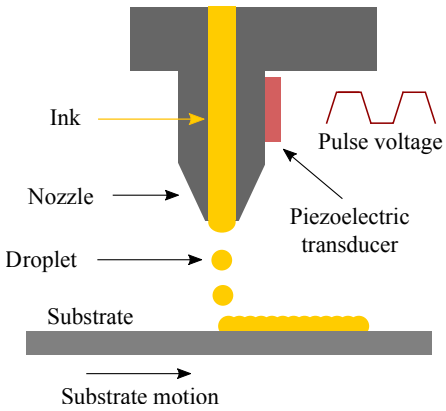


Fig. 3.5 Schematic of piezoelectric inkjet printing

The speed of the ejected droplet can be controlled by varying the shape of the voltage pulse in DoD technique. Moreover, comparing to CIJ, the resolution is improved in DoD, since the point of deposition is determined by the printhead movement relative to the substrate and not by the droplet flight path.

However, PIJ and TIJ DoD systems are not able to produce droplets with a broad range of size distributions from the same nozzle. The printing resolution is limited to

20 to 50um due to the nature of the materials to be printed and also to the statistical variability provided by fluid-based deposition technologies, through physical effects such as the flight direction of droplets and their spreading on the substrate [121], [135].

For getting higher and higher resolutions in terms of the feature size, inkjet systems requires the use of smaller sized nozzles which faces the difficulty of manufacturing and also the problem of nozzle clogging. Also, the droplet placement accuracy for these processes is not high enough. So, the quest for getting higher and higher resolutions at higher and higher printing speeds with more precision and accuracy led to the development of various novel modern IJP methods.

II. Electrohydrodynamic Inkjet printing

In order to obtain higher resolution and better droplet placement accuracy, the inkjet system utilizes externally applied electric field. This elegant way of manipulating droplet sizes, their ejection frequencies and placement on the substrate using externally applied electric fields is called as the Electrohydrodynamic Inkjet printing (EHD-IJP) technology.

Unlike the conventional IJP methods, it pulls the liquid inks out of the nozzle rather than pushing it. As a result, it is able to produce ink-drops of size 2 to 5 orders of magnitude smaller than the nozzle size [136] which is not possible in case of the conventional IJP systems. The elaborated working principle of this printing technology can be found in [137]. Figure 3.6 shows the schematic of EHD-IJP system (Source: [137]).

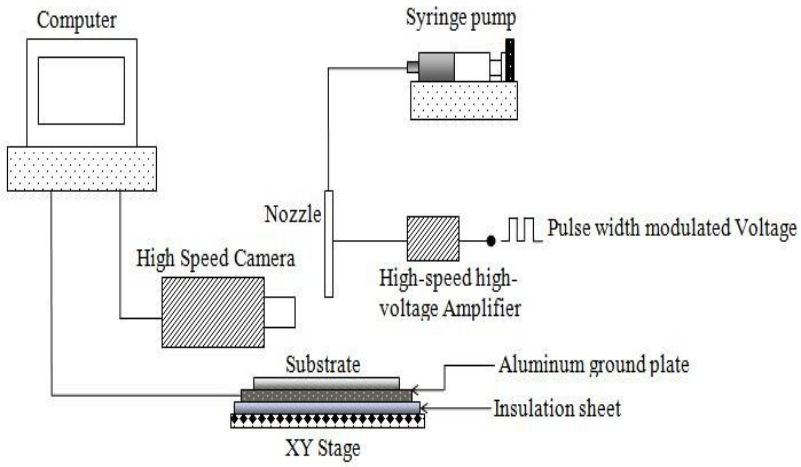


Fig. 3.6 Schematic of electrohydrodynamic inkjet printing system

The applications in printable electronics require higher print rates, better resolution and higher reliability. Thus, PE represents an important application area that can take advantage of both the extremely high-resolution capabilities of EHD-IJP, as well as its compatibility with a range of functional inks.

Different printed electronic devices require different fabrication processes regarding to the resolution, uniformity, and pattern complexity. EHD-IJP uses three types of printing: electrospraying (for thin film layers), electrospinning (for interconnections), and EHD jetting (for making electrodes). Thus, this technique has great potential to offer complex and high resolution printing and is opening new routes to nanotechnology.

The control of the droplet size and modes of the electrospraying offer a wide spectrum of practical applications. This printers eject liquid jets due to the electrohydrodynamic instability. Its main components consists of a liquid supply system to supply liquids at desired flow rates to the tip of a conducting nozzle and a DC power source to apply voltages across the conducting nozzle and the substrates. Depending upon the type of the applied voltage, either CIJ mode (constant DC voltage) or DoD mode (pulse DC voltage) can be obtained. To generate uniform micro-drops for high-resolution printing, the pulsed-DC voltage method is superior to continuous-DC voltage methods because of its controllability.

This technology has been a target of much research because of its ability to generate drops of very small size as compared to the other inkjet techniques for the same nozzle sizes. [138] concluded that this technique can be used for printing of conductive lines for metallization in printed circuit boards and backplanes of printable transistors. [139] showed applications in fabricating conductive micro-tracks and micro-connects and printed silver tracks with feature size down to 35 microns. Wang and Stark [140] demonstrated 3D silver micro-structures with 100um resolution. Youn *et al* [141] showed 6um silver lines using a tilted nozzle. [142] printed a set of silver lines with a few hundred nanometers in thickness and with a few hundred micrometers in width with EHD-PIJ. [143] demonstrated the high resolution printing with print feature sizes in the range from nearly 240nm to 5nm.

III. Superfine Inkjet printing

Superfine Inkjet technology (SIJ), invented by Kazuhiro Murata, at National Institute of AIST in Japan, is another interesting technique to form super-fine sub-micron wiring patterns and three-dimensional structures. This technique, drawing its heritage from the electrospraying technology, enables ejection of super-fine droplets smaller in

size (1/10) and volume (1/1000) than those by the conventional DoD IJP technique [144]–[146].

SIJ is a novel sub-class of electrohydrodynamic printing, in which, oscillating electric field is used to generate the necessary pressure for droplet ejection. This mechanism enables the generation of sub-femtoliter droplets, which translates to a resolution of approximately 1um on the substrate in suitable wetting conditions. Figure 3.7 shows the schematic of SIJ system. The elaborated working principle of this printing technology can be found in [146], [147].

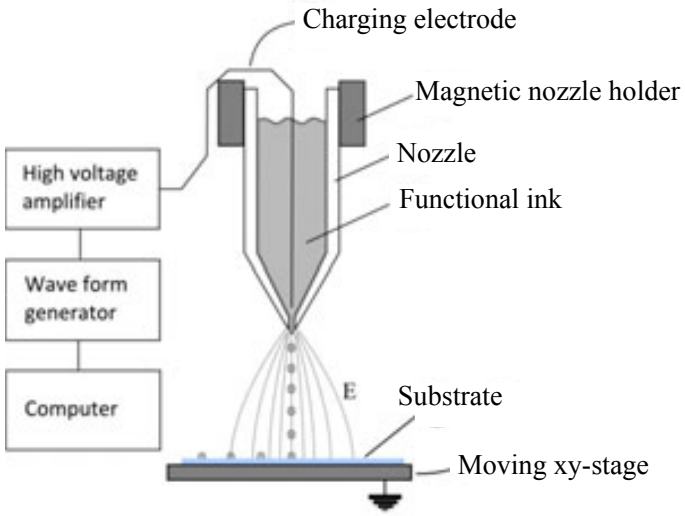


Fig. 3.7 Schematic of super-fine inkjet printing system

In conventional technologies, the minimum feature size depends on ink viscosity and surface tension, the kinetic energy of the droplet, the surface energy and the volume of the droplet. The resolution can be improved by surface treatment or reducing droplet volume or nozzle size prior to the printing process. In contrast, it is possible to control the printing resolution during the SIJ operation, since the droplet volume depends on the strength of the applied electric field.

However, for optimizing the process in respect to the ink suitability and printing condition, some requirements must be satisfied: stable jetting, line uniformity, temperature budget tolerance, and etc. Interesting experiments for ink stability, conductor width, topography, and resistance, as well as, process optimization has been shown in [148] for SIJ process.

IV. Aerosol jet printing

Aerosol Jet printing (AJ) is an innovative non-contact and mask-less additive printing technique for fine structures below $50\mu m$, developed by Optomec [149], and considered as a potential competitor of inkjet printing [150]. It is a novel direct-write technology that uses a focused aerosol spray to deposit material high resolution [151]. Figure 3.7 shows the schematic of AJ system.

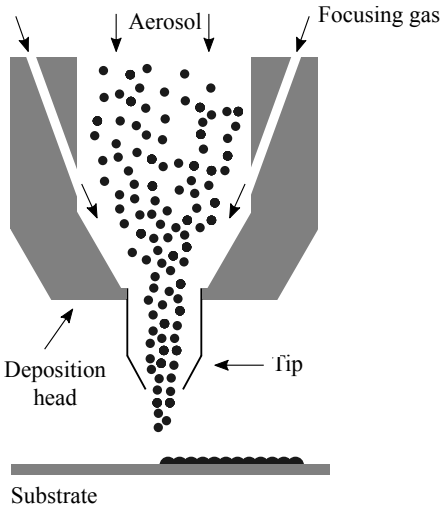


Fig. 3.8 Schematic of aerosol jet printing system

However, all of the above-mentioned modern digital printing techniques are still in early stages of development, therefore, are more used for printing fine lines and tracks rather than printing stack of layers to build devices such as OTFTs. Thus, most of the state of the art devices and circuits are fabricated either in conventional digital/analog printing techniques, or by using the well-established lithography processes.

3.4 Organic thin film transistors

Transistors based on organic semiconductors as the active layer to control current flow are commonly referred to as Organic Field Effect Transistors (OFET). In organic electronics, the term MOSFET (Metal-Oxide-Semiconductor FET) is not applicable because of the gate dielectric is not an oxide but an insulator, therefore the suitable term is MISFET (Metal-Insulator-Semiconductor FET). The most useful organic transistor implementation for practical applications is the Organic Thin Film Transistor (OTFT).

TFT concept was initially proposed and developed by Paul Weinmer in the 1960´s for transistors based on polycrystalline inorganic semiconductors such as evaporated cadmium sulfide [152]. The concept was later extended to TFTs based on plasma-enhanced chemical-vapor deposited (PECVD) hydrogenated amorphous silicon (a-Si:H) TFTs [153]. Today, a-Si:H TFTs are widely employed as the pixel drive devices in active-matrix liquid-crystal displays on glass substrates. TFTs using organic material (OTFTs) were first reported in the 1980s [154].

During the last decades, there has been a lot of investigation on developing and improving the capabilities of OTFTs. The performance of organic semiconductors has improved to the point where they are considered to replace amorphous silicon in TFTs for active matrix display backplanes [155], [156].

In this section, we review the basics of OTFTs: device operation and structures, characterization and modelling, and design-process techniques for performance improvement.

3.4.1 Operation and characteristics

In traditional crystalline Silicon FET (c-Si FETs), the source and drain are doped so as to create two back-to-back p-n junctions that block the flow of current in both directions in the channel. The gate is coupled to the channel – the gap between the drain and source – across the gate dielectric forming a capacitor to the channel charge sheet. When the gate/channel capacitor is strongly biased (more than threshold voltage) to repel majority carriers and attract minority carriers, an inversion layer is formed at the channel/gate dielectric interface. This short circuits the back-to-back diodes at source and drain, forming a resistor whose value is determined by the sheet charge density at the surface.

When the gate voltage exceeds the threshold voltage, inversion occurs. Applying gate voltage beyond the threshold will accumulate more charge in the channel and the transistor enters to linear region. For a given gate voltage, as a larger V_{DS} is applied, the field induced by the gate is partially canceled on the drain end. At this moment, the charge density at the drain end decreases and therefore, the current increment rate decrease. When the drain voltage equals to threshold voltage, *pinch-off* is said to have occurred and the device enters to saturation region, in which current stops increasing as V_{DS} increases. In this case, the devices are ideally seen as a current source.

The OTFT or OFET has a different structure and working principle. Although the basic gate capacitor is similar to c-Si FET, the contacts of OFET are not doped but deposited onto the substrate or gate insulator, depending on the device structure.

They work through the creation and elimination of a sheet of charge carriers at the gate dielectric/body interface. In contrast to MOSFET, an OFET device operates only in accumulation region. When the device is biased in an operating region which eliminates the sheet charge in the channel ($V_{\mathrm{GS}} < V_{\mathrm{T}}$, V_{T} is the threshold voltage), the device is insulating and almost no current flows (cut-off region). Of course the semiconducting material and its resistance affect this small amount of current flow.

When the gate is biased so that a sheet of charge is formed between the source and drain, channel is accumulated and current can flow through the channel. The amount of charge flow depends on the magnitude of $\mathrm{V_{DS}}$. At low drain voltages ($V_{\mathrm{GS}} - V_{\mathrm{DS}} > V_{\mathrm{T}}$), the current increases linearly with the drain voltage, according to the Ohm´s law. In this condition, devices is said to be in linear region, and can be modeled as a resistor whose resistivity is determined by the mobility and geometrical factors ($\mu\frac{W}{L}$), where W and L are the channel width and length [157]. The current in this region is indicated as 3.1

$$I_{\mathrm{D}} = \frac{W}{L}\mu.C_{\mathrm{i}}(V_{\mathrm{GS}} - V_{\mathrm{T}} - \frac{V_{\mathrm{DS}}}{2})V_{\mathrm{DS}} \tag{3.1}$$

Similar to c-Si transistors, as $\mathrm{V_{DS}}$ increases, the channel current increases until the field from the drain cancels the gate field and applies less than the threshold field ($V_{\mathrm{GS}} - V_{\mathrm{DS}} < V_{\mathrm{T}}$). At this point, $\mathrm{I_D}$ slows its rate of increase and the device appears to saturate. At this point, the saturation current can be determined by substituting $\mathrm{V_{DS}}$=$\mathrm{V_{GS}}$-$\mathrm{V_T}$ in the linear region equation and simplifying to determine:

$$I_{\mathrm{D}} = \frac{1}{2}\frac{W}{L}\mu.C_{\mathrm{i}}(V_{\mathrm{GS}} - V_{\mathrm{T}})^2 \tag{3.2}$$

For better understanding of the organic transistor behavior, its operation is separated into three regions. The schematic diagram of the current flow in an OTFT with the operation regions is shown in Figure 3.9.

Figure 3.10 shows the structure and operating regions of NMOS c-Si FET and P-type OFET.

3.4.2 Physical structure

The physical structure of an OTFT requires at least four layers; semiconductor, metal for source/drain, insulator and another metal for gate. Depending on the relative

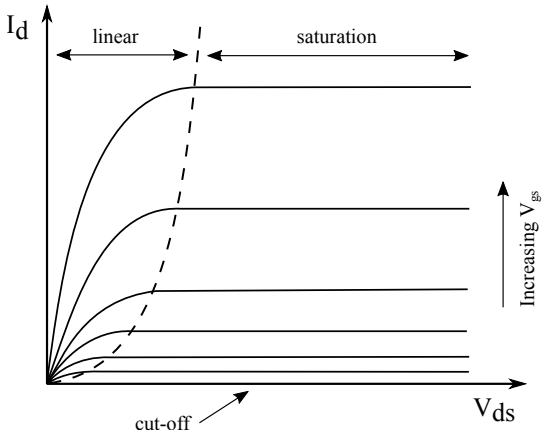


Fig. 3.9 I-V transfer curves of an OTFT separating the operation regions

placement of these layers, there are four common architectures of bringing these stack of layers together: Bottom-Gate Bottom-Contact (BG-BC), Bottom-Gate Top-Contact (BG-TC), Top-Gate Bottom-Contact (TG-BC), and Top-Gate Top-Contact (TG-TC, as shown in Figure 3.11. These can be categorized as two topologies: coplanar and staggered.

Coplanar stands for a charge carrier injection from the edges of the source/drain contacts (small injection area) coplanar to the channel. BG-BC and TG-TC architectures correspond to this category. In contrast, in staggered structure, the carrier injection takes place on a large area and must cross the semiconductor layer in order to reach the channel BG-TC and TG-BC belong to this category, what leads to a larger channel on-resistance.

Every structure has its advantages and disadvantages, and depending on semiconductor material and fabrication process, some architectures have priorities over the others. For example, the presence of an energy barrier at the interfaces between the organic semiconductor and the source and drain contacts is expected to impede the exchange of charge carriers between the contacts and the semiconductor. Experiments and simulations have shown that for the same energy barrier height, TFTs with a staggered structure have the advantage of being less affected by this energy barrier than TFTs with a coplanar structure [158]–[161]. However, in case of the BG-BC structure, the effect of the energy barrier on the carrier exchange efficiency can be substantially reduced by modifying the surface of the source and drain contacts with a thin organic monolayer carrying an appropriate dipole moment [162] or with a thin metal oxide [163]–[165].

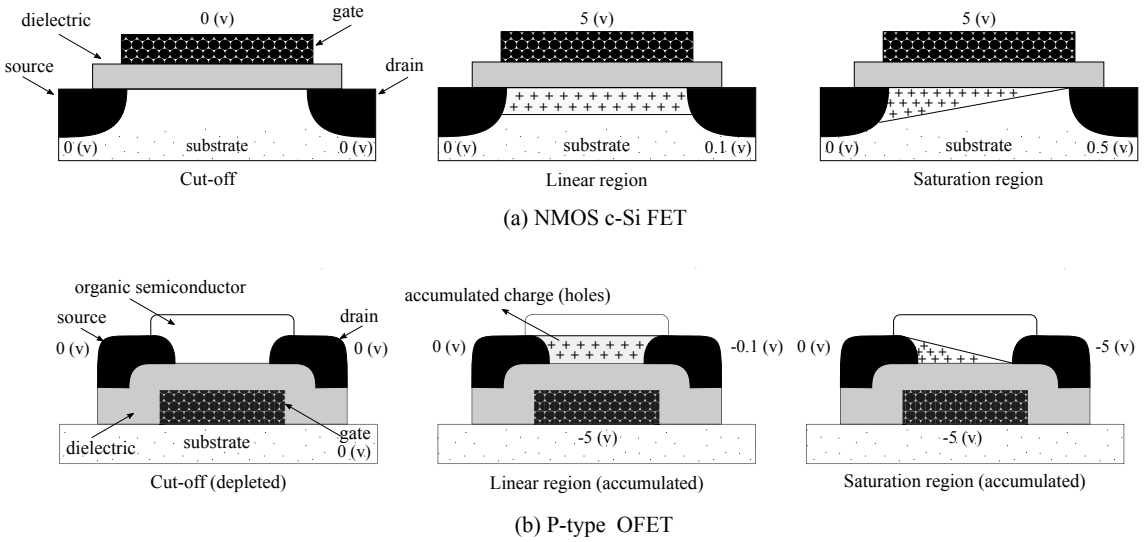


Fig. 3.10 FET structure and regions of operation

An important advantage of the BG-BC structure is that the gate dielectric layer and the source and drain contacts are prepared before the organic semiconductor is deposited. The reason why this is important is that many high-mobility organic semiconductors, especially vacuum-deposited small-molecule materials, but also many high-mobility polymers, adopt a thin-film micro-structure that is very sensitive to external perturbations. For example, vacuum-deposited pentacene films undergo an irreversible phase transition, associated with a substantial drop in carrier mobility, when exposed to organic solvents, such as those employed for the solution-based deposition of polymer gate dielectrics and in photolithographic contact patterning processes [166]. With the BC-BG structure, methods involving solvents and/or thermal treatments can be safely employed to prepare the gate dielectric and the contacts without harming the semiconductor layer. However, this configuration has the disadvantage that the organic semiconductor is deposited on two different materials simultaneously: the gate dielectric and the source/drain contacts, so the morphology of the organic thin film can be disrupted by the non-uniformity of the prior profile and to the wetting/dewetting processes due to different surface tension. Moreover, an encapsulation is often required to protect the semiconductor from oxygen/moisture.

In BG-TC structure, in which S/D electrodes are printed after the semiconductor layer, the contact resistance is reduced. Furthermore, typical organic semiconductors have a hydrophobic surface, which can cause the S/D electrodes to dewet, resulting in the loss of the line integrity, what is a critical aspect for printing narrow source and

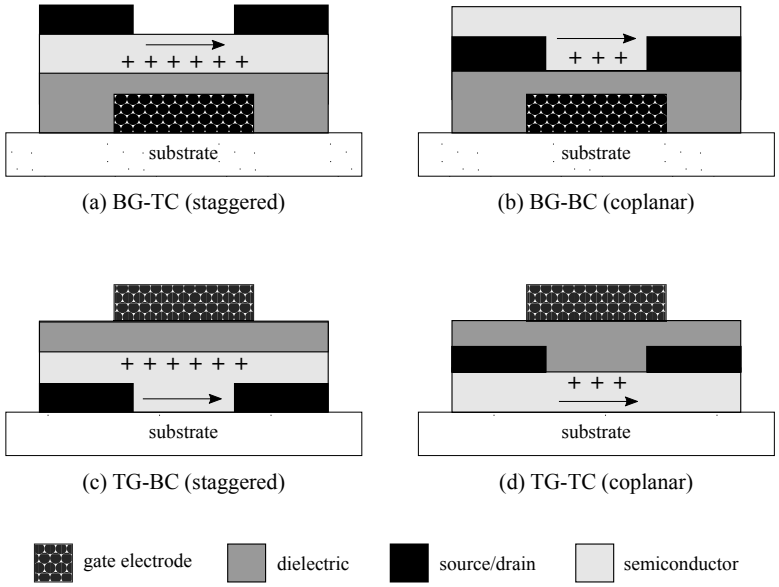


Fig. 3.11 Schematic cross-section of common OTFT architectures

drain patterns. It has to be taken into account that the mobility and threshold voltage of OTFTs can exhibit thickness dependence.

In staggered structures, the related contact resistance can be modeled with the current-crowding concept [167]. The so-called TG-BC architecture looks more like a traditional MOSFET. Here the semiconductor deposition is the second process step meaning that it has to withstand subsequent steps as well, and the layers deposited afterwards act as passivation barriers, protecting the semiconductor.

In terms of process integration, TG-BC and TG-TC structures are the most challenging, as the semiconductor layer is deposited underneath. In this case, the selection of materials and solvents is crucial. The subsequent deposition of the dielectric material can either damage or unintentionally dope the underlying organic semiconductor.

3.4.3 Characterization and modeling

Modeling of organic transistors provides a common language for the discussion of the characteristics and behavior of the device. The parameters measured in device characterization are the raw material with which the device behavior, as well as, an insight about the physical process can be summarized. In order to build complex circuit and estimate the optimized performance, it is necessary to simulate the circuit with the corresponding model of the OTFTs. Those models can be formulated at different levels (electrical, logical, temporal, etc.)

IEEE 1620-2004 standard [168] lays out a procedure for OTFT parameter extraction which fits device curves to simplified large signal long channel crystalline silicon device model with some adaptations. It defines ways to extract the figures of merit of OTFTs. Those include the threshold voltage (V_T), the charge carrier mobility ( ), I_{on}/I_{off} ratio, and contact resistance (R_c).

The relatively high variability observed in the characteristics of OTFTs makes it challenging to have a stable and reliable model with low tolerance. Thus, one of the main goals in organic electronic domain is to obtain a model as accurate as possible for organic transistors, while its parameters should ideally keep some physical meaning. In order to model the electrical behavior of the OTFTs, the device needs to be electrically tested and characterized to extract the desired parameters. The main figures of merit for characterization of organic FETs are I-V and C-V curves, which are shown in Figure 3.12

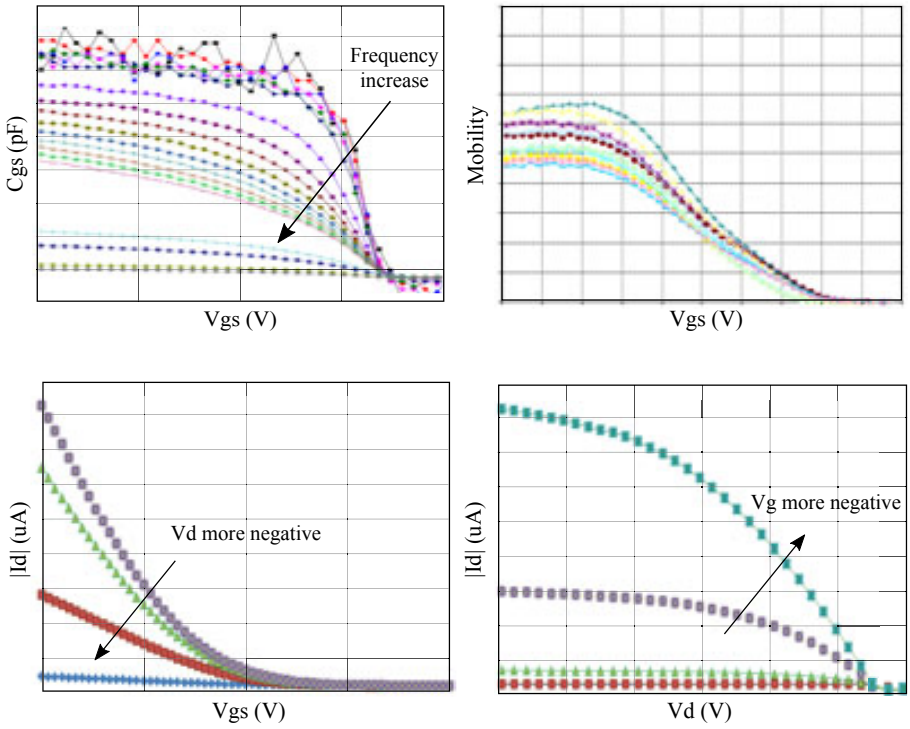


Fig. 3.12 OTFT figures of merit

Field-effect mobility ( ) parameter is the drift velocity of the charge carrier flowing through the semiconductor from source to drain when an electric field is applied. This parameter strongly affects the operation speed of the transistor and has a fundamental importance when fast logic circuits are desired. Additionally, ( ) is used as a figure of merit for evaluating the performance of semiconductor materials. A high mobility, as

well as high I_{on}/I_{off} ratio is desirable qualities for OTFTs. There are several ways of extracting the mobility from I-V transfer curves in the literature. The V_{GS}-dependent mobility can be calculated from:

$$\mu = \frac{L}{WC_{i}V_{D}}.\frac{\partial I_{D}}{\partial V_{G}} \tag{3.3}$$

Threshold voltage (V_T) of OTFTs does not have a unique definition, which is universally accepted by the community. Measurement of V_T is complicated due to relatively gradual turn-on of the device. In c-Si, the threshold voltage is defined as the point, where the inversion occurs in metal-insulator-semiconductor capacitance. In contrast, because organic semiconductor never achieves inversion, hence no definite threshold voltage can be defined, but only a voltage at which the device begins accumulating charges (referred to flat band voltage in c-Si devices) and current flowing.

Several approaches were reported to extract the threshold voltage. One is to obtain the gate voltage when the current deviates from the exponential character expected from purely diffusive transport, as shown in Figure 3.13 (a). Another method is to extrapolate the linear part of $\sqrt{I_D} - V_{GS}$ curve to intercept on the V_{GS} axis, shown in Figure 3.13 (b). Another method to extract the threshold voltage is by measuring capacitance-voltage characteristics of the C-V curve, when the drain and source are held together [157].

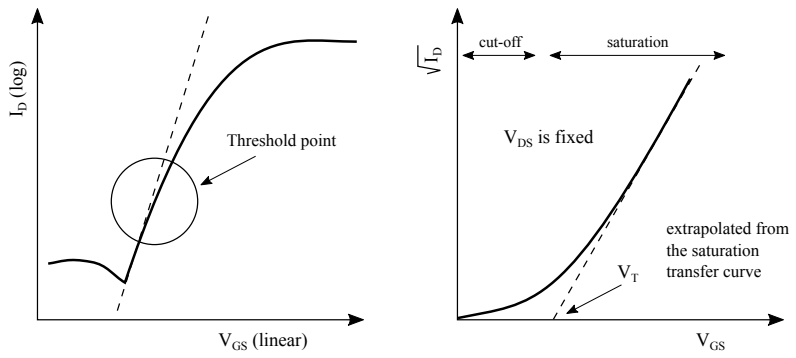


Fig. 3.13 Threshold extraction methods

Contact resistance (R_C) is an inherent limitation to the performance of the OTFTs due to the energy level mismatch between the organic semiconductor HOMO and the work function of the contact metal. It includes all series resistance that does not scale with channel length. This resistance includes the drain and source composition, the

interface between the semiconductor and the contacts, and edge induced morphological or other structural changes, which change the resistance. As the channel length of organic thin-film transistors (TFTs) is reduced in order to improve the dynamic TFT performance, the total resistance and hence the effective field-effect mobility and the transconductance of the TFTs become more and more limited by the contact resistance, rather than by the channel resistance.

Studies about contact resistance in OTFTs are extensively reported in the literature [169]–[171]. Extraction of contact resistance is found to be crucial in characterization of organic transistors as it obscures mobility extraction. There are several methods such as scaling approach [172], gradual channel approximation [173], and transmission line [174] exist in the literature for extracting the contact resistance of the OTFTs.

According to transmission line method, the total resistance of an OTFT is given by sum of the contact resistances (R_{S} and R_{D}) and the channel resistance (R_{ch}), where R_{ch} scales with the channel length, as shown in Figure 3.14.

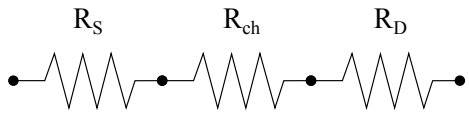


Fig. 3.14 Schematic of contact and channel resistance of OTFT

According to [175], the total on-resistance of the transistor can be shown as:

$$R_{\mathrm{total}} = (\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{DS}}}(L))^{-1} = R_{\mathrm{D}} + R_{\mathrm{S}} + R_{\mathrm{ch}}(L) \tag{3.4}$$

By assuming that the device is symmetrical, ($R_{\mathrm{S}} = R_{\mathrm{D}} = R_{\mathrm{C}}/2$), [175] represents the 3.4 as:

$$R_{\mathrm{total}} = R_{\mathrm{C}} + r_{\mathrm{ch}}.L \quad with: \quad r_{\mathrm{ch}} = \frac{1}{W\mu_{\mathrm{FE,i}}C_{\mathrm{i}}(V_{\mathrm{GS}} - V_{\mathrm{T,i}})} \tag{3.5}$$

Where, $V_{\mathrm{T,i}}$ is the intrinsic threshold voltage and $\mu_{\mathrm{FE,i}}$ is the field-effect intrinsic mobility.

More details about the physics, structures, operation, and modelling of OTFTs and organic semiconductors can be found in these publications [176]–[181].

3.5 Digital logic families

Process variation is an important drawback of many existing printing technologies. These variations are result of the adopted low-temperature, and low-cost manufacturing approach, which limits the control over the process. Also, some intrinsic limitations of the organic materials can cause the variation in device performance. All these variations can lead to considerable deviation from the desired performance, which are called *"soft faults"* [182].

Besides, *"hard faults"* (permanent faults) may also be introduced during fabrication, as defects, or they may occur during the lifetime of the device and circuits. Well-known physical phenomena that lead to operational hard faults are the breakdown of layers such as gate insulator, and electro-migration. Defects introduced during the fabrication, such as, unexpected material drop or dust onto the substrate, and large layer-to-layer misalignment, often manifest themselves in a similar fashion. In general, high resolution printing technologies are more prone to these defects, since the margin for error is smaller. Consequently, these faults make it challenging to have a robust organic circuit with high complexity.

One way to control the soft and hard faults, and hence improving the yield, is to optimize the fabrication process in respect to variability and layer registration accuracy, which is more related to technology side and is not the topic of this thesis. On the other side, hard faults can be monitored or controlled largely by circuit design approaches (such as fault tolerant techniques). For example, large number of transistors in a circuit enhances the sensitivity to hard faults, hence, the probability of circuit failure increases. Therefore, the proper selection of a design logic style, able to take into account the specific technology variability, can improve dramatically the yield and degree of complexity that can be achieved in circuits.

3.5.1 Complementary MOS technology

Complementary Metal Oxide Semiconductor (CMOS) logic devices, which consist of both NMOS and PMOS transistors, are the most common devices used today in the high density, large number transistor count circuits found in everything from complex microprocessor integrated circuits to signal processing and communication circuits.

Static CMOS

Static CMOS in the most common design style of complementary MOS technology, in which p-type and n-type transistor networks are used to connect the output of

the logic device to the either the power supply or ground rails for a given input logic state. This structure is popular because of its inherent high noise margins, lower power requirements, high operating clock speed, and ease of implementation at the transistor level. There never exists a direct path between V_{DD} and GND, which means the static power is almost zero, depending on the slope of the digital signals) and not taking into consideration leakage currents. Figure 3.15 depicts the schematic and NAND2 implementation of static CMOS logic style.

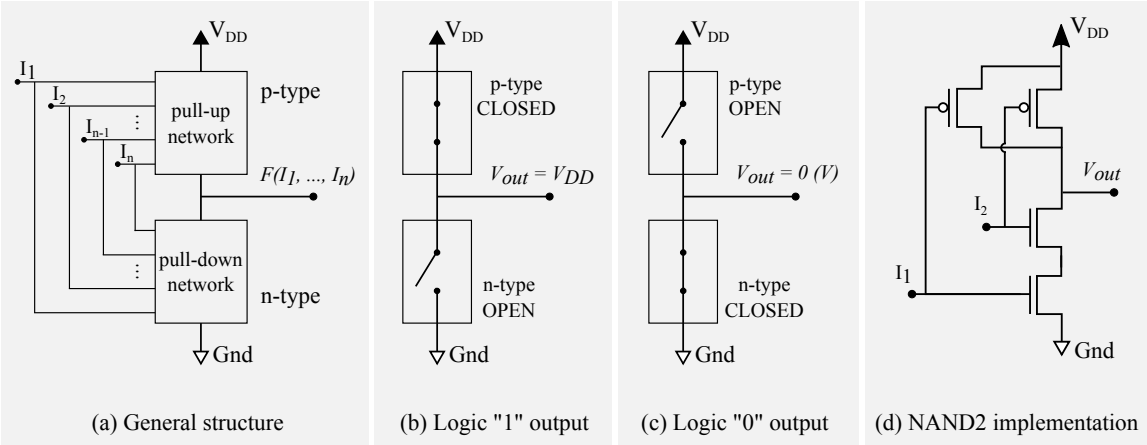


Fig. 3.15 Static CMOS logic style operating principle

The typical static and dynamic behavior of the inverter built by this logic style is shown in Figure 3.16 (b, c). Some important parameters in the static in-out characteristics of an inverter are the separation of logic "high" ($\mathrm{V_{OH}}$), and "low" ($\mathrm{V_{OL}}$) level, the maximum gain ($\mathrm{A_{max}}$) and the position of trip point ($\mathrm{V_{trip}}$). The definition of each of the parameters is illustrated in Figure 3.16 (b).

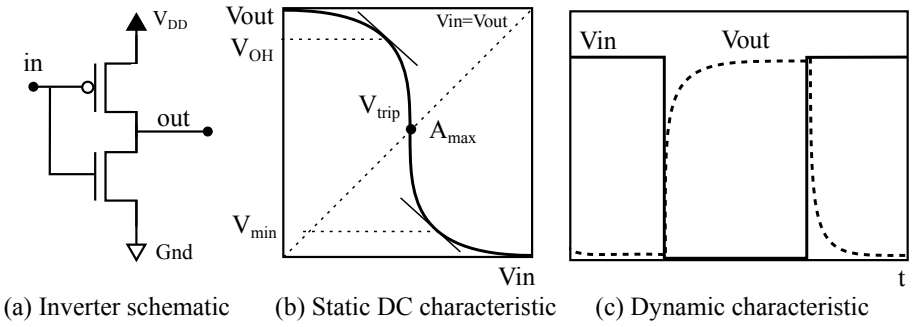


Fig. 3.16 Static CMOS logic style characteristics

The static realization of CMOS circuits is expensive in terms of area, due to the fact that every logic gates requires PMOS pull-up network and NMOS pull-down network, therefore, the total number of transistors is twice the number of inputs ($2N$, where N is the number of inputs). Area is an important issue in printed electronics, where conservative design rules and large distance between n-type and p-type semiconductor area must be observed. The high transistor count results then in a strong increase in the area of the printed static digital circuits with higher complexity. For instance, a master-slave D flip flop, consisting of 2 Inverters and 8 number of NAND2 gates, requires 36 transistors, which is fairly a large number. Large number of transistors enhances the circuit sensitivity to hard faults, hence, the probability of circuit failure increases.

Dynamic CMOS

An alternative to static CMOS digital design style is dynamic logic, which enables implementation of more compact circuits. Dynamic logic is distinguished from static one in that it uses a clock signal in its implementation of combinational circuits. This clock is used to synchronize transitions in sequential logic circuits and the output is driven high or low during two distinct phases of the clock cycle. Figure 3.17 shows the dynamic logic implementation of a CMOS 2-input NAND.

In the first phase, when clock is low –*setup/precharge phase*–, the output is driven high regardless of the input values. In this phase the load capacitor of the gate is charged. Because the transistor at the bottom is turned off, it is impossible for the output to be driven low during this phase. When the clock is high – *evaluation phase* – the output will be pulled low or stays high according to the NMOS pull-down combinational logic. Figure 3.17 depicts the schematic and NAND2 implementation of dynamic CMOS logic style.

Dynamic True Single Phase Clock (TSPC) flip flop [183] was designed and fabricated on flexible plastic substrates with high performance OTFTs, based on small molecule organic semiconductors in solution [184], consisting of only 11 transistors, compared to the 36 transistors needed for a static master-slave D flip flop.

Despite the speed and low area occupation, dynamic logic has a few potential limitations and bottlenecks that static logic does not have. Dynamic logic requires a minimum clock rate slow enough that the output state of each dynamic gate is refreshed before the charge in the output capacitance leaks out enough to cause the digital state of the output to change. In this style, to be able to implement dynamic logic, the technology needs to feature p-type OTFTs with a negative threshold and

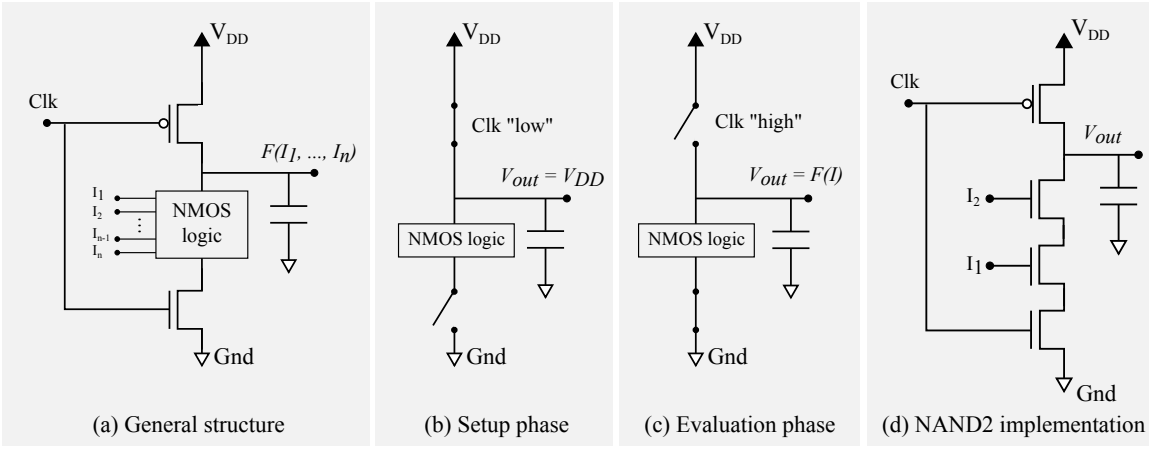


Fig. 3.17 Dynamic CMOS logic style

n-type OTFTs with a positive one, so that both types of transistors can be well switched-off. A comparative analysis of static and dynamic CMOS Logic design is provided in [185].

Transmission gates

Another alternative to reduce the transistor count is complementary Transmission Gates (TG) style, which is based on using a p-type and n-type transistors together for passing a logic. For silicon transistors, typically n-type transistor passes "0" logic level well but, "1" logic poorly, while p-type ones work on the contrary. Thus a combination of n- and p- type transistors, being able to pass "0" by NMOS, and "1" by PMOS is a clever way to obtain pure "0" and "1" signals. Figure 3.18 depicts the schematic and a 2-bit multiplexer implementation of transmission CMOS logic style.

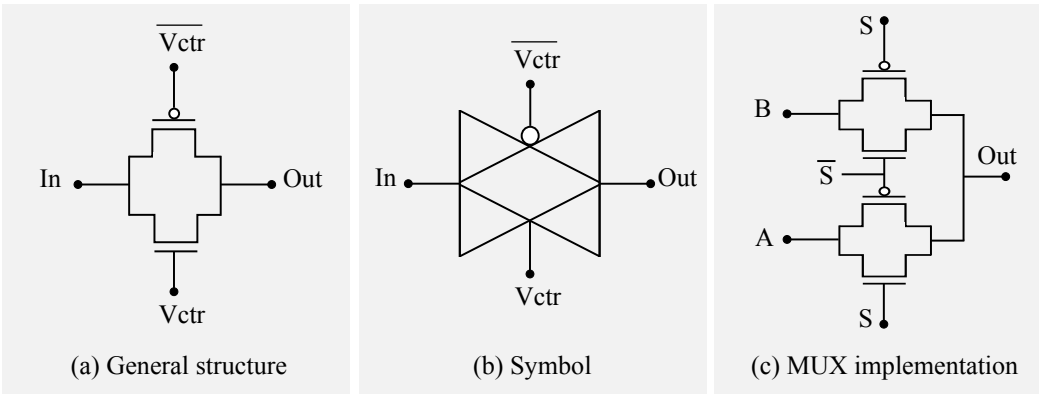


Fig. 3.18 Transmission gate CMOS logic style

Compared to fully-static implementations, the TG-based flip flop has a lower number of transistors and therefore, it is smaller and less vulnerable to parametric variations. However, in TG-based flip flops, it is important to keep the TGs switched off at $V_{GS} = 0$. In other words, there must be a well-defined range of V_{GS} (around zero) where both p-type and n-type transistors are off, which is normally not the case for pentacene p-type OTFTs with positive V_T. Consequently, whenever the Clk signal goes off, TGs are likely to go from a fully-on state to slightly-on, instead of turning completely off. This can easily result in problems such as race between the master and the slave flip flops. From this perspective, static flip flops are more robust with respect to threshold voltage variations [182].

3.5.2 Unipolar logic style (PMOS)

Although complementary logic has demonstrated reliable and robust results in development of organic circuits, there are still some limitations in respect to materials and technologies to implement CMOS design. Firstly, n-type organic semiconductors are still not as mature as p-type ones, showing lower carrier mobility, therefore, there is not a large number of them comparing to p-type organic semiconductors. Another limitation is related to lack of general technological processes that are able to integrate and bring together both OTFT types in a common complementary flow onto the same substrate.

Besides, many of the printing technologies are limited to the feature sizes of some microns or tens of micron, which leads to fairly large transistor. So, as the number of transistors in the circuit increases, the occupying space on the substrate, as well as hard faults, increases. This is even more challenging for CMOS technology, in which two networks of p-type and n-type transistors are responsible for realizing the functionality in a complementary fashion.

That being said, an alternative logic design style for printed electronics, which uses only P-type organic transistor, is ratioed PMOS technology. In this style, the drive network of transistors is responsible for realizing the logic, and the active load, which is always one single p-type transistor, connects the output to GND. The functionality of the circuit depends on the load connection manner, and the ratio between the dimension of drives and load transistors.

This is similar to the silicon n-MOS logic used in the 1980s, except that in the silicon technology, one could use the electrical doping of the semiconductor to define a different threshold voltage for the driver and load transistors, while in organic TFT

technology no reproducible method is known to control the threshold voltage of two adjacent transistors independently by doping.

Ratioed PMOS style helps reducing the number of transistors to almost half ($N+1$, where N is the number of inputs), and also patterning and materials stability issues are minimized, since only one type semiconductor is used. Despite reducing the transistor count and occupying area, this logic style suffers from some drawbacks: Firstly, due to the fact that the load transistor is always "on", there is a path between V_{DD} and GND, when the drive transistor is "on". This leads to a higher static power consumption comparing with CMOS style. Secondly, the output rise and fall times are asymmetrical because of the asymmetrical drive and load networks. Furthermore, there is a playoff between high switching speed, which requires a large load transistor, and a high noise margin, which requires a small load transistor.

A critical parameter of FET operation is the threshold voltage ($\mathrm{V_T}$). If this is negative for a p-type device, the transistor is denoted as an enhancement device. This is because the transistor is normally off when the gate voltage is zero, and it is switched on by applying a gate voltage that enhances the channel charge. If the threshold voltage is positive for a p-type FET, then the device is normally on when the gate voltage is zero, and this is called depletion device, because the channel must be further depleted to switch the device off. According to the polarity of threshold voltage, there are two ratioed logic style: 1) Zero-$\mathrm{V_{GS}}$, 2) Diode-connected, either of which has pros and cons based on device characteristics and circuit performance.

Zero-$\mathrm{V_{GS}}$ load logic family

In a p-type-only technology, it is favored that the drain–source current of the load transistor be kept constant as much as possible. This can be done by connecting the gate of the load transistor to its source, being called $Zero - V_{\mathrm{GS}}$ structure. This architecture is also known as depletion-load inverter, since it only works using two depletion-mode transistors with positive threshold voltage ($V_{\mathrm{T}} > 0$). The schematic of an inverter for this style is depicted in Figure 3.19 (a).

When the input is set to a low value ($V_{\mathrm{in}} = 0$), the drive transistor has a large negative (V_{GS}), hence a hole-conducting channel is present and the channel resistance of drive OTFT is very small compared to the channel resistance of load one with $V_{\mathrm{GS}} = 0$. Therefore, the resistive divider between drive and load transistors pulls-up the output close to V_{DD}. Obviously, the output never reaches to V_{DD}, since there is always a voltage drop on the $Zero - V_{\mathrm{GS}}$ load.

When the input value rises to V_{DD}, both drive and load transistors have $V_{\mathrm{GS}} = 0$. In this case, the output is desired to be as low as possible but drive transistor is still on, and V_{out} can be calculated by a voltage-divider in Equation 3.6. In order to pull-down the output value as low as possible, the load transistor should be sized much larger than the drive one ($\simeq$ 5 to 10 times), so that $R_{\text{on-drive}} >> R_{\text{on-load}}$. This is why this style is known as **ratioed** PMOS.

$$V_{\mathrm{out}} = V_{\mathrm{DD}} \cdot \frac{R_{\text{on-load}}}{R_{\text{on-drive}} + R_{\text{on-load}}} \tag{3.6}$$

The typical static behavior of the inverter built by this logic style is shown in Figure 3.19 (b). The separation of logic levels depends strongly on the drive to load ratio. It is desired to obtain a low-to-high logic distance as close as $\mathrm{V_{DD}}$. The maximum gain ($\mathrm{A_{max}}$) is the maximum slope of the in-out curve and depends on the transconductance of the drive transistor and the output resistance. The trip point ($\mathrm{V_{trip}}$) is where the input and output voltages are the same, and is ideally similar to the maximum gain point, which should be at the center of the supply range. In this logic style, the trip point usually does not occurs at the center of supply voltage, which is due to the positive threshold of drive transistor. This asymmetric position of the trip point strongly affects the noise margin values.

Regarding the dynamic behavior of this logic family, it is easy to understand that the pull-down delay is much larger than the pull-up delay, as the pull-down current provided by $Zero - V_{\mathrm{GS}}$ load is much smaller than the transient pull-up current provided by the driver [186], shown in Figure 3.19 (c).

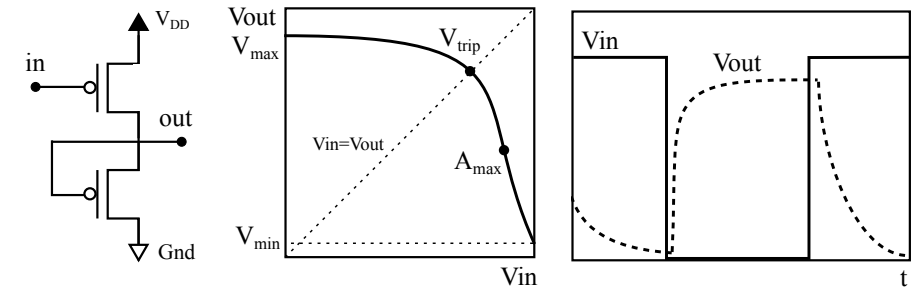


Fig. 3.19 $Zero - V_{\mathrm{GS}}$ logic style

Diode-load logic family

An alternative unipolar ratioed logic style, which is compatible with enhancement-mode transistors with negative threshold voltage ($V_{\mathrm{T}} < 0$), is diode-load or enhancement-load logic family, because a transistor with shorted gate-drain has diode-like current–voltage characteristics. The schematic of an inverter for this style is depicted in Figure 3.20 (a).

When the input is low, the V_{GS} of both the drive and load transistors are initially equal to $-V_{\mathrm{DD}}$. According to the voltage divider in Equation 3.6, by sizing the drive OTFT larger than load one, one can pull-up the output node to V_{DD}. As the input arises to high value, the load transistor will be at first heavily on and will easily pull-down the output node against the driver, which is off.

The typical static behavior of the inverter built by this logic style is shown in Figure 3.20 (b). As it is seen, the separation of logic levels is not as high as Zero-V_{GS} style, and the maximum gain depends on the transconductance of both drive and load transistors. The position of the trip point is often asymmetric also in this style, because of the fact the large drive transistor switches-on very rapidly when the input goes low.

The best feature about this logic style is switching speed. As the load transistor is diode-connected, a fully on transistor provides at the beginning of the transient the pull-down current. The pull-down and pull-up delay in this style is pretty faster than in Zero-V_{GS} logic (Figure 3.20 (c)).

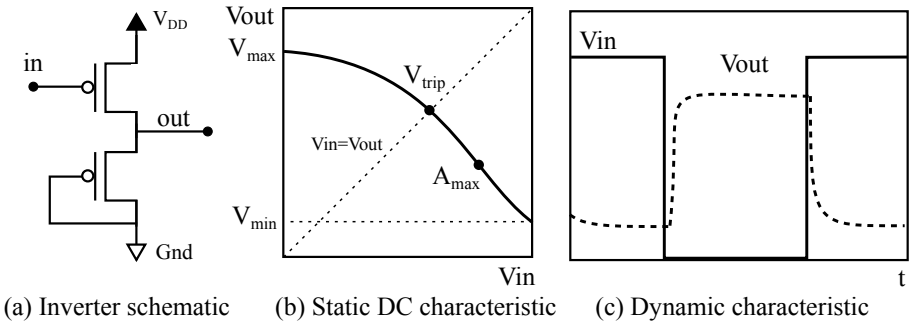


Fig. 3.20 Diode-load logic style

The Zero-V_{GS} inverter yields a relatively high gain and noise margins as compared to the diode-load inverter. Although there are some bottlenecks in terms of speed and robustness against large threshold voltage variation, the higher gain of the former one justifies why it is nowadays very common in an OTFT-based circuit design. Moreover, pentacene is the benchmark semiconducting material for organic electronic circuits, and pentacene OTFTs often behave as depletion-mode p-type transistors with positive

threshold voltage ($V_T > 0$). Thus, Zero-V_{GS} is more frequently used in the state of the art organic circuits.

The availability of second threshold voltage would be beneficial for the characteristics of the inverters, similar to the silicon n-MOS logic used in the 1980´s. One option to obtain multiple threshold voltage is the addition of a second gate in the technology. Several publications address the structure, characteristics and benefits of dual-gate OTFTs in building blocks for digital circuits [187], [188]. The main advantages of dual-gate OTFTs are increasing the noise margins and shifting the trip point towards $V_{DD}/2$.

3.6 Integrated circuit design: configurable circuit

Development of organic circuits and systems has outgrown the laboratory and is emerging at this very moment. Recent publications have demonstrated complex analogue and digital organic electronic circuits, such as RFID tags [189]–[191], analog building blocks for organic smart sensor systems [192], Analog to Digital Converters (ADCs) [193], organic comparator [194], 8-bit microprocessors with 3381 transistors [195] that has been recently advanced [196], flexible large-area temperature sensor [197], a 240-stage shift register employing 13440 OTFTs [198], a high-frequency amplitude-modulated demodulator [199], and etc. These achievements, roughly comparable to early stage of silicon electronics in 1980s, are expanding the current envelope of integrated organic transistor circuit designs.

Regarding the semi-custom cell-based design methodology, some works addressing the design of standard cell libraries for organic and printed electronics have been presented in recent years. Uppili *et al.*, in [200], and Huang and Cheng, in [201], propose standard cell libraries for flexible substrates. However, both of the works are based on inorganic a-Si:H TFTs. Also, Huang and Cheng have not manufactured designs with the proposed library and, although Uppili *et al.* explore an automated design flow, it is not clear if the proposed library is based on the ASIC data models and formats, which would make it difficult to use their library into the VLSI tool chain.

Since the main focus of this thesis is on development of semi-custom field-configurable circuits for printed electronics, I provide three most important and related state of the art organic, flexible customizable circuits.

In 2011, Ishidia *et al* presented User Customizable Logic Paper (UCLP), with Sea-Of-Transmission-Gates (SOTG) of 2-V organic CMOS and inkjet printed interconnects. The proposed UCLP can be used for prototyping of large-area electronics

and educational applications. Learners can study and experience the operation of integrated circuits by using inkjet printing, which provides the field-configurability of the chips. In UCLP, papers that contain an array of vias and organic SOTG film are stacked (Figure 3.21 (a)). The 2-V CMOS transistors, with minimum channel length equal to $20\mu m$, are prefabricated on polyimide film. Figure 3.21 shows the 8×8 SOTG cell array and the details of a single cell [27].

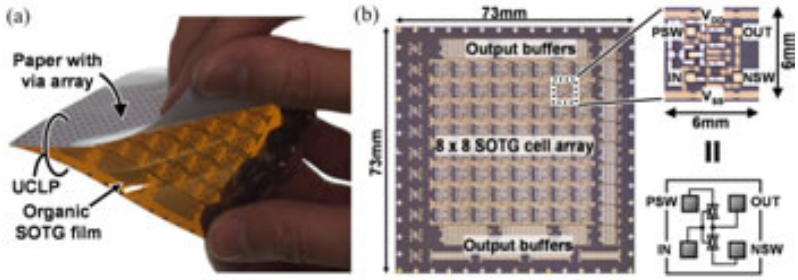


Fig. 3.21 User customizable logic paper

In 2014, Myny *et al* presented Print-Programmable Read Only Memory (P2ROM) [202] by using a hybrid oxide organic complementary thin film technology, in which the n-type transistors are based on a solution-processed n-type metal-oxide semiconductor, and the p-type transistors use an organic semiconductor, both with channel length equal to $5\mu m$ [203]. Figure 3.22 depicts the die picture of the instruction generator and micrograph image of the inkjet printed area of the instruction generator (Source: [202]).

In 2014, Sou *et al* presented Programmable Array Logic (PAL) [204], in which array of transistors with a channel length of $5\mu m$ of the same construction as used in Plastic Logic´s high yielding and uniform active matrix manufacturing process [205], [206] were used. This is a mature and well-established process, based on solution processing and laser patterning, which yields to high density circuits. The PAL featured 8 inputs, 8 outputs, 32 product terms, and have 1260 p-type polymer transistors in a 3-metal process using diode-load logic. Conductive silver wires and PEDOT:PSS resistors between transistors or logic blocks were inkjet printed for quick configuration of transistors. A single circuit design of 2:4 demultiplexer driving an electrophoretic ink (E-ink) display up to $70 \times 70mm^2$ on a single flexible transparent plastic foil was demonstrated on the PAL, shown in Figure 3.23 (Source: [204]).

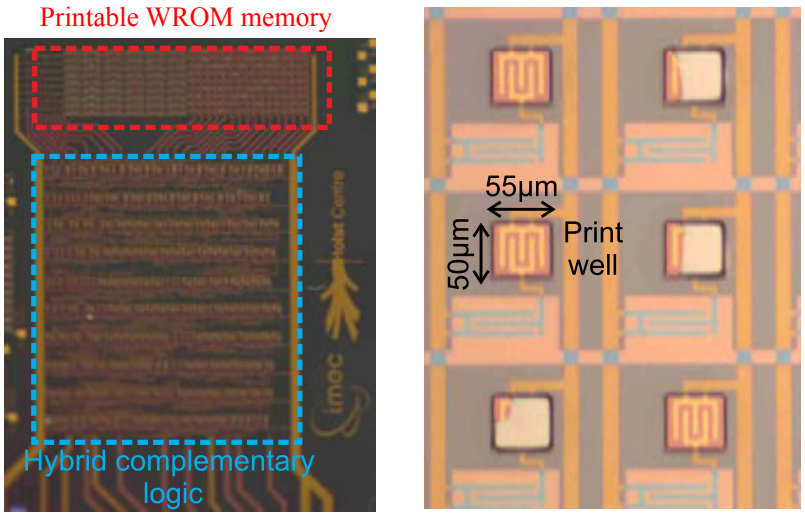


Fig. 3.22 Die picture of the instruction generator and a micrograph image of the inkjet printed area

3.7 Summary

Organic synthetic chemistry has yielded a tremendous variety of materials suitable for organic electronics. Several inks with improved processability, performance, stability, and throughput have been and certainly will continue to be developed. Organic semiconductor materials (polymer, small molecule, and polymer-small molecule blends) have been developed as the key material for building organic thin film transistors on flexible substrates. In the recent years, this research field has been enabling novel, thin, lightweight and extremely cost-efficient electronic systems.

The mass printing techniques (flexography, gravure, offset, and screen printing) have a long history in printing on paper and textiles, to which printing on polymeric foils can be added now. Common benefits are the widespread and well-understood processing steps and conditions required for large volumes to be printed, up to 200,000 m/h for offset printing. A general and important drawback of these techniques, in particular for fast operating electronic devices meeting Moore's law, is the low resolution, typically down to 20um.

The limited resolution and quality of the mass printing techniques has led to the request for new, high-throughput R2R lines integrating more recently developed, alternative an high-resolution patterning lithography techniques. Especially for these high-resolution patterning strategies, the dimensional instability, deformations and variations in thickness of the foils contribute to the given challenges of developing large-area, flexible electronics patterned by a R2R strategy. Other than in batch mode,

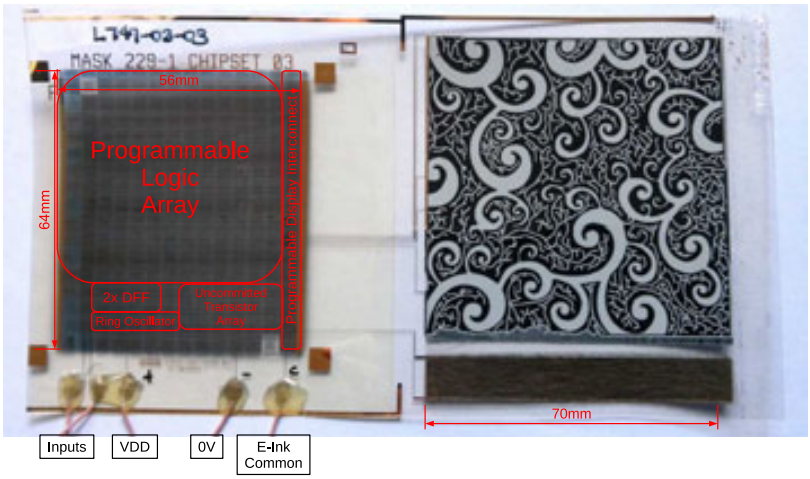


Fig. 3.23 Photograph of the 2:4 demultiplexer on the PAL with its 70mm by 70mm E-ink display on the same flexible plastic substrate

accurate registration and therefore alignment of a multilayer device is not economically feasible.

Inkjet printing is a simple process and is easily combined with mass printing and high-resolution patterning strategies. It is a low-cost, non-contact, low-impact patterning technique benefiting from the flexibility of digital mastering. Digital printing is more customizable, produces less waste and reduces fabrication costs. The limited resolution of conventional IJP (approximately 20um) has been compensated by modern digital printing techniques, such as electrohydrodynamic inkjet, super-fine inkjet, aerosol jet, and etc., with feature size down to sub-micron. However, these techniques are not developed to print complex organic devices like OTFTs, but only for circuit metallization and fine line printing.

Photolithography is probably the most established patterning technique with an extreme resolution bandwidth, suitable for fabricating organic thin film transistors. However, the high initial and processing costs combined with a relatively low throughput and patterning area make it less attractive for low-cost fabrication of large-area and flexible devices. Furthermore, substrates and organic materials are exposed to corrosive etchants, high-energy radiation, and high temperatures during processing.

Recent improvements in development of field-effect transistors using organic materials have led to design and fabrication of complex digital and analog circuits. However, soft and hard faults have been the main bottlenecks for developing robust and reliable printed electronic circuits. Those faults can either be compensated by material and technological improvements, which are already being addressed by the community,

or they can be minimized by adopting circuit design methodologies and selection of proper logic family for digital blocks.

Selection of logic family depends on the available transistor types and fabrication process in the printing technology. Static CMOS technology is the most common and reliable one with very low static power and high performance, but it is expensive in terms of area and transistor count. This can lead to lower yield at transistor level, since increasing the number of transistors increases the probability of hard faults. Dynamic and transmission gate logic families overcome this challenge by reducing the transistor count, however, they still require both n- and p-type transistors.

Nowadays, most of the technologies are using only p-type transistors, due to its higher mobility and availability, as well as, fabrication simplicity in comparison with CMOS style, which brings together both n- and p-type organic semiconductors on the same substrate. Therefore, ratioed unipolar (p-type) logic style helps reducing the transistor count, and increasing fabrication simplicity. According to the transistor operation mode (enhancement or depletion), either Zero-V_{GS} or Diode-load structure should be used.

Zero-V_{GS} is prone to higher gain noise margins as compared to the diode-load inverters, although it is not as fast as its counterpart in terms of stitching speed. Most of the developed cells and libraries in this thesis are implemented through Zero-$V|_{GS}$ p-type ratioed logic family.

The state of the art configurable logic arrays and memories, which are taking the advantages of semi-custom circuit design methodology in ASIC industry, were also introduced in this chapter. All of these promising arrays have been fabricated through mature and high yield printing technologies with small feature sizes, and later were configured by using inkjet printing technique, as a mask-less additive technology.

Chapter 4

DESIGN-TECHNOLOGY INTERACTION

Designing devices and circuits demands a basic knowledge of materials, process and interaction among concepts, tools and technologies coming from different engineering disciplines. Designers are responsible for mapping the application requirements, function and performance, into descriptions that can be fabricated using well-established and standardized technological processes. To facilitate manufacturability, the entire fabrication process for any given technology should be controlled by the foundry. Therefore, process and design engineers use standard rules and formats to exchange information while working independently of each others. This set of information for any given technological process is its Process Design Kit (PDK), and is composed of documentation and a set of files related to a given EDA tool customized for the target technology. These technology-related information could be summarized as below:

- Technology files, describing the different layers definitions available in the target technology;
- Geometrical design rules to provide the knowledge of minimum material width, separation, overlap, and etc. for single or multiple layer(s);
- Compensation rules and patterns to be applied to final layouts in order to provide maximum matching between the fabricated samples with the designed layout.
- Electrical models and parameters for the different basic structures (layers, resistors, capacitors, transistors, and etc.); and
- A library of very basic devices easy to reuse and scale to adapt to different designs.

In a bottom-up approach, there is information moving from a physical level (printing patterns and layers, physical, geometrical and electrical properties and characteristics), passing through a basic device level (connections, resistors, capacitors, diodes, transistors, antennas), up to a component level (parameterized devices, digital cells, analog blocks, special filters). Also, characterization, refinement and modeling steps need to be performed at each abstraction level in order to correctly and efficiently associate them.

In the case of PE, the gap between technologists and designers is larger than silicon-based electronics. The technology side is a compendium of engineering (chemistry, printing, materials...) with a depth knowledge, but difficult to combine in a convergent way to reach a useful and stable technology to address robust enough microelectronics development. In contrast, Electronic engineers are used to work with different approaches; never making their hands dirty in the technology domain. Thus, a PDK allows them to work at well-known higher abstraction levels: from geometrical design rules, electrical parameters/models, characterized basic structures and devices up to higher levels as cell-based design or even HDL-based development.

Moreover, PDK can provide EDA tools to efficiently meet some specific demands that a specific technology may have. As an example, PE designs may have different quality of results by applying distinct drop patterns and ink densities according to previously printed layers [207]. However, this possibility cannot be explored with regular EDA tools (and its consequent data models) and PE designs demand for new tools to investigate this topic. Thus, the PDK is the first bridge and abstraction level between technology and design to avoid circuit designers facing enormous amount of technology-related details and process, while keeping them devoted to reliable circuit design.

In this chapter, the concept of design parameterization for process development as well as its applications in design rules formalization, design of basic devices, and automatic characterization is explained. Then, several physical layout styles of OTFTs for electrical performance optimization are proposed. Afterwards, the complete cell libraries development will be addressed including design, prototyping, and characterization. Finally, full-custom and cell-based semi-custom logic and circuits are developed and some are prototyped as a proof of concept.

4.1 Design for process development

Providing information to feed the PDK, usually requires the generation and characterization of a huge number of test structures. This is a very hard job for any new-born technology specially due to the fact that the PDK always needs to be updated for each minor or major evolutions and improvements in the technology. These evolutions are quite frequent in the emerging technologies such as PE. In order to speed up PDK´s development and updates, it is important to have a systematic methodology (automated when possible) to cover the processes from technology development and characterization to specific PDK generation.

In the following subsections, I address automatic approaches for test structure generations and its subsequent characterization environment.

4.1.1 Parameterized Cells (PCells)

In the way to automate the test structure generation, one of the key concepts in design automation is "Parameterized Cell", or (PCells). The idea of PCells was first proposed by Beahm *et al.* in 1996, and was used for generating dense layout of VLSI circuits [208].

PCell is a piece of code (master cell) whose instantiation or execution by EDA software allows the customization of certain design parameters to address the generation of a physical representation (layout) as a function of such parameters value. Every time a PCell is executed/interpreted, a set of available instantiations (views) for the customized parameters is generated.

The PCell concept is widely used in the design of custom silicon-based microelectronic circuits due to the complexity of the integrated circuits (IC) structures and design rules governing their physical implementation. Although all modern IC foundries provide design kits with libraries of PCells for speeding-up the physical design cycle, the parametrized concept is barely used by the PE community.

The use of PCells-based strategy has many benefits on the PE circuit design phase, being able to quickly generate custom error-free cells. These benefits become even more evident when designing large matrices of devices for their characterization and modelling, where the same type of device (resistor, transistor, etc.) or test structure must appear hundreds of times with different geometrical construction variations.

The procedure to create the test matrices is done through scripting. With only minor modifications in the code, these scripts can be adapted to generate the characterization vehicle for each different cell, just selecting the PCell to instantiate, the parameters

to modify, the range of its values, the step between variations or the number of them. The script can also automatically place the test pads for the electrical probing tips and draw the electrical connections from pads to pins of each specific PCell instance. Apart from the reduction of design time and the correctness-by-construction provided by the combination of PCells and scripts to place it, the strategy that we proposed also provides several advantages:

- *Arbitrary position*: Each time a PCell and its corresponding test pads are placed, the script stores its absolute position in a text file called Test Vehicle Description (TVD). This file will contain the placing position of every cell in the matrix, and will be used as an input for an automatic probe-station used in the characterization environment. If the relative disposition of the test pads inside a cell remains constant, the test probes can automatically be moved along the cells in the matrix. Furthermore, the separation between cells does not need to be constant [209].

- *Area Optimization*: Since the separation between cells could be arbitrary, the script can place them taking into account its size, avoiding large areas without printed designs and therefore maximizing the number of devices to place into the whole test area.

- *Unique device identification along the process*: The script generates a label for each PCell placed in the layout, and physically draws the label close to the cell to visually identify it. In addition, this label is stored next to the position of the cell in the TVD file described before.

- *Device parameter registration*: Along with each device identification and position, the script stores in the TVD file the design parameters names and values of each placed PCell. This allows a more accurate characterization and analysis protocols to correlate results and measurements with specific design parameters.

The Pcells developed in this work are coded in Python [210] scripting language due to its high readability and relative simplicity. They are adapted to be instantiated by the free layout editor Glade [211]. In this work, Pcell strategy has been used for two main purposes: (1) Technology Design Rules Characterization (DRC), (2) Active and passive device design.

4.1.2 PCell for design rules characterization

In the late 1970´s, the concept of design rules revolutionized integrated circuits design [212]. The initial idea was to abstract physics to a point where the design engineers address physical layout to develop devices and circuits with sufficient certainty without the need of a deep knowledge of process and materials.

Design rules are a set of geometric restrictions imposed to the different layers fabricated by the foundry that designers have to respect. These rules guarantee that layout representations match final printed patterns within an accepted tolerance and enable working circuits with an optimal balance of yield versus circuit integration density.

Regardless of the choice of technology, a common fabrication goal is to produce circuits with the required function and performance at a minimum cost. Cost, for a given process, depends directly on the area occupied by the circuit and the process yield. Therefore, decreasing the circuit area is one of the optimization goals for designers to get the maximum integration density. Furthermore, the maximum performance of the circuit is usually obtained using minimum possible dimensions (i.e. transistor channel length) of layers since this reduces the parasitic capacitance and increases the gain. Thus, knowing the boundary geometrical conditions in layout design helps the designers to improve the circuit performance.

In PE, the intrinsic characteristics of functional materials lead to different constraints on device technology. The electrical performance of printed devices and circuits can be improved by characterizing the conditions or parameters that lead to different printed morphologies. For example, in case of inkjet printing, there are some artifacts of printed features such as scalloping and/or bulging lines [213], which are due to discrete drop nature of inkjet printing and require balancing between drop size, drop space, and ink-substrate interaction [214], [215].

Furthermore, layer-to-layer interactions must be considered for multi-layer devices such as diode, capacitors, and OTFTs. Faults and failures appear due to the irregularity of the underling surfaces and solvents incompatibility between layers. For example, the well-known coffee-ring effect may lead to two types of errors for a two-layer structure: breaks in the top layer at the corners due to excessively high coffee-ring peaks in the bottom layer, breaks in the bottom layer for large surfaces since the structure is too thin in the middle of the ring [213].

The set of design rules for different printing technologies is similar but it needs to cope with the above-mentioned features of process and used materials.

When printing structures for electronics, two main geometrical criteria should be met. The first requirement is to ensure proper continuity and isolation in each single layer; for instance, the minimum width and spacing of a metal layer are defined in order to guarantee that there is no discontinuity in individual lines while there is enough space between two lines on the same layer to avoid short circuits. The second requirement is layer-to-layer registration, according to the topologies required to build working multi-layer devices such as OTFTs, diodes, etc. Most devices use a combination of stacking layers with device-specific rules and design parameters. The design rules for one metal layer on top of an isolation layer are usually different from the metal on top of another metal or organic semiconductor.

In this work, a scalable model for design rule extraction is proposed. It uses a generic format to be applicable to most of the fabrication processes (regardless of the number of layers). Every rule will be characterized by one parameter whose value depends on its specific fabrication features. Design rule values depend on the precision and resolution of the printer machinery, the alignment accuracy between layers, the material interaction and growth, and also on the decision concerning the acceptable yield of the process.

I am proposing a methodology (based on PCells) to extract design rules for any specific technology in four consecutive steps: (1) Formalization of a complete set of design rules to a set of drawing layers, (2) Automatic layout generation of matrices of the designed rules using PCells and scripts, (3) Fabrication of the generated test structures, and (4) Characterization of the fabricated structures to obtain the design rules.

1. Formalization of design rules to set of drawings

Geometrical design rules can be classified into three main categories.

- *Single-layer rules*: This group of rules refers to the minimum width of a line, minimum spacing of two lines in the same layer, and minimum notch and corner of a layer guaranteeing neither discontinuity nor short-circuit faults. Figure 4.1 shows the design parameters for this category.

  Width: The distance between inside facing edges of individual shapes

  Spacing: The distance between outside facing edges of shapes from same layer

  Notch: The distance between outside facing edges of the same shape

  Corner: The distance between the outside facing concave nexus of a shape and the outside edge of a second shape from the same layer.

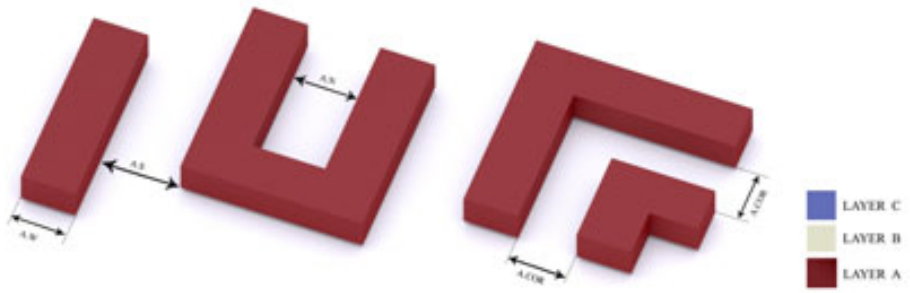


Fig. 4.1 Single-layer design rules

- *Two-layers rules*: These rules refer to the minimum width, spacing, extension, margin, and overlap of two layers adjacent or overlapping each other. These rules are dependent on both the printing accuracy of each layer and the inter-layer alignment quality. Figure 4.2 shows the possible cases of this category.

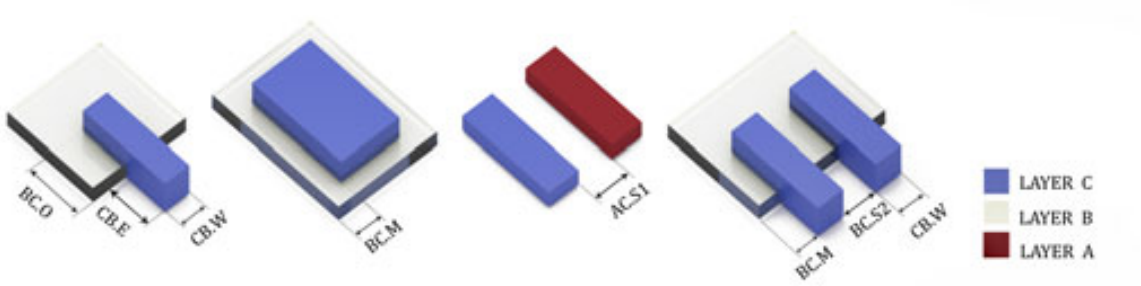


Fig. 4.2 Two-layers design rules

Width: The distance between inside facing edges of individual shapes located on top of the other layer.

Spacing: The distance between outside facing edges of shapes from different layers. It can also be considered as the distance between outside facing edges of shapes from the same layer on top of another layer.

Notch: The distance between outside facing edges of the same shape on top of a different layer.

Corner: The distance between the outside facing concave nexus of a shape and the outside edge of a second shape from a different layer. It can also be considered as the distance between the outside facing concave nexus of a shape and the outside edge of a second shape from the same layer on top of another layer.

Extension: The distance between the butting edges of a two overlapping layers to the inner facing edge of top layer.

Margin: The distance between inside facing edge of a layer to outside facing edges of another layer, when the shapes from two layers are overlapping.

Overlap: The distance between an inside facing edge of a layer to the inside facing edge on another layer, when the shapes from two layers are overlapping and one layer has extended edge(s).

- *Multi-layers rules*: Multi-layer rules are the ones specified for various layers building devices such as OTFTs, diodes and capacitors. Figure 4.3 shows the possible cases of this category. The rules´ definition is the same as two-layers ones, but in this case they are overlapped with one or more layer(s).

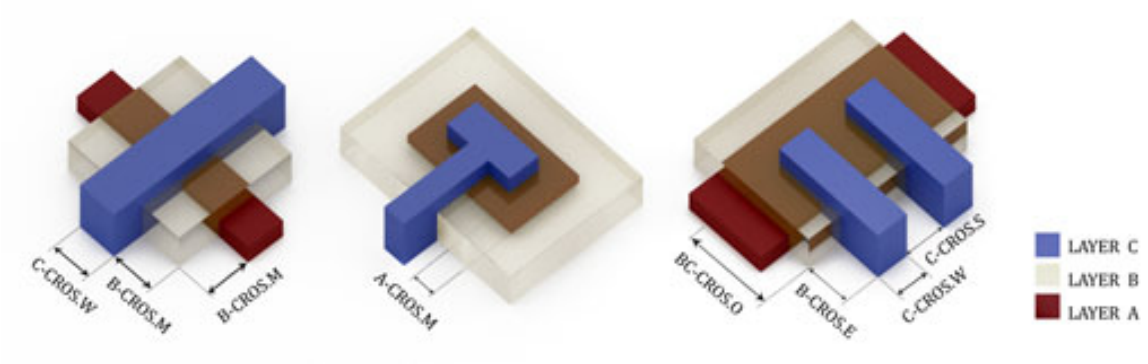


Fig. 4.3 Multi-layers design rules

Table 4.1 shows the list of formalized design rules related to several layers combination. In case of multi-layers, by increasing the number of layers, the combination of design rules for each layer increases but they still can be extracted from the below rules.

2. Automatic layout generation of test structures

In order to determine the design rule (minimum and tolerance) for each structure, once the printing process is fixed, a set of test structures are designed using the PCell approach. In order to obtain enough statistical data for accurate extraction of each design value, matrices of test vehicles with repetition of structures in a specified range has to be generated. By increasing the number of repetitions for each set of design parameters, the obtained design rule value will be more accurate.

The procedure to create the test matrices is done through python scripts. The script instantiates the PCells with corresponding design rule, and take it under analysis as the input parameters to sweep through a range depending on the printing technology

Table 4.1 Set of formalized design rules

Rule	Category	Description
X.W	Single-layer	Min. width of layer X
X.S	Single-layer	Min. spacing of layer X
X.N	Single-layer	Min. notch of layer X
X.COR	Single-layer	Min. corner of layer X
XY.S1	Two-layers	Min. spacing between layer X and Y
XY.S2	Two-layers	Min. spacing of layer X over/under Y
XY.W	Two-layers	Min. width of layer X over/under Y
XY.N	Two-layers	Min. notch of layer X over/under Y
XY.COR	Two-layers	Min. corner of layer X over/under Y
XY.M	Two-layers	Min. margin of layer X and Y
XY.O	Two-layers	Min. overlap of layer X and Y
XY.E	Two-layers	Min. extension of layer X out of Y
X-CROS.W	Multi-layers	Min. width of layer X in combination with other layers
X-CROS.S	Multi-layers	Min. spacing of layer X in combination with other layers
X-CROS.COR	Multi-layers	Min. corner of layer X in combination with other layers
XY-CROS.E	Multi-layers	Min. extension of layer X out of Y in combination with other layers
XY-CROS.O	Multi-layers	Min. overlap of layer X and Y in combination with other layers
XY-CROS.M	Multi-layers	Min. margin of layer X and Y in combination with other layers

and machinery resolution. Technology file is also called for the pcell execution. It is an external file provided by the technology and specifies the stack of layers, process and electrical parameters.

Figure 4.4 depicts the simplified concept of the PCells and scripts applied to generate a matrix of test vehicles to characterize their corresponding design rules.

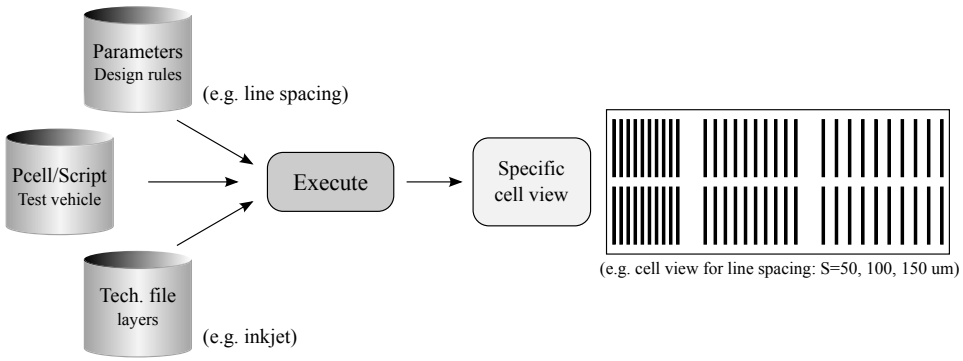


Fig. 4.4 Simplified concept of PCells for DRC test vehicle generation

A sample of the PCells coded in python for generation of the test vehicles related to line width and spacing is shown in Appendix B. The default values are (w=200um, s=100um), and they are scalable according to the target technology. Execution of this code will only generate 10 parallel lines with the default values as w and s. A portion

of the script coded in python for generation of 15 different instantiation of the previous pcell test vehicle is also shown in Appendix B. In this example, the range of the lines width is between 40um to 200um, in steps of 40um, and the spacing is varying between 80um to 240um in steps of 80um. "$Pitch - x$", and "$Pitch - y$" are the pitch of each instantiation in x and y axis.

After running the above-mentioned script, the physical layout as well as the TVD files is generated. The TVD file, where X and Y positions, device label and parameters are separated by comma is shown in Appendix B. Figure 4.5 depicts the generated layout. In this work, all of the test vehicle matrices were generated in the freeware IC layout editor from Peardrop Design Systems, called GLADE [211].

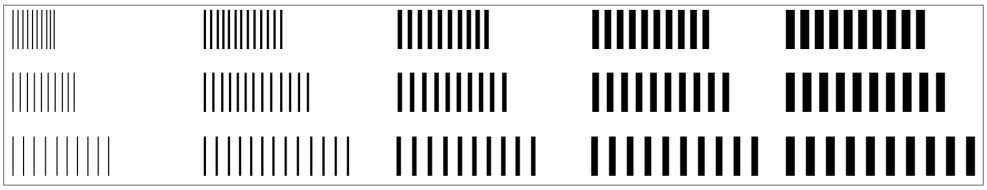


Fig. 4.5 Layout of the width and spacing test vehicle matrix

3. Fabrication of the test structures

The aforementioned test vehicle matrixes could be fabricated in any printed technology by changing the design parameters according to the technology restrictions. As a proof of concept, same methodology was adapted to characterize a set of geometrical design rules for inkjet printing technology. The layouts of the design rules that are necessary for printing active and passive devices in this technology were designed and are shown in Appendix A. The technology consists of two metal layers (MET1, MET2), a resistive layer (RESIST), a dielectric layer (DIE), and an organic semiconductor layer (OSC). The S2S process based on laboratory printing platforms (Dimatix-DMP2831)[216] at Technical University of Chemnitz (TUC)[217] was used for printing the test vehicle matrices.

Figure 4.6 shows the printed test vehicle matrix for MET1 width, spacing, and corner rules.

4. Characterization of the test structures

Characterization of enormous number of DRC test vehicles is a tedious work due to the large quantity of designed and fabricated structures. Thus, an automatic characterization environment, shown in Figure 4.7 (Source [209]), has been implemented

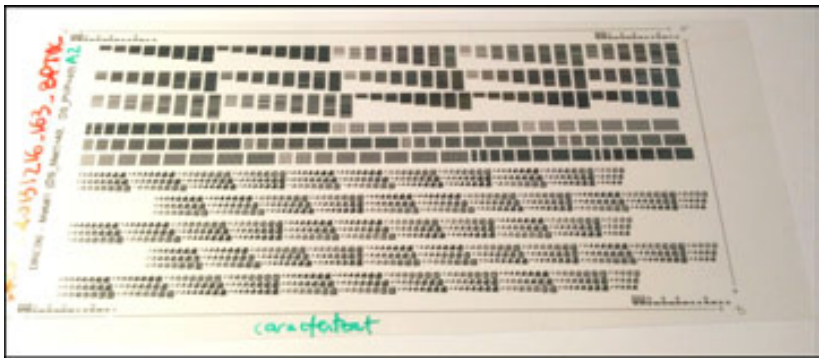


Fig. 4.6 Test vehicle matrices for MET1 width, spacing and corner rules, inkjet printed at TUC

in order to address the characterization of the large amount of data coming from fabricated test structures. The system uses a semi-automatic Cascade Microtech Summit Series probe station [218] in combination with all the suitable measurement instruments for the test.

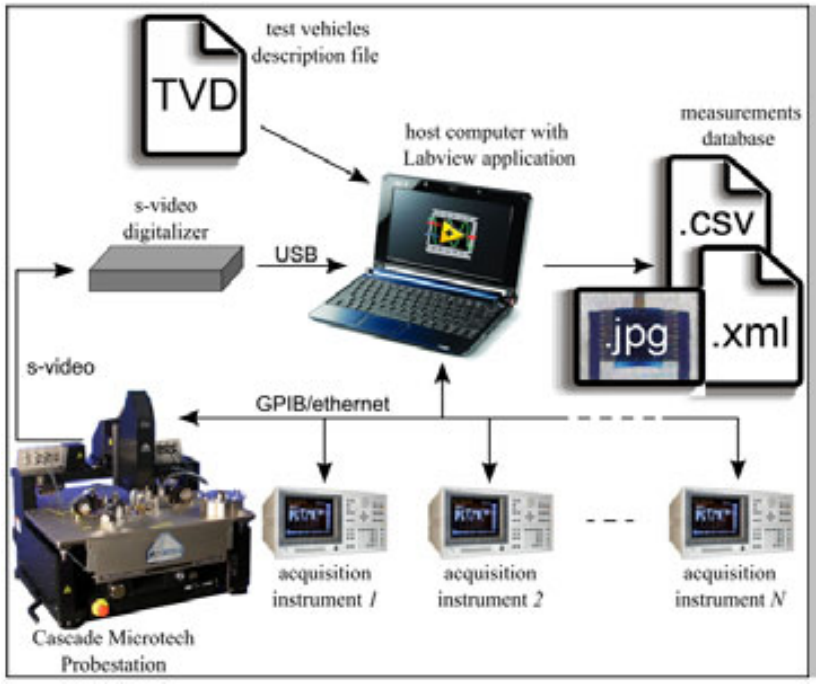


Fig. 4.7 Automatic characterization environment

Labview software is used to control all the associated equipment, and the computer running the Labview application acts as host and is in charge of configuration settings, actions control, status checks, and data exchange with the semi-automatic probe station and the associated instruments. The communication between all the actors can be

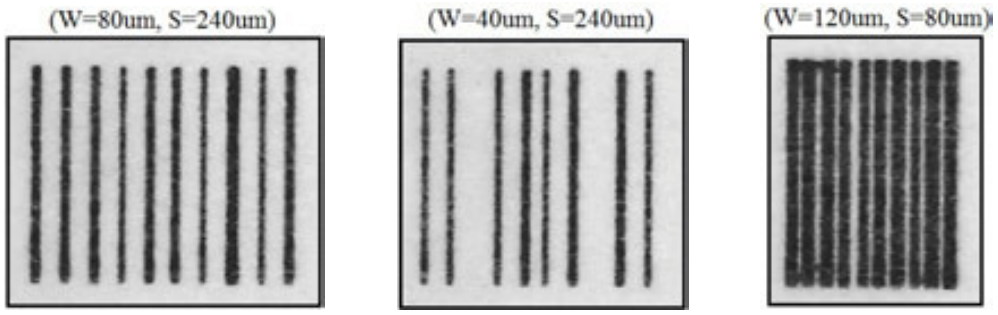
established through GPIB, Ethernet bus, USB, and other commonly used standards transparent to the user.

TVD file generated (See Section 4.1.1) in design cycle is used as an input for the semi-automatic probe station to record the essential information of each structure, to manage the move between structures and to track data.

The printed structures can be characterized either by using powerful optical-based (image-based) metrology techniques [215], [219] or fast and automated electrical characterization techniques [209], [220]. When testing a DRC structure electrically, the goal is to check the continuity/isolation of printed lines. So the **Pass/Fail** strategy is used in this case [209]. This is usually used for obtaining the minimum width and spacing of conductive layers.

There are cases where it is not possible to apply electrical characterization to extract the design rules, because the layers under study are not conductive. If so, it is necessary to analyze the test structures through an optical characterization. However, this method can also be applied to conductive layers. For optical characterization of test vehicles, the proposed system in Figure 4.7 uses a microscope with a video acquisition device connected to the PC. This allows the Labview application to capture images of each individual test vehicle. The probe-station ensures a high-precision positioning (less than 1um error), enabling an accurate optical characterization of DRC structures.

Later in post-processing step, the validity of the assigned design parameters for any specific test vehicle will be checked by image processing. This can also help the technologist to further analyze the origin of the failure. Figure 4.8 shows the optical analysis of the printed test vehicles related to width and spacing of a metal layer. It can be seen that the designed width and spacing in case (b) and (c) respectively are below the limitation and the structure is not printed properly.



(a) Accepted W and S (b) Failing width (c) Failing spacing

Fig. 4.8 Optical characterization of printed test vehicles for width and spacing rules

By optical characterization of the printed arrays of test vehicles and compiling the extracted data, the minimum design rules can be obtained by using the extracted statistical results. As an example, Table 4.2 presents the statistical analysis of minimum width for a metal layer, extracted from 10584 printed test vehicles. It collects the percentage of well printed lines with acceptable **continuity** and without any interruption. The X and Y axises represent the line width and separation sweeping range. It is immediate to see that for width of 200um, the effectiveness is 100%, while there is a higher chance of having failing printed line with 40um width.

Table 4.2 Percentage of printing continuous line for different line widths and separations

	W=40um	W=60um	W=80um	W=100um	W=120um	W=140um	W=160um	W=180um	W=200um
S=40um	82.24	92.23	98.54	99.21	99.80	100.00	100.00	100.00	100.00
S=60um	88.73	91.58	97.06	98.54	99.92	99.57	100.00	100.00	100.00
S=80um	86.04	95.64	97.21	99.25	100.00	100.00	100.00	100.00	100.00
S=100um	81.23	92.29	99.24	99.81	100.00	100.00	99.91	100.00	100.00
S=120um	93.78	88.36	98.38	98.89	100.00	100.00	100.00	100.00	100.00
S=140um	90.19	91.33	96.55	99.51	99.02	99.94	100.00	100.00	100.00
S=160um	87.88	89.58	96.84	98.91	100.00	99.00	100.00	100.00	100.00
S=180um	87.17	93.64	97.17	99.25	100.00	100.00	100.00	100.00	100.00
S=200um	90.01	91.28	98.19	100.00	100.00	100.00	100.00	100.00	100.00
S=220um	92.64	94.20	95.89	99.68	100.00	100.00	100.00	99.99	100.00
S=240um	85.09	93.69	96.40	99.44	100.00	100.00	100.00	100.00	100.00

A similar table is generated for the study of the design rule for minimum metal line separation depicted in Table 4.3. The results suggest that for this specific printing technology, it is not possible to print two parallel metal lines with no contact between them, when the separation is only 40um. In return, with the separation value higher than 120um, the percentage rises above 90%, and for S=240um, the line **isolation** is guaranteed to 100%.

4.1.3 PCell for device design

According to the natural technology evolution, the first libraries to be developed are the ones containing the basic passive and active devices. Table 4.4 shows the elements of the basic passive and active devices library, to be developed as pcells. The second column contains the design parameters of each cell, which will drive the specific cell-view generation. Specifying the value of each design parameter defines the geometric shape of the cell view.

Some parameters are mutually exclusive, like the length/resistance on the resistor or the area/capacitance on the capacitor. It means that the circuit designer can choose

Table 4.3 Percentage of printing properly unconnected parallel metal lines for different line widths and separations

	W=40um	W=60um	W=80um	W=100um	W=120um	W=140um	W=160um	W=180um	W=200um
S=40um	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
S=60um	5.84	3.02	8.98	11.25	8.96	21.59	25.93	34.00	38.09
S=80um	22.29	28.47	33.91	35.26	41.18	50.24	55.72	58.46	68.52
S=100um	59.04	67.52	71.43	82.14	86.09	89.11	92.10	94.58	97.24
S=120um	91.27	94.55	94.81	95.45	97.56	94.88	95.72	98.12	98.99
S=140um	95.14	95.22	96.18	95.82	96.81	97.28	98.11	98.96	99.17
S=160um	99.15	99.84	99.00	100.00	99.97	99.66	100.00	100.00	100.00
S=180um	100.00	100.00	99.99	99.07	100.00	100.00	100.00	99.01	100.00
S=200um	99.60	100.00	100.00	99.08	100.00	99.58	99.09	100.00	99.63
S=220um	99.77	99.21	100.00	100.00	100.00	100.00	99.99	100.00	100.00
S=240um	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00	100.00

to modify one parameter of each pair, and the other one will be automatically modified according to the specified values. As an example, if a designer fixes the Width and capacitance of a capacitor, the plate Length will be automatically calculated through the previous parameters values and the capacitance per unit area. In this example, the capacitance per unit area is a technology parameter acquired from the TDK technology files, and cannot be modified by the circuit designer.

Table 4.4 Basic passive and active devices library elements

Cell	Design parameter	Parameter description
Linear Resistor	W, L, R	strip width, strip length, resistance
Snake Resistor	W, L, R, Z	strip width, vertical bar length, resistance, z-meanders number
Capacitor	W, L, C	upper plate width, upper plate length, capacitance
Square Inductor	W, S, R, N	turn width, turn spacing, interior turn radius, number of turns
Diode	W, L	upper contact width, upper contact length
PMOS transistor	W, L, NF	channel width, channel length, number of fingers

The pcell structure is as follows. After writing the pcell information and importing both the libraries and geometrical design rules, the user design parameters are checked in order to guarantee a DRC-clean cell. Then, the electrical parameters of the devices are calculated and presented. Following that, the layout is generated according to the x and y defined bounds, as well as design parameters.

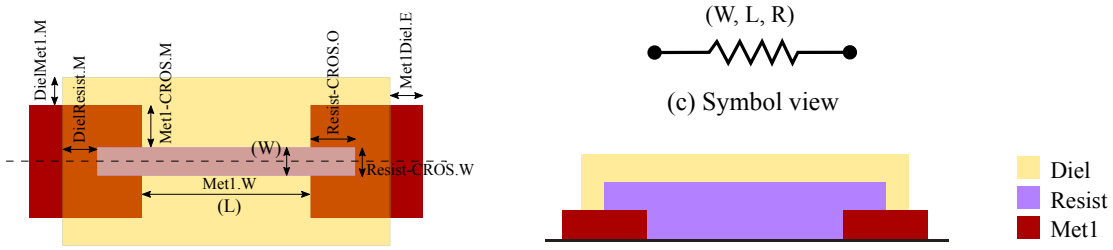
All of these passive and active devices were inkjet printed on a (S2S) process based on a combination of industrial printing platform (Dimatix-DMP3000) [221] and laboratory printing platforms (Dimatix-DMP2831) [216] and using organic materials. Later, they were characterized and optimized in respect to their electrical behavior,

and the analysis is shown in [119]. So, the fabrication process and characterization results are not shown here in this work.

Linear resistor

Resistor is one of the most elementary passive devices in a cell library and is usually used as a component in analog circuit. It consists of a bar of a resistive material that provides a voltage across its terminals by resisting the flow of charge through itself. It contains a strip of homogeneous material with two conducting pads at their ends.

Organic conductive materials can be used as resistive materials due to its low conductivity compared with inorganic metallic materials. Conductive polymer (PEDOT:PSS), which is a mixture of two polymers, was used as the resistive material with conductivity in range of 3 10^3 and 9 10^3 S/m. As shown in Figure 4.9, first a layer of silver nanoparticle ink is deposited as the contact pads. Following that, PEDOT:PSS as the resistor layer and an insulator layer to protect the polymer of moisture were deposited on top.



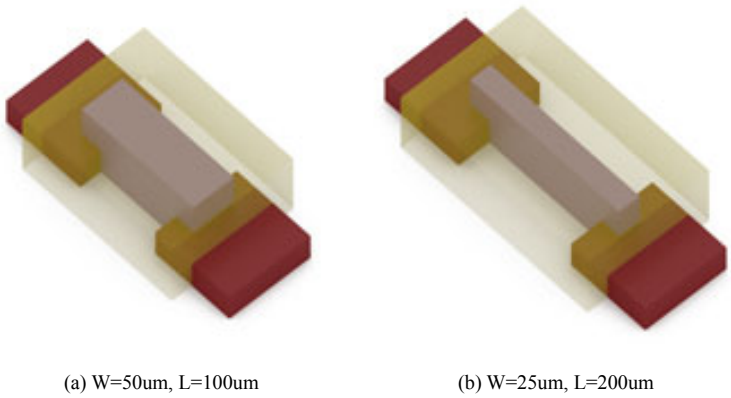
(a) Top-view layout (b) Cross section view

Fig. 4.9 Linear resistor layout information

The resistance value depends on the width (W) and length (L) of the resistive rectangle layer, and its sheet resistance, where W and L are design parameters of the pcell. As an example, the pseudo pcell code for this device is shown in Appendix B. Figure 4.10 depicts two different instantiations of the corresponding pcell with different dimensions.

Snake resistor

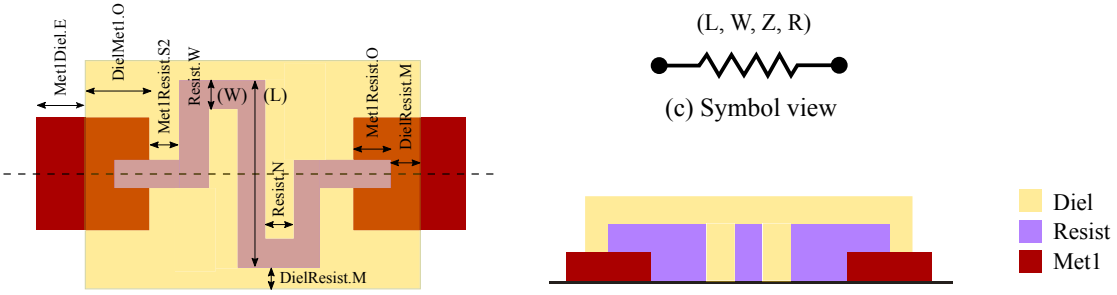
Snake resistor, also known as meander resistor or serpentine resistor, is made off two or more number of meanders forming a snake shape. The resistance value is depending on the width (W) and length (L) of the bars, and number of meanders (Z), as well as the sheet resistance of the resistive material, where W, L, and Z are design parameters



(a) W=50um, L=100um (b) W=25um, L=200um

Fig. 4.10 Two instantiations of linear resistor pcell

of the pcell. Figure 4.11 shows the top-view layout with design rules (a) and cross section (b) of the snake resistor.



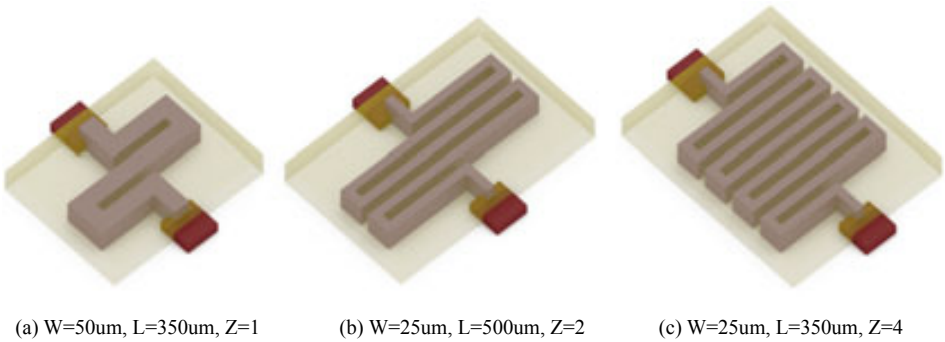
(a) Top-view layout (b) Cross section view

Fig. 4.11 Snake resistor layout information

Figure 4.12 depicts two different instantiations of the corresponding pcell with different dimensions.

Capacitor

Capacitor provides impedance to current inversely proportional to the frequency of an applied voltage. Capacitance is a measure of the ability of a device to store energy in the form of separated charge or in the form of an electric field. They are used for blocking direct-current and alternating-current devices, for bypassing unwanted alternating-current components to ground, and as frequency-determining devices in resonant circuits. When a capacitor encounters rapid increase in voltage, its impedance reduces greatly. This property is very useful for protecting more important devices in the

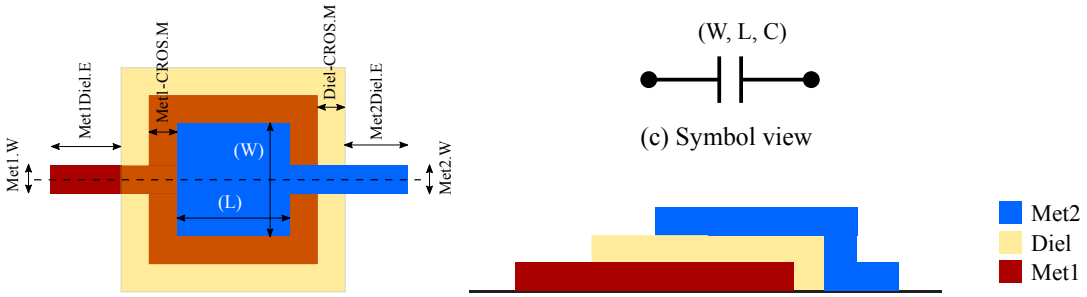


(a) W=50um, L=350um, Z=1 (b) W=25um, L=500um, Z=2 (c) W=25um, L=350um, Z=4

Fig. 4.12 Two instantiations of snake resistor pcell

circuits. Capacitors are often connected in parallel with those important components, and if an unexpected voltage surge should occur, capacitor will short and draw most of the current, thus protecting the other component [222].

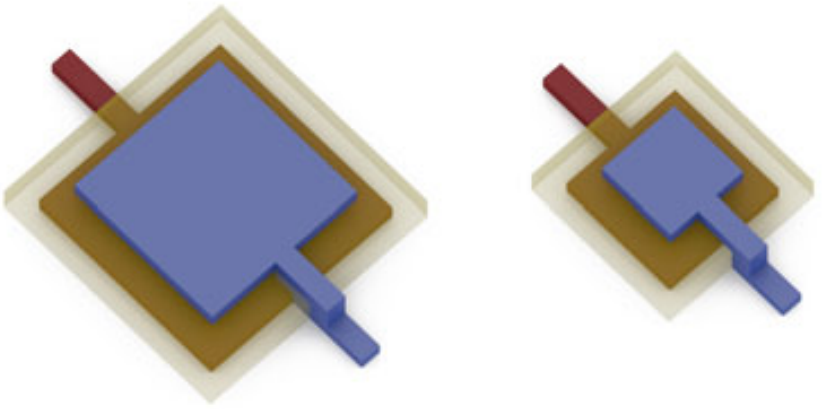
In its simplest form, it consists of an insulator or dielectric material sandwiched between two parallel conducting metallic plates and one of the most common types of monolithic capacitors is Metal-Insulator-Metal (MIM). The capacitance value is a function of width (W) and length (L) of the overlapping conductor´s rectangle, the relative dielectric constant and the thickness of the dielectric or oxide, as well as the permittivity of free space. W, L are the design parameters for the pcell and the rest are technology and construction parameters. Figure 4.13 shows the top-view layout with design rules (a) and cross section (b) of the capacitor.



(a) Top-view layout (b) Cross section view

Fig. 4.13 Capacitor layout information

Figure 4.14 depicts two different instantiations of the corresponding pcell with different dimensions.



(a) W=200um, L=200um (b) W=50um, L=50um

Fig. 4.14 Two instantiations of capacitor pcell

Square inductor

Inductance is the constant of proportionality which relates the voltage to the rate of change in the current. A small amount of voltage is needed to maintain a steady current through an inductor. However, in order to change the current flow rapidly, a large voltage is required, thus, inductors resist current surges. Similar to the idea of connecting capacitor in parallel to important component, inductors often connect in series to those devices, in order to protect the device from unexpected current surge. Inductors store the energy in the form of moving charges or magnetic fields. Inductors are also used for eliminating unwanted frequencies. They attenuate or reduce high frequencies while allowing low frequencies to pass with little attenuation.

Square inductor is a type of inductor which is made of a squared patterned turns of conductor layer with extended tails or termination at both ends. Its inductance value depends on the spacing turn (S), interior turn radius (R), width (W) of conductor turns, and number of turns (T), as well as some construction parameters. S, R, W, and N are the design parameters for the square inductor pcell. Figure 4.15 shows the top-view layout with design rules (a) and cross section (b) of the square inductor.

Figure 4.16 depicts two different instantiations of the corresponding pcell with different dimensions.

Diode

Diode is one of the simplest semiconductor devices, which is voltage-controlling device, and allows current to pass in one direction with a low applied voltage. In the other

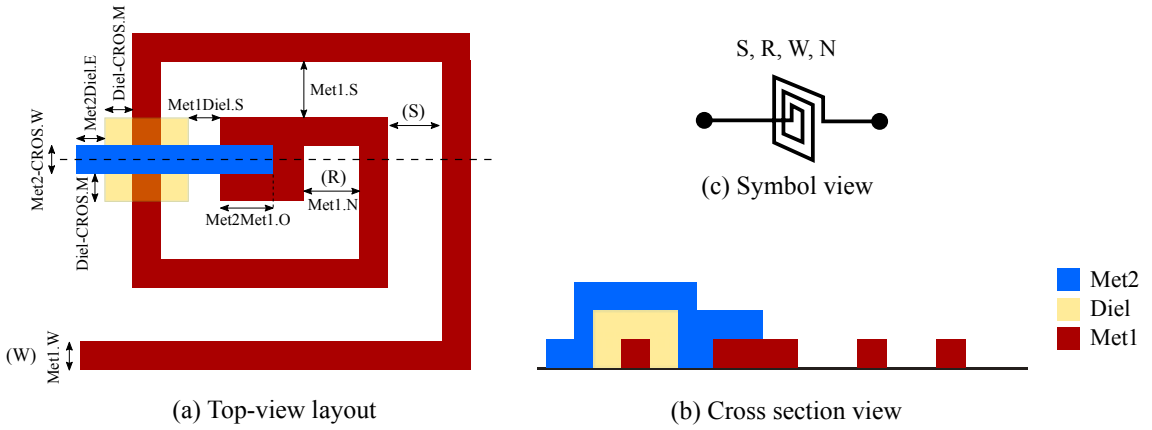


Fig. 4.15 Square inductor layout information

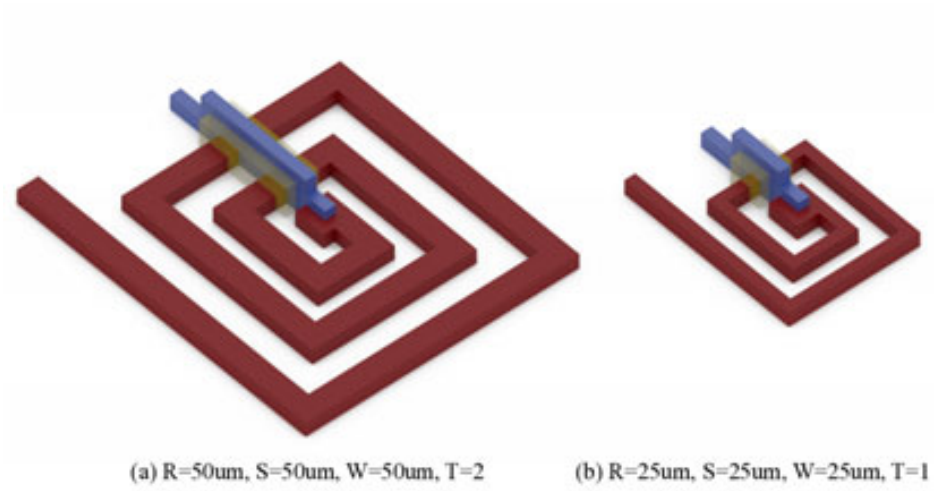


Fig. 4.16 Two instantiations of square inductor pcell

direction, a much higher voltage (reverse bias) is required for current to flow. One of the most common type of diodes is OLED, which are useful for flexible displays, and lighting. Diodes are made of two conductor plated acting as cathode and anode, and semiconductor, resistance, and dielectric at the middle. Design parameters for diode pcells are the width (W) and length (L) of the upper metallic layer. Figure 4.17 shows the top-view layout with design rules (a) and cross section (b) of the diode.

Figure 4.18 depicts two different instantiations of the corresponding pcell with different dimensions.

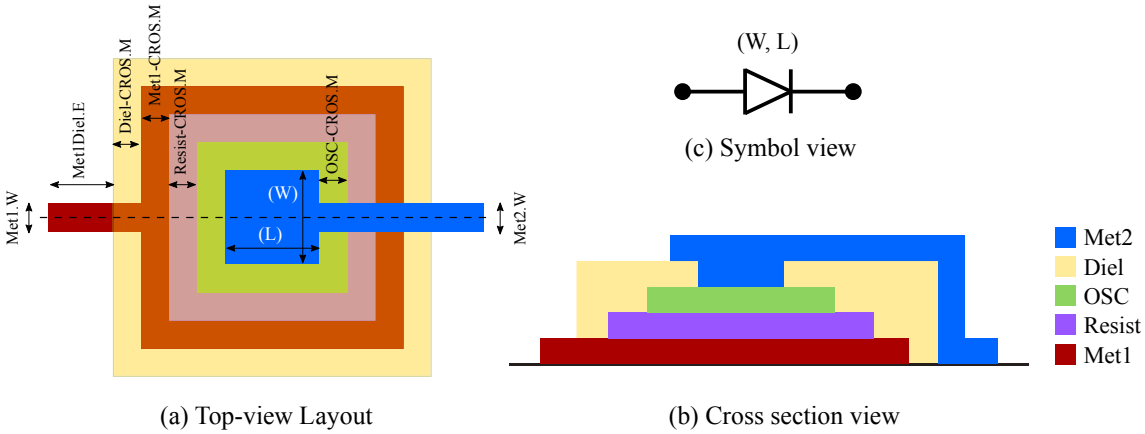


Fig. 4.17 Diode layout information

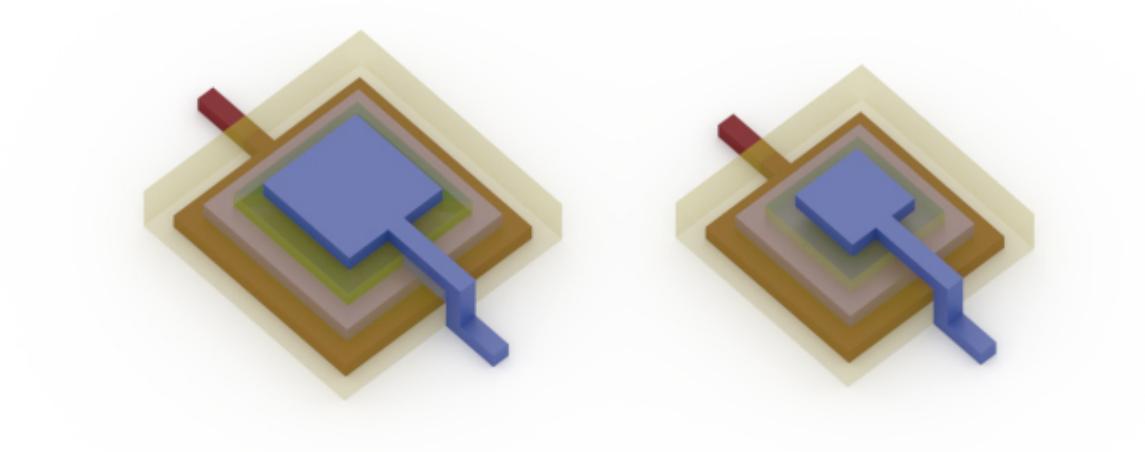


Fig. 4.18 Two instantiations of diode pcell

P-type OTFT

The concept of OTFTs and its materials, technology process, and stack of layers were explained in Chapter 3. In this section, coplanar bottom-gate OTFT layout is generated as an example for pcell approach. Channel width (W), number of fingers (nf), and channel length (L) are the design parameters for OTFT pcell. Figure 4.19 shows the top-view layout with design rules (a) and cross section (b) of the PMOS OTFT.

Figure 4.20 depicts three different instantiations of the corresponding pcell with different dimensions.

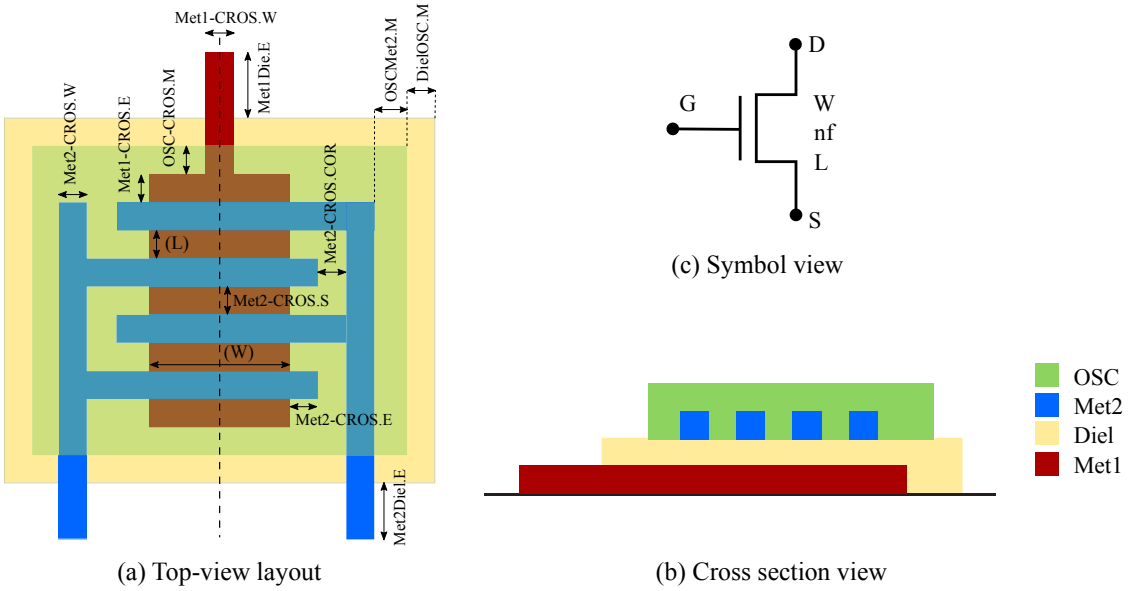
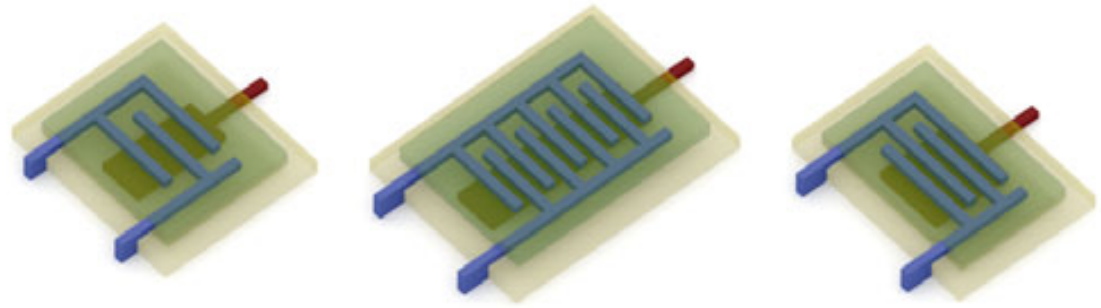


Fig. 4.19 Organic thin film transistor layout information

4.2 Improvement of OTFTs: design optimization

Process yield, variability and scalability are some of the critical issues for scaling-up integrated circuits in PE. The organic materials and fabrication process as well as physical layout design play a significant role in controlling the performance of OTFTs. In order to achieve the performance required by the applications, the basic devices such as OTFTs have to be designed to be electrically reliable and stable.

Some electrical features of the devices such as I_{on}, I_{off}, transcondunctance, gate and parasitic capacitance are partially controllable by changing the physical layout design. Furthermore, in digital logic gates, some static and dynamic principles like DC gain,



(a) W=60um, L=69um, nf=2 (b) W=50um, L=23um, nf=8 (c) W=100um, L=23um, nf=3

Fig. 4.20 Two instantiations of OTFT pcell

noise margins, power dissipation, propagation delays, and operating frequency could be analyzed and optimized in layout design stage, leading to the desired performance with the highest possible reliability facing complex circuits and systems.

However, there are trade-offs between performance and stability of devices that appear when changing design styles and parameters such as transistor dimensions, layers overlapping areas, and aspect ratio. Thus, in large scale circuits, providing an optimal layout design is very important to manage process variations coming from materials and fabrication processes, existing between run-to-run and substrate-to-substrate.

In this section, three layout styles are proposed for the Top-Gate Bottom-Contact OTFTs fabricated through a photolithography process. Their impact on electrical behavior has been investigated and discussed through characterization analysis [223].

In order to obtain accurate and reliable results and comparison, several hundreds of devices with different dimensions from each topology were designed through the automated layout generation by using pcell scripts. Glade free IC layout editor tool has been used for pcell instantiation, running script, and generating the layouts. Due to restrictions of Glade tool for drawing circular shape layouts, MaskEngineer software, developed by Phoenix [224], was used for designing the layout of circular shape transistors. MaskEngineer provides the object-oriented design environment for mask layout. In contrast to glade, drawing of any shape and connection is realized through mathematical functions and expressions by programing, which allows reduced design time.

For large scale characterization of the transistors, the similar approach as mentioned in Section 4.1.2 was adapted. Characterization of OTFTs was performed using Keithley parameter analyzer in conjunction with a semi-automated probe-station allowing reliable statistical analysis and uniformity measurement to be performed over the substrate area.

In order to compare the behavior of the transistors with different topologies, they were characterized and analyzed in respect to their performance parameters (i.e. I_{on}, I_{off}, V_{th}, V_{on}, Mobility, and parasitic capacitance) extracted from their current-voltage (I-V), mobility-voltage (u-V), and capacitance-voltage (C-V) curves. Finally, yield and parameter variation will be analyzed and compared between design styles. Some other detailed characterization and measurements (life time, stability, degradation, and etc.) were performed, but are not mentioned here, because they are out of the scope of this thesis. Also, some measurement such as temperature-dependency has not been performed yet and are planned for feature works.

4.2.1 Fabrication technology

The transistors were fabricated using mask-based photolithography and dry-etching technology at Centre for Process Innovation (CPI) [225] in collaboration with NeuDrive Limited [226]. This is a high yield, high performance technology, in which OTFTs are fabricated through a 5 mask patterning process with channel length of 4um. FlexOS^{TM} ink platform, which is a combination of small molecule and semiconducting polymer with good uniformity, is used as OSC for OTFTs [226]. It has charge mobility levels of >4cm^2/Vs (in short channel transistors: <10um). The OTFT process flow diagram is shown in Figure 4.21 and explained below.

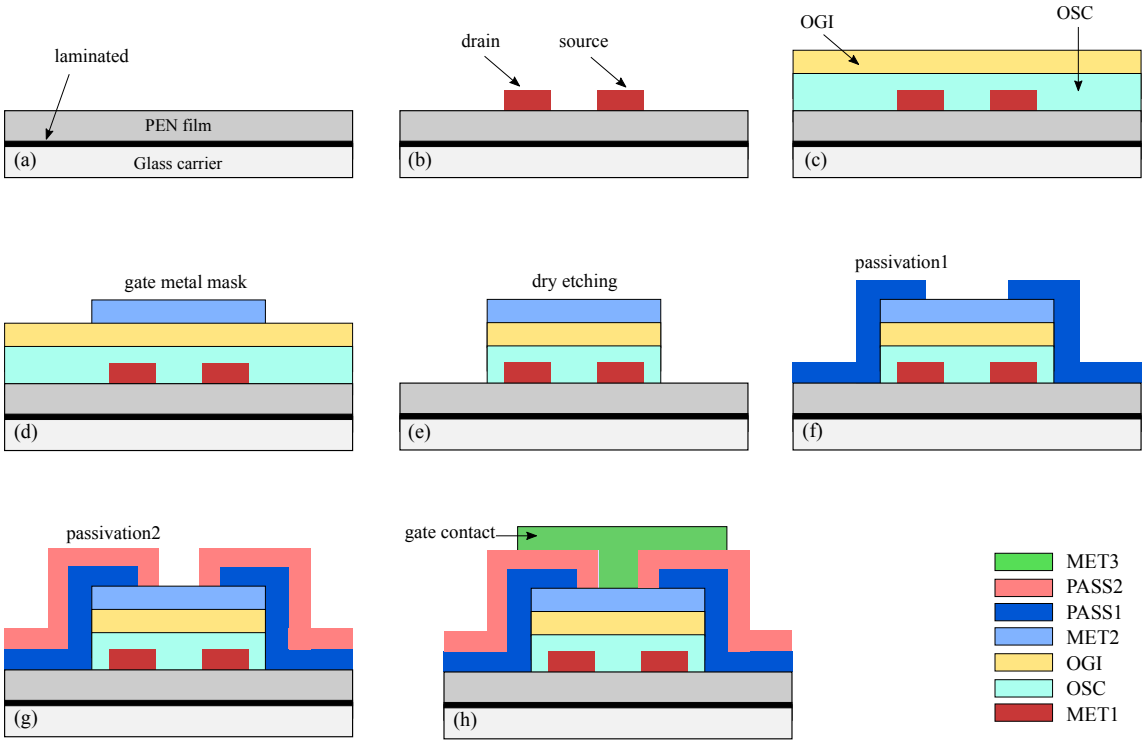


Fig. 4.21 5-mask photolithography process flow diagram for NeuDrive-CPI technology

First, photolithography was used to define geometries of gold (Au) electrodes (source/drain) with 50nm thickness evaporated onto SU8-planarized Corning Eagle glass substrate. The electrodes were plasma cleaned and functionalized with a pentafluorobenzenethiol (PFBT) self-assembled monolayer (SAM). A 20nm thick film of semiconducting ink was immediately deposited over the substrate by spin coating at 1750 rpm. Then, a 300nm thick film of Cytop (Asahi Glass Chemicals, Japan) giving a capacitance per unit area of 6.2 nf.cm^{-2}, was spin coated to act as the Organic Gate Insulator (OGI). The 2nd metal electrode was then evaporated and photo-patterned.

This electrode serves as an etch mask for the O_2 plasma removal of excess areas of OSC and dielectric from the substrates in order to reduce parasitic effects in the final devices. Following this, two passivation layers were coated and patterned photolithographyically to implement vias between 1^{st} metal (source/drain), 2^{nd} metal and the gate contact, which is patterned using the 5^{th} mask [227].

4.2.2 Layout design styles

Interdigitated OTFT

Interdigitated structure was first proposed by M. B. Das *et al* in 1971 for high frequency insulated gate field effect transistors [228]. In this structure, the source and drain electrodes are defined such that each is in the form of a comb, the fingers of the source comb being interdigitated with the fingers of the drain comb and the current carrying channel being located at the surface region parts between adjacent interdigitated source and drain fingers. The initial idea behind this technique is to provide a large current flow by increasing the channel width.

Due to the fact that low mobility and thus low current capacity is a key issue in development of organic transistors, we have employed the same topology for designing the top-gate bottom-contact OTFTs in PE. However, confusions in the design of such a transistor arise with respect to the geometry of the electrodes and definition of the active area. For that, I propose two topologies with different definitions of active area.

1. **Fully Overlapped Interdigitated OTFT**

   In Fully-Overlapped (FO) interdigitated topology, gate layer totally overlies (with some few micrometer margin) the source and drain electrodes, fingers and the intermediate surface channel region. Figure 4.22 depicts the top-view layout and cross section of this OTFT. The main advantage of this layout style is providing the most efficient version concerning the ratio between the transistor width (related to circuit speed) and transistor surface (related to circuit area). The finger width and channel length are shown in the figure and the channel width is $(N \times W_{\mathrm{f}})$, where N is the number of fingers, and W_{f} is finger width.

   However, such a form is not entirely satisfactory, due to the gate electrode lying over fingers and source/drain electrodes, the overlap capacitance is high and cause undesired parasitic, lowering the circuit performance. Moreover, the real channel size is not easily extractable since there is an extra non-linear channel

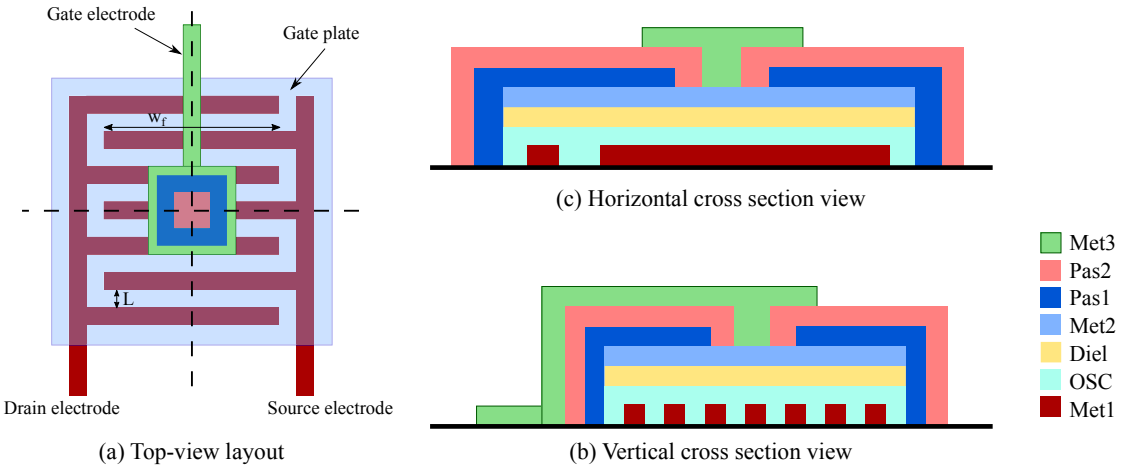


Fig. 4.22 FO style layout information

width on the corner of finger and also the channel length changes according to the corner separation of fingers and electrodes.

2. **Partially Overlapped Interdigitated OTFT**

   In order to overcome the bottlenecks of FO structure, I proposed Partially-Overlapped (PO) interdigitated topology, in which the gate electrode partially overlies the fingers and the surface channel region, but is separated from source/drain electrodes. Figure 4.23 depicts the top-view layout and cross section of this style. Thus, the key point here is that the gate to source/drain overlap is minimized comparing to FO version, and also the real channel width and length fit quite well to the assigned ones, and are fixed through entire channel region. This allows more accurate parameter extraction and can guarantee more predictable behavior in higher scales. Obviously, the total channel width for PO devices is less than that of FO ones for the same occupied space.

C-shaped OTFT

In the interdigitated devices, the gate-source parasitic capacitance (C_{gs}) is usually similar to the gate-drain one (C_{gd}) in off regime, since the overlapping area and the dielectric insulator is similar in both cases. For short length devices, the intrinsic capacitance is not far larger than parasitic one due to the fact that channel length is not much larger than overlapping length.

Sometimes, it is desired to reduce the gate/drain parasitic capacitance of the device, which can be realized by an unsymmetrical design style. For this case, OTFTs with

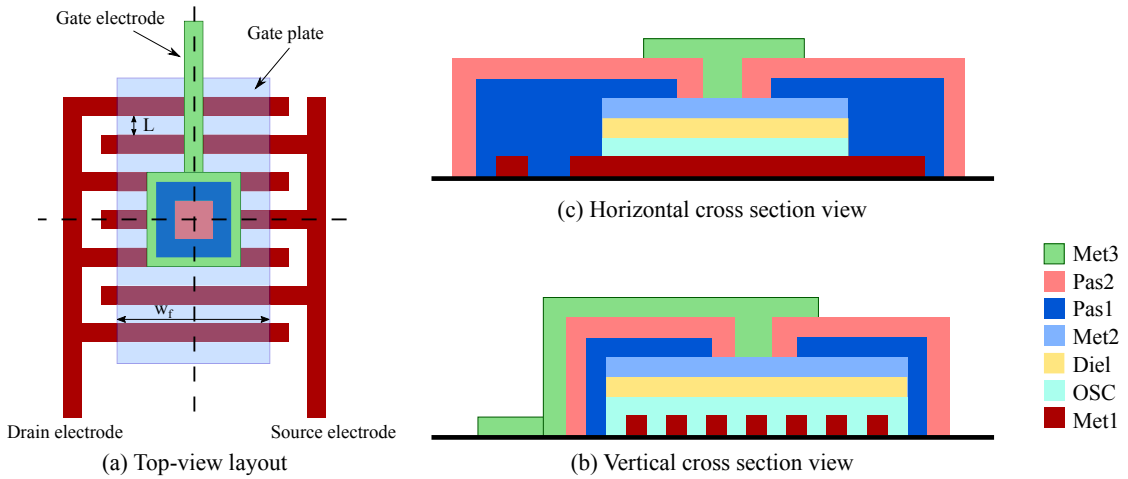


Fig. 4.23 PO style layout information

two fingers, where the gate overlapping area on drain side is less than (almost half) source side, is designed. We called them C-shape or U-shape (depending on fingers orientation), due to the fact that two fingers form a "C" shape as shown in Figure 4.24. This style could also be FO and PO, but for having a minimized gate-drain capacitance, PO C-shaped devices is recommended.

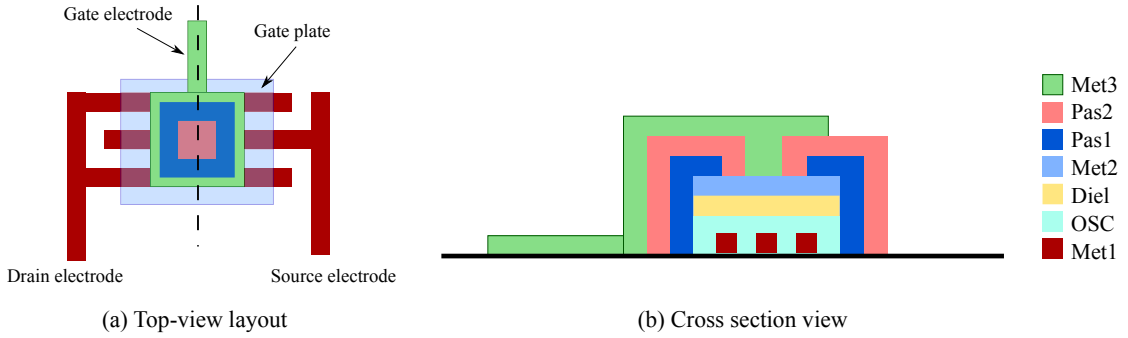
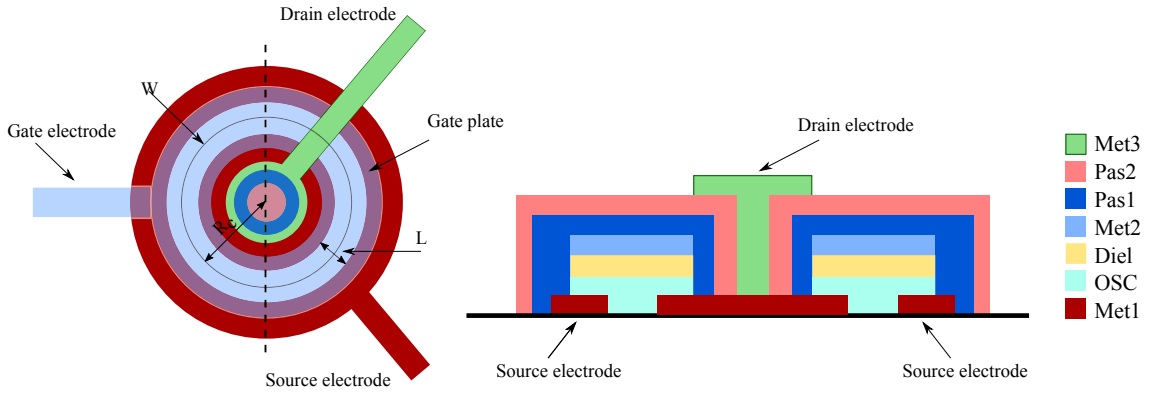


Fig. 4.24 C-shaped style layout information

C-shaped topology is basically designed for small OTFTs and cells with low drive strength. Due to the lack of interdigitating feature, for having a large channel width, the source/drain fingers should be extremely long to compensate. Thus, it occupies too much area in the substrate and makes the OTFT unsymmetrical (long but narrow). This is sometimes good for 2D arrays of OLED pixels.

Corbino OTFT

Linear devices may sometimes perfectly align with the highest mobility orientation of organic semiconductor crystal and they might align with the lowest mobility orientation of the crystal in another area of substrate. For this reason another type of OTFTs is proposed with circular shape, where it samples all orientations of the crystal at the same time. This OTFT design style is called Corbino, shown in Figure 4.25. Similar to C-shaped devices, corbino transistors provide less gate-drain overlaying area, which generates less parasitic gate/drain capacitance.



(a) Top-view layout (b) Cross section view

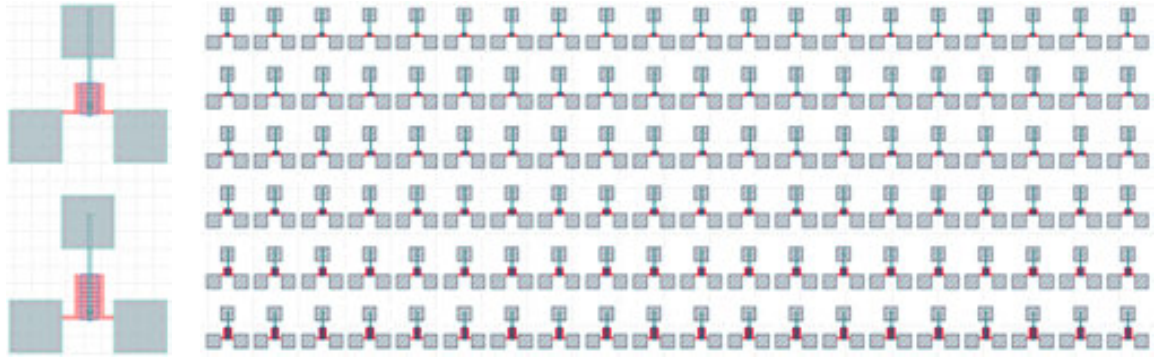
Fig. 4.25 Corbino style layout information

In this structure, the channel length is defined as the space between outer edge of the drain circle and the inner edge of source circle. The channel width is the perimeter of the circular channel region and is calculated as: $W = 2R_c$, where R_c is the radius of the circular channel region. For the same reason as U-shape design style, corbinos are mostly used for small/medium devices, except for too small devices (W<200µm), where drain circle is not big enough for via opening.

4.2.3 Automated layout generation, Fabrication

Automated generation of array of transistors with different dimensions (i.e. channel length, width, and number of fingers) was realized by using the pcell codes and scripts in python language. The pseudo code for the generation of partially-overlapped devices is demonstrated in Appendix B. In the first instantiation of this code the generated transistor will have ($W = 100\ m\ L = 4\ m\ nf = 4\ m$). By using script similar to Listing B.2 (shown also in Appendix B), an array of this device with different dimensions can be generated.

Figure 4.26 (a) depicts two sample cell views of PO interdigitated OTFT with different channel width and number of fingers, and Figure 4.26 (b) is an array of 6×20 OTFTs (120) generated automatically and distributed regularly with a large range for W and nf parameters sweep. Pads of $150 \times 150 \mu m^2$ have been also designed for each transistor for its test by $50 \mu m$ radius Beryllium Copper tips.



(a) Two instantiations

(b) Regular array of PO Interdigitated OTFTs with channel width and funmber of finger sweep

Fig. 4.26 Generated layout of a regular array of PO interdigitated transistors

Large amount of OTFTs with different design styles have been fabricated through several fabrication runs. First three runs, which date back to 2013-2014 have been fabricated in clean room 1 facilities with maximum substrate size of 4 inch. Later in 2015, the fabrications were improved to 700 m^2 100 (ISO 5) clean room with robot handling, and cassette to cassette transfer facilities, with substrates greater than 8 inch in size. This enables test and develop applications at 8 inch, 12 inch, GEN2 and roll to roll sizes.

The above-mentioned technology improvement has yielded higher process yield and better layer-to-layer alignment. This has enabled higher degree of density with smaller geometrical design rules, which has to shorter channel length for transistors ($4 \mu m$), while in the first three runs the minimum feature size was $6 \mu m$. Shorter channel length and better alignment, consequently has slightly improved the performance of the transistors.

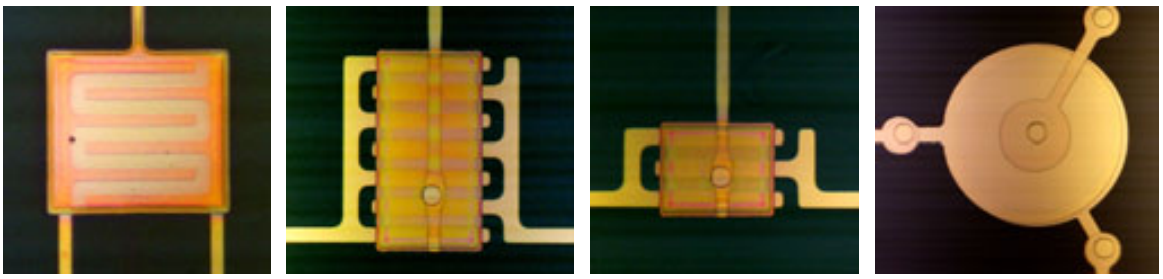
OTFT arrays and some logic blocks were designed and fabricated through those runs with different performance and features, which makes the performance comparison difficult. Thus, I chose two criteria for selection of reference array for each type: (1) All being fabricated at the same fabrication run and plate, (2) Choosing the array with the best performance from each style. Table 4.5 shows a summary of the fabricated devices and also the selected ones as a reference for comparison.

Table 4.5 List of designed and fabricated OTFTs

	FO interdigitated	PO interdigitated	C-shaped	Corbino
Minimum length (μm)	4	4	4	6
Width range (μm)	40-1880	40-1880	40-360	120-660
Number of reference OTFTs (μm)	200	200	200	150

The images of the fabricated plates during 6 runs at NeuDrive-CPI technology and the corresponding floorplan for each run is presented in Appendix A.

Figure 4.27 is also a micro-graph of the fabricated devices for all proposed layout styles. In order to show the fabricated transistors better, testing pads are cropped in this image.



(a) FO interdigitated (b) PO interdigitated (c) C-shaped (d) Corbino

Fig. 4.27 Micro-graph of the fabricated OTFTs

4.2.4 Large scale characterization of OTFTs

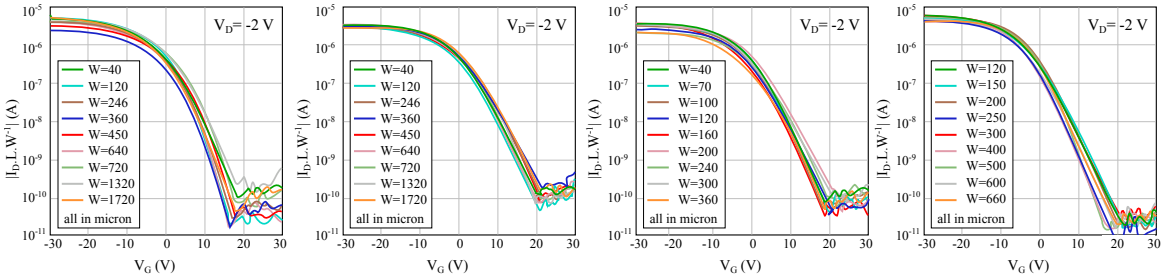
The fabricated arrays of OTFTs introduced in Section 4.2.2 were analyzed using performance parameters extracted from their I-V and C-V curves. The large scale characterization of devices will provide new inputs to identify potential layout style candidates for circuit implementation. However, not all of the characterization platforms and methods were available and used for every run and period of time, due to the consecutive (in time) design, fabrication and test strategy. Characterization of all devices have been done at electrical test laboratory of IMB-CNM and/or CPI.

I-V measurements

The static current-voltage (I-V) measurements were performed using keithley parameter analyzer in conjunction with a semi-automated probe-station allowing reliable statistical analysis and uniformity measurement to be performed over the substrate area. Figure 4.28 shows the width- and length-normalized (I_D.L/W) transfer characteristics in linear

regime ($V_{\mathrm{D}} = -2V$) for several OTFTs with a range of channel widths and minimum length for four layout styles.

As it is seen, partially-overlapped interdigitated devices represent the best repeatability with low deviation. The small variation in I-V characteristics of fully-overlapped devices is due to the fact that the real channel width is slightly different from the designed one, which is as a result of non-linearity on the corners of the channel width. This can also bring some difficulties in device modelling.



(a) Fully-overlapped interdigitated (b) Partially-overlapped interdigitated (c) C-shaped (d) Corbino

Fig. 4.28 Width- and length-normalized transfer plots in linear regime ($V_{\mathrm{D}} = -2V$). L_{min} is $4\mu m$ and $6\mu m$ for linear and corbino devices respectively

Turn-on voltage of the devices are located around 15-25 (V), which can be decreased to some extend by heating the devices. For FO transistors, turn-on voltage is lower than PO ones. Another important factor in transfer characteristics of the OTFTs is the $\mathrm{I_{on}/I_{off}}$ ratio, which is between 10^5-10^7, and is maximum for corbino-shape, and minimum for PO devices. The reason for higher $\mathrm{I_{off}}$ current of PO devices is due to incomplete etching of the organic semiconductor layer around the foot of the etched OSC and dielectric stack (using MET2 as a hard mask). The remaining semiconductor can result a small parasitic current between source and drain electrode whereas in FO style, the parasitic pathway is not present.

To study the variation in OTFT styles, and for comparing the transfer characteristics in different regimes, a subset of 20 transistors from each category with similar channel dimension were tested and the results are shown in Figure 4.29. For linear devices the channel length and width are $360\mu m$ and $4\mu m$ respectively, which leads to ($W/L = 90$), while the minimum length of the corbino transistors is $6\mu m$, and therefore, the width is designed $540\mu m$ in order to have similar aspect ratio as linear OTFTs.

Excellent repeatability of I-V characteristics can be observed when comparing PO, C-shaped and corbino devices, with average maximum saturation current of 322, 317, and 321 (μA), respectively. However, measured saturated current of FO transistors is 358 (μA), which is around 11% higher than others. The main reason for that is again

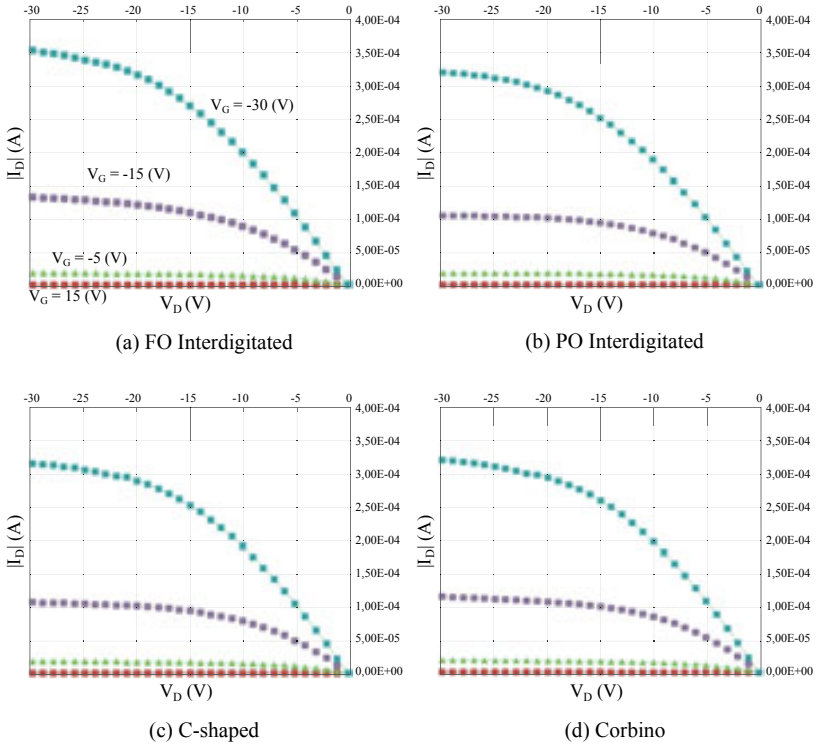


Fig. 4.29 Average I_D-V_D of 20 transistors from each category with similar aspect ratio

the corner section of channel in FO style that has not been calculated as a channel, but it exists. As the number of fingers increases, the corner effect increases. When using transistors in circuits, specially analog circuits, the channel width is required to be designed accurately for better fitting with the simulations. Thus, for larger interdigitated transistors, partially-overlapped design style is optimized in respect to accurate parameter extraction and modelling and matching.

Saturation mobility of similar devices is also illustrated in Figure 4.30. Its value has been calculated from Equation 3.3, which is in direct relation with channel dimensions (W, L). The mobility variation of fully-overlapped devices seem to be larger than the rest of devices, and due to larger real channel width, the average of mobility for this style is less than others.

Threshold voltage of all 80 devices were calculated similar way as Figure 3.13 in Chapter 3, and a small variation was observed for its value. For partially overlapped devices, it is between 9-11 (V), while the variation is larger for fully overlapped transistors, 8-13.5 (V). The number of occurrences of different V_{th}, I_{on}/I_{off} ratio, and mobility values for all design styles are shown in Figure 4.31.

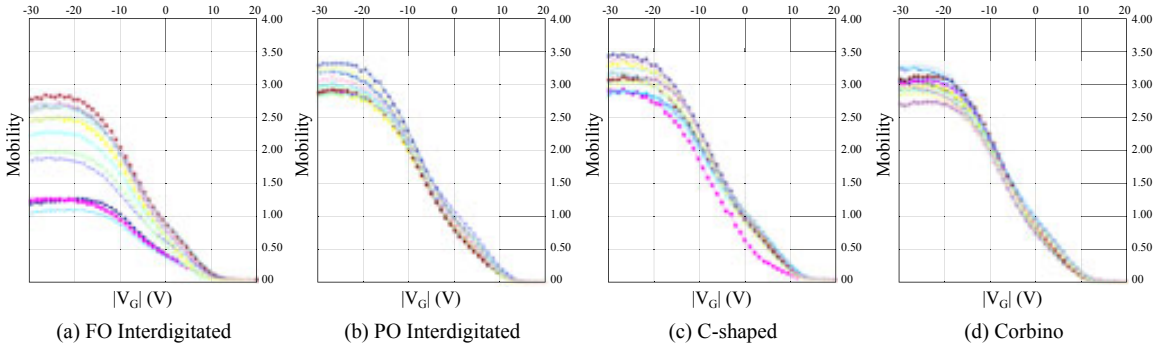


Fig. 4.30 Mobility curves of 20 transistors from each category with similar aspect ratio

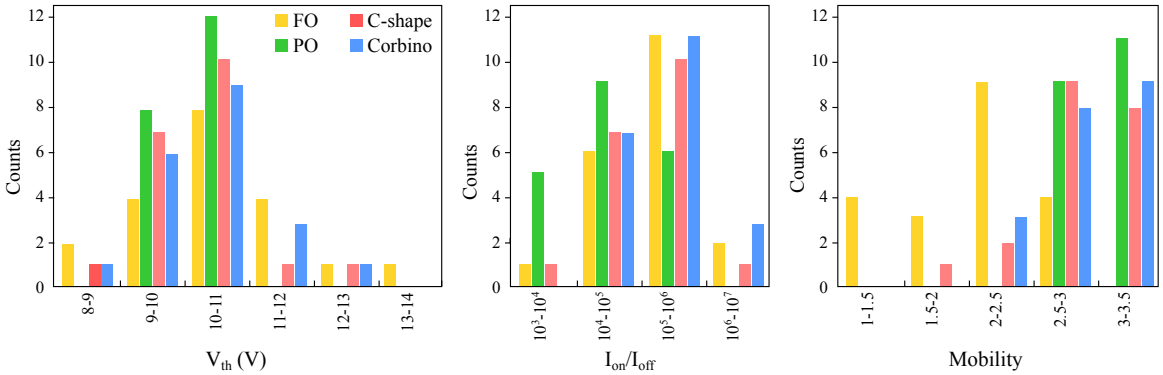


Fig. 4.31 Histogram of calculated threshold voltage, current ratio, and mobility for 29 transistors from each category

C-V measurements

The ac operation of OTFTs is essentially based on a capacitive coupling between the gate electrode and the semiconductor layer. Therefore, studying capacitance-voltage (C-V) characteristics is fundamental to understand the device behavior. In general, it is found that useful information is obtained from C-V measurements made for two different conditions: quasi-static and high frequency.

Quasi-static conditions correspond closely to equilibrium. Conventionally, a quasi-static C-V measurement is made by sweeping bias voltage applied to the gate-source so that the surface of the semiconductor changes from depletion to accumulation. During this procedure, the transient charging current of the Metal-Insulator-Semiconductor (MIS) capacitance is measured as a function of time. Obviously, integration of charging current over time merely results in measurement of the charge stored in the MIS capacitor; hence, capacitance as a function of voltage is determined by elementary identification of the product of capacitance and voltage as stored charge ($CV = Q$).

The quasi-static CV measurement of the fabricated OTFTs is investigated as a combination of two hypothetical parts: (1) Overlap capacitance (C_{ov}), which is the standard MIS capacitance of the sandwich structure made of gate, insulator, organic semiconductor, and source/drain electrodes (2) C_{ch} is the capacitance of the structure with peripheral organic semiconductor, which is not in direct contact with source/drain electrodes, and is known as channel capacitance.

Since the partial capacitance are in parallel, the CV characteristic of the overall structure (C_{tot}) is equal to the sum of the individual characteristics [229], [230]. Figure 4.32 presents an illustration of these hypothetical sections, as well as, their C-V characteristics for unit capacitance area.

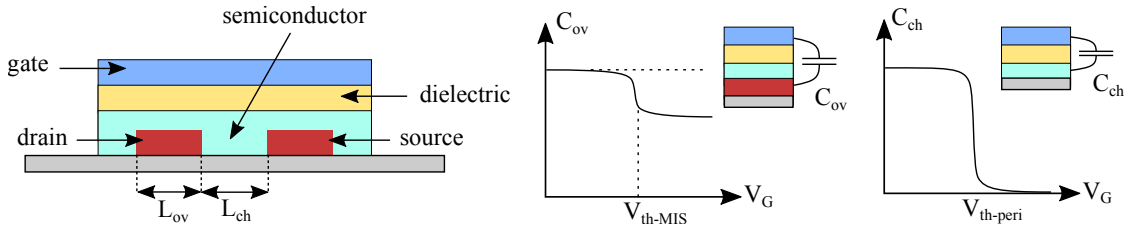


Fig. 4.32 Capacitance contribution of OTFT and their C-V representation

C_{ch} depends on the gate bias. Since the charge carriers can be injected into and removed from the peripheral film through the adjacent semiconducting layer, C_{ch} increases to maximum when the peripheral semiconductor film is in accumulation and decays to zero once it is depleted. C_{ov} changes slightly by voltage sweep. Depending on the applied bias, it changes between maximum when the charge carriers accumulate at the dielectric interface, and a minimum when the semiconductor film is depleted so that only the charge carriers on the Au electrodes respond to the gate bias. However, the changes on C_{ov} is smaller than changes in C_{ch}.

In quasi-static measurements, capacitance is measured directly by integrating charging current. However, CV measurements can also be made by superimposing a small sinusoidal oscillating signal on the voltage sweep and measuring the corresponding impedance directly as a function of bias voltage.

The capacitance-voltage (C-V) characteristics of the devices were measured by using Agilent 4294A precision impedance analyzer at frequencies from 5KHz to 12MHz in ambient air, and at room temperature. In order to measure the quasi-static characteristics of the fabricated OTFTs, the drain and source electrodes are electrically shorted and connected to the low terminal of the impedance analyzer, while the gate

electrode was connected to the high terminal. A DC potential sweep from -40 to +40 along with a superimposed AC voltage (V_{m}) of 500 mV was applied to the gate.

Figure 4.33 shows the C-V measurement of four type of OTFT layouts with similar channel width. Although the channel length of corbino devices is slightly larger than linear ones, all the measured samples have similar channel width ($W = 360\ \ m$). This is because C_{ov} is directly dependent on the gate overlapping area, which is function of channel width.

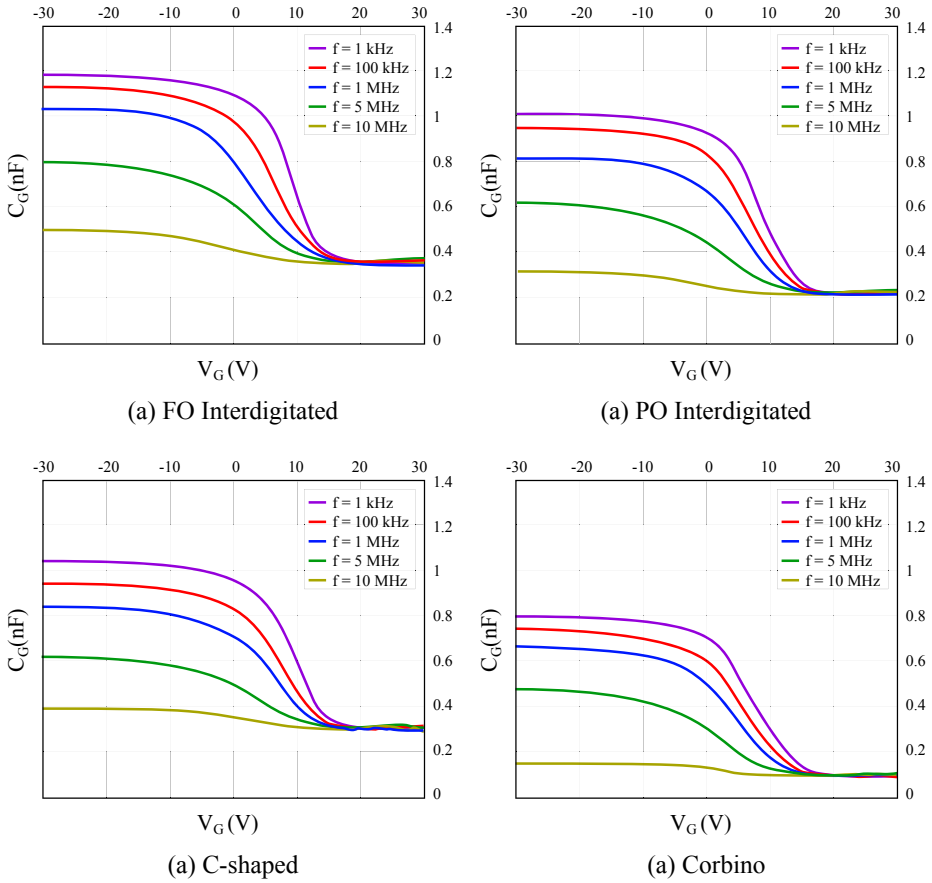


Fig. 4.33 Capacitance-voltage (C-V) characteristics of four OTFTs with similar channel width and different layout styles

The C-V curves show a transmission from depletion (at high positive voltages) to accumulation (high negative voltages). The capacitance increases and saturates as the gate voltage decreases, indicating the formation of an accumulation channel. As the frequency increases, the accumulated charges in the gate-induced channel cannot follow the signal. The maximum capacitance is measured for the lowest measured frequency (1 KHz) in accumulation region, and the minimum capacitance is observed in depletion region.

As mentioned before, the measured capacitance has two main contributions: (1) The geometrical capacitance between the gate and the channel (C_{ch}), and (2) The overlap capacitance (C_{ov}) between the gate and source/drain electrodes which equals to C_{min}. The later one can be directly read on the C-V curve, in a regime where there is no channel (depletion regime: V_G=30 (V)). This value can also be calculated from Expression 4.1.

$$C_{ov} = C_I \quad A_{ov} \tag{4.1}$$

where C_I and A_{ov} are the insulator capacitance per unit area ($6nF\,cm^{-2}$), and overlapping surface between gate and source/drain electrodes. In order to measure the accurate overlapping area for each design style, and match it with measured C_{ov}, the layout of the OTFTs is shown in Figure 4.34. In order to simplify the structure, the top gate contact (MET3), which is electrically in contact with MET2 gate and does not provide much parasitic capacitance, is ignored for calculations. Since the overlap surface of C-shaped transistors is similar to PO interdigitated ones with 2 number of fingers (n=2), its layout is not shown in this figure.

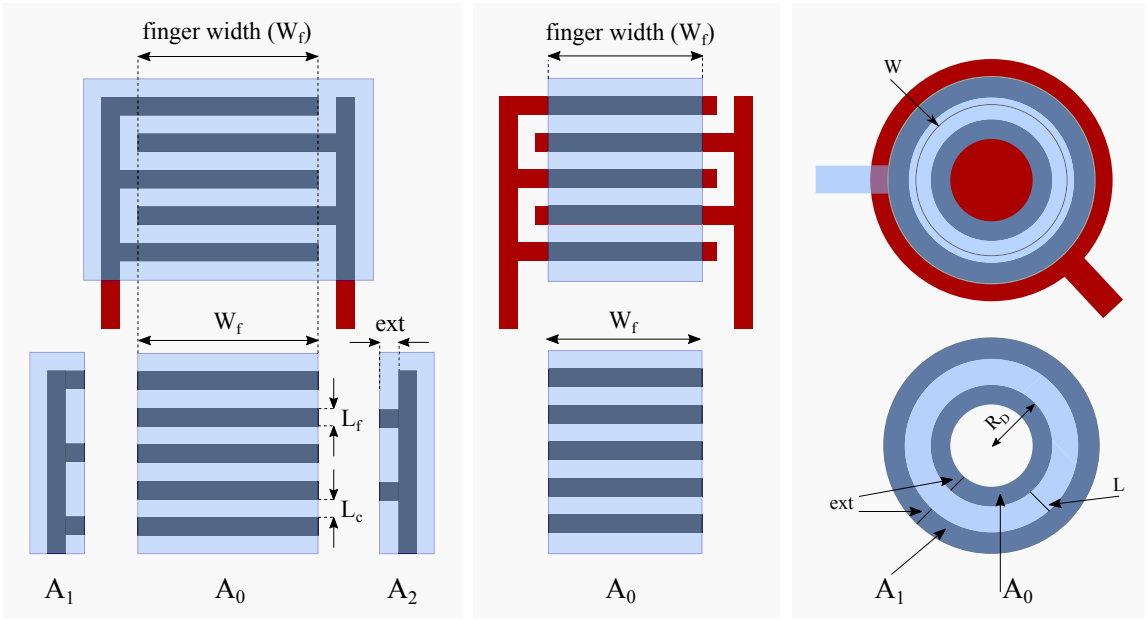


Fig. 4.34 Gate overlap surface with drain/source

The overall overlapping surface of FO interdigitated structures is parsed into three main regions: (1) A_0, which is related to the fingers overlap, (2, 3) A_1 and A_2, which

are related to electrodes and small extensions. Therefore, $A_{ov}=A_0+A_1+A_2$, where each contributor is calculated as below:

$$A_0 = (n+1).W_{\mathrm{f}}.L_{\mathrm{f}} \tag{4.2}$$

$$A_1 + A_2 = L_{\mathrm{f}}.(2.L_{\mathrm{f}} + 2.L_{\mathrm{c}} + ext)(n+1) \tag{4.3}$$

The tested FO transistors have ($W_{tot}=360\mu m$), with ($W_f=60$, and $n=6$). Taking into account the insulator capacitance per unit area ($\approx 6nF.cm^{-2}$), and calculated A_{ov} from Equations 4.2 and 4.3, the overlap capacitance in depletion regime is calculated:

$$FO : C_{\mathrm{ov}} = C_{\mathrm{I}}.(A_0 + A_1 + A_2) = 6 \times (3780 + 1827)\frac{nF}{cm^2}.\mu m^2 = 0.34pF \tag{4.4}$$

The calculated overlap capacitance value ($C_{ov\text{-}cal}$=0.34 pF) for FO interdigitated devices is very close to the measured one in depletion regime ($C_{ov\text{-}meas}$=0.36 pF).

For PO interdigitated and C-shaped devices, A_1 and A_2 is not present, and it leads to quite smaller parasitic capacitance. Therefore, $A_{ov}=A_0$, where A_0 is also calculated from Equation 4.2. The tested PO interdigitated and C-shaped transistors in Figure 4.33 have $W_{tot}=360\mu m$, with (W_f=60, and n=6) and (W_f=180, and n=2) for PO and C-shaped, respectively. Therefore, the overlap capacitance can be calculated as below:

$$PO : C_{\mathrm{ov}} = C_{\mathrm{I}}.A_0 = 6 \times (3780)\frac{nF}{cm^2}.\mu m^2 = 0.23pF \tag{4.5}$$

$$C - shaped : C_{\mathrm{ov}} = C_{\mathrm{I}}.A_0 = 6 \times (4860)\frac{nF}{cm^2}.\mu m^2 = 0.29pF \tag{4.6}$$

Similarly, the calculated overlap capacitance value for PO ($C_{ov\text{-}cal}$=0.23 pF) and c-shape ($C_{ov\text{-}cal}$=0.29 pF) devices is very close to the measured one in depletion regime ($C_{ov\text{-}meas}$=0.21pF and 0.30pF). It is clear that for C-shape structure the overlapping area of large width devices ($W_{\mathrm{f}} > 100\mu m$) is slightly higher PO ones. Thus it is desired to use C-shape devices when small channel width is required.

Regarding the corbino transistors, the gate overlap surface is also parsed into two main regions: drain (A_0), and source (A_1). They are simply calculated from conventional equation for annulus surface, in which inner and outer radius for A_0 are (R_{in0}=R_D-ext) and (R_{out0}=R_D), and for A_1, they are (R_{in1}=R_D+L), and (R_{out1}=R_D+L+R_S) respectively.

$$A_{ov} = A_0 + A_1 = \pi({R_{out0}}^2 - {R_{in0}}^2) + \pi({R_{out1}}^2 - {R_{in1}}^2) \tag{4.7}$$

The channel width of the tested corbino devices is $W = 360\mu m$, and C_{ov} is:

$$Corbino : C_{ov} = C_I.(A_0 + A_1) = 6 \times (989 + 1159)\frac{nF}{cm^2}.\mu m^2 = 0.13pF \tag{4.8}$$

The calculated value is also very similar to the measured one ($C_{ov\text{-}meas}$=0.1 pF). As it is demonstrated corbino and PO interdigitated devices have the lowest overlap parasitic capacitance, and are recommended design styles for circuit applications, where low parasitic and high operating frequency is desired. The main drawback of the corbino devices is that they occupy more space comparing to interdigitated ones, and it is because of their round shape. Therefore, partially-overlapped devices are the best candidate for being both parasitic- and area-effective.

4.3 Ratioed p-type Inverters

In this section, we present inverter circuit as the most basic and important logic gate in digital integrated circuits. First, the selected logic style and its characteristics are presented, and then the designed and fabricated inverters are characterized statically and dynamically, in order to extract the electrical behavior of the circuit.

The high positive turn-on voltage ($\approx 20V$) seen in the transfer plots in Figure 4.28 result is *normally on* transistors. As discussed in Section 3.5, Zero-V_{GS} logic style is the best candidate for implementing circuits, when only p-type transistors with positive threshold voltage is available in the technology.

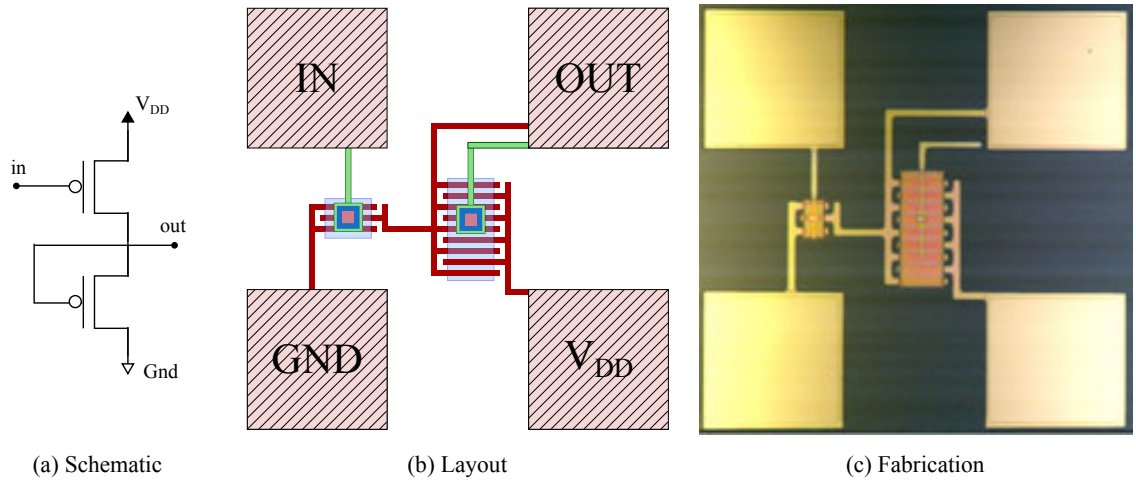
To aid circuit design prior to fabrication, the response of inverters can be simulated using the extracted transistor model. However, due to the process variation at early stages of the thesis and also the limitations in device modelling, circuit simulation has not been possible until the moment of writing the thesis. Therefore, several inverters

with different drive to load ratios were designed, fabricated, and tested, in order to obtain the optimum ratio and transistor dimensions.

Although all types of the transistor layouts (presented in Section 4.2.2) were used for designing inverter circuits, we only show partially-overlapped interdigitated ones, since they have shown higher performance, less variation, and better repeatability.

4.3.1 Design and fabrication

In Zero-V_{GS} design style, it is desired to size the load transistor larger than drive one. Therefore, an array of 40 inverters with four different load to drive ratios of (3, 5, 7, and 9) were designed by using pcell codes and scripts. The minimum channel length for all the transistors were fixed to ($L = 4\ \ m$), and only the channel width changes. The total channel width for the drive transistor is fixed to 50 m, and for the load is 150, 250, 350, and 450 m respectively. Figure 4.35 shows the schematic, layout, and fabricated Zero-V_{GS} inverter, with load to drive ration of 7. All of the designed inverters have four large pads (150 m 150 m) for electrical testing.



(a) Schematic (b) Layout (c) Fabrication

Fig. 4.35 Zero-V_{GS} inverters

4.3.2 Static characterization

In order to evaluate the performance of the inverter gates, 40 fabricated inverters were characterized to obtain the static in-out transfer curve. Figure 4.36 shows the transfer curves of all the tested inverters with different load to drive ratio (3, 5, 7, and 9) for several supply voltages (20, 30, 40, and 50 V). The average transfer curve for every 10 inverter in its category is illustrated in Figure 4.37, as well as the average gain.

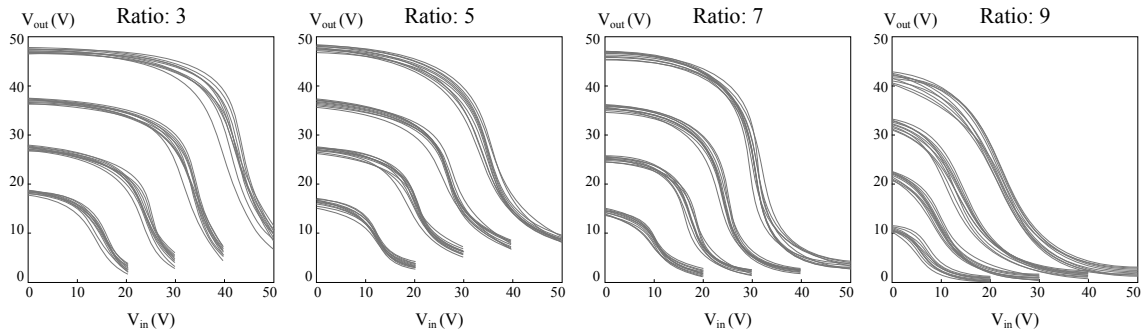


Fig. 4.36 Static in-out characteristics of the inverters

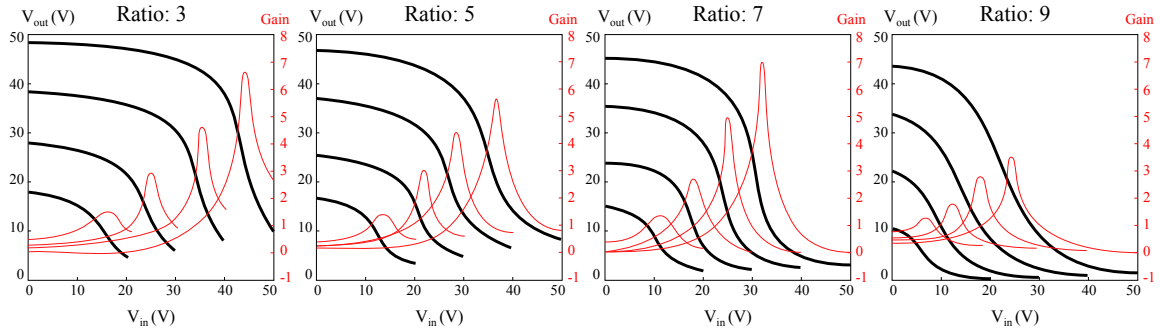


Fig. 4.37 Average static transfer curve and unity gain of the inverters

According to Figure 4.37, the gain of the inverters are almost similar for load to drive ratios of 3, 5, and 7. Inverters with load to drive ratio of 7 has slightly higher gain, equal to 7 for V_{DD}=50 (V), while ratio 9 has the lowest gain (3.6).

To ensure the proper operation of the digital circuit, one has to take into account some stability considerations. In particular, the Noise Margin (NM) of an inverter is an important figure for the stability of the digital circuits. It was originally defined as the maximum allowable spurious signal that can be accepted by a device when used in a system while still giving correct operation.

For an inverter, it is possible to define the high and low voltages V_{OH} (minimum output high voltage) and V_{OL} (maximum output low voltage). Furthermore, one can define the transition points V_{IH} and V_{IL}, where V_{IH} is the minimum input high voltage that can be treated as a high voltage at the input of an inverter and V_{IL} is the maximum input low voltage that can be treated as a low voltage at the input of an inverter. If one has an inverter satisfying the relationships:

$$V_{\mathrm{in}} \leq V_{\mathrm{IL}} \rightarrow V_{\mathrm{out}} \geq V_{\mathrm{OH}} \tag{4.9}$$

$$V_{\text{in}} \geq V_{\text{IH}} \rightarrow V_{\text{out}} \leq V_{\text{OL}} \tag{4.10}$$

$$V_{\text{IH}} \geq V_{\text{IL}} \tag{4.11}$$

Then the high noise margin (NM_{H}) and the low noise margin (NM_{L}) are defined mathematically as:

$$NM_{\text{H}} = V_{\text{OH}} - V_{\text{IH}} \tag{4.12}$$

$$NM_{\text{L}} = V_{\text{IL}} - V_{\text{OL}} \tag{4.13}$$

To ensure a stable operation of the inverter, its noise margins NM_{H} and NM_{L} need to be sufficiently positive. The noise margin of a logic gate is directly related to the reliable and robust operation of the logic circuit: the higher the noise margin, the more reliable the circuit. As the circuit complexity (expressed by the number of transistors in a circuit) increases, the noise margin can even be related to circuit yield [231].

According to Equations 4.9 and 4.10, the forbidden working region for the inverter is shown in Figure 4.38 (a) (Source: [231]). There are several methods to calculate the value of noise margin, and we have chosen the Maximum Equal Criteria (MEC), in which the NM value is side of the biggest square that fits in the inverter curve loop $V_{\text{out}} = f(V_{\text{in}})$ and $V_{\text{out}} = f^{-1}(V_{\text{in}})$. Figure 4.38 (b) illustrates the concept of the MEC to calculate NMs.

Noise margin value of the inverters is influenced by many factors and transistor parameters, such as the output resistance parameter (λ), threshold voltage difference between drive and load transistors (ΔV_{T}), and mobility difference between drive and load transistors ($\Delta\mu$), which have been investigated in [231]

NM of the fabricated Zero-V_{GS} inverters for different ratios at $V_{\text{DD}} = 50$ (V) were studied in order to obtain the best ratio, in respect to robustness, and it is shown in Figure 4.39. The trip point (V_{trip}), which is where the input and output voltages are the same, is an important static characteristic of the inverter and it directly affects the

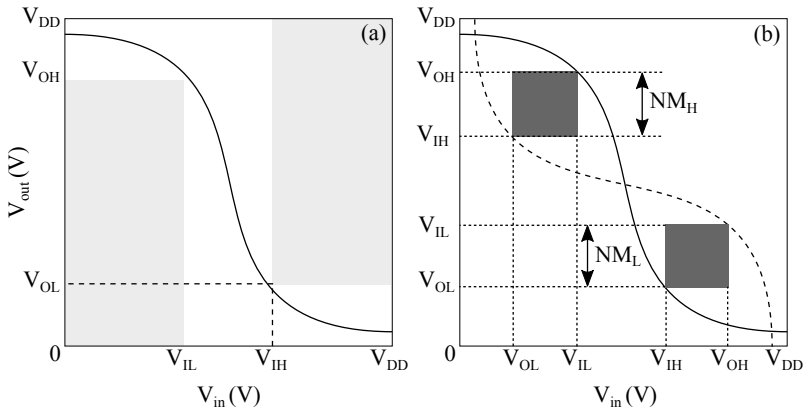


Fig. 4.38 Inverter transfer curve: noise margin and forbidden area definition

noise margin values. In an ideal inverter, the trip point should coincide with the point of maximum gain and be at the centre of the supply (shown in Figure 4.39).

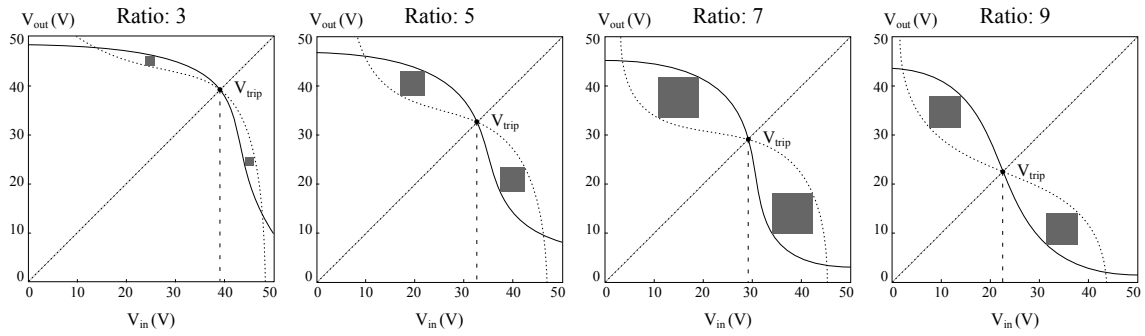


Fig. 4.39 Calculation of the noise margin for inverters with different load to drive ratios

It is seen that the load to drive ratio of 7 offers the highest noise margins, since the side of the generated square is larger than the others. Furthermore, the trip point for ratio7 and 9 are almost located at the center of supply voltage, while for ratio 3 and 5, it is shifted to around 40, and 33 (V) respectively. The output swing of the transfer curves is also strongly dependent on the load to drive ratio, and for ratios 7, and 9 it is the highest. This is because of the voltage divider when $V_{\text{in}} = V_{\text{DD}}$. and both drive and load transistors are on at $V_{\text{GS}} = 0$.

According to the static characteristics of the inverters, it is obvious that the load to drive ratio of 7 provides the optimum behavior in respect to noise margin, output swing, trip point, and gain. Therefore, from now on, only inverters with this ratio will be used for further characterization and use in digital circuits.

4.3.3 Dynamic characterization

Another typical type of analysis performed on digital circuits is dynamic analysis that can be AC, transient, and noise analysis. AC and noise analysis are quite specific for analog circuits that operate on continuous signals and they do not apply for logic circuits (specially for high supply voltages).

Transient analysis is critical for characterization of digital logic circuits, and is the key factor for defining the maximum operation frequency and speed of the circuits. For that, there are some important parameters in dynamic characterization of inverters, which are propagation delay and rise/fall times. The definition of propagation delays and rife/fall time is shown in Figure 4.40.

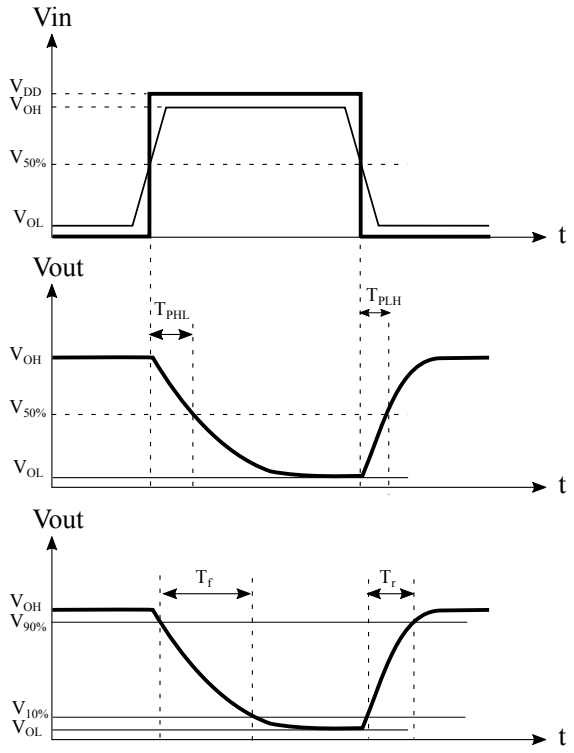


Fig. 4.40 Definition of propagation delays and rise/fall time for inverters

Due to the ratioed nature of the implemented unipolar inverters in this thesis, the pull-down delay is much larger than the pull-up delay, as the pull-down current provided by the load OTFT is much smaller than the transient pull-up provided by the driver. The reason is that the pull-up phase is realize by fully accumulated driver transistor when $V_{\mathrm{GS}} = -V_{\mathrm{DD}}$, while the pull-down phase is realize by load transistor when $V_{\mathrm{GS}} = 0$.

The dynamic performance of a logic family is characterized by propagation delay of its basic inverter. The average delay is defined as the average of low-to-high (V_{PLH}) and the high-to-low (V_{PHL}) propagation delays, as shown in Equation 4.14

$$T_P = \frac{T_{PHL} + T_{PLH}}{2} \tag{4.14}$$

The propagation delay increases as the fan-out increases, therefore, the maximum fan-out is defined according to the maximum acceptable propagation delay time.

The dynamic characterization of the inverters was realized by using a pico-probe in order not to load the output node with extra capacitance. A 30 (v) p-p input pulse with 100 KHz was applied to the inverter. The "in" and "out" signals are shown in Figure 4.41. The output signal should be scaled by 1.8X, which is the attenuation factor of the Pico-probe used to measure the output, thus, the p-p output swing is 28.8 (V). Fall and rise times are measured by the oscilloscope, and shown at the bottom of the signals ($T_f = 0.7\mu s, T_r = 0.4\mu s$).

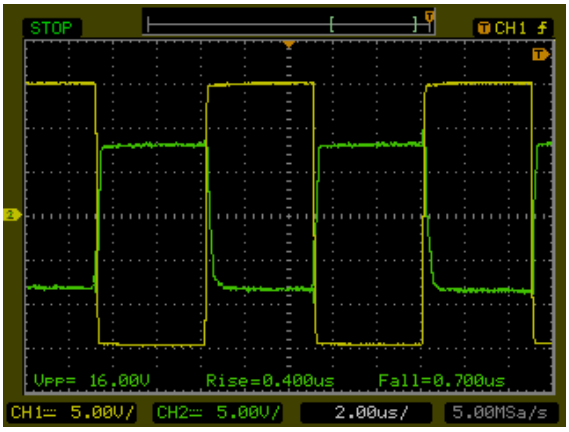


Fig. 4.41 Dynamic characterization (in-out curve) of the inverter

The high-to-low and low-to-high propagation delays are also measured and equal to $T_{PHL} = 0.28\mu s, T_{PLH} = 0.13\mu s$, therefore, the propagation delay of the inverters is calculated from Equation 4.15, and is equal to: $T_P = 0.2\mu s$.

$$T_P = 0.5T_{PHL} + 0.5T_{PLH} \rightarrow T_P = 0.5(0.28\mu s) + 0.5(0.13\mu s) = 0.2\mu s \tag{4.15}$$

Further improvement for reducing the inverter propagation delay can be done by increasing the mobility of organic semiconductor, and reducing the channel length, and also reducing the parasitic overlap between gate and source/drain electrodes.

4.3.4 Ring oscillator

There has been a steady progress in increasing both the speed and complexity of organic integrated circuits. A very important and indicative circuit, which can give a comprehensive description of the printing technology and its adapted circuit design technique, is ring oscillator. It is used for on-circuit clock generation, but also for determining the speed of a given design technology, accounting for the effects of the organic materials, interconnections, and design styles. Ring oscillator is basically a chain of odd number of inverters in a ring, whose output oscillate between two voltage levels (maximum output swing). The output of the last inverter is fed back into the first one. Usually, one or two inverters are used after the chain in order to improve the output signal shape, being called "buffer". Figure 4.42 shows the schematic of a five stage ring oscillator that has been taken as the reference during this thesis.

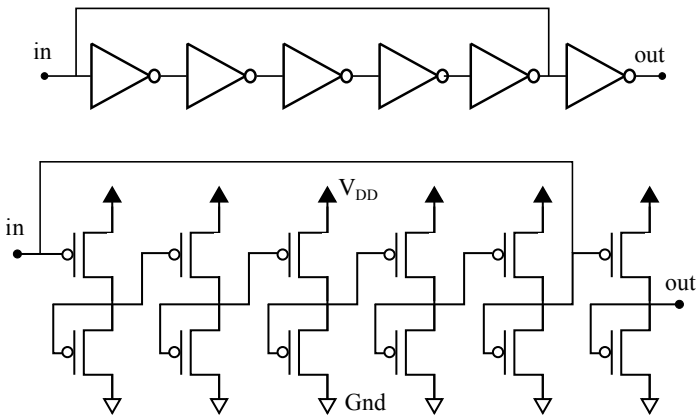


Fig. 4.42 Schematic of a 5-stage ring oscillator with an output buffer

Several ring oscillator circuits have been implemented in the state of the art by using both solution processing and vacuum evaporation of organic semiconductor. The most important parameter in characterization of ring oscillators is the oscillation frequency, which is dependent on the number of stages, the minimum transistor channel length, and the propagation delay of each inverter, being known as stage delay. Table 4.6 lists some of the implemented ring oscillators for organic electronics in the literature (source: [232]).

Table 4.6 Comparison of the state of the art ring oscillators

Technology	number of stages	L (μm)	f (KHz)	T_P (μs)	Reference
Mass printed R2R unipolar	7	100	0.004	17900	[233]
Mass printed R2R unipolar	5	45	0.006	16700	[234]
Mass printed R2R unipolar	5	40	0.3	333	[235]
Vacuum R2R unipolar	5	40	2.16	46.3	[236]
Spin-coated ambipolar	5	5	0.35	286	[237]
Spin-coated ambipolar	3	5	182	0.91	[238]
Spin-coated ambipolar	5	5	42	2.38	[239]
Spin-coated unipolar	11	4	31.4	1.45	[240]
Spin-coated unipolar	7	5	22	3.3	[241]
Spin-coated unipolar	7	1.5	100	0.712	[242]
Spin-coated unipolar	7	2.5	45	1.6	[243]
Inkjet complementary	5	5	80	1.25	[244]
Solution processed	7	5	2.9	24.6	[245]
Evaporated unipolar	5	5	0.59	170	[246]
Evaporated unipolar	19	2	66	0.4	[247]
Evaporated unipolar	11	1	150	0.3	[248]
Evaporated unipolar	5	2	440	0.23	[249]
Evaporated complementary	2	200	0.004	0.5	[250]
Evaporated complementary	1	14.7	0.004	3.1	[251]
Evaporated complementary	3	13.9	0.004	0.89	[252]
Inkjet unipolar	19	5	0.5	52.6	[253]
Inkjet complementary	5	20	714	0.14	[254]
Spin-coated unipolar	5	4.6	529	0.189	[232]
Spin-coated unipolar	5	4	617	0.162	This work

In this work, we are showing ring oscillators with better performance in respect to the oscillation frequency and stage delay, by spin coating the FlexOS^{TM} organic semiconductor, which is a combination of small molecule and semiconducting polymer with good uniformity. The fabrication process is similar to the one explained in Section 4.2.1.

Many arrays of ring oscillators have been designed and fabricated during the thesis, and several parameters have been swiped in order to characterize the circuit performance and effect of each parameter, such as, channel width and length, number of stages, source/drain electrode width, load to drive ratio in inverters, and etc. However, I skip mentioning the detailed results of each parameter influence, since the main focus of the thesis is to design similar circuits in semi-custom manner through the use of Inkjet-configurable Gate Arrays (Chapter 5).

That being said, I mention the characterization of 30 number of 5-stage ring oscillator circuits with output buffer, using PO interdigitated OTFTs with minimum channel length equal to ($L = 4\mu m$). The inverters in the ring oscillators are similar

to the ones that were studied in previous chapter. Figure 4.43 is a micrograph of the fabricated 5-stage ring oscillator.

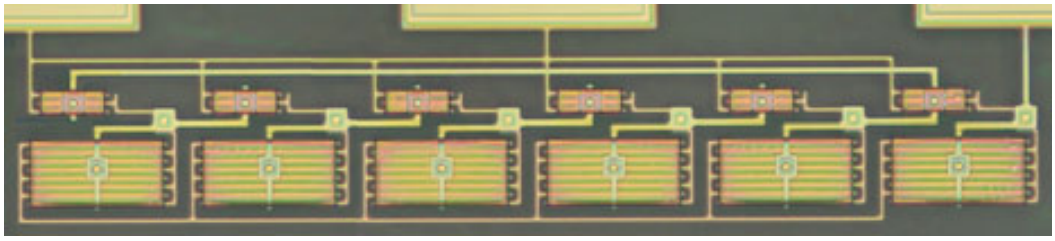
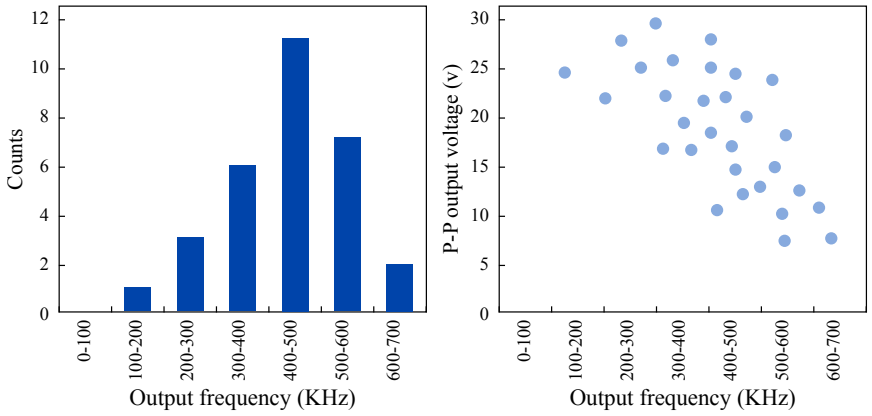


Fig. 4.43 Micro-graph of the fabricated 5-stage ring oscillator

All of the ring oscillators were tested by using the same pico-probe. It was found necessary to increase the supply voltage to 30V to initiate stable oscillation with 40V being typical. Figure 5.31 (a) is a histogram shown the number of ring oscillators with output frequency in the 100KHz band, and (b) is the output frequency versus p-p swing of the ring oscillator for 30 samples.



(a) Histogram of RO count with F (b) Frequency vs. p-p output swing

Fig. 4.44 Histogram of the ring oscillators

Figure 4.45 shows the maximum oscillation frequency obtained from the tested ring oscillators, which is 617KHz with 8.64 (V) output swing. The displayed voltage should be scaled by 1.8X to account for the pico-probe impedance mismatch with the oscilloscope.

According to the stage delay of inverters in previous section, the expected oscillation frequency of the ring oscillators can be estimated by using the Equation 4.16, where N is the number of stages.

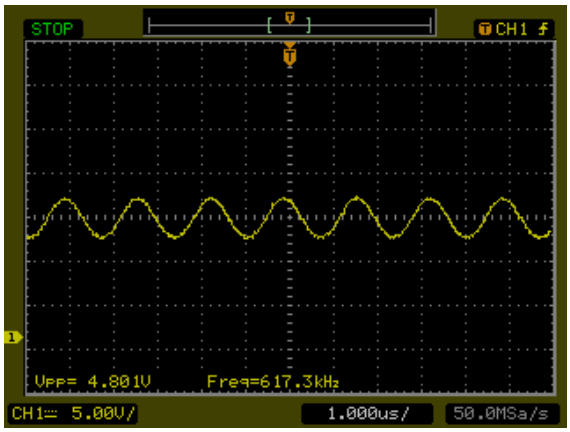


Fig. 4.45 Output voltage of a ring oscillator with highest oscillation frequency

$$F = \frac{1}{2NT_{\mathrm{P}}} = \frac{1}{2 \times 5 \times 0.2\mu s} = 500KHz \tag{4.16}$$

The measured results show that the average frequency of 30 tested ring oscillators is ($F_{\mathrm{average}} = 451KHz$), and the maximum oscillation frequencies ($F_{\mathrm{measured}} = 617KHz$) is even 23% higher than the calculated value ($F_{\mathrm{calculated}} = 500KHz$), and is the highest frequency comparing to the table 4.6.

Reduction in finger (drain and source) width from $5\mu m$ to $2\mu m$ was shown to improve the stage delay of the inverters two times in [255]. Therefore, it is expected to permit the oscillation frequency in excess of 1 MHz by reducing the finger width from $8\mu m$ to $2\mu m$. However, it requires process improvement and patterning with higher resolution, which is being investigated.

4.4 Summary

In this chapter, we tried to address the global goal of building a bidirectional bridge around the PDK concept to allow an early co-development of technology and design issues for its rapid deployment on the application arena. The original idea behind the development of PDK is to facilitate manufacturability of any particular process, by providing standard rules and formats to be exchanged between technology and designer engineers. For any given technological process, its PDK consists of a set of information, such as, technology files, geometrical design rules, compensation rules and patterns, electrical models, and a library of very basic devices.

Geometrical design rules are set of physical rules, provided by process engineers that should be respected by design engineer in order to ensure that there is no short or open circuit in the final prototype. To address the extraction of geometrical design rules, that are critical when developing new technologies, we proposed a methodology and a semi-automatic environment that goes from formalization of design rules and Pcell-based automatic test vehicle generation to the computer-based setup management, operation and results collection (measurements and pictures) and delivery for its further analysis.

Later, the pcells, as a technology-independent approach, was used to develop the basic libraries consisting of passive (resistors, capacitors, and inductors) and active devices (diodes and transistors) for any given technology. In particular, a clean room photolithography process was taken as reference for development of OTFTs. Different factors, such as, materials, fabrication technologies, and physical layout styles, affect the electrical parameters of organic transistors. In this thesis the later factor have been investigated and several layout styles (Interdigitated, Corbino, C-shaped) were proposed and compared for achieving the optimized one in respect to the performance and reliability of transistors. After static and dynamic characterization of all of the devices, partially-overlapped interdigitated OTFTs with lower variability and higher performance was selected as the best candidate for further implementation of organic electronic circuits.

Due to the fact that the p-type transistors are so-called depletion-mode with positive threshold voltage, the Zerp-V_{GS} ratioed style was selected as the logic family and inverters and nand logic gates were designed and optimized in respect to their electrical performance. Finally, ring oscillators with maximum oscillation frequency of 617 KHZ, and average of 451 KHZ for 30 ring tested circuits was demonstrated, which can even be improved by reducing the parasitic overlap between gate and the source/drain electrodes.

Chapter 5

INKJET-CONFIGURABLE GATE ARRAY (IGA)

Currently, most of the printed electronic circuits are yet designed by specifying the layout of each individual transistor and their interconnections; using a full-custom design methodology. Full-custom design is extremely labor-intensive, time consuming for complex circuits and advanced computer software is required in the design process. Additionally, several mask sets are required in order to transfer the circuit designs onto the wafer, and the mask cost is not shared between different applications. Even for mid-yield processes (considering faults at transistor level), it cannot avoid causing very low yield at circuit level as the failure of one transistor will let the failure of the whole circuit functionality.

In contrast, array-based semi-custom design methodology, (See Section2.3) alleviate the often prohibitive time and expense of design and fabrication, by separating the master slice manufacturing process from functional personalization step. A mask set for generic array of pre-defined cells and transistors is used to partially fabricate device. The fabricated chips/foils will be stockpiled in large quantities regardless of customer orders. The customization of the master slices to desired functionalities is realized by using final metal layer mask(s), which is known as metallization/personalization/customization step. In this way, the costs of the shared masks are spread over all applications and only the cost of the final customising mask is additional. These two steps take place in different moments in time, but through the same photolithography process.

In this work, the novel concept of Inkjet-configurable Gate Arrays (IGA) as a design-manufacturing method for organic electronics is proposed. It brings together the advantages of gate array circuit design methodology, fault tolerance, and field-configurability feature, through the best use of digital printing techniques. In the

proposed approach, the first manufacturing step, which is the fabrication of the IGA bulk or master foils/chips through mask-based photolithographic technology, is similar to conventional gate array industry. But, the second step (metallization) in silicon gate arrays, which requires generation of new mask(s) for individual circuit personalization, can be replaced by a single process of mask-less digital printing technique.

Field-configurability allows the designer to customize pre-fabricated IGA bulks in the field (at home) without disassembling or returning it to its manufacturer. Thus, circuit implementation with specific functionality can be mapped onto individual IGA foil, by adding final wiring step by using digital printing technique in the field, due to the availability and low-cost of additive manufacturing techniques, such as inkjet.

The main advantage of this approach is increasing functional capabilities by using digital Drop-on-Demand (DoD) printing to customize every individual fabricated master slice (master foil) to its unique functionality. The use of additive mask-less printing techniques enables quick and accurate placement of wires and interconnects at a very low cost, thus avoiding the need for EEPROM devices or a new mask for functionality personalization. IGA for functionality personalization, and its corresponding design flow is introduced and explained in Section5.3. Some IGAs taking the benefits of this feature were designed and fabricated through a high-yield high-performance photolithography process.

Fault tolerance technique allows the adoption of a failure map to use only working transistors when personalizing the system to a desired functionality. Thus, the advantage of adopting fault tolerance technique in IGA is obtaining high yield at system-level out of mid yield foils at device-level (OTFTs). Section5.5 explains about fault tolerant feature in IGA, as well as the corresponding design flow, and some fabricated foils through a mid-yield all-inkjet process.

5.1 First step: IGA bulk

Similar to conventional gate arrays, the first manufacturing step is fabrication of the IGA bulk, or master foils, in which regular arrays of pre-defined OTFTs or logic cells, surrounded by uncommitted wire channels are manufactured in large volume. These foils, which are categorized in different families in respect to the integration complexity and available resources, can be stockpiled in large quantities regardless of the final application.

However, design and fabrication of IGA bulk in printed and organic electronics is not as straightforward as silicon industry, in which well-established processes and their

corresponding PDK facilitate the design-technology interaction. Printed electronics, as a technology that uses organic (sometimes with also inorganic) materials to implement all the layers of the circuit on non-crystalline substrates, includes a large variety of fabrication processes (printed or evaporated) that has led to a collection of printed devices and circuits with distinct resolutions, circuit area (foil or chip), and stack of layers. Each technology uses its own fabrication process, materials, and layers.

These layers are being mapped into classical EDA functional layers and physical design rules. Thus technology information related to layout design of devices and circuits differs largely from technology to technology. In order to design the IGA master foil scalable and compatible with any printing technology, pcell approach has been used. Therefore, the IGA bulk can be generated through a set of pcells, which take the technology file (stack of layers and their geometrical design rules), and device parameters (transistor channel length and width) as inputs and generate the desired layout, according to the particular technology and design constraints.

The basic structure of the proposed IGA is made of four pcells: (1) Basic bulk cell, (2) Wire cell, (3) Inter-cell connection, and (4) I/O pads and power rails. Each of them is defined and explained below. The IGA structure is shown in Figure 5.1 in an abstract view. Generally, the number of basic bulk cells, pads, and width of the wire channel is parameterizable and scalable thanks to pcell approach.

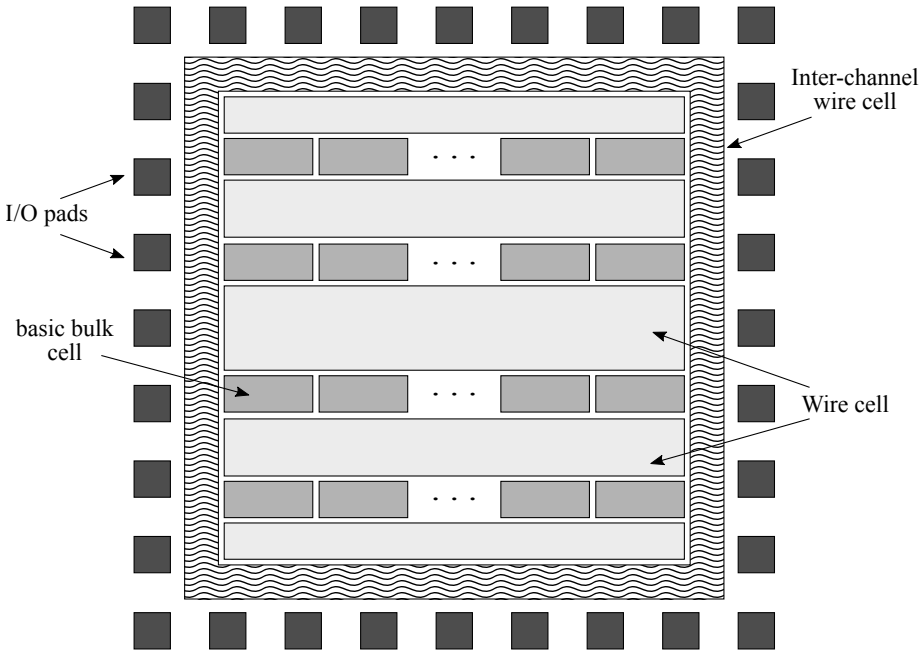


Fig. 5.1 Abstract view of the proposed IGA structure

5.1.1 Basic bulk cell

Basic Bulk Cell (BBC), which consists of a small array of unconnected OTFTs, is the most basic element of the IGA structure, and is responsible for the generation of elementary logic gates, such as Inverter, NAND, and NOR. Basically, each of these elementary gates are made of a pull-up network (drive) and pull-down network (load). There are several factors, affecting the number, type, and dimensions of drive and load transistors inside a BBC block.

Selection of the digital logic family depends on the existing transistors (p-type only, or p- and n- types) in the technology by which the IGA is fabricated. For example, if both p-type and n-type organic transistors are available in the technology, CMOS logic style would be the best candidate. Otherwise, when the process is restricted to p-type only transistors, one can choose either $Zero - V_{\mathrm{GS}}$ or diode-load logic style, depending on if transistors operate as depletion-mode or enhancement-mode. The dimensions of the drive and load transistors also depend on the similar issue. (See Section3.5).

The number of drive and load transistors in BBC cell depends strongly on the yield of the technology at OTFT-level, and also the logic style. For clean room processes with very high yield, where almost all of the transistors are expected to work properly ($\approx 99.99\%$ yield), this number only depends on the logic style. In this case, for CMOS logic family similar number of drive and load transistor is expected in each BBC block, while for ratioed p-type style, the number of drive OTFTs is expected to be at least twice as the number of load ones. This is due to the fact that in ratioed p-type style, the pull-down network is always made of one load transistor, and the function is realized through the pull-up network. More analysis on selection of number of drive and load transistors are brought in Sections 5.3 and 5.5 for each type of manufacturing technology.

Lack of a reliable transistor model and circuit simulation has made the job difficult for the circuit designers to design logic gates with accurate transistor dimensions and drive to load ratio. According to state-of-the-art logic synthesis technologies using And-Inverter-Graphs (AIG), that represents a structural implementation of the logical functional of a circuit, any network of logic gates can be expressed in terms of AND (which is NAND+INV) gates and inverters. This conversion does not lead to unpredictable increase in memory use and run time, but an efficient representation in comparison with other forms (such as binary decision diagrams or BDDs).

Considering two above-mentioned reasons and also the technology limitations, Inverter and NAND2 (and optionally NAND3, NAND4, etc. to reduce transistor count) logic gates, which show better static and dynamic performance, tend to be the most

reliable logic gates for building combinational or sequential circuits. Therefore, the BBC blocks are desired to be capable of NAND and INV implementation.

Figure 5.2 depicts a sample BBC consisting of 4 load and 8 drive p-type transistors, arranged in 4-4-4 (drive1-load-drive2) fashion. Drive transistors are separated into two groups, and each group is dedicated for building Inverters and NAND2 gates, depending on the dimensions. This is a generic figure, showing the concept of OTFT arrangement in BBC, and the details about the transistors' dimension and layout is not given.

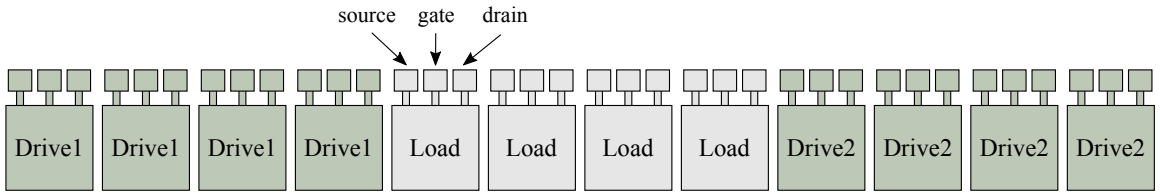


Fig. 5.2 Abstract view of a BBC block with 4-4-4 (drive1-load-drive2) arrangement

5.1.2 Wire cell

Wire Cell (WC) is a grid of uncommitted interconnections and vias that are designed for connecting the transistors and cells together. Typically, most of the fabrication or printing technologies in organic electronics are restricted to two or three metal layers. This makes it complex to design the IGA in sea-of-gates (channel-less) fashion, where the wiring connections pass over the transistors. Therefore, a set of pre-defined channels at the top and bottom of every BBC block are devoted for WC, in a similar style as channeled gate arrays.

Wire cell is made of two horizontal and vertical metal tracks, forming a grid of interconnections. Vertical tracks are pre-connected to gate, drain and source electrodes of each transistor in BBC blocks, and are isolated from horizontal one by means of dielectric layer(s). Any desired connectivity between the transistors´ electrodes to other ones (either intra-BBC, or inter-BBC) can be realized by connecting the corresponding vertical wire to a horizontal one, through the via opening at their intersection. The proposed structure for this interconnection method is introduced and explained in details in Section 5.2. The basic structure of the WC consists of two type of horizontal track: (1) Local wires, (2) Global wires.

1. *Local wires:* As mentioned before, BBC blocks are aimed to realize elementary logic gates such as Inverters and NAND gates. Local Wires (LW) are the short

horizontal metallic tracks distributed with the same length as BBC. Thus, they are designed to connect the intra-BBC transistors to build those elementary logic gates. The number of LWs depends strongly on the number of transistors in each BBC, as well as the combination of drive and load arrangement. It should also be selected in respect to the technology yield. The lower the yield, the fewer they should be.

2. *Global wires:* When the basic logic gates are made inside the BBCs, now it is time to connect them together to build more complex circuit. Global Wires (GW) are the long horizontal metallic tracks (same layer as LW), which are distributed in parallel with LWs, and aim to connect the inter-BBC logic gates together. The selection of the number of GWs in each wire channel depends on the complexity of IGA structure (how many BBCs are located in each row). The more BBCs in a row, the more GWs in a wire channel. The length of the GWs depends directly on the IGA size (complexity), which means as the IGA is bigger in respect to the number of BBCs in a row, the GW length is longer so to be capable of connecting any signal from any part of the BBCs together.

Due to the fact that the connection density is usually higher at the middle of the gate array, the wire cells located at the middle have more number of local and global connections, comparing with bottom and top wire cells. Figure 5.3 depicts a sample wire cell consisting of 5 local and 3 global wire tracks for two corresponding BBC blocks, as well as V_{DD}, and ground power rails. In the previous section the BBC had (4-4-4) combination of drive1-load-drive2, but here the BBC is scaled down to 2-2-2 for better fitting and visibility.

5.1.3 Inter-channel wire cell

Local and global wire cells are used for interconnections between the transistors and gates in one row of BBC channel. However, IGA structure is built of several row of channels, and the interconnection between those channels, and also core-to-pads, are realized by means of Inter-channel Wire Cell (IWC) blocks. This block has the same structure as the wire cells (grid of horizontal and vertical metal tracks), except that there is no local and global wires. IWC blocks are located around the core of IGA between the channels and the I/O pads. The number of horizontal track should be similar to the sum of local and global wire tracks, in order to be capable of connecting each of these tracks to a desired one in another row.

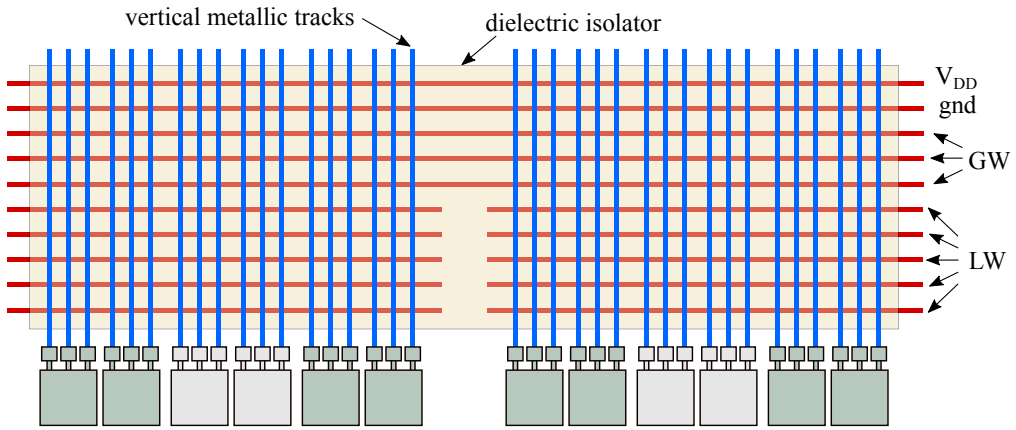


Fig. 5.3 General illustration of wire cell, consisting 5 local, and 3 global wires, plus 2 power rails for 2 consecutive BBC blocks

5.1.4 I/O pads and power rails

Similar to any conventional silicon-based gate array, the IGA structure has a uniform array of I/O signal pads and power rails (V_{DD}, GND) that are surrounding the core (in a core-limited strategy). Connections between pads and inter-cell connections are also configurable. Since the power rails are long rings of metallic tracks and they drive more current than each individual wire inside the IGA core, they are typically wider than the others.

5.2 Second step: IGA metallization

In the second manufacturing step (metallization) of the proposed IGA methodology, every individual master foil can be customized to a unique functionality by adding a final metal layer on top of the bulk structure. This metal layer, which will be printed on wire channels, interconnects the basic devices to build complex circuits. The main difference between the conventional gate arrays, and the proposed IGA is in this step, through the best use of digital direct-write on-demand printing technique, instead of preparing a new mask for customizing the foils to every individual functionality.

Functional materials are deposited onto wire cells, using patterns defined by Electronic Design Automation (EDA) tools, enabling cost-effective and rapid prototyping of several geometries rather than mask-based processes which require complex processing steps (such as photolithography-metallization, fuses, dual-gate devices, and etc.). Material loss is minimal due to additive manufacturing and no functional materials

have to be removed as in mask-based processes. Using additive digital printing gives further flexibility to the interconnection process by enabling individual chip-by-chip personalization and design changes at the last stage of the production chain.

Printing one metal layer requires much simpler process than building the complete OTFT structure with several layers of different materials. Digital mask-less printing techniques are the best candidates for customization since they allow low-cost, quick, and accurate placement of functional wires. It also allows users to customize their IGA sufficiently "at home", adding the field-configurability feature to gate arrays.

Figure 5.4 shows the simple process flow of using desktop digital printer to customize several IGA master foils to different functionalities.

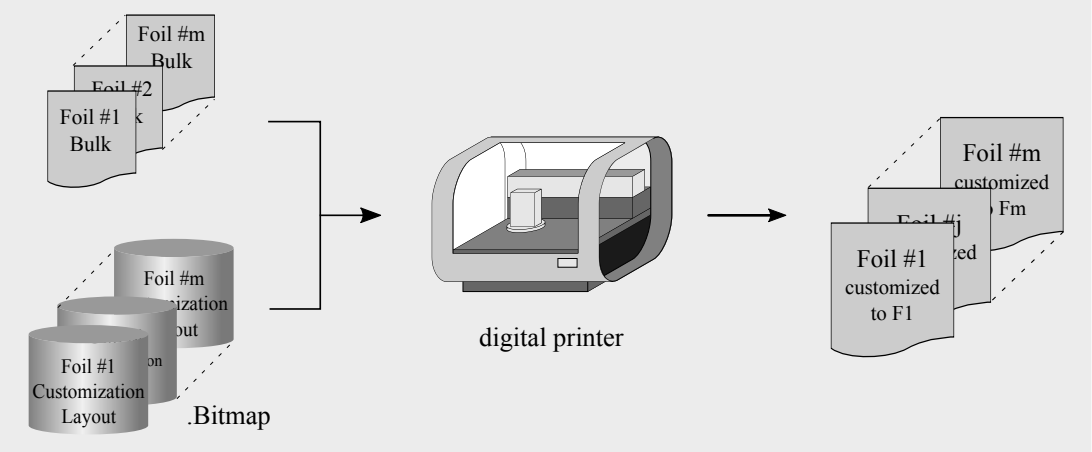


Fig. 5.4 IGA metallization flow by using desktop digital printer

5.2.1 DoD Interconnection methodologies

According to the trend towards steady miniaturization and enhanced complexity as predicted by Moore´s law, it is desired to optimize the wiring structure of the IGAs, to achieve a sufficiently high integration density at a suitable operating frequency for applications. At the same time metallization yield and material waste reduction must also be improved to make the approach commercially viable. Low-resistive and reliable wiring of the pre-defined master foils would eventually lead to robust complex digital circuits.

In order to increase the wiring density, several design and technological approaches, such as FPGAs or sea-of-gates methodology, use regular structures together with complex wiring by increasing number of metal wiring layers or reducing their dimensions. Each of these approaches possesses inherent challenges and limitations. Shrinking

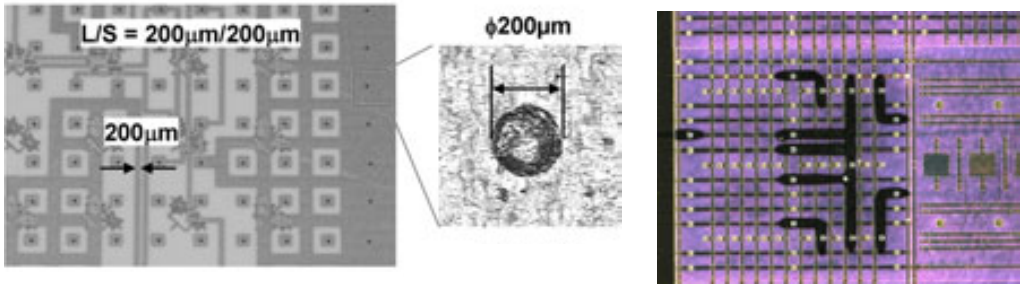
down the metal line width and space reduces conductance of connections and thus increases wire delay. Adding wiring layers is a straightforward means of providing greater function density per circuit. However, added layers invariably translate to added cost. It is therefore imperative to make the most efficient use of real estate used for wiring in order to keep the number of wiring layers to a minimum.

Moreover, the IGA master foils usually take the advantage of high-resolution photolithography technique with minimum feature sizes around few microns ($< 10\mu m$). Since the wiring cells also follow the geometrical design rules similar to OTFTs, the overall dimensions of the WC blocks are proportional to BBC blocks. On the other hand, most of the digital additive deposition technologies have lower density/resolution and often suffer from higher process variability for small feature sizes. Therefore, there is a large undesired gap between the resolution of photolithographic IGA master foils and the metallization wires printed by digital printing techniques, especially for conventional inkjet ($20 - 50\mu m$ in the best conditions). This gap and also the process variability of digital printers can cause low customization yield at circuit level, as a result of undesired electrical shorts or open circuits when printed onto the photolithographic patterned wiring cells.

Therefore, in order to improve the yield, people usually scarifies the first high-resolution fabrication step, and design transistor or logic arrays with larger separation, in order to make it compatible with low-resolution metallization printing technique. In the state of the art, inkjet has been used for customization of programmable circuits and memories, such as, UCLP [27], PAL [204], and P2ROM [202].

In the aforementioned configurable arrays, wiring metallization step is realized by printing conductive interconnects using inkjet, shown in Figure 5.5 (Source: [27], [204]). Inkjet wires tend to be relatively large compared to the transistors dimensions that they connect. The minimum design rule for wire width and separation (W/S) in [27] is $200/200\mu m$ and in [204] is $250/250\mu m$ compared with 20 and 5 μm channel length respectively. Thus, all of those promising interconnection techniques are subjected to the low resolution of the digital printing techniques, which reduces the overall circuit density.

Taking the above-mentioned considerations (limited number of wiring layers, resolution difference, and digital printing process variability) into account, therefore, the challenge is to design a wiring cell structure so that: (1) it makes the most efficient use of real estate used for wiring in order to keep the number of wiring layers to a minimum (2) it would be as much as possible compatible with metallization techniques



(a) UCLP (b) PAL

Fig. 5.5 Photographs of the inkjet-printed interconnects

resolution, and (3) the process variation of digital printing affects customization step less.

The novel approach described in this thesis permits the increase of functionality, efficiency and density in printed circuits (although it is also applicable to integrated circuit). It is the development of a reliable interconnection based on building a metallic via using drop-on-demand printing technologies. These via structures are selective interconnecting structure that can be viewed as a DoD metallization step for IGA. I am proposing two wiring methodologies: (1) line-configurable wire cell, and (2) drop-configurable wire cell, to attain the previously-mentioned requirements of wiring cell.

I. Line-configurable wires cell

The first design methodology is based on printing fine lines onto the selective uncommitted IGA wire cells, in order to form an electrical connection. For IGA metallization by using this method, short lines are required to interconnect the terminals of the pre-defined transistors together, and build logic gates and circuits. Then, final circuit with particular functionality is implemented by printing slightly longer lines to connect the BBC block together and finally to the I/O pads [256]. The proposed connection structure is composed of two key elements: (1) the pre-defined high-resolution cross of metallic tracks with via, and (2) the final customization short track (illustrated in Figure 5.6). The interconnection formation is made of:

- A first conductive track at the bottom, with specified locations for interconnection
- An insulating layer with its via opening
- A second conductive track perpendicular to the first metal layer and adjacent to the via, with no electrical connection with the first layer.

- A square of second conductive track on top of the defined via opening, being connected to first conductive layer.
- A further optional metallic short track, when presents, will connect the line and square of the second metallic layer, thus, implement a short circuit between the first and second metallic layers.

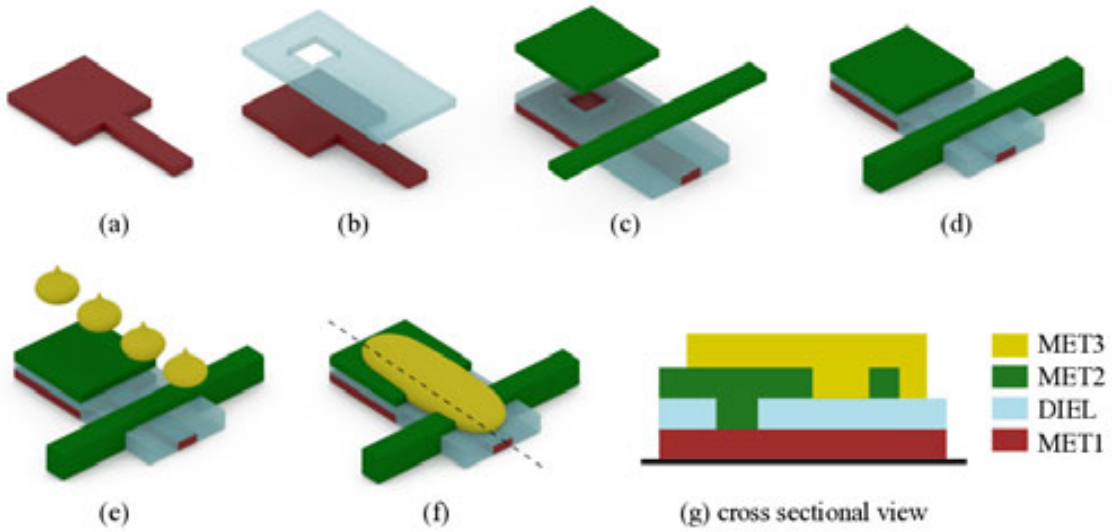


Fig. 5.6 Line-configurable interconnection structure

In order to test the functionality of this method and its applicability in IGA wire cells, test vehicles similar to the WC blocks in IGA covering all possible cases of local and global wires interconnection are designed. A systematic way of generating large amount of test vehicles has been adopted in order to generate a uniform array of same cells with different features such as line width and separation (for different metallization technologies) by using pcells and scripts.

This structure is almost generic and adoptable to any printing technology, however, it requires modifications of the stack of layers, design rules, and probably the slight changes in the layout. Since photolithography process (introduced in Section 4.2.1) with transistor channel length down to ($4\mu m$) has been used to fabricate IGA master foils, the test vehicles are also designed to be manufactured by this technology. The fabrication process consists of photolithography of Au for two metallic layers, and two passivation layers coated and patterned to allow Via formation between metals for later wiring. These test vehicles are aimed to be metallized by digital printing techniques to check their feasibility for IGA metallization. The structure is made of:

- Parallel horizontal (MET1) wires, connected to pads at the bottom of the structure (these wires are aimed to interconnect the OTFT terminals to build circuits.)
- Two passivation layers of Polivinylalcohol and SU8 (crosslinked) in order to isolate Au (MET1) from upper metal layer.
- Via (passivation opening) of $10\mu m^2, and 16\mu m^2$ on certain places on MET1 wires, adjacent to expected location of the next metal.
- Parallel vertical (MET2) wires, crossing over (but isolated) MET1 lines, connected to upper pads (these wires are expected to be connected to OTFT terminals in IGA topology).
- Squares of MET2 on top of via opening, being connected to MET1 through the vias.
- Final SU8 passivation layer, which works as an encapsulation layer on top of all devices and cells.
- SU8 via openings for final metallization.

In order to implement the connection between bottom pads (B_i) and top pads (T_i), a final metallization (MET3) track is needed to short circuit MET2 vertical wires with their adjacent squares. MET1 to MET2 connection is realized through the square via. Figure 5.7 shows the schematic of the proposed test vehicles before and after metallization. For better illustration of the test vehicles, the final SU8 passivation layer is not shown.

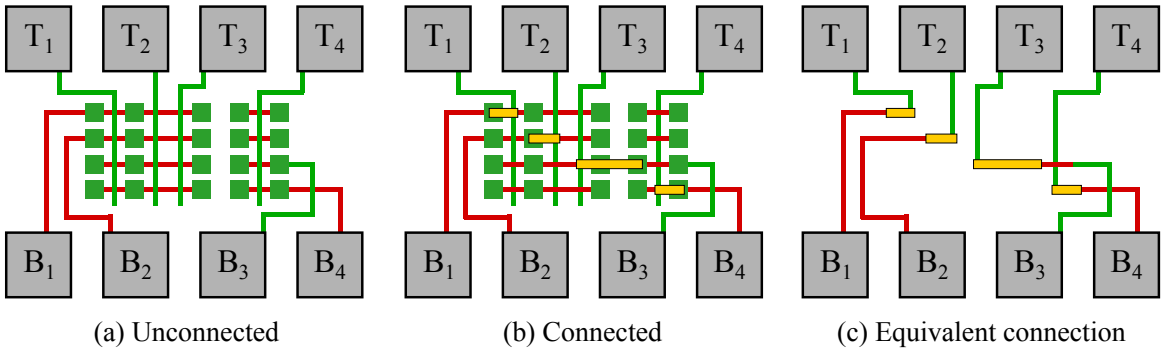


Fig. 5.7 Test vehicles for line-configurable interconnection structure

Several arrays of test vehicles were designed and manufactured for different metallization resolution in respect to printed line width and separation. Figure 5.8 shows

a zoomed-in section of the metallized test vehicle with its design parameters. MET3 line width (W) can change from $6\mu m$ for modern digital printers (SIJ) to $50\mu m$ for conventional inkjet printer. its length (L) should be as sufficient as to connect the via opening to the corresponding vertical MET2 line, and it should not be too large to make undesired short circuit with the next vertical MET2 line. Due to the structure of this methodology, the case of printing two parallel MET3 only happens in a situation when the corresponding MET1 lines should be connected to a common MET2 line, for example, two parallel MET3 lines connecting H1 and H2 to V1 means H1, H2, and V1 are connected together. Thus there is no need to take the minimum separation of MET3 line into account. Consequently, the minimum value of parameter (S) is defined by two factors: (1) the spacing design rule for MET2 in photolithographic process, (2) if the width of MET3 (W) is larger than the square via (in this case $25\mu m$), which is the case for inkjet printing for example.

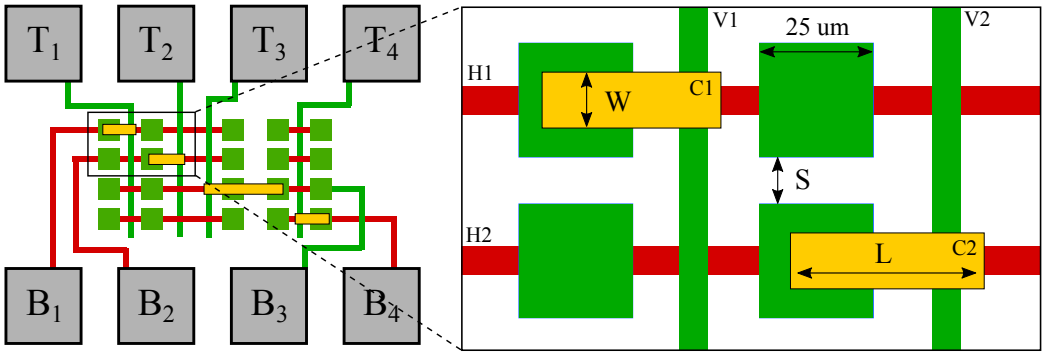


Fig. 5.8 The design parameters of the line-configurable wiring test vehicle

The key drawback of this methodology is the need to print long wires, which can vary between tens of microns (e.g. $30 - 80\mu m$ in case of intra-BBC interconnection shown in Figure 5.7), hundreds of microns (e.g. $100 - 500\mu m$ in case of inter-BBC interconnection), up to even some millimeters (e.g. $0.1 - 2mm$ in case of core-to-pad interconnection). Although some of the digital printing techniques can print fine lines down to some few microns of width, when the desired patterns (especially fine lines) are printed onto the stack of layers with different features, the resolution and shape of the final printed line can change unpredictably. This can cause accidental electrical shorts or open circuits when printed onto the photolithographic patterned interconnection structures, and a failure of one connection might cause the entire circuit to fail.

Moreover, our experiments show that printing fine lines with inkjet printer, which is the most well-established and low-cost available technique comparing with modern ones, on top of the substrates with some layers below is very complex, and the

expected resolution and minimum width cannot be achieved. Thus, for having reliable connections, realized by inkjet-printed fine lines onto the line-configurable wire cells, the spacing of the tracks must be increased dramatically. However, by increasing the wire cells size, costs may be increased since a larger gate array area may be required for a same number of devices. That being said, there is a need to provide improvements to the wiring method.

II. Drop-configurable wires cell

The main idea to overcome the above-mentioned issue for line-configurable wire cell is to skip printing of long fine lines. Here, we are presenting a methodology, by which one can realize the selective interconnects by deposition of conductive **dots/drops** instead of printing conductive tracks, and is called Drop-configurable wiring methodology [257]. This method partially eliminates or alleviates some of the limitations of previous implementations in which the interconnections were realized by printing short or in some cases long fine tracks. It also improves the wiring density, and enables the use of several digital printing technologies, with even lower resolution for circuit customization.

The proposed connection structure is composed of two main elements: (1) the pre-defined high-resolution cross of metallic layers with a **"bank"**, and (2) the final customization drop (illustrated in Figure 5.9). The interconnection formation is made of:

- A first conductive track at the bottom
- An insulating layer with its via
- An inner area of the second conductive track covering the via and connecting with the first conductive track
- An outside ring on the same second conductive layer that does not contact the inner area of the same layer
- A further optional metallic DoD layer that, when presents, will implement a short circuit between the inner area and outer ring and thus between first and second conductive tracks.

The combination of the first metal square, via opening, the inner square and outer ring of second metal is called **bank**, which is the desired location of final DoD drop for providing the connection. Printing DoD drops on top of the second conductive surface

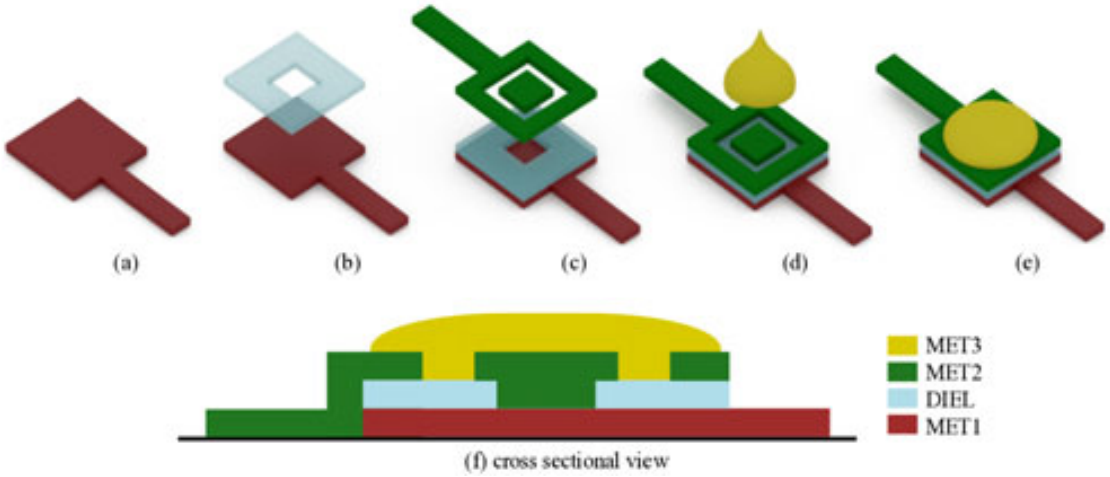


Fig. 5.9 Drop-configurable interconnection structure

showed better conductive behavior than printing it on a deep metal plus dielectric via hole. Thus, the inner square of the bank is designed to provide the connection with the first metallic layer.

In order to test the functionality of this method and its applicability in IGA wire cells, test vehicles similar to the WC blocks in IGA are designed. A systematic way of generating large amount of test vehicles has been adopted in order to generate a uniform array of same cells with different features such as bank width and separation (for different metallization technologies) by using pcells and scripts.

Similar to line-configurable methodology, this structure is generic and adoptable to any printing technology, however, it requires modifications of the stack of layers, design rules, and probably the slight changes in the layout. Since photolithography process (introduced in Section 4.2.1) with transistor channel length down to ($4\mu m$) has been used to fabricate IGA master foils, the test vehicles are also designed to be manufactured by this technology. The fabrication process consists of photolithography of Au for two metallic layers, and two passivation layers coated and patterned to allow via formation between metals for later wiring. These test vehicles are aimed to be metallized by digital printing techniques to check their feasibility for IGA metallization. The structure is made of:

- Parallel horizontal (MET1) wires, connected to pads at the bottom of the structure (these wires are aimed to interconnect the OTFT terminals to build circuits.)

- MET1 squares on top of the horizontal lines, forming the first layer of the bank.

- Two passivation layers of Polivinylalcohol and SU8 (crosslinked) in order to isolate Au (MET1) from upper metal layer.
- Via (passivation opening) of 10 m^2 and 16 m^2 on top of the MET1 squares.
- Squares of MET2 on top of the via openings, forming the inner area of the bank, and making the connection with MET1
- Parallel vertical (MET2) structures forming the outer ring of the bank.
- MET1 wires, connecting the upper bank of each column to the pads at the top of the structure.
- Final SU8 passivation layer, which works as an encapsulation layer on top of all devices and cells.
- SU8 via openings on top of the banks for final metallization.

In order to improve the density of structure (less separation of MET1 horizontal wires), banks are placed in a Zig-Zag fashion. Connection between bottom pads (B_i) and top pads (T_i), are implemented by printing a final drop of MET3 to short circuit the inner and outer shapes of the MET2 on the banks. Figure 5.10 shows the schematic of the proposed test vehicles before and after metallization. For the same reason as before, SU8 passivation layer and its openings are not shown in this figure.

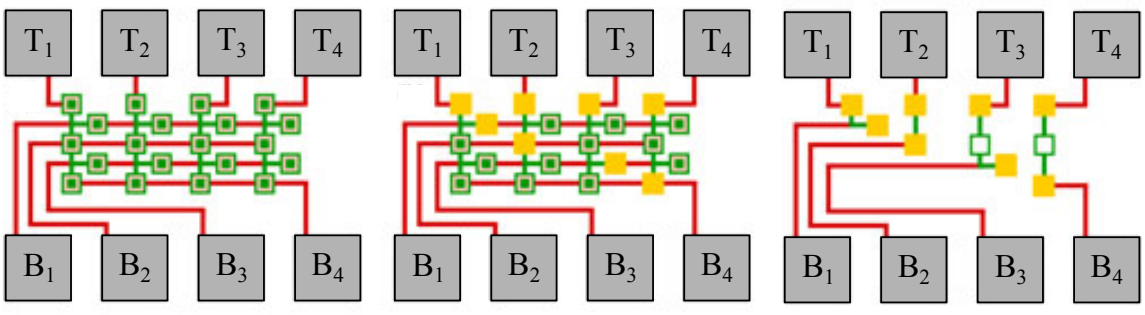


Fig. 5.10 Test vehicles for drop-configurable interconnection structure

Several arrays of test vehicles were designed and manufactured for different metallization resolution in respect to the bank width and separation. Figure 5.11 shows a zoomed-in section of the metallized test vehicle with its design parameters. For bank width, the minimum possible value (W_{min}) is limited by the photolithography design

rules. The minimum width of the via openings for passivation layers are 10 and 16 m, and the width of inner MET2 square should respect the minimum overlap of MET2 layer with passivation. Thus, the width of inner MET2 square is set to $W_{\text{inner-MET2}} = 22\ m$. Besides, in order not to cause any unexpected short circuit between this square and the outer MET2 ring, the minimum MET2 separation ($S_{\text{MET2}} = 5\ m$) should be respected, and eventually the outer ring needs to have the minimum MET2 width ($W_{\text{MET2}} = 9\ m$). Taking all these rules into account the minimum bank width can be calculated as:

$$W_{\text{min}} = W_{\text{inner-MET2}} + 2\,S_{\text{MET2}} + 2\,W_{\text{MET2}} \qquad W_{\text{min}} = 22 + 10 + 18 = 50\ m \quad (5.1)$$

Thus, the designed range of bank width in the test vehicle array was: ($W = 50\ 60\ 70\ m$). Regarding the minimum separation, the range is ($S = 30\ 40\ 50\ m$), and the aim is to maximize the circuit density as much as possible.

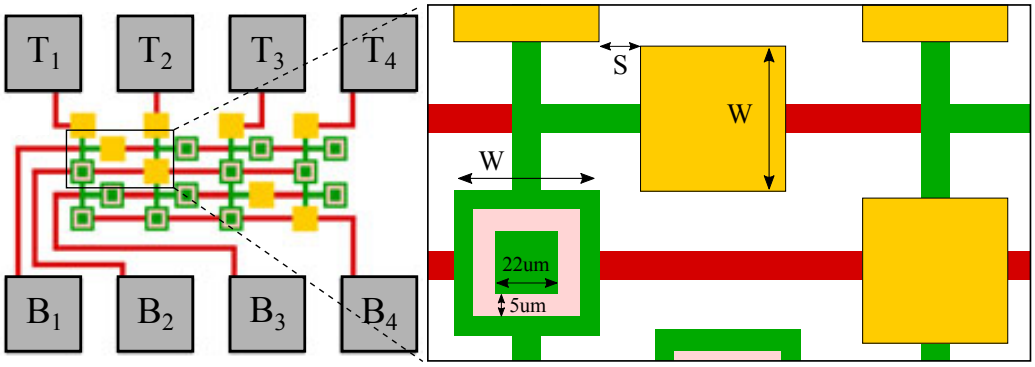


Fig. 5.11 The design parameters of the drop-configurable wiring test vehicle

Additionally, a second test vehicle, called “via chain”, has been designed in order to check the repeatability of the connection banks. In this test vehicle, the width and space of the connection banks are kept constant (W=70 µm, S=50 µm), and a variable number of via banks (2, 4, 8, 16, 32) have been placed between two pads. The aim is to check the resistance between two pads after wiring the banks, in order to calculate the resistance per wired-bank accurately with the variability given by the DoD printing process. The layout of unwired and wired test vehicles including 8 banks between two pads are shown in Figure 5.12.

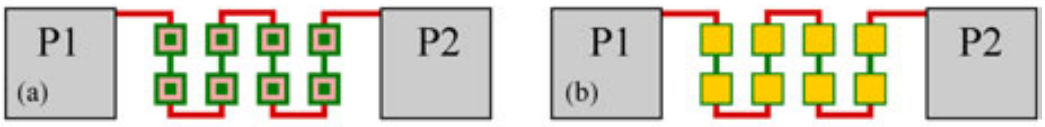


Fig. 5.12 Via chain test vehicles for drop-configurable structure

5.2.2 Metallization techniques

Several conventional and modern digital printing techniques for metallization of the proposed test vehicles, and consequently IGAs, can be employed, and in this thesis inkjet printing (IJP), aerosol jet (AJ), superfine inkjet (SIJ), and electrohydrodynamic (EHD) techniques were used. Brief introduction to each of these printing techniques are given in Section (3.3). The DoD wiring methodologies, their corresponding test vehicles, and IGAs using this interconnection styles have been designed in different periods of the thesis, and therefore, not all of the digital printing techniques were available at each moment. Table 5.1 shows the available and used printing techniques for the DoD wiring methodologies.

Table 5.1 Available metallization techniques

Test vehicle	SIJ	AJ	IJP	EHD
Line-configurable			x	x
Drop-configurable		x		

Figure 5.13 shows the fabricated samples of different test vehicles for line-configurable, and drop-configurable structures. For the line-configurable structure, the wiring width can be up to $W = 25\ \ m$, and for drop-configurable ones, the drop width and separation is ($W = 70\ \ m\ \ S = 50\ \ m$) in this image. The via chain test vehicles is made of 8 consecutive banks.

Superfine Inkjet (SIJ)

In order to reach the highest IGA wiring density, its customization should use fine lines with smallest possible width. Thus, the goal is to print lines with the minimum possible width so that they will not limit the transistor density of the circuit (lowest wiring cost). Wiring lines should not extend out of their assigned location in the test vehicles. In order to obtain the minimum printable width with high yield, and also to check the usability and reproducibility of the technology, different line widths have been selected (6 m 12 m and 20 m).

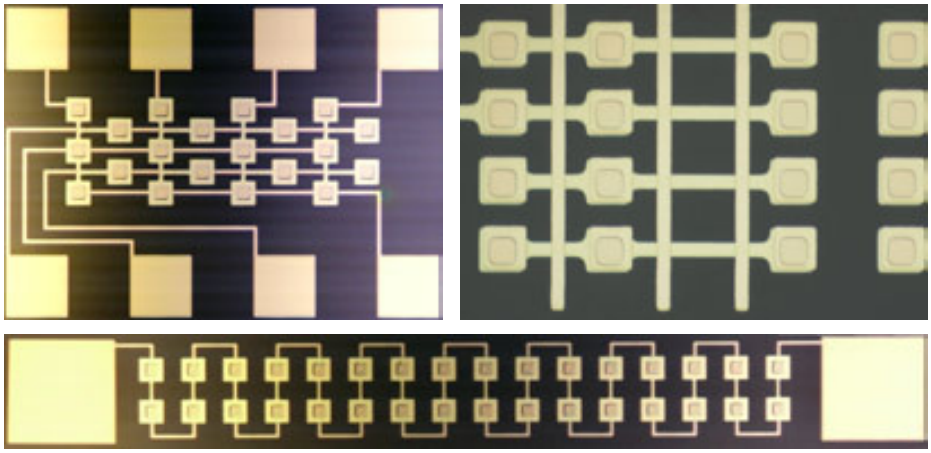


Fig. 5.13 Fabricated samples of test vehicles

The input printing pattern for SIJ machinery is a simple text file in which the start and end coordinates of each line with a complementary code corresponding to its desired width are written (e.g. “1”: 6um, “2”: 12um, and “3”: 20um). Each code represents a specific set of parameter values which produce the desired line width. The parameters relate to the strength, waveform and frequency of the oscillating voltage between the grounded printing plate and the ink meniscus at the tip of the nozzle.

The oscillating voltage determines the strength of the electric field, which determines the size of the ink droplets. This means that the electrical parameters of the substrate material, especially conductivity, will also affect the size of the ejected droplet. Specifically, if the substrate material is non-conductive, charge accumulation at the substrate surface occurs during printing. In case of unipolar waveform, the charge accumulation will decrease the effective electric field at the meniscus leading to smaller droplet size [258], [259].

Before carrying out the printing trials the substrate surface was cleaned and activated using 10 minutes of oxygen plasma cleaning with O_2 flow of 2 sccm, pressure of 100 mTorr and RF power of 100 W. The purpose of the surface treatment is not only to clean the surface from possible contaminants, but also to activate it. The activation makes the wetting properties of the surface more uniform and leads to more uniform conductors.

For metallization of line-configurable test vehicles, silver nanoparticle ink NPS-J, product of Harima Chemical Group, Inc. was chosen. The ink parameters are given in Table 5.2 (Source: [260]).

In order to find the suitable parameter values, a calibration print run must be done for each desired line width. After the calibration, the actual conductors can be printed.

Table 5.2 Harima NPS-J ink parameters

Parameters	Value
Particle size	$\approx 12nm$
Solid content	65 wt%
Sintering condition	220℃for 60 min
Resistivity	$3\mu\Omega cm$
Solvent	Cyclododecene

The calibrated parameters for each line width are given in Table 5.3. The layer count for each individual conductor was five. Based on the desired line widths, the chosen nozzle type was the Standard Nozzle. In order to make the conductors sufficiently thick, multiple layers have to be printed. In this case, we used 5 layers for all three cases.

Table 5.3 Calibrated parameters for different line widths

$Width(\mu m)$	$V_{\text{bias}}(V)$	$V_{\text{max}}(V)$	Wave form	Frequency (Hz)
6	200	250	Sinusoidal	700
12	200	257	Sinusoidal	700
20	200	263	Sinusoidal	700

The main challenge in printing on this substrate was the limited space for process optimization. When the edge between dielectric and metal surface is very sharp, an open circuit might appear since the ink is not able to wet the edge properly. This is especially important in case of narrow conductors since they are also the thinnest. The issue could be remedied by optimizing the layer count for the narrowest conductors. Another issue is that the jetting depends on the conductivity of the substrate material (see above). This means that the change from metallic to dielectric surface might affect the size of the generated droplet and thus the uniformity of the resulting conductor.

However, even further optimizations cannot overcome some of the anomalies. Looking at the spreading of the ink, it depends heavily on the surface material. Since a single print covers both dielectric and metallic surface with distinct wetting properties, the resulting conductor will always have two distinct line widths. This can be seen as the bulging/narrowing of conductors at the interface of two materials. This problem can be solved by using surface pretreatments for substrate surface energy control [261]–[263].

Figure 5.14 shows the SIJ-wired line-configurable test vehicles, using three different wiring width ($W = 6, 12, 20\mu m$)

For drop-configurable metallization, ULVAC Au-ink was chosen as the best candidate for the printing tests due to its high boiling point solvent (Cyclododecene, T_{boil}=232℃)

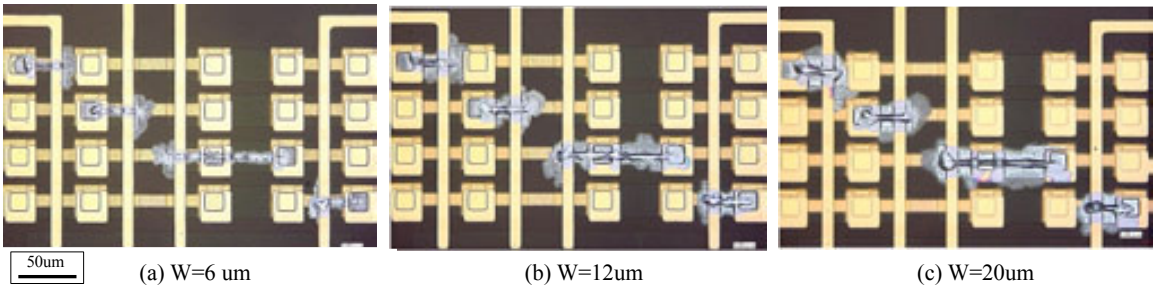


Fig. 5.14 SIJ-wired line-configurable test vehicles

which leads to slow solvent evaporation rate at the nozzle tip and reduced possibility of clogged nozzle due to drying up of the ink. The material and processing parameters of the ink are given in Table 5.4 (Source: [264]).

Table 5.4 ULVAC AU-ink parameters

Parameters	Value
Solid content	$50wt\%$
Sintering condition	250°Cfor 60 min
Resistivity	$8\mu\Omega cm$
Solvent	Cyclododecene

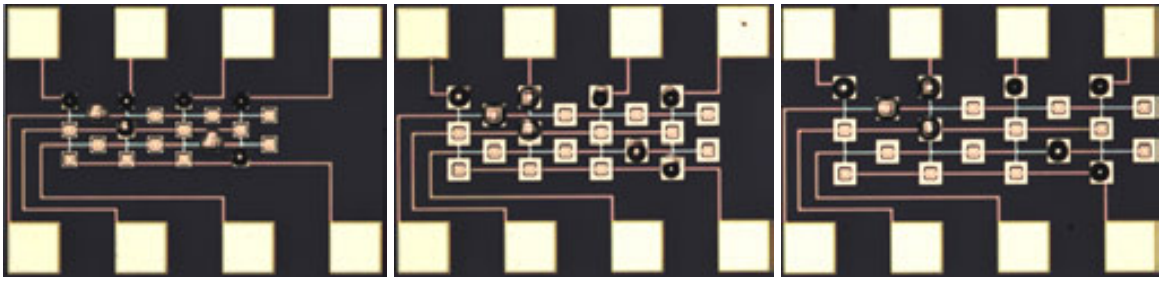
Printing of the MET3 interconnects was accomplished by using a bumping mode whereby each bank is filled with multiple ink layers consisting of numerous sub-picoliter sized droplets. The number of layers, the number and volume of the droplets in each layer and the idle time between the subsequent layers determine the volume and spreading of the bump. The latter affects especially the spreading of the ink since it determines how much of the solvent will evaporate between printing of the layers. If the spreading is not enough, the MET2 ring might not wet properly leading to open circuit whereas too large spreading might cause short circuits between subsequent bank. In this case the optimal results were achieved using the print parameters given in Table 5.5.

Bipolar jetting voltage ($V_{\text{bias}} = 0V$) was chosen to prevent possible charge accumulation on the surface, which might cause print artifacts such as droplet deflection [265]. Because of this, the droplet ejection frequency is twice the voltage frequency (i.e. 140 Hz instead of 70 Hz); with 0.4 second holding time the resulting droplet number per layer will be 56. It must be noted here, that the V_{max} had to be decreased during the printing, as there was a tendency for the bumps to spread more as the printing preceded.

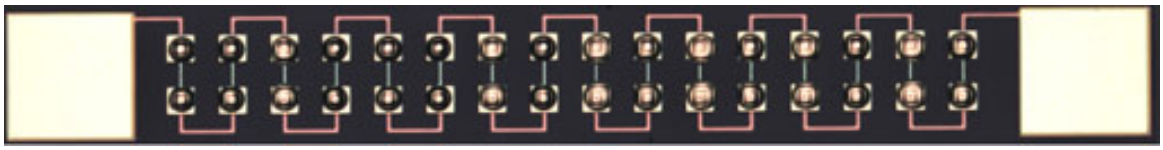
Table 5.5 Print parameters for SIJ bumping

Parameters	Value
Waveform	Sine wave
$V_{\max}$	450 to 460 V
V_{bias}	0 V
Voltage frequency	70 KHz
Holding time per layer	0.4 sec
Idle time between layers	1.2 sec
Number of layers per bump	40

Figure 5.15 shows the both SIJ-wired drop-configurable test vehicles for different bank width and spacing, and 32 number of banks in the chain.



(a) W=50um, S=30um (b) W=70um, S=30um (c) W=70um, S=50um



(d) 32 serial bank-chain

Fig. 5.15 SIJ-wired drop-configurable test vehicles

Aerosol jet (AJ)

AJ printing employs a continuous ink flow system as opposed to DoD systems that eject discrete drops of a specific volume through a piezo-driven print-head. Furthermore, unlike DoD systems AJ printed track widths are a function of process gas/exhaust flow. Therefore, by tuning the gas flows manually the operator can adjust the properties of the aerosol jet beam.

AJ printing can also be influenced by surface energy in the same way as conventional inkjet, especially for low viscosity liquids. Higher viscosity pastes can be printed by AJ and these can be less susceptible to movement due to differences in surface energy, which is a crucial factor in how ink wets, and determines how receptive the surface is

to the ink. Initial printing trials yielded poor wetting characteristics on the substrate surface.

Thus, a 30 second O_2 plasma treatment with a 50 sccm gas flow rate at 70W forward power was used to significantly change the surface energy, making the substrate surface more receptive to the printed ink. The printing process was manually tuned to produce the most uniform printing possible; process and exhaust flows were equilibrated within 10% pressure tolerance. The ink used for these trials was Cabot®CSD-32 Ag nano-dispersion.

A fundamental limitation of the AJ printing technique became apparent when printing tracks $< 100\mu m$ in length. The AJ printed tracks demonstrated a characteristic bulge at the beginning and end of the track. Due to the short line lengths required, the bulged regions coalesced to form a droplet rather than a track, therefore significantly reducing the definition of the printed feature.

The narrowest possible line width of $15\mu m$ has been obtained, and also for wider lines, the bulge characteristic at the beginning and the end of the lines caused short circuit with adjacent wires. For this reason, with the current setup, $15\mu m$ line width is expected to offer the highest yield.

Figure 5.16 shows some wires printed by AJ, onto the test vehicles. Although the ink is spreading on the right side of the longest printed line, it does not make any unnecessary short circuit between two adjacent pads, because the ink spread does not reach to the next vertical Met2 line.

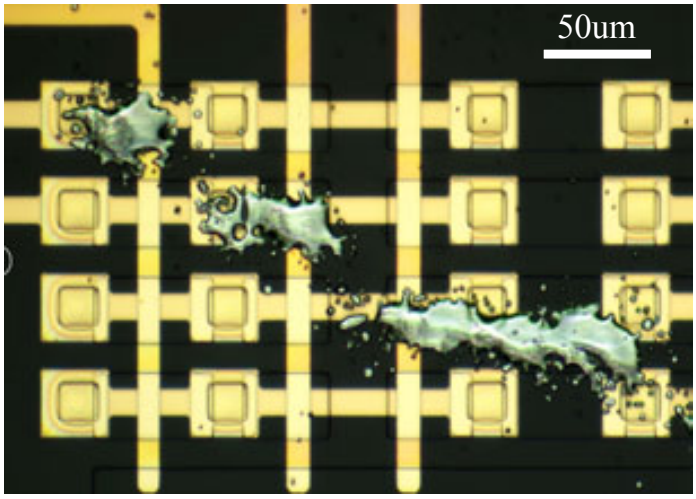


Fig. 5.16 AJ-wired line-configurable test vehicles

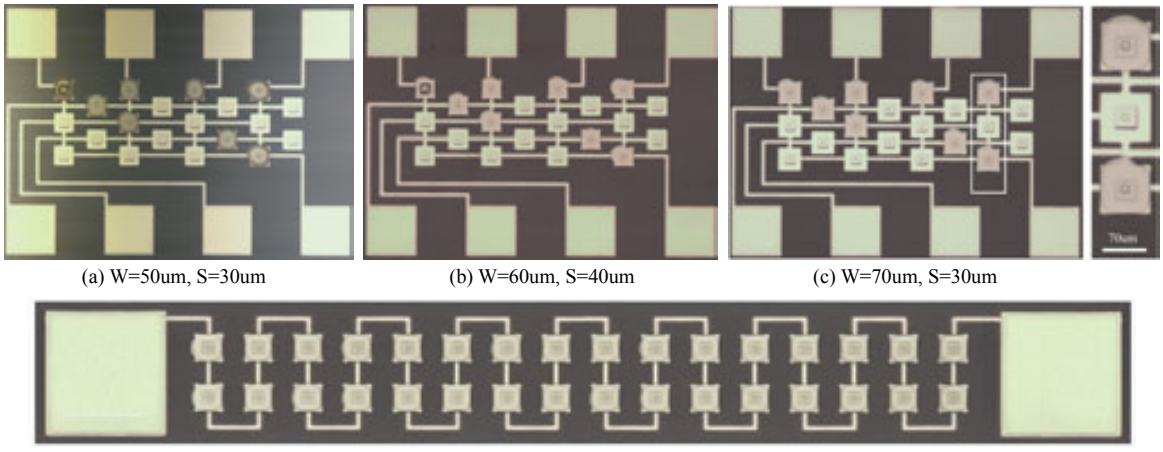
Due to the limitations of AJ system for printing small and discrete drops, this printing technique was not used for wiring the drop-configurable test vehicles.

Inkjet printing (IJP)

Due to the challenges for wiring the line-configurable structures (e.g, low resolution, statistical variability provided by fluid-based piezoelectric deposition technologies, and unpredictable printed shapes onto the stack of layers with different features), IJP offered a very low yield for wiring this structure. Thus, only drop-configurable methodology has been metallized by IJP, since it is more adoptable and reduces the risk of such faults.

Dimatix DMP2831 printer was used to jet a conductive silver ink (Silverjet DGP-40LT-15C) through a 10pL nozzle print head. The substrate was heated to 60°Cduring printing and following printing the ink was cured at 115°Cfor 60 minutes.

Each printed connection consisted of a single pixel 10pL droplet therefore any misdirected nozzle would result in a circuit failure. This was mitigated by inserting a leader pattern into the design. The leader pattern allowed the jetting to stabilise before the pattern was printed. This consisted of a series of 1 pixel drops located in an unobtrusive section of the substrate. Figure 5.17 shows the both IJP-wired drop-configurable test vehicles for different bank width and spacing, and 32 number of banks in the chain.



(a) W=50um, S=30um (b) W=60um, S=40um (c) W=70um, S=30um

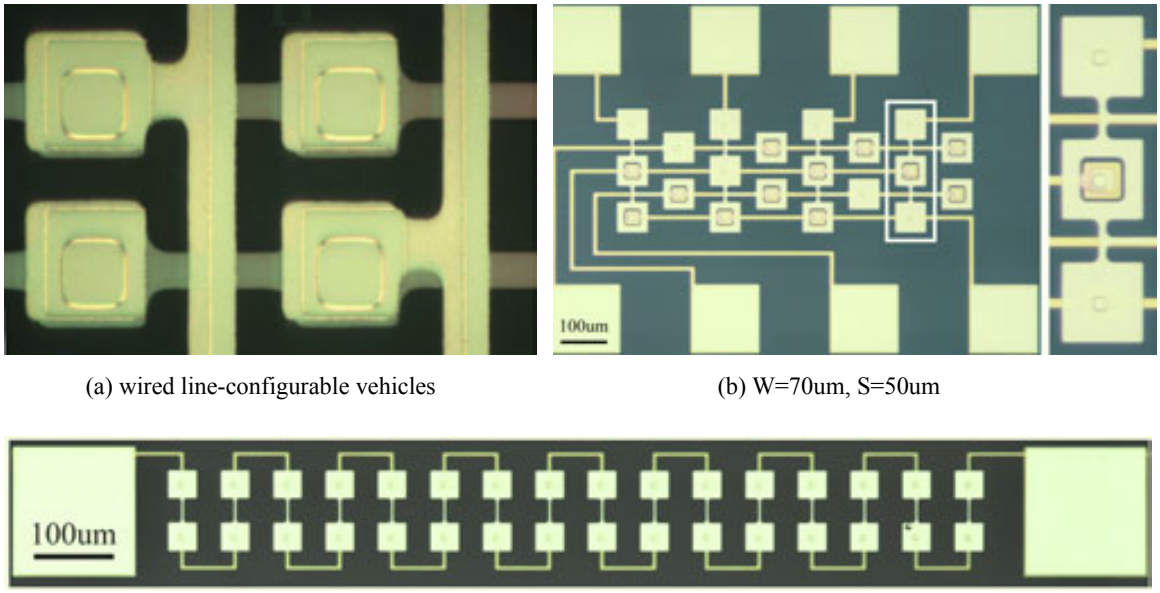
(d) 32 serial bank-chain

Fig. 5.17 IJP-wired drop-configurable test vehicles

Photolithography (PH)

The test vehicles for line-configurable and drop-configurable structures have been also wired by using photolithography technology, similar to the one by which test vehicles were fabricated. A new mask for MET3 were designed, patterned, and fabricated

onto the test structures by the same gold material layer. As expected, very fine and accurate connections have been build (shown in Figure 5.18). The photolithographic metallization of line-configurable test vehicles are not very clear, since the lines (MET3) are printed by using the same gold material as (MET2). For this reason, the image is zoomed-in in Figure 5.18 (a). Due to the high accuracy, and reliability of all the wired test vehicles, only one sample for each test vehicle is shown as a proof of concept.



(a) wired line-configurable vehicles

(b) W=70um, S=50um

(d) 32 serial bank-chain

Fig. 5.18 Photolithographic-wired test vehicles

5.2.3 Results and comparison

Both types of wiring methodologies and their metallized test vehicles have been characterized to check repeatability, reliability, resistivity, and yield. Finally the result of the digital printing techniques have been compared with photolithography ones in order to obtain the most reliable wiring methodology and its corresponding technique. While characterizing the structures, two issues have been considered as the yield criteria: hard faults and soft faults.

Line-configurable metallization

In order to check the true connectivity of the desired interconnections, pad-to-pad resistance of 8 test vehicles (32 connections) for each printed technology has been

measured by LCR meter. It has to be taken into account that the measured values are the resistances between top and bottom pads (T_i,B_i), which is accumulation of three resistances:

- Resistance of the MET1 and MET2 wires connecting to the pads (R_M)
- Resistance of the via made of MET1, MET2, (and MET3) (R_V)
- The contact resistance of the final printed lines (R_C)

$$R_T = R_M + R_V + R_C \tag{5.2}$$

where R_T is the total measured pad-to-pad resistance, and it is desired to extract the value of R_C from 5.2.

Failures in printing can happen during the metallization process due to some physical phenomena (misalignment, unexpected drops, nozzle break down, and etc.). These failures, known as hard faults, cause undesired open or short circuit, and let the entire connection to fail. Thus, the resistance between two pads (T_i,B_i) can be "zero" or some Kilo or Mega Ohms.

Furthermore, due to the variations in the width, length and thickness of the printing lines (soft faults), the measured pad-to-pad resistance is not equal for all similar cases. For example, the measured resistances between pads (T_1 and B_i) for two similar test vehicles are not similar. This variation is expected to be only due to the final metallization step, since the rest of the structure is fabricated through photolithography process with high accuracy.

Taking both hard faults and soft faults into account, it is desired to extract the acceptable printed line by withdrawing out-range resistance values from the samples. This was done in two steps: First, according to the statistics and expected wire resistance of each technology some extremely high values (some order of magnitudes higher than the majority of measured data) have been withdrawn from the samples and are considered as hard fault. This allows obtaining the real mean value (μ) of wiring resistance. Table 5.6 shows the number of hard faults for each technology.

Experimental results show that very narrow SIJ printed lines ($6, 12\mu m$) have low performance and very low yield and require more process development and optimization. In order to have a meaningful understanding and fair comparison of different technologies, narrow SIJ lines are not taken into account in the statistical population.

Table 5.6 Hard faults and yield for metallization of line-configurable text vehicles

Tech.	SIJ ($20\mu m$)	AJ	PH
Total samples	32	32	32
Hard faults	4	9	1
Yield_H (1−Hard-faults/Total)	88%	72%	97%

Figure 5.19 shows the histogram of the measured resistance after the first data filtering.

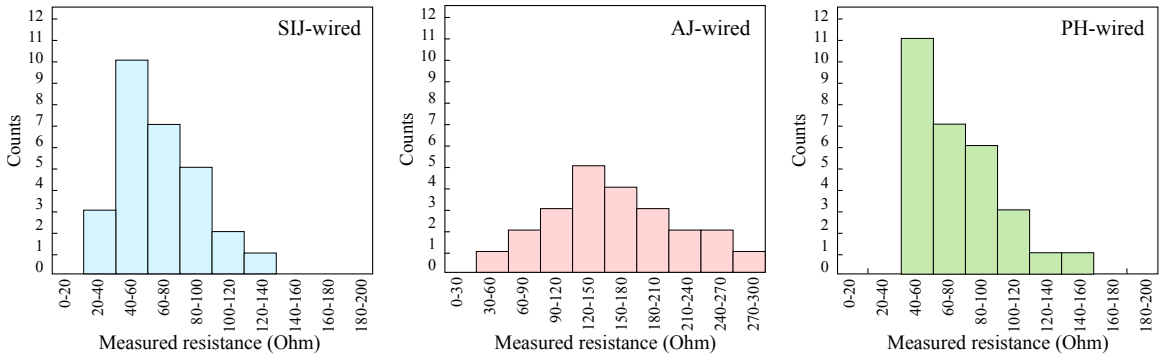


Fig. 5.19 Histogram of the measured resistance for line-configurable test vehicles

The second step for further filtering, and pulling out the samples that are heavily affected by soft faults is realized according to three-sigma rule of thumb or so-called 68-95-99-7 rule [266]. This rule expresses that nearly all of values lie within a band around the mean in a normal distribution with a width of one, two and three standard deviations, respectively. Thus, the average value (μ), and standard deviation (σ) of the measured resistances after first filtering are calculated, and $\mu \pm 3\sigma$ is chosen as the yield criteria for filtering data in respect to soft faults (shown in Table 5.7).

Table 5.7 Soft faults and yield for metallization of line-configurable text vehicles based on three-sigma rule of thumb

Tech.	SIJ ($20\mu m$)	AJ	PH
$\mu(\Omega)$	67.43	160.75	74.72
σ	22.63	61.44	26.34
$\mu \pm 3\sigma$	0-135	0-345	0-154
Total samples	28	25	31
Soft faults	0	0	0
Yield_S (1−Soft-faults/Total)	100%	100%	100%
Yield ($Yield_\text{H} \times Yield_\text{S}$)	88%	72%	97%

As expected, the photolithographically patterned lines offer the highest yield but still not 100%, which is due to the fact that the process uses contact photolithography and hence is prone to defects where the mask becomes dirty due to the contact with the sample. Cleaning the masks is not 100% effective. Variations in resistance are likely to be due to the differences in metal step coverage of the SU8 via, as well as the variable length of the connecting wires between the pads.

In order to obtain the best repeatability in SIJ, it is safer to avoid too narrow connections such as 6 and $12\mu m$ width. The thickness of the conductors also affects the yield and as mentioned earlier, the thickness was controlled by the number of printed layers. In this case, five layers were used for all three widths. Since the layer thickness depends on the layer width, same number of layers should result in conductors with different thicknesses. Using Wyko NT1100 optical profilometer, thickness was measured to be approximately $0.35\mu m$, $1\mu m$ and $1.1\mu m$ for $6\mu m$, $12\mu m$ and $20\mu m$ wide conductors, respectively. Thus, increasing the thickness of the conductor also improves the yield.

Regarding the standard deviation, a large variation is expected when via coverage is not complete, as observed with the $6\mu m$ SIJ and the $15\mu m$ AJ printed wiring. Furthermore, in AJ, the wire thickness is not uniform (it varies in the range $15-30\mu m$), which causes resistance variation as well.

Table 5.7 shows that the average resistance of SIJ and PH wired test vehicles is very close and smaller that AJ-wired ones. This is also similar for the standard deviation, which means that the soft faults (process variations) can be more effective when wiring IGAs with AJ rather than SIJ or PH. However, all the measured values (even for AJ) still fit in $\mu \pm 3\sigma$, which means soft faults are not affecting the metallization yield.

R_C has to be obtained from Equation 5.2 in order to compare and evaluate the contact resistance caused by each printing technology. For that, R_V and R_M should be calculated before. According to the previous process characterization extracted from extra test vehicles (shown in A), the resistance of every single via is measured as: ($R_V = 10\Omega$). Furthermore, R_M can be obtained by using 5.3 which is resistance of a regular three-dimensional conductor.

$$R_M = R_s.\frac{L}{W} \tag{5.3}$$

where R_s, L, and W are the sheet resistance, length and width of MET1 and MET2 layers. According to the process characterization extracted from extra test vehicles (shown in A), and also material information, sheet resistance of MET1 and MET2 layers

(with 50nm) thickness are 0.5 and 1 Ω/sq respectively. The width of all patterned lines is $9\mu m$ (minimum design rule value). Thus, R_M is different for each couple of Top-Bottom pad connections (T_i, B_i) since lengths of MET1 and MET1 wires are different. By using Equation 5.3, all R_M values for (T_i, B_i) are calculated. Afterwards, by knowing R_T, R_M, and R_V we can find R_C. Eventually, according to Equation 5.4, the sheet resistance (R_{sMET3}) of printed MET3 layer can be calculated for each (T_i, B_i).

$$R_C = R_{sMET3} \cdot \frac{L}{W_c} \tag{5.4}$$

Where W_c and L are the drawn width and measured length of the final printed MET3 layer. Table 5.8 shows the average sheet resistance of MET3 layer printed by three technologies according to its line width.

Table 5.8 Calculated average sheet resistance of digital printing technique

Tech.	SIJ	SIJ	SIJ	AJ	PH
$W_C(\mu m)$	6	12	20	15	9
$R_{sMET3}(\Omega/sq)$	26.5	2.3	1.53	19.5	1.3

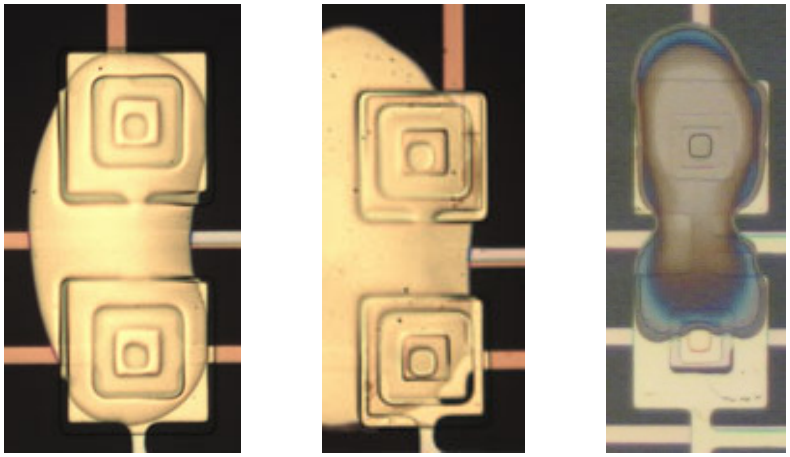
According to Table 5.8, photolithographically patterned lines have the minimum sheet resistance although they are not the widest wires. However, printing broader features risks a short between neighboring lines, requiring a new gate array wiring channel design to lower connection density.

Obviously, the sheet resistance of the SIJ printed wires decreases by increasing the wire width, and the best lines show a slightly higher sheet resistance than PH ones. Comparing to PH and wide SIJ lines, AJ has almost one order of magnitude higher sheet resistance and also experiments show that the ink spread in AJ is larger than the other techniques which might cause unexpected short circuit in several parts of the circuit.

Drop-configurable metallization

In order to extract the minimum configurable bank width and separation, the metallized wire test vehicles (both IJP and SIJ) were optically characterized. Statistical results from 2 arrays of 9 test vehicles (18 test vehicles in total) with $W = 50, 60, 70\mu m$ and $S = 30, 40, 50\mu m$ show that, the printed drops are well placed and cover the entire bank area without much extension or undesired short circuit for all cases, except $S = 30\mu m$.

When the minimum designed value for bank separation is ($S = 30\mu m$), there are 2 and 3 failures for IJP-wired, and SIJ-wired test vehicles, respectively. These failures are due to small separation of banks, which cause undesired connection between the printed drops (shown in Figure 5.20), and are considered as hard faults.



(a) SIJ (b) SIJ (c) IJP

Fig. 5.20 Occurrence of hard faults when wiring drop-configurable test vehicles for small bank separation

Regarding the bank width (W), the minimum designed value ($W = 50\mu m$) is almost the minimum possible width for patterned structure due to the photolithography design rules, and it shows almost 100% yield or better say (99.99%). Thus, $W = 50\mu m, S = 40\mu m$ can be fixed as the bank width and separation, when using this structure in IGAs wire cells.

In order to extract the contact resistance (R_C) of filled banks for each metallization technology, the pad-to-pad resistance (R_T) of four arrays of metalized via chain test vehicles were measured. Each array includes series of 2, 4, 8, 16, and 32 banks. The measured results shows that the soft faults, caused by process variation, is not as much as line-configurable structures. The reason is that the final printing layer in this methodology is not long wires, where the resistance would change dramatically depending on the width, length and thickness of the printed lines. The measured R_T is separated into two resistive components between two pads:

- Resistance of the MET1 and MET2 wires connecting to the pads (R_M)
- Contact resistance of the wired banks, multiplied by number of banks ($N.R_C$)

$$R_{\mathrm{T}} = R_{\mathrm{M}} + N.R_{\mathrm{C}} \tag{5.5}$$

where N is the number of banks in the serial chain, and $\mathrm{R_M}$ can be estimated by using the classical expression 5.3 for the resistance of a rectangular three dimensional conductor. Therefore, expressions 5.3 and 5.5 were used to calculate the contact resistance of one single SIJ-wired and IJP-wired bank, as well as PH ones. Table 5.9 shows the resistance calculations of the via chain test vehicles wired by three technologies.

Table 5.9 Resistance calculation of the wired via chain test vehicles

#Banks	R_{M}	IJP			SIJ			PH		
		R_{T}	$N.R_{\mathrm{C}}$	R_{C}	R_{T}	$N.R_{\mathrm{C}}$	R_{C}	R_{T}	$N.R_{\mathrm{C}}$	R_{C}
2	175	209	34	17	202	27	13	197	22	11
4	174	241	67	17	222	48	12	216	42	10
8	151	300	149	19	293	141	17	259	108	13
16	147	491	343	21	333	186	12	340	193	12
32	170	868	698	22	496	299	9	508	338	10

Finally, the average contact resistance per wired bank is calculated for each printing technology and shown in Table 5.10

Table 5.10 Average contact resistance per wired bank

	$R_{\mathrm{C\text{-}IJp}}$	$R_{\mathrm{C\text{-}SIJ}}$	$R_{\mathrm{C\text{-}PH}}$
Average (Ω)	19.2	12.6	11.2

The calculated average contact resistance per bank for IJP and SIJ is pretty similar to PH one, and also very close to the value provided by technology information (10Ω). Tables 5.9, 5.10 demonstrate the feasibility of digital printing techniques (either high- or low-resolution) with the proposed drop-configurable wiring methodology. Furthermore, this contact resistance value is far smaller than the "on" or "off" resistance of the transistors ($K\Omega, M\Omega$), which enables the use of digital printing techniques for wiring the unconnected array of transistors in the IGAs, with as less effect as possible on the transistor and hence the implemented circuit performance.

Comparing to line-configurable wire style, the results show that the resistance, yield, variability, and scalability of drop-configurable style is optimized a lot. Besides, the compatibility of the proposed structure with inkjet printing, as the most cost-effective

available digital printing technique, has made it the best candidate for wire channels in the IGAs. Consequently, most of the IGAs designed for photolithography technology (presented in the next section) use drop-configurable wiring methodology.

5.3 IGA for functionality personalization

The first and most important feature to address about IGA is the hybrid approach to merge the benefits of clean-room and digital printing processes. Fabrication of the master foils can take advantages of high-yield clean-room processes to enable pre-fabrication of high-performance basic devices. Taking OTFTs as basic elements of the array, high-resolution patterning would result in a larger bandwidth and higher switching speed while the geometric (parasitic) capacitance, the operation voltage and power consumption will be reduced. In addition, an improved on/off ratio at lower costs with a higher yield on smaller areas is possible. Following that step, personalization of IGAs can be realized by the best use of additive digital printing techniques, where no mask or subtractive process is required.

The main advantage of this method is that each fabricated foil can be customized to its unique functionality by using low-cost materials and digital drop-on-demand (DoD) printers, which enable quick and accurate placement of interconnects. This method also allows customizing every individual foil thus increasing functional capabilities such as OTP-ROM memories at lower cost (i.e. to implement ID codes or MAC addresses or specific calibration patterns) since it avoids the use of at least one mask.

5.3.1 Automated design flow

Personalizing the design flow and related EDA tools is important for IGAs, since specific masks have to be automatically generated for every individual foil, due to its individual functionalities. The proposed flow is illustrated in Figure 5.21.

The IGA architecture is developed using a hierarchical pcell based strategy to be easily adapted to design and technology changes such as design rules updates and process improvements. Pcells and Python scripts were adopted to be instantiated in GLADE freeware IC layout editor. Technology file (containing information about the stack of layers and their identification for EDA tools), together with the IGA design parameters are the input sources for the IGA architecture generator pcell script. IGA design parameters include its size, and the number of BBC blocks, logic design family

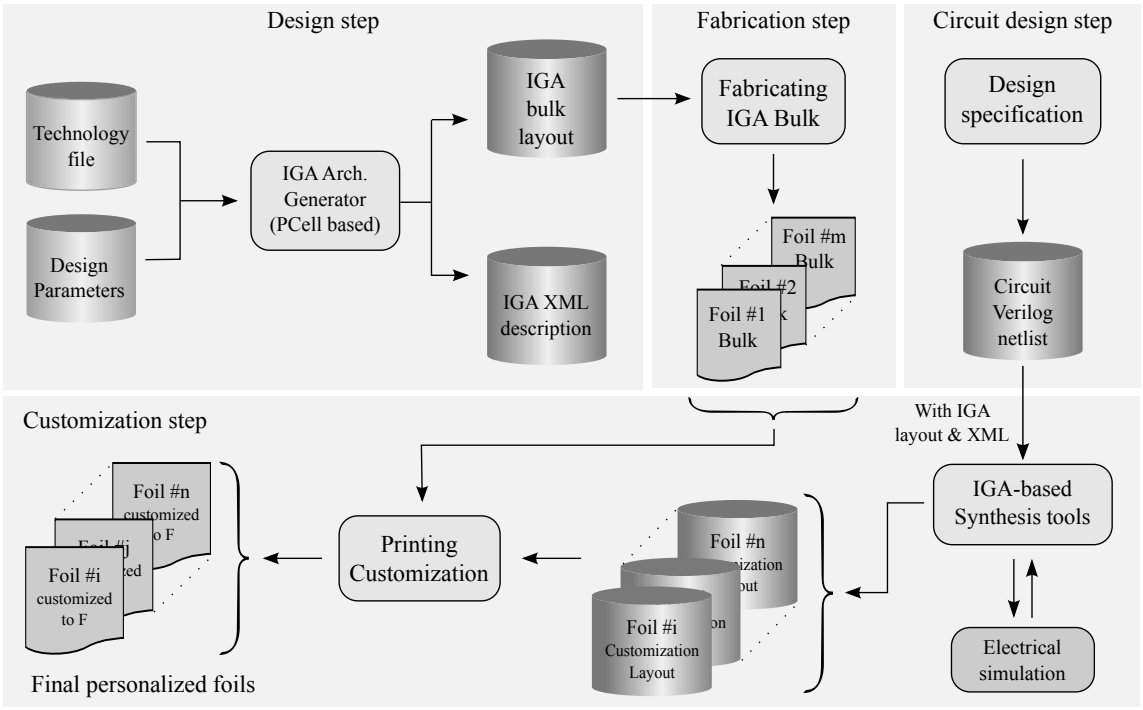


Fig. 5.21 Schematic of the design, fabrication, and customization flow in case of IGAs for functionality personalization

and its corresponding drive and load transistors´ dimensions, the width of the wire channels, number of local and global wires, number of pads, and etc.

The procedural IGA architecture generator will provide the physical layout to be printed, as well as an XML (Extensible Markup Language) description of the IGA structure. The XML file (optional) represents the information about the location of transistors and routing elements for later circuit implementation. In fabrication step, several master foils/substrates of the IGA bulk will be fabricated and stored, being called as: Foil #1 Bulk, Foil #2 Bulk, ..., and Foil #m Bulk. These foils contain similar and uncommitted IGA structure and dimensions.

In order to implement a digital circuit with its particular functionality of a reasonable complexity (i.e. $<$100k gates), the first step is to have the Register-Transfer Level (RTL) description of the circuit from the design specifications (behavioral description). RTL is a design abstraction, which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers and the logical operations (combinational logics) performed on those signal. Then, the RTL-level description, which is usually coded in Verilog HDL (Hardware Description language), gets translated to gate-level or transistor-level description, being called the Verilog netlist. Netlist is a description of

the connectivity of the circuit, consisting of a list of the terminals (or so-called "pins") of all the devices (in this case, transistors), and their interconnections.

The customization step requires providing to the IGA-based synthesis tool: (1) The circuit functionality, described in Verilog netlist; and (2) The IGA layout structure. As a result of P&R (Place and Route) processing, a new XML file will be generated containing the detailed routing information for every foil. Finally the generated file, is converted to the proper format to be used as input pattern for the digital printer. In most of the cases, the proper input pattern is a bitmap file for the digital printers (Inkjet, Aerosol jet), and some modern digital printers such as superfine inkjet require a text file as an input.

In this thesis, the main focus of the automated flow is in respect to the design step and automated generation of the IGA bulks, therefore, most of the benchmark circuits have been manually implemented onto the IGA foils, due to their simplicity. However, the proposed automated design-customization flow is generic and can be used for more complex circuits, where synthesised netlist, and P&R algorithms are required. These algorithms are useful to optimize the circuit performance in respect to several cost functions, such as area optimization, parasitic effect minimization, critical path improvement, and etc.

5.3.2 Photolithographic IGA

As a proof of concept, I have designed several IGAs for mask-based photolithography and dry-etching technology, which was described in Section 4.2.1. Design and development of each sections of the IGAs are explained below.

OTFTs and BBC blocks

As explained before, the ratioed p-type logic family with Zero-V_{GS} load topology, with drive to load ratio of (1/7) for inverters (and 1/14 for NAND2), has been selected inside BBC blocks. This is due to the fact that the transistors work in the depletion-mode with positive threshold voltage. For choosing the number and arrangement of drive and load transistors, obviously, ratioed p-type style requires more number of drive transistors than load ones. Therefore, 6 drive and 3 load transistors arranging as 3-3-3 (drive1-load-drive2) were chosen. Other combinations such 2-2-2, 4-4-4, or even 4-3-4, and 2-3-2 could be chosen which provides a trade-off between the BBC size and number of BBCs for specific IGA size. In the cases where the technology offers very high yield ($\approx 99.99\%$), increasing the number of transistors in BBC does not have any advantage.

This issue will be discussed later in 5.5. Figure 5.22 shows the schematic of BBC block, as well as the layout of the drive and load transistors. In this example, the transistors´ dimensions are as below:

Drive1: $(W_{\mathrm{f}} = 66\ \ m\ \ nf = 4\ \ L = 4\ \ m\ \ W = 264\ \ m)$
Drive2: $(W_{\mathrm{f}} = 66\ \ m\ \ nf = 2\ \ L = 4\ \ m\ \ W = 132\ \ m)$
Load: $(W_{\mathrm{f}} = 231\ \ m\ \ nf = 8\ \ L = 4\ \ m\ \ W = 1848\ \ m)$
$(\frac{W}{L})_{\mathrm{L}} = 7\ (\frac{W}{L})_{\mathrm{D1}} = 14\ (\frac{W}{L})_{\mathrm{D2}}$

where, W_f is the finger width, nf is the number of fingers. Drive1 is dedicated only to inverter gates, and Drive2 is for NAND2 cells.

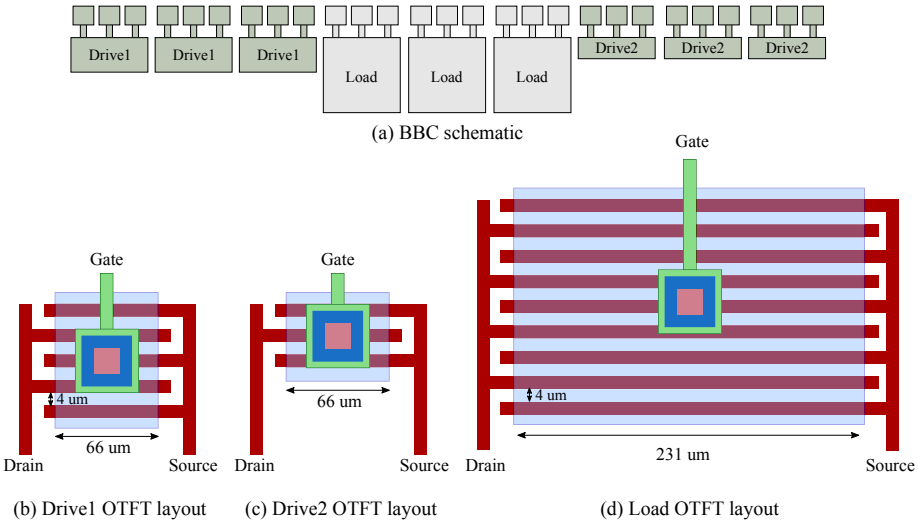


Fig. 5.22 An example of schematic and fabricated BBC block, with the layout of its transistors

Wire cells

IGAs with both wiring styles (line-configurable and drop-configurable) have been designed and manufactured during the thesis. However, due to the fact that metallization of drop-configurable wire cells have shown higher yield and reliability, IGAs with this structure is being mentioned here. An example of line-configurable IGAs is also shown in A.

There is a trade-off between the number of drive and load transistors inside the BBC cell and the wiring channel height. By increasing the BBC size, more local wires are required to build more elementary gates inside the BBC, and also more global wires are required for connecting those gate inter-BBCs. Besides, the number of local wires depend strongly on the type and number of the elementary gate(s) that is going

to be implemented inside the BBC, which can change for different cases. Furthermore, placement and routing algorithm is another key factor in determining the WC size. Taking all into account, obtaining an accurate and optimized value for number of local and global wires is a complex and confusing job.

However, it is desired that the wire channel is large enough to be capable of implementing all the possible logic gates (from the technology library) in one BBC. On the other hand, it should not be too large to occupy too much space in the IGA bulk, since the cost of wire channels in respect to area is much higher than BBC cells. As an example, the BBC block mentioned in Section 5.3.2 with 6 drive and 3 load testable transistors (with pads) occupies ($0.6 \times 6.6mm^2 = 3.96mm^2$). This value can be reduced down to ($0.075 \times 6.4mm^2 = 0.48mm^2$) in real life without testable pads, which is still limited in length by the spacing of drop-configurable wiring banks. Dimensions of each drop-configurable local wire in the WC is almost ($0.075 \times 6.4mm^2 = 0.48mm^2$), which is similar to the BBC block. This means that for adding every single local or global wire, we are adding an area cost similar to one BBC block.

For the BBC block with six drive and three load transistors, an arrangement of 6 local and 5 global wires, beside 2 power rails for V_{DD} and ground was chosen. This combination is capable of implementing several Inverter, and NAND gates. Figure 5.23 shows the schematic of the drop-configurable wire channel on top of BBC block.

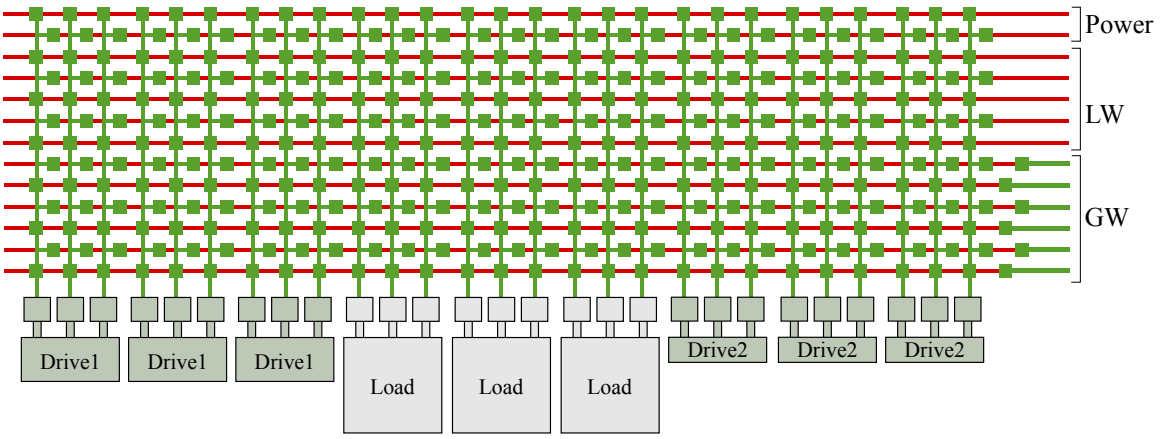


Fig. 5.23 An example of schematic of wire channel and BBC block

Figure 5.24 shows a sample of small prototype IGA, consisting of 6 BBC blocks (3-3-3 arrangement) which has 54 OTFTs in total, and 54 I/O pads. The total area of the IGA is $0.65 \times 2.15cm^2 = 1.4cm^2$. As shown in the captured image, the transistors in prototype IGAs have bid pads ($0.2 \times 0.2mm^2$) for gate, source, and drain electrodes. Those pads are designed for characterizing the transistors, although it is a high-yield

process and there is no need to test whether or not they are working. Due to the limitations of the available space in fabrication runs at NeuDrive-CPI, these structures are aimed both for IGA, and process development. Thus they can be tested to extract parameters and run-to-run comparison.

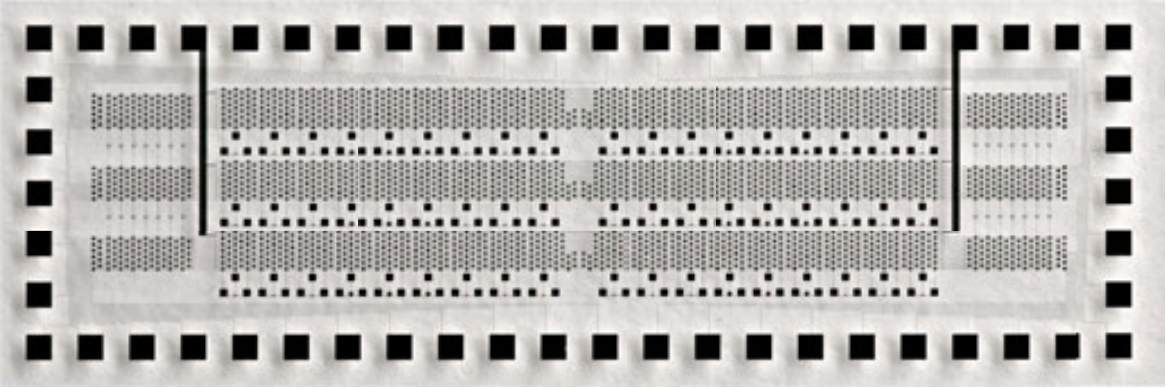


Fig. 5.24 A small prototype of IGA fabricated by photolithography technology

Further IGAs without testable OTFT have been designed and fabricated, in order to increase the density. The largest designed IGA consists of 28 BBC blocks with 252 OTFTs, occupying 1 7 2 $2cm^2 = 3\ 7cm^2$ (shown in Figure 5.25)

Considering the trend towards increasing circuit complexity, it is important to increase the integration density. Table 5.11 provides a comparison of transistor density in our proposed IGAs (4 m process) and the state of the art 8*8 SOTG cell array [27] (20 m process), and PAL [204] (5 m process). Although the proposed IGA structure is channel-based structure (not sea-of-gates), it offers the highest transistor density comparing to other arrays existing in the literature, because it is fabricated at a high resolution technology, and also the wire cell is developed to be optimized for space. The number of transistors per unit area is almost twice as PAL, and 10 times more than UCLP. Another important feature is the number of transistors per unit area per minimum transistor length, which is 2.5 times higher than PAL, and 48 times more than UCLP.

Table 5.11 Transistor density comparison

	8	8*SOTG*	PAL	IGA
# Transistors		384	1260	252
Chip area (cm_2)		53.3	35.8	3.7
Transistors/cm^2		7	35	68
(Transistors/cm^2) $L_{\min}$		0.35	7	17

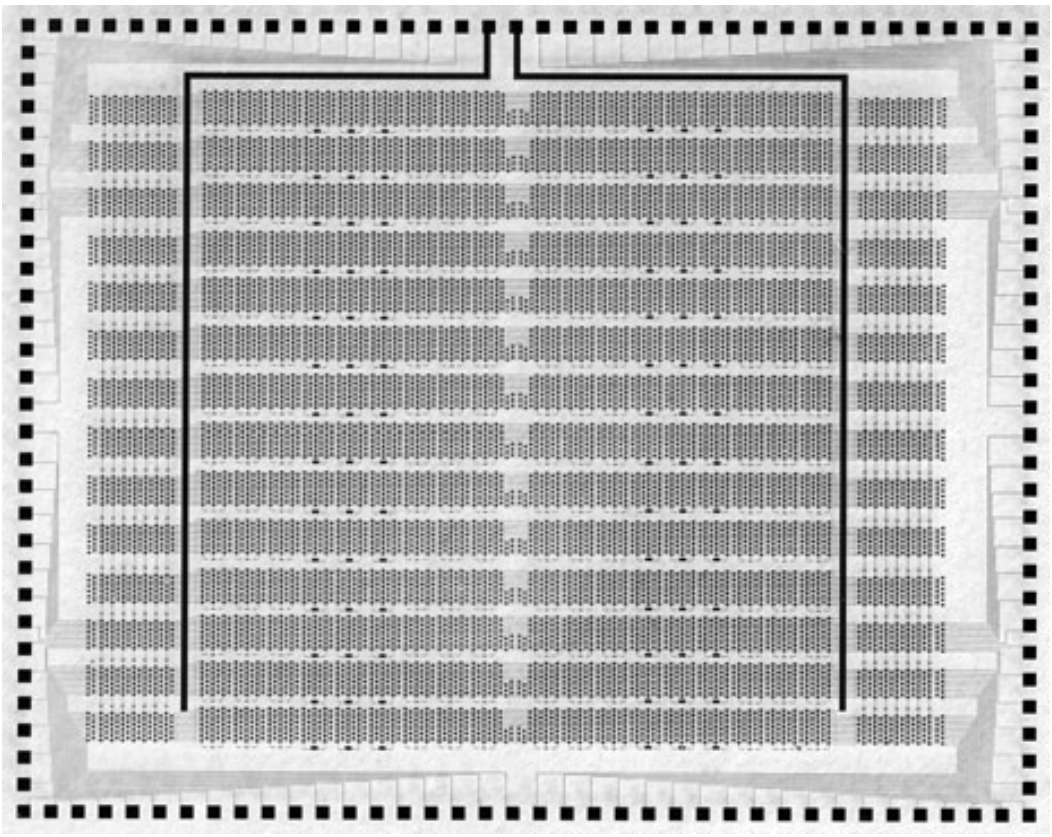


Fig. 5.25 A large prototype of IGA fabricated by photolithography technology

Similar to FPGAs, where there are different devices with different sizes (number of transistors and logic blocks), performance (speed) and capabilities (specialized I/O and functions), the IGA master foils can also be manufactured in different sizes and the user can select the desired foil according to the circuit complexity required for the final application. Thus, IGAs with small sizes (small number of BBC cells and narrow wire cells) can be used for simple applications and prototypes, while IGAs capable of implementing complex circuits with thousands of transistors (such as controller unit for flexible display, microprocessors, and etc.) will have larger dimensions.

Nowadays, all the designs are being fabricated on $20 \times 20 cm^2$ substrates which allows IGA with 12 times bigger dimensions than the current large IGAs. This can lead to integration of almost 3000 number of transistors, which enables Large-Scale Integration (LSI), similar to 1970´s for conventional electronics. Implemented circuits on top of photolithographic IGAs will be shown and discussed later in Section 5.4.

5.4 Circuit implementation

As a proof of concept, some elementary circuits have been implemented onto the IGAs, and will be shown in this section. It should also be mentioned that some benchmark circuits, which are mostly used in flexible electronic applications are being developed and implemented onto the IGAs. However, due to some limitations in respect to the timing of thesis and fabrication runs, they have not been ready (either prototyped or characterized) to be shown in the thesis.

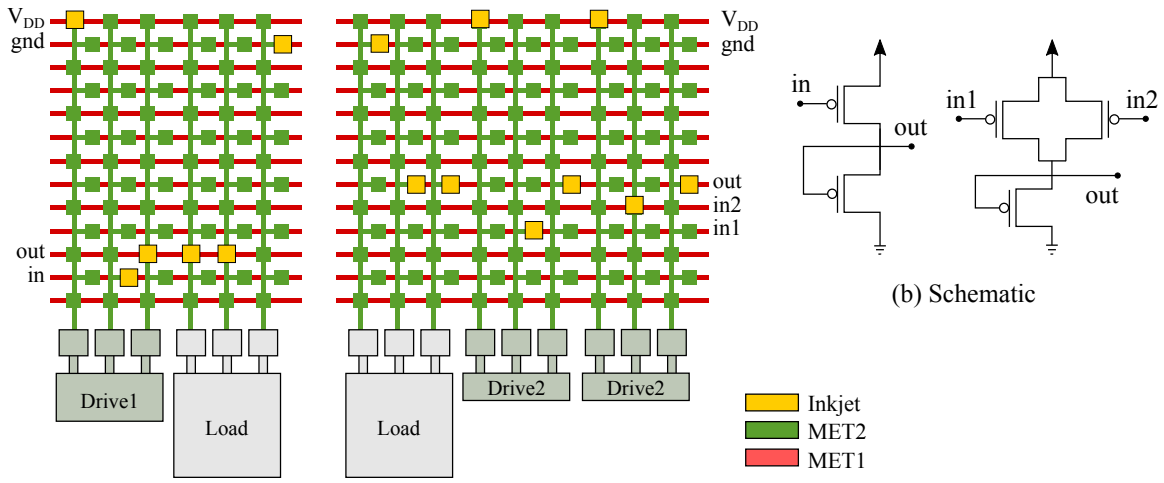
The small transistor-based IGAs fabricated by photolithography technology at NeuDrive-CPI, with transistor channel length of $4\mu m$, have been used as the reference for implementation of most of the elementary logic circuits. The functional circuits and benchmarks, with higher transistor count, have been implemented onto the large IGAs. The metallization of all the IGAs has been realized by using Dimatix 2831 inkjet printer, following the similar procedure as explained in section 5.2.2.

5.4.1 Basic logic gates: INV, NAND2

Initially, transistors are IJP-wired to build inverter and nand2 circuits with Zero-V_{gs} load for ratioed logic style. Figure 5.26 shows the schematic and layout of the implanted circuits inside the IGA. The gate, source, and drain electrodes of the OTFTs are connected to the vertical MET2 wires in the first fabrication process. Later in customization step, each of these electrodes is connected to a horizontal MET1 wire by an inkjet (yellow) drop. For example, the gate of the drive transistor is connected to "in" signal, and also the source and drain are connected to "Vdd" and "out" signals, respectively. For the Zero-Vgs load transistor, gate and source are connected to the same "out" wire, and the drain is connected to ground.

Figure 5.27, is an image of the section of IJP-wired IGA, which was used to build the inverter circuit. The wires related to V_{DD} and gnd are connected to the global ring of power supply with $50\mu m$ width, which is distributed around the IGA foil (not shown). As it is illustrated, the connection banks for each vertical line is located in a Zig-Zag pattern to optimize the area in respect to via width and separation.

In order to check the variation of the inverter behavior, caused by the parasitic effects of the wiring channels, three inverters have been IJP-wired in different corners of one IGA. The static characterization of the inverters is shown in Figure 5.28 (a). Characterization results show that there is a very small variation in static behavior of the inverters in different parts of the IGA, caused by the wiring resistance applied to the ratioed inverter. Slight changes in resistance of the connections will modify the



(a) Layout of metallization of IGA for inverter and nand2 gates

Fig. 5.26 Implemented inverter and NAND2 circuits in the IGA

drive to load ratio, causing the small variation in the output curves. However, this variation does not affect the overall behavior of the inverter.

The customization patterns (MET3) have been also deposited by photolithography process in order to obtain highest reliability and repeatability, as well as providing a comparison between photolithography and digitally printed circuits. Another experiment was done to check the matching of inverters´ electrical behavior when using digital printing techniques and mask-based technologies. For that, an IJP-wired inverter on one IGA foil is compared to its corresponding one that was wired by photolithography on another IGA foil, shown in Figure 5.28 (b). Both inverters were implemented by using the same drive and load OTFTs in the similar sections of two IGA foils. This means that the resistive effect of the wire cells inside the IGA is similar for both case and only different wiring technique can be the reason for different behavior. Figure 5.28 (b) shows that there is a perfect matching of two inverters wired by different technologies, which means the electrical behavior of an inkjet wired inverter is very similar to the photolithography wired one.

The dynamic behavior of the IJP-wired inverters and nand2 gates have also been characterized in order to extract the rise time (T_r), fall time (T_f), high-to-low and low-to-high propagation delays (T_{PHL}, T_{PLH}) and thus the maximum capable operation speed. A 30 (v) p-p input pulse with 100 KHz was applied to the inverter. The "in" and "out" signals are shown in Figure 5.29. The output signal should be scaled by 1.8X, which is the attenuation factor of the pico-probe used to measure the output. Thus, the p-p output swing of 27.4 is observed for the IJP-wired inverter. Fall and

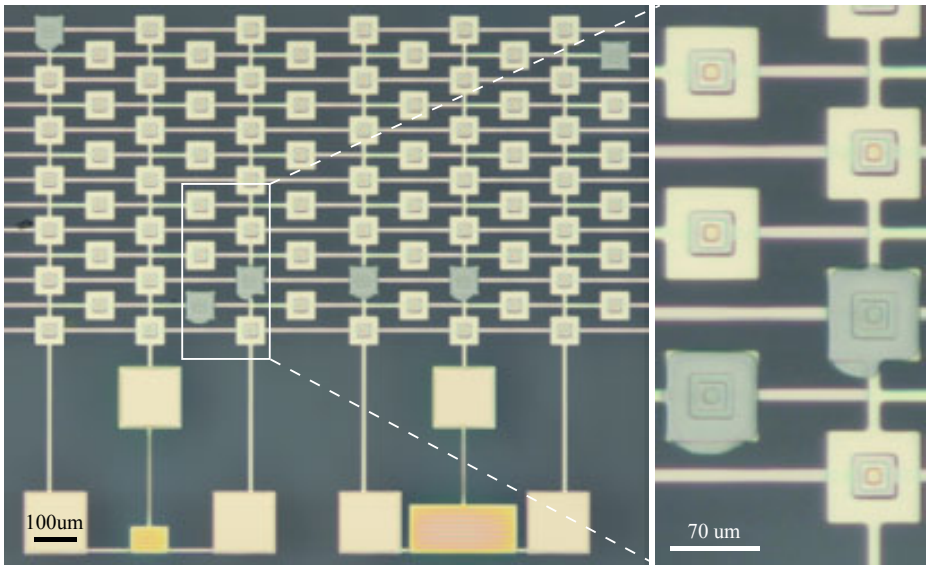


Fig. 5.27 Micro-image of the IJP-wired inverter circuits in the IGA

rise times are measured by the oscilloscope, and shown at the bottom of the signals ($T_{\mathrm{f}} = 2.4\mu s, T_{\mathrm{r}} = 1.1\mu s$).

The high-to-low and low-to-high propagation delays are also measured and equal to $T_{\mathrm{PHL}} = 1.5\mu s, T_{\mathrm{PLH}} = 0.7\mu s$, therefore, the propagation delay of the IJP-wired inverters are calculated from Equation 5.6, and is equal to: $T_{\mathrm{P}} = 1.1\mu s$.

$$T_{\mathrm{P}} = 0.5T_{\mathrm{PHL}} + 0.5T_{\mathrm{PLH}} \rightarrow T_{\mathrm{P}} = 0.5(1.5\mu s) + 0.5(0.7\mu s) = 1.1\mu s \qquad (5.6)$$

5.4.2 Ring oscillator

Some 5-stage ring oscillators have been wired inside the IGA by using IJP and photolithography. Figure 5.30 is the micrograph of the IJP-wired 5-stage ring oscillator with one output buffer. Due to the fact that this circuit requires 6 inverters, which means 6 drive and 6 load transistors, it occupies two BBC blocks, and therefore, I have shown only one section (3 drives) of the circuit for better fitting. As it is illustrated, source terminal of the all drive transistors is connected to power supply, and the gate of each transistor is connected to the drain of the next one.

20 ring oscillators were built on different sections of 5 different IGA foils (10 IJP-wired, 10 PH-wired). All of the ring oscillators were tested by using the same pico-probe. It was found necessary to increase the supply voltage to 30 (V) to initiate stable oscillation with 40 (V) being typical. Figure 5.31 (a) is a histogram showing the

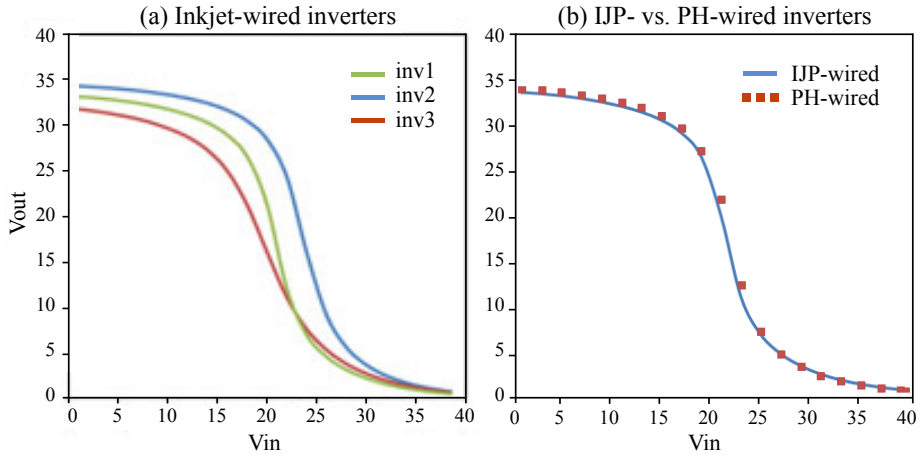


Fig. 5.28 Static characterization (in-out curve) of IJP-wired inverter on different corners of the IGA

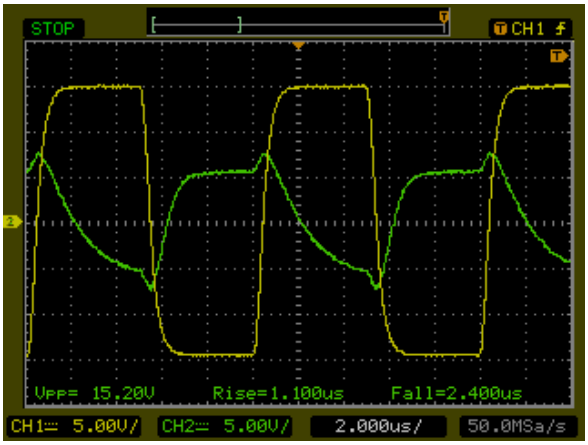


Fig. 5.29 Dynamic characterization (in-out curve) of IJP-wired inverter onto the IGA

number of wired ring oscillators with output frequency in the 10KHz band, and (b) is the output frequency versus p-p swing of the ring oscillator for 20 wired samples.

Figure 5.32 shows the maximum frequency obtained by IJP-wired ring oscillators, which is 74KHz for 7.9 (V) output swing.

According to the stage delay of inverters in previous section, the expected oscillation frequency of the ring oscillators can be estimated by using the Equation 5.7, where N is the number of stages.

$$F = \frac{1}{2NT_{\mathrm{P}}} = \frac{1}{2 \quad 5 \quad 1\,1 \;\; s} = 91KHz \tag{5.7}$$

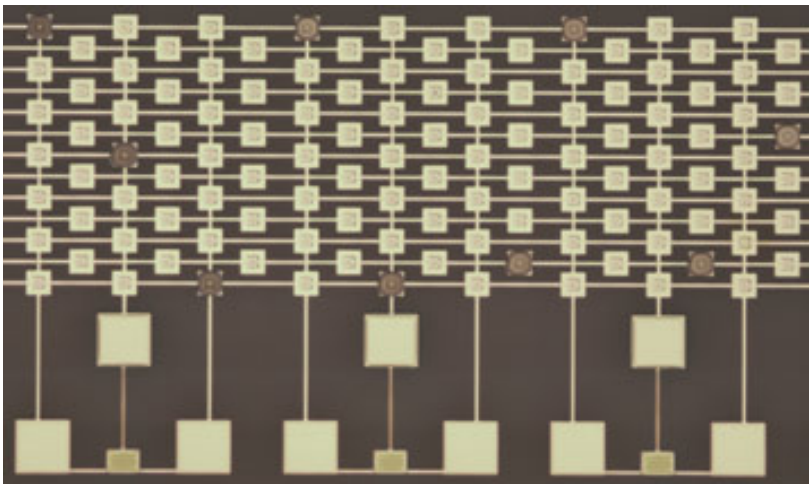
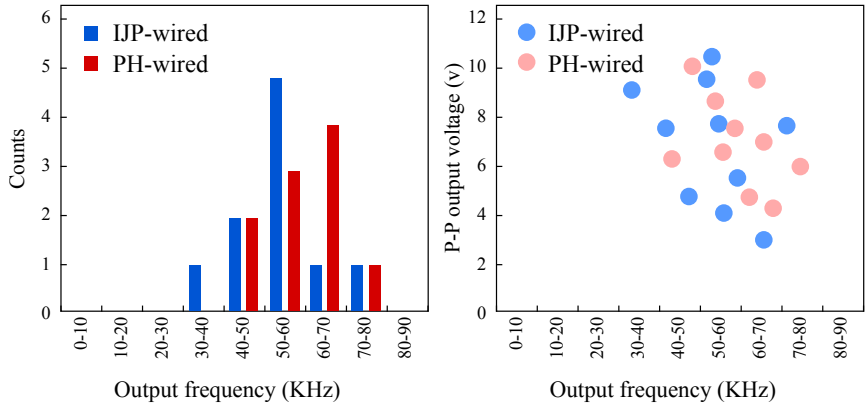


Fig. 5.30 Schematic and the layout of the IJP-wired ring oscillator circuit



(a) Histogram of RO count with F (b) Frequency vs. p-p output swing

Fig. 5.31 IJP- and PH-wired ring oscillators inside photolithography IGAs

The measured results show that the maximum oscillation frequencies ($F_{\text{measured}} = 74KHz$) is very close to the calculated value ($F_{\text{calculated}} = 91KHz$), and the small difference can be due to the fact that parasitic capacitance of the wiring cells in IGAs affect the ring oscillators more than single inverters. The average measured frequency of IJP-wired ring oscillators is ($F_{\text{average-IJP}} = 54KHz$), and for the PH-wired ones is ($F_{\text{average-PH}} = 59KHz$). This shows a very good matching between two different metallization techniques, and makes inkjet the best candidate for IGA metallization.

However, the difference between the frequency and output swing of full-custom ring oscillators (see Section 4.3.4) and the semi-custom ones is a lot (less that one order of magnitude). The main reason for that is the parasitic effect of wiring channels. Long and narrow resistive wires that are distributed all over the IGA wire cells provide a

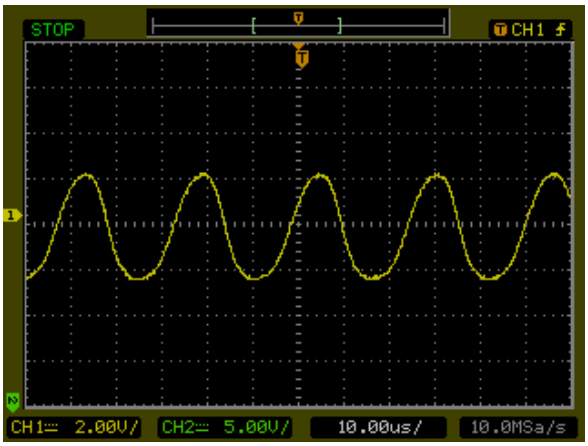


Fig. 5.32 Output voltage of IJP-wired ring oscillator with highest oscillation frequency

high resistive factor, which affects the output swing of the ring oscillator. Besides, the Metal-Insulator-Metal (MIM) capacitance generated from the grid of two metal layers contributes as a parasitic factor, and reduced the operation speed of the circuit.

Two solutions have been proposed recently, and are being developed: First, the wire cells are improved in respect to the parasitic effects, and the proposed structure is presented in Section 6.2; Secondly, the concept of cell-based IGA can reduce the above-mentioned issue dramatically, since the inverters and nand gates are already built in full-custom manner.

5.5 IGA for yield improvement

Many of the current printing technologies especially the non-clean-room ones (gravure, partial or full-inkjet, etc.) are suffering from high process variation, which are results of soft faults. The adopted low-temperature, and low-cost manufacturing approach, as well as, intrinsic limitations of the organic materials can cause the variation in device performance, which leads to considerable deviation from the desired performance of the final circuit.

Another bottleneck in these printing technologies is low/mid-yield at device level, which are results of hard faults during the fabrication (layer break-down, layer-to-layer misalignment, and undesired drops or dust onto the substrates) or lifetime of the devices. Yield at device level is defined as the number of working transistors out of the whole fabricated transistors. Mid-yield at transistor level causes very low yield at circuit level: either custom- or semi-custom-designed ones.

For custom-designed or standard cell semi-custom circuits, all the transistors are in direct contact together and build functional blocks of the circuit, therefore, an existence of a hard fault for even one single transistor, often causes the entire circuit to fail. In case of gate arrays, not all of the existing transistors in the array are used to build the functional logic. However, as long as the hard faults are not recognized, the final customized circuit is not safe from including failing transistors, which, again can fail the entire circuit functionality.

One solution is to customize several numbers of gate array master chips/foils to similar functionality, in respect to the expected yield of the technology, so that at least one or two of them work properly. However, the big challenge in this case for printed electronics is that the yield, as well as fault distribution, can differ even within the same technology, either foil-to-foil or run-to-run. Thus, calculating and estimating the technology yield is not an straightforward way of dealing with variable yield.

In this work, we present a design-manufacturing methodology to overcome the above-mentioned issues related to variable technology yield, by best use of fault-tolerance techniques. Fault-tolerance methodology allows the designers to build circuits from only working transistors, by providing them the failure map of each individual printed foil. For that, a new step, being known as characterization, is required at the middle of bulk generation and circuit customization.

Therefore, fully working (high-yield) circuits can be obtained out of mid-yield foils through three consecutive processes (separated in time): (1st) A regular array of unconnected testable transistors are designed and printed, (2nd) All the printed transistors are characterized individually by means of an automatic characterization environment, to report the distribution of Known Good OTFTs (KGOs), (3rd) EDA tools produce the wiring pattern for the requested functionality, taking into account the failure map of every individual foil, and thus, only KGOs are wired by using digital printing.

Individual OTFT characterization can also provide detailed information about the electrical behavior of the transistors, such as mobility, I_{on}, I_{off}, V_T, and on-resistance that can be used to monitor process results. Moreover, for implementing analog circuits, which require transistors with less electrical behavior variation, an accurate and detailed characterization of the transistors provides more reliable and robust design.

5.5.1 Automated design flow

The main difference between the automated design flow of IGAs for yield improvement and functionality personalization is the added characterization step in IGAs for yield improvement. The proposed flow is illustrated in Figure 5.33.

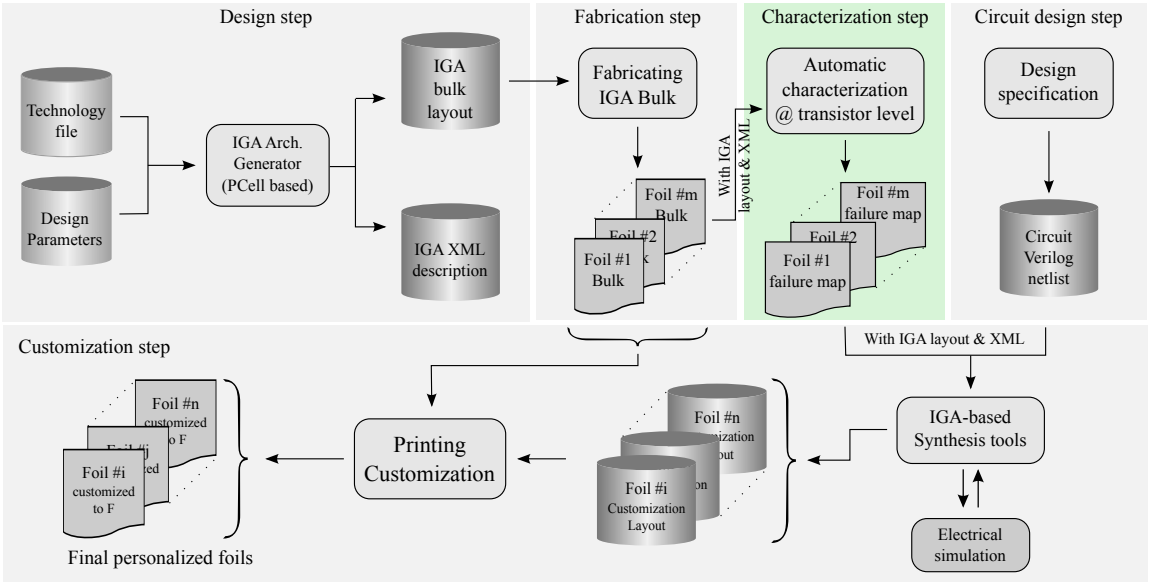


Fig. 5.33 Schematic of the design, fabrication, and customization flow in case of IGAs for yield improvement

In this case, once several foils with the same structure were printed, they are ready to be characterized in order to extract the KGOs distribution for each individual foil. An automatic characterization environment has been developed in order to speed up and facilitate the electrical characterization of large amount of transistors placed in a regular array, following IEEE 1620 standard for printed and organic transistors [168]. Semi-automatic Cascade Microtech Summit Series probe station, in combination with all the suitable measurement instruments has been used (Section 4.1.2).

The transistors will be tested for several features (such as short circuit between gate and drain/source, channel short, gate current leakage, and device stability), as well as electrical bias sweep. As a result, two text files of CSV and XML containing the characterization results, KGO distribution matrix, and potentially transistor model are generated.

The customization step requires providing to the IGA-based synthesis tool: (1) the circuit functionality, described in Verilog netlist; (2) the IGA layout structure; and (3) the failure map or KGO distribution of each individual foil. In this case the P&R

(Place and Route) step and its corresponding detail routing file varies between foil to foil, even for the same circuit netlist. The reason is that each foil has its own KGO distribution, and therefore, requires its specified logic placement and detailed routing. Finally the generated file, is converted to the proper format (bitmap, or text) to be used as input pattern for the digital printer.

5.5.2 All-Inkjet IGA

As a proof of concept, IGAs for all-inkjet technology (explained in Section 4.1.2) has been designed and fabricated on a S2S process to enable high alignment accuracy at Technical University of Chemnitz (TUC). OTFTs and other cells are developed based on a combination of industrial printing platform (Dimatix-DMP3000) [221] and laboratory printing platforms (Dimatix-DMP2831) [216].

Design and generation of IGA bulk

Due to the fact that only p-type organic transistors were available in this technology, ratioed p-type cell style is selected. The process development and OTFT performance optimization in this technology can be found in [119]. Thus, I skip detailed explanation about development of OTFTs and their electrical parameters. The proposed layout of a transistor in this technology is shown in Figure 5.34.

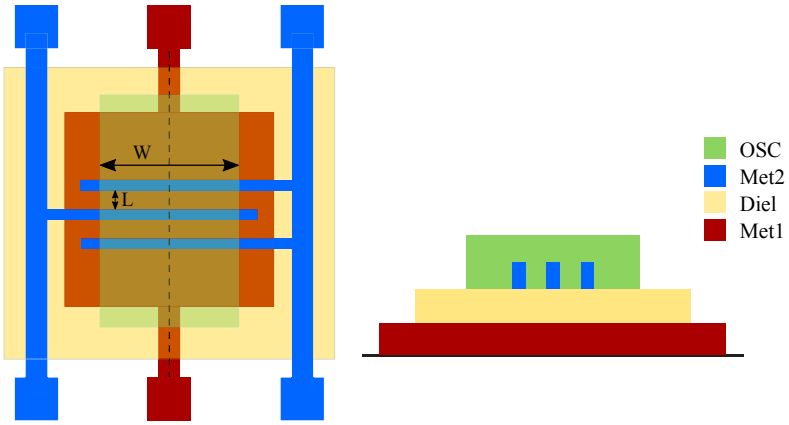


Fig. 5.34 Layout of the all-inkjet OTFTs

The important feature when designing BBC blocks of the IGA in this technology is the operation mode of the OTFTs. Figure 5.35 shows the I-V transfer curves of

the p-type OTFTs shown in Figure 5.34, with ($W_{\mathrm{f}} = 750\ \ m\ \ nf = 2\ \ L = 69\ \ m\ \ W = 1500\ \ m$).

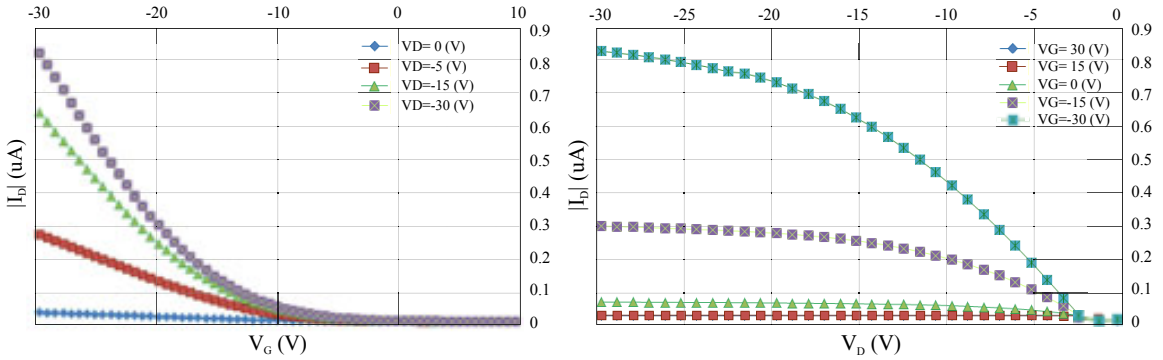


Fig. 5.35 I-V transfer curves of the all-inkjet p-type OTFTs

As it can be seen, the threshold voltage of these transistors is around -10 (V), making them enhancement-mode transistors. As explained before in Section 3.5.2, the best ratioed logic family for enhancement-mode transistors is **diode-load** style, with three power rails (V_{DD}, V_{SS}, gnd). The gate and drain of the load transistor is always connected to V_{SS} and gnd, respectively. For this logic family, the drive transistor is expected to be larger than the load one, and this ratio is set to 8 for inverters, and 16 for NAND2 gates:

Drive1: ($W_{\mathrm{f}} = 750\ \ m\ \ nf = 8\ \ L = 69\ \ m\ \ W = 6000\ \ m$)
Drive2: ($W_{\mathrm{f}} = 750\ \ m\ \ nf = 12\ \ L = 69\ \ m\ \ W = 9000\ \ m$)
Load: ($W_{\mathrm{f}} = 750\ \ m\ \ nf = 1\ \ L = 69\ \ m\ \ W = 750\ \ m$)
$(\frac{W}{L})_{\mathrm{D2}} = 2\,(\frac{W}{L})_{\mathrm{D1}} = 16\,(\frac{W}{L})_{\mathrm{L}}$

Figure 5.36 depicts the layout of the drive and load transistors inside the all-inkjet IGA.

Since, ratioed style is selected for building logic gates, it is expected to have more number of drive transistors than load ones. Choosing the number of drive and load transistors is strongly dependent on the average yield of the technology. It is desired to have BBCs capable of at least two or more logic gates.

Several fault injection analysis has been done in order to obtain the most optimum number of drive and load transistors, in respect to maximum possible inverter and NAND2 gates. However, as the failure distribution matrix is different between foils and runs, and also due to the yield variability, there is no reliable optimum combination of drive and load OTFTs. Previous analysis of the yield and process variation for arrays

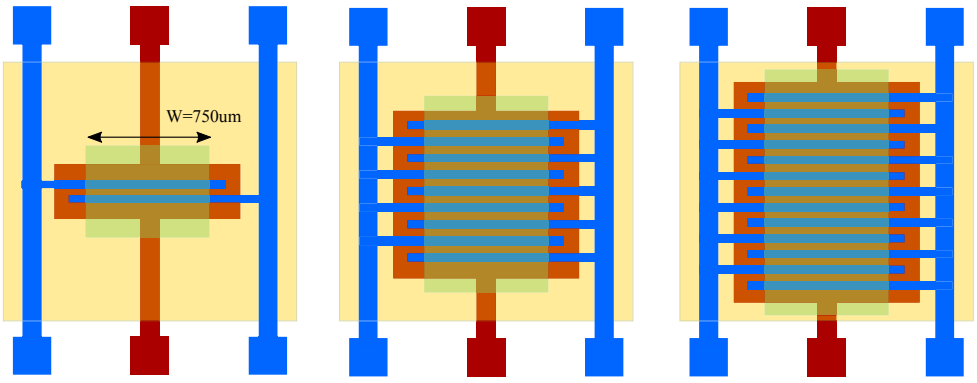


Fig. 5.36 Layout of the all-inkjet OTFTs used inside the IGA

of OTFTs printed in this technology were done in [119]. The results show that the maximum achieved yield at transistor level is around 70%.

Taking the dependency of drive and load combination on the technology yield, and AIG representation of the final desired circuit, I have chosen 4-4-4 (drive1-load-drive2) as the reference for designing the all-inkjet IGA bulks.

The wire cell and inter-channel wire cells are almost similar to the line-configurable wiring style with some modification related to the stack of layers and geometrical design rules. Wider power rails ($W = 500\ \ m$) are distributed on both sides of the BBC and wire cells and connected to their corresponding pads.

Figure 5.37 depicts a sample all-inkjet IGA, including 210 unconnected transistors and occupying 79 130(mm_2) of space, fabricated at TUC. Each transistor has pads with dimensions (500 500 m_2), connected to top and bottom of gate, drain, and source terminals.

Characterization

We have used a similar semi-automated characterization procedure, which were used for testing large array of devices during the thesis, based on adaption of microelectronics instruments [209]. The transistors array were tested for several features (such as short circuit between gate and drain/source, channel short, gate current leakage, and device stability), as well as electrical bias sweep (shown in Figure 5.35). As a result, two text files of CSV and XML containing the characterization results, and KGO distribution matrix were generated. Due to the sequential nature of inkjet printing, for which we can consider that every transistor has individual properties (including faults), these files will reflect the inherent statistical variability given for the fabrication process.

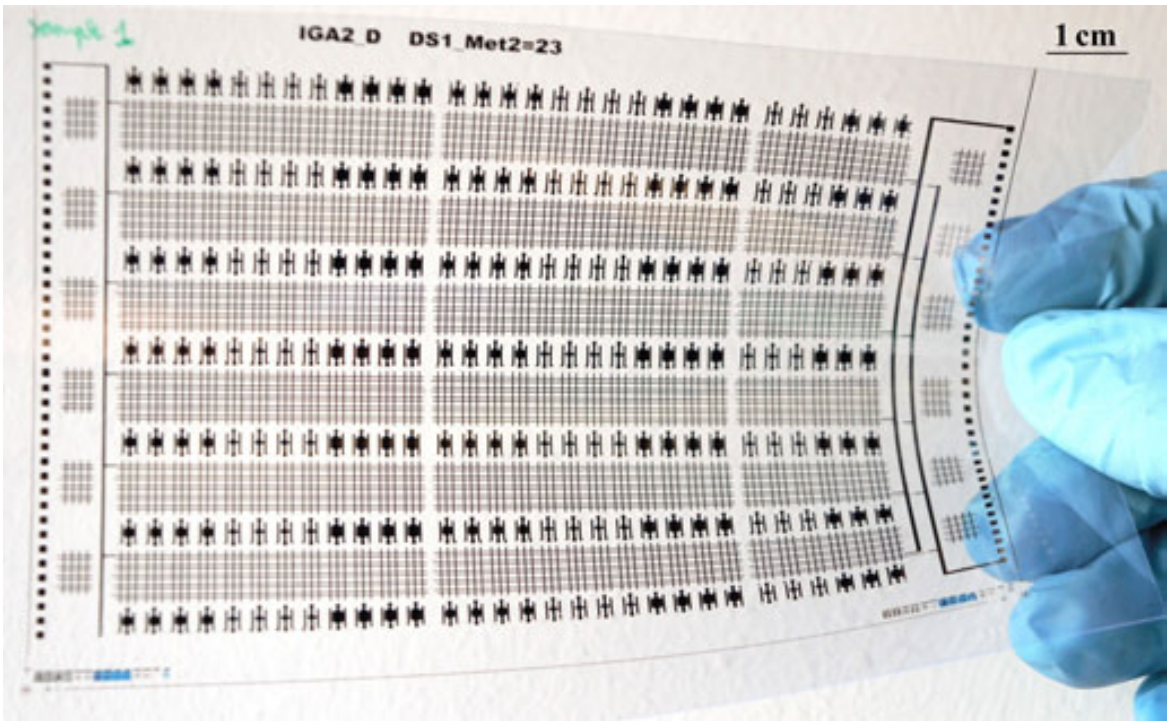


Fig. 5.37 Fabricated IGA by all-inkjet printing technology

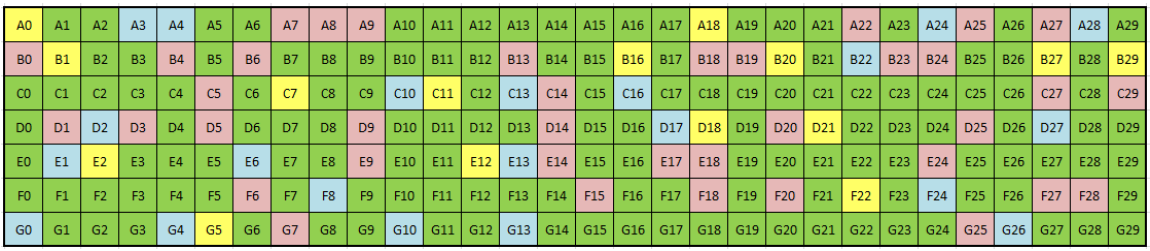
Figure 5.38 shows a sample of generated KGO distribution matrix, which related to two different foils, with similar IGA bulk layout of Figure (5.37). As it can be seen, the failure maps are different for the same run but different foils. Thus those fabricated and characterized foils (both labeled with corresponding IDs with their KGO distribution matrix) can be stockpiled, and used later for customization.

In total, 20 number of IGAs with similar dimensions were fabricated through the inkjet technology at TUC. A4 foil were chosen as the substrate, in which 4 IGA bulks can fit, therefore 5 number of A4 sheets were printed, containing 20 bulks in total. The yield at transistor level changes from 28% to 64%, and the average for 20 samples is 48%. Figure 5.39 is a the distribution of yield for all fabricated IGAs.

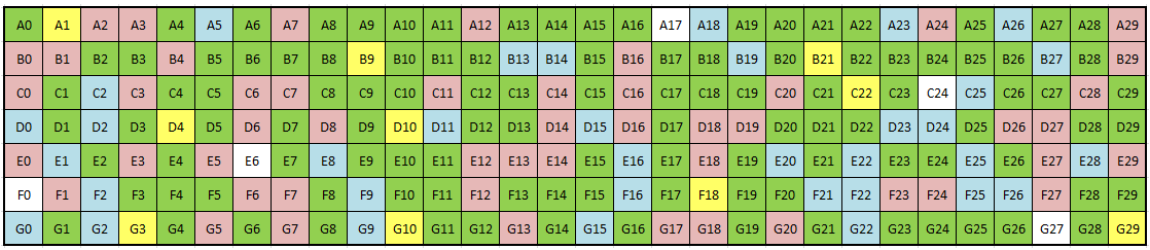
Customization

The main difference between the customization of all-inkjet IGAs and photolithographic IGAs refers to the management of the KGO maps coming from foil testing. This would require differentiated synthesis process for every foil having a different failure map.

Some of the synthesis steps can be reused from current EDA tools. One of them is the circuit synthesis from its high level description (i.e. in VHDL) to produce a



(a) All-inkjet IGA: Foil #1



(b) All-inkjet IGA: Foil #2

Fig. 5.38 KGO distribution matrices of two IGA foils with similar bulk layouts

netlist of Boolean functions. Another is the global and detailed routing and the final verification. Specific EDA steps that have to be implemented are:

- The technology mapping of Boolean functions to logic gates that depends on the available OTFTs (yield)
- Placement of logic gates according to the yield and KGO distribution
- Pre-routing to asset on the available connectivity according to the KGO map

For low number of transistors and few foils this process can be done manually, but when any of those two aspects grow, there is a clear need of design automation tools. Manual implementation will also be important at the initial phase of formulating the algorithms and procedures that EDA tool can implement. In this thesis, a 2-bit Multiplexer has been implemented manually onto two IGAs with different KGO matrices. Figure 5.40 illustrates MUX2 circuit diagrams in terms of inverters and NAND2 gates.

The 2-bit MUX circuit requires three nand2, and one inverter gates, which means 11 transistors in total (1 drive1, 6 drive2, and 4 load). According to the failure map of

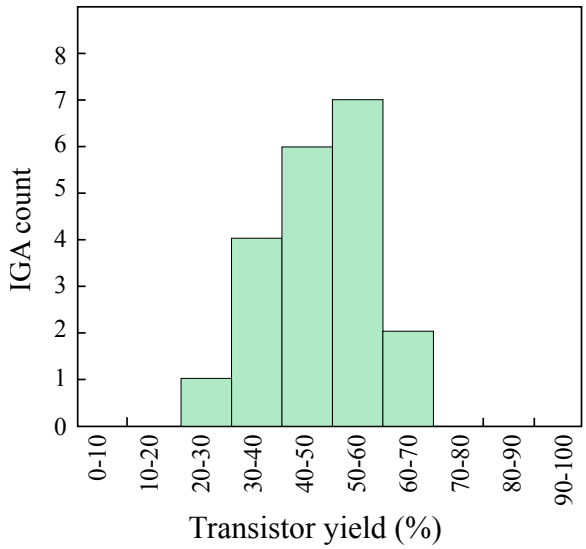
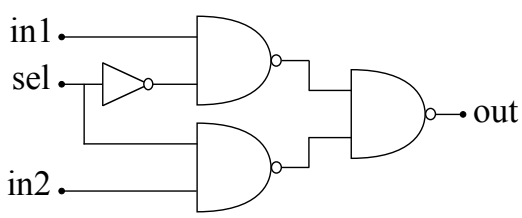


Fig. 5.39 Yield histogram for 20 printed IGAs



Select	Inputs		Out
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

Fig. 5.40 2-bit Multiplexer circuit

foil#1 and foil#2 (Figure 5.38), this circuit can be implemented by using two BBC blocks on top-left corner of the IGA bulk. Figure 5.41 (a) shows the schematic of those two BBC block, and the final metallization pattern for 2-bit MUX is shown in Figure 5.41 (b, c) for two foils. Yellow squares on top of the wire channels are the metallization points that connect MET1 to MET2.

All-inkjet IGAs are still in development and there are large variations in run-to-run and foil-to-foil. Furthermore, in the previously printed IGAs, some undesired spreading and breaking of dielectric layer in the wiring channels have caused hard faults, and consequently, make it impossible to metallize the IGAs. However, by choosing safer margins and more improvement in the process stability and reproducibility, it is expected to obtain customizable IGAs in this technology.

5.6 Summary

In this chapter, the novel concept of Inkjet-configurable Gate Arrays for mapping digital organic electronic circuits on top of pre-designed array of unconnected transistors were introduced. IGA, as a design-technology methodology, takes its heritage from gate arrays in silicon industry. Thus the well-established array-based semi-custom design methodology can be easily adapted adapt to it.

Additionally, digital printing DoD technologies, such as inkjet and superfine jet, allow individual customization avoiding the need for OTPROM or E2PROM devices. This concept is closer to the popular FPGA one since it can be implemented using inkjet printers and metallic materials (in printer cartridges) "at home".

Presented IGA approach can be used to improve the productivity at the level of fully functional circuits out of foils with mid yield. Each array of pre-designed unconnected OTFTs needs to be tested individually in an automatic characterization environment and a unique XML representation of the KGOs for each IGA structure has to be generated. Later on, logic gates and circuits will be implemented by wiring the KGOs.

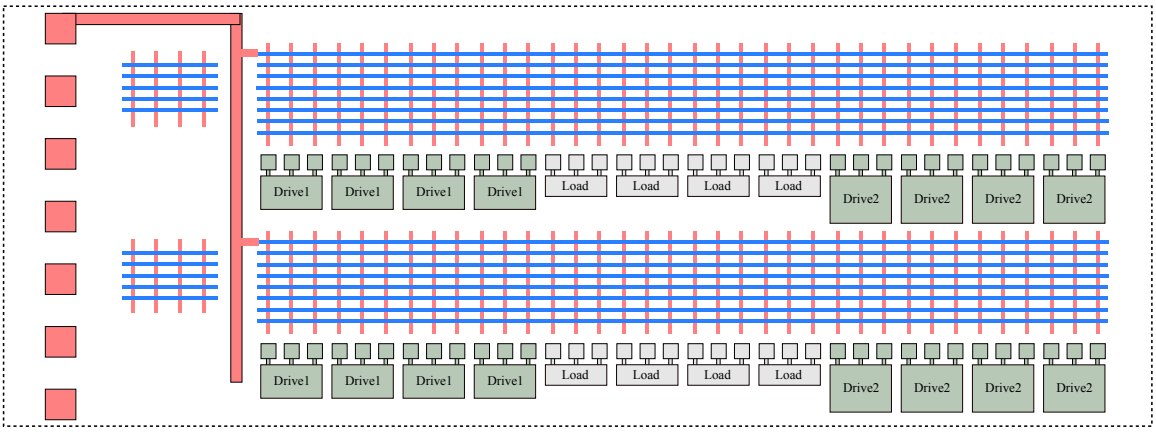
IGA structure is built of four main cells, which are parameterizable and scalable according to the process technology and metallization techniques. Scalability and technology-independency strategies provided by Parameterizable Cell (PCell) have been used to adapt IGA structures to the currently fast technology evolution.

Photolithographic IGAs for improving the functionality personalization were presented in this chapter. Several IGA foils, with transistor-based structure and cell-based structure were fabricated through high-performance high resolution photolithography technology.

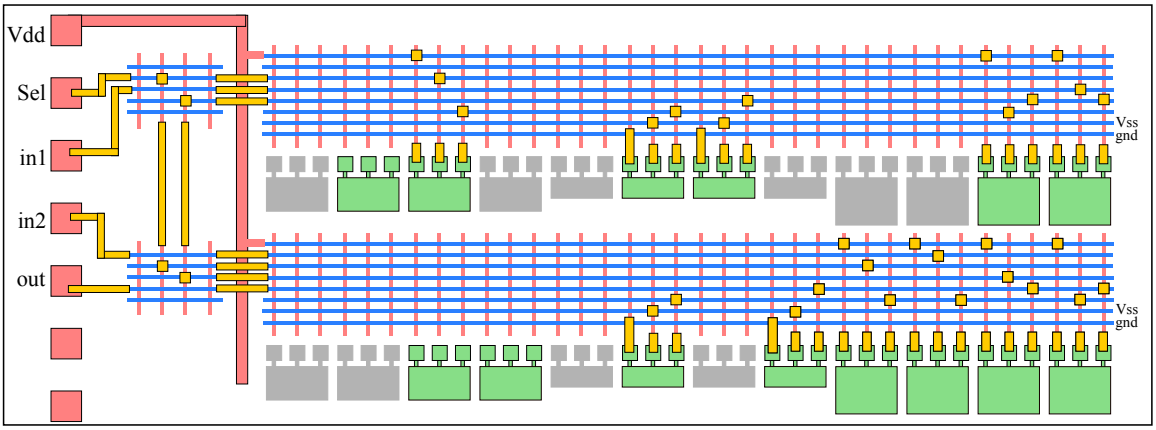
As a proof of concept, basic digital logics (inverter and nand2), as well as ring oscillator circuits with Zero-VGS load connection has been implemented on several IGA foils by using inkjet printer for the metallization step. The static and dynamic analysis of the inkjet-wired circuits were compared with corresponding photolithographically patterned ones and good matching is obtained.

All-inkjet IGAs were also presented in this chapter, with the aim of yield improvement. The inkjet fabricated IGA foils offer mid-yield ($\approx 50\%$) at transistor level, which can lead to a very high yield (99%) at circuit level, by adopting the fault tolerance techniques, in which the failure map and KGO distribution matrix is provided after characterization of unconnected devices.

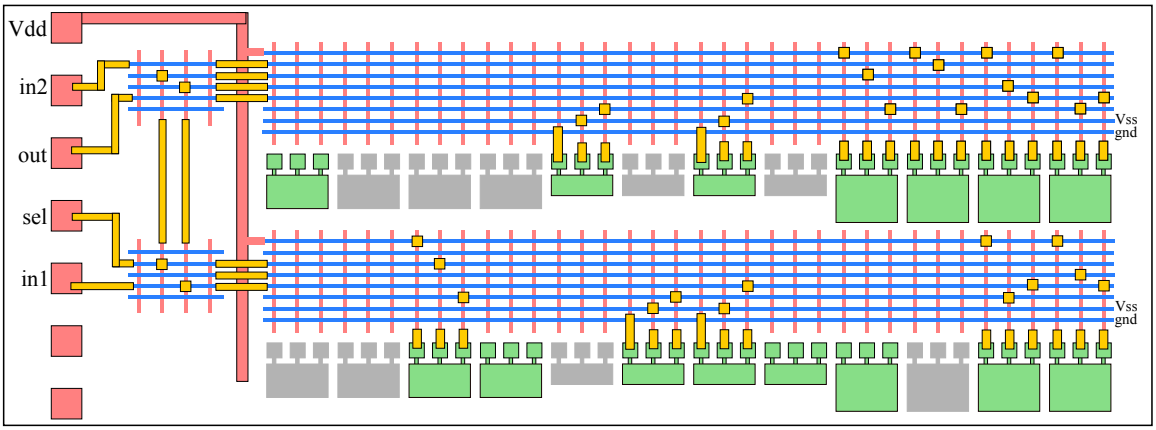
This work has validated the concept of inkjet-configurable gate arrays (IGA) by demonstrating the synergy between high performance photolithography printed devices, and inkjet printing as a metallization step.



(a) Two BBC blocks on top-left corner of the IGA



(b) 2-bit Multiplexer implemented on foil #1



(c) 2-bit Multiplexer implemented on foil #2

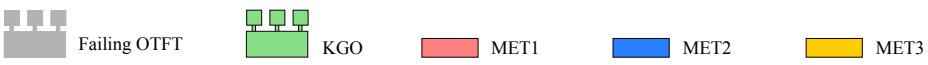


Fig. 5.41 2-bit Multiplexer implementation on two IGA foils with different KGO distributions

Chapter 6

CONCLUSION

6.1 General conclusion

The objective of this thesis was to provide a semi-custom circuit design methodology for development of printed and organic electronic circuits. For that, two well-established concepts from ASIC industry were adapted: (1) Gate Array, (2) Field-Configurability. Gate array concept separates the fabrication of master foils from functional personalization step, and field-configurability allows the personalization of gate arrays in-the-field, without returning the master foils to manufacturer for further metallization process. In the way to combine the gate array design methodology with field-configurability concept for organic electronics, a hybrid approach was proposed to take the advantages of clean-room processes and digital printing techniques.

The concept of process design kit and the necessary information to provide the bridge between technologists and circuit designers were introduced. One of the most important steps in PDK development for any new-born technology is to design a large number of test vehicles for characterization of geometrical design rules, basic devices, and circuits. For that, the parametrization concept was introduced and parameterizable cells were used for designing large matrices of test vehicles.

Improvement of organic thin film transistors, as the most important element in organic electronic circuits, was addressed by defining several physical layout styles: (1) Partially-overlapped interdigitated, (2) Fully-overlapped interdigitated, (3) C-shaped, and (4) Corbino. 750 number of OTFTs were designed, fabricated, and characterized in order to obtain the optimized design style in respect to the electrical behavior of the devices. Partially-overlapped interdigitated transistors offered the best uniformity and repeatability in terms of threshold voltage, I_{on}/I_{off}, and mobility values. Besides,

partially-overlapped and corbino devices, showed less parasitic overlap capacitance, due to the minimized gate-source/drain overlap.

Later, Zero-V_{GS} load inverter and nand circuits, as the most elementary logic gates for development of digital circuits, were designed and fabricated by using high-performance photolithography technology. Static and dynamic characterization results of the circuits were analyzed in order to optimize the circuit behavior. The optimized load to drive ratio of 7 was obtained for Zero-V_{GS} load inverters, due to the highest noise margin and DC gain values, as well as the centered trip point.

Finally, design and fabrication of 5-stage ring oscillators with transistor channel length ($L = 4\mu m$), as one of the most important and indicative circuits, which can give a comprehensive description of the printing technology and its adapted circuit design technique, were addressed. The oscillation frequency of $617KHz$, with stage delay equal to $0.162\mu s$ were demonstrated for custom-designed ring oscillators.

We proposed the novel concept of Inkjet-configurable Gate Array, as a design-technology methodology to map digital circuits on top of pre-fabricated transistor arrays in two separated manufacturing steps. The first step, which is the fabrication of the IGA master foils, through the high-performance photolithography process, is similar to conventional gate arrays. The second step, known as metallization/personalization in silicon gate arrays, which requires generation of new mask(s) for individual circuit personalization, is replaced by a single process of mask-less drop-on-demand digital printing technique, allowing individual personalization of each foil to its unique functionality.

The basic structure of the IGA, which is fabricated by clean-room process, consists of four main cells: (1) Basic bulk cell, (2) Wire cell, (3) Inter-cell connection, (4) I/O pads and power rails. Small and large photolithography IGA prototypes (including 54 and 252 transistors) were fabricated and the maximum transistor density of 68 transistors per cm^2 was obtained. These values are far higher than the state of the art programmable logic arrays. In order to further improve the circuit density and metallization yield and time, we also introduced the concept of cell-based IGA, in which transistor arrays are replaced by logic gates (e.g. inverter, nand). In this approach, the transistor density was improved to 197 number of OTFTs per cm^2.

Line-configurable and drop-configurable DoD wiring methodologies were presented in this thesis, to be used as the Wire cell inside the IGA, aiming to connect the array of pre-designed and unconnected OTFTs together to build functional circuits. Three mask-less digital printing techniques were successfully used for metallization of the designed wire test vehicles: (1) Inkjet; (2) Superfine Jet; and (3) Aerosol Jet printing.

The results were compared to photolithography wired test vehicles and very good matching and high yield was observed.

The wiring yield of the metallized line-configurable structures was 88%, 72%, and 97% for SIJ, AJ, and PH techniques respectively, while the sheet resistance of the printed metals were 1.53, 19.5, 1.3 ohms respectively. The results were improved dramatically for drop-configurable structures, and the wiring yield is now increased to 99.99% for IJ, SIJ, and PH techniques, in good aligning conditions. The resistance per bank for the drop-configurable structures was calculated as 19.2, 12.6, and 11.2 ohms for IJ, SIJ, and PH respectively.

20 ring oscillator circuits, similar to the custom-designed ones, were IJ-wired and PH-wired onto the photolithography IGAs, demonstrating the synergy between high-resolution lithography patterns and mid/low-resolution digital printing. Maximum oscillation frequency of $74KHz$, was observed for IJ-wired ring oscillators inside the IGAs. The average oscillation frequency was 54 and $59KHz$ for IJ-wired and PH-wired ring oscillators respectively.

As mentioned before, the inkjet-wired drop-configurable DoD wiring structures (Section 5.2.1), offer almost 100% yield under good alignment conditions. However, hard faults, caused by physical phenomena such as nozzle break-down or ink spread, are inevitable while printing patterns (even simple drops) by high variability processes (e.g. inkjet, superfine jet). Therefore, customization of IGAs through the drop-configurable wire structures is not error-free and occurrence of unexpected faults is possible, especially when the number of expected drops increases. Therefore, it is desired to reduce the number of printing drops in order to reduce the failure chance.

Besides, the grid of interconnections in WC is inherently prone to parasitic capacitance of overlapping metals, and resistance of long narrow wires. For building a specific circuit, as the number of required connections (drops) reduces, the use of wiring channels, and consequently the parasitic effects of them reduces as well.

Another important feature in implementation of organic circuits is the density. There is usually a tradeoff between the IGA size and its integration capability. It is always desired to increase the capability of the IGA master foils in respect to the number of transistors and implementable gates, while keeping the total size of the IGA master foils as low as possible.

Taking three above-mentioned factors into account, I am proposing a design-manufacturing methodology to improve the IGAs in respect to the customization yield, parasitic effects, density, and functionality. In this methodology, being called "Cell-based IGA" style, the array of unconnected OTFTs are replaced by array of

custom-designed inverters and nand2 gates. The structure of the BBC block in the proposed IGA bulk is shown in Figure 6.1, in which (NAND2, INV, NAND2) gates are placed instead of (drive1-load-drive2). Those gates are place with the combination of (3-4-3), since nand2 gates are more commonly used than inverters.

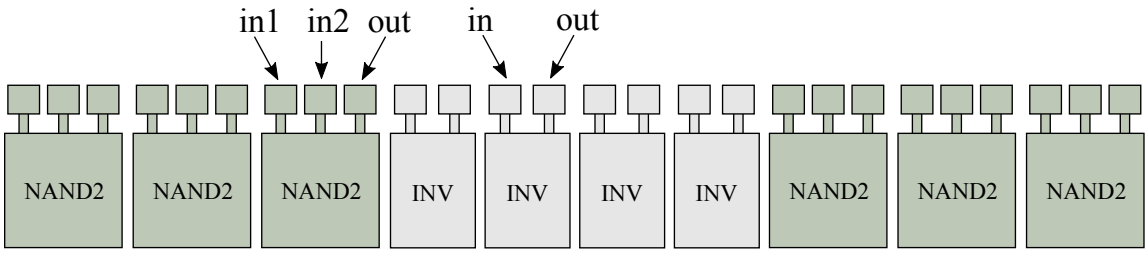


Fig. 6.1 Schematic of the BBC block in the proposed Cell-based IGA bulk

There are several advantages about this IGA style which are listed below.

Firstly, it improves the metallization yield Y_M, which is the number of properly printed drops out of the total number of printed drops:

$$Metallization - yield : Y_M(\%) = 100 \times \frac{N_{GD}}{N_{TD}} \tag{6.1}$$

where N_{GD}, and N_{TD} are the number of good drops and total number of drops, respectively. Metallization is the last step to implement a circuit onto the IGAs, and even if one of the printed drops is objected to any kind of fault, it can let the entire circuit to fail. Therefore, it is important to maximize the metallization yield as much as possible.

As discussed before, the metallization yield is dependent on the DoD interconnection methodology used in the wiring cells of IGA structure, and also the alignment and reliability of the printing technique. In Section 5.2.1, the metallization yield of several digital printing techniques were studied, and it was around $70-97\%$ for line-configurable structures, and 99.99% for drop-configurable structures in good alignment condition. Taking the metallization yield and the required number of drops (N_D) into account, the fabrication yield Y_F is calculated as below:

$$Fabrication - yield : Y_F(\%) = 100 \times (\frac{Y_M}{100})^{N_D} \tag{6.2}$$

This means that there is a chance of obtaining a working foil in the first try or maybe in the millionth try. In order to guarantee that after metallizing "N" number of IGA foils to similar circuit, there is at least *one* foil working properly, we have to calculate how many IGA foils should be metallized (Equation 6.3)

$$N = (\frac{Y_{\mathrm{F}}}{100})^{-1} \tag{6.3}$$

In order to find out how many drops are required onto the IGA bulk for building a particular circuit, one should know the number of transistors, gates, and nodes. We have synthesized some digital logic and benchmarks circuits in respect to two important cost functions: (1) number of transistors, (2) depth levels, which defines the number of gates in the critical path. Only inverter and nand2 gates are used in the library. The synthesised combinational and sequential circuits are the ones that are typically used in most of the printable and flexible electronics applications, such as RFID tags, display row drivers, and etc. Table 6.1 shows the information about target circuits, which are synthesized in respect to the number of transistor as a cost function. Obviously, as the number of transistors is minimized, the required number of drops is also reduced. It also has to be mentioned that DFF is also made of inverter and nand2 gates.

In this table, *Nets* and *Net-loads* are the number of nets in the synthesised circuit, and the total number of loads, respectively. For example, a singular *Nets* might be the intersection of two or more signals (*Net-loads*). In order to count for the required number of drops to build the desired circuit on top of cell-based IGA, one should know *Net-loads* value. As it is seen in the table, some of the PE-oriented circuits for LCD driver and RFID tags exist in the literature, and some of them are proposed in this work, and are being developed. The schematic of the proposed circuits are in the Appendix A.

Table 6.2 compares the required number of drops for building circuits onto the transistor-based IGA with cell-based IGA. The number of drops for both transistor-based IGA and cell-based IGA can be calculated from Equation 6.4 and 6.5.

$$Transistor - based : N_{\mathrm{D}} = 3 \times N_{\mathrm{T}} + X \tag{6.4}$$

$$Cell - based : N_{\mathrm{D}} = N_{\mathrm{Nl}} + Y \tag{6.5}$$

Table 6.1 PE-oriented Benchmark circuits

Circuits	INV	NAND2	DFF	Transistors	Levels	Nets	Net-loads
Decoder 2-to-4	6	4	0	24	4	12	18
Decoder 3-to-8	16	12	0	68	6	31	48
Decoder 4-to-16	28	24	0	128	6	56	92
MUX 2	1	3	0	11	4	7	8
MUX 4	2	9	0	31	6	17	21
MUX 8	7	23	0	83	10	41	54
MUX 16	20	47	0	181	14	87	115
Demux 2	3	2	0	12	4	7	9
Demux 4	8	6	0	34	6	17	24
Demux 8	18	14	0	78	8	36	54
Demux 16	30	26	0	138	8	61	98
SIPO Shift register 4	0	0	4	112	2	7	16
SIPO Shift register 8	0	0	8	224	2	11	32
SIPO Shift register 16	0	0	16	448	2	19	64
Sync. counter 2	8	6	2	90	8	18	28
Sync. counter 3	13	11	3	143	10	29	47
Sync. counter 4	18	16	4	196	12	40	66
LCD row driver [267]	15	12	3	150	3	33	56
LCD driver (counter)	27	25	3	213	9	59	94
LCD driver (demux)	24	23	4	229	10	55	90
LCD driver (shift register)	0	0	8	224	2	11	32
RFID tag (comb.) [268]	37	41	4	309	15	93	140
RFID tag (seq.) [268]	53	41	12	565	15	117	180

where N_{D}, N_{T}, and N_{Nl} are the number of required drops, number of transistors, and number of Net-loads, respectively. X and Y are the number of drops that are required for interconnection of BBC in the rows. Obviously X and Y are negligible comparing to N_{T} and N_{Nl}, and we skip them in the below table.

It can be seen that the required number of drops for metallization of transistor-based IGAs is much higher than the required drops for cell-based IGAs. This can obviously result in increasing the probability of faulty metallization for transistor-based IGAs. Table 6.3 and 6.4 show the minimum number of foils that should be metallized to a similar circuit, in order to guarantee that one can obtain at least one working foil (according to 6.2 and 6.3). The calculations are realized for different metallization yield assumptions for both transistor-based and cell-based IGAs.

It is clear that the required number of cell-based IGA foils to be metallized to similar circuit is far less than the one for transistor-based IGAs. For 99.99% metallization yield, it is almost guaranteed that any of the mentioned circuits can be implemented through the first foil. For 99% metallization yield, the difference between transistor-based IGAs and cell-based IGAs is very practical and deterministic. It can also be concluded that it

Table 6.2 Required number of drops for building the PE-oriented Benchmark circuits onto IGAs

Circuits	Transistors	Net-loads	N_D (transistor-based)	N_D (cell-based)
Decoder 2-to-4	24	18	72	18
Decoder 3-to-8	68	48	204	48
Decoder 4-to-16	128	92	384	92
MUX 2	11	8	33	8
MUX 4	31	21	93	21
MUX 8	83	54	249	54
MUX 16	181	115	543	115
Demux 2	12	9	36	9
Demux 4	34	24	102	24
Demux 8	78	54	234	54
Demux 16	138	98	414	98
SIPO Shift register 4	112	16	336	16
SIPO Shift register 8	224	32	672	32
SIPO Shift register 16	448	64	1344	64
Sync. counter 2	90	28	270	28
Sync. counter 3	143	47	429	47
Sync. counter 4	196	66	588	66
LCD row driver	150	56	450	56
LCD driver (counter)	213	94	639	94
LCD driver (demux)	229	90	687	90
LCD driver (shift register)	224	32	672	32
RFID tag (comb.)	309	140	927	140
RFID tag (seq.)	565	180	1695	180

is almost impossible to wire both types of IGAs by digital printing techniques with yield less than 99%, especially for larger circuits. Consequently, drop-configurable structures are the best candidate to be used in the IGAs´ wire cell. Inkjet printing technique with good alignment condition can offer very high metallization yield, making it the best available alternative for cost-effective customization of cell-based IGAs.

Integration of the full-custom elementary cells into the BBC block allows placing higher number of transistors into the IGA master foil. This is due to the fact that there is no need to use the wire channels for building elementary logic gates but they are already custom designed and pre-fabricated. Obviously, the custom-designed gates will occupy less space than semi-custom made gates in the IGA. Thus, a higher hierarchical level of abstraction can be used, allowing higher circuit density.

A small prototype cell-based IGAs with the same size as the previous IGAs in Figure 5.24 were designed and fabricated. Here, the BBC blocks are made of (3-4-3) gate combination, as shown in Figure 6.2. The V_{DD} and Gnd pins are pre-connected to their corresponding global wires. The inverter and NAND2 gates have testable pads for similar reason to previous IGAs.

Table 6.3 Minimum number of foils metallized to similar circuit in order to guarantee working circuit on transistor-based IGA

Circuits	Transistor-based IGAs				
	70%	80%	90%	99%	99.99%
Decoder 2-to-4	1,42E+11	9,50E+06	1,97E+03	2,06E+00	1,01E+00
Decoder 3-to-8	3,98E+31	5,88E+19	2,16E+09	7,77E+00	1,02E+00
Decoder 4-to-16	3,04E+59	1,63E+37	3,72E+17	4,74E+01	1,04E+00
MUX 2	1,29E+05	1,58E+03	3,24E+01	1,39E+00	1,00E+00
MUX 4	2,55E+14	1,03E+09	1,80E+04	2,55E+00	1,01E+00
MUX 8	3,72E+38	1,35E+24	2,48E+11	1,22E+01	1,03E+00
MUX 16	1,29E+84	4,19E+52	7,02E+24	2,34E+02	1,06E+00
Demux 2	3,77E+05	3,08E+03	4,44E+01	1,44E+00	1,00E+00
Demux 4	6,31E+15	7,67E+09	4,65E+04	2,79E+00	1,01E+00
Demux 8	1,77E+36	4,75E+22	5,10E+10	1,05E+01	1,02E+00
Demux 16	1,35E+64	1,32E+40	8,78E+18	6,41E+01	1,04E+00
SIPO Shift register 4	1,11E+52	3,65E+32	2,37E+15	2,93E+01	1,03E+00
SIPO Shift register 8	1,24E+104	1,33E+65	5,61E+30	8,57E+02	1,07E+00
SIPO Shift register 16	1,54E+208	1,77E+130	3,15E+61	7,35E+05	1,14E+00
Sync. counter 2	6,66E+41	1,46E+26	2,26E+12	1,51E+01	1,03E+00
Sync. counter 3	2,84E+66	3,75E+41	4,27E+19	7,46E+01	1,04E+00
Sync. counter 4	1,21E+91	9,62E+56	8,04E+26	3,69E+02	1,06E+00
LCD row driver	5,08E+69	4,07E+43	3,90E+20	9,21E+01	1,05E+00
LCD driver (counter)	9,60E+98	8,42E+61	1,73E+29	6,15E+02	1,07E+00
LCD driver (demux)	2,62E+106	3,78E+66	2,73E+31	9,97E+02	1,07E+00
LCD driver (shift register)	1,24E+104	1,33E+65	5,61E+30	8,57E+02	1,07E+00
RFID tag (comb.)	3,93E+143	6,85E+89	2,61E+42	1,11E+04	1,10E+00
RFID tag (seq.)	3,62E+262	1,83E+164	3,62E+77	2,50E+07	1,18E+00

Further cell-based IGAs without testable gates have been designed and fabricated, in order to increase the density. The largest designed IGA consists of 28 BBC blocks with 112 inverters and 168 NAND2 gates, which means 728 OTFTs. It occupies $1.7 \times 2.2cm^2 = 3.7cm^2$ space. Table 6.5 provides a comparison of transistor density of cell-based IGAs ($4\mu m$ process) and the IGAs from section 5.3.

Table 6.5 shows that the proposed cell-based IGA increases the circuit density almost three times for similar fabrication process and IGA total size.

Another advantage of the proposed cell-based IGA is the design optimization in respect to time and complexity of functionality implementation. When the number of printing drops that are required for circuit implementation reduces, metallization of IGAs take less time, and consequently, it is simpler to be printed.

The total customization time is the sum of three steps: (1) pre-printing time (T_1), which is the time spent for printer and ink preparation, probable surface treatment, alignment, etc; (2) printing time (T_2), which is the duration of printing drops; (3) post-printing, which is the time spent for cleaning and final treatment.

Table 6.4 Minimum number of foils metallized to similar circuit in order to guarantee working circuit on cell-based IGA

Circuits	Cell-based IGAs				
	70%	80%	90%	99%	99.99%
Decoder 2-to-4	6,14E+02	5,55E+01	6,66E+00	1,20E+00	1,00E+00
Decoder 3-to-8	2,72E+07	4,48E+04	1,57E+02	1,62E+00	1,00E+00
Decoder 4-to-16	1,78E+14	8,24E+08	1,62E+04	2,52E+00	1,01E+00
MUX 2	1,73E+01	5,96E+00	2,32E+00	1,08E+00	1,00E+00
MUX 4	1,79E+03	1,08E+02	9,14E+00	1,23E+00	1,00E+00
MUX 8	2,32E+08	1,71E+05	2,96E+02	1,72E+00	1,01E+00
MUX 16	6,51E+17	1,40E+11	1,83E+05	3,18E+00	1,01E+00
Demux 2	2,48E+01	7,45E+00	2,58E+00	1,09E+00	1,00E+00
Demux 4	5,22E+03	2,12E+02	1,25E+01	1,27E+00	1,00E+00
Demux 8	2,32E+08	1,71E+05	2,96E+02	1,72E+00	1,01E+00
Demux 16	1,51E+15	3,14E+09	3,05E+04	2,68E+00	1,01E+00
SIPO Shift register 4	3,01E+02	3,55E+01	5,40E+00	1,17E+00	1,00E+00
SIPO Shift register 8	9,05E+04	1,26E+03	2,91E+01	1,38E+00	1,00E+00
SIPO Shift register 16	8,20E+09	1,59E+06	8,48E+02	1,90E+00	1,01E+00
Sync. counter 2	2,17E+04	5,17E+02	1,91E+01	1,32E+00	1,00E+00
Sync. counter 3	1,91E+07	3,59E+04	1,41E+02	1,60E+00	1,00E+00
Sync. counter 4	1,67E+10	2,49E+06	1,05E+03	1,94E+00	1,01E+00
LCD row driver	4,73E+08	2,67E+05	3,65E+02	1,76E+00	1,01E+00
LCD driver (counter)	3,64E+14	1,29E+09	2,00E+04	2,57E+00	1,01E+00
LCD driver (demux)	8,73E+13	5,27E+08	1,31E+04	2,47E+00	1,01E+00
LCD driver (shift register)	9,05E+04	1,26E+03	2,91E+01	1,38E+00	1,00E+00
RFID tag (comb.)	4,86E+21	3,69E+13	2,55E+06	4,08E+00	1,01E+00
RFID tag (seq.)	7,63E+27	2,78E+17	1,72E+08	6,10E+00	1,02E+00

T_1, and T_3 are related to the compatibility of materials, and substrates with the printing machinery and is independent of the structure, either transistor-based or cell-based IGA. Thus, T_1, and T_3 are similar for both types of IGA. However, T_2 is strongly dependent on the number of drops that are aimed to be printed. Due to the fact that the number of printing drops is reduced for cell-based IGAs, therefore, T_2, and consequently T_{total} is reduced for cell-based IGAs. This also reduces the complexity of metallization printing and errors in respect to drop alignment.

Finally, the concept of fault tolerance was added to IGA, being used for the cases that the IGA master foils are fabricated by mid-yield printing technologies, such as inkjet or gravure. fault tolerance technique adapts the failure map of the transistor arrays, and connects only Known Good Transistors (KGOs) for building functional circuits. This way, the faulty transistors will be withdrawn from the final circuit, leading to achieve a high yield at circuit-level out of mid-yield at transistor level. Two inkjet printed IGA foils were characterized as a proof of concept, and a 2-bit MUX

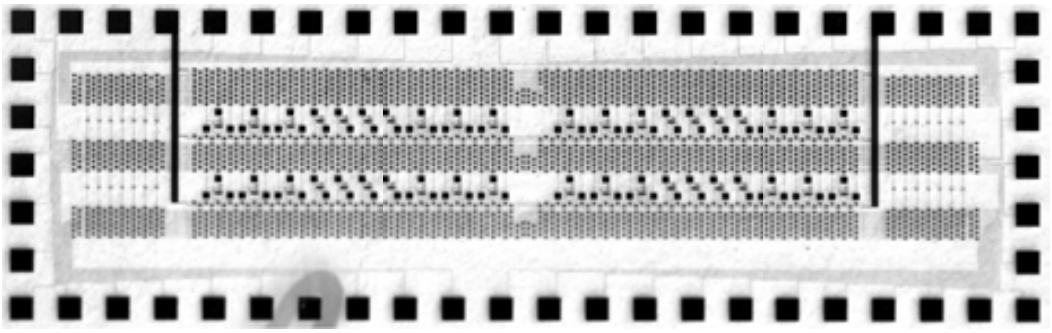


Fig. 6.2 A small prototype of cell-based IGA fabricated by photolithography technology

Table 6.5 Transistor density comparison between IGA and cell-based IGA

	IGA	Cell-based IGA
# Transistors	252	728
Chip area (cm_2)	3.7	3.7
Transistors/cm^2	68	197
(Transistors/cm^2) $L_{\min}$	17	49

circuit was designed on top of the characterized foils, taking their failure map into account.

6.2 Future work

Regarding the full-custom designed circuits, more complex combinational (MUX, Decoder, Encoder, and etc.) and sequential (DFF, Counter, Shift register, and etc.) circuits have been designed and fabricated (shown in AppendixA), opening the door to more complex circuits and targeting the real printed/organic electronics applications. The fabricated devices are being characterized and it is expected to publish the results in early future.

Regarding the IGA and its corresponding structures, several improvements are being realized to optimize the electrical behavior of the final implemented circuits. Firstly, the proposed wire cell in Figure 6.3 shows the initial idea for reducing the parasitic effects of the wiring grid inside the IGA structure. According to the presented results in chapter 4 and 5, there has been a large difference between the full-custom and semi-custom designed circuits, which is due to the resistance and capacitance of the wiring structures inside the IGA. By increasing the wire width, and decreasing the metal overlaps, the RC parasitic effect is expected to reduce, hence improving the circuit performance.

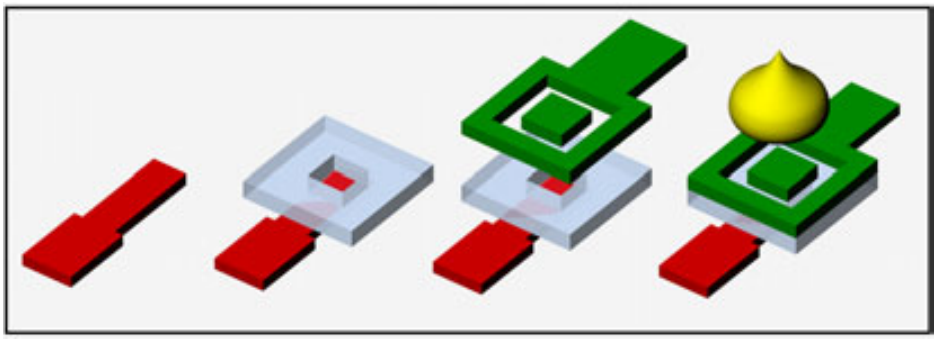


Fig. 6.3 proposed drop-configurable bank structure to reduce parasitic effects

Further improvements in transistor-based and cell-based IGAs are being undertaken and are expected to improve the performance of the final circuit, and also making the IGA foils capable of more complex circuits, addressing some important applications of PE, such as display drivers, RFID tags, and etc.

Another work for my future plan is to focus more on the parameter extraction, and device modelling of the designed and fabricated OTFTs. This will open the door for more complex circuits, specially targeting analog circuits, in which circuit simulation is a key step for performance improvement.

6.3 List of publications

Journals

1. M. Mashayekhi, L. Winchester, L. Evans, T. Pease, M.-M. laurila, M. Mäntysalo, S. Ogier, L. Terés, and J. Carrabina, "Evaluation of aerosol, superfine inkjet, and photolithography printing techniques for metallization of application specific printed electronic circuits", *IEEE Transactions of Electron Devices*, vol. 63, no. 3, pp. 1246-1253, 2016, Impact factor: 2.207

2. J. Carrabina, M. Mashayekhi, J. Pallarès, L. Terés, "Inkjet-configurable Gate Arrays (IGA)", *IEEE Transactions on Emerging Topics in Computing*, Early access, vol. PP, Issue 99, pp. 1-1, 2016. Impact factor: 3.19

3. M. Mashayekhi, A. Conde, T. Ng, P. Mei, E. Ramon, C. Martinez-Domingo, A. Alcalde, L. Terés, J. Carrabina, "Inkjet printing design rules formalization and improvement", *IEEE Journal of Display Technology*, vol. 11, Issue 8, pp. 658-665. 2015, Impact factor: 1.925

4. M. Llamas, M. Mashayekhi, A. Alcalde, J. Pallarès, F. Vila, A. Conde, J. Carrabina, L. Terés, "Development of Digital Application Specific Printed Electronics Circuits: From Specification to Final Prototypes", *IEEE Journal of Display Technology*, vol. 11, Issue 8, pp. 652-657. 2015, Impact factor: 1.925

5. M. Mashayekhi, L. Winchester, M.-M. Laurila, M. Mäntysalo, S. Ogier, L. Terés, J. Carrabina, "Chip-by-Chip Configurable Interconnection using Digital Printing Techniques", *IEEE Transactions of Electron Devices*, Under revision.

Conference presentations and posters

1. M. Mashayekhi, S. Ogier, T. Pease, L. Terés, J. Carrabina, "Comparison of design styles for top-gate bottom-contact OTFTs", *Proceedings of Conference on Design of Circuits and Integrated Systems (DCIS) - IEEE Conference publications*, Nov. 2015, Lisbon, Portugal.

2. M. Mashayekhi, M. Llamas, J. Pallarès, F. Vila, L. Terés, J. Carrabina, "Development of a standard cell library and ASPEC design flow for Organic Thin Film Transistor technology", *Proceedings of Conference on Design of Circuits and Integrated Systems (DCIS) - IEEE Conference publications*, Nov. 2014, Madrid, Spain.

3. M. Mashayekhi, M. Llamas, C. Martinez-Domingo, E. Ramon, J. Pallarès, F. Vila, A. Conde, L. Terés, J. Carrabina, "Formalization of design rules and generation of related structures using pcells", *LOPEC Conference*, 2014, Munich, Germany.

4. M. Mashayekhi, M. Llamas, J. Pallarès, F. Vila, L. Terés, J. Carrabina, "Technology-independent Fault-tolerant Gate Array in Printed Electronics", *International Conference on Computer Aided Design for Thin-Film Transistors - CADTFT*, 2014, China.

5. S. Ogier, M. Simms, M. Mashayekhi, L. Terés, J. Carrabina, "0.5MHz 5 stage ring oscillator circuits and low cost customization technologies for organic logic devices", *Innovations in Large-Area Electronics Conference*, Feb. 2016, Robinson College, cambridge, UK.

6. J. Carrabina, M. Mashayekhi, M. Llamas, T. Pease, M.-M. laurila, M. Mäntysalo, S. Ogier, L. Terés, "Customization technology and tols for building printed

circuits", *Proceedings of 6th International conference on Flexible and Printed Electronics - ICFPE*, 2015, Taipei, Taiwan.

7. M. Llamas, M. Mashayekhi, J. Matos, A. Reis, J. Carrabina, "Optimization on cell-library design for digital Application Specific Printed Electronics Circuits", *Proceedings of International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, 2014, Spain.

8. M. Llamas, M. Mashayekhi, J. Pallarès, F. Vila, L. Terés, J. Carrabina, "A novel ASPEC design flow", *International Conference on Computer Aided Design for Thin-Film Transistors - CADTFT*, 2014, China.

9. M. Llamas, M. Mashayekhi, J. Pallarès, F. Vila, J. Carrabina, L. Terés, "Top-down design flow for application specific printed electronics circuits (ASPECs)", *Proceedings of Conference on Design of Circuits and Integrated Systems (DCIS) - IEEE Conference publications*, Nov. 2014, Madrid, Spain.

10. M. Llamas, M. Mashayekhi, J. Matos, A. Reis, J. Carrabina, "Technology mapping tools for building optimal circuits", *LOPEC Conference*, 2015, Munich, Germany.

Bibliography

[1] G. Moore, "Bcramming more components onto integrated circuits," *Apr*, vol. 19, pp. 114–117, 1965.

[2] R. H. Dennard, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted mosfet's with very small physical dimensions," *Solid-State Circuits, IEEE Journal of*, vol. 9, no. 5, pp. 256–268, 1974.

[3] S. Kunić and Z. Šego, "OLED technology and displays," in *ELMAR, 2012 Proceedings*, IEEE, 2012, pp. 31–35.

[4] T. Tsujimura, T. Hakii, and S. Noda, "A color-tunable polychromatic organic-light-emitting-diode device with low resistive intermediate electrode for roll-to-roll manufacturing," 2015.

[5] C.-L. Fan, Y.-C. Chen, C.-C. Yang, Y.-K. Tsai, and B.-R. Huang, "Novel ltps-tft pixel circuit with oled luminance compensation for 3d amoled displays," *Journal of Display Technology*, vol. 12, no. 5, pp. 425–428, 2016.

[6] J. Shin, S.-W. Baek, S. Lee, M. Kim, J.-Y. Lee, and K. Choi, "Efficient green organic light-emitting diodes by plasmonic silver nanoparticles," 2015.

[7] M. Mizukami, S. Oku, S.-I. Cho, M. Tatetsu, M. Abiko, M. Mamada, T. Sakanoue, Y. Suzuri, J. Kido, and S. Tokito, "A solution-processed organic thin-film transistor backplane for flexible multiphoton emission organic light-emitting diode displays," *Electron Device Letters, IEEE*, vol. 36, no. 8, pp. 841–843, 2015.

[8] K. Ishida, T.-C. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, *et al.*, "Insole pedometer with piezoelectric energy harvester and 2 v organic circuits," *Solid-State Circuits, IEEE Journal of*, vol. 48, no. 1, pp. 255–264, 2013.

[9] L. Grande, V. T. Chundi, D. Wei, C. Bower, P. Andrew, and T. Ryhänen, "Graphene for energy harvesting/storage devices and printed electronics," *Particuology*, vol. 10, no. 1, pp. 1–8, 2012.

[10] W. Cao and J. Xue, "Recent progress in organic photovoltaics: Device architecture and optical design," *Energy & Environmental Science*, vol. 7, no. 7, pp. 2123–2144, 2014.

[11] F. De Rossi, T. M. Brown, and T. Pontecorvo, "Flexible photovoltaics for light harvesting under led lighting," in *Environment and Electrical Engineering (EEEIC), 2015 IEEE 15th International Conference on*, IEEE, 2015, pp. 2100–2103.

[12] T. Meister, K. Ishida, R. Shabanpour, B. K. Boroujeni, C. Carta, F. Ellinger, N. Munzenrieder, L. Petti, G. A. Salvatore, G. Troster, *et al.*, "Bendable energy-harvesting module with organic photovoltaic, rechargeable battery, and a-igzo tft charging electronics," in *Circuit Theory and Design (ECCTD), 2015 European Conference on*, IEEE, 2015, pp. 1–4.

[13] S. Kim, B. Cook, T. Le, J. Cooper, H. Lee, V. Lakafosis, R. Vyas, R. Moro, M. Bozzi, A. Georgiadis, *et al.*, "Inkjet-printed antennas, sensors and circuits on paper substrate," *Microwaves, Antennas & Propagation, IET*, vol. 7, no. 10, pp. 858–868, 2013.

[14] P. Jakimovski, T. Riedel, A. Hadda, and M. Beigl, "Design of a printed organic rfid circuit with an integrated sensor for smart labels," in *Systems, Signals and Devices (SSD), 2012 9th International Multi-Conference on*, IEEE, 2012, pp. 1–6.

[15] R. Ganesan, J. Krumm, S. Pankalla, K. Ludwig, and M. Glesner, "Design of an organic electronic label on a flexible substrate for temperature sensing," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, IEEE, 2013, pp. 423–426.

[16] M. M. Tentzeris, S. Kim, R. Vyas, A. Traille, P. Pons, H. Aubert, A. Georgiadis, and A. Collado, "Inkjet-printed "zero-power" wireless sensor and power management nodes for iot and "smart skin" applications," in *Microwaves, Radar, and Wireless Communication (MIKON), 2014 20th International Conference on*, IEEE, 2014, pp. 1–7.

[17] V. R. Marinov, "Embedded flexible hybrid electronics for the internet of things," in *International Symposium on Microelectronics*, International Microelectronics Assembly and Packaging Society, vol. 2015, 2015, pp. 000 006–000 013.

[18] M. M. Tentzeris, S. Kim, A. Traille, H. Aubert, K. Yoshihiro, A. Georgiadis, and A. Collado, "Inkjet-printed rfid-enabled sensors on paper for iot and "smart skin" applications," in *Applied Electromagnetics and Communications (ICECom), 2013 21st International Conference on*, IEEE, 2013, pp. 1–4.

[19] S. L. Swisher, M. C. Lin, A. Liao, E. J. Leeflang, Y. Khan, F. J. Pavinatto, K. Mann, A. Naujokas, D. Young, S. Roy, *et al.*, "Impedance sensing device enables early detection of pressure ulcers in vivo," *Nature communications*, vol. 6, 2015.

[20] M. Takamiya, H. Fuketa, K. Ishida, T. Yokota, T. Sekitani, T. Someya, and T. Sakurai, "Flexible, large-area, and distributed organic electronics closely contacted with skin for healthcare applications," in *Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on*, IEEE, 2014, pp. 829–832.

[21] J. Smith, B. Katchman, D. Kullman, U. Obahiagbon, Y.-K. Lee, B. O'Brien, G. Raupp, K. Anderson, and J. Blain Christen, "Application of flexible oled display technology to point-of-care medical diagnostic testing,"

[22] J. Smith, E. Bawolek, Y. Lee, B. O'Brien, M. Marrs, E. Howard, M. Strnad, J. Blain Christen, and M. Goryll, "Application of flexible flat panel display technology to wearable biomedical devices," *Electronics Letters*, vol. 51, no. 17, pp. 1312–1314, 2015.

[23] W. Zhu, K. Yao, and Z. Zhang, "Design and fabrication of a novel piezoelectric multilayer actuator by thick-film screen printing technology," *Sensors and Actuators A: Physical*, vol. 86, no. 3, pp. 149–153, 2000.

[24] M. Hambsch, K. Reuter, M. Stanel, G. Schmidt, H. Kempa, U. Fügmann, U. Hahn, and A. Hübler, "Uniformity of fully gravure printed organic field-effect transistors," *Materials Science and Engineering: B*, vol. 170, no. 1, pp. 93–98, 2010.

[25] P. F. Moonen, I. Yakimets, and J. Huskens, "Fabrication of transistors on flexible substrates: From mass-printing to high-resolution alternative lithography strategies," *Advanced materials*, vol. 24, no. 41, pp. 5526–5541, 2012.

[26] *Organic and Printed Electronics Summary OE-A Roadmap, 6th Edition 2015*, http://www.oe-a.org/roadmap, OE-A.

[27] K. Ishida, N. Masunaga, R. Takahashi, T. Sekitani, S. Shino, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "User customizable logic paper (uclp) with sea-of transmission-gates (sotg) of 2-v organic cmos and ink-jet printed interconnects," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 1, pp. 285–292, 2011.

[28] A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, and H. Sirringhaus, "Programmable logic circuits for functional integrated smart plastic systems," *Organic Electronics*, vol. 15, no. 11, pp. 3111–3119, 2014.

[29] K. Myny, S. Smout, M. Rockele, A. Bhoolokam, T. H. Ke, S. Steudel, K. Obata, M. Marinkovic, D.-V. Pham, A. Hoppe, *et al.*, "30.1 8b thin-film microprocessor using a hybrid oxide-organic complementary technology with inkjet-printed p 2 rom memory," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, IEEE, 2014, pp. 486–487.

[30] *Printed Electronics Market worth*, http://www.marketsandmarkets.com/PressReleases/printed-electronics-market.asp, MarketsandMarkets.

[31] *Printed, Organic & Flexible Electronics Forecasts, Players & Opportunities 2016-2026*, http://www.idtechex.com/research/reports/printed-organic-and-flexible-electronics-forecasts-players-and-opportunities-2016-2026-000457.asp?viewopt=desc, IDTechEx.

[32] W. S. Wong and A. Salleo, *Flexible electronics: Materials and applications*. Springer Science & Business Media, 2009, vol. 11.

[33] T. N. Ng, D. E. Schwartz, L. L. Lavery, G. L. Whiting, B. Russo, B. Krusor, J. Veres, P. Bröms, L. Herlogsson, N. Alam, *et al.*, "Scalable printed electronics: An organic decoder addressing ferroelectric non-volatile memory," *Scientific reports*, vol. 2, 2012.

[34] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic nonvolatile memory transistors for flexible sensor arrays," *Science*, vol. 326, no. 5959, pp. 1516–1519, 2009.

[35] S. Brown and J. Rose, "Architecture of fpgas and cplds: A tutorial," *IEEE Design and Test of Computers*, vol. 13, no. 2, pp. 42–57, 1996.

[36] L. Terés, "Head of Integrated Circuits and Systems (ICAS) Group at IMB-CNM, Barcelona-Spain,"

[37] E. Hamdy, J. McCollum, S.-O. Chen, S. Chiang, S. Eltoukhy, J. Chang, T. Speers, and A. Mohsen, "Dielectric based antifuse for logic and memory ics," in *Electron Devices Meeting, 1988. IEDM'88. Technical Digest., International*, IEEE, 1988, pp. 786–789.

[38] J. a. Birkner, A. Chan, H. Chua, A. Chao, K. Gordon, B. Kleinman, P. Kolze, and R. Wong, "A very-high-speed field-programmable gate array using metal-to-metal antifuse programmable elements," *Microelectronics Journal*, vol. 23, no. 7, pp. 561–568, 1992.

[39] D. M. H. Neil H.E. WESTE, *CMOS VLSI Design, a circuit and system perspective*. Addison-Wesley, 2011.

[40] *Xilinx*, http://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale-plus.html, Xilinx Vitix FPGAs.

[41] *Xilinx*, http://www.xilinx.com/products/silicon-devices/fpga/spartan-6.html, Xilinx Spartan FPGAs.

[42] *Altera stratix series*, https://www.altera.com/products/fpga/stratix-series.html, Stratix FPGAs and SOCs.

[43] *Altera*, https://www.altera.com/products/fpga/cyclone-series.html, Altera Cyclone FPGAs.

[44] *Altera*, https://www.altera.com/, Altera FPGAs and SOCs.

[45] *Altera stratix series*, https://www.altera.com/support/support-resources/operation-and-testing/dev-hardcopystx.html, Stratix FPGAs and SOCs.

[46] *Altera APEX 20K device family*, https://www.altera.com/support/support-resources/operation-and-testing/dev-hardcopyapex.html, APEX 20k ASIC family.

[47] *Altera APEX 20K device family*, https://www.altera.com/products/general/devices/apex/overview.html, APEX FPGAs and SOCs.

[48] E. Rhodes, *ASIC Basics: Black and White Edition*. Lulu. com, 2008.

[49] M. Pope and C. E. Swenberg, *Electronic processes in organic crystals and polymers*. Oxford University Press on Demand, 1999.

[50] D. Zielke, A. C. Hübler, U. Hahn, N. Brandt, M. Bartzsch, U. Fügmann, T. Fischer, J. Veres, and S. Ogier, "Polymer-based organic field-effect transistor using offset printed source/drain structures," *Applied Physics Letters*, vol. 87, no. 12, p. 123 508, 2005.

[51] B. Hamadani, D. Gundlach, I. McCulloch, and M. Heeney, "Undoped polythiophene field-effect transistors with mobility of 1 cm2 v-1 s-1," *Applied physics letters*, vol. 91, no. 24, p. 3512, 2007.

[52] H. Sirringhaus, R. Wilson, R. Friend, M. Inbasekaran, W. Wu, E. Woo, M. Grell, and D. Bradley, "Mobility enhancement in conjugated polymer field-effect transistors through chain alignment in a liquid-crystalline phase," *Applied Physics Letters*, vol. 77, no. 3, pp. 406–408, 2000.

[53] G. Wang, J. Swensen, D. Moses, and A. J. Heeger, "Increased mobility from regioregular poly (3-hexylthiophene) field-effect transistors," *Journal of applied physics*, vol. 93, pp. 6137–6141, 2003.

[54] S. K. Park, C.-C. Kuo, J. E. Anthony, and T. N. Jackson, "High mobility solution-processed otfts," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, IEEE, 2005, 4–pp.

[55] S. K. Park, J. E. Anthony, and T. N. Jackson, "Solution-processed tips-pentacene organic thin-film-transistor circuits," *Electron Device Letters, IEEE*, vol. 28, no. 10, pp. 877–879, 2007.

[56] T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith, and T. D. Jones, "High performance organic thin film transistors," in *MRS Proceedings*, Cambridge Univ Press, vol. 771, 2003, pp. L6–5.

[57] H. Tan, B. Wang, S. Kamath, J. Chua, M. Shojaei-Baghini, V. R. Rao, N. Mathews, and S. Mhaisalkar, "Complementary organic circuits using evaporated and inkjet printing of pqt," *Electron Device Letters, IEEE*, vol. 31, no. 11, pp. 1311–1313, 2010.

[58] T. D. Anthopoulos, B. Singh, N. Marjanovic, N. Sariciftci, A. M. Ramil, H. Sitter, M. Colle, and D. M. de Leeuw, "High performance n-channel organic field-effect transistors and ring oscillators based on c60 fullerene films," *Applied Physics Letters*, vol. 89, no. 21, pp. 213 504–213 504, 2006.

[59] B. Kjellander, W. T. Smaal, J. E. Anthony, and G. H. Gelinck, "Inkjet printing of tips-pen on soluble polymer insulating films: A route to high-performance thin-film transistors," *Advanced Materials*, vol. 22, no. 41, pp. 4612–4616, 2010.

[60] J. Smith, W. Zhang, R. Sougrat, K. Zhao, R. Li, D. Cha, A. Amassian, M. Heeney, I. McCulloch, and T. D. Anthopoulos, "Solution-processed small molecule-polymer blend organic thin-film transistors with hole mobility greater than 5 cm2/vs," *Advanced Materials*, vol. 24, no. 18, pp. 2441–2446, 2012.

[61] R. Hamilton, J. Smith, S. Ogier, M. Heeney, J. E. Anthony, I. McCulloch, J. Veres, D. D. Bradley, and T. D. Anthopoulos, "High-performance polymer-small molecule blend organic transistors," *Advanced Materials*, vol. 21, no. 10-11, pp. 1166–1171, 2009.

[62] D. De Leeuw, M. Simenon, A. Brown, and R. Einerhand, "Stability of n-type doped conducting polymers and consequences for polymeric microelectronic devices," *Synthetic Metals*, vol. 87, no. 1, pp. 53–59, 1997.

[63] T. Ashimine, T. Yasuda, M. Saito, H. Nakamura, and T. Tsutsui, "Air stability of p-channel organic field-effect transistors based on oligo-p-phenylenevinylene derivatives," *Japanese Journal of Applied Physics*, vol. 47, no. 3R, p. 1760, 2008.

[64] T. D. Anthopoulos, F. B. Kooistra, H. J. Wondergem, D. Kronholm, J. C. Hummelen, and D. M. de Leeuw, "Air-stable n-channel organic transistors based on a soluble c84 fullerene derivative," *Advanced Materials*, vol. 18, no. 13, pp. 1679–1684, 2006.

[65] C. Drury, C. Mutsaers, C. Hart, M. Matters, and D. De Leeuw, "Low-cost all-polymer integrated circuits," *Applied Physics Letters*, vol. 73, no. 1, pp. 108–110, 1998.

[66] G. Gelinck, T. Geuns, and D. De Leeuw, "High-performance all-polymer integrated circuits," *Applied Physics Letters*, vol. 77, no. 10, pp. 1487–1489, 2000.

[67] K. B. Blodgett and I. Langmuir, "Built-up films of barium stearate and their optical properties," *Physical Review*, vol. 51, no. 11, p. 964, 1937.

[68] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, "Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films," *Applied Physics Letters*, vol. 76, no. 14, pp. 1941–1943, 2000.

[69] Y. Matsuhisa, K. Yamae, H. Tsuji, V. Kittichungchit, N. Ide, and T. Komoda, "Highly efficient oled lighting for eco-solution," in *Microoptics Conference (MOC), 2013 18th*, IEEE, 2013, pp. 1–2.

[70] T. Sauter, W. Hortschitz, H. Steiner, M. Stifter, H. Chiao, H. W. Zan, H.-F. Meng, and P. Chao, "Making optical mems sensors more compact using organic light sources and detectors," in *Emerging Technology and Factory Automation (ETFA)*, IEEE, 2014, pp. 1–4.

[71] M. Koden, "Flexible substrates and non-ito transparent electrodes for organic electronics," in *Active-Matrix Flatpanel Displays and Devices (AM-FPD), 2015 22nd International Workshop on*, IEEE, 2015, pp. 13–16.

[72] R. Soukup, A. Hamáček, and J. Řeboun, "Organic based sensors: Novel screen printing technique for sensing layers deposition," in *Electronics Technology (ISSE), 2012 35th International Spring Seminar on*, IEEE, 2012, pp. 19–24.

[73] S. R. Forrest, "The path to ubiquitous and low-cost organic electronic appliances on plastic," *Nature*, vol. 428, no. 6986, pp. 911–918, 2004.

[74] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, *et al.*, "All-printed and roll-to-roll-printable 13.56-mhz-operated 1-bit rf tag on plastic foils," *Electron Devices, IEEE Transactions on*, vol. 57, no. 3, pp. 571–580, 2010.

[75] J. A. Rogers, Z. Bao, A. Dodabalapur, and A. Makhija, "Organic smart pixels and complementary inverter circuits formed on plastic substrates by casting and rubber stamping," *Electron Device Letters, IEEE*, vol. 21, no. 3, pp. 100–103, 2000.

[76] M. Weaver, L. Michalski, K. Rajan, M. Rothman, J. Silvernail, J. J. Brown, P. E. Burrows, G. L. Graff, M. E. Gross, P. M. Martin, *et al.*, "Organic light-emitting devices with extended operating lifetimes on plastic substrates," *Applied Physics Letters*, vol. 81, no. 16, pp. 2929–2931, 2002.

[77] G. H. Gelinck, A. Kumar, D. Moet, J.-L. P. van Steen, A. J. van Breemen, S. Shanmugam, A. Langen, J. Gilot, P. Groen, R. Andriessen, *et al.*, "X-ray detector-on-plastic with high sensitivity using low cost, solution-processed organic photodiodes," 2016.

[78] M. Kane, J. Campi, M. Hammond, F. Cuomo, B. Greening, C. Sheraw, J. Nichols, D. Gundlach, J. Huang, C. Kuo, *et al.*, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 534–536, 2000.

[79] G. Orecchini, R. Zhang, J. Agar, D. Staiculescu, M. Tentzeris, L. Roselli, and C. Wong, "Inkjet printed organic transistors for sustainable electronics," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, IEEE, 2010, pp. 985–989.

[80] J. Kawahara, P. A. Ersman, K. Katoh, and M. Berggren, "Fast-switching printed organic electrochemical transistors including electronic vias through plastic and paper substrates," *Electron Devices, IEEE Transactions on*, vol. 60, no. 6, pp. 2052–2056, 2013.

[81] B. Kang, W. H. Lee, and K. Cho, "Recent advances in organic transistor printing processes," *ACS applied materials and interfaces*, vol. 5, no. 7, pp. 2302–2315, 2013.

[82] ——, "Recent advances in organic transistor printing processes," *ACS applied materials & interfaces*, vol. 5, no. 7, pp. 2302–2315, 2013.

[83] Y. D. Park, H. S. Lee, Y. J. Choi, D. Kwak, J. H. Cho, S. Lee, and K. Cho, "Solubility-induced ordered polythiophene precursors for high-performance organic thin-film transistors," *Advanced Functional Materials*, vol. 19, no. 8, pp. 1200–1206, 2009.

[84] *Iso 14644-1:2015*, http://www.iso.org/iso/catalogue_detail?csnumber=53394, Cleanroom and associated controlled environments.

[85] B. Päivänranta, A. Langner, E. Kirk, C. David, and Y. Ekinci, "Sub-10 nm patterning using euv interference lithography," *Nanotechnology*, vol. 22, no. 37, p. 375 302, 2011.

[86] J. P. Silverman, "X-ray lithography: Status, challenges, and outlook for 0.13 μm," *Journal of Vacuum Science & Technology B*, vol. 15, no. 6, pp. 2117–2124, 1997.

[87] D. P. Sanders, "Advances in patterning materials for 193 nm immersion lithography," *Chemical reviews*, vol. 110, no. 1, pp. 321–360, 2010.

[88] B. D. Gates, Q. Xu, M. Stewart, D. Ryan, C. G. Willson, and G. M. Whitesides, "New approaches to nanofabrication: Molding, printing, and other techniques," *Chemical reviews*, vol. 105, no. 4, pp. 1171–1196, 2005.

[89] M. Kane, J. Campi, M. Hammond, F. Cuomo, B. Greening, C. Sheraw, J. Nichols, D. Gundlach, J. Huang, C. Kuo, *et al.*, "Analog and digital circuits using organic thin-film transistors on polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, pp. 534–536, 2000.

[90] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "Patterning pentacene organic thin film transistors," *Journal of Vacuum Science & Technology B*, vol. 20, no. 3, pp. 956–959, 2002.

[91] H. S. Hwang, A. Zakhidov, J.-K. Lee, J. A. DeFranco, H. H. Fong, G. G. Malliaras, and C. K. Ober, "Photolithographic patterning in supercritical carbon dioxide: Application to patterned light-emitting devices," in *Flexible Electronics and Displays Conference and Exhibition, 2008*, IEEE, 2008, pp. 1–4.

[92] D. Gundlach, J. Royer, S. Park, S. Subramanian, O. Jurchescu, B. Hamadani, A. Moad, R. Kline, L. Teague, O. Kirillov, *et al.*, "Contact-induced crystallinity for high-performance soluble acene-based transistors and circuits," *Nature materials*, vol. 7, no. 3, pp. 216–221, 2008.

[93] M. Péter, F. Furthner, J. Deen, W. J. de Laat, and E. R. Meinders, "Lithographic patterning of metals on flexible plastic foils," *Thin Solid Films*, vol. 517, no. 10, pp. 3081–3086, 2009.

[94] Y.-Y. Lin, D. Gundlach, S. Nelson, and T. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics," *IEEE Electron Device Letters*, vol. 18, no. 12, pp. 606–608, 1997.

[95] K. L. McCall, S. D. Ogier, B. A. Brown, S. R. Rutter, M. Palumbo, Y. U. Lee, L. A. Evans, and T. J. Pease, "Low voltage high mobility organic semiconductors for flexible display applications," in *IDW Proceedings*, 2012.

[96] F. C. Krebs, J. Fyenbo, and M. Jørgensen, "Product integration of compact roll-to-roll processed polymer solar cell modules: Methods and manufacture using flexographic printing, slot-die coating and rotary screen printing," *Journal of Materials Chemistry*, vol. 20, no. 41, pp. 8994–9001, 2010.

[97] D. R. Gamota, P. Brazis, K. Kalyanasundaram, and J. Zhang, *Printed organic and molecular electronics*. Springer Science & Business Media, 2013.

[98] J. B.-H. Tok and Z. Bao, "Recent advances in flexible and stretchable electronics, sensors and power sources," *Science China Chemistry*, vol. 55, no. 5, pp. 718–725, 2012.

[99] T. Mäkelä, T. Haatainen, P. Majander, and J. Ahopelto, "Continuous roll to roll nanoimprinting of inherently conducting polyaniline," *Microelectronic engineering*, vol. 84, no. 5, pp. 877–879, 2007.

[100] M. K. Kwak, K. H. Shin, E. Y. Yoon, and K. Y. Suh, "Fabrication of conductive metal lines by plate-to-roll pattern transfer utilizing edge dewetting and flexographic printing," *Journal of colloid and interface science*, vol. 343, no. 1, pp. 301–305, 2010.

[101] X. Yin and S. Kumar, "Flow visualization of the liquid emptying process in scaled-up gravure grooves and cells," *Chemical engineering science*, vol. 61, no. 4, pp. 1146–1156, 2006.

[102] Z. Dirk, C. H. Arved, H. Ulrich, B. Nicole, B. Matthias, F. Uta, F. Thomas, V. Janos, and O. Simon, "Polymer-based organic field-effect transistor using offset printed source/drain structures," *Applied Physics Letters*, vol. 87, no. 12, 2005.

[103] N. Choi, H. Wee, S. Nam, J. Lavelle, and M. Hatalis, "A modified offset roll printing for thin film transistor applications," *Microelectronic Engineering*, vol. 91, pp. 93–97, 2012.

[104] G. A. Jones, "Printers' national environmental assistance center,"

[105] R. Søndergaard, M. Hösel, D. Angmo, T. T. Larsen-Olsen, and F. C. Krebs, "Roll-to-roll fabrication of polymer solar cells," *Materials today*, vol. 15, no. 1, pp. 36–49, 2012.

[106] S. E. Shaheen, R. Radspinner, N. Peyghambarian, and G. E. Jabbour, "Fabrication of bulk heterojunction plastic solar cells by screen printing," *Applied Physics Letters*, vol. 79, no. 18, pp. 2996–2998, 2001.

[107] D. A. Pardo, G. E. Jabbour, and N. Peyghambarian, "Application of screen printing in the fabrication of organic light-emitting devices," *Advanced Materials*, vol. 12, no. 17, pp. 1249–1252, 2000.

[108] F. C. Krebs, J. Alstrup, H. Spanggaard, K. Larsen, and E. Kold, "Production of large-area polymer solar cells by industrial silk screen printing, lifetime considerations and lamination with polyethyleneterephthalate," *Solar energy materials and solar cells*, vol. 83, no. 2, pp. 293–300, 2004.

[109] I. E. H. El Jazairi, T. Trigaud, and J.-P. Moliton, "Otft with silk screen printed drain and source," *Micro and Nanosystems*, vol. 1, no. 1, pp. 46–49, 2009.

[110] M. Guerin, A. Daami, S. Jacob, E. Bergeret, E. Benevent, P. Pannier, and R. Coppard, "High-gain fully printed organic complementary circuits on flexible plastic foils," *IEEE transactions on electron devices*, vol. 58, no. 10, pp. 3587–3593, 2011.

[111] X. Ji, P. M. Hallam, S. M. Houssein, R. Kadara, L. Lang, and C. E. Banks, "Printable thin film supercapacitors utilizing single crystal cobalt hydroxide nanosheets," *RSC Advances*, vol. 2, no. 4, pp. 1508–1515, 2012.

[112] H. Sirringhaus, T. Kawase, R. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. Woo, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, 2000.

[113] T. Kawase, H. Sirringhaus, R. H. Friend, T. Shimoda, *et al.*, "Inkjet printed via-hole interconnections and resistors for all-polymer transistor circuits," *Advanced Materials*, vol. 13, no. 21, p. 1601, 2001.

[114] T. Sekitani, Y. Noguchi, U. Zschieschang, H. Klauk, and T. Someya, "Organic transistors manufactured using inkjet technology with subfemtoliter accuracy," *Proceedings of the National Academy of Sciences*, vol. 105, no. 13, pp. 4976–4980, 2008.

[115] T. N. Ng, B. Russo, B. Krusor, R. Kist, and A. C. Arias, "Organic inkjet-patterned memory array based on ferroelectric field-effect transistors," *Organic Electronics*, vol. 12, no. 12, pp. 2012–2018, 2011.

[116] D. Redinger, S. Molesa, S. Yin, R. Farschi, and V. Subramanian, "An ink-jet-deposited passive component process for rfid," *IEEE transactions on electron devices*, vol. 51, no. 12, pp. 1978–1983, 2004.

[117] S. E. Molesa, S. K. Volkman, D. R. Redinger, A. F. Vornbrock, and V. Subramanian, "A high-performance all-inkjetted organic transistor technology," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, IEEE, 2004, pp. 1072–1074.

[118] S. Chung, J. Jang, J. Cho, C. Lee, S.-K. Kwon, and Y. Hong, "All-inkjet-printed organic thin-film transistors with silver gate, source/drain electrodes," *Japanese Journal of Applied Physics*, vol. 50, no. 3S, 03CB05, 2011.

[119] E. Ramon, "Inkjet printed microelectronic devices and circuits," PhD thesis, Universidad Autònoma de Barcelona, 2014.

[120] M. Singh, H. M. Haverinen, P. Dhagat, and G. E. Jabbour, "Inkjet printing—process and its applications," *Advanced materials*, vol. 22, no. 6, pp. 673–685, 2010.

[121] H. Sirringhaus, T. Kawase, R. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. Woo, "High-resolution inkjet printing of all-polymer transistor circuits," *Science*, vol. 290, no. 5499, pp. 2123–2126, 2000.

[122] T. Hebner, C. Wu, D. Marcy, M. Lu, and J. Sturm, "Ink-jet printing of doped polymers for organic light emitting devices," *Applied Physics Letters*, vol. 72, no. 5, pp. 519–521, 1998.

[123] Y. Gizachew, L. Escoubas, J. Simon, M. Pasquinelli, J. Loiret, P. Leguen, J. Jimeno, J. Martin, A. Apraiz, and J. Aguerre, "Towards ink-jet printed fine line front side metallization of crystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, S70–S82, 2011.

[124] M. F. van Hest, S. E. Habas, J. M. Underwood, R. M. Pasquarelli, P. Hersh, A. Miedaner, C. J. Curtis, and D. S. Ginley, "Direct write metallization for photovoltaic cells and scaling thereof," in *Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE*, IEEE, 2010, pp. 003 626–003 628.

[125] D.-H. Lee, S.-Y. Han, G. S. Herman, and C.-h. Chang, "Inkjet printed high-mobility indium zinc tin oxide thin film transistors," *Journal of Materials Chemistry*, vol. 19, no. 20, pp. 3135–3137, 2009.

[126] V. Pekkanen, M. Mäntysalo, K. Kaija, P. Mansikkamäki, E. Kunnari, K. Laine, J. Niittynen, S. Koskinen, E. Halonen, and U. Caglar, "Utilizing inkjet printing to fabricate electrical interconnections in a system-in-package," *Microelectronic Engineering*, vol. 87, no. 11, pp. 2382–2390, 2010.

[127] L. Xie, G. Yang, M. Mantysalo, L.-L. Xu, F. Jonsson, and L.-R. Zheng, "Heterogeneous integration of bio-sensing system-on-chip and printed electronics," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 4, pp. 672–682, 2012.

[128] K. Myny, S. Smout, M. Rockelé, A. Bhoolokam, T. H. Ke, S. Steudel, B. Cobb, A. Gulati, F. G. Rodriguez, K. Obata, *et al.*, "A thin-film microprocessor with inkjet print-programmable memory," *Scientific reports*, vol. 4, p. 7398, 2014.

[129] K. Myny, S. Smout, M. Rockelé, A. Bhoolokam, T. H. Ke, S. Steudel, K. Obata, M. Marinkovic, D.-V. Pham, A. Hoppe, *et al.*, "30.1 8b thin-film microprocessor using a hybrid oxide-organic complementary technology with inkjet-printed p 2 rom memory," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, IEEE, 2014, pp. 486–487.

[130] T. N. Ng, D. E. Schwartz, L. L. Lavery, G. L. Whiting, B. Russo, B. Krusor, J. Veres, P. Bröms, L. Herlogsson, N. Alam, *et al.*, "Scalable printed electronics: An organic decoder addressing ferroelectric non-volatile memory," *Scientific reports*, vol. 2, p. 585, 2012.

[131] H. Kipphan, *Handbook of print media: Technologies and production methods*. Springer Science & Business Media, 2001.

[132] D. A. Herron, *Continuous ink jet printer*, US Patent 4,636,808, Jan. 1987.

[133] J. Mei, M. R. Lovell, and M. H. Mickle, "Formulation and processing of novel conductive solution inks in continuous inkjet printing of 3-d electric circuits," *IEEE transactions on electronics packaging manufacturing*, vol. 28, no. 3, pp. 265–273, 2005.

[134] J. Heilmann and U. Lindqvist, "Effect of drop size on the print quality in continuous ink jet printing," *Journal of Imaging Science and Technology*, vol. 44, no. 6, pp. 491–494, 2000.

[135] W. Tang, Y. Chen, J. Zhao, S. Chen, L. Feng, and X. Guo, "Inkjet printing narrow fine ag lines on surface modified polymeric films," in *Nano/Micro Engineered and Molecular Systems (NEMS), 2013 8th IEEE International Conference on*, IEEE, 2013, pp. 1171–1174.

[136] S. Mishra, K. L. Barton, A. G. Alleyne, P. M. Ferreira, and J. A. Rogers, "High-speed and drop-on-demand printing with a pulsed electrohydrodynamic jet," *Journal of Micromechanics and Microengineering*, vol. 20, no. 9, p. 095 026, 2010.

[137] P. V. Raje and N. C. Murmu, "A review on electrohydrodynamic-inkjet printing technology,"

[138] K.-H. Choi, A. Khan, H.-C. Kim, K. Rahman, K.-R. Kwon, N. M. Muhammad, and Y.-H. Doh, *Electrohydrodynamic inkjet-micro pattern fabrication for printed electronics applications*. INTECH Open Access Publisher, 2011.

[139] K. Wang, M. D. Paine, and J. P. Stark, "Fully voltage-controlled electrohydrodynamic jet printing of conductive silver tracks with a sub-100 μm linewidth," *Journal of applied physics*, vol. 106, no. 2, p. 024 907, 2009.

[140] K. Wang and J. P. Stark, "Direct fabrication of electrically functional microstructures by fully voltage-controlled electrohydrodynamic jet printing of silver nano-ink," *Applied Physics A*, vol. 99, no. 4, pp. 763–766, 2010.

[141] D.-H. Youn, S.-H. Kim, Y.-S. Yang, S.-C. Lim, S.-J. Kim, S.-H. Ahn, H.-S. Sim, S.-M. Ryu, D.-W. Shin, and J.-B. Yoo, "Electrohydrodynamic micropatterning of silver ink using near-field electrohydrodynamic jet printing with tilted-outlet nozzle," *Applied Physics A*, vol. 96, no. 4, pp. 933–938, 2009.

[142] D.-Y. Lee, J.-C. Lee, Y.-S. Shin, S.-E. Park, T.-U. Yu, Y.-J. Kim, and J. Hwang, "Structuring of conductive silver line by electrohydrodynamic jet printing and its electrical characterization," in *Journal of physics: Conference series*, IOP Publishing, vol. 142, 2008, p. 012 039.

[143] J.-U. Park, M. Hardy, S. J. Kang, K. Barton, K. Adair, D. kishore Mukhopadhyay, C. Y. Lee, M. S. Strano, A. G. Alleyne, J. G. Georgiadis, *et al.*, "High-resolution electrohydrodynamic jet printing," *Nature materials*, vol. 6, no. 10, pp. 782–789, 2007.

[144] K. Murata, "Super-fine ink-jet printing for nanotechnology," in *MEMS, NANO and Smart Systems, 2003. Proceedings. International Conference on*, IEEE, 2003, pp. 346–349.

[145] K. Murata, J. Matsumoto, A. Tezuka, Y. Matsuba, and H. Yokoyama, "Super-fine ink-jet printing: Toward the minimal manufacturing system," *Microsystem technologies*, vol. 12, no. 1-2, pp. 2–7, 2005.

[146] K. Murata, "Direct fabrication of super-fine wiring and bumping by using inkjet process," in *Polytronic 2007-6th International Conference on Polymers and Adhesives in Microelectronics and Photonics*, IEEE, 2007, pp. 293–296.

[147] ——, *Ultrafine fluid jet apparatus*, US Patent 7,434,912, Oct. 2008.

[148] M.-M. Laurila, "Super inkjet printed redistribution layer for a MEMS device," Master's thesis, Tampere University of Technology, 2015.

[149] *Optomec official website*, http://www.optomec.com, Optomec.

[150] T. Seifert, E. Sowade, F. Roscher, M. Wiemer, T. Gessner, and R. R. Baumann, "Additive manufacturing technologies compared: Morphology of deposits of silver ink using inkjet and aerosol jet printing," *Industrial & Engineering Chemistry Research*, vol. 54, no. 2, pp. 769–779, 2015.

[151] C. Goth, S. Putzo, and J. Franke, "Aerosol jet printing on rapid prototyping materials for fine pitch electronic applications," in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, IEEE, 2011, pp. 1211–1216.

[152] P. K. Weimer, "The tft a new thin-film transistor," *Proceedings of the IRE*, vol. 50, no. 6, pp. 1462–1469, 1962.

[153] P. Le Comber, W. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electronics Letters*, vol. 6, no. 15, pp. 179–181, 1979.

[154] A. Tsumura, H. Koezuka, and T. Ando, "Macromolecular electronic device: Field-effect transistor with a polythiophene thin film," *Applied Physics Letters*, vol. 49, no. 18, pp. 1210–1212, 1986.

[155] H. Sirringhaus, P. Brown, R. Friend, M. M. Nielsen, K. Bechgaard, B. Langeveld-Voss, A. Spiering, R. A. Janssen, E. Meijer, P. Herwig, *et al.*, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, no. 6754, pp. 685–688, 1999.

[156] M. L. Chabinyc and A. Salleo, "Materials requirements and fabrication of active matrix arrays of organic thin-film transistors for displays," *Chemistry of materials*, vol. 16, no. 23, pp. 4509–4521, 2004.

[157] I. Kymissis, *Organic Field Effect Transistors: Theory, Fabrication and Characterization*. Springer Science & Business Media, 2008.

[158] P. Necliudov, M. Shur, D. Gundlach, and T. Jackson, "Modeling of organic thin film transistors of different designs," *Journal of applied Physics*, vol. 88, no. 11, pp. 6594–6597, 2000.

[159] C.-H. Shim, F. Maruoka, and R. Hattori, "Structural analysis on organic thin-film transistor with device simulation," *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 195–200, 2010.

[160] D. Gupta, M. Katiyar, and D. Gupta, "An analysis of the difference in behavior of top and bottom contact organic thin film transistors using device simulation," *Organic Electronics*, vol. 10, no. 5, pp. 775–784, 2009.

[161] D. Gundlach, L. Zhou, J. Nichols, T. Jackson, P. Necliudov, and M. Shur, "An experimental study of contact effects in organic thin film transistors," *Journal of Applied Physics*, vol. 100, no. 2, p. 024 509, 2006.

[162] D. Gundlach, J. Royer, S. Park, S. Subramanian, O. Jurchescu, B. Hamadani, A. Moad, R. Kline, L. Teague, O. Kirillov, *et al.*, "Contact-induced crystallinity for high-performance soluble acene-based transistors and circuits," *Nature materials*, vol. 7, no. 3, pp. 216–221, 2008.

[163] D. Kumaki, T. Umeda, and S. Tokito, "Reducing the contact resistance of bottom-contact pentacene thin-film transistors by employing a moox carrier injection layer," *Applied Physics Letters*, vol. 92, no. 1, pp. 13 301–13 301, 2008.

[164] B. Stadlober, U. Haas, H. Gold, A. Haase, G. Jakopic, G. Leising, N. Koch, S. Rentenberger, and E. Zojer, "Orders-of-magnitude reduction of the contact resistance in short-channel hot embossed organic thin film transistors by oxidative treatment of au-electrodes," *Advanced functional materials*, vol. 17, no. 15, pp. 2687–2692, 2007.

[165] F.-C. Chen, Y.-S. Lin, T.-H. Chen, and L.-J. Kung, "Efficient hole-injection in highly transparent organic thin-film transistors," *Electrochemical and solid-state letters*, vol. 10, no. 6, H186–H188, 2007.

[166] D. Gundlach, T. Jackson, D. Schlom, and S. Nelson, "Solvent-induced phase transition in thermally evaporated pentacene films," *Applied Physics Letters*, vol. 74, no. 22, pp. 3302–3304, 1999.

[167] T. Richards and H. Sirringhaus, "Analysis of the contact resistance in staggered, top-gate organic field-effect transistors," *Journal of Applied Physics*, vol. 102, no. 9, p. 094 510, 2007.

[168] I. 1620, *IEEE standard test methods for characterization of organic transistors and materials*, 2004.

[169] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. N. Jackson, "Contact resistance in organic thin film transistors," *Solid-State Electronics*, vol. 47, no. 2, pp. 297–301, 2003.

[170] A. Petrović, E. Pavlica, G. Bratina, A. Carpentiero, and M. Tormen, "Contact resistance in organic thin film transistors," *Synthetic Metals*, vol. 159, no. 12, pp. 1210–1214, 2009.

[171] J. Zaumseil, K. W. Baldwin, and J. A. Rogers, "Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination," *Journal of Applied Physics*, vol. 93, no. 10, pp. 6117–6124, 2003.

[172] P. Servati, D. Striakhilev, and A. Nathan, "Above-threshold parameter extraction and modeling for amorphous silicon thin-film transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 11, pp. 2227–2235, 2003.

[173] A. Valletta, A. Daami, M. Benwadih, R. Coppard, G. Fortunato, M. Rapisarda, F. Torricelli, and L. Mariucci, "Contact effects in high performance fully printed p-channel organic thin film transistors," *Applied Physics Letters*, vol. 99, no. 23, p. 233 309, 2011.

[174] M. Shur, M. Hack, and J. G. Shaw, "A new analytic model for amorphous silicon thin-film transistors," *Journal of applied physics*, vol. 66, no. 7, pp. 3371–3380, 1989.

[175] H. Sirringhaus, N. Tessler, D. Thomas, P. Brown, and R. Friend, "High-mobility conjugated polymer field-effect transistors," in *Advances in Solid State Physics 39*, Springer, 1999, pp. 101–110.

[176] I. Kymissis, *Organic Field Effect Transistors: Theory, Fabrication and Characterization*. Springer Science & Business Media, 2008.

[177] W. Brütting, *Physics of organic semiconductors*. John Wiley & Sons, 2006.

[178] A. Dodabalapur, "Organic and polymer transistors for electronics," *Materials Today*, vol. 9, no. 4, pp. 24–30, 2006.

[179] H. Klauk, "Organic thin-film transistors," *Chemical Society Reviews*, vol. 39, no. 7, pp. 2643–2666, 2010.

[180] C. Reese, M. Roberts, M.-m. Ling, and Z. Bao, "Organic thin film transistors," *Materials today*, vol. 7, no. 9, pp. 20–27, 2004.

[181] C. D. Dimitrakopoulos and D. J. Mascaro, "Organic thin-film transistors: A review of recent advances," *IBM Journal of Research and Development*, vol. 45, no. 1, pp. 11–27, 2001.

[182] S. Abdinia, T.-H. Ke, M. Ameys, J. Li, S. Steudel, J. Vandersteen, B. Cobb, F. Torricelli, A. van Roermund, and E. Cantatore, "Organic cmos line drivers on foil," *Journal of Display Technology*, vol. 11, no. 6, pp. 564–569, 2015.

[183] J. Yuan and C. Svensson, "High-speed cmos circuit technique," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, 1989.

[184] S. Jacob, S. Abdinia, M. Benwadih, J. Bablet, I. Chartier, R. Gwoziecki, E. Cantatore, A. Van Roermund, L. Maddiona, F. Tramontana, *et al.*, "High performance printed n and p-type otfts enabling digital and analog complementary circuits on flexible plastic substrate," *Solid-State Electronics*, vol. 84, pp. 167–178, 2013.

[185] R. Sharma and S. Verma, "Comparitive analysis of static and dynamic cmos logic design," in *IEEE International Conference on Computing and Communication Technologies*, 2011, pp. 231–4.

[186] E. Cantatore and E. Meijer, "Transistor operation and circuit performance in organic electronics," in *Solid-State Circuits Conference, 2003. ESSCIRC'03. Proceedings of the 29th European*, IEEE, 2003, pp. 29–36.

[187] G. Gelinck, E. Van Veenendaal, and R. Coehoorn, "Dual-gate organic thin-film transistors," *Applied Physics Letters*, vol. 87, no. 7, p. 073 508, 2005.

[188] K. Myny, M. J. Beenhakkers, N. A. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Unipolar organic transistor circuits made robust by dual-gate technology," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1223–1230, 2011.

[189] V. Fiore, P. Battiato, S. Abdinia, S. Jacobs, I. Chartier, R. Coppard, G. Klink, E. Cantatore, E. Ragonese, and G. Palmisano, "An integrated 13.56-mhz rfid tag in a printed organic complementary tft technology on flexible substrate," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 6, pp. 1668–1677, 2015.

[190] M. Guerin, E. Bergeret, E. Benevent, P. Pannier, A. Daami, S. Jacob, I. Chartier, and R. Coppard, "Design of organic complementary circuits for rfid tags application," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, 2012.

[191] P. Jakimovski, T. Riedel, A. Hadda, and M. Beigl, "Design of a printed organic rfid circuit with an integrated sensor for smart labels," in *Systems, Signals and Devices (SSD), 2012 9th International Multi-Conference on*, IEEE, 2012, pp. 1–6.

[192] H. Marien, M. S. Steyaert, E. Van Veenendaal, and P. Heremans, "Analog building blocks for organic smart sensor systems in organic thin-film transistor technology on flexible plastic foil," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 7, pp. 1712–1720, 2012.

[193] H. Marien, M. Steyaert, N. van Aerle, and P. Heremans, "An analog organic first-order CT $\Delta\Sigma$ ADC on a flexible plastic substrate with 26.5 db precision," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*, IEEE, 2010, pp. 136–137.

[194] R. Wanjau, D. Donaghy, and M. Raja, "Design of a high gain organic comparator for use in low-cost smart sensor systems," in *Ph. D. Research in Microelectronics and Electronics (PRIME), 2015 11th Conference on*, IEEE, 2015, pp. 37–40.

[195] K. Myny, E. Van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 1, pp. 284–291, 2012.

[196] K. Myny, S. Smout, M. Rockelé, A. Bhoolokam, T. H. Ke, S. Steudel, B. Cobb, A. Gulati, F. G. Rodriguez, K. Obata, *et al.*, "A thin-film microprocessor with inkjet print-programmable memory," *Scientific reports*, vol. 4, p. 7398, 2014.

[197] D. D. He, I. A. Nausieda, K. K. Ryu, A. I. Akinwande, V. Bulovic, and C. G. Sodini, "An integrated organic circuit array for flexible large-area temperature sensing," Institute of Electrical and Electronics Engineers, 2010.

[198] D. Raiteri, P. van Lieshout, A. van Roermund, and E. Cantatore, "Positive-feedback level shifter logic for large-area electronics," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 2, pp. 524–535, 2014.

[199] S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, *et al.*, "Variation-based design of an am demodulator in a printed complementary organic technology," *Organic Electronics*, vol. 15, no. 4, pp. 904–912, 2014.

[200] S. G. Uppili, D. R. Allee, S. M. Venugopal, L. T. Clark, and R. Shringarpure, "Standard cell library and automated design flow for circuits on flexible substrates," in *Flexible Electronics Displays Conference and Exhibition*, 2009.

[201] T. C. Huang and K. T. Cheng, "Design for low power and reliable flexible electronics: Self-tunable cell-library design," *Journal of Display Technology*, vol. 5, no. 6, pp. 206–215, 2009.

[202] K. Myny, S. Smout, M. Rockelé, A. Bhoolokam, T. H. Ke, S. Steudel, K. Obata, M. Marinkovic, D.-V. Pham, A. Hoppe, *et al.*, "30.1 8b thin-film microprocessor using a hybrid oxide-organic complementary technology with inkjet-printed p 2 rom memory," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, IEEE, 2014, pp. 486–487.

[203] M. Rockelé, D.-V. Pham, J. Steiger, S. Botnaras, D. Weber, J. Vanfleteren, T. Sterken, D. Cuypers, S. Steudel, K. Myny, *et al.*, "Solution-processed and low-temperature metal oxide n-channel thin-film transistors and low-voltage complementary circuitry on large-area flexible polyimide foil," *Journal of the Society for Information Display*, vol. 20, no. 9, pp. 499–507, 2012.

[204] A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, and H. Sirringhaus, "Programmable logic circuits for functional integrated smart plastic systems," *Organic Electronics*, vol. 15, no. 11, pp. 3111–3119, 2014.

[205] P. Too, H. Vandekerckhove, G. Fichet, M. J. Harding, and M. J. Banach, "Recent advances in the reliability of otfts," in *SPIE Organic Photonics+ Electronics*, International Society for Optics and Photonics, 2012, pp. 847 807–847 807.

[206] S. Burns, K. Reynolds, W. Reeves, M. Banach, T. Brown, K. Chalmers, N. Cousins, M. Etchells, C. Hayton, K. Jacobs, *et al.*, "A scalable manufacturing process for flexible active-matrix e-paper displays," *Journal of the Society for Information Display*, vol. 13, no. 7, pp. 583–586, 2005.

[207] E. Ramon, C. Martínez-Domingo, A. Alcalde-Aragonés, J. Carrabina, A. Conde, J. Pallarés, and L. Terés, "Large-scale fabrication of all-inkjet printed organic thin film transistors: A quantitative study," in *NIP & Digital Fabrication Conference*, Society for Imaging Science and Technology, vol. 2014, 2014, pp. 455–460.

[208] M. E. Beahm, T. I. Chappell, and R. V. Joshi, *Parameterized cells for generating dense layouts of vlsi circuits*, US Patent 5,920,486, Jul. 1999.

[209] A. Conde, J. Pallarès, L. Terés, C. Martínez, E. Ramon, and J. Carrabina, "Pcell based devices & structures for printed electronics and related semiautomatic characterization loop," in *Proceedings of the XVIII Conference on the Design of Circuits and Integrated Systems*, 2013.

[210] *Python programming language*, http://www.python.org.

[211] *K. sabine*, http://www.peardrop.co.uk, Glade IC Layout Editor.

[212] C. Mead and L. Conway, *Introduction to VLSI systems*. Addison-Wesley Reading, MA, 1980, vol. 1080.

[213] D. Soltman and V. Subramanian, "Inkjet-printed line morphologies and temperature control of the coffee ring effect," *Langmuir*, vol. 24, no. 5, pp. 2224–2231, 2008.

[214] B. J. Kang and J. H. Oh, "Geometrical characterization of inkjet-printed conductive lines of nanosilver suspensions on a polymer substrate," *Thin Solid Films*, vol. 518, no. 10, pp. 2890–2896, 2010.

[215] E. Ramon, C. Martínez-Domingo, and J. Carrabina, "Geometric design and compensation rules generation and characterization for all-inkjet-printed organic thin film transistors," *Journal of Imaging Science and Technology*, vol. 57, no. 4, pp. 40 402–1, 2013.

[216] *Fujifilm Dimatix DMP-2831*, http://www.fujifilmusa.com/products/industrial_inkjet_printheads/deposition-products/dmp-2800/.

[217] *Fraunhofer ENAS Printed Functionalities*, http://www.enas.fraunhofer.de/en/departments/PF.html.

[218] *Summit Semi-automated Probe System*, https://www.cascademicrotech.com/products/probe-systems/200mm-wafer/summit.

[219] F. Vila, J. Pallarès, E. Ramon, and L. Terés, "A systematic study of pattern compensation methods for all-inkjet printing processes,"

[220] M. Mashayekhi, A. Conde, T. N. Ng, P. Mei, E. Ramon, C. Martinez-Domingo, A. Alcalde, L. Terés, and J. C. Bordoll, "Inkjet printing design rules formalization and improvement," *Journal of Display Technology*, vol. 11, no. 8, pp. 658–665, 2015.

[221] *Fujifilm Dimatix DMP-3000*, http://www.fujifilmusa.com/press/news/display_news?newsID=880182.

[222] M. Pecht, *Handbook of electronic package design*. CRC Press, 1991, vol. 76.

[223] M. Mashayekhi, S. Ogier, T. Pease, L. Teres, *et al.*, "Comparison of design styles for top-gate bottom-contact otfts," in *Design of Circuits and Integrated Systems (DCIS), 2015 Conference on*, IEEE, 2015, pp. 1–9.

[224] *Phoenix software*, http://www.phoenixbv.com/product.php?prodid=777&submenu=dfa&prdgrpID=2&prodname=MaskEngineer, MaskEngineer: Solution for micro and nano technologies.

[225] *Centre for Process Innovation*, https://www.uk-cpi.com/printable-electronics/, CPI, NETPark National Printable Electronics Centre, Durham-UK.

[226] *NeuDrive Limited*, http://neudrive-public.sharepoint.com/, Macclesfield, Cheshire-UK.

[227] C. P. Watson, B. A. Brown, J. Carter, J. Morgan, and D. M. Taylor, "Organic ring oscillators with sub-200 ns stage delay based on a solution-processed p-type semiconductor blend," *Advanced Electronic Materials*, 2016.

[228] M. B. Das and R. D. Josephy, *High frequency, high power igfet with interdigital electrodes and plural looped gate*, US Patent 3,586,930, Jun. 1971.

[229] K.-D. Jung, C. A. Lee, D.-W. Park, B.-G. Park, H. Shin, and J. D. Lee, "Admittance measurements on ofet channel and its modeling with–network," *IEEE electron device letters*, vol. 28, no. 3, pp. 204–206, 2007.

[230] C. Ucurum and H. Goebel, "Quasi-static capacitance–voltage characteristics of pentacene-based metal–oxide–semiconductor structures," *Microelectronics Journal*, vol. 44, no. 7, pp. 606–611, 2013.

[231] S. De Vusser, J. Genoe, and P. Heremans, "Influence of transistor parameters on the noise margin of organic digital circuits," *IEEE Transactions on Electron Devices*, vol. 53, no. 4, pp. 601–610, 2006.

[232] C. P. Watson, B. A. Brown, J. Carter, J. Morgan, and D. M. Taylor, "Organic ring oscillators with sub-200 ns stage delay based on a solution-processed p-type semiconductor blend," *Advanced Electronic Materials*, 2016.

[233] A. C. Hübler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, *et al.*, "Ring oscillator fabricated completely by means of mass-printing technologies," *Organic Electronics*, vol. 8, no. 5, pp. 480–486, 2007.

[234] A. Hübler, G. Schmidt, H. Kempa, K. Reuter, M. Hambsch, and M. Bellmann, "Three-dimensional integrated circuit using printed electronics," *Organic Electronics*, vol. 12, no. 3, pp. 419–423, 2011.

[235] J.-M. Verilhac, M. Benwadih, A.-L. Seiler, S. Jacob, C. Bory, J. Bablet, M. Heitzman, J. Tallal, L. Barbut, P. Frère, *et al.*, "Step toward robust and reliable amorphous polymer field-effect transistors and logic functions made by the use of roll to roll compatible printing processes," *Organic Electronics*, vol. 11, no. 3, pp. 456–462, 2010.

[236] E. R. Patchett, A. Williams, Z. Ding, G. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, and D. M. Taylor, "A high-yield vacuum-evaporation-based r2r-compatible fabrication route for organic electronic circuits," *Organic Electronics*, vol. 15, no. 7, pp. 1493–1502, 2014.

[237] T. D. Anthopoulos, S. Setayesh, E. Smits, M. Cölle, E. Cantatore, B. de Boer, P. W. Blom, and D. M. de Leeuw, "Air-stable complementary-like circuits based on organic ambipolar transistors," *Advanced Materials*, vol. 18, no. 14, pp. 1900–1904, 2006.

[238] A. J. Kronemeijer, E. Gili, M. Shahid, J. Rivnay, A. Salleo, M. Heeney, and H. Sirringhaus, "A selenophene-based low-bandgap donor–acceptor polymer leading to fast ambipolar logic," *Advanced Materials*, vol. 24, no. 12, pp. 1558–1565, 2012.

[239] W. Roelofs, S. Mathijssen, J. Bijleveld, D. Raiteri, T. Geuns, M. Kemerink, E. Cantatore, R. Janssen, and D. de Leeuw, "Fast ambipolar integrated circuits with poly (diketopyrrolopyrrole-terthiophene)," *Applied Physics Letters*, vol. 98, no. 20, p. 203 301, 2011.

[240] M. H. Choi, B. S. Kim, and J. Jang, "High-performance flexible tft circuits using tips pentacene and polymer blend on plastic," *IEEE Electron Device Letters*, vol. 33, no. 11, pp. 1571–1573, 2012.

[241] D. Gundlach, J. Royer, S. Park, S. Subramanian, O. Jurchescu, B. Hamadani, A. Moad, R. Kline, L. Teague, O. Kirillov, *et al.*, "Contact-induced crystallinity for high-performance soluble acene-based transistors and circuits," *Nature materials*, vol. 7, no. 3, pp. 216–221, 2008.

[242] J. Smith, R. Hamilton, M. Heeney, D. M. de Leeuw, E. Cantatore, J. E. Anthony, I. McCulloch, D. D. Bradley, and T. D. Anthopoulos, "High-performance organic integrated circuits based on solution processable polymer-small molecule blends," *Applied Physics Letters*, vol. 93, no. 25, p. 253 301, 2008.

[243] X. Zhang, H. Bronstein, A. J. Kronemeijer, J. Smith, Y. Kim, R. J. Kline, L. J. Richter, T. D. Anthopoulos, H. Sirringhaus, K. Song, *et al.*, "Molecular origin of high field-effect mobility in an indacenodithiophene–benzothiadiazole copolymer," *Nature communications*, vol. 4, 2013.

[244] K.-J. Baeg, S.-W. Jung, D. Khim, J. Kim, D.-Y. Kim, J. B. Koo, J. R. Quinn, A. Facchetti, I.-K. You, and Y.-Y. Noh, "Low-voltage, high speed inkjet-printed flexible complementary polymer electronic circuits," *Organic Electronics*, vol. 14, no. 5, pp. 1407–1418, 2013.

[245] A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, and H. Sirringhaus, "Programmable logic circuits for functional integrated smart plastic systems," *Organic Electronics*, vol. 15, no. 11, pp. 3111–3119, 2014.

[246] U. Zschieschang, H. Klauk, M. Halik, G. Schmid, and C. Dehm, "Flexible organic circuits with printed gate electrodes," *Advanced materials*, vol. 15, no. 14, pp. 1147–1151, 2003.

[247] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, *et al.*, "Organic rfid transponder chip with data rate compatible with electronic product coding," *Organic Electronics*, vol. 11, no. 7, pp. 1176–1179, 2010.

[248] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, *et al.*, "Megahertz operation of flexible low-voltage organic thin-film transistors," *Organic Electronics*, vol. 14, no. 6, pp. 1516–1520, 2013.

[249] P. Heremans, J. Genoe, S. Steudel, K. Myny, S. Smout, P. Vicca, C. Grillberger, O. R. Hild, F. Furthner, B. van der Putten, *et al.*, "Thin-film transistors and circuits on plastic foil," in *2009 IEEE International Electron Devices Meeting (IEDM)*, IEEE, 2009, pp. 1–4.

[250] M. Kitamura, Y. Kuzumoto, S. Aomori, and Y. Arakawa, "High-frequency organic complementary ring oscillator operating up to 200 khz," *Applied physics express*, vol. 4, no. 5, p. 051 601, 2011.

[251] U. Kraft, M. Sejfić, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. N. Burghartz, E. Weber, and H. Klauk, "Flexible low-voltage organic complementary circuits: Finding the optimum combination of semiconductors and monolayer gate dielectrics," *Advanced Materials*, vol. 27, no. 2, pp. 207–214, 2015.

[252] T.-H. Ke, R. Müller, B. Kam, M. Rockele, A. Chasin, K. Myny, S. Steudel, W. D. Oosterbaan, L. Lutsen, J. Genoe, *et al.*, "Scaling down of organic complementary logic gates for compact logic on foil," *Organic Electronics*, vol. 15, no. 6, pp. 1229–1234, 2014.

[253] B. C. Kjellander, W. T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans, and G. H. Gelinck, "Optimized circuit design for flexible 8-bit RFID transponders with active layer of ink-jet printed small molecule semiconductors," *Organic Electronics*, vol. 14, no. 3, pp. 768–774, 2013.

[254] B. Kim, M. L. Geier, M. C. Hersam, and A. Dodabalapur, "Inkjet printed circuits on flexible and rigid substrates based on ambipolar carbon nanotubes with high operational stability," *ACS applied materials & interfaces*, vol. 7, no. 50, pp. 27 654–27 660, 2015.

[255] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, *et al.*, "Organic rfid transponder chip with data rate compatible with electronic product coding," *Organic Electronics*, vol. 11, no. 7, pp. 1176–1179, 2010.

[256] M. Mashayekhi, L. Winchester, L. Evans, T. Pease, M.-M. Laurila, M. Mäntysalo, S. Ogier, L. Terés, and J. Carrabina, "Evaluation of aerosol, superfine inkjet, and photolithography printing techniques for metallization of application specific printed electronic circuits," *IEEE Transactions on Electron Devices*, vol. 63, no. 3, pp. 1246–1253, 2016.

[257] S. Ogier, *Printed via connection.* UK Patent pending, 1601515.8, 2015.

[258] C. Wei, H. Qin, N. A. Ramırez-Iglesias, C.-P. Chiu, Y.-s. Lee, and J. Dong, "High-resolution ac-pulse modulated electrohydrodynamic jet printing on highly insulating substrates," *Journal of Micromechanics and Microengineering*, vol. 24, no. 4, p. 045 010, 2014.

[259] H. Qin, J. Dong, and Y.-S. Lee, "Ac-pulse modulated electrohydrodynamic jet printing and electroless copper deposition for conductive microscale patterning on flexible insulating substrates," *Robotics and Computer-Integrated Manufacturing*, 2015.

[260] *Harima datasheet*, https://www.harima.co.jp/en/products/electronics/pdf/brochure14e_21.pdf, Harima.

[261] J. Lin, P. Dahlsten, J. Pekkanen, M. Linden, M. Mäntysalo, and R. Österbacka, "Surface energy patterning for inkjet printing in device fabrication," in *SPIE Photonic Devices+ Applications*, International Society for Optics and Photonics, 2009, pp. 74171D–74171D.

[262] R. Verkuijlen, M. Van Dongen, A. Stevens, J. van Geldrop, and J. Bernards, "Surface modification of polycarbonate and polyethylene naphtalate foils by uv-ozone treatment and μplasma printing," *Applied Surface Science*, vol. 290, pp. 381–387, 2014.

[263] M. Mäntysalo and P. Mansikkamäki, "Inkjet-deposited interconnections for electronic packaging," in *NIP & Digital Fabrication Conference*, Society for Imaging Science and Technology, vol. 2007, 2007, pp. 813–817.

[264] *ULVAC AU-ink datasheet*, http://www.ulvac.com/specialty-materials-services/nano_metal_inks.cfm, ULVAC AU-ink.

[265] H. T. Yudistira, V. D. Nguyen, P. Dutta, and D. Byun, "Flight behavior of charged droplets in electrohydrodynamic inkjet printing," *Applied Physics Letters*, vol. 96, no. 2, p. 023 503, 2010.

[266] *68–95–99.7 rule*, https://en.wikipedia.org/wiki/68-95-99.7_rule, Three-sigma rule of thumb.

[267] G. Gelinck, P. Heremans, K. Nomoto, and T. D. Anthopoulos, "Organic transistors in optical displays and microelectronic applications," *Advanced materials*, vol. 22, no. 34, pp. 3778–3798, 2010.

[268] K. Myny, M. J. Beenhakkers, N. A. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "A 128b organic rfid transponder chip, including manchester encoding and aloha anti-collision protocol, operating with a data rate of 1529b/s," in *2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, IEEE, 2009, pp. 206–207.

Appendix A

Layouts and floorplans

Layout of the DRC test vehicles matrics

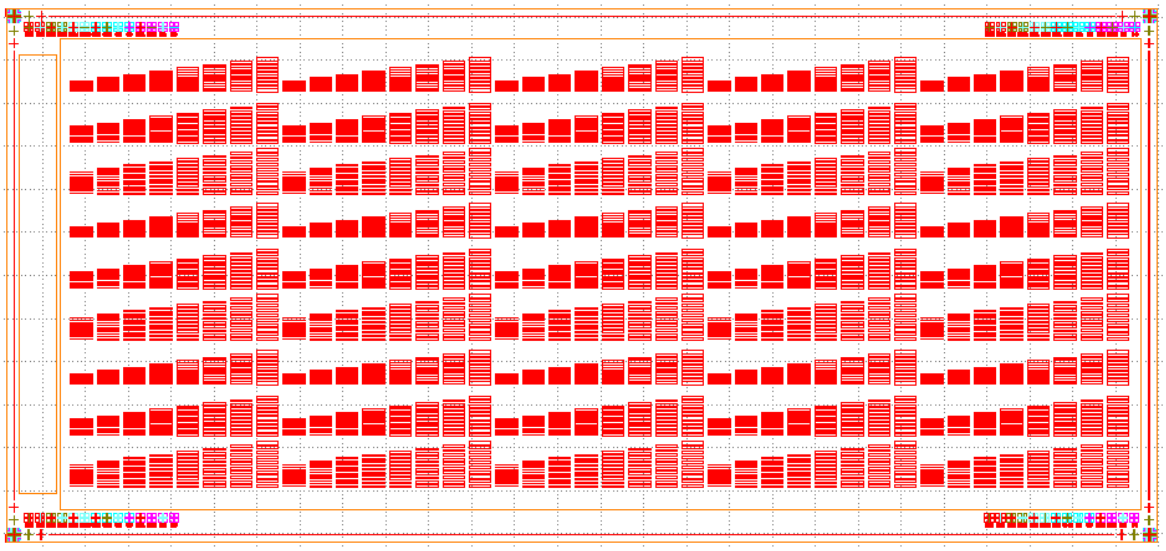


Fig. A.1 Test vehicles for width and space of horizontal MET1 bars

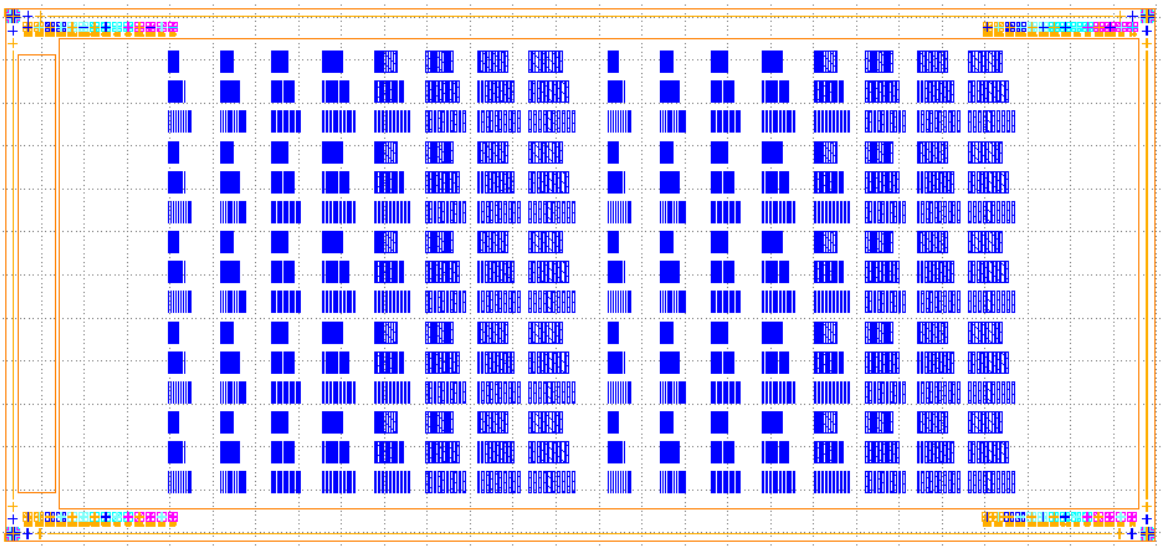


Fig. A.2 Test vehicles for width and space of vertical MET2 bars

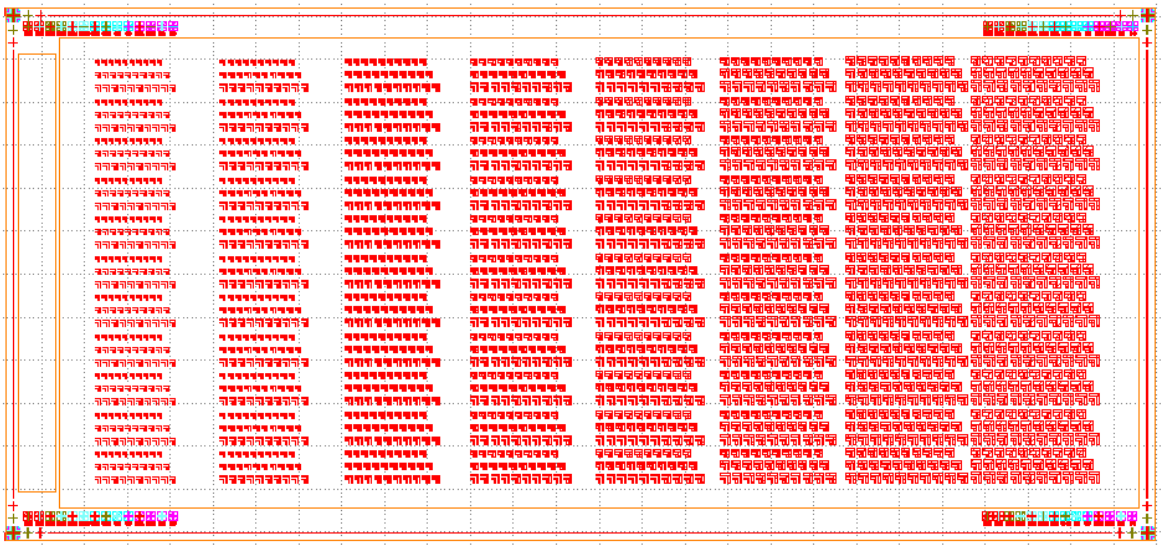


Fig. A.3 Test vehicles for corner spacing of MET1

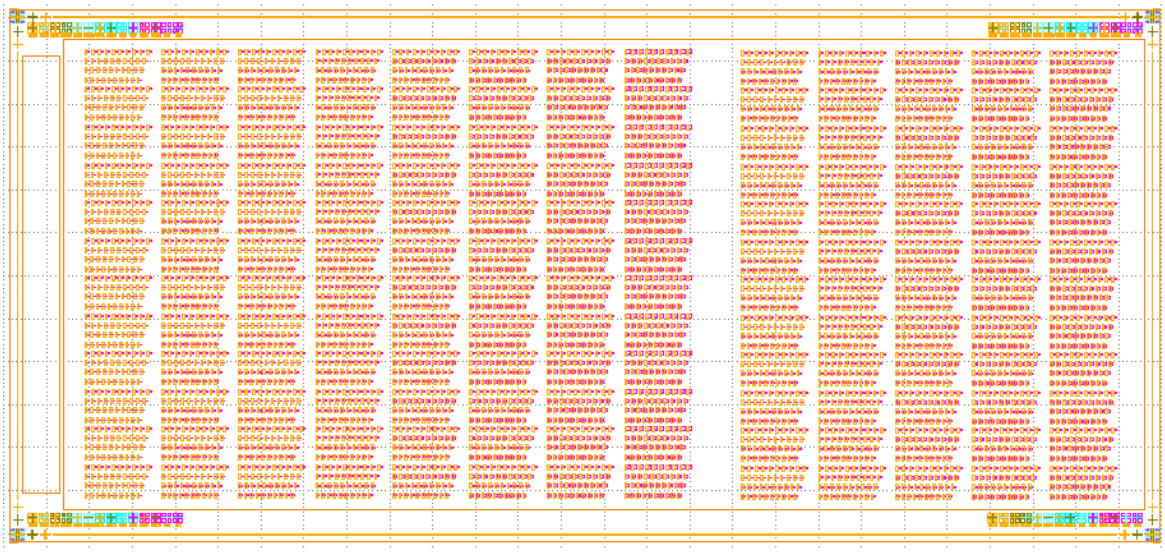


Fig. A.4 Test vehicles for extension, overlap, and width of two layers together

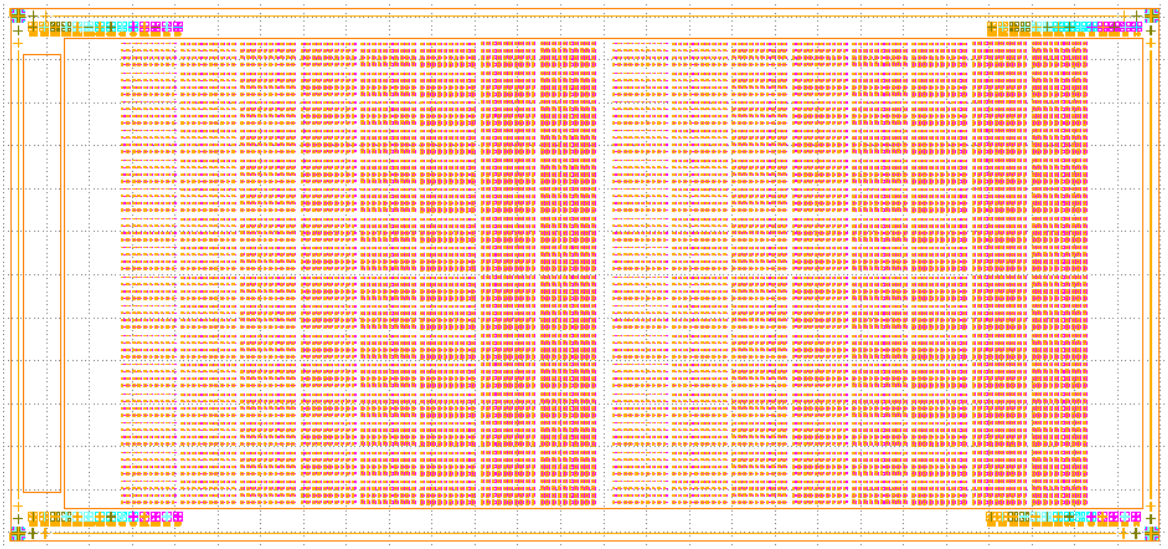


Fig. A.5 Test vehicles for extension, overlap, and width of two layers together (another shape)

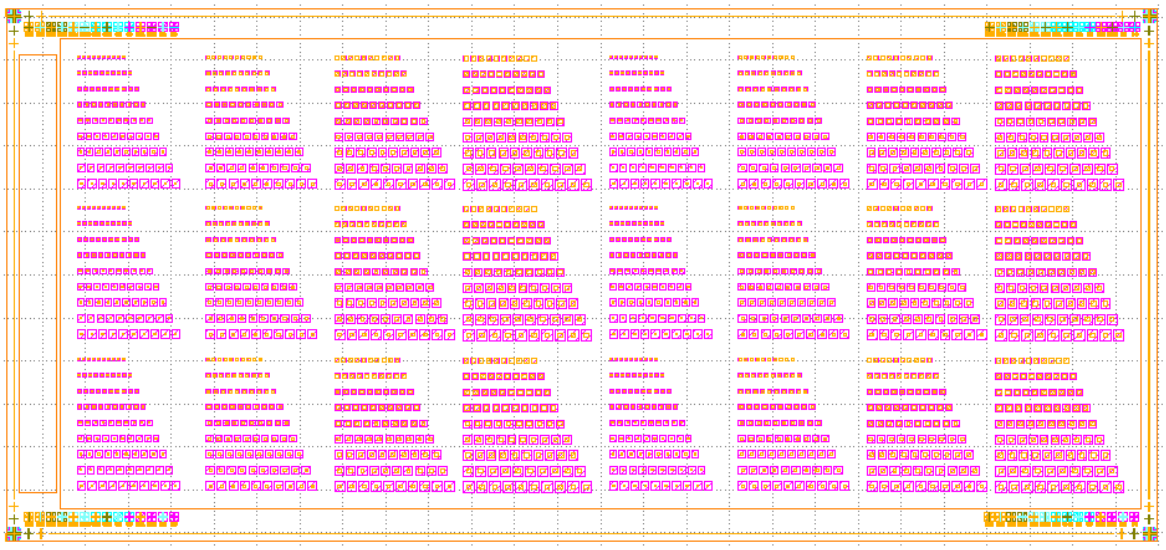


Fig. A.6 Test vehicles for extension and width of two layers together

Fig. A.7 Test vehicles for spacing and width of two layers together

Fig. A.8 Zoomed test vehicles for width and space of horizontal MET1 bars

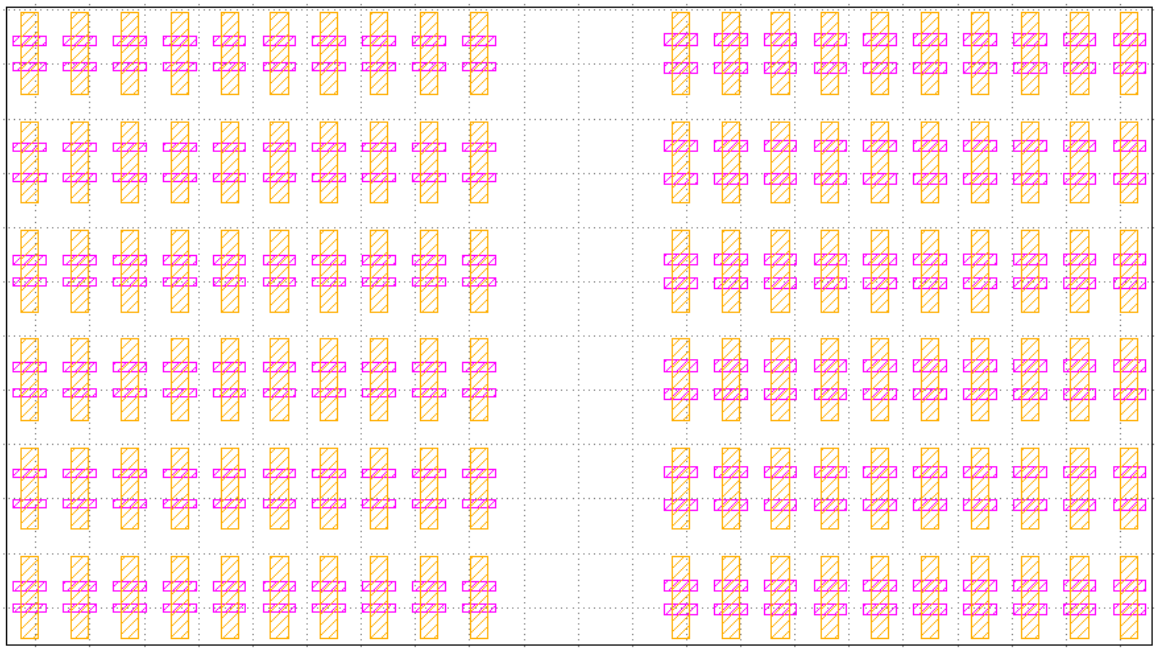


Fig. A.9 Zoomed test vehicles for spacing and width of two layers together

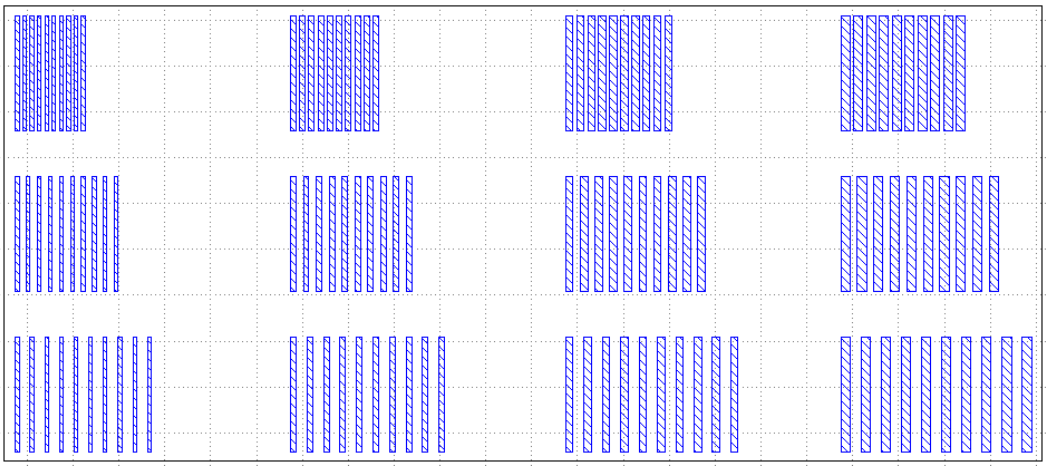


Fig. A.10 Zoomed test vehicles for width and space of vertical MET2 bars

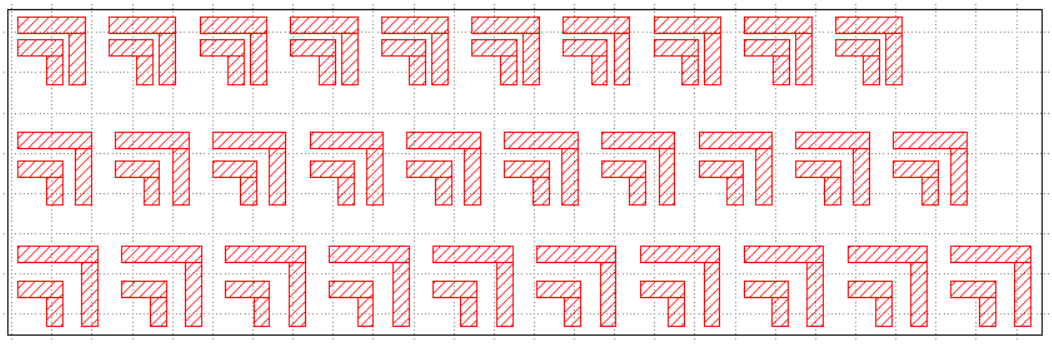


Fig. A.11 Zoomed test vehicles for corner spacing of MET1

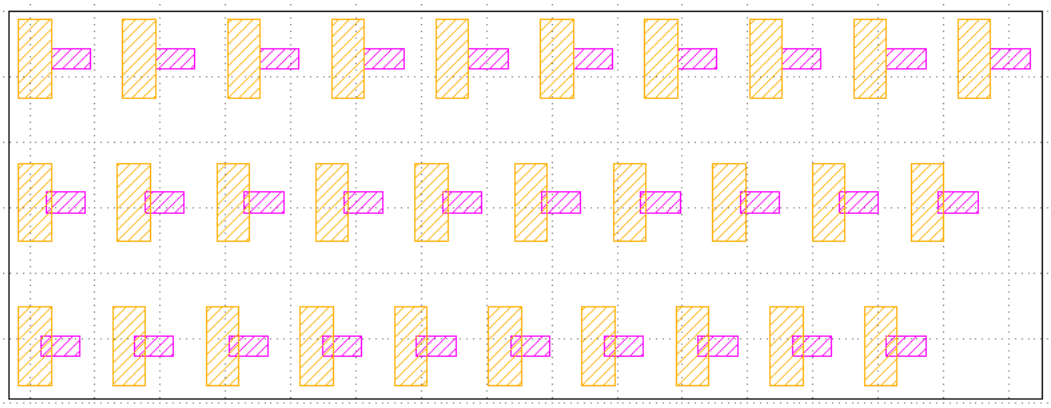


Fig. A.12 Zoomed test vehicles for extension, overlap, and width of two layers together

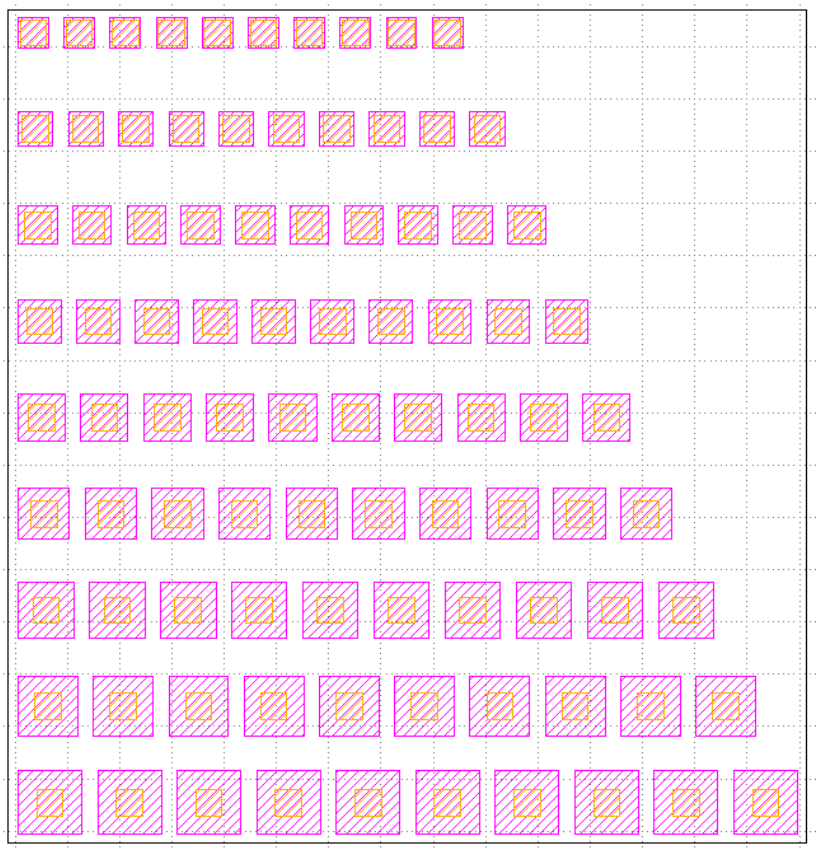


Fig. A.13 Zoomed test vehicles for extension and width of two layers together

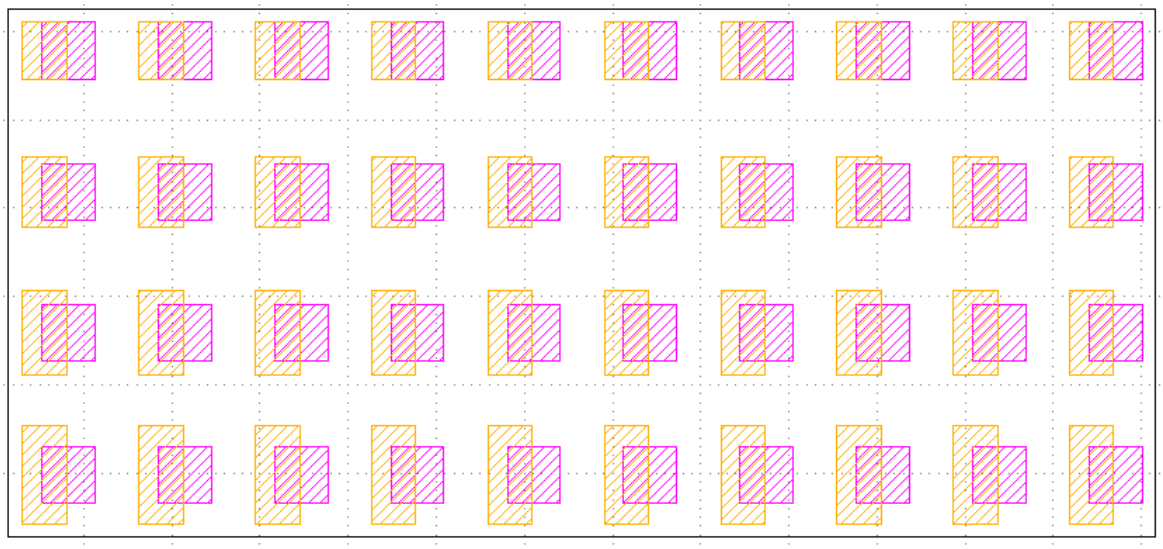


Fig. A.14 Zoomed test vehicles for extension, overlap, and width of two layers together (another shape)

Layout of the transistor arrays

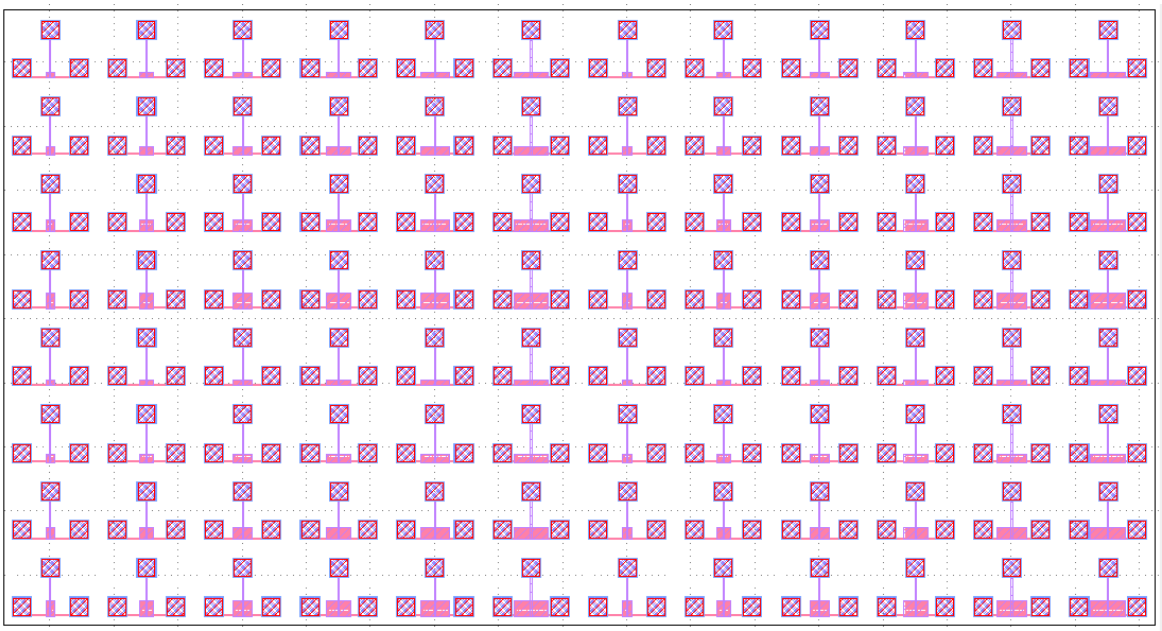


Fig. A.15 Array of fully overlapped Interdigitated OTFTs

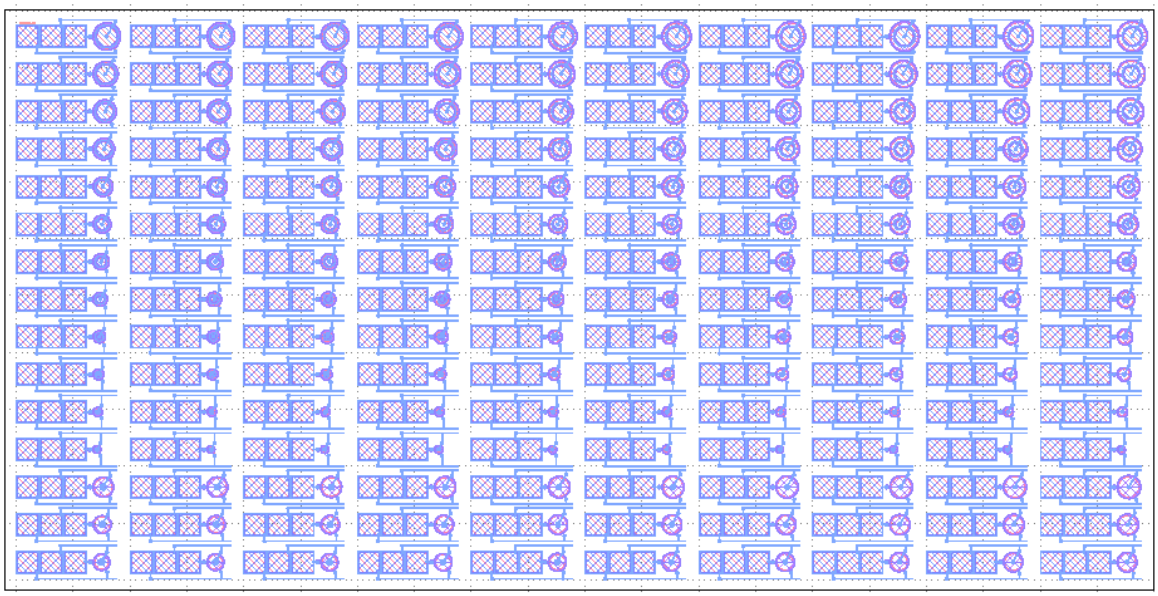


Fig. A.16 Array of Corbino OTFTs

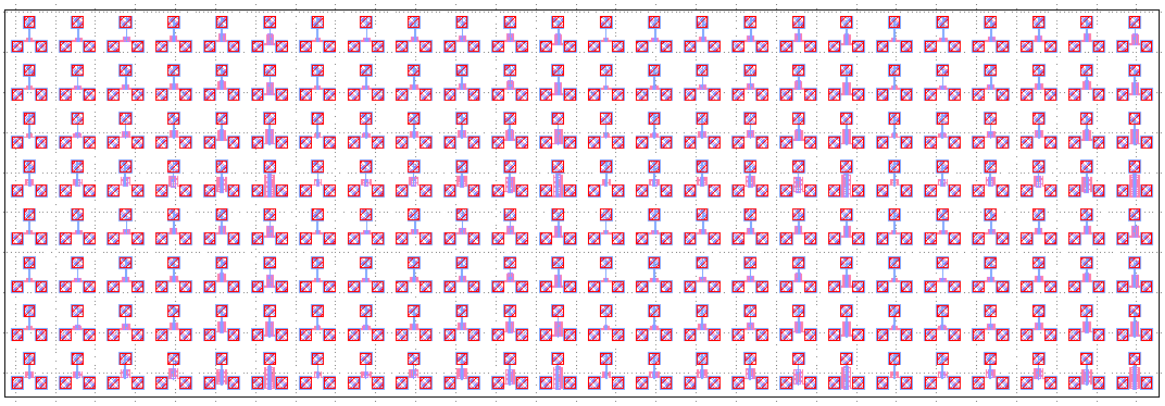


Fig. A.17 Array of partially overlapped Interdigitated OTFTs

Layout of logic gates and circuits

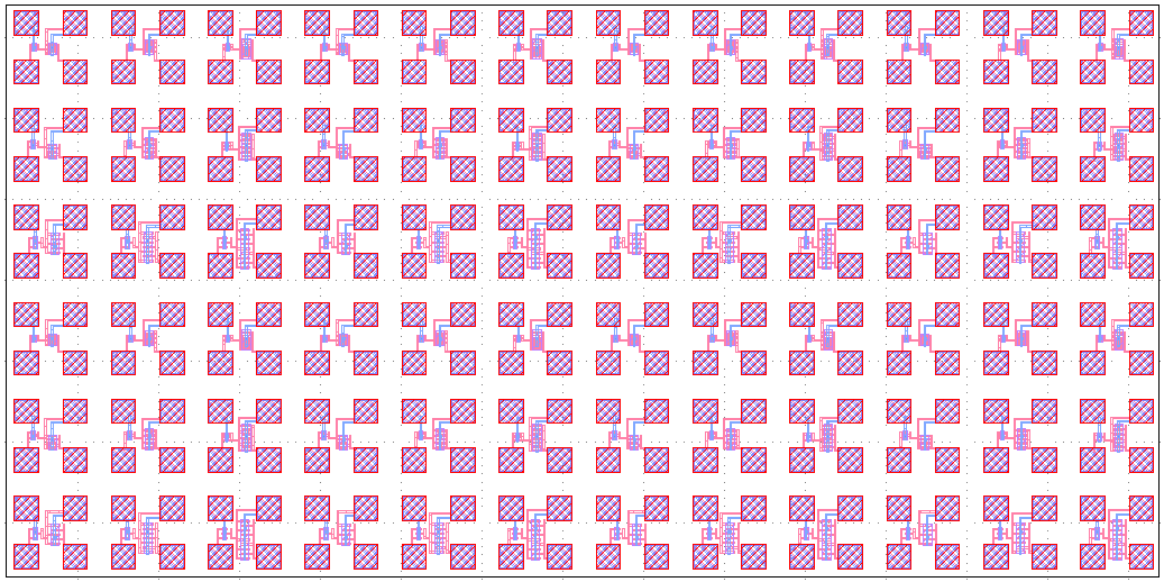


Fig. A.18 Inverters layout

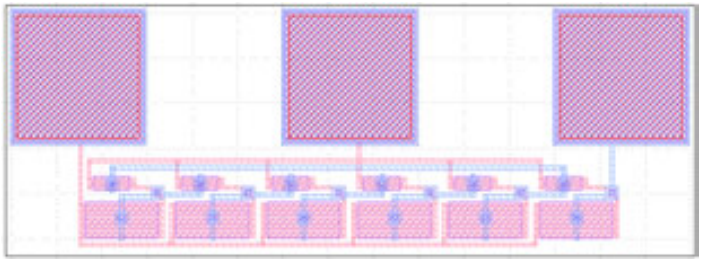


Fig. A.19 5-stage Ring oscillator layout

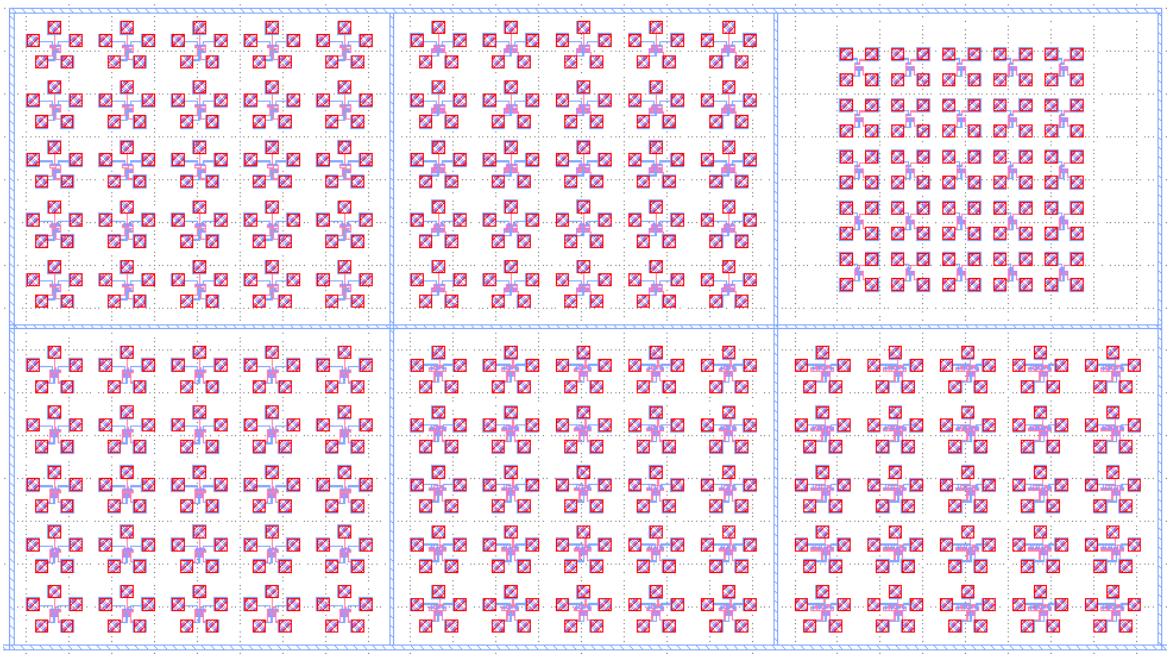


Fig. A.20 Digital logic gates (NAND, NOR, INV) layout

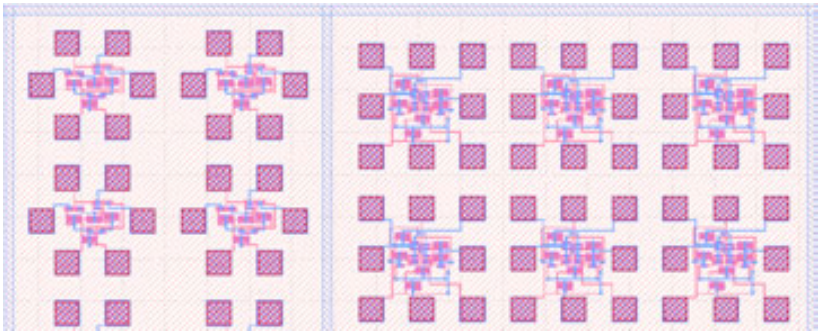


Fig. A.21 2-bit MUX and 2-to-4 decoder circuit layout

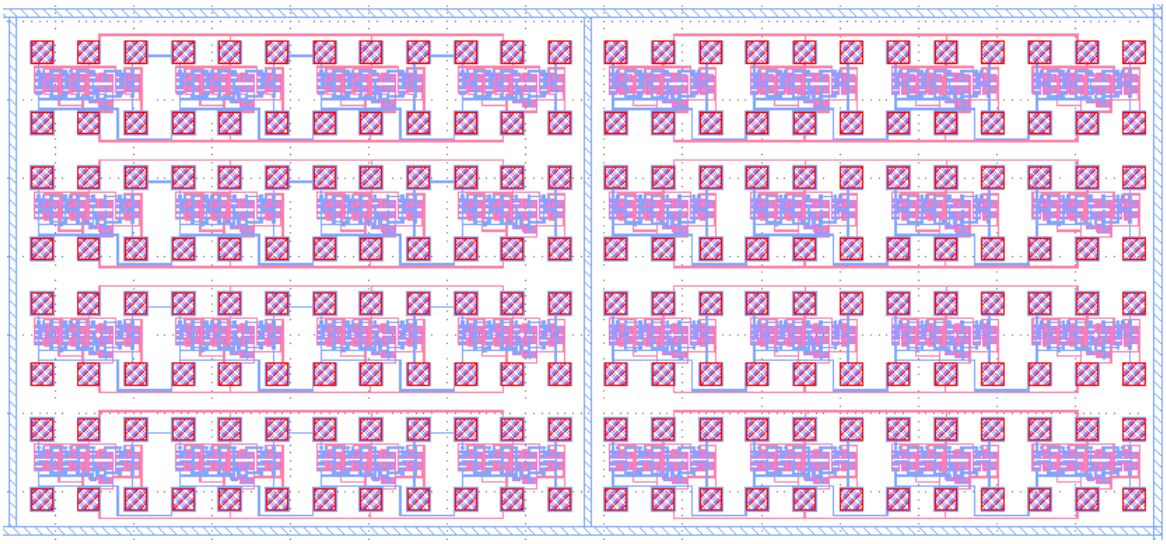


Fig. A.22 Sequential circuits (shift registers) layout

Layout of the IGAs

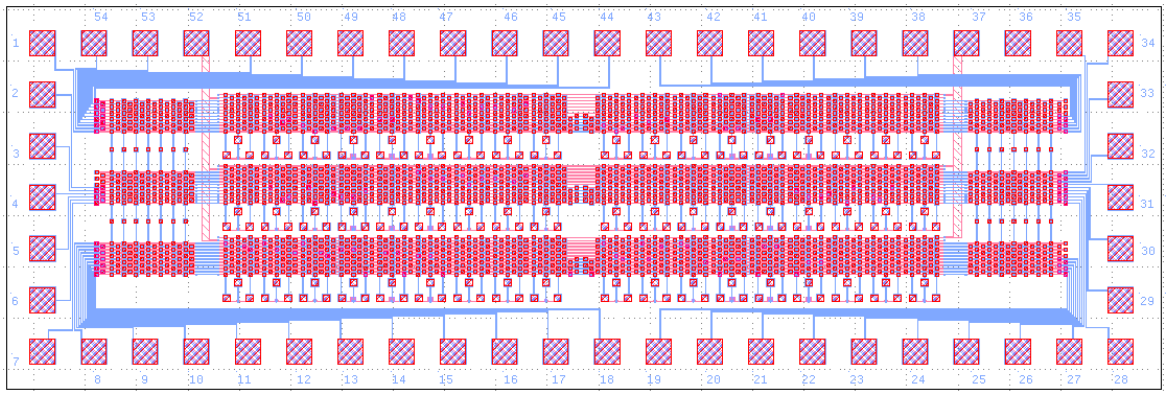


Fig. A.23 Small transistor-based IGA

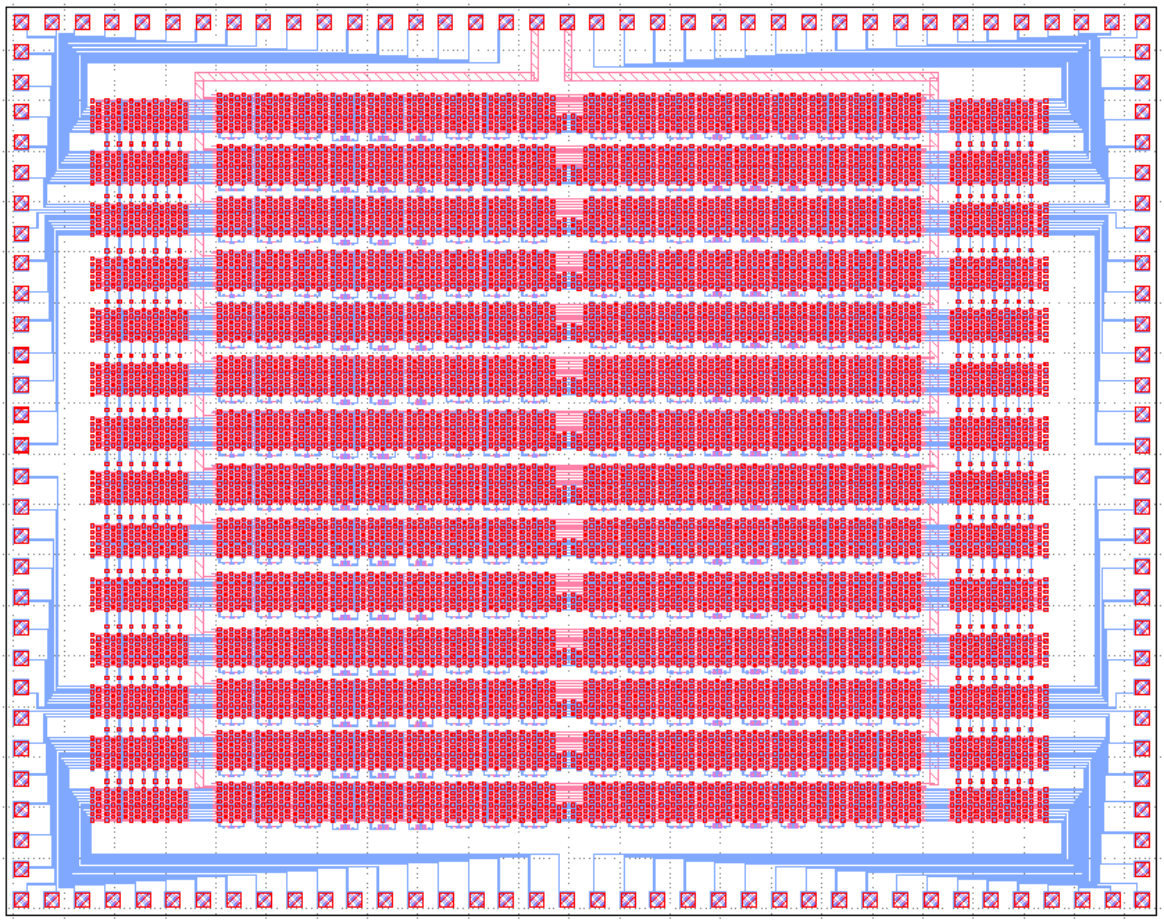


Fig. A.24 Large transistor-based IGA

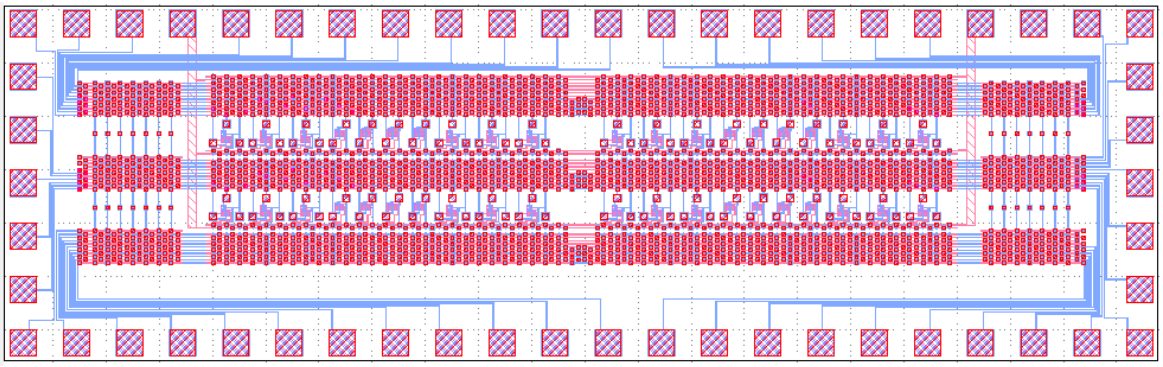


Fig. A.25 Small cell-based IGA

Layout of the wire cell test structures

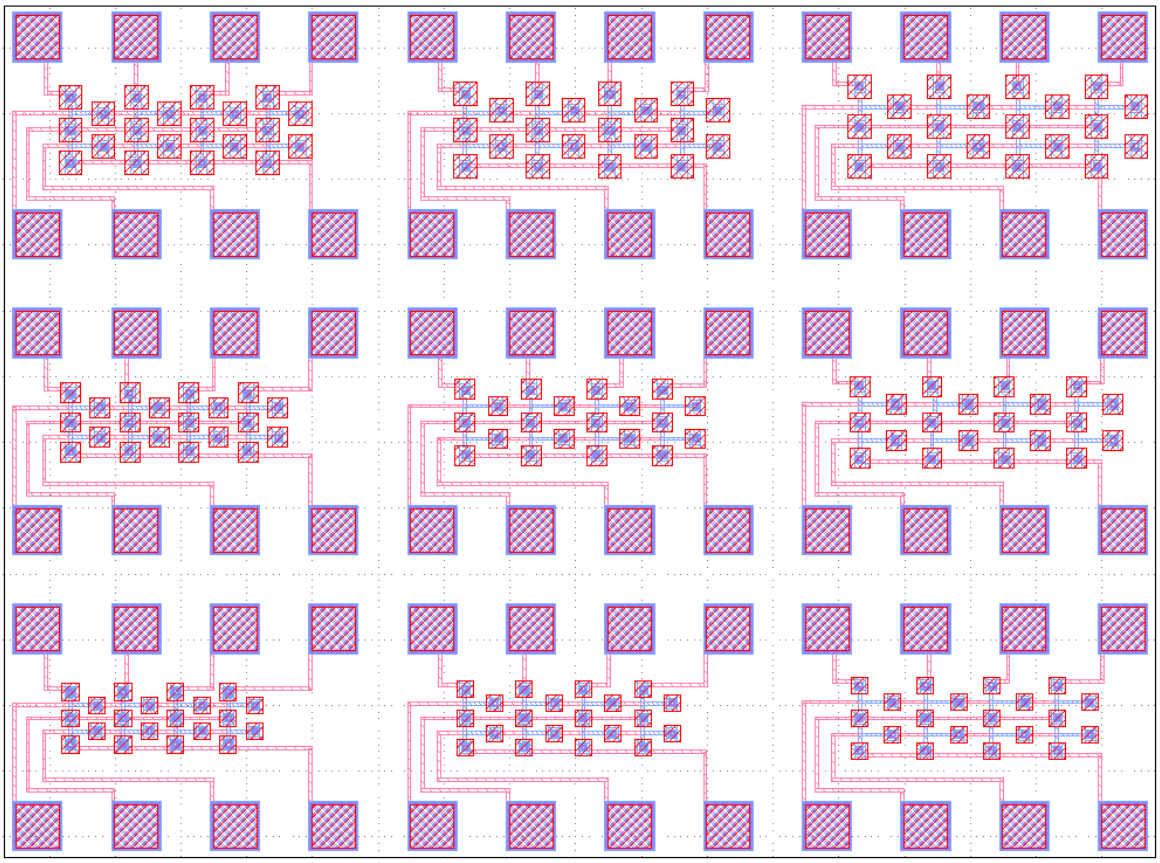


Fig. A.26 DoD configurable test structures layout

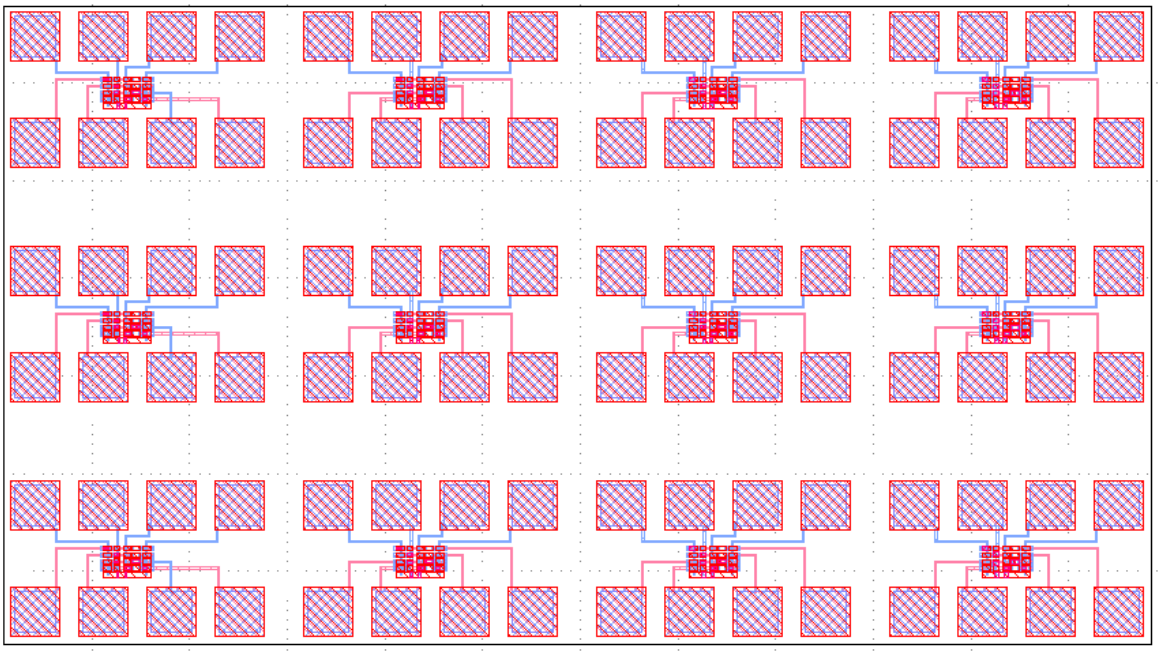


Fig. A.27 Line configurable test structures layout

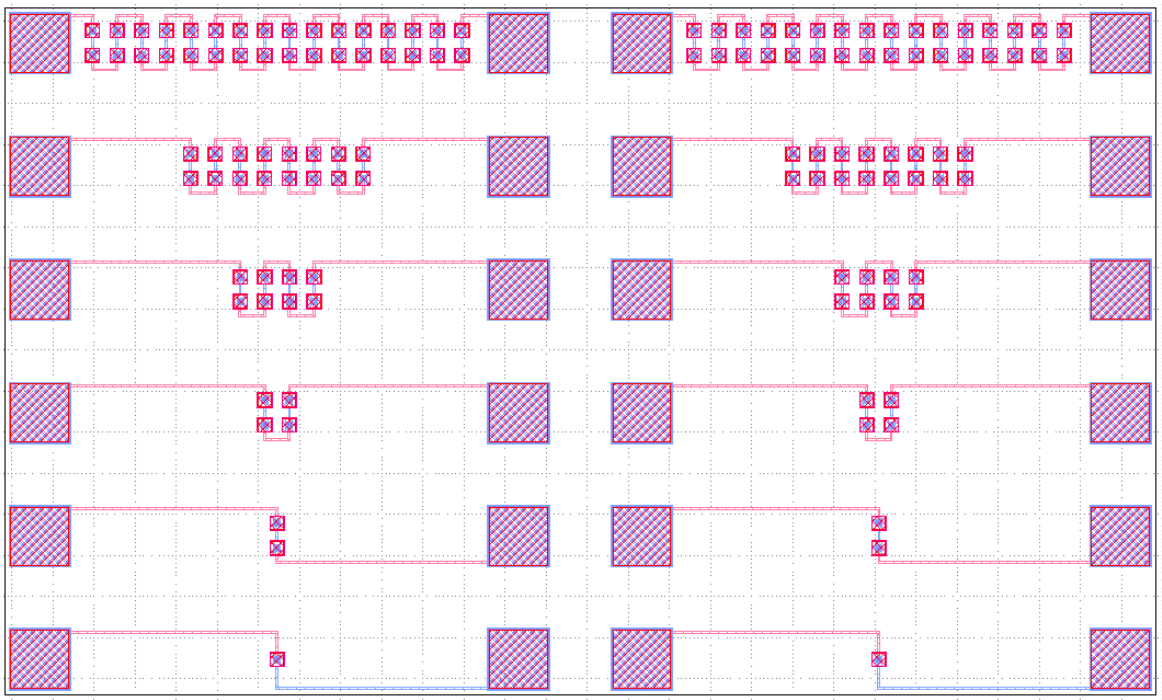


Fig. A.28 Via chain test structures layout

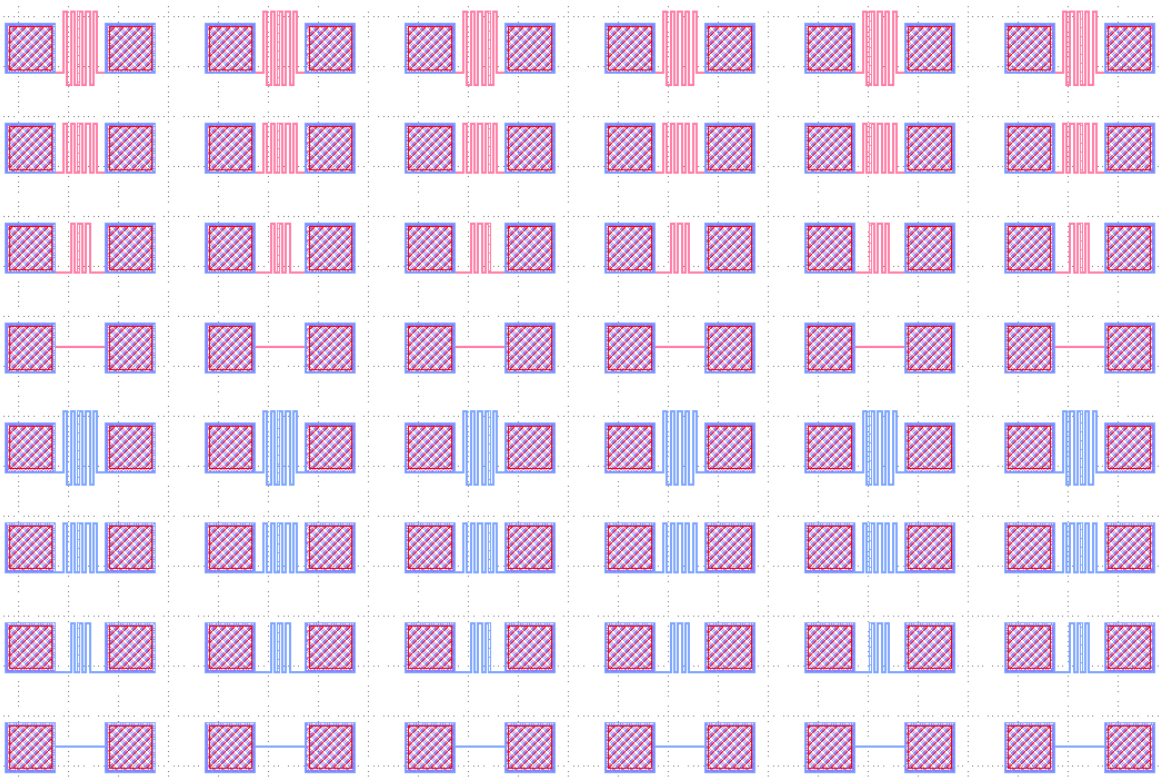


Fig. A.29 Metal resistance test structures layout

Layout of the fabrication runs

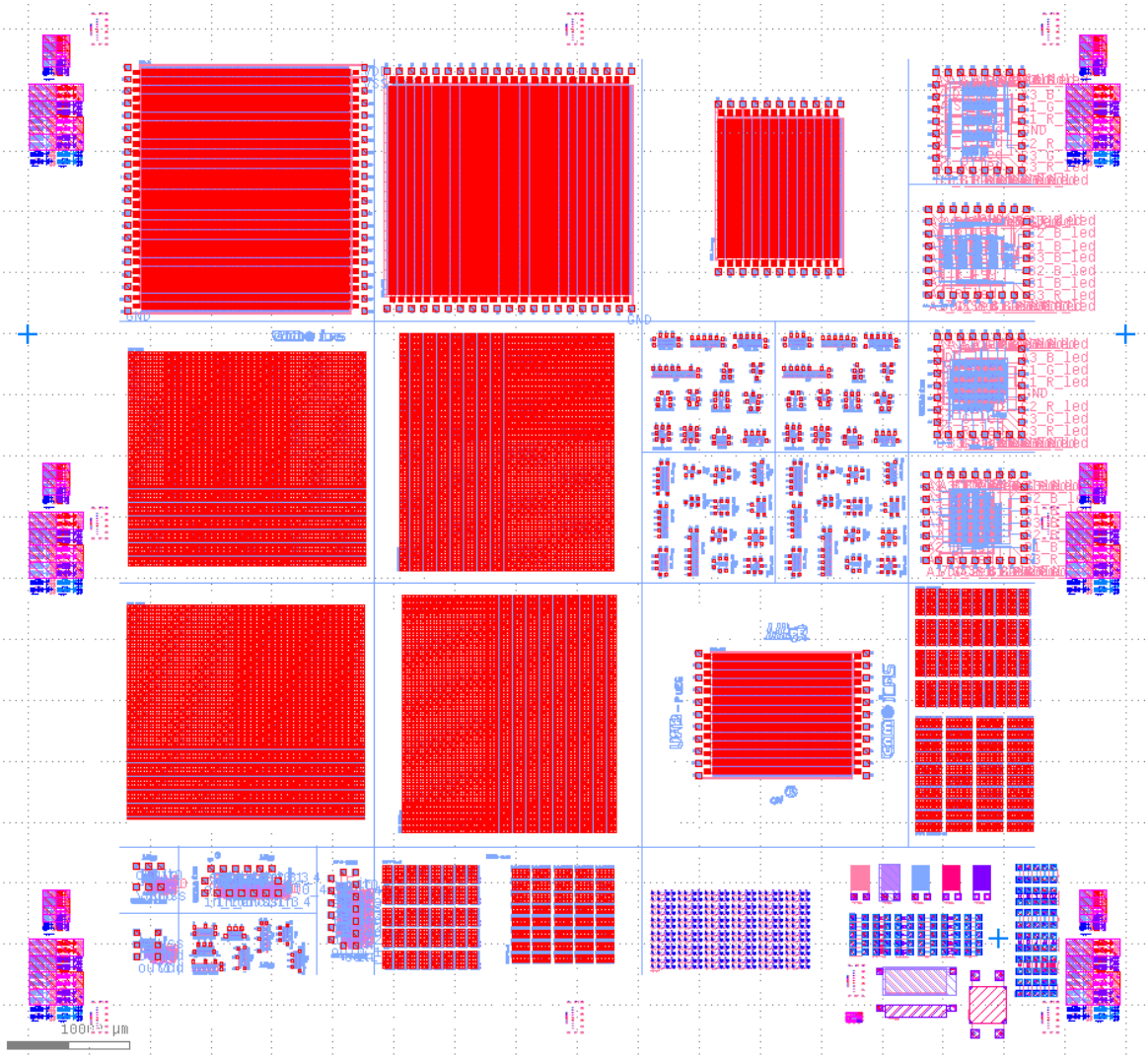


Fig. A.30 Run1 layout

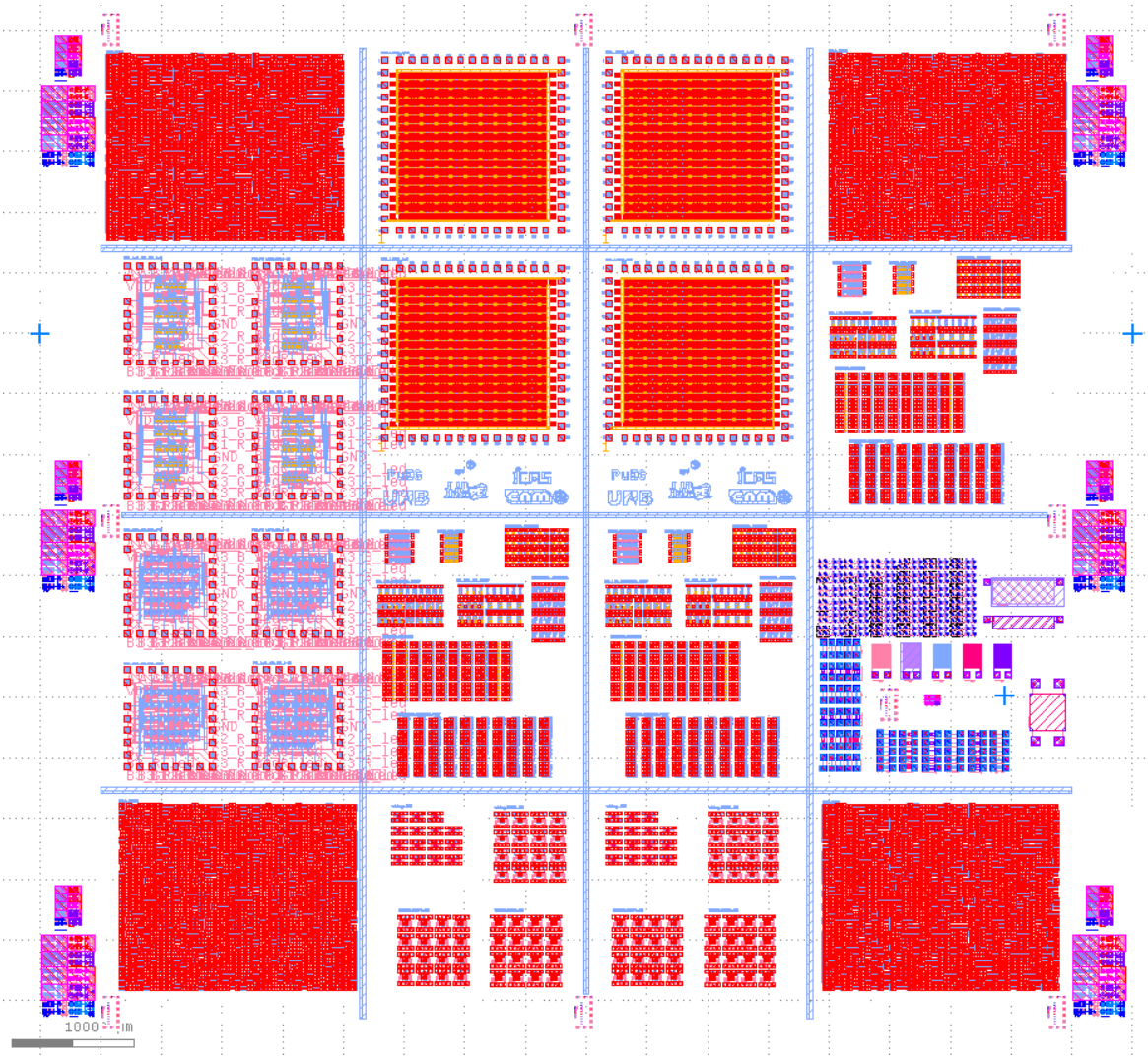


Fig. A.31 Run2 layout

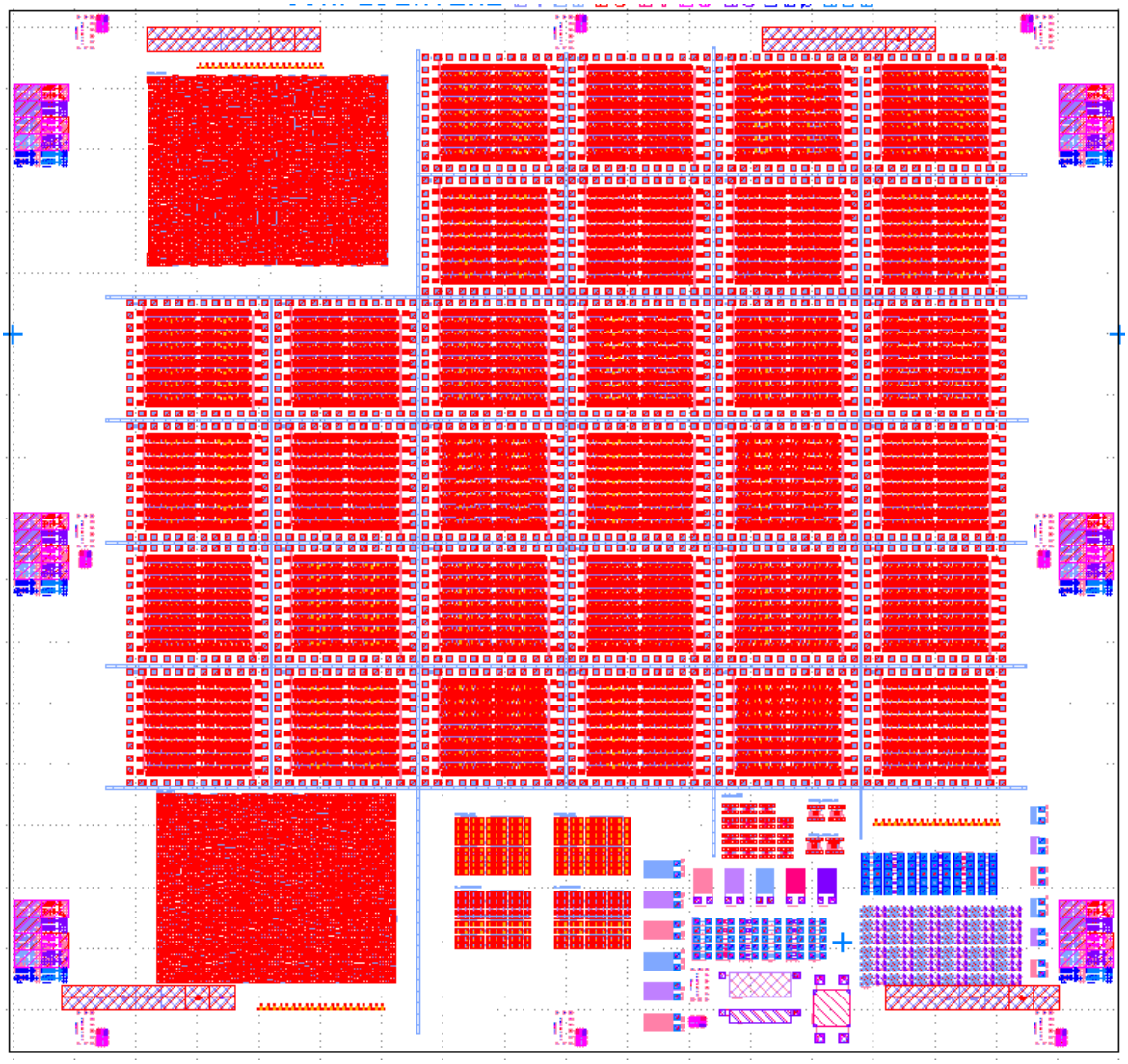


Fig. A.32 Run3 layout

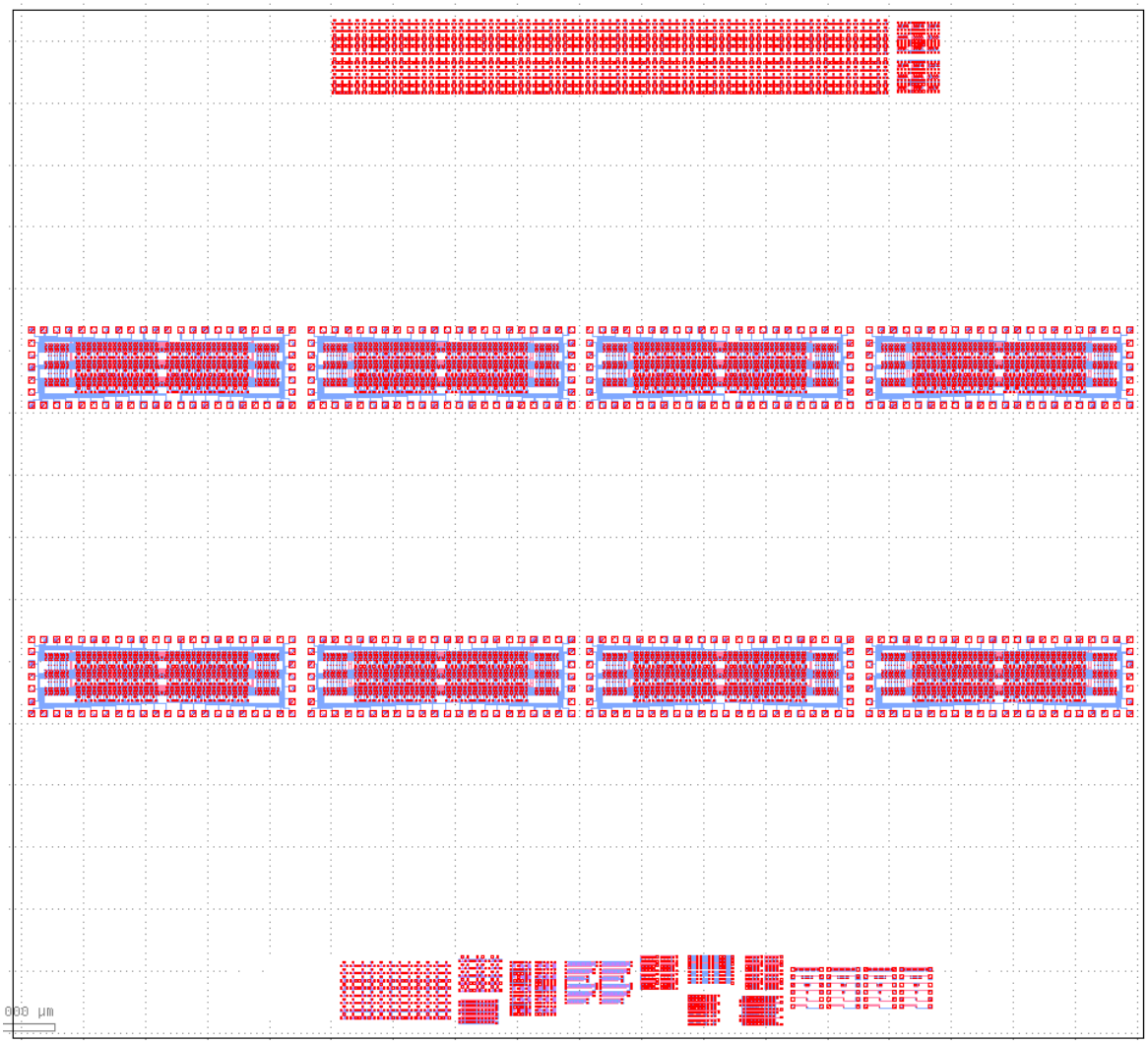


Fig. A.33 Run4 layout

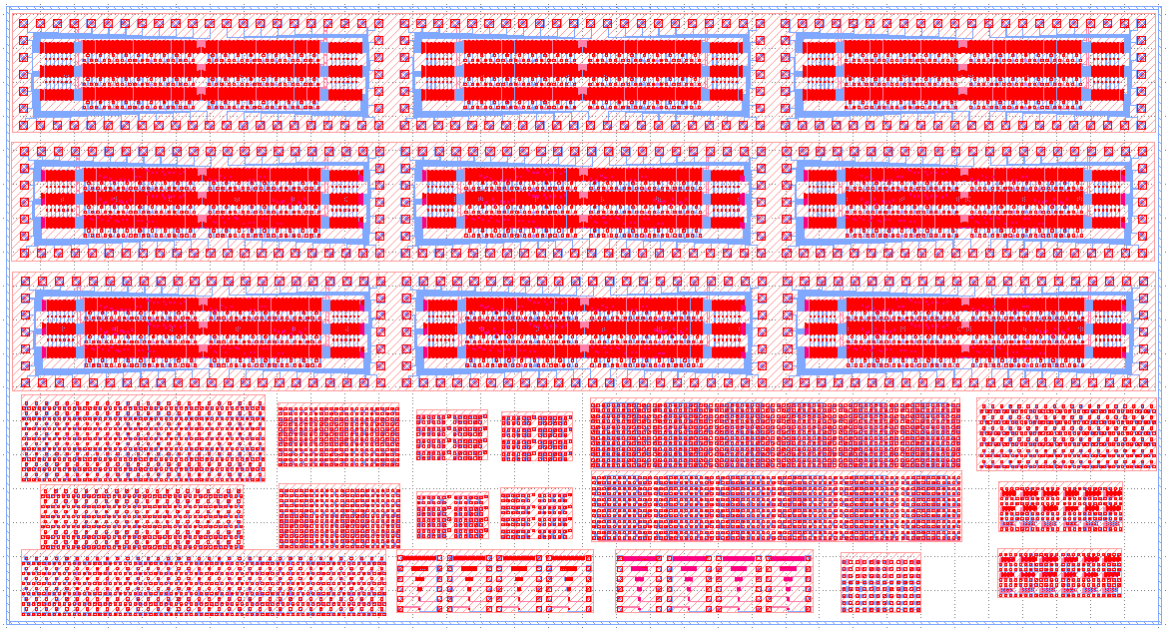


Fig. A.34 Run5 layout

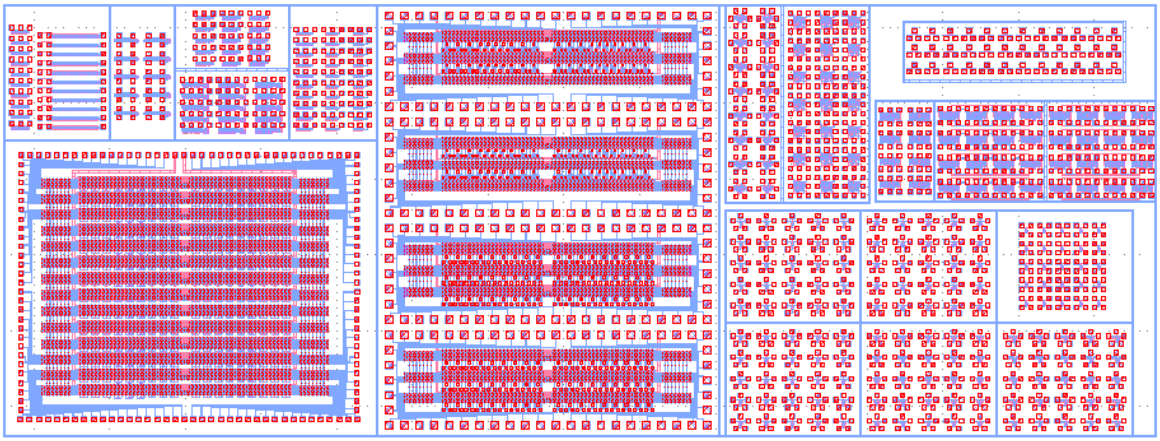


Fig. A.35 Run6 layout

Floorplan of the fabrication runs

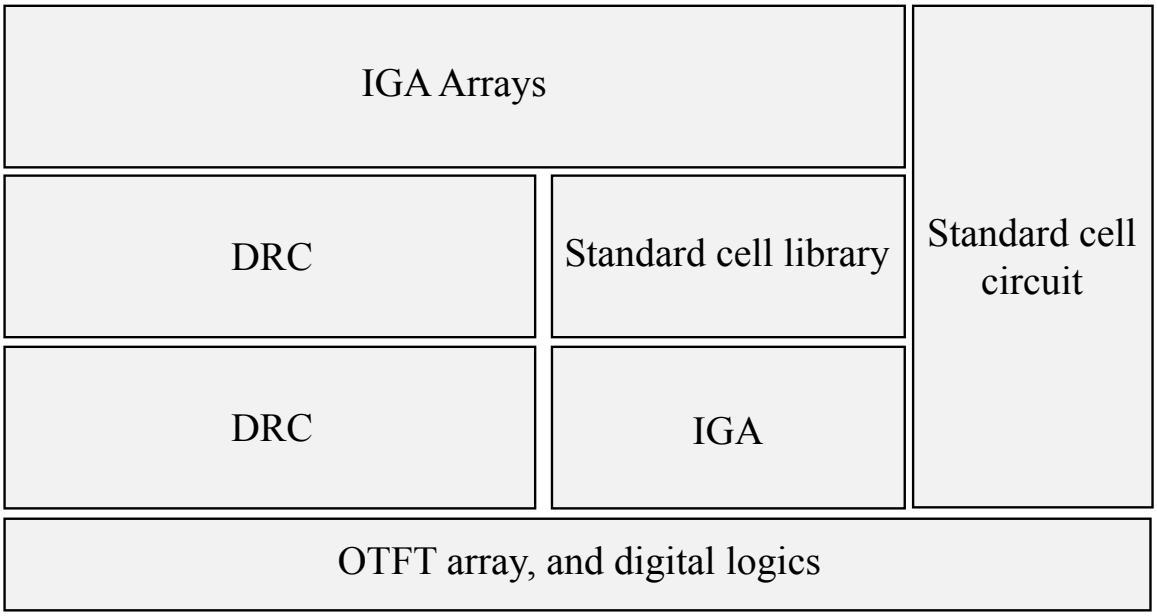


Fig. A.36 Run1 floorplan

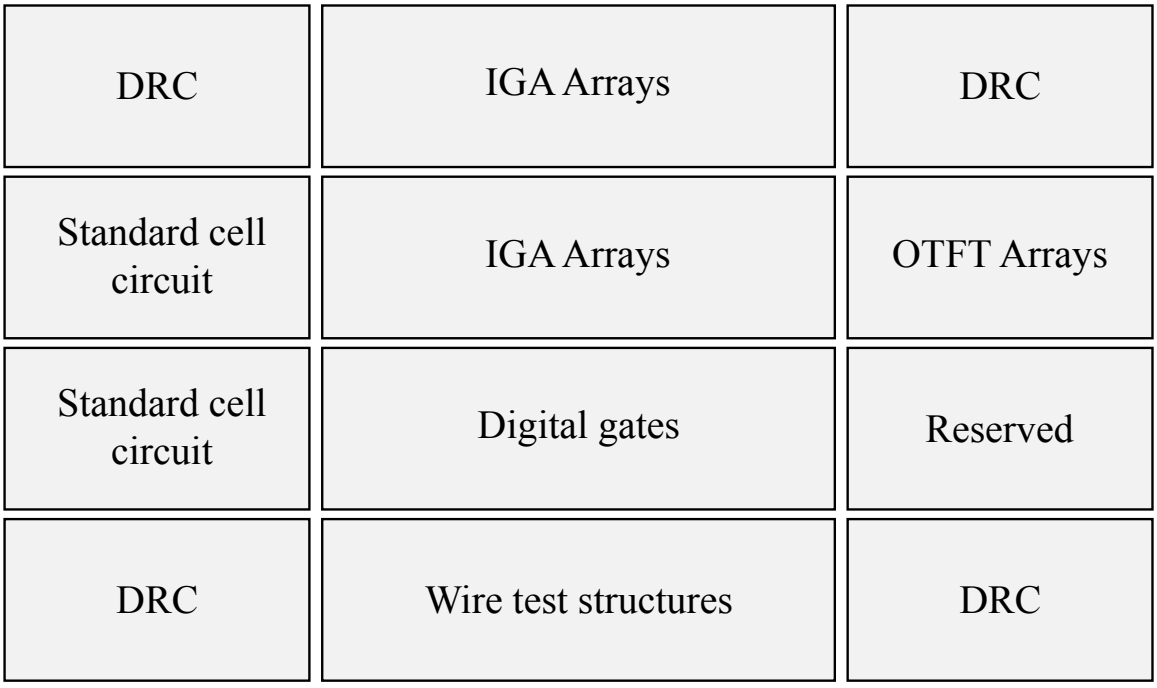


Fig. A.37 Run2 floorplan

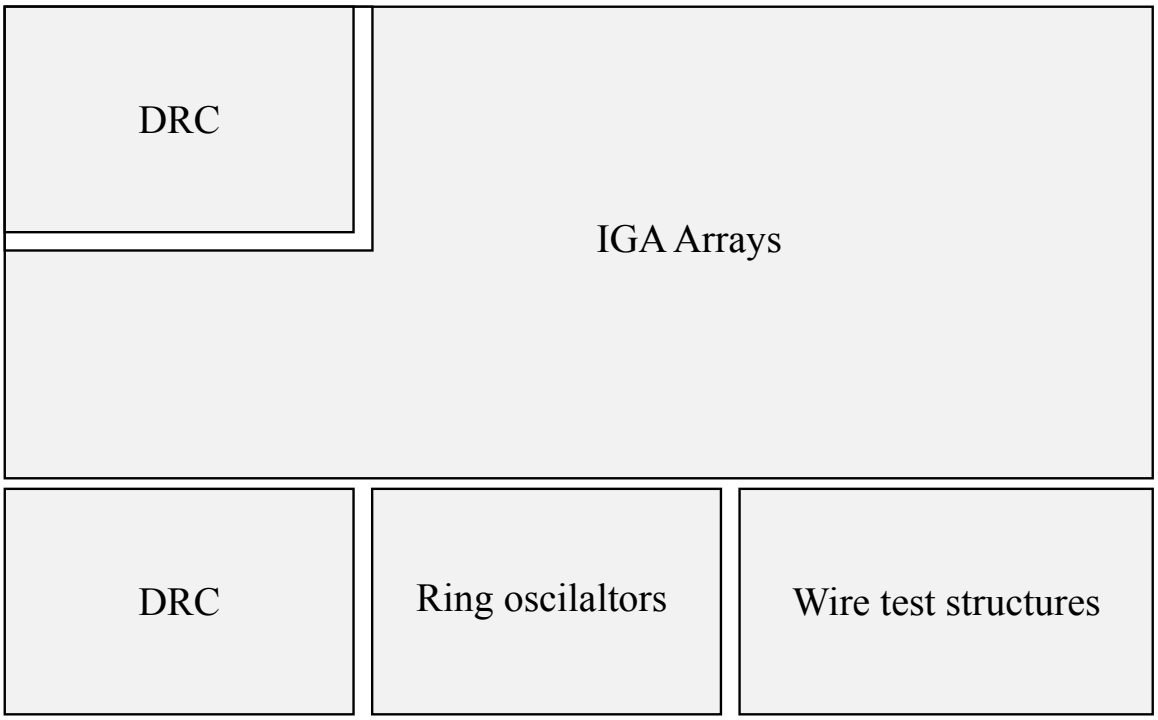


Fig. A.38 Run3 floorplan

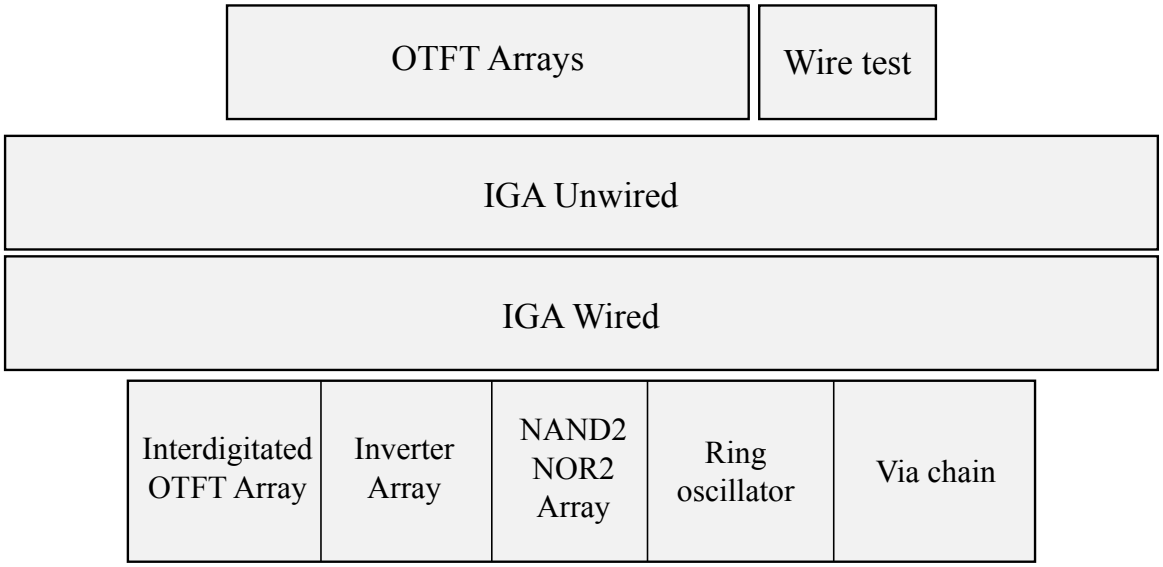


Fig. A.39 Run4 floorplan

<table>
<tr><td colspan="6">IGA Unwired</td></tr>
<tr><td colspan="6">IGA Wired</td></tr>
<tr><td colspan="6">IGA Wired</td></tr>
<tr><td>Interdigitated OTFT Array</td><td>Inverter Array</td><td>NAND2 Array</td><td>NOR2 Array</td><td>Ring oscillator</td><td>Current Mirrors</td></tr>
<tr><td>Interdigitated OTFT Array</td><td>Inverter Array</td><td>NAND2 Array</td><td>NOR2 Array</td><td>Ring oscillator</td><td>Wire test vehicles</td></tr>
<tr><td colspan="2">Interdigitated OTFT Array</td><td colspan="2">Via chain unwired</td><td>Via chain wired</td><td>Wire test vehicles</td></tr>
</table>

Fig. A.40 Run5 floorplan

<table>
<tr><td>Ring oscillators</td><td rowspan="2">IGA</td><td>Combinational circuits</td><td>Sequential circuits</td></tr>
<tr><td>Large IGA</td><td colspan="2">Digital gates</td></tr>
</table>

Fig. A.41 Run6 floorplan

Appendix B

PCell codes and scripts

Listing B.1 is the sample of the PCells coded in python for generation of the test vehicles related to line width and spacing.

Listing B.2 is portion of the script coded in python for generation of 15 different instantiation of the previous pcell test vehicle. In this example, the range of the lines width is between 40um to 200um, in steps of 40um, and the spacing is varying between 80um to 240um in steps of 80um. "$Pitch - x$", and "$Pitch - y$" are the pitch of each instantiation in x and y axis. In order to show the main part of the script that generates the matrix, the rest of the code, related to header, wrappers import, and layers definition is deleted. Also, the parameter range and steps usually have to be large in order to obtain enough data for more accurate extraction of minimum design rules, but in this case, I have simplified the steps so that the generated files are easier to handle during the thesis.

Listing B.3 shows the TVD file, where X and Y positions, device label and parameters are separated by comma.

Listing B.4 is the pseudo pcell code for linear resistor.

Listing B.5 is the pseudo code for the generation of partially-overlapped devices.

```
# pcell name: pcell-ws,
# purpose: width and spacing of the layer
# technology: TDK4PE Barcelona - Inkjet
# V1.0  2013/07/10 by Mohammad Mashayekhi

# Import the db wrappers
from ui import *

# The entry point. The function name *must* match the filename.
def WS_vertical_Met1(ccv, w=100, s=100, l=2500, material="Metal1",
    num_reps=10) :

    lib = ccv.lib()
    dbu = lib.dbuPerUU()
    tech = lib.tech()

    # dbu conversions
    width = int(w * dbu)
    space = int(s * dbu)
    length = int(l * dbu)
    layer = tech.getLayerNum(material, "drawing")

    # Create first rectangle object (not actually drawing it)
    rect = Rect(0, 0, width, -length)
    for i in range(num_reps):

        # Draw rectangle
        ccv.dbCreateRect(rect, layer)

        # Move rectangle origin
        rect.offset(space + width, 0)

    ## Update the bounding box
    ccv.update()
```

Listing B.1 PCells code of width and spacing test vehicle

```
...

def script_ws(ccv, pcell_name="pcell-ws") :

    # load the pcell
    ui().loadPCell(lib.libName(), pcell_name)
    origin = Point(0,0)

    x_parameter = "w"        # parameters to modify along x axis
    x_variations = 5         # number of variations along x axis
    initial_x = 40           # initial x parameter
    delta_x = 40             # parameter variation along the x axis
    y_parameter = "s"        # parameters to modify along y axis
    y_variations = 3         # number of variations along y axis
    initial_y = 80           # initial y parameter
    delta_y = 80             # parameter variation along the y axis
    pitch_x = 6000           # x separation between instances
    pitch_y = 3500           # y separation between instances
    y_tags = "ABCDEFGHIJKLMNOPQRST" # instance labeling

    output_file = 'C:/.../script_ws.txt' #  TVD file
    f = open(output_file, 'w')

    # Double loop instantiating PCell instances
    for j in range(int(y_variations)) :
        for k in range(int(x_variations)) :

            # Calculate position of each instance
            xpoint = k*pitch_x
            ypoint = -j*pitch_y
            origin = Point(xpoint*dbu, ypoint*dbu)

            # Calculate pcell parameters and update TVD
            x_value = initial_x + k * delta_x
            y_value = initial_y + j * delta_y
            f.write(str(xpoint) + ', ' + str(ypoint) + ', ' + y_tags[j]
   + str(k) + ', w=' + str(x_value) + ' s=' + str(y_value) + '\n')

            # Instantiating PCell and setting its parameters
            celltest = ccv.dbCreatePCellInst(lib.libName(), pcell_name,
   "layout", origin)
            celltest.dbReplaceProp(x_parameter, x_value)
            celltest.dbReplaceProp(y_parameter, y_value)
            ccv.dbUpdatePCell(celltest)

    f.close()
```

Listing B.2 Script for generation of width and spacing test vehicle matrix

```
#TVD file generated on 2013/10/23
# Design Rules test vehicle - width and spacing
# X, Y, ID, w, s
0,        0,      A0,      w=40,     s=80
6000,     0,      A1,      w=80,     s=80
12000,    0,      A2,      w=120,    s=80
18000,    0,      A3,      w=160,    s=80
24000,    0,      A4,      w=200,    s=80
0,       -3500,   B0,      w=40,     s=160
6000,    -3500,   B1,      w=80,     s=160
12000,   -3500,   B2,      w=120,    s=160
18000,   -3500,   B3,      w=160,    s=160
24000,   -3500,   B4,      w=200,    s=160
0,       -7000,   C0,      w=40,     s=240
6000,    -7000,   C1,      w=80,     s=240
12000,   -7000,   C2,      w=120,    s=240
18000,   -7000,   C3,      w=160,    s=240
24000,   -7000,   C4,      w=200,    s=240
```

Listing B.3 TVD file for width and spacing test vehicle matrix

```
...
def rlin_lw(ccv, w=200, l=1000, wcon=1000, lcon=750) :
    DR0 = R1_W #DesignRule0: minimum width of RESIS1
  ...
    # design rules check
    if w < DR0.value :
        w = DR0.value
        ccv.dbReplaceProp("w", w)
        print DR0.error_mssg, "Setting w to", w, "um"
        ccv.update()
  ...
    # Print resistance info
    rlin = rsh*l/w
    rcon = 1000*rcons/(w*DR3.value)
    print "rlinw parameters: l =", l, "um; w =", w, "um; rlin =", rlin,
   "ohm; rcon = 2 *", rcon, "mohm."

    # X & Y bounds definition
    a_x = lport - overl_resmet1 - diext_overes
    b_x = a_x + diext_overes

    # Layout generattion: e.g, Create resistor strip
    layer = tech.getLayerNum(rlayer, "drawing")
    rect = Rect(b_x, -a_y, e_x, a_y)
    ccv.dbCreateRect(rect, layer);
  ...

    # Resistor label
    layer = tech.getLayerNum(tlayer, "drawing")
    ltext = "l=" + str(l) + "u w=" + str(w) + "u"
    labelpoint = Point((c_x + d_x)/2, -50*dbu)
    label = ccv.dbCreateLabel(labelpoint, ltext, R0, 0.05*dbu, 4, layer)
  ...

    ## Update the bounding box, and center all PCell elements
    ccv.update()
```

Listing B.4 PCell code for linear resistor

```
# Cell Name: Interdigitated PO_OTFT, Technology: NeuDrive-CPI
# v0.1 2015/05/21 by M.Mashayekhi

from ui import *
def po2(cv, w=100, l=4, nf=4, gt=100) :

  ...

    # Active area
    layer = tech.getLayerNum(clayer2, "drawing")
    rectangle = Rect( (-w/2)*dbu, 0, (w/2)*dbu, (6*(nf+1)+(2*ext)+(nf)*l)*dbu)
    cv.dbCreateRect(rectangle, layer)

    # Source/ drain electrodes
    layer = tech.getLayerNum(clayer1, "drawing")
    rectangle = Rect( (-6-l-ext-w/2)*dbu, ext*dbu, (-l-ext-w/2)*dbu, (-ext+6*(nf+1)+(2*ext)+(nf)*l)*dbu)
    rectangle = Rect( (l+ext+w/2)*dbu, ext*dbu, (6+l+ext+w/2)*dbu, (-ext+6*(nf+1)+(2*ext)+(nf)*l)*dbu)
    cv.dbCreateRect(rectangle, layer)

  # fingers
    if (nf % 2 == 0): #even
        for i in range(nf/2+1):
            layer = tech.getLayerNum(clayer1, "drawing")
            rectangle = Rect( (-l-ext-w/2)*dbu, (ext+(i)*2*(l+6))*dbu, (w/2+ext)*dbu, (6+ext+(i)*2*(l+6))*dbu)
            cv.dbCreateRect(rectangle, layer)

        for i in range(nf/2):
            layer = tech.getLayerNum(clayer1, "drawing")
            rectangle = Rect( (-ext-w/2)*dbu, ((ext+6+l)+(i)*2*(l+6))*dbu, (w/2+ext+l)*dbu, ((ext+12+l)+(i)*2*(l+6))*dbu)
            cv.dbCreateRect(rectangle, layer)
    else: #odd
        for i in range((nf+1)/2):
            layer = tech.getLayerNum(clayer1, "drawing")
            rectangle = Rect( (-l-ext-w/2)*dbu, (ext+(i)*2*(l+6))*dbu, (w/2+ext)*dbu, (6+ext+(i)*2*(l+6))*dbu)
            cv.dbCreateRect(rectangle, layer)

        for i in range((nf+1)/2):
            layer = tech.getLayerNum(clayer1, "drawing")
            rectangle = Rect( (-ext-w/2)*dbu, ((ext+6+l)+(i)*2*(l+6))*dbu, (w/2+ext+l)*dbu, ((ext+12+l)+(i)*2*(l+6))*dbu)
            cv.dbCreateRect(rectangle, layer)

  ...

    cv.update()
```

Listing B.5 PCell code for generation of parametrized interdigitated partially overlapped OTFT

Appendix C

Standard cell library

Application Specific Printed Electronic Circuits (ASPEC), which is a circuit designed and customized for a special application rather than intended for general-purpose use, is the equivalent term for ASIC but for printed electronics. Standard cell library for printed electronics is a set of basic digital logic gates to build any required combinational and sequential circuits.

Standard cell design methodology allows full automation of the physical design process using automated place and route EDA tools. In addition, it significantly helps speeding up the circuit development time as the blocks can be synthesized from high level description (Verilog, VHDL) using the library. This design methodology increases the circuit reliability, in the sense that the design process is less error-prone considering that the cells are pre-designed and verified.

In this section, we are trying to extend the digital design for organic electronics by presenting an ASIC-like standard cell library, and a fully automated design flow to synthesize ASPECs. The proposed library is developed under the data models and formats currently used by the ASIC tools and design flows. This allows the use of VLSI tool chains o design and synthesize ICs for ASPECs by applying the well-established automated design flow from ASIC industry.

Library overview

The proposed standard cell library is based on the clean room photolithography process with $4\mu m$ channel length, similar to the one in previous sections. Lack of a reliable transistor model and circuit simulation has made the job difficult for the circuit designers to design logic gates with accurate transistor dimensions and drive to load ratio. According to And-Inverter-Graph (AIG), which is a graph that represents a

structural implementation of the logical functionality of a circuit network, any network of logic gates can be expressed in terms of AND (which is NAND+INV) gates and inverters. This conversion does not lead to unpredictable increase in memory use and run time, but an efficient representation in comparison with other forms.

For two above-mentioned reasons and also the technology limitations, inverter and nand logic gates, which show better static and dynamic performance, tend to be the most reliable logic gates for the proposed standard cell library. Therefore, the initial version of the standard cell library consists of 4 combinational gates of inverter, nand2, nand3, and nand4, plus a D flip flop for sequential circuits, and filler cells. However, more logic gates such as, NOR2, NOR3, NOR4, XOR, XNOR, OAI, AOI, MUX, Adder, and Latch (most of them in two different drive strengths) are under development, in order to extend the library to more complex gates. Table C.1 lists the existing cells in the library, as well as transistor count and geometrical information. The height of all the cells are fixed to $450 = \mu m$.

Table C.1 List of developed cells in the library

Cell name	Function	Transistor count	Cell width (μm)
INV	Inverter gate	2	400
NAND2	2 input NAND gate	3	475
NAND3	3 input NAND gate	4	525
NAND4	4 input NAND gate	4	575
DFF	D flip flop with reset and enable	39	2150
Fill	Filler cell	0	100

In order to be used together, as the building blocks of a circuit, cells have to share some common characteristics to constitute a library. These shared characteristics among the cells are thought to make shorter the design time without decreasing the quality of result and circuit reliability. This can be achieved, for instance, by allowing routing of power rails by abutment or even establishing simple patterns when designing cells' I/O pins. The name commonly attributed to this set of standard positions and dimensions to be respected by the cells from a library is the library template.

Figure C.1 shows the template adopted in the proposed library (inverter in this case). The developed cells are 14 metal tracks tall with a variable width corresponding to an integer number of placing grid sites. Since the adopted technology has only two routing (MET1, MET3) layers and both of them are used into cell layouts, the I/O pins are designed in such a way that they could be accessed for routing both above and below the power lines, whereas routing blockages are drawn in between power lines.

This architecture features two wide power tracks and each I/O pin has 2 available routing points inside cell boundary plus 2 more optional ones.

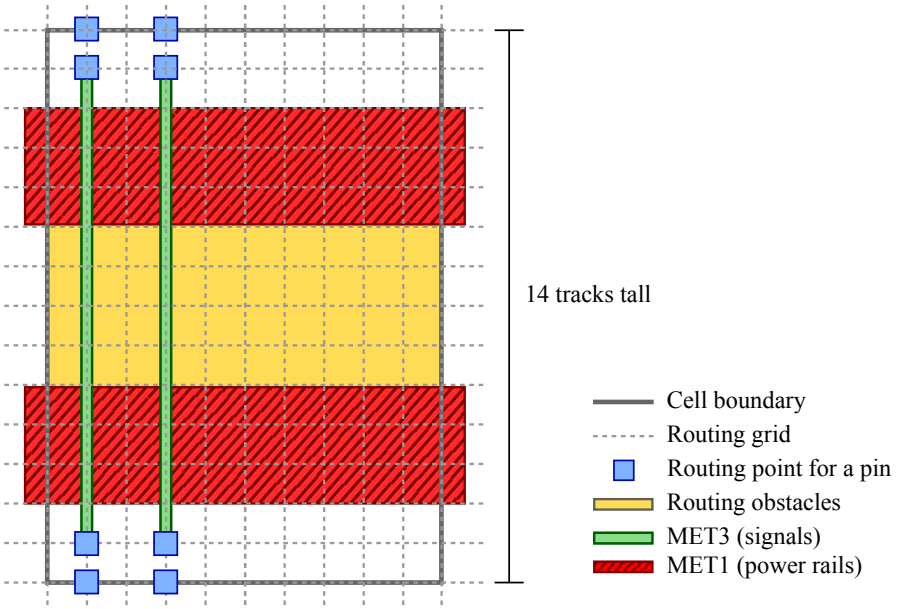


Fig. C.1 Cell abstract of the designed inverter, illustrating the proposed physical template

The developed library is described in all necessary views to perform the usual tasks involved in ASIC commercial flows for integrated circuit designs. The main goal is to enable an automated design flow for ASPEC designs by using the same well-established ASIC design flow, tools and I/O files. In this sense, the proposed library views are presented in Table C.2.

Table C.2 List of developed views in the proposed standard cell library

View Name	Extension	View Description
Technology Lib.	*.lib*	Logic, timing, power and area information of the cells
Geometric Lib.	*.lef*	Information about the physical layout: DRC and abstract info
Simulation Lib.	*.v*	Behavioral information of the cells for simulation intents
Cell Netlists	*.spi*	Instance-based transistor netlist: instances, nets, and attributes
Cell Layouts	*.gds*	Planar geometric shapes, labels, and etc. in a binary format

Static and dynamic characterization of the cells have been shown in previous section. Different timing and power characterization of the cells have been and are being developed and are not shown here, as they are out of the main scope of the thesis.

Automated design flow

Figure C.2 is the proposed automated design flow, adopted from regular ASIC design flow.

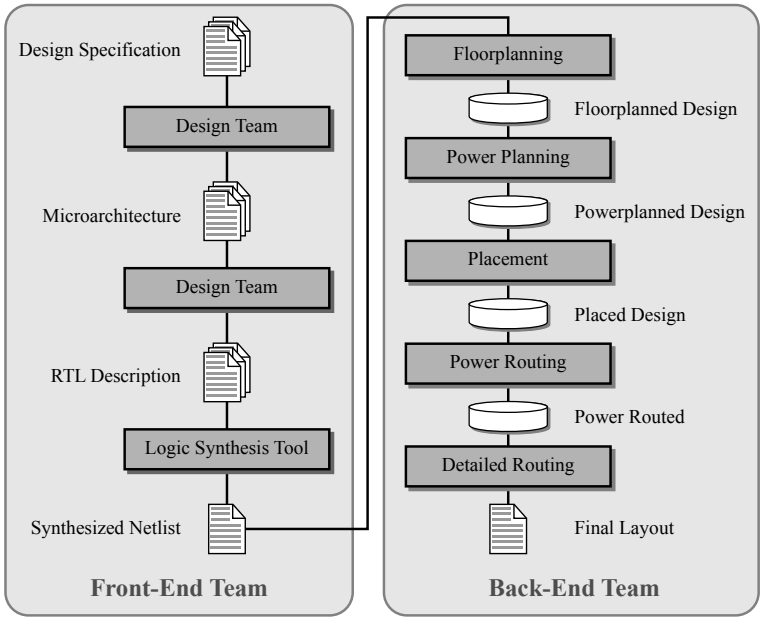
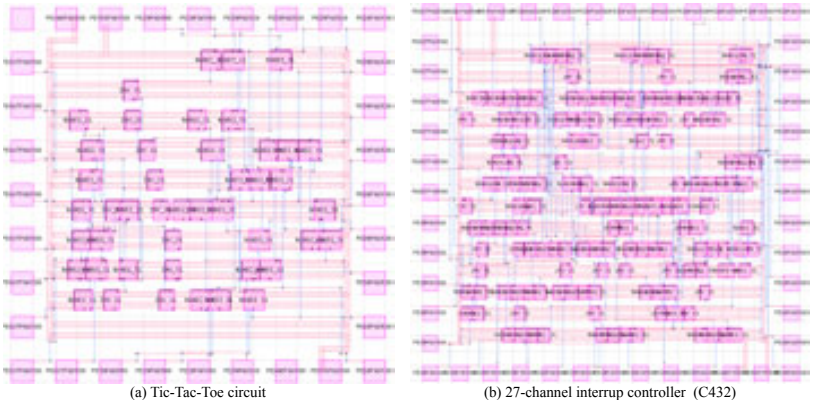


Fig. C.2 Proposed automated design flow, adopted from regular ASIC design flow

Implemented circuit

As a proof of concept, we have designed a 27-channel interrupt controller and Tic-Tac-Toe game circuit by using the proposed standard cell library (Figure C.3).



(a) Tic-Tac-Toe circuit (b) 27-channel interrup controller (C432)

Fig. C.3 Implemented benchmark circuits by using the proposed standard cell library