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On the Source of Oscillatory Behaviour during Switching of Power Enhancement Mode GaN HEMTs

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Abstract: With Gallium Nitride (GaN) device technology for power electronics applications being ramped up for volume production, an increasing amount of research is now focused on the performance of GaN power devices in circuits. In this study, an enhancement mode GaN high electron mobility transistor (HEMT) is switched in a clamped inductive switching configuration with the aim of investigating the source of oscillatory effects observed. These arise as a result of the increased switching speed capability of GaN devices compared to their silicon counterparts. The study identifies the two major mechanisms (Miller capacitance charge and parasitic common source inductance) that can lead to ringing behaviour during turn-off and considers the effect of temperature on the latter. Furthermore, the experimental results are backed by SPICE modelling to evaluate the contribution of different circuit components to oscillations. The study concludes with good design techniques that can suppress the effects discussed.

Keywords: wide band gap semiconductors; III–V semiconductors; gallium compounds; enhancement; GaN; HEMT; switching; parasitics; inductance; SPICE; clamped; Miller capacitance

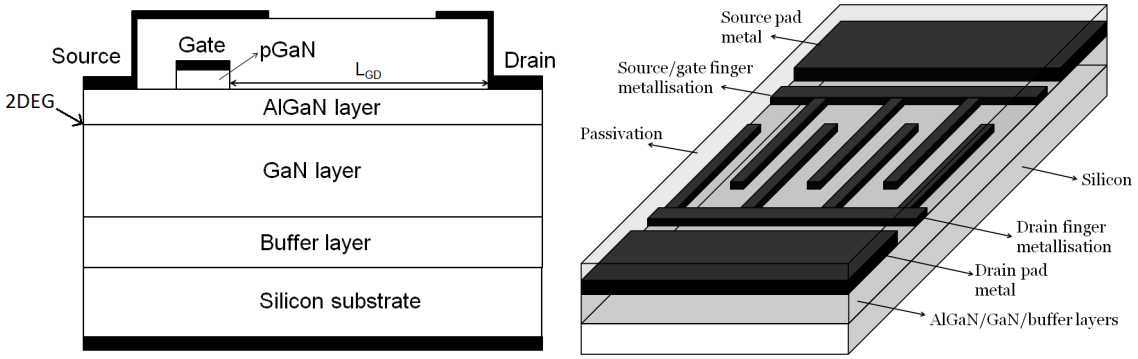
1. Introduction

In the last decade, an extensive amount of research has focused on the development of power devices using AlGaN/GaN heterostructures grown on silicon substrates. In particular, efforts have focused on the development of enhancement mode switches in the 100–650 V range. Devices with very competitive specific R_{on} compared to the existing silicon metal-oxide-semiconductor field effect transistor (MOSFET) technologies have been reported both in academia and industry [1,2]. Additionally, the use of GaN devices can lead to lower switching losses, thus allowing an increase in switching frequency and therefore an overall increase in power density and efficiency of power conversion equipment [3–5]. Therefore, with GaN device technology being ramped up for volume production an increasing amount of research is now focused on the performance of GaN devices in various power electronic converters such as, boost, buck-boost, half-bridge and indirect matrix inverter topologies [5–7]. This study focuses on the challenges circuit design engineers are presented with when using GaN devices and in particular focuses on how parasitic components can create oscillatory behaviour and therefore lead to additional circuit losses. Ways to optimise the gate drive circuit in order to achieve a robust design are also discussed. Two major sources of ringing are identified in literature [8], one of which relates to the device Miller capacitance and controlling the dV/dt rate and the other relates to the presence of parasitic common source inductance in the circuit. The effects of

these mechanisms were examined for a 650 V enhancement mode GaN HEMT by switching it in an inductive clamped switching configuration both at room and increased temperatures. Extensive SPICE simulations were used to support the analysis.

2. Device Structure and Characteristics

A normally-off HEMT device based on p-gate technology (see cross-section in Figure 1a) was used in this study. The device has a lateral configuration with an AlGaN/GaN heterostructure grown epitaxially on a silicon wafer. A buffer layer is used to allow a high quality GaN layer to be grown despite the significant lattice mismatch between GaN and Si as described in [9]. Finally, a thin cap GaN layer was added at the gate with a high p+ doping concentration to achieve normally-off operation. The device has an inter-digitated layout as shown in the schematic design in Figure 1b and was packaged in TO-220 before characterisation. The device has a voltage and current rating of 650 V and 15 A respectively and an $R_{ds}(on)$ of 130 mΩ.



(**a**) Cross section (**b**) Inter-digitated layout

Figure 1. AlGaN/Gallium Nitride (GaN) heterostructure p-gate enhancement mode high electron mobility transistor (HEMT).

The HEMT device under test differs from a silicon power MOSFET in several aspects. Conduction occurs through a two dimensional electron gas (2DEG) which is formed at the AlGaN/GaN interface [10]. High mobility of carriers ($\mu \approx 1700$ cm^2/Vs) and a shorter drift region for a given breakdown due to higher critical electric field (E_{br} = 3.3 MV/cm) [11] can lead to very low drift region charge, Q_{gd}. Furthermore, the device gate charge Q_g is measured to be 3.1 nC compared to 35 nC in corresponding state of the art silicon devices [12]. As a consequence, the GaN HEMTs can switch at much higher speeds than silicon MOSFETs. A low threshold voltage of 2 V is typically observed in p-gate GaN HEMTs [13,14]. This is also the case in the device under test that shows a threshold voltage of 1.5 V. Furthermore, substantial current leakage is observed through the gate contact at high V_g bias (>8 V) due to the non-insulated gate structure [14] as opposed to a metal-oxide-semiconductor (MOS)-like gate. This results in a narrower operational gate bias window. The internal gate resistance, R_{gi} was measured to be 1.9 Ω. An on-state gate bias voltage of 4 V is applied to achieve minimum $R_{ds}(on)$ and gate leakage. The transfer characteristic and transconductance of the device at a range of temperatures can be seen in Figure 2.

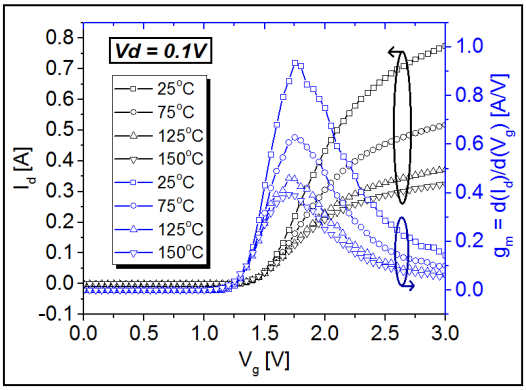


Figure 2. GaN HEMT transfer characteristic and transconductance at room and increased temperatures.

3. Experimental Method

Experimental measurements were carried out using a clamped inductive switching circuit that is shown schematically in Figure 3. The current and voltage waveforms were recorded with a Tektronix DPO5104 oscilloscope. The circuit consists of an external gate resistance (this will be referred to as simply R_g as the same value was used for both R_{gh} and R_{gl} for all measurements) which in association with the internal impedance of the gate driver (R_{sink}—see Figure 3) used has a large influence on the switching performance of the circuit by controlling the switching conditions (dI/dt rate, dV/dt rate). A high-speed MOSFET driver was used (TC4452V, Microchip, Chandler, AZ, USA). The square pulse input to the gate driver was provided by an Agilent 33220A. The main inductor L1 (500 µH) behaves as a constant current source. The HEMT characterised corresponds to the device under test (DUT) shown in the circuit. A silicon carbide diode (C3D10060, CREE, Durham, NC, USA) was used as the clamping diode (D1). Gate voltage was measured with a TPP1000 probe (Tektronix, Beaverton, OR, USA). Drain-source voltage was measured with a TPP0850 probe (Tektronix, Beaverton, OR, USA). The drain current was measured with a TCP0030A current probe (Tektronix, Beaverton, OR, USA) by inserting a wire-bridge in series with the DUT. Power source, circuit and sensing probe related parasitic inductances and capacitances are included in the schematic (C_1, L_d, L_g, L_s, C_{gd}, C_{gs}, C_{ds}, L_2, R_2). To obtain the measurements at increased temperatures the devices were heated in a custom made plastic oven placed on the board. A SPICE model for the device under test was developed by adjusting a model provided by GaN Systems for a 650 V, 15 A E-HEMT (GS66504B, GaN Systems, Ottawa, ON, Canada) and used in LTspice IV. The SPICE model used consisted of a sub-circuit rather than a physical model and allowed adjustments to be made more easily to the internal parasitic inductances (L_{gi}, L_{si}, L_{di}) and resistances (R_{gi}, R_{si}, R_{di}) of the three terminals and the voltage-dependent device capacitances (C_{gdi}, C_{gsi}, C_{dsi}) as illustrated in the schematic in Figure 4a. These components are the result of device design and as such are specific to a given technology. Parasitic inductances and resistances were estimated through measurements and simulations (Q3D extractor, Ansys, Canonsburg, PA, USA). Device capacitances were measured using a Keithley 4200 parameter analyser and are plotted in Figure 4b. Theoretical equations which describe the device capacitance-voltage curves were fitted to the measurements (see Figure 4b) and implemented in the SPICE model. The switching performance of the device was investigated at both device turn-on and turn-off during a double pulse test. A 400 V off-state bias (V_{off}) was used and a range of on-state current values were obtained by adjusting the gate drive pulse width.

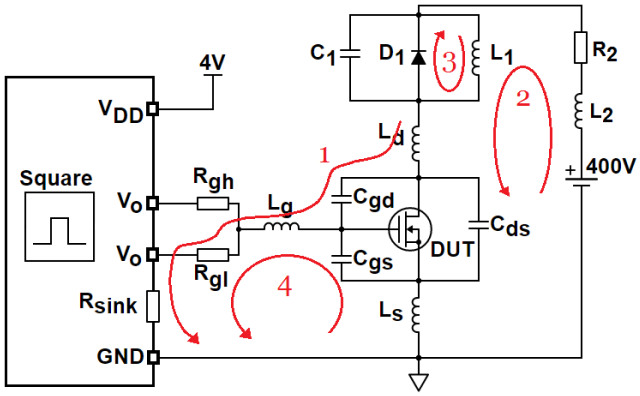
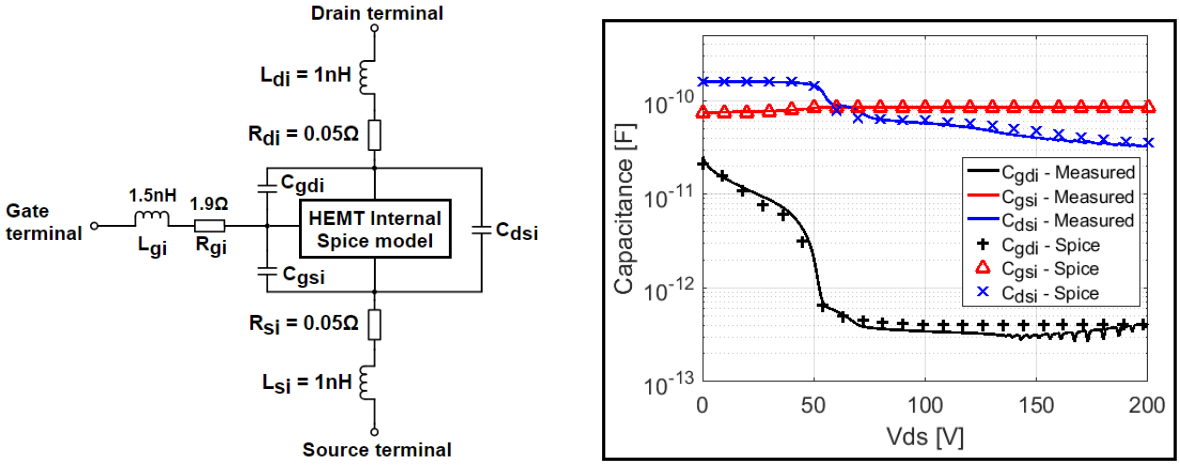


Figure 3. Clamped inductive swithing circuit.



(**a**) HEMT DUT SPICE model (**b**) Measured and SPICE model capacitance

Figure 4. SPICE model parameters adjusted.

4. Results and Discussion

The increased switching speed of GaN devices leads to higher *dV/dt* and *dI/dt* values and can make the circuit more susceptible to oscillatory behaviour. This section focuses on discussing the origins of the oscillations observed, first analysing the relevant effects during device turn-off and then extending the analysis to cover device turn-on. Understanding these effects is a very important step to produce a circuit and device design unaffected by oscillations.

4.1. dV/dt Related Effect

During device turn-off the drain voltage is rising steeply. A high *dV/dt* causes a current to flow through the Miller capacitance (C_{gd}) and then R_g as illustrated by path 1 in Figure 3. A sufficiently high voltage drop across Rg can turn the device on during switching and cause oscillations. Furthermore, as the voltage rises above 400 V the diode turns on abruptly changing the current path in the circuit (from loop 2 to loop 3 as seen in Figure 3) thus creating oscillations as energy is transferred between the passive components in the two current loops. Any ringing in the power loop is also coupled to the gate terminal via the Miller capacitance. These effects were observed very clearly in both experimental results and SPICE simulations.

The waveforms in Figure 5a refer to the simulation of the circuit in Figure 3 and will be used as a reference for the following analysis. The reference values for components in the circuit are as follows: R_g = 68 Ω, L_g = 2 nH, L_s = 3 nH, L_d = 40 nH (note that this includes the parasitic inductance contribution from the current sensing probe used to measure I_d), C_{ds} = 10 pF, C_{gd} = 8 pF, C_{gs} = 5 pF,

C_1 = 20 pF, L_2 = 40 nH, R_2 = 0.5 Ω. In the reference curves it is important to note the negligible ringing on all waveforms. Nonetheless, the switching current level in the reference curves is fairly low (2 A) and as will be described in Section 4.2 current level plays a significant role in the ringing behaviour observed. Furthermore, it is worth pointing out that the starting value of external gate resistance (R_g) used in the model is quite significant. R_g was therefore subsequently modified and its impact on the switching waveforms was studied. R_g was initially decreased from 68 Ω to 50 Ω. This has a significant effect on the drain voltage *dV/dt* which increases from 4.7 V/ns to 6 V/ns. Furthermore, the gate waveform shows a shorter plateau and a slight drain voltage overshoot. However, no significant ringing is observable (not shown here). As the gate resistance is further decreased to 10 Ω a very high *dV/dt* (26 V/ns) results in overshoot of the drain voltage during turn-off and ringing on the drain current. The ringing is coupled on the gate signal through C_{gd} and oscillatory behaviour is also observed on the gate terminal as seen in Figure 5b.

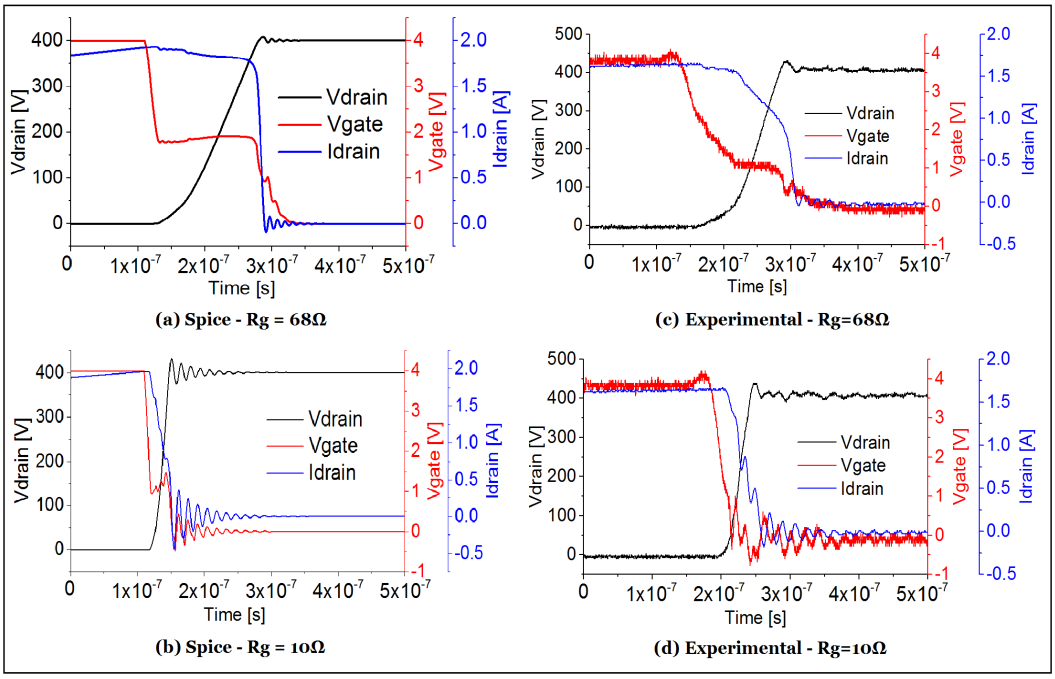


Figure 5. SPICE simulated and experimental HEMT turn-off waveforms: (**a**) SPICE-R_g = 68 Ω; (**b**) SPICE-R_g = 10 Ω; (**c**) Experimental-R_g = 68 Ω; (**d**) Experimental-R_g = 10 Ω.

The same trend was observed when the gate resistance was varied in the experimental circuit. An additional gate resistance (R_g) of 68 Ω produced a *dV/dt* of 6 V/ns which is close to the simulated value and a clean waveform was recorded as seen in Figure 5c. When the resistance was reduced to 10 Ω the *dV/dt* rate increased to 17 V/ns and ringing was observed as seen in Figure 5d. A good match was achieved between experimental measurements and SPICE simulations. Note that the resistance of the driving circuit R_{sink} needs to also be considered in this analysis. A second driver (Microchip TC4432V, Microchip, Chandler, AZ, USA) was used in this study with different current capability/sink resistance. The second driver with higher sink resistance allowed turn-off without ringing with a lower additional gate resistance.

The same source of oscillations was observed during device turn-on. A higher *dV/dt* rate is observed during turn-on both experimentally (22 V/ns) and in SPICE simulations (36 V/ns). A good match was again achieved between SPICE simulations and experimental measurements as seen in Figure 6. A spike is observed in both gate current and drain current. Since a gate voltage spike can damage the device if operated close to the maximum gate bias rating, its possible maximum value should be taken into consideration when choosing a suitable gate drive bias. It is worth mentioning

that a slight discrepancy between the measured and simulated oscillation frequency is observed in Figures 5 and 6. This relates to the values of the parasitic components in the power loop (L_2, C_1, L_d) which may not be fully accounted for in the SPICE model.

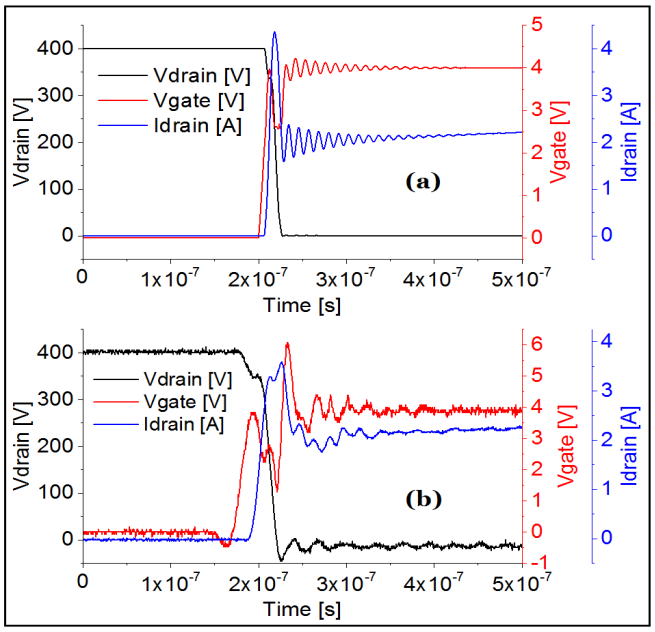


Figure 6. HEMT turn-on waveforms with R_g = 10 Ω: (**a**) SPICE simulation; (**b**) Experimental.

4.2. dI/dt Related Effect

A second area of concern arises due to the inductance-capacitance-resistance (LCR) resonant tank formed by the common source inductance (L_s), gate capacitance, and gate drive pull down loop as seen in path 4 of Figure 3 which needs to be damped in order to avoid an equivalent positive voltage ringing across the gate [8]. L_s is therefore identified as a critical parameter for good performance. During turn-off, *dI/dt* coupled with L_s causes a considerable voltage drop to develop across the inductance with the source voltage V_s swinging negative when referenced to ground. This voltage drop can be seen on the gate voltage waveform (note this is V_g-ground) at the end of the plateau where *dI/dt* is at its peak (300 A/µs) as seen in Figure 5. This gate swing would not be observed without the presence of L_s as an ideal RC gate discharge would be expected (not shown here). This swing is also observed in the experimental turn-off of the device (see Figure 5c) and suggests the presence of a considerable L_s.

Starting again from the reference circuit described in Section 4.1 oscillations arising from the gate loop LCR resonant tank were observed when the switching current level in the SPICE simulation model was increased (from 2 A to 7 A) as seen in Figure 7a. Similar oscillatory behaviour was observed in experimental measurements as can be seen in Figure 7b. Oscillations commenced only as the switching current level was increased due to higher current leading to faster *dI/dt* (I_d = 6.5 A, *dI/dt* = 90 A/µs). Ringing is observed primarily on the gate voltage (V_g) with a frequency of approximately 600 MHz as measured in SPICE. These oscillations could turn the device back on during switching creating additional losses that can raise the temperature via self-heating and eventually cause reliability problems. In addition, slight oscillations are observed in the simulated drain voltage and current which increase in amplitude as switching current level is increased further. It is important to highlight that oscillations on current waveform observed in the simulations may not be observable in experimental measurements due to the bandwidth of the current probe used. In fact, the current probe used in this experiment had a maximum bandwidth up to 120 MHz while the frequency of the oscillations as measured from the drain voltage ringing is approximately 700 MHz, which is very close to the simulated value. To verify the cause of the oscillations in the experimental circuit, parasitic inductance

in the form of a wire was added between source and ground. This led to ringing becoming much more severe and appearing at lower current levels as expected. The same trend was observed when Ls was more easily varied in the SPICE model (not shown here).

The turn-on of the device was also investigated under these conditions and oscillations were again observed both experimentally and in SPICE simulations as seen in Figure 7c,d. Equivalently to the turn-off, the turn-on associated oscillations were found to be dependent on the *dI/dt* rate. During the turn-on, however, the *dI/dt* rate was found to be higher than during turn-off (I_d = 6 A, dI/dt = 105 A/µs) leading to oscillations generated at a lower current level than during turn-off.

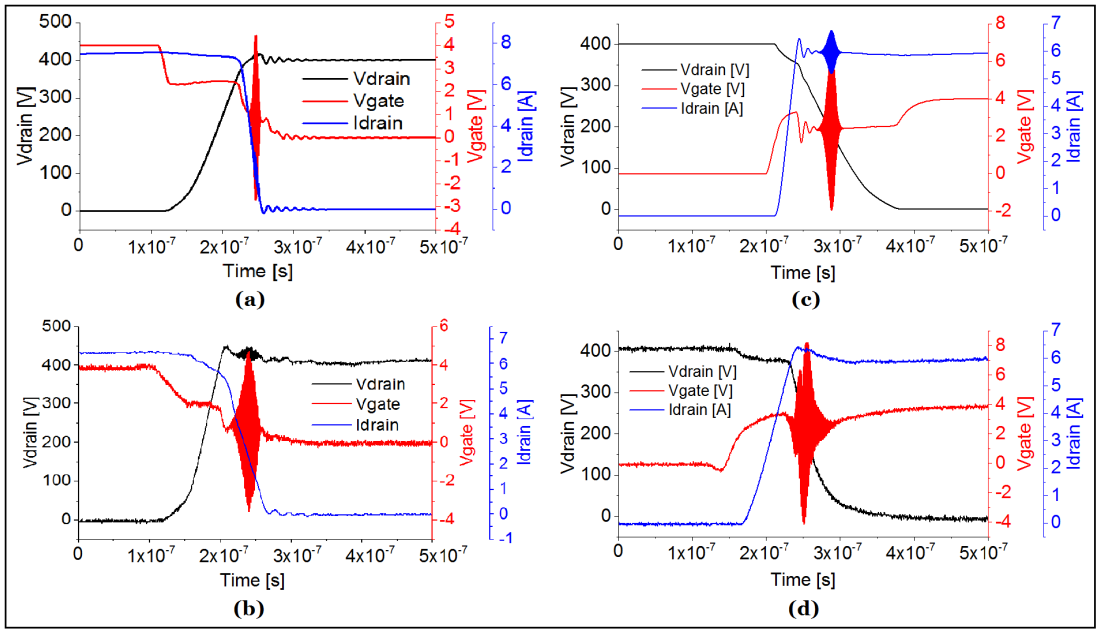


Figure 7. *dI/dt* related oscillations in SPICE simulated and experimental HEMT turn-off and turn-on waveforms: (**a**) SPICE turn-off; (**b**) Experimental turn-off; (**c**) SPICE turn-on; (**d**) Experimental turn-on.

Increased Temperature

The effect of temperature on oscillations caused by the parasitic common source inductance was also investigated. It is observed that the maximum current level that can be switched without the presence of ringing increases with increasing temperature. Figure 8 shows switching at a current level of 5 A where ringing is observed at room temperature but no such ringing is observed at a temperature of 150 °C. It is interesting to note the appearance of oscillations at a lower current level compared to Figure 7b. These turn-off measurements were taken using a second HEMT device with a higher internal parasitic inductance further confirming the analysis in Section 4.2. The *dI/dt* rate is lower at increased temperature and falls to 66 A/µs compared to 81 A/µs at room temperature. This could be a result of the increase in gate metallisation resistance observed at increased temperature and can thus be the reason behind the improved stability observed at higher temperature. Furthermore, as observed in Figure 2 the transconductance in the device is reduced at increased temperatures and this can also account for a reduction in oscillations observed as demonstrated in [15].

It is therefore important to understand that in this instance, a self-heating effect created by the presence of oscillations which can lead to additional losses, can act as to reduce the oscillations present when switching. Nonetheless, self-heating can lead to other adverse effects such as increase in device R_{on}, increased probability for time dependent dielectric breakdown and higher overall losses.

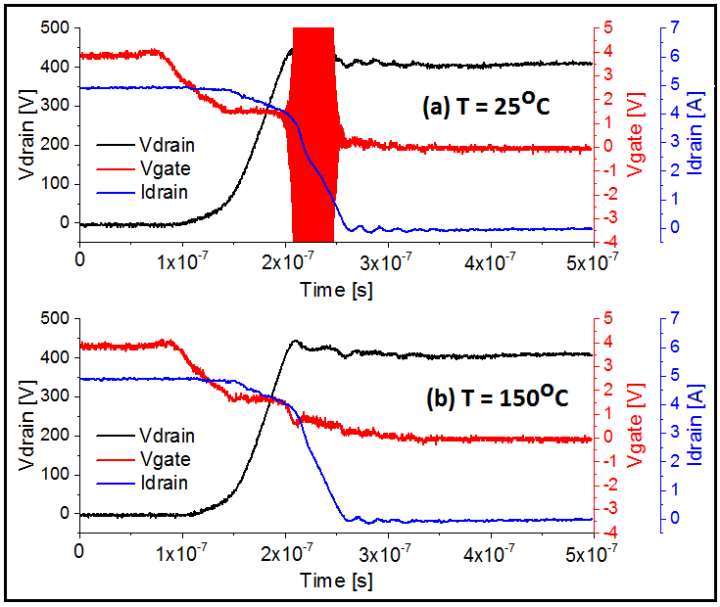


Figure 8. Effect of temperature on experimental turn-off waveforms of HEMT device.

4.3. Good Design Suggestions

4.3.1. Optimising Gate Drive Circuit to Address dV/dt Related Ringing

An optimised circuit is more immune to ringing caused by dV/dt effect as discussed in Section 4.1 if:

- R_1 is high enough to control dV/dt, but not too high to generate a significant voltage drop when the discharge current of C_{gd} is flowing through. A trade-off is thus revealed. To allow stable switching the rate of switching of the device needs to be reduced however this can lead to increased losses.
- Smart driving is used such as an active Miller clamp function as seen in commercially available drivers (e.g. FOD8318, Fairchild, Sunnyvale, CA, USA). This function avoids a large C_{gd} discharge current flowing through R_1 by grounding the gate through the turn-on of a transistor when a certain voltage is developed across R_1.
- Gate inductance L_g is minimised as SPICE simulations reveal that gate inductance acts as to increase the amplitude of the oscillations observed. This is a result of the storage of energy when current is flowing through L_g.
- The gate is driven to a negative voltage at turn-off to ensure unwanted device turn-on is avoided. This can however add cost and complexity to the design [16].

4.3.2. Use of Ferrite Bead to Address dI/dt Related Ringing

As discussed in Section 4.2 it becomes apparent that to achieve a good design it is essential to reduce L_s as much as possible. Nonetheless, other solutions that can lead to a more robust design should also be considered. Increasing the gate drive sink resistance can help damp the LCR resonance however that could create other issues as described in Section 4.1. The addition of a ferrite bead that is resistive at the resonant frequency can achieve the same result with less increase in Miller turn-on sensitivity [8]. A ferrite bead exhibits three response regions: inductive, resistive and capacitive depending on the signal frequency as can be seen in Figure 9 [17]. The appropriate ferrite bead has to be chosen in order to be resistive in the range of frequency at which the oscillations occur. A ferrite bead by Tai Tech Advanced Electronics was used in the experimental set-up [18]. A SPICE model for the particular component was not available so the model of a ferrite bead with similar characteristics by Wurth Electronics was used in the simulation circuit [19].

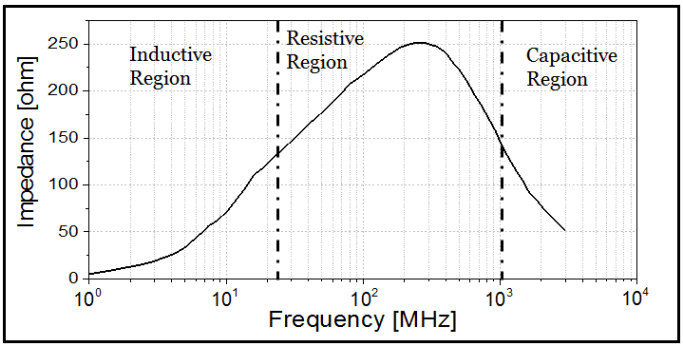


Figure 9. Ferrite bead impedance against signal frequency.

The effect of the bead in successfully damping the oscillations observed was verified using both the SPICE circuit and experimental measurements. In the SPICE model, the ferrite bead was added to the gate track and optimized for the frequency at which oscillations were observed (600 MHz). The resulting waveform can be seen in Figure 10a.

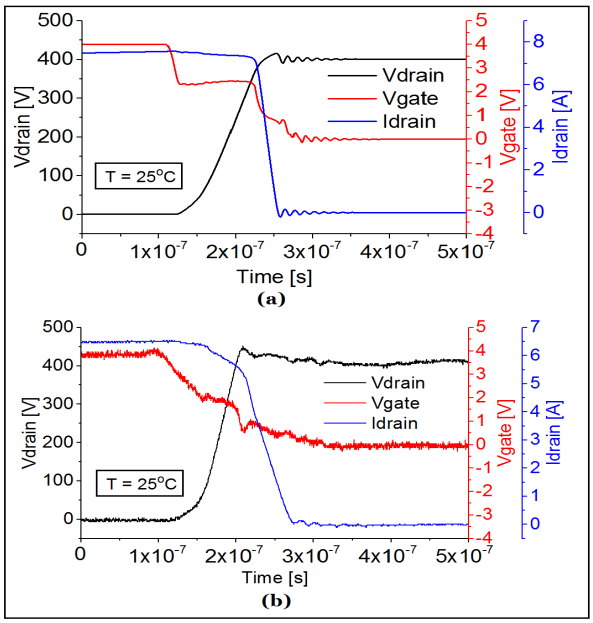


Figure 10. Effect of ferrite bead on ringing observed in (**a**) SPICE simulated and (**b**) experimental circuit turn-off waveforms seen in Figure 7a,b.

In the experimental circuit the bead was placed around the gate leg of the TO-220 package of the device. The resulting switching turn-off waveform can be seen in Figure 10b. Oscillatory behaviour was successfully eliminated in both the experimental results and the SPICE simulations illustrating the effectiveness of the ferrite bead.

5. Conclusions

Two major issues, *dV/dt* and *dI/dt* induced oscillations that arise as a result of the increased switching speed capability of GaN devices compared to their silicon counterparts are identified experimentally and successfully modelled in SPICE. These issues were revealed by investigating the turn-off and turn-on of a GaN E-HEMT device during a double pulse test in a clamped inductive switching configuration. Limiting the current through the device Miller capacitance and therefore a control of the drain voltage rise (*dV/dt*) during turn-off are essential in achieving a good circuit design.

Furthermore, the need to minimise the common source inductance in order to avoid severe ringing on the gate waveform is also demonstrated. The use of a ferrite bead in order to damp the oscillation observed has also been illustrated. Finally, it is shown that more robust switching is possible when the device operates at an increased temperature. The self heating effect is, in this respect, beneficial as it can reduce the oscillations.

Author Contributions: Gianluca Camuso, Loizos Efthymiou, Giorgia Longobardi and Florin Udrea conceived the experiments, Gianluca Camuso and Loizos Efthymiou designed the experiments, Terry Chien and Max Chen provided the devices under test, Loizos Efthymiou and Gianluca Camuso performed the experimental measurements, Gianluca Camuso and Loizos Efthymiou performed the SPICE simulations, Gianluca Camuso, Loizos Efthymiou, Giorgia Longobardi and Florin Udrea analysed the data with contributions from Terry Chien and Max Chen, Loizos Efthymiou wrote the paper, Gianluca Camuso, Giorgia Longobardi and Florin Udrea proofread the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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