Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics

DOI:
10.1063/1.4991919

Document Version
Accepted author manuscript

Digital power and performance analysis of inkjet printed ring oscillators based on electrolyte-gated oxide electronics

Gabriel Cadilha Marques,[1,2,a)] Suresh Kumar Garlapati,[2,b)] Simone Dehm,[2] Subho Dasgupta,[2,c)] Horst Hahn,[2,d)] Mehdi Tahoori,[1] and Jasmin Aghassi-Hagmann[2,3]

[1)] *Chair of Dependable Nano Computing (CDNC), Department of Computer Science, Karlsruhe Institute of Technology (KIT), Karlsruhe 76131, Germany*

[2)] *Institue of Nanotechnology (INT), Karlsruhe Institute of Technology (KIT), Eggenstein-Leopoldshafen 76344, Germany*

[3)] *Department of Electrical Engineering and Information Technology, Offenburg University of Applied Sciences, Offenburg 77652, Germany*

Printed electronic components offer certain technological advantages over their silicon based counterparts, like mechanical flexibility, low process temperatures, maskless and additive manufacturing possibilities. However, to be compatible to the fields of smart sensors, Internet of Things and wearables, it is essential that devices operate at small supply voltages. In printed electronics mostly silicon dioxide or organic dielectrics with low dielectric constants have been used as gate isolators, which in turn has resulted in high power transistors operable only at tens of volts. Here, we present inkjet printed circuits which are able to operate at supply voltages as low as ≤ 2 V. Our transistor technology is based on lithographically patterned drive electrodes, the dimensions of which are carefully kept well within the printing resolutions; the oxide semiconductor, the electrolytic insulator and the top-gate electrodes have been inkjet printed. Our inverters show a gain of ~ 4 and 2.3 ms propagation delay time at 1 V supply voltage. Subsequently built 3-stage ring oscillators start to oscillate at a supply voltage of only 0.6 V with a frequency of ~ 255 Hz and can reach frequencies up to ~ 350 Hz at 2 V supply voltage. Furthermore, we have introduced a systematic methodology for characterizing ring oscillators in the printed electronics domain, which has been largely missing. Benefiting from this procedure, we are now able to predict the switching capacitance and driver capability at each stage, as well as the power consumption of our inkjet printed ring oscillators. These achievements will be essential for analyzing the performance and power characteristics of future inkjet printed digital circuits.

The application domains such as Internet of Things (IoT), smart sensors and wearables may benefit from printed electronics (PE) technology where the devices can be printed onto flexible or rigid substrates. Most of the devices in PE, are based on organic materials and suffer from high supply voltage requirements (> 10 V).[1–3] On the other hand, some examples of low voltage organic devices can also be found in the literature.[2,4–10] The reasons behind the need of high supply voltages is the low carrier mobility of p-type organic materials and low performance of printed or vacuum deposited gate dielectrics that have been used. In addition the scarcity of n-type organic semiconductors and p-type inorganic semiconductors leads to missing complementary circuits in both domains,[11] except their realization in hybrid systems.[2,12]

Lithographically patterned ring oscillator structures based on organic field-effect transistors (OFETs) are able to perform at high frequency (200 kHz) but at the same time require high supply voltage (-60 V).[13] All-printed ring oscillators, where the passive structures are also printed, based on OFETs operate at high supply voltages (~ -40 V) with frequencies below 5 Hz.[14,15] An OFET based 11-stage ring oscillator operating at only 3 V supply with a frequency of 1.7 Hz was also reported in literature.[7] By using an complementary design, the frequency was increased to ~ 22 Hz.[5] Xia et al. achieved reasonable performance (~ 150 Hz) at 2 V supply voltage with ring oscillators based on electrolyte-gated OFETs.[16]

Owing to the advantage of low voltage operation with electrolyte-gating, we design our circuits with electrolyte-gated transistors (EGFETs). In addition, our EGFETs have an n-type, precursor derived indium oxide (In_2O_3) channel; polycrystalline indium oxide is known to exhibit very high mobility values, of the order of 100 cm^2/Vs,[17,18] which is in fact the main difference of the present technology over the previously mentioned organic electronic circuits.[16] Moreover, due to the huge gate capacitance (4.33 $\mu F/cm^2$),[18] we are able to design circuits operating at a supply voltage of < 2 V.[19–21] It is expacted that our devices are stable in air over a month as published previously for a similar device architecture.[22]

To build an inverter, the EGFET is combined with a resistor (transistor-resistor logic).[20] In complementary technology, an inverter consists of a p-type transistor to pull up and a n-type transistor to pull down the signal.[23] In oxide electronics equal-performance p-type EGFETs do not exist; their electrical performance is orders of magnitudes lower than for n-type EGFETs. Earlier some of the authors have demonstrated complementary inverter

[a)] gabriel.marques@kit.edu

[b)] School of Chemistry, Faculty of Science and Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

[c)] Department of Materials Engineering, Indian Institute of Science, Bangalore 560012, India

[d)] KIT-TUD Joint Research Laboratory, Institute of Materials Science, Technische Universität Darmstadt (TUD), Darmstadt 64287, Germany

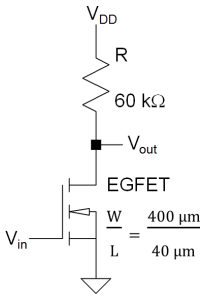


Figure 1. Schematic of an inverter in resistor-transistor logic.

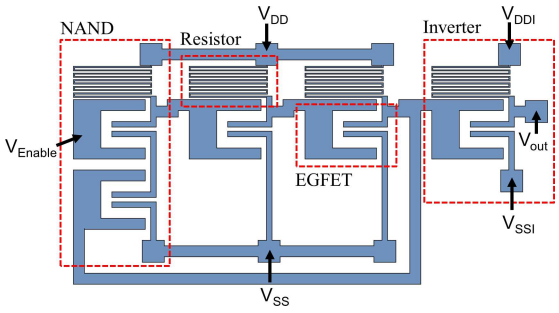


Figure 2. Layout of a three stage ring oscillator.

based on oxide semiconductors,[24,25] however, the p-type transistor have not been fully reliable to drive the current needed in a ring oscillator structure.

In our design, the resistor is chosen to be 60 kΩ, the channel width (W) 400 μm and the channel length (L) 40 μm (Fig. 1). For an applied input voltage (V_{in}) below the EGFETs threshold, the channel is not formed and the output node (V_{out}) is pulled up to the supply voltage (V_{DD}). With increasing input voltage, the channel of the EGFET will become more conductive and the output node will be pulled down to the source supply (V_{SS}).

Accordingly, an inverter is able to flip the input signal from *logic* 0 to *logic* 1 and vise versa. The *logic* 1 value is defined by the supply voltage and the *logic* 0 value by the source supply, which is grounded here. A signal transition at the input will have a delayed feedback at the output. The time it takes for a signal to propagate from the input to the output is then defined by the propagation delay time (τ_p):

$$\tau_p = \frac{\tau_{P10} + \tau_{P01}}{2}, \tag{1}$$

where τ_{P10} and τ_{P01} are the response times for *logic* 1 to *logic* 0 and *logic* 0 to *logic* 1 transitions at the output. The τ_{P10} and τ_{01} response times are measured as time difference between the input and output at 50 % swing. The propagation delay basically results from the switching capacitance C_{SW} of the inverter which needs to be charged or discharged over a transition. The switching capacitance contains all input capacitances of gates connected to the output node, parasitic and wiring capacitances.[23]

Next, we have built 3-stage ring oscillators. Ring oscillator structures are key circuit structures to characterize the process, technology as well as circuit parameters, such as minimum supply voltage and power/performance. The measured frequency of the output signal is the summation of the propagation delay time of each inverter stage.[23] In ring oscillator circuits, an odd number of inverters are connected in series and the output of the last inverter is wired to the input of the first one. When the supply voltage is applied, the ring oscillator starts to oscillate with the frequency defined by the delay of each inverter stage.

As can be seen in the Layout (Fig. 2), our 3-stage ring oscillator is connected to an output stage. The additional inverter at the output ensures that the oscillation is not influenced by the measurement set-up. Moreover, the first stage of the ring oscillator is a NAND-gate instead of an inverter. With the NAND-gate as the first stage it is possible to switch the oscillation on and off. If the first input of the NAND-gate (V_{enable}) is set to *logic* 0, the output of the NAND-gate is always *logic* 1 and the ring oscillator stops oscillating (quiescence state). In the case of V_{enable} is set to *logic* 1, the NAND-gate acts as an inverter and the ring oscillator oscillates (active state).[26,27]

The NAND-gate is used to measure the quiescent (I_{DDQ}) and active (I_{DDA}) currents drawn by the ring oscillator when operating in static or in dynamic mode, correspondingly. With the quiescent and active currents it is possible to quantify the current flow through the ring oscillator during switching:

$$I_{SW} = I_{DDA} - I_{DDQ}\,\frac{2\alpha}{2\alpha+1}, \tag{2}$$

where $2\alpha + 1$ is the number of stages and α is a constant.[26,27]

The static power dissipation of the ring oscillator is

$$P_{stat} = I_{DDQ}\,V_{DD}, \tag{3}$$

while the active power consumption is determined by

$$P_{dyn} = C_{SW}\,V_{DD}^2\,(2\alpha+1)\,f = I_{SW}\,V_{DD}, \tag{4}$$

where C_{SW} is the switching capacitance and f is the frequency of the ring oscillator.[26,27] The total power consumption is then the sum of the static and dynamic power:

$$P_{tot} = P_{stat} + P_{dyn} \tag{5}$$

Throughout operation the switching capacitance, present at each stage is expressed as

$$C_{SW} = \frac{I_{SW}}{V_{DD}}\,2\tau_p, \tag{6}$$

where the propagation delay

$$\tau_p = \frac{1}{2\,(2\alpha+1)\,f} \tag{7}$$

is the weight time for the charging-discharging process.[26,27]

In general, a signal delay can be described with a resistor-capacitance replacement circuit ($\tau = RC$). Therefore using Equations (6) and (7), the switching resistance is given by:[26,27]

$$R_{SW} = \frac{V_{DD}}{2\,I_{SW}}. \tag{8}$$

In order to fabricate the devices, the passive structures (resistors, drain and source electrodes) have been patterned by e-beam lithography on a sputtered indium tin oxide (ITO) glass substrate. Next, an indium oxide precursor ink is inkjet printed between source and drain electrodes using Dimatix 2831 printer. The indium oxide precursor ink is made by dissolving indium nitrate salt (0.05 M $In(NO_3)_3 \cdot xH_2O$) in de-ionized water and glycerol (4:1), stirred for 2 hours and filtered. After printing the channel, the substrate is annealed at 400°C for 2 hours.[18,20] Here, the process temperature is higher than most of the polymer substrates can tolerate. However, by the use of indium oxide nanoparticle channel instead of indium oxide precursor inks, it is possible to reduce the process temperature even down to room temperature.[24] On top of the channel a lithium ion-conducting composite solid polymer electrolyte (CSPE) is printed and dried at room temperature.[18,20] The CSPE consists of 0.3 g polyvinyl alcohol (PVA) dissolved in 6 g dimethyl sulfoxide (DMSO) and 0.07 g lithium perchlorate ($LiCLO_4$) dissolved in 0.63 g propylene carbonate (PC). Both solutions are stirred until becoming homogeneous and filtered to obtain the CSPE. When the CSPE film is dried, a layer of PEDOT:PSS, acting as the top-gate electrode, is printed above the CSPE positioning vertically above the channel region.[20]

As our focus was on the characterization of reliable ring oscillator structures, we had chosen lithographically structured ITO films as passive structures in combination with an indium oxide precursor ink, annealed at high temperatures, to reduce process complexity and thus sources of variations. However, to be compatible with flexible electronics the passive structures should be printed with carbon or metallic inks and the channel material could be replaced with a nanoparticle ink requiring only room temperature for processing. This fully printed approach will indeed suffer from device performance reduction but it is still expected to be adequate for circuit design.

Our circuits are characterized with Agilent 4156C precision semiconductor parameter analyzer. The enable signal (V_{enable}) is controlled by Keithley 3390 arbitrary waveform generator and the oscillation is recorded with Yokogawa DL6104 digital oscilloscope. The ring oscillator is contacted through a SÜSS MicroTec probe station as indicated by the arrows in Fig. 2. The active and quiescence currents are measured at the supply voltage (V_{DD}) node of the ring oscillator. Since the output inverter is electrically isolated from the ring oscillator (separated supplies V_{DD} and V_{SS}), the supply voltage of the output inverter (V_{DDI}) is fixed at 2 V, to ensure that the output inverter is in saturation and the frequency is measured properly. All measurements were performed at 50 % humidity level and at room temperature (295 K).

In Fig. 3 the output characteristic as well as the gain of our inverter at a supply voltage of 1 V is shown. The maximum gain is 4.4 at an input voltage of 0.55 V, which is close to $V_{DD}/2$. The propagation delay time was measured to 2.3 ms.

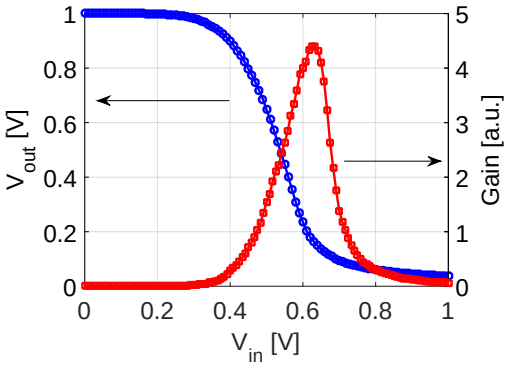
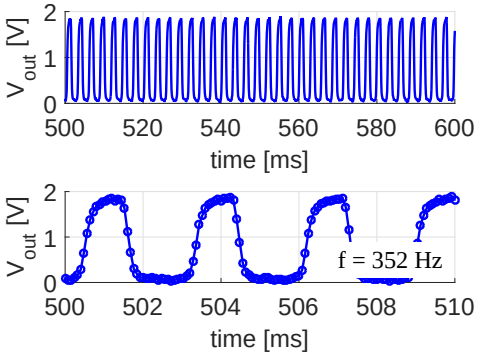
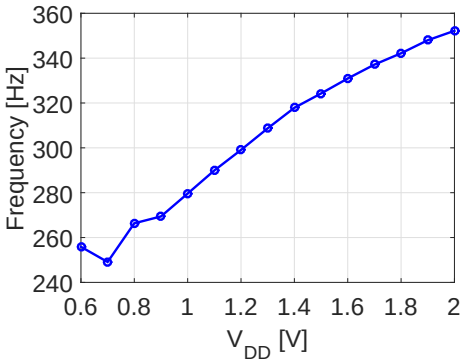


Figure 3. Output characteristics of an inverter with gain at a supply voltage of 1 V.

As can be seen from Fig. 4a, that the output signal of our ring oscillator has a swing from 0 to $\sim$ 1.9 V at 2 V supply voltage. The achieved frequency is 352 Hz as estimated with a Fast Fourier Transform (FFT) algorithm. The frequency rises linearly for lower supply voltages ($<$ 1.2 V) from 256 Hz at 0.6 V to 290 Hz at 1.1 V. Starting from 1.3 V supply voltage, the frequency starts to flatten (Fig. 4b). The reason for this supply voltage dependency is that at low voltages the switching capacitance rises (Fig. 5a) with the supply voltage but at the same time the driver capability of the ring oscillator also rises, compensating the effect of increasing switching capacitance and boosting the frequency. The driver ca-



(a)



(b)

Figure 4. (a) Output characteristics of an three-stage ring oscillator at a supply voltage V_{DD} of 2 V. (b) Dependency of the frequency f from the supply voltage V_{DD}.

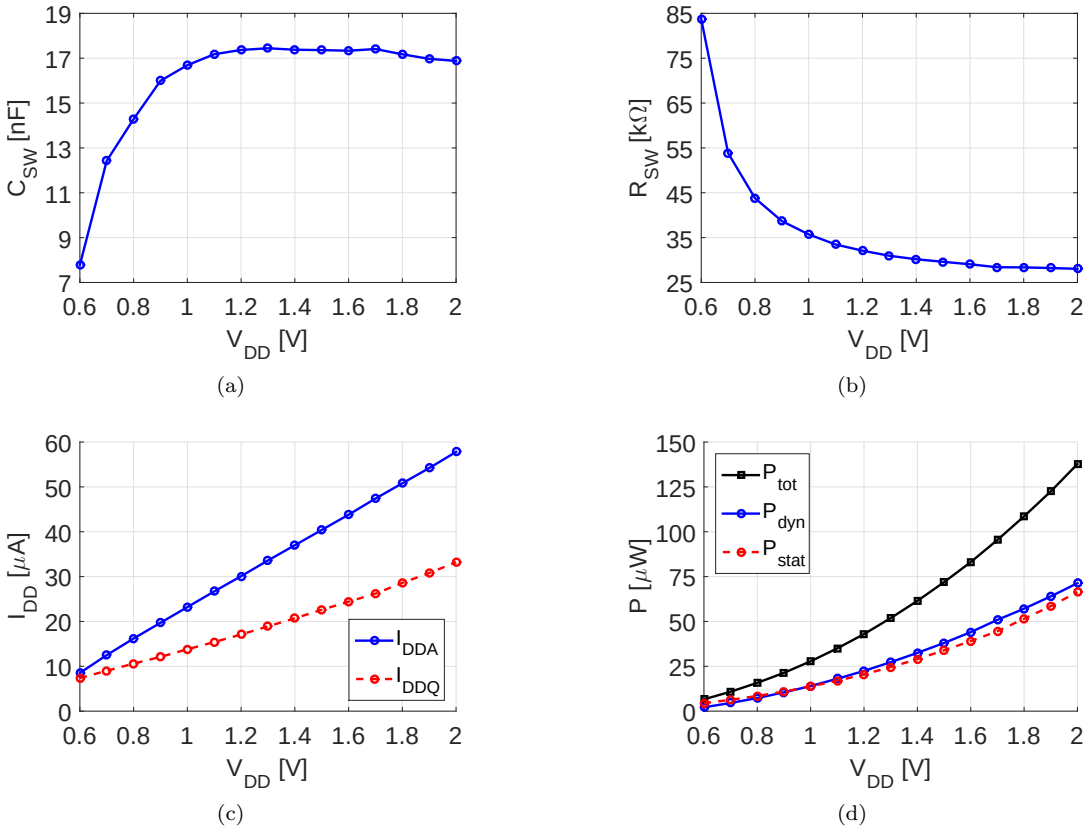


Figure 5. Dependendy of (a) the switching capacitance C_{SW}, (b) the switching resistance R_{SW}, (c) the current I_{DD} drawn by the ring oscillator and (d) the power consumption P from the supply voltage V_{DD}.

pability of ring oscillators can be estimated through the switching resistance (Fig. 5b).[26,27] At higher supply voltages ($>$ 1.3 V), all EGFETs are saturated and the driver capability of the ring oscillator is limited by the pull up resistors, leading the driver capability of the ring oscillator to saturate. Since the switching capacitance also starts to saturate at higher supply voltages, the slope of the frequency starts to flatten.

Ring oscillator structures can also become important to determine the minimum supply voltage at which circuits can operate within a given technology. In case of the present technology, we noticed that below 0.6 V the ring oscillator does not oscillate. Therefore, the minimum supply voltage for our technology lies at $\sim$ 0.6 V (Fig. 4b), which is extremely low value for a printed electronic circuit.

Next, a linear dependence of the active and quiescence currents with the supply voltage has been recorded (Fig. 5c). This linear dependence is obvious since we are using resistors for the pull up network in our designs. After measuring the active and quiescence currents, the power consumption can be estimated by using Equations (3) - (5). The total power rises from 6.6 μW to 137.7 μW at supply voltages of 0.6 V and 2 V respectively (Fig. 5d). Static and dynamic powers are in the same range because of the use of the resistor in the pull up network, causing a continuous and non-negligible leakage current.

In summary, we have prepared electrolyte-gated FETs based on indium oxide semiconductor as channel material. The high field-effect mobility, resulting from the indium oxide, in combination with the high gate capacitance of the electrolytic gate insulator allows us to operate printed circuits at very low supply voltages (0.6 V), which is comfortably within the range for IoT of wearable applications. The individual inverters have also shown reasonable gain of $\sim$ 4 at 1 V supply voltage. Three-stage ring oscillators based on this methodology demonstrate reasonable switching frequencies ($\sim$ 352 Hz at 2 V supply voltage). The power consumption climbed from $\sim$ 7 μW to $\sim$ 138 μW with respect to the supply voltage of 0.6 V and 2 V respectively.

We believe that this approach to fabricate, design and characterize the ring oscillator structures will facilate circuit design methodologies for low voltage, inkjet printed circuits, paving the way toward design and fabrication of low-cost, low-power in various emerging IoT, smart sensors and wearable applications.

This work was financially supported by the Helmholtz Gemeinschaft in the form of Helmholtz Virtual Institute under the grant number VI530.

[1] L. Feng, W. Tang, J. Zhao, R. Yang, W. Hu, Q. Li, R. Wang, and X. Guo, Scientific Reoports **6**, 1 (2016).

[2]J. S. Chang, A. F. Facchetti, and R. Reuss, IEEE Journal on Emerging and Selected Topics in Circuits and Systems **7**, 7 (2017).
[3]M. G. Mohammed and R. Kramer, Advanced Materials , 1604965 (2017).
[4]H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature Letter **445**, 745 (2007).
[5]T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, Nature Materials **9**, 1015 (2010).
[6]W. Xiong, Y. Guo, U. Zschieschang, H. Klauk, and B. Murmann, IEEE Journal of Solid-State Circuits **45**, 1380 (2010).
[7]I. Nausieda, K. K. Ryu, D. D. He, A. I. Akinwande, V. Bulovic, and C. G. Sodini, IEEE Transactions on Electron Devices **58**, 865 (2011).
[8]S. Abdinia, F. Torricelli, G. Maiellaro, R. Coppard, A. Daami, S. Jacob, L. Mariucci, G. Palmisano, E. Ragonese, F. Tramontana, A. van Roermund, and E. Cantatore, Organic Electronics **15**, 904 (2014).
[9]L. Feng, W. Tang, J. Zhao, Q. Cui, C. Jiang, and X. Guo, IEEE Transactions on Electron Devices **61**, 1175 (2014).
[10]H. Fuketa, K. Yoshioka, Y. Shinozuka, K. Ishida, T. Yokota, N. Matsuhisa, Y. Inoue, M. Sekino, T. Sekitani, M. Takamiya, T. Someya, and T. Sakurai, IEEE Transactions on Biomedical Circuits and Systems **8**, 824 (2014).
[11]H. Sirringhaus, Advanced Materials **26**, 1319 (2014).
[12]K. Hong, Y. H. Kim, S. H. Kim, W. Xie, W. D. Xu, C. H. Kim, and C. D. Frisbie, Advanced Materials **26**, 7032 (2014).
[13]W. Clemens, W. Fix, J. Ficker, A. Knobloch, and A. Ullmann, Journal of Materials Research **19**, 19631973 (2004).
[14]D. Zielke, A. C. Hbler, U. Hahn, N. Brandt, M. Bartzsch, U. Fgmann, T. Fischer, J. Veres, and S. Ogier, Applied Physics Letters **87**, 123508 (2005).
[15]A. Huebler, F. Doetz, H. Kempa, H. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, and U. Hahn, Organic Electronics **8**, 480 (2007).
[16]Y. Xia, W. Zhang, M. Ha, J. H. Cho, M. J. Renn, C. H. Kim, and C. D. Frisbie, Advanced Functional Materials **20**, 587 (2010).
[17]P. K. Nayak, M. N. Hedhili, D. Cha, and H. N. Alshareef, Applied Physics Letters **103**, 033518 (2013).
[18]S. Garlapati, N. Mishra, S. Dehm, R. Hahn, R. Kruk, H. Hahn, and S. Dasgupta, Applied Materials & Interfaces **5(22)**, 11498 (2013).
[19]S. H. Kim, K. Hong, W. Xie, K. H. Lee, S. Zhang, T. P. Lodge, and C. D. Frisbie, Advanced Materials **25**, 1822 (2013).
[20]G. C. Marques, S. K. Garlapati, D. Chatterjee, S. Dehm, S. Dasgupta, J. Aghassi, and M. B. Tahoori, IEEE Transactions on Electron Devices **64**, 279 (2017).
[21]W. Xie, X. Zhang, C. Leighton, and C. D. Frisbie, Advanced Electronic Materials **3**, 1 (2017).
[22]B. Nasr, D. Wang, R. Kruk, H. Roesner, H. Hahn, and S. Dasgupta, Advanced Functional Materials **23**, 1750 (2013).
[23]Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. (Cambridge University Press, New York, NY, USA, 2009).
[24]T. T. Baby, S. K. Garlapati, S. Dehm, M. Häming, R. Kruk, H. Hahn, and S. Dasgupta, ACS Nano **11(29)**, 3591 (2015).
[25]S. K. Garlapati, T. T. Baby, S. Dehm, M. Hammad, V. S. K. Chakravadhanula, R. Kruk, H. Hahn, and S. Dasgupta, Small **11**, 3591 (2015).
[26]M. Bhushan and M. B. Ketchen, *Microelectronic Test Structures for CMOS Technology*, 1st ed. (Springer-Verlag New York, New York, NY, USA, 2011).
[27]M. Bhushan and M. B. Ketchen, *CMOS Test and Evaluation*, 1st ed. (Springer-Verlag New York, New York, NY, USA, 2015).