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Integrated Design of Motor Drives using Random Heuristic Optimization for Aerospace Applications

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Abstract

High power density for aerospace motor drives is a key factor in the successful realization of the More Electric Aircraft (MEA) concept. An integrated system design approach offers optimization opportunities, which could lead to further improvements in power density. However this requires multi-disciplinary modelling and the handling of a complex optimization problem that is discrete and non-linear in nature. This paper proposes a multi-level approach towards applying random heuristic optimization to the integrated motor design problem. Integrated optimizations are performed independently and sequentially at different levels assigned according to the 4-level modelling paradigm for electric systems. This paper also details a motor drive sizing procedure, which poses as the optimization problem to solve here. Finally, results comparing the proposed multi-level approach with a more traditional single-level approach is presented for a 2.5 kW actuator motor drive design. The multi-level approach is found to be more computationally efficient than its counterpart.

Introduction

The More Electric Aircraft (MEA) concept offers exciting benefits in improving fuel efficiency, reducing operating and maintenance costs, and cutting down carbon emissions, making future air-travel cheaper and cleaner. By replacing traditional hydraulic, mechanical and pneumatic powered systems, such as fuel pumping, wing ice protection, Environmental Control System (ECS) and actuations, with electrical systems, improved flexibility, weight reduction and fuel efficiency gains are possible [1].

In modern, highly electrified aircraft, instead of bleeding air from the engine for use in the Environmental Control System (ECS), compressors powered by electricity are used to regulate cabin temperature and pressure. This improves fuel efficiency of the main engines. Also, the replacement of traditional hydraulic circuits with Electrical Hydro-static Actuators (EHAs) has provided advantages in terms of weight, volume and reliability. Taking a step further into the future of commercial aviation, EHAs can be replaced with Electro-Mechanical Actuators (EMAs), in order to eliminate the hydraulic fluids adoption. This is particular attractive for aircraft operators from a cost and maintenance point of view. However, EMA technologies are currently only limited to Secondary Flight Controls or military applications due to potential ball-screw jamming issue. In order to widespread EMA technologies, this issue needs to be addressed using appropriate technology [2].

With increasing electrification, an increasing number of power electronics converters and electrical machines are needed onboard. Their power density and efficiency remain a key challenge to be overcome in order to fully benefit from the MEA concept.

Recent developments in wide-bandgap semiconductor technology has brought a step change in the field of power electronics research. New switching devices, such as silicon carbide MOSFETs, offer the prospect of power converters which are power dense, highly efficient and are able to operate at high temperatures [3]. For filter inductors, Nano-crystalline and iron powder materials are increasingly popular over ferrites as they offer higher saturation flux density, lower hysteresis losses and lower DC bias effects [4]. For electro-mechanical power conversion in a typical EMA application, Permanent Magnet Synchronous Machines (PMSM) are often favored due to their high torque density, excellent efficiency and good power factor. By utilizing different slot-pole combinations (in particular non-overlapping fractional slot topologies) and advanced thermal management techniques, power density limits for electrical machines are also constantly expanding [5].

To assess the impact of recent advancements at a subsystems level on the overall motor drive weight, the interactions between components and the influence of design variables has to be well understood. For example, reducing weight of passive filters by increasing the converter switching frequency can increase losses in other parts of the circuit, requiring additional cooling capacity. As a result, this can lead to increased total weight.

Therefore, integrated approach to the motor drive design with an appropriate optimization method is required to reach a ‘true’ optimal weight. Posing the motor drive design as an optimization problem, several approaches can be taken to solve it. A deterministic approach was adopted in [6] for the optimization of an aerospace motor drive, employing a Pareto-front chart of the desired objectives, formulated by sweeping through design variables. Statistical approaches with evolutionary algorithms like Genetic Algorithms (GA) or Particle Swarm Optimization (PSO) for electrical system designs have also been proposed [7]. In [8], an integrated weight optimization for a helicopter swashplate actuation system, consisting of fault-tolerant electrical machines and power converters, was performed using PSO.

Further, considering the computational cost with the multitude of design variables involved in these statistical approaches, systematic and multi-level methods have been proposed over the recent years to tackle these optimizations more efficiently. [9] [10].

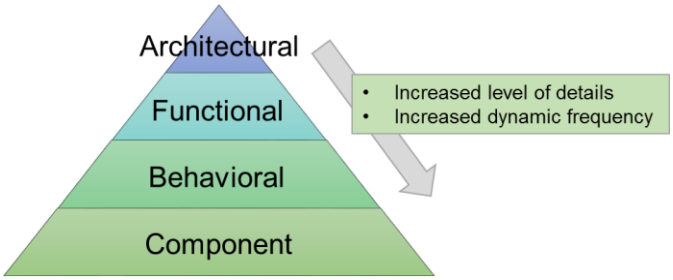

Figure 1: 4-level Modelling Paradigm

To systematically model a motor drive, a 4-level modelling paradigm has been proposed [2]. The paradigm can be seen in Figure 1. Within this paradigm, each lower level successively represents higher modelling details and dynamic frequency. The component level represents the system behavior for Electro-Magnetic Interference (EMI) frequencies above 100 kHz. The behavioral level represents the system behavior for frequencies between 10 kHz and 100 kHz, considering switching harmonics in the converter waveforms. The functional level represents system behavior for frequencies between 10 Hz to 10 kHz. The fundamental harmonics of the AC power transfer typically falls within this range. Finally, the architectural level represents system behavior for frequencies below 10 Hz. The load cyclic frequency usually fall within this range. This modelling paradigm formulates the basis of the approach proposed in this paper to perform multi-level integrated optimizations.

The pre-requisite for successful optimizations is a well-defined problem. For practical weight optimization of a motor drive, this can only be achieved by first having accurate sizing models. Therefore this paper also presents the sizing models developed for a motor drive.

The paper is organized as follows: Section II presents the system topology considered; Section III presents the multi-level approach and the sizing models developed; Section IV shows results comparing the proposed multi-level approach against the traditional single-level approach for random heuristic optimizations.

System Topology

The considered application is in driving an electro-mechanical linear actuator rated up to 2.5 kW. The load profile considered is cyclic, moving a load linearly from point A to B and back to A within a time period with a specified acceleration and peak velocity.

The selected motor drive topology consists of an electrical machine controlled by a two-level Voltage-Sourced Back-to-Back Converter (VSBBC) interfaced with the AC grid via input filters.

The electrical machine considered is a 12-slot, 10-pole surface mounted Permanent Magnet Synchronous Machine (PMSM) which adopts fractional slot double-layer, non-overlapped, concentrated winding. This slot/pole combination provides the advantage of increased fault tolerance as the phases are physically isolated from each other and have inherently high self-inductances fault current limitations in the event of winding short-circuits [11].

A single-stage L filter is employed at the grid side providing 1st order low pass attenuation to meet power quality requirements. Grid-side EMI filters are considered to be designed separately from the motor drive and are hence excluded from the motor drive design procedure. Assuming short cables between the power converter and electrical machine, the machine-side EMI filters are also excluded in this work.

For good heat dissipation and compactness, two six-pack IGBT-Diode power modules, mounted onto the same heat-sink, are considered for the VSBBC implementation. The semiconductor cooling method selected is forced-air convection, consisting of an aluminum heat-sink with extruded plate fins and a constant speed commercial fan. The motor drive is assumed to be physically located within the aircraft, where it is not exposed to extreme environmental conditions.

The current aerospace electrical standards require braking circuits at the DC-link to prevent any regenerative power from being fed back into the grid. However, [12] shows that the impact of average energy regenerated from an actuator on the grid is low. Hence, no braking circuits are considered here.

An overview of the motor drive architecture can be seen in Figure 2.

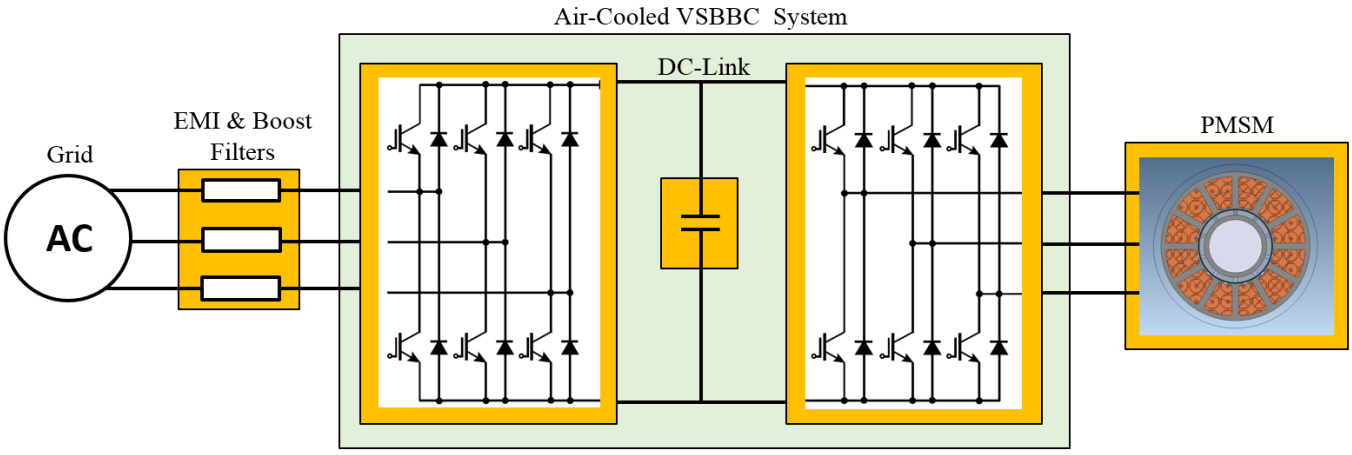

Figure 2: Overview of motor drive architecture considered

Multi-level Optimization

Genetic Algorithm (GA)

Due to both the complexity and non-linear nature of the optimization problem, random heuristic methods are chosen over classical optimization algorithms. Specifically, GA is selected to better handle non-linear constraints.

The only constraint handling method applied in this work is the 'death penalty' method, where infeasible design points are 'sentenced' with maximum fitness. Compared to other constraint handling methods, this is most computationally efficient and easy to implement as no further calculations are necessary to estimate the violations after infeasible design points are rejected. However, it is limited to problems where feasible area constitutes a large portion of the entire search space. This is because it does not exploit information from infeasible design points to guide its search. [13, 14].

The software implementation of the algorithm is done through the MATLAB global optimization toolbox because of its incorporated parallel processing capability.

Single-level vs. Multi-level Optimization

The traditional single-level approach of optimizing all design variables at once in one large design space is computationally expensive. In contrast, a multi-level framework divides the large design space into several subspaces. This was proposed in [10] and was termed as the Sequential Subspace Optimization Method (SSOM). Subspaces are first formed based on a 'significance factor'. Then optimizations are performed in the subspaces sequentially, where optimized values from one level form the baseline parameters for the next level. The process is carried out iteratively (as seen in Figure 3) until a termination criteria is met. The multi-level framework was shown to be more computationally efficient compared to the single-level framework.

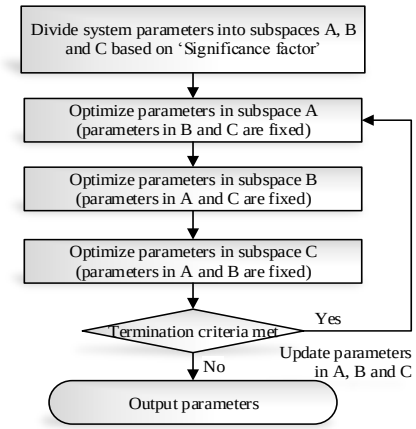

Figure 3: Sequential Subspace Optimization Method (SSOM)

Multi-level Problem Formulation

The integrated motor-drive design is formulated into a multi-level optimization problem based on the 4-level modelling paradigm. Firstly, the relationship between model outputs and design variables are identified. Next, model outputs along with their associated design variables are assigned to levels/subspaces based on dynamic frequencies.

An example is presented below, where design variables considered are machine diameter, machine flux density limits, machine length-diameter ratio, machine slot dimensions (stator opening and tooth-tip height), converter switching frequency and converter DC-link voltage.

A. Architectural level (Below 10 Hz)

Model outputs that have low dynamic frequency like machine continuous torque and peak machine torque are assigned to this level. For a surface mounted PMSM, the machine continuous torque capability is current limited and dependent on volume of permanent magnet (PM) and q-axis currents. On the other hand, for a given speed and voltage, the machine peak torque capability is voltage limited and dependent on machine synchronous inductance. The associated design variables are machine diameter, flux density limits and length-diameter ratio, which affects the PM volume and machine synchronous inductance.

B. Functional level (Between 10 Hz and 10 kHz)

Model outputs like machine torque ripple, winding losses, hysteresis losses and semiconductor device conduction losses are assigned to this level. At steady-state, torque ripple is closely linked with the machine winding/slot configuration, whereas the mentioned losses are linked with the fundamental frequency of AC power transfer. The associated design variables are machine flux density limits, stator slot dimensions and converter DC-link voltage.

C. Behavioral level (Between 10 kHz and 100 kHz)

Model outputs like current switching ripple, machine eddy current losses, inductor eddy current losses and semiconductor device switching losses are assigned to this level. At steady-state, these model outputs are a function of the voltage waveforms coming out of the power converter. The associated design variables are converter DC-link voltage and switching frequency.

D. Component level (Above 100 kHz)

Model outputs representing EMI behavior are assigned to this level. However, as EMI filters are considered to be designed separately from the motor drive, this level is excluded from this example.

The relationships above are summarized in Figure 5.

Motor Drive Optimization Problem

The motor drive sizing procedure is seen in Figure 4. In the optimization, this procedure takes in design variables and system constraints and outputs total weight as objective function.

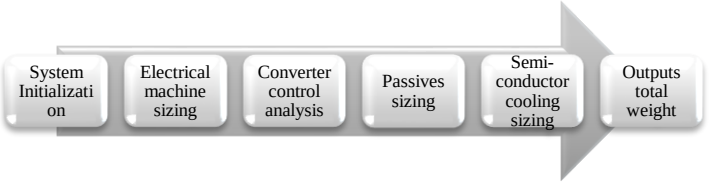

Figure 4: Sizing procedure of the main objective function

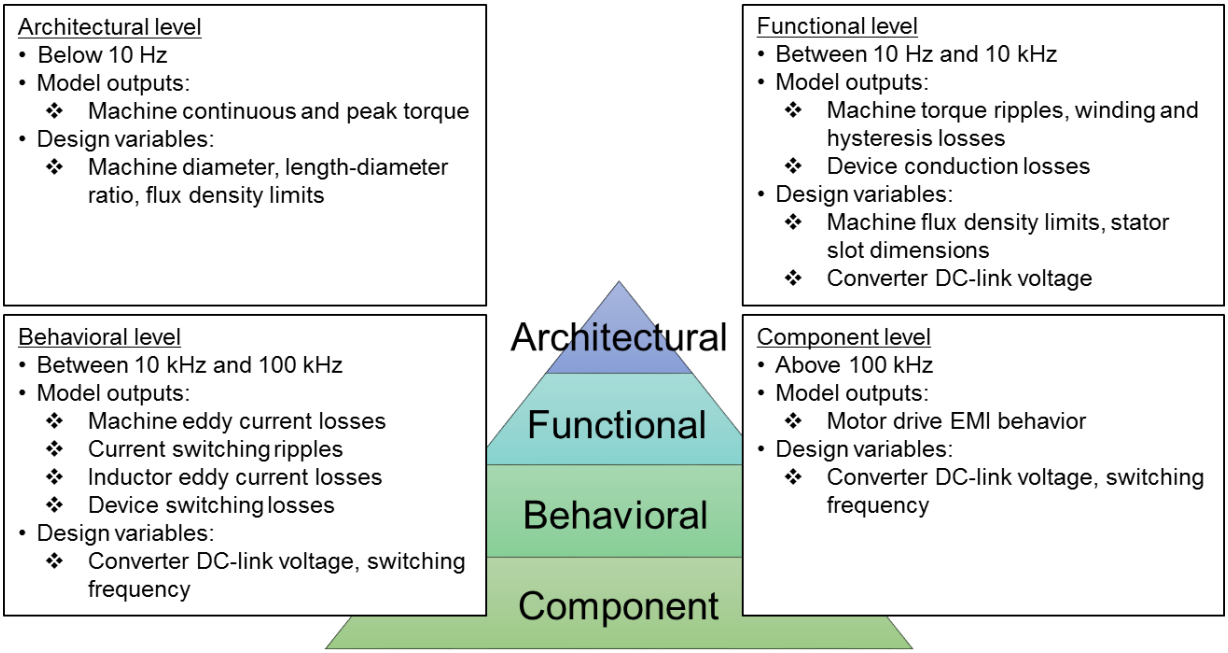

Figure 5: Design variables grouped based on 4-level paradigm

Electrical Machine Sizing

The machine slot-pole combination chosen is 12-slot 10-pole (Figure 6) as result of previous trade-off studies. It is dimensioned analytically based on Maxwell fundamental electro-magnetic equations and the principle of energy conservation [15].

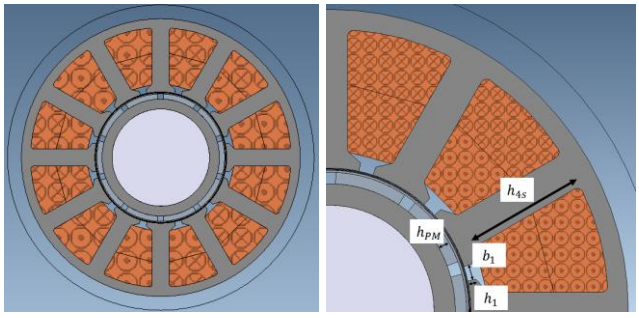

Figure 6: 12-slot 10-pole Machine in Use

Most PMSM optimizations from previous work [9] [10] employ the permanent magnet height h_{PM}, stator tooth height h_{4s} and number of stator winding turns $N_{turn,s}$ as design variables. However, in the sizing method employed, these parameters are determined internally through embedded iteration loops.

The first iteration loop is required to consider variations in air-gap leakage flux, expressed as effective PM width α_{PM}, when h_{PM} is varied. The second iteration loop is required to consider variations in losses and inductances L_d, which affects stator current I_{ph}, when machine geometry is varied. The machine design procedure exits when constraints or limits are violated to avoid un-converging iterations.

An overview of the design procedure can be seen from Figure 7. The machine weight is given as output.

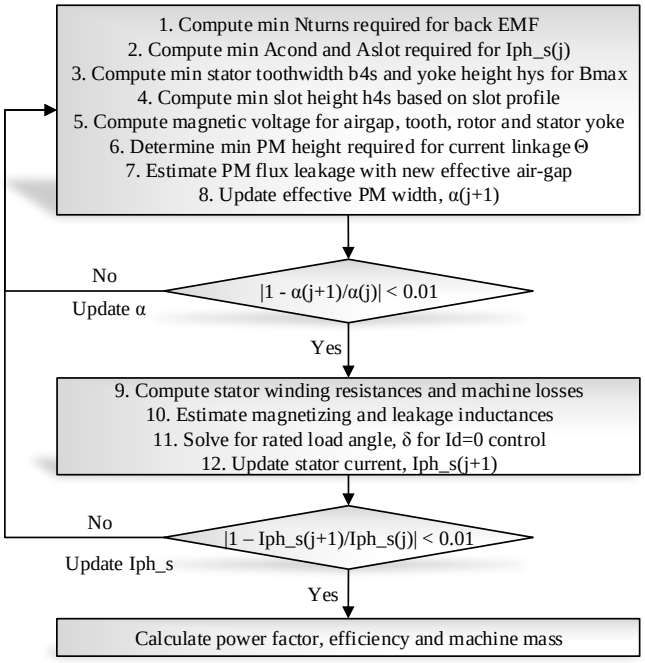

Figure 7: PMSM design procedure

However, the machine sizing function implemented can be further improved in two aspects, which are currently not included in the scope of work:

A) By implementing a thermal model to consider power losses and heat dissipation from the machine windings [16]
B) By implementing a robust and computationally efficient Dynamic Magnetic Reluctance Network (DMRN) to consider local saturations within the stator of the machine.

The resulting machine geometry from the sizing method is evaluated using Finite Element (FE) software and its output performance is checked against load requirements.

Control and Steady State Analysis

Motor Drive Control

For the VSBBC control, rotating frame vector control is employed. To obtain the frame transformation angle, the Network Side Converter (NSC) uses a Phase-Locked Loop (PLL) and the Machine Side Converter (MSC) employs a speed sensor at the machine. The NSC is controlled to impose a desired DC-link voltage while ensuring Power Factor Correction (PFC) at the grid side connection. On the other hand, the MSC is controlled to obtain desired machine speed under different load conditions.

The current control loop bandwidth has to be adequately smaller, for example, 10 times smaller, than switching frequency to ensure controllability. This forms a lower constraint for the switching frequency design variable in the optimization.

Passives Design

The required grid side boost inductance L_B and DC-link capacitance C_{DC} have be determined. Sufficient boost inductance is chosen to ensure that the input current ripple harmonics meet the power quality requirements from the grid. On the other hand, DC-link capacitance is chosen to provide attenuation of DC-link voltage transients due to sudden and externally triggered load changes.

The current ripple limits are defined up to the 40th harmonic in the power quality standard of DO-160E. Hence for a grid frequency of 400 Hz, only current ripple up to 16 kHz are considered.

The grid side power quality requirement is initially expressed as a maximum peak-to-peak current ripple ΔI_{PP} at the converter switching frequency f_{sw}. The required inductance is determined using (1).

$$L_B = \frac{V_{max}}{f_{sw}\Delta I_{PP}} \tag{1}$$

with $V_{\max}$ being the maximum voltage drop across the boost inductor.

With L_B, a fundamental period of the time-domain input switching current waveform is computed. A Fast Fourier Transform (FFT) and Total Harmonic Distortion (THD) analysis is performed on the waveform and checked against the DO-160E limits. The design procedure is halted if the limits are exceeded.

In order to determine the required DC link capacitance, the energy storage criterion is adopted. In an externally triggered event where rated output load is suddenly removed, input currents flowing through the boost inductors are immediately controlled to zero by the NSC current controller. During this process, the DC-link capacitor acts as an energy storage to absorb the transient energy and limit the voltage overshoot. The required capacitance for this operation can be determined using (2).

$$C_{DC} = \frac{t_{iCL(NSC)}}{V_{dc}V_{\text{overshoot}}}\left[\frac{3L_B}{4}\left(\frac{I_{ph}^2}{t_{iCL(NSC)}}\right)+\frac{P_{load}}{\eta_{MSC}}\right] \tag{2}$$

with current closed loop time constant $t_{iCL(NSC)}$, maximum voltage overshoot $V_{\text{overshoot}}$, rated output load power P_{load} and MSC rated efficiency η_{MSC}.

Resulting control and passive component values are evaluated in time-domain electrical simulations of a back-to-back converter using PLECS. Input current THD and DC-link voltage overshoot are then checked against requirements.

Steady-State Analysis

Assuming a 60 degrees discontinuous PWM modulation (DPWM1) with a minimum losses algorithm, the average and RMS currents through the IGBT and diodes is mathematically derived for the converters. This is done using turn-on times and averaging conduction current over individual sectors of the space vector hexagon [17]. For a fixed converter modulation index M and power factor angle ϕ, the NSC current values are calculated using (3) - (6)

$$I_{IGBT,ave} = 6 - \frac{\sqrt{3}\pi M_{pk}\cos\phi}{12\pi} I_{pk} \tag{3}$$

$$I_{Diode,ave} = 6 + \frac{\sqrt{3}\pi M_{pk}\cos\phi}{12\pi} I_{pk} \tag{4}$$

$$I_{IGBT,rms}^2 = \frac{2\pi - \sqrt{3}\left(3 + 4M_{pk}\cos\phi\right)}{24\pi} I_{pk}^2 \tag{5}$$

$$I_{Diode,rms}^2 = \frac{4\pi + \sqrt{3}\left(3 + 4M_{pk}\cos\phi\right)}{24\pi} I_{pk}^2 \tag{6}$$

Likewise for the MSC, their values are calculated using (7) - (10)

$$I_{IGBT,ave} = 6 + \frac{\sqrt{3}\pi M_{pk}\cos\phi}{12\pi} I_{pk} \tag{7}$$

$$I_{Diode,ave} = 6 - \frac{\sqrt{3}\pi M_{pk}\cos\phi}{12\pi} I_{pk} \tag{8}$$

$$I_{IGBT,rms}^2 = \frac{2\pi + \sqrt{3}\left(3 + 4M_{pk}\cos\phi\right)}{24\pi} I_{pk}^2 \tag{9}$$

$$I_{Diode,rms}^2 = \frac{4\pi - \sqrt{3}\left(3 + 4M_{pk}\cos\phi\right)}{24\pi} I_{pk}^2 \tag{10}$$

Worst-case steady-state RMS current ripple going through the DC-link capacitor is calculated using (11) and (12) [18].

$$I_{C(\text{MaxRMS})} = I_{C(NSC,RMS)} + I_{C(MSC,RMS)} \tag{11}$$

$$I_{C(RMS)} = \frac{\hat{I}_{ph}}{\sqrt{2}}\sqrt{\left[2M\left\{\frac{\sqrt{3}}{4\pi} + \cos^2\phi\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right\}\right]} \tag{12}$$

Weight Estimation for Boost Inductors

Toroidal powder cores with magnetic material Molypermalloy MPP60 from core manufacturer Magnetics Inc. are considered because of their excellent AC and DC magnetization properties. Additionally, only single-layer windings are considered to minimize parasitic winding capacitance. Wire-spacing ratio $\alpha_{spacing}$ is set to 1 and desired ratio of permeability drop $\gamma_{desired}$ at rated current compared to zero current is chosen as 0.8.

The physical size of the boost inductor is primarily a function of peak input current I_{pk} and L_B. To find the smallest inductor core, an iterative algorithm is employed to sweep through a library of discrete cores. This local library is created using data from core manufacturer Magnetics Inc. and contains information of the different available core dimensions and their inductance factors.

The maximum number of turns $N_{\max}$ for an inner diameter ID of a core, constrained by the inner window area is calculated using (13).

$$N_{max} = \frac{\pi\left(ID - (d_{wire} + 2h_{ins})\right)}{(1 + \alpha_{spacing})(d_{wire} + 2h_{ins})} \tag{13}$$

with diameter of wire d_{wire} and height of wire insulations h_{ins}. Next, the minimum core cross-sectional area $A_{core(min)}$ is calculated using (14).

$$A_{Core,min} = \frac{I_{pk} L_B}{\mu_0 \mu_R \gamma_{desired} H_{max} N_{max}} \tag{14}$$

with maximum magnetic field strength H_{max} taken from the material datasheets. This represents the first criterion and cores which do not meet the minimum cross-sectional area value are rejected.

The minimum number of turns $N_{\min}$ to obtain the desired inductance at zero current L_0 is calculated with (15).

$$N_{min} = \sqrt{\frac{L_0}{AL_0}} \tag{15}$$

with manufacturer-given nominal inductance factors AL_0 for the each specific core. If $N_{\min}$ is larger than $N_{\max}$, this indicates that the chosen core is physically unable to accommodate the required number of turns with its window area and is hence eliminated from selection. This forms the second criterion.

The rated magnetic field strength H, flux density B and the ratio of permeability drop γ_{actual} at rated operating point is calculated using manufacturer material data. If γ_{actual} is smaller than $\gamma_{desired}$, the core is also eliminated from selection. This forms the third criterion.

Lastly, total power losses and temperature rise T_{rise} is estimated using a simplified thermal model given the unwounded core surface area, mean length per turn MLT and wire resistivity. If temperature rise exceeds a chosen value, the core is eliminated from selection. This forms the final criterion.

By sweeping through the library in order of increasing core volume, the first core able to meet all four criteria is selected and its final weight is given as output. An overview of this process is seen in Figure 8.

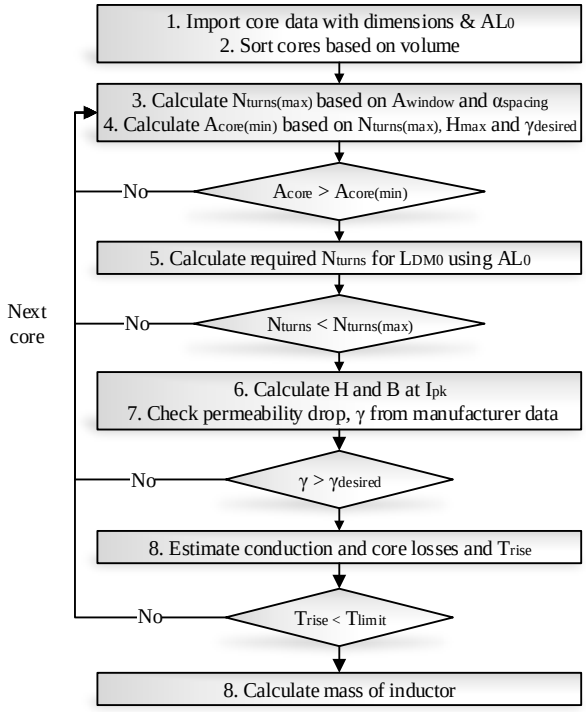

Figure 8: Differential Mode (DM) Inductor Physical Sizing Algorithm

A three-dimensional plot showing relationship between inductor weight, inductance and rated current is obtained with the above method (as seen in Figure 9).

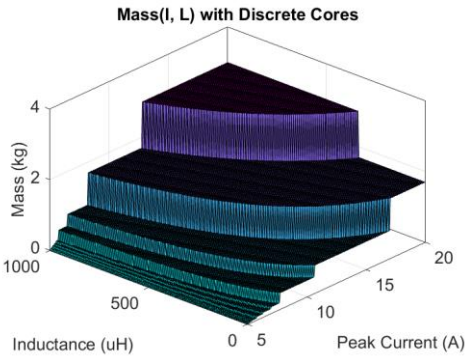

Figure 9: Mass vs Inductance for Single-layer Toroidal Inductors using Molypermalloy MPP60 material (Magnetics)

Weight Estimation for DC-Link Capacitor

Film capacitors are considered for the DC-link capacitors. In comparison to their electrolytic counterparts, they have better current ripples tolerance and hence a longer operational lifetime.

The physical size of a film capacitor is primarily a function of worst case RMS currents and C_{dc}. Data for the MKP DC-link of B2562x series film capacitors are imported from manufacturer EPCOS to create a local library. The 900V rated variants are selected here for the motor drive sizing.

The relationship between volume, capacitance and maximum current ripple is obtained (as seen in Figure 10). These relationships are linearized in (16) and (17) to size capacitors of 100 - 1500µF.

$$Vol_{Cap} = 1.11 \cdot 10^{-6} \frac{\mathrm{m}^3}{\mu\mathrm{F}} \cdot C_{Rated} + 1.57 \cdot 10^{-4}\mathrm{m}^3 \qquad (16)$$

$$I_{C,maxRMS} = 0.04 \frac{\mathrm{A}}{\mu\mathrm{F}} \cdot C_{Rated} + 38.25\mathrm{A} \qquad (17)$$

With capacitor volume and an average weight density of EPCOS film capacitors of $1.08 \cdot 10^3$ kg/m^3, the final weight of the capacitor can be estimated.

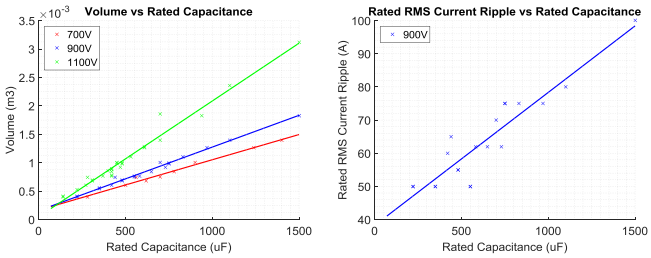

Figure 10: Relationship between Capacitance vs Volume (Left); Capacitance vs Max RMS Current Ripple (Right)

Weight Estimation for Semiconductor Cooling System

Two six-pack IGBT-Diode power modules are placed on a common heat-sink for forced-convection cooling. The arrangement can be seen in Figure 11.

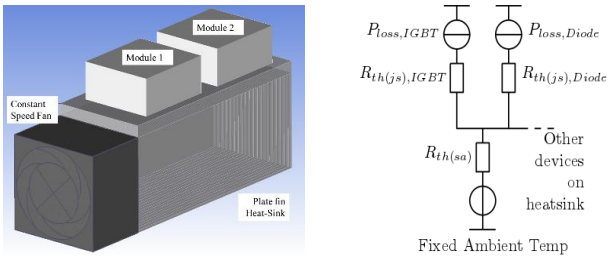

Figure 11: Cooling System Considered (Left); Simplified Thermal Resistance Network employed (Right)

Semiconductor Losses Evaluation

The total power losses as a function of device junction temperature is estimated using (18) and (19). An iteration loop is employed for the devices to arrive at their steady-state junction temperature value.

$$P_{cond}(T_j) = U_{forward}(T_j) * I_{ave} + R_{forward}(T_j) * I_{rms}^2 \qquad (18)$$

$$P_{sw}(T_j) = f_{sw} * E_{total}(T_j) \qquad (19)$$

Semiconductor Area Based Heat-Sink Sizing

In a traditional converter design, the semi-conductor power module is first selected and a heat-sink is subsequently optimized to provide it with cooling. However, this approach has its shortcomings because if baseplate-to-heat-sink surface area is fixed, very little room for the heat-sink weight optimization is left even when semi-conductor losses are reduced.

This is true especially for forced-air convection cooling, where cooling performance is mainly dependent on air-flow velocity and pressure drop. Given a fan performance curve and heat-sink surface area, optimal heat-sink fin count and fin thickness values can be found for minimum heat-sink thermal resistance $R_{th(sa)}$[19]. Thus attempts to reduce heat-sink weight by varying fin count and thickness can negatively impact cooling performance.

When semiconductor losses are generated, heat flows through multiple layers like the substrate and baseplate to arrive at the heat-sink for dissipation. Using a simplified Cauer thermal network, the thermal resistances are grouped into two parts: junction-to-case thermal resistance $R_{th(js)}$ and case-to-ambient thermal resistance $R_{th(sa)}$ (as seen in Figure 11). Both of these thermal resistances are a function of semi-conductor chip area A_{chip} and surface area at the module baseplate-to-heatsink junction $A_{moduleBP}$.

To better link semi-conductor losses with its heat-sink weight, a non-conventional approach is used. It is based on the Semiconductor Area Comparison (SAC) method proposed in [17]. This non-conventional approach aims to first find the minimum A_{chip} and subsequently $A_{moduleBP}$ to keep the device junction temperature within limits. With $A_{moduleBP}$ the heat-sink is then sized to provide minimum thermal resistance.

As power losses are increased, in order to keep the device junction temperature within limits, $R_{th(js)}$and $R_{th(sa)}$ have to decrease. This is achieved by increasing A_{chip} and $A_{moduleBP}$. This is however done at the expense of an increased total weight due to the increased heat-sink baseplate size.

When A_{chip} is varied, the corresponding chip conduction losses P_{cond}, switching losses P_{sw} and junction-case thermal resistance $R_{th(js)}$ are will inherently change. Empirical relationships derived in [17] are employed to quantify the relationship between A_{chip} and corresponding chip P_{cond}, P_{sw} and $R_{th(js)}$.

To quantify the relationship between A_{chip} and $A_{moduleBP}$, a statistical analysis is performed using commercially available semi-conductor/packaging manufacturers data.

Firstly, rated current vs. bare-die area relationship for 1200V IGBT4-T4, EM4 Diode and CAL4 Diode bare dies is plotted and linearized as seen from Figure 12. The IGBT4 (T4) current-chip area density value is estimated to be 1.07A/mm^2. On the other hand, for the EM4 Diode and CAL4 Diode, their current-chip-area density values are estimated to be 2.12 A/mm^2 and 1.84A/mm^2 respectively.

Secondly, rated current vs. smallest power module base-plate area relationship, for 1200V IGBT4-T4 six-pack IGBT-Diode power modules, is plotted and linearized as seen from Figure 12. This gives an estimated current-module-baseplate-area density of 0.0257 A/mm^2

for a manufacturer that employs EM4 Diodes and 0.0282 A/mm^2 for another manufacturer that employs CAL4 Diodes.

Using rated current values and considering 6 pairs of IGBT-diodes per module, simplified expressions (20) and (21) can be derived, linking total chip area $A_{Chip(Total)}$ to module baseplate area.

$$A_{Module(Infineon)} = 4.63\ A_{Chip(Total)} + 361.75\ \text{mm}^2 \quad (20)$$

$$A_{Module(Semikron)} = 4.00\ A_{Chip(Total)} + 603.80\ \text{mm}^2 \quad (21)$$

The limitation of this proposed approach is in its simplified relationship. When considering packaging parasitics, chip separations and chip placements within a power module, $A_{ModuleBP}$ is actually not purely a function of $A_{chip(Total)}$.

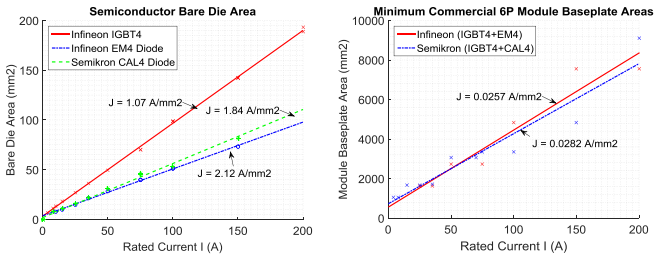

Figure 12: Linearized Relationship between Commercial Semiconductor Bare Die Area (Left) and 6-Pack Modules Base-plate Areas (Right)

To begin the heat-sink sizing algorithm, an initial minimum A_{chip} is set based on a minimum current-chip area density value. Given A_{chip} value, the corresponding chip P_{cond}, P_{sw} and $R_{th(js)}$ and $A_{ModuleBP}$ can be empirically found as described above.

The power module length-width ratio K_{lw} is fixed at 2:1 and a minimum clearance γ_{cl} at each side is fixed at 1cm. Hence, with $A_{ModuleBP}$, the heat-sink surface area $A_{HSSurface}$ and width-length dimensions can be sized.

Employing equations from [19] and using a fixed fan's performance curve, the optimal heat-sink fin count and fin thickness to give a minimum thermal resistance value $R_{th(sa)}$ can be found using the MATLAB FMINCON function.

Lastly, with $R_{th(js)}$ and $R_{th(sa)}$ for a given $A_{chip(total)}$, the power losses and device junction temperature can be estimated. The steady-state device junction temperature values are derived using an iteration loop. If the junction temperature limits are exceeded, $A_{chip(total)}$ is increased and the procedure is started over again.

A summary of the proposed algorithm can be seen in Figure 13.

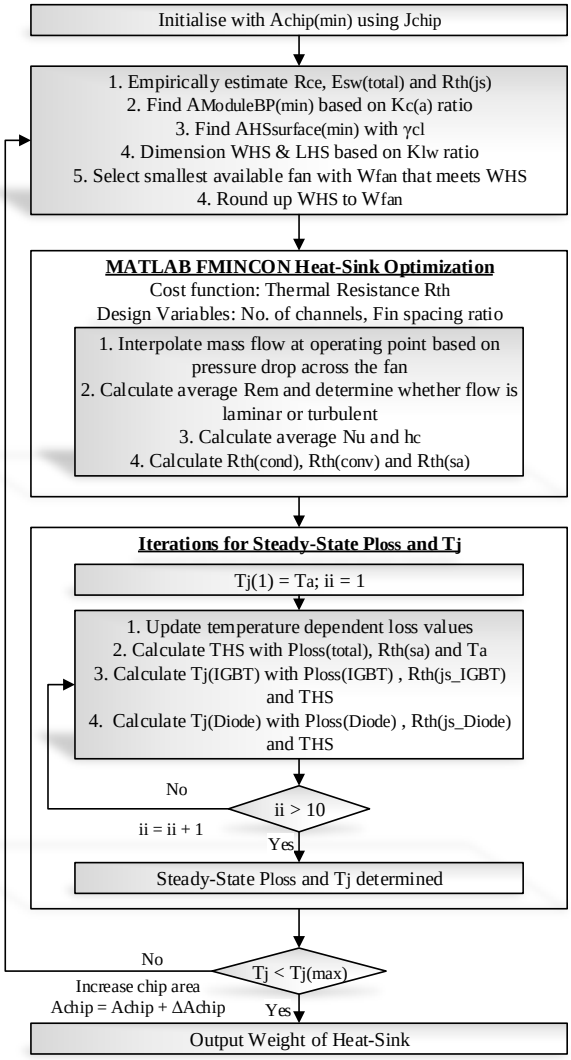

Figure 13: Proposed Semiconductor Area Heat-sink Sizing Algorithm

Resulting heat-sink dimensions are validated with simple thermal 3D Finite Element Analysis using ANSYS IcePak.

Results & Discussion

A multi-level optimization is performed using the proposed method for a 2.5 kW actuator motor drive and it is compared against a single-level approach of applying random heuristic optimizations. GA is applied with 90 generations for the multi-level approach and 30 generations for the single-level approach. The used platform consists of a standard desktop PC equipped with an Intel Core i7-920 @ 2.67 GHz processor and 11GB of RAM."

For single-level optimization, the 7 design variables mentioned in the above sections are optimized in one large design space all at once. In contrast, for the multi-level optimization, 3 design variables are optimized in subspace 1, followed by 4 design variables in subspace 2 and another 2 design variables in subspace 3.

Results of the optimization performance (as seen in Table 1) indicate faster convergence speed for the multi-level optimization as expected. A significantly lower mean cost function is also obtained for the final

population using the proposed multi-level approach showing good convergence.

Table 1: Comparison of Optimization Approaches

		Single-level Approach	Multi-level Approach
Time taken in total		8940.28 seconds	7096.68 seconds
Generations		30	90 (30 in each subspace)
Best cost functions	Subspace 1	NA	11.21
	Subspace 2	NA	11.21
	Subspace 3	NA	11.21
	Final	11.27	11.21
Mean cost functions	Subspace 1	NA	38.35
	Subspace 2	NA	25.50
	Subspace 3	NA	14.77
	Final	32.19	14.77

Further analysis of the proposed optimization framework and comparison is still on-going.

Conclusions

Traditionally, the design optimization of a motor drive is performed in a single large design space where all design variables are included. This paper employs a multi-level approach instead, where the single large design space is divided into subspaces with fewer design variables each. Independent optimizations are carried out sequentially and moving from one subspace to another, optimal design variables form the baseline parameters for the succeeding optimization run. The proposed formulation of the multi-level optimization problem is based on the 4-level modelling paradigm for a motor drive. Results of the proposed multi-level optimization method show that it is more computationally efficient compared than its counterpart.

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