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High frequency transient comparison based fault location in distribution systems with DGs

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ABSTRACT

Distributed Generations (DGs) in the distribution systems are connected into the buses using power electronic converters. During fault, it is challenging to provide a constant impedance model for DGs in the system frequency due to the variable converter control strategies. System frequency impedance measurement based fault locations can be influenced by the converters' fault behavior. This paper addresses this problem by proposing a wide-area high frequency impedance comparison based fault location technique. The high frequency impedance model of DG is provided. Based on the constant DG impedance model in high frequency range, the faulted line sections can be distinguished by comparing the measured impedance differences without requiring the exact distribution system parameters. Simulation results show that the proposed wide-area transient measurements based fault location method can provide accurate faulted sections in the distribution systems with DGs regardless of the load and DG output variations, measurement noise, unbalanced loads and islanding operations.

Keyword: Fault location; High frequency impedance model; Transient measurement; Distribution systems with DGs

1. Introduction

With the development of the power electronic devices and the renewable energy generations, Distributed Generations (DGs) are increasingly used in the distribution level to reduce the power transmission losses. With planed controls and regulations, DGs can provide power supply to the local loads in case of the main system faults in the form of micro-grids[2][3]. Due to the varying output profiles and relatively low energy density, DGs are connected to the grid with the assistance of converters. This leads to limited fault currents and unique fault transient characteristics (unpredicted internal impedances in the system frequency) from the DG side. Conventional protection and fault location methods might be influenced by the fault current contributed from DGs. Currently, the DG's installation volume is small compared with the main grid and this influence can be ignored. However, in future, where the high density DG penetration is realized [3], this influence will be dramatic and might lead to malfunction of the protection and fault locations.

Considering the existence of the DGs, fault locations in the distribution system can be classified into two groups: the one based on the system impedance estimation and the one based on wide-area voltage sag information.

The conventional system frequency impedance based fault location methods have been employed in industry for quite a longtime. The single-ended technique which uses the pre-fault and post fault information was introduced by Takagi firstly [4][5]. This technique was then modified and extended [6-16] to deal with unknown variables such as the fault distances, the remote-end infeed currents and the fault resistances. Using both the real and imaginary part of the system impedance equations the influences of the fault resistance can be reduced [6][7][15]. For some papers [8][12], the remote-end current is assumed to be equal to the local side pre-fault measurement and the iteration procedure is carried out to balance the assumption errors. However, this error increases with the fault resistance and might lead to un-converged iterations. The load impedances are assumed to be not changed and can be derived from pre-fault load flow calculations [9-10],[15-16] but in the distribution level the loading situation can very significantly and this might lead to enlarged fault location errors. When DGs are considered during fault locations [17-18], synchronization is required from all the available measurement nodes and the load impedances have to be a known value.

Lately, the wide-area measurement based techniques are investigated to overcome the fault location errors in the rela-

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tively large distribution systems. Unlike the conventional impedance based methods, the relationships between the changes of the system impedance (caused by different faults) and the changes of the voltages at different system nodes are used. The voltage variations (voltage sag/increase) are monitored [19-26] to locate faults. The system pre-fault and post-fault steady state voltages at different system nodes are recorded to calculate the voltage sags of different fault scenarios and a map of the voltage variations for different faults can be derived by off-line simulations. Fault location is performed by comparing the pre-calculated maps with on-line measurement using the different pattern recognition algorithms such as the adaptive neuro-fuzzy inference system, the primal-dual interior algorithm [25], the artificial neural network [23] and the decision-tree method [24]. Those methods can adapt to different network topologies by updated off-line simulations. When the DGs are involved [27-29], for most of the mentioned methods, the DGs are considered as additional branches and linearly modeled as constant voltage sources with fixed internal impedances. Considering the DGs fault ride through controls, this model might not be correct and can cause fault location errors.

Most of the impedance and voltage sag based methods use constant impedance models and a voltage source to represent the DGs in the system frequency domain in both normal operations and faults. However, considering the control algorithms, this system frequency model of the DG might not be accurate enough for fault location. Typically, Photovoltaic (PV) inverters can control the current to be within 110% of the rating value (using the current limitation of the inner current control loop) about 1-2 cycles after fault occurs. The inverters exact output fault current depends on the fault distance and fault impedance levels (voltage drops). It is challenging to use only one equation to represent the entire fault transient period of the DGs in the system frequency. When large volumes of DGs are connected in the future, those factors might bring errors to the currently applied fault locations. Also, the DG's distorted output waveform (mostly appears in the low frequency range) will cause errors to the system frequency measurement.

Considering the potential drawbacks of the system frequency measurement based fault locations, for future applications, this paper proposes a fault location in distribution systems with DGs using wide-area high frequency transient measurement. The high frequency impedance DG model that is independent from the control loop logics is provided. Based on the DG model, the high frequency impedance comparison fault location method is developed. The IEEE 123 nodes distribution system that considers unbalanced loading is used to verify the proposed fault location method.

The rest of the paper is organized as follow: after the introduction the basic fault location theory and the high frequency models of DGs are investigated in the Section 2, simulation results are provided and discussed in the Section 3, the overall conclusions are given in the Section 4.

2. Fault location algorithm

2.1 High frequency impedance comparison based fault location

With the development of the "smart grid", smart metering units and other Intelligent Electronic Devices (IEDs) have been commonly utilized in the distribution systems. Accompanied with the circuit breakers/isolators, the faulted sections can be located and isolated from the system without interrupting the normal operation of the rest healthy system.

For the uncompensated distribution systems, both the phase to phase faults and phase to ground faults are considered in this paper. For system grounded with Peterson coils (compensated), single-phase to ground fault is not considered. High-impedance fault location has been a difficult problem in distribution network, and it also has a great influence on the traditional protection method. In this paper, aiming at the scenario of high proportion DGs in distribution network, a fault location method is proposed, which is independent of DG control strategy and output power. The problem of high impedance fault is not the focus of this article. Most of the DGs are connected to the grid with Y/Δ or Y/Y connection transformers. DGs will not add any ground loop to the system and not cause much influences to the conventional fault location algorithm for ground faults in the compensated distribution systems.

For faults with enlarged fault currents, the short circuit fault creates voltage transients (arcs and voltage sudden changes) from the fault inception point that acts as a similar "step transient" with opposite value of the pre-fault voltage amplitude added to the fault point as shown in Fig.1(a). And then, according the Laplace transform, the "step" voltage transient has damping wideband frequency information [30]-[31] throughout the frequency domain as shown in the Fig.1(b). The high frequency transient information in the frequency domain is used as a "source" for the proposed fault location.

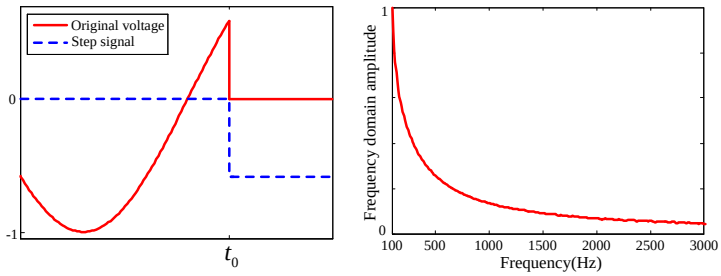


Fig.1 The Schematic diagram of voltage transients (a) Voltage changes in fault (b) Frequency domain amplitude results of voltage transients

The basic algorithm of the proposed method can be explained using a simple system as shown in Fig.2. The IEDs measure the time-domain transient signal of three phase voltage and current, and then the components of different frequencies are acquired by time-frequency transformation method to calculate the impedance value of the corresponding frequency.

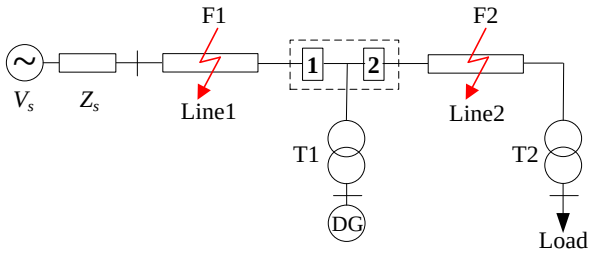


Fig.2 The configuration of simplified distribution system

As shown in Fig.2, the system consists of an equivalent source V_S (contains a three phase voltages in a [3x1] matrix) and system impedance Z_S (contains a three phase supply impedances in a [3x1] matrix), DGs, loads and line sections (contains three phase self and mutual impedances in a [3x3] matrix). Two IEDs and isolation breakers are installed at the location "1" and "2" within the dashed rectangular box which is call the IED group. For a short circuit fault (F1 or F2), regarding only the high frequency domain of the transient waveforms, the system frequency voltage source (V_S) and the low frequency harmonics and distortions generated by the source and DG can be ignored. For fault F1, regarding only the high frequency domain, the equivalent system is shown in the Fig.3.

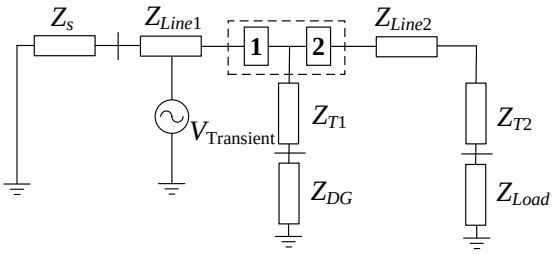


Fig.3 The system configuration in high frequency domain

The high frequency impedances measured by the IEDs within the IED group are:

$$Z_1 = (Z_{T1} + Z_{DG}) // (Z_{Line2} + Z_{T2} + Z_{Load}) \quad (1)$$

$$Z_2 = (Z_{Line2} + Z_{T2} + Z_{Load}) \quad (2)$$

Thus

$$Z_1 = (Z_{T1} + Z_{DG}) // Z_2 \quad (3)$$

The Z_{Line1} and Z_{Line2} are the line high frequency impedance. The Z_{T1}, Z_{T2} and Z_{DG}, Z_{Load} are the transformer, DG and load impedances respectively in the high frequency domain. Z_1 and Z_2 are the measured high frequency impedance of the faulted phases from IED1 and IED2.

Equation (2)-(3) shows that the measured high frequency impedance from IED2 (Z_2) is always larger than Z_1 (for the faulted phases) from IED1 due to the extra paralleled impedance when the fault is imposed to the left side of the IED group (F1). Otherwise for the F2, the measured impedances are:

$$Z_1 = Z_{Line1} + Z_S \quad (4)$$

$$Z_2 = (Z_{T1} + Z_{DG}) // Z_1 \tag{5}$$

Comparing the measured impedance values, the fault location F1 and F2 can be distinguished regardless of the variations of the fault impedance and the load impedance. The proposed fault location method is realized using the three-phase voltage transient and three-phase current transient. The relationship of the high-frequency voltage, current and the fault phase self-impedance is determined by the loop which the high-frequency component current flows after fault. The self-impedance of the faulted phase is calculated and then compared to achieve location. There is no need to decompose positive sequence, negative sequence and zero sequence component. For power lines/cables, the self-inductance is much larger than the mutual-inductance. And with the frequency increases, the difference of impedance value between self-inductance and mutual-inductance will be greater. Therefore, for the high frequency consideration, ignoring the mutual-inductance will has little effect on the calculation results.

This location method relies on the system high impedance model. For the lamp components such as the lines/cables, transformers and passive loads, the high frequency model can be converted using its system frequency impedance value. Actually, in the interested high frequency range limited to up to 3kHz, the inductance will dominate the impedance value. The conversion error can be minimum. The reason that 3kHz limitation is used is due to that: power distribution system contains cables, transformers and motors are regarded as a highly inductive system. To have a good Signal to Noise Ratio (SNR), the measured transients are effective at relative low frequencies. The high frequency information above 3kHz will be greatly attenuated by the inductive of the distribution system. Also, the standard current and voltage transducers normally offer good frequency response below 3kHz. Considering the system characteristics the limitation of the measurement units and the data processing boards, the interested frequency is chosen to be below 3kHz. In this frequency range, the system parasitic capacitance can be ignored.

The most important factor of the proposed fault location method is the high frequency impedance model of the DGs. This is investigated in the part 2.2 of this section.

2.2 High frequency domain impedance model of DG

DGs connected to the grid with the power electronic converters can be classified into two groups: the directly grid connected DGs as the DFIG and the inverter interfaced DGs as the Permanent Magnet Synchronous Generator (PMSG), PV and fuel cells. The high frequency impedance model of the DFIG has been introduced by the previous published paper [32] and inverter interfaced DGs are the focus of modeling within this paper.

The PMSG, PV and fuel cells are the typical renewable DGs connected to the grid through inverters. Most of these DGs have low DC voltage outputs and requires a boost circuit before converted to the AC as shown in Fig.4.

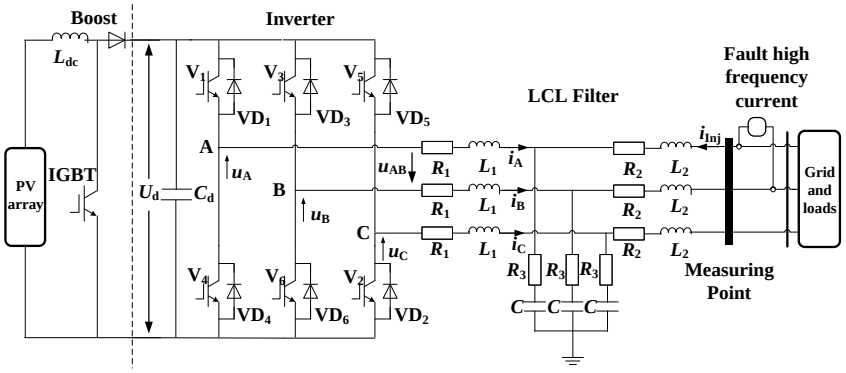


Fig.4 The configuration of the PV DG with a fault as a high frequency disturbance

In Fig.4, the equivalent DC output (from the PV array) is enlarged by the boost converter then converted to AC by the controlled IGBT inverter. The inverter is interfaced with the grid by a "T" filter [33]. For the control design (steady state), only the R_1, L_1, R_2 and L_2 are considered and the filter capacitor which only creates paths for high frequency distortions is ignored. During the initial of the fault (for example, between phase A and phase B) which is seen as a voltage step, a current transient on the filtering inductor is created. The initial of the current transient has decayed frequency domain information [30]-[31] as in introduced at the beginning of the part 2.1. The high frequency current injected from the fault point will flow through the inverter and all the three phases. By analysis the paths of the injected high frequency current, the DG high frequency equivalent impedance can be calculated.

For a simplified analysis, the power electronic devices are regarded as ideal devices whose on-state is viewed as a short circuit and off-state as an open circuit in the interested high frequency range.

According to the potential clamp effect of DC voltage at the capacitor (U_d) and the complementary on-off control law of upper and lower bridge arms in the same phase (the upper and lower bridge arms cannot be on and

off at the same time), it can be concluded that a certain IGBT's on-off control has complete correspondence to on-off state of the bridge arm in which the IGBT situated, thereby the Pulse-Width Modulation (PWM) voltage wave (u_A) can correspond completely with the on-off state of bridge arms in phase. For instance, when u_A is positive, bridge arm 1 will be on; and when u_A is negative, bridge arm 4 will be on. Also, according to the relation law between i_A and freewheeling diode state in phase A, the on-off state of elements (V_1,VD_1,V_4,VD_4) in phase A bridge arms can be concluded: When i_A is positive , V_1 or VD_4 will be on; and when i_A is negative , V_4 or VD_1 will be on.

The high voltage level of u_{AB} ($+U_d$) corresponds to the on-state of bridge arm 1 and 6, and V_1, V_6 are controlled at its on-state at this time (the on/off state of the VD1 and VD6 are decided by the current direction). Utilizing the combination of i_A and i_B directions, whether the IGBT or the freewheeling diode is the actual path of the current can be worked out. Similarly, the low voltage level of u_{AB} ($-U_d$) means the on-state of bridge arm 3 and 4, and the zero voltage level of u_{AB} (0) means the on-state of bridge arm 1and 3 or 4 and 6. Detailed analysis of the case $-U_d$ and the case "0" is of the same way as the case $+U_d$.

Based on all the analyses, rule of on-off states of all bridge arms and elements in the whole inverter as well as their timing conversion sequence can be concluded from the PWM voltage waves and current waves of three phases. Due to the reverse blocked diode in the boost circuit and the very low impedance of the DC link capacitor in the high frequency range, little fault transient will go through the boost circuit. The boost converter can be roughly considered as open circuit in high frequency. For a fault between the phase A and phase B, the paths for the transient current signal can be summarized into four categories:

(1) IGBT4, IGBT5 and Diode6 are conducting.

In this condition, the transient current from the phase A is diverted to two branches after the IGBT4:

a) Flows through Diode6 to phase B;

b) Flows through C_d (DC side capacitor) and IGBT5 to phase C, and finally flows back to phase B through the three-phase common connection point of the shunted filter.

(2) IGBT5, Diode1 and Diode6 are conducting.

In this situation, the transient current from phase A is diverted to two branches after the Diode1:

(a) Flows through C_d (DC side capacitor) and Diode6 to phase B;

(b) Flows through IGBT5 to phase C, and finally flows back to phase B through the three-phase common connection point of the shunted filter.

(3) IGBT3, Diode1 and Diode2 are conducting.

In this situation, the transient current from phase A is diverted to two branches after the Diode1:

(a) Flows through IGBT3 to phase B;

(b) Flows through C_d (DC side capacitor) and Diode2 to phase C, and finally flows back to phase B through the three-phase common connection point of the shunted filter.

(4) IGBT3 and Diode1 are conducting.

In this situation, the transient current from phase A flows through Diode1 and IGBT3 to phase B.

The four impedance structures presented represent the possible impedance structures of high-frequency component loop for all the different switching conditions of the inverter. For this fault location method, it is demonstrated that DG has the stable high-frequency impedance value in the high-frequency component network after fault and this impedance is not related to its specific control setting values.

The current paths for above four conductions are shown in the Fig.5.

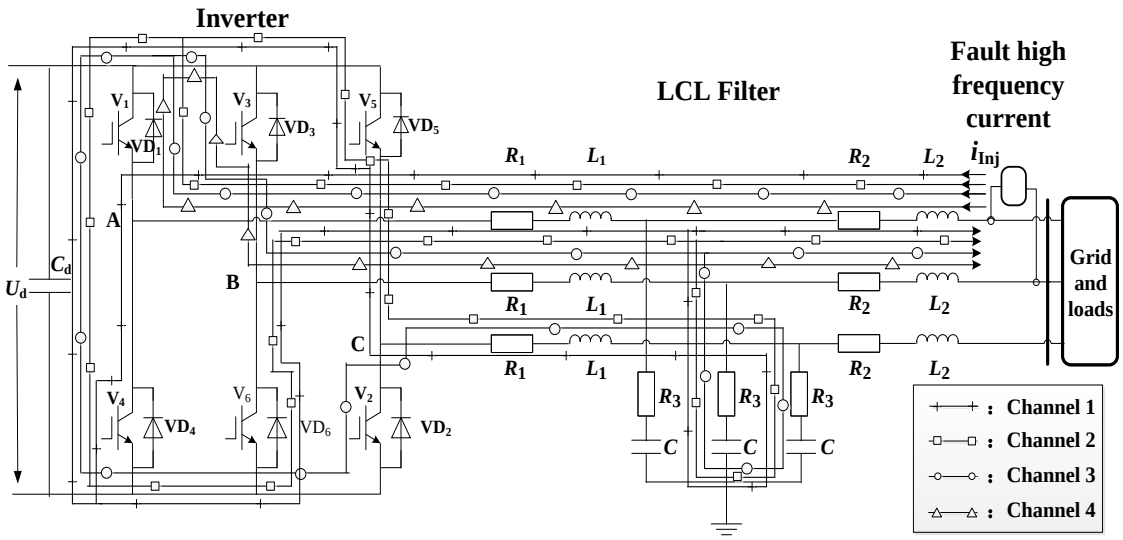
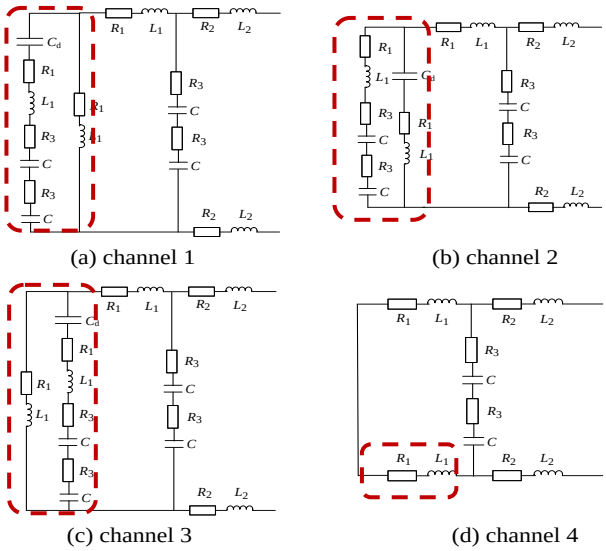


Fig.5 The paths for the fault transient current between phase A and phase B

As shown in the Fig.5, compared with symmetric operating state, the transient current (generated by fault between phases or between phase and ground) will create asymmetrical loops. The current transient flows from phase A into not only phase B but also phase C. For these four situations, the equivalent impedance networks from measuring point are shown in the Fig.6.



(a) channel 1 (b) channel 2

(c) channel 3 (d) channel 4

Fig.6 The high frequency impedance seen from the fault transients point

Although presented as different circuit topologies as shown in the dashed rectangular boxes of the Fig.6, the equivalent high frequency impedances are dominated by the high frequency inductance and capacitance values and have small difference. Ignoring the small resistance value, the first three topologies (Fig.6 (a)-(c)) have the same equivalent impedances. Compared with circuits within dashed rectangular boxes of the first three topologies, the forth one does not have a paralleled capacitor. However, for paralleled connected inductance and capacitance, the total impedance value will be dominated by the inductance in the relatively low frequency range and by the capacitance in the relatively high frequency range. This will result in very small impedance difference between the four topologies in a relatively low frequency as shown in the Fig.7.

As shown in the Fig.7, both the impedance amplitudes and its phase angles of the four topologies (in the Fig.6) have small differences in the frequency range below 3kHz. For practical utilizations, this difference can be ignored. In this case, for the interested frequency range less than 3kHz, seen from the fault transient point, the high frequency impedance of inverter based DGs can be approximately represented by one circuit as shown in the Fig.6 (a).

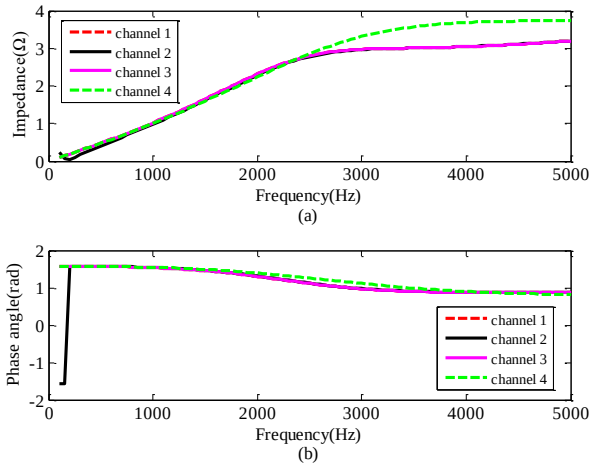


Fig.7 High frequency impedances of all four topologies

For modeling a DG at the system frequency, the DG source output equations (such as the PV battery models) and the control logic equations are considered. For different control algorithms and source output characteristics, the equations vary and it is difficult to build an accurate model that is suitable for all the control designs. However, in the high frequency range, the fault high frequency transient is bypassed by the inverter due to the DC link capacitors (act as short circuit in the high frequency) and the model of the DG can be simplified by the modeling of the inverters. The other advantage of using the high frequency model is that the control algorithm is not considered due to the fact that control response time that is about several tens to hundreds ms is much longer than the fault initial transient. Due to this fact, the high frequency model of the DG will not change in case of DGs with different control settings and power ratings.

3. Simulation results

3.1 Results of DG high frequency impedance modeling

In the impedance measurement based fault location technique, the high frequency impedance model of the DG is required to distinguish the faulted sections. The proposed high frequency impedance models of different DGs are verified using a 0.5MW PV built in the Matlab/Simulink platform [33]. The detailed parameters of the DGs are provided in the Appendix. During a fault, the transients of the faulted phases are recorded and then converted into the frequency domain for impedance estimation.

Both the voltage and current data are recorded by a short rectangular window (12ms in total length and 6ms after the transients) with a 50kHz sampling frequency. The captured data is filtered with a cut-off frequency of 3.5kHz and then transformed into frequency domain for high frequency impedance estimation. The 3.5kHz cut-off frequency is used to maintain a good SNR in the interested frequency range. The 50kHz sampling frequency can provide adequate frequency resolution to capture the initial fault transients and be within the data processing limitation of a practical signal processing board.

Compared with the results shown in Fig.7, seen from the high voltage side of the DTs, the measurement impedance is dominated by the transformer inductance as shown in Fig.8. The DG connected to grid through inverters will have slightly less accurate impedance estimation in the high frequency range due to the inverter switching frequency (at about 2kHz). This difference can be reduced after performing with curve fittings and the error can be ignored for fault location considering the relatively large DT inductance.

In the high frequency range, the calculated impedance is dominated by the large reactance value (this is especially true when the DT transformer is considered) and estimated resistance will have poor accuracy. This results in a large error in the phase angle results. However, the proposed fault location only uses only the comparison of impedance amplitude and the phase angle error will not cause fault location differences. Also, due to the fact that only the amplitude information is used, the measured data from all the IEDs in the large distribution system dose not have to be synchronized.

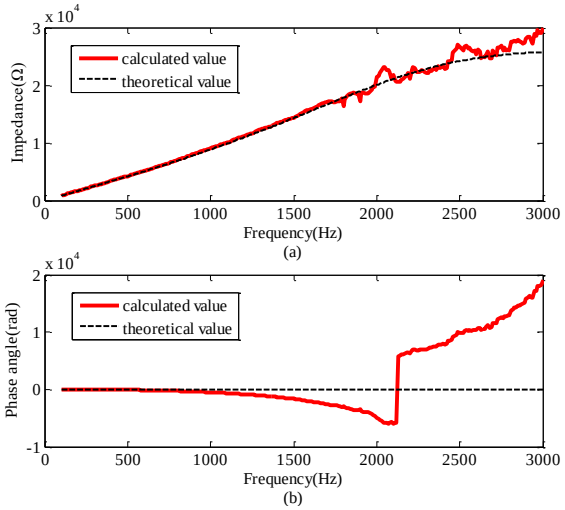


Fig.8 High frequency impedance seen from the high voltage side of the DT (a) Amplitude results (b) Phase angle results

3.2 Results of fault location

The proposed fault location scheme is further tested using simulation results from a large distribution system. The IEEE 123 nodes distribution system[34] that has different length of laterals and unbalanced loads at the end of some distribution feeders is used. DGs are added in the testing system (the original IEEE 123 nodes system does not have DGs) as shown in the Fig.9. Detailed parameters are provided in the Appendix.

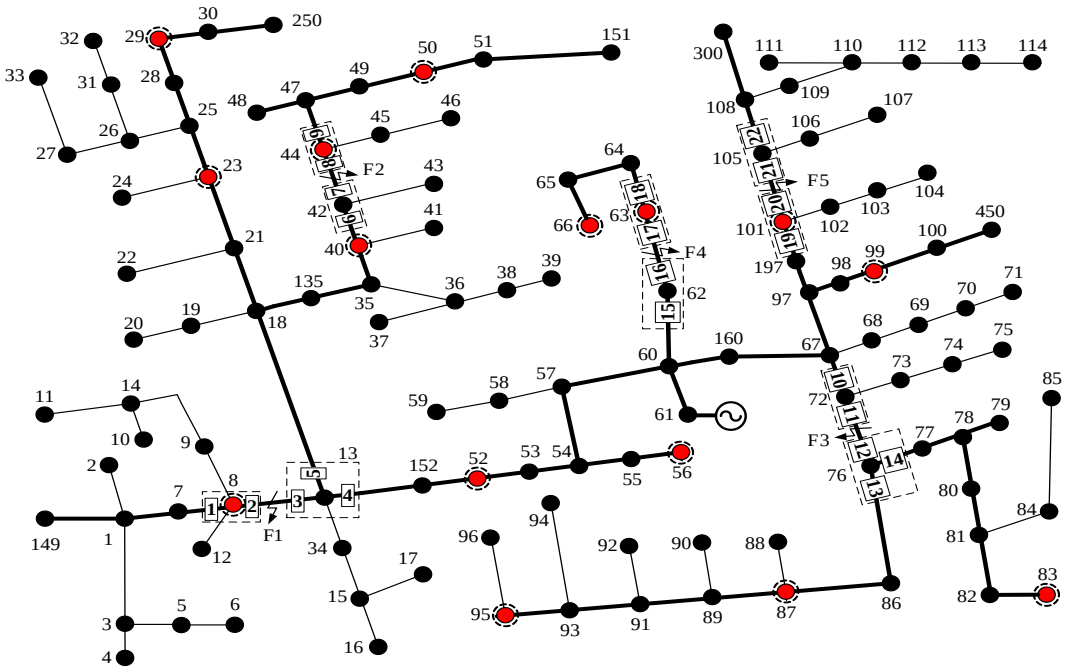


Fig.9 Configuration of the IEEE 123 nodes testing distribution system with DGs

As shown in the Fig.9, the distribution system contains different lengths of lines which connect multiple loads (the black nodes) and DGs (the red nodes with dashed circle). The three-phase main lines in the system have been bold highlighted, and all the IEDs are installed at the main line nodes. The detail parameters of the DGs, loads and lines of the system are provided in the Appendix.

Radom faults (taking phase-A to phase-B fault with 20Ω fault resistance as example) are placed in the system and the measured impedance from the IEDs that are nearby the faults are shown in the Table1. Considering signal processing speed of a practical data processing board, not all the high frequency range impedance values (as shown in the Fig.7) are used and only results of 1.5kHz impedance are employed as shown in the Table 1.

The neighboring IEDs (installed closed to each of the nodes) are pre-arranged into different groups (the 10 dashed rectangular boxes of Fig.8). For all the faults, the faulted section can be easily distinguished comparing the impedance value within each IED groups. For example, as shown in the Table1, when F5 occurs, the measured high frequency

impedances are: $Z_{19} > Z_{20}$ (this indicates a fault to the right side of the group 9) and $Z_{21} < Z_{22}$ (this indicates a fault to the left side of the group 10) and the faulted section can be fixed as between the group 10 and the group 9. This algorithm can be applied to the other groups, such as $Z_{13} > Z_{12}$ and $Z_{14} > Z_{12}$ indicates that the F5 is located to the left side of the group 6. For each of the faults, using the fault direction information derived from all the groups, the faulted section can be located. The solid rectangular boxes in the Table1 indicate the fault is located to the right side of the groups and the dashed rectangular boxes indicate the fault is located to the left side of the groups.

Table 1

The high-frequency impedances at estimated at 1.5kHz from each IED during different fault scenarios

Group number	IED measuring impedance	F1	F2	F3	F4	F5
1	Z_1	39898.3926	39887.1066	39926.2117	39917.4772	39926.1380
	Z_2	7382.5085	7380.4199	7387.6561	7386.0401	7387.6425
2	Z_3	457.3442	7383.5359	7390.7747	7389.1581	7390.7611
	Z_4	605.2855	605.1148	1493.7741	1493.4473	1493.7713
	Z_5	1870.8578	559.2902	1872.1621	1871.7524	1872.1586
3	Z_6	4544.1162	491.4290	4547.2830	4546.2881	4547.2745
	Z_7	4723.5181	480.4179	4726.8098	4725.7757	4726.8010
4	Z_8	4721.0905	4717.9657	4724.3805	4723.3469	4724.3717
	Z_9	7908.1912	7902.9579	7913.7013	7911.9693	7913.6865
5	Z_{10}	2272.9757	2272.3325	526.0824	2273.1321	2273.4339
	Z_{11}	2362.6604	2361.9919	511.5022	2362.8231	2363.1367
6	Z_{12}	2360.3049	2359.6370	2360.5101	2360.4674	2360.7807
	Z_{13}	4725.8698	4724.5319	4726.2812	4726.1961	4726.8232
	Z_{14}	5692.8262	5691.2151	5693.3211	5693.2183	5693.9740
7	Z_{15}	3903.4933	3902.3887	3904.6166	477.0277	3904.6094
	Z_{16}	4474.2300	4472.9640	4475.5173	469.7075	4475.5090
8	Z_{17}	4472.7745	4471.5090	4474.0614	4472.8985	4474.0531
	Z_{18}	7231.8669	7229.8213	7233.9471	7232.0665	7233.9336
9	Z_{19}	7177.2311	7175.1998	7178.6916	7177.7257	457.5737
	Z_{20}	14134.3926	14130.3939	14137.2671	14135.3640	443.6553
10	Z_{21}	14131.5312	14127.5331	14134.4051	14132.5024	14132.6529
	Z_{22}	17125.1023	17120.2547	17128.5880	17126.2836	17126.4651

Faults located to the right side of IED groups

Faults located to the left side of the IED groups

As introduced in the Section 2, comparing the estimated impedances within each IED and exchanging the results from IEDs, the proposed fault location can correctly decide the faulted sections and is immune to the fault impedance and the load variations. In case of loss communication of some of the IEDs or for a system with fewer IEDs than the presented system, the proposed method can still work but provide a relatively enlarged fault location area.

In the high frequency domain, the inverter's DC capacitor banks act as a short circuit and isolate the power generation part of the DGs. For DGs with different primary sources, such as the wind turbine with the Permanent-Magnetic Synchronous Generator (PMSG), the inverter based high frequency impedance model will still be suitable for fault location. However, compared with the PV, the PMSG will normally have a rated installation volume of 2MW and this leads to larger grid connected filtering inductor which has different high frequency impedance. This will result in difference of the each of the estimated values in the Table 1 but the comparison trend will be the same for the same set of fault scenario.

The noise would add errors to the impedance based fault locations. However, the proposed method employs the comparison results to locate fault rather than a fixed value. The noise will only influence the impedance values, but will not cause significant influence to the fault location results.

The high frequency impedance results in Table2 are the results with 2% white noise. Compared with the results derived from no noise situation (Table1), it can be seen that the noise did have certain impact on the specific impedance values from the measurement point, but this impact is small and the magnitude relation of the high-frequency impedance is not changed very much. Therefore, the overall location results will not be affected.

This method is also effective when the distribution system with DGs works as a islanding system. For example, when the main system connection node (the Node 61 in the system) is opened the DGs are operating in the islanding situation. The impedance of islanding situation at 1.5kHz from each IED are shown in Table 3.

In an islanded system, if the DGs' output power matches with the load consumption power, the system operates in the system frequency (50Hz). Otherwise, if the DGs provide more/less power than the load consumption power, the system will operates at a frequency higher/lower than the system frequency. In case of this frequency deviation exceeds the islanding protection threshold DGs will be disconnected from the grid by its own protections. This paper uses only the high frequency impedance comparison results to location the fault. During the fault location, the system frequency is short circuited as discussed in the Section II and the system frequency variation will not influence the fault location results. The

situations that DGs are tripped by the islanding protections will lead to different estimated impedance values (similar as the load variations) seen from each of the IEDs but the comparison trend will not be changed as shown in the Table3.

This paper uses the comparison of the IEDs impedance estimation results to located fault. The exact system parameters are not required and it is immune to the system topology variations. This algorithm does not require synchronized measurement and this reduces the strength on real time communications. IED communication failure, will not results in total wrong fault location results but enlarged fault location error.

Table 2

The high-frequency impedances at estimated at 1.5kHz from each IED during different fault scenarios with 2% white noise

Group number	IED measuring impedance	F1	F2	F3	F4	F5
1	Z_1	38569.8498	40465.7596	39424.4244	38732.5748	40722.2668
	Z_2	7316.2984	7487.4528	7487.4528	7371.1429	7423.7483
2	Z_3	456.3876	7296.7380	7290.7471	7399.1413	7360.7122
	Z_4	604.0873	603.9770	1500.3390	1495.7991	1487.7772
	Z_5	1922.6459	557.0225	1864.5756	1860.4987	1864.6590
3	Z_6	4612.6729	490.0858	4556.8995	4544.1088	4576.8524
	Z_7	4794.3033	483.5585	4781.7142	4779.9972	4791.2148
4	Z_8	4689.3640	4768.0930	4701.3451	4707.7756	4737.7578
	Z_9	7924.1587	8043.5871	8096.1492	7848.2476	7971.5980
5	Z_{10}	2275.5985	2280.7258	526.6417	2278.8483	2281.8406
	Z_{11}	2368.8808	2352.6931	512.7831	2377.6684	2370.9214
6	Z_{12}	2431.9209	2356.8083	2361.5349	2401.7931	2337.9832
	Z_{13}	4708.5791	4757.8381	4697.7363	4744.9101	4768.5435
	Z_{14}	5656.0248	5782.4556	5769.2248	5744.7815	5806.5344
7	Z_{15}	3978.9935	4009.6932	3891.4758	477.9554	3918.1607
	Z_{16}	4771.2215	4844.7043	4683.8184	470.3795	4787.0564
8	Z_{17}	4426.2369	4563.3848	4468.3695	4669.0500	4412.6863
	Z_{18}	7081.6010	7283.7723	7488.9004	7339.1921	7189.8066
9	Z_{19}	7321.2594	7055.6626	7286.5632	7376.5296	456.2748
	Z_{20}	14013.0526	14956.7758	14209.4082	13893.1436	442.5840
10	Z_{21}	14362.9742	13962.4219	14178.2538	14271.2264	13910.0794
	Z_{22}	17154.2413	17470.7704	17495.8551	16944.2974	17551.4767

Faults located to the right side of IED groups

Faults located to the left side of the IED groups

Table 3

The high-frequency impedances at estimated at 1.5kHz from each IED during islanding situation

Group number	IED measuring impedance	F1	F2	F3	F4	F5
1	Z_1	39899.3551	39897.6914	39922.5414	39915.3675	39919.7600
	Z_2	7383.0131	7382.3798	7386.9773	7385.6503	7386.4627
2	Z_3	593.2120	7385.4964	7390.0957	7388.7681	7389.5809
	Z_4	868.6218	868.5655	1493.6367	1493.3682	1493.5326
	Z_5	1870.9457	777.1678	1871.9898	1871.6533	1871.8594
3	Z_6	4544.3290	639.6551	4546.8644	4546.0467	4546.5475
	Z_7	4723.7392	627.2628	4726.3747	4725.5247	4726.0453
4	Z_8	4721.3115	4718.1560	4723.9456	4723.0960	4723.6163
	Z_9	7908.5592	7903.2745	7912.9717	7911.5471	7912.4198
5	Z_{10}	2273.0982	2272.9507	728.2325	2273.0117	2273.0709
	Z_{11}	2362.7878	2362.6345	712.6018	2362.6978	2362.7594
6	Z_{12}	2360.4322	2360.2790	2360.8376	2360.3423	2360.4038
	Z_{13}	4726.1257	4725.8202	4726.9361	4725.9467	4726.0692
	Z_{14}	5693.1334	5692.7643	5694.1108	5692.9169	5693.0650
7	Z_{15}	3903.7041	3903.4512	3904.2575	636.8468	3903.9855
	Z_{16}	4474.4713	4474.1812	4475.1056	623.8632	4474.7937
8	Z_{17}	4473.0157	4472.7257	4473.6498	4473.5249	4473.3381
	Z_{18}	7232.2559	7231.7860	7233.2810	7233.0802	7232.7767
9	Z_{19}	7177.6187	7177.1536	7178.0327	7177.3459	597.5407
	Z_{20}	14135.1529	14134.2342	14135.9679	14134.6132	574.0161
10	Z_{21}	14132.2913	14131.3728	14133.1062	14131.7518	14134.6202
	Z_{22}	17126.0284	17124.9198	17127.0166	17125.3784	17128.8452

Faults located to the right side of IED groups

Faults located to the left side of the IED groups

4. Conclusions

This paper proposes a high frequency impedance comparison based fault location method for systems with DGs. The high frequency impedance model of inverter interfaced DG (PV) is provided for theoretical support. Compared with the system frequency impedance and/or voltage measurement based methods, the proposed method considers detailed DG models and is not influenced by the DG steady state control logic and the low frequency distortions during a fault. The short data window which only includes 6ms post-fault transients is used to prevent the influence of the control loops that normally have a cascade response time larger than several tens ms. The fault location method uses only the high frequency comparison of the neighboring IEDs to decide the faulted sections without requiring the exact system parameters. It is suitable for the distribution systems that are frequently modified by adding/removing some of lines and nodes. Simulation results show that the proposed fault location can cope with measurement errors caused by the noise and unbalanced loads and provide good fault location results in the complicated distribution system, even in the DG's islanding situation.

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Appendix

Table 1

Parameters of PV model in tested system

Parameter	Value	Parameter	Value
rated power	0.5 MW	rated voltage	380 V
DC side capacitor(C_d)	5000 μF	DC side voltage	800 V
inverter side inductance(L_1)	0.05 mH	inverter side resistance(R_1)	0.0001 Ω
grid side inductance(L_2)	0.025 mH	grid side resistance(R_2)	0.0001 Ω
filter capacitor(C)	50 μF	filter resistance(R_3)	1.2 Ω

Table 2

Line parameters in tested system

Line type		Phasing	Resistance per unit length (Ω/km)	Reactance per unit length (Ω/km)
Overhead lines	1	A B C N	0.290	0.651
	2	C A B N	0.287	0.662
	3	B C A N	0.284	0.670
	4	C B A N	0.290	0.651
	5	B A C N	0.284	0.670
	6	A C B N	0.287	0.662
	7	A C N	0.284	0.670
	8	A B N	0.284	0.670
	9	A N	0.826	0.837
	10	B N	0.826	0.837
	11	C N	0.826	0.837
Underground lines	12	A B C	0.953	0.445

Table 3

Network parameters in tested system

Node A	Node B	Length (m)	Line type	Node A	Node B	Length (m)	Line type	Node A	Node B	Length (m)	Line type
1	2	53.3	10	40	42	76.2	1	80	81	144.8	6
1	3	76.2	11	42	43	152.4	10	81	82	76.2	6
1	7	91.4	1	42	44	61.0	1	81	84	205.7	11
3	4	61.0	11	44	45	61.0	9	82	83	76.2	6
3	5	99.1	11	44	47	76.2	1	84	85	144.8	11
5	6	76.2	11	45	46	91.4	9	86	87	137.2	6
7	8	61.0	1	47	48	45.7	4	87	88	53.3	9
8	12	68.6	10	47	49	76.2	4	87	89	83.8	6
8	9	68.6	9	49	50	76.2	4	89	90	68.6	10
8	13	91.4	1	50	51	76.2	4	89	91	68.6	6
9	14	129.5	9	51	151	152.4	4	91	92	91.4	11
13	34	45.7	11	52	53	61.0	1	91	93	68.6	6
13	18	251.5	2	53	54	38.1	1	93	94	83.8	9
14	11	76.2	9	54	55	83.8	1	93	95	91.4	6
14	10	76.2	9	54	57	106.7	3	95	96	61.0	10
15	16	114.3	11	55	56	83.8	1	97	98	83.8	3
15	17	106.7	11	57	58	76.2	10	98	99	167.6	3
18	19	76.2	9	57	60	228.6	3	99	100	91.4	3
18	21	91.4	2	58	59	76.2	10	100	450	243.8	3
19	20	99.1	9	60	61	167.6	5	101	102	68.6	11
21	22	160.0	10	60	62	76.2	12	101	105	83.8	3
21	23	76.2	2	62	63	53.3	12	102	103	99.1	11
23	24	167.6	11	63	64	106.7	12	103	104	213.4	11
23	25	83.8	2	64	65	129.5	12	105	106	68.6	10
25	26	106.7	7	65	66	99.1	12	105	108	99.1	3
25	28	61.0	2	67	68	61.0	9	106	107	175.3	10
26	27	83.8	7	67	72	83.8	3	108	109	137.2	9
26	31	68.6	11	67	97	76.2	3	108	300	304.8	3
27	33	152.4	9	68	69	83.8	9	109	110	91.4	9
28	29	91.4	2	69	70	99.1	9	110	111	175.3	9
29	30	106.7	2	70	71	83.8	9	110	112	38.1	9
30	250	61.0	2	72	73	83.8	11	112	113	160.0	9
31	32	91.4	11	72	76	61.0	3	113	114	99.1	9
34	15	30.5	11	73	74	106.7	11	135	35	114.3	4
35	36	198.1	8	74	75	121.9	11	149	1	121.9	1
35	40	76.2	1	76	77	121.9	6	152	52	121.9	1
36	37	91.4	9	76	86	213.4	3	160	67	106.7	6
36	38	76.2	10	77	78	30.5	6	197	101	76.2	3
38	39	99.1	10	78	79	68.6	6				
40	41	99.1	11	78	80	144.8	6				

Table 4

Modified load parameters in tested system

Node	Phase A(kVA)	Phase B(kVA)	Phase C(kVA)	Node	Phase A(kVA)	Phase B(kVA)	Phase C(kVA)
1	40+j20	0	0	64	75+j35	75+j35	75+j35
2	0	20+j10	0	65	35+j25	35+j25	70+j50
4	0	0	40+j20	66	70+j50	40+j20	75+j35
5	0	0	20+j10	68	20+j10	0	0
6	0	0	40+j20	69	40+j20	0	0
7	20+j10	40+j20	20+j10	70	20+j10	0	0
9	40+j20	0	0	71	40+j20	0	0
10	20+j10	0	0	72	40+j20	75+j35	35+j25
11	40+j20	0	0	73	0	0	40+j20
12	0	20+j10	0	74	0	0	40+j20
16	0	0	40+j20	75	0	0	40+j20
17	0	0	20+j10	76	105+j80	70+j50	70+j50
19	40+j20	0	0	77	70+j50	40+j20	70+j50
20	40+j20	0	0	79	40+j20	70+j50	40+j20
22	0	40+j20	0	80	40+j20	40+j20	20+j10
24	0	0	40+j20	82	40+j20	70+j50	105+j80
28	40+j20	75+j35	35+j25	83	75+j35	40+j20	20+j10
30	35+j25	40+j20	40+j20	84	0	0	20+j10
31	0	0	20+j10	85	0	0	40+j20
32	0	0	20+j10	86	40+j20	20+j10	75+j35
33	40+j20	0	0	87	20+j10	70+j50	40+j20
34	0	0	40+j20	88	40+j20	0	0
35	40+j20	35+j25	75+j35	90	0	40+j20	0
37	40+j20	0	0	92	0	0	40+j20
38	0	20+j10	0	94	40+j20	0	0
39	0	20+j10	0	95	40+j20	20+j10	40+j20
41	0	0	20+j10	96	0	20+j10	0
42	20+j10	40+j20	70+j50	98	40+j20	70+j50	40+j20
43	0	40+j20	0	99	35+j25	40+j20	75+j35
45	20+j10	0	0	100	70+j50	40+j20	40+j20
46	20+j10	0	0	102	0	0	20+j10
47	35+j25	35+j25	35+j25	103	0	0	40+j20
48	70+j50	70+j50	70+j50	104	0	0	40+j20
49	35+j25	70+j50	35+j25	105	35+j25	40+j20	75+j35
51	20+j10	70+j50	70+j50	106	0	40+j20	0
53	40+j20	70+j50	40+j20	107	0	40+j20	0
55	20+j10	70+j50	70+j50	109	40+j20	0	0
58	0	20+j10	0	111	20+j10	0	0
59	0	20+j10	0	112	20+j10	0	0
60	20+j10	75+j35	20+j10	113	20+j10	0	0
62	75+j35	35+j25	40+j20	114	20+j10	0	0
63	40+j20	75+j35	40+j20				