Remedial Strategies of T-NPC Three-Level Asymmetric Six-phase PMSM Drives Based on SVM-DTC

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***Abstract*—In this paper, novel remedial direct torque control (DTC) schemes are proposed for open-circuit faults in T-type neutral-point-clamping (T-NPC) three-level asymmetric six-phase PMSM drives. First, a simplified space vector modulation (SVM) is designed and applied for DTC controlled asymmetric six-phase drive, in such a way that both good current harmonic performance and fast dynamic response are available. Based on the SVM-DTC scheme, a remedial strategy is proposed for the open-circuit faults in phase windings. The key is to derive the relationship between the stator fluxes and the stator voltages of all phases under faulty condition. Then, a derived perturbation term is compensated for normal voltage references, and the fault tolerant scheme is thus implemented without changing control structure of normal condition. The remedial DTC schemes are also studied and proposed for open-switch faults in T-NPC six-phase drives. The modulation methods are redesigned for the faults in half-bridge switches and neutral-point-clamping switches. The experiments are carried out on a laboratory prototype to verify the validity and performance of the proposed fault tolerant control schemes.**

***Index Terms*—Asymmetric six-phase PMSM drives, T-NPC inverter, SVM-DTC, fault tolerant control.**

I. INTRODUCTION

RECENTLY, the interests in multiphase motor drives have drawn more attractions in many industrial applications, especially for high-power and high-reliability applications such as electric elevator, aerospace, electric vehicle, and ship propulsion [1-5]. The main advantages of multiphase motor drives over three-phase ones can be summarized as following: lower torque pulsations, lower current stress on semiconductors and machine windings, lower DC link current harmonics, larger power rating, and higher fault tolerant capability [6-8]. On the other hand, the T-NPC three-level inverters become more popular for low-voltage and high-reliability applications due to their superior harmonic performance and better fault tolerant control capability [9-10]. Table I compares the performance of T-NPC three-level topology with two-level topology and diode clamped NPC (D-NPC) three-level topology [11-13]. The T-NPC three-level inverter offers the advantages of low voltage harmonics, small common-mode voltage, small electromagnetic interference (EMI), high efficiency and high fault tolerant capability. Since the power switch in half bridge withstand full voltage of DC link, the T-NPC three-level inverter is suitable for low-voltage applications compared to D-NPC three-level inverter. In terms of open-switch faults, the faulty leg in two-level inverter has to be removed completely. For D-NPC three-level inverter, the faulty leg is also useless when one inner switch of the leg is open. Compared to them, the faulty leg of T-NPC three-level inverter can still be used for fault tolerant control, no matter which switch breaks down. In case of an open-phase fault, the faulty phase can be connected to neutral point of DC link in three-level inverter through circuit reconstruction. The three-level inverter has good control over neutral point voltage, which is difficult for two-level inverter to balance [14-15].

TABLE I
PERFORMANCE COMPARISON

	Two-level	D-NPC three-level	T-NPC three-level
IGBT voltage	U_{dc}	$U_{dc}/2$	$U_{dc}/2$, U_{dc}
Harmonics	high	low	low
Loss (5-30 kHz)	large	middle	small
EMI	large	small	small
Fault tolerant capability	low	middle	high

In the asymmetric six-phase machines, the 6th order harmonic torque pulsation can be eliminated due to the opposition of these components produced by two sets of three-phase windings [16]. Nevertheless, large low-order current harmonics will appear without effective suppression. The emergence of vector space decomposition (VSD) method

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proposed in [17] makes it possible for SVM scheme to be applied in multiphase motors, where the low-order harmonics can be eliminated by designing the SVM scheme [18-20]. However, the low-order harmonics induced from back EMF and asymmetry on harmonic subspace can not be compensated by design of SVM.

Several common control techniques are presented and compared in [21]. The use of current loop and SVM in FOC can achieve superior stator currents, but its dynamic response is limited. The switch-table based DTC (ST-DTC) is a robust control method, which is able to track torque and flux references fast by selecting voltage vectors directly. By combining SVM and DTC, the SVM-DTC can offer well-defined harmonic spectrum, reduced torque and flux pulsations, and fast dynamic response. Therefore, the SVM-DTC is considered a good solution for general-purpose drives within a wide power range. However, to the best of authors' knowledge, the study of SVM-DTC has been limited in two-level inverter fed drives. The investigation of SVM-DTC for multilevel multiphase drive is still absent today.

As aforementioned, the multiphase drives have higher fault tolerant capability with more phase legs compared to three-phase system. Among various faults of motor drives, the open-phase fault is a typical one and it can be caused by power electronics devices or stator windings. So far, many fault tolerant control schemes have been proposed to cope with open-phase faults in multiphase drive systems. The simplest solution is to cut off the whole fault winding [22]. As a result, the phase number of multiphase motor is degraded and the maximum output power is reduced. In [23], the models of a six-phase induction machine have been deduced for both healthy and faulty conditions, and the fuzzy logic control and sliding mode control (SMC) have been adopted to estimate rotor position. However, the faulty condition of the motor winding must be detected offline, which are not suitable for the faulty condition occurring during the operating motor. Furthermore, the fault tolerant control technique for five-phase permanent-magnet motors with trapezoidal back electromotive forces under various open-circuit conditions has been proposed in [24]. The fault tolerant control in [25-26] presents the optimized copper loss for multiple-channel motor drives. The loss of faulty phase is compensated by increasing the current amplitude of the healthy phases. But they are based on field oriented control (FOC) and limited to discussion of two-level inverters fed drives. The literature [27] builds the five-phase induction motor (IM) model in faulty condition and reconstructs complex SVM based on the model with structural unbalance. The ST-DTC technique is extended to the open-phase fault operation. Different from them, a novel SVM-DTC based open-phase fault tolerant control is proposed for T-NPC three-level inverters fed asymmetric six-phase PMSM drives. The complexity of the proposed fault tolerant scheme does not increase with inverter levels. Besides, the whole control system is almost unchanged before and after introduction of fault tolerant control in the proposed scheme. It should be noted that effective fault detection is very important for fault tolerant control, since proper remedial measures can be taken after detection of fault. Since the emphasis of this paper is to study fault tolerant control schemes for T-NPC inverters fed six-phase PMSM drives, the concrete methods about fault detection will not be discussed in details in this paper. The related research about fault diagnosis of electric drives could be found in some previous literatures [28-30].

In power converters, the open-switch fault is also a common problem. As aforementioned, the T-NPC inverter can provide higher fault tolerant ability besides good harmonic performance. Actually, some researches have been taken for open-switch faults in the T-NPC inverters [31-33]. The fault tolerant control schemes based on SVM have been proposed for grid-connected T-NPC rectifiers with unit power factor in [32]. When open-switch fault occurs in neutral-point-clamping switches, the current distortion and fluctuation in mid-point of DC link can be mitigated with the proposed scheme. In [34], the discussion of open-switch faults has been presented for both half-bridge switches and neutral-point-clamping switches. However, to the best of authors' knowledge, all previous researches about fault tolerant control of T-NPC inverters are focused on three-phase system, and mitigation of fluctuation in neutral-point voltage for DC link is limited. Different from that, the DTC based fault tolerant operation is studied for open-switch faults in T-NPC inverters fed asymmetric six-phase PMSM drive. The fault tolerant schemes have been proposed for open-circuit faults in both half-bridge switches and neutral-point-clamping switches. Due to the controllability of redundant small voltage vectors in healthy converter channel, the current distortion and the fluctuation in neutral-point voltage of DC link can be suppressed effectively.

The motivation of this paper is to construct a high-power high-reliability drive system for low-voltage applications. Therefore, a simplified VSD-SVM based DTC is designed for the T-NPC three-level asymmetric six-phase PMSM drives, which inherits good harmonic performance of SVM and fast dynamic performance of DTC. Furthermore, in the proposed scheme, the motor current controller is omitted and the DTC generates the voltage references for the SVM strategy with the torque and stator flux requirements. Based on that, a fault tolerant control scheme is proposed for open-phase faults in the drive with direct compensation of terminal voltages of electrical machine. Thus, no large disturbance will be induced in motor currents after the fault tolerant control is put into effect. The SVM strategy has clear definition and description of voltage vectors. By combing SVM with DTC, it is possible to synthesize the lost voltage vectors with remaining voltage vectors, in such a way that symmetric operation can be achieved for open-switch faults in the drive with the proposed fault tolerant control method of this paper.

The contents of this paper are listed as follows: The configuration of driving system and modeling of asymmetric six-phase PMSM are given in section II. Then, a two-step VSD-SVM based DTC scheme is developed in section III. In section IV, the fault tolerant control for open-phase fault is proposed based on voltage compensation. In section V, the modulation methods are redesigned for the faults in half-bridge switches and neutral-point-clamping switches. In section VI, experimental results are given to verify the performance of the proposed schemes. Finally, the conclusions are drawn in section VII.

II. Configuration and Modeling

Fig. 1 shows the configuration of the T-NPC inverter fed asymmetric six-phase PMSM drives. This system combines the advantages of T-NPC three-level topology and multiphase motor drives. The asymmetric six-phase PMSM drive in this paper has two sets of three-phase windings, which are spatially shifted 30 electric degrees with isolated neutrals.

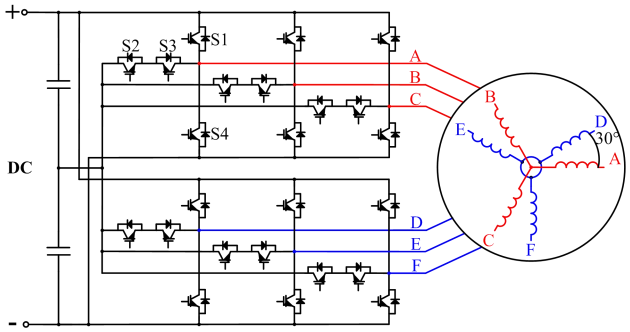


Fig. 1. Asymmetric six-phase PMSM drive.

The voltage and flux models are expressed as:

$$\begin{cases}\mathbf{u}_s=R_s\mathbf{i}_s+p\boldsymbol{\psi}_s\\ \boldsymbol{\psi}_s=\mathbf{L}_s\mathbf{i}_s+\psi_f\mathbf{F}(\theta)\end{cases} \tag{1}$$

where, $\mathbf{u}_s$ is stator voltage, $\mathbf{i}_s$ is stator current vector, $\boldsymbol{\psi}_s$ is stator flux vector, and ψ_f is the rotor flux vector. θ is the phase angle between the *d*-axis and phase A winding.
The distribution function $\mathbf{F}(\theta)$ is given as:

$$\mathbf{F}(\theta)=\Big[\cos(\theta),\cos(\theta-\frac{2\pi}{3}),\cos(\theta+\frac{2\pi}{3}),\cos(\theta-\frac{\pi}{6}),\cos(\theta-\frac{5\pi}{6}),\cos(\theta+\frac{\pi}{2})\Big]^T \tag{2}$$

The inductance matrix $\mathbf{L}_s$ can be expressed as :

$$\mathbf{L}_s=L_{ls}\mathbf{I}_6+L_{ms}\mathbf{A}+L_{mr}\mathbf{B} \tag{3}$$

where L_{ls} is leakage inductance, $\mathbf{I}_6$ is six dimensional identity matrix, L_{ms} is the stator main inductance, and L_{mr} is the magnetic reluctance inductance [34].

$$[\mathbf{A}]=\begin{bmatrix}1&-\frac{1}{2}&-\frac{1}{2}&\frac{\sqrt3}{2}&-\frac{\sqrt3}{2}&0\\ -\frac{1}{2}&1&-\frac{1}{2}&0&\frac{\sqrt3}{2}&-\frac{\sqrt3}{2}\\ -\frac{1}{2}&-\frac{1}{2}&1&-\frac{\sqrt3}{2}&0&\frac{\sqrt3}{2}\\ \frac{\sqrt3}{2}&0&-\frac{\sqrt3}{2}&1&-\frac{1}{2}&-\frac{1}{2}\\ -\frac{\sqrt3}{2}&\frac{\sqrt3}{2}&0&-\frac{1}{2}&1&-\frac{1}{2}\\ 0&-\frac{\sqrt3}{2}&\frac{\sqrt3}{2}&-\frac{1}{2}&-\frac{1}{2}&1\end{bmatrix} \tag{4}$$

$$[\mathbf{B}]=\begin{bmatrix}B_1&B_3&B_5&B_2&B_4&B_6\\ B_3&B_5&B_1&B_4&B_6&B_2\\ B_5&B_1&B_3&B_6&B_2&B_4\\ B_2&B_4&B_6&-B_5&-B_1&-B_3\\ B_4&B_6&B_2&-B_1&-B_3&-B_5\\ B_6&B_2&B_4&-B_3&-B_5&-B_1\end{bmatrix} \tag{5}$$

where, $B_1=\cos(2\theta)$, $B_2=\cos(2\theta-\frac{\pi}{6})$, $B_3=\cos(2\theta-\frac{2\pi}{3})$, $B_4=\cos(2\theta-\frac{5\pi}{6})$, $B_5=\cos(2\theta-\frac{4\pi}{3})$, $B_6=\cos(2\theta-\frac{3\pi}{2})$.

According to the vector space decomposition (VSD) approach [17], the voltage and current space vectors of the asymmetric six-phase motor can be decomposed into three two-dimensional orthogonal subspaces: α-β, x-y, and o_1-o_2. Eq. (6) presents the VSD matrix:

$$[\boldsymbol{T}_{VSD}]=\begin{bmatrix}\alpha\\ \beta\\ x\\ y\\ o_1\\ o_2\end{bmatrix}=\frac{1}{3}\begin{bmatrix}1&-\frac{1}{2}&-\frac{1}{2}&\frac{\sqrt3}{2}&-\frac{\sqrt3}{2}&0\\ 0&\frac{\sqrt3}{2}&-\frac{\sqrt3}{2}&\frac{1}{2}&\frac{1}{2}&-1\\ 1&-\frac{1}{2}&-\frac{1}{2}&-\frac{\sqrt3}{2}&\frac{\sqrt3}{2}&0\\ 0&-\frac{\sqrt3}{2}&\frac{\sqrt3}{2}&\frac{1}{2}&\frac{1}{2}&-1\\ 1&1&1&0&0&0\\ 0&0&0&1&1&1\end{bmatrix} \tag{6}$$

III. Proposed DTC Scheme Based on VSD-SVM

Fig. 2 shows the DTC scheme for the asymmetric six-phase PMSM drive based on VSD-SVM. The main work is to propose a simplified two-step VSD-SVM for asymmetric six-phase three-level inverter and incorporating an efficient harmonic current controller. With the feedback of voltage and current components in α-β subspace, the electromagnetic torque T_e and the stator flux ψ_s are estimated. Based on the stator flux error between the reference value and the estimated value, the voltage references are obtained [35]. Then, the amplitude and angle of the voltage reference, namely u_{ref} and φ_{ref} are provided for the two-step VSD-SVM, which in turn generates switching pulses by merging voltage perturbations from closed-loop harmonic current controller on x-y subspace.

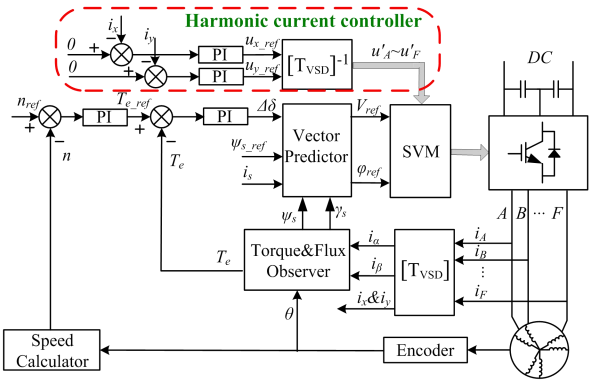


Fig. 2. Control diagram of DTC for asymmetric six-phase PMSM drive based on VSD-SVM.

A. Torque and flux estimation

The calculation of stator flux is shown in Fig. 3, which is developed based on current model. Compared to voltage model based stator flux observer, the current model based observer is constrained by voltage signals. When the open-circuit faults occur in inverters or the motor windings, the stator flux can still be calculated accurately with current model based stator flux observer. The torque can be estimated according to the following equations:

$$T_e = 3n_p(\psi_{s\alpha} i_{s\beta} - \psi_{s\beta} i_{s\alpha}) \tag{7}$$

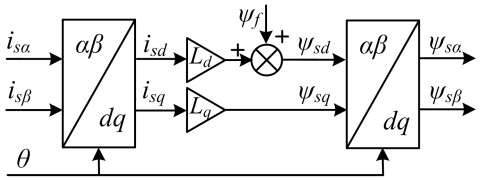


Fig. 3. Calculation of stator flux based on current model.

B. Voltage vector prediction

Fig. 4 shows the principle of stator flux control, where, γ_s is the stator flux angle and γ_r is the rotor flux angle. The error of stator flux vector $\Delta\boldsymbol{\psi}_s$ establishes the relationship between the stator flux vector reference $\boldsymbol{\psi}_{s\_ref}$ and the voltage vector reference $\mathbf{V}_{ref}$:

$$\Delta\boldsymbol{\psi}_s = \boldsymbol{\psi}_{s\_ref} - \boldsymbol{\psi}_s = \mathbf{V}_{ref} T_s \tag{8}$$

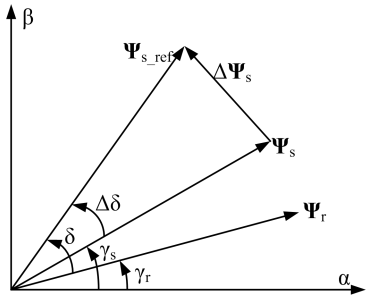


Fig. 4. Principle of stator flux control.

C. Simplified SVM

The output voltage of each T-NPC inverter leg could be $U_{dc}/2$, 0 and $-U_{dc}/2$, which are represented by 2, 1 and 0 respectively. So, the six-phase T-NPC three-level VSI can produce 729 (3^6) primitive voltage space vectors totally. Fig. 5 shows the voltage vectors on the *α-β* subspace and *x-y* subspace. It has been verified in [17] that it is the nonzero voltage vectors on *x-y* subspace that produces large current harmonics in multiple phase windings. Therefore, an effective way of reducing current harmonics is to maintain the average volt-seconds of voltage vectors on *x-y* subspace to be zero and make the average volt-seconds of the voltage vectors equal to the reference voltage on *α-β* subspace. Massive primitive vectors increase the control flexibility, and make the SVM scheme difficult to design. Therefore, a simplifying criterion has to be designed for selecting primitive vector candidates. Also, the voltage vector selection and synthesis should be optimized for harmonic components on *x-y* subspace. To optimize the voltage vector synthesis, the SVM scheme is designed into two steps. The first step is to utilize two primitive switching vectors to synthesize the new harmonic-free vectors by forcing the average volt-seconds of voltage vectors on *x-y* subspace to be zero. The second step is to use two synthesized harmonic-free vectors to compose the reference voltage vector. Dissembling the voltage vector synthesis process into two independent steps could reduce the complexity of the SVM scheme. The principles of selecting primitive voltage vectors are proposed as follows: 1) No level transition between 2 and 0 in a single switching period. 2) Maintain sufficient small voltage vectors for stabilizing the mid-point voltage in DC link. 3) Full utilization of DC link voltage. 4) Force average volt–seconds of voltage vectors on *x-y* subspace to be zero.

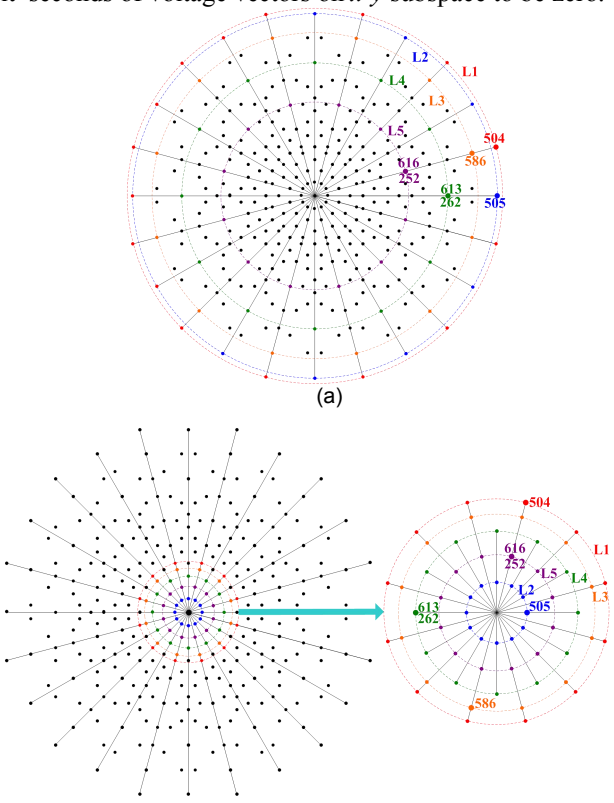


Fig. 5. Inverter voltage vectors: (a) *α-β* subspace; (b) *x-y* subspace.

TABLE II
AMPLITUDES OF SELECTED VECTORS

	α-β	*x-y*
L_1	$\frac{\sqrt{6}+\sqrt{2}}{6}U_{dc}$	$\frac{\sqrt{6}-\sqrt{2}}{6}U_{dc}$
L_2	$\frac{2+\sqrt{3}}{6}U_{dc}$	$\frac{2-\sqrt{3}}{6}U_{dc}$
L_3	$\frac{3\sqrt{2}+\sqrt{6}}{12}U_{dc}$	$\frac{3\sqrt{2}-\sqrt{6}}{12}U_{dc}$
L_4	$\frac{\sqrt{3}+1}{6}U_{dc}$	$\frac{\sqrt{3}-1}{6}U_{dc}$
L_5	$\frac{\sqrt{6}+\sqrt{2}}{12}U_{dc}$	$\frac{\sqrt{6}-\sqrt{2}}{12}U_{dc}$

As shown in Fig. 5(a) and Fig. 5(b), the 729 voltage vectors are mapped onto α-β subspace and x-y subspace for the three-level asymmetric six-phase PMSM drive, which are presented in decimal. For example, the vector 210201 in ternary can be denote as 586 in decimal. The colorful points are used to represent the selected ones, which can be classified into five groups according to their amplitudes on α-β subspace: L_1, L_2, L_3, L_4, and L_5. The amplitudes of five groups of primitive vectors are listed in Table II.

In the first step of voltage vector synthesis, the vectors with the same direction on α-β subspace of L_1 and L_3, the vectors of L_3 and L_5 and the vectors of L_2 and L_4 are selected to compose the three groups of new vectors, namely $L_{1\text{-}3}$, $L_{3\text{-}5}$, $L_{2\text{-}4}$, respectively. The synthesized vectors of the first step on α-β subspace is shown in Fig. 6. The constraint is to maintain the average volt-seconds of voltage vectors on x-y subspace to be zero. Thus, the distribution of dwelling time for selected vectors are calculated by forcing components in x-y subspace to be zero according to amplitudes of different layers in Table II. As shown in Table III, $P_{i\text{-}j(i)}$ and $P_{i\text{-}j(j)}$ are time weight coefficients of voltage vectors of L_i and L_j, which compose new vectors of group $L_{i\text{-}j}$. The sum of $P_{i\text{-}j(i)}$ and $P_{i\text{-}j(j)}$ is one. The amplitudes of three groups of newly synthesized harmonic-free vectors are listed in Table IV.

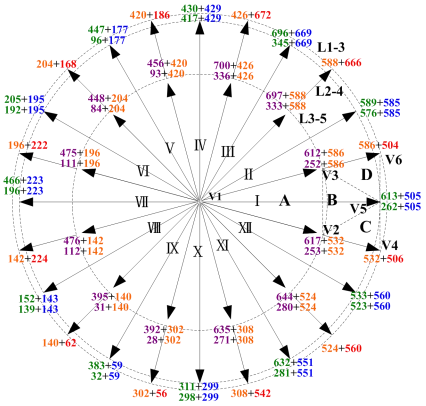


Fig. 6. Harmonic-free vectors on α-β subspace.

TABLE III
DISTRIBUTION OF DWELLING-TIME OF SELECTED VECTORS

	$L_{1\text{-}3}$	$L_{2\text{-}4}$	$L_{3\text{-}5}$
$P_{i\text{-}j(i)}$	$2\sqrt{3}-3$	$\frac{-1+\sqrt{3}}{2}$	$\sqrt{3}-1$
$P_{i\text{-}j(j)}$	$4-2\sqrt{3}$	$\frac{3-\sqrt{3}}{2}$	$2-\sqrt{3}$

TABLE IV
AMPLITUDES OF NEW SYNTHESIZED VECTORS

	$L_{1\text{-}3}$	$L_{2\text{-}4}$	$L_{3\text{-}5}$
α-β	$\frac{3\sqrt{2}-\sqrt{6}}{3}U_{dc}$	$\frac{\sqrt{3}}{3}U_{dc}$	$\frac{\sqrt{6}}{6}U_{dc}$
x-y	0	0	0

In the second step, the newly synthesized 36 vectors are divided into sectors from I to XII in Fig. 6, Each sector contains one zero vector $\mathbf{V}_1$ and five non-zero vectors $\mathbf{V}_2$-$\mathbf{V}_6$, which divide sector I into four sub-sectors, namely A, B, C and D. The reference voltage vector is synthesized by three nearest new vectors in the second step. For instance, when the reference voltage vector is located in sub-sector B, new vectors $\mathbf{V}_2$, $\mathbf{V}_3$ and $\mathbf{V}_5$ participate in the synthesis process. If the mid-point voltage of DC link is lower than $U_{dc}/2$, the voltage vectors used are 617 (211212), 523 (201201), 616 (211211), 586 (210201), 613 (211201) and 505 (200201). In order to limit the switching actions while promising good harmonic performance, it is necessary to rearrange the switching sequence based on the volt-second balancing principle [36]. The corresponding switching sequence of the case above is designed in Fig. 7. The lower voltage levels are placed at the starting and the end of PWM period to avoid level transition between 2 and 0.

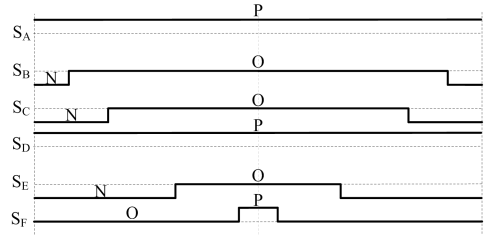


Fig. 7. Switching pattern.

D. Current harmonics suppression

Although the proposed SVM can limit the harmonics from inverter side, there may be possible current harmonics induced from harmonics in back-EMF and asymmetry in phase windings. In order to compensate the harmonic components, the scheme in this paper introduces a closed-loop controller for harmonic subspace, as shown in Fig. 2. The closed-loop harmonic controller generates the voltage reference u_{x_ref} and u_{y_ref} on x-y subspace. With the inverse transform of VSD matrix, the voltage reference are converted into six-phase voltage compensation values, namely u'_A~u'_F. These six-phase compensation voltages are converted linearly into perturbation of switching action instants of each phase, and the final switching pulses are generated.

IV. FAULT TOLERANT SCHEME FOR OPEN-PHASE FAULT

The idea of the proposed fault tolerant control is to derive the voltage difference between terminal voltage of the faulty phase under normal condition and back-EMF of the faulty phase under open-circuit fault. Then, the voltage difference will be compensated purposely by other healthy phases. As shown in Fig. 8, phase F is in open-circuit fault. The terminal voltage of phase F under normal condition is u_F, and the total back-EMF of the whole faulty winding is u_{EMF}. Thus, the voltage different Δu_F will be derived with the following analysis. This voltage difference will be compensated by the remaining healthy phases.

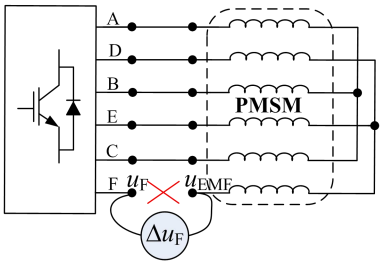


Fig. 8. The diagram of open-circuit fault in phase F.

Since the phase voltages of the asymmetric six-phase PMSM comply the symmetric restraints, the phase voltages can be expressed by phase-to-phase voltages as following:

$$\begin{bmatrix} u_A \\ u_B \\ u_C \\ u_D \\ u_E \\ u_F \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & 1 & 1 & 0 & 0 & 0 \\ -1 & 1 & 1 & 0 & 0 & 0 \\ -1 & -2 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & 1 & 1 \\ 0 & 0 & 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & -1 & -2 & 1 \end{bmatrix}\begin{bmatrix} u_{AB} \\ u_{BC} \\ 0 \\ u_{DE} \\ u_{EF} \\ 0 \end{bmatrix} \tag{9}$$

The voltage on α-β and x-y subspaces can be expressed by the line voltages and faulty phase voltage based on Eq. (9) and VSD matrix in Eq. (6).

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_x \\ u_y \end{bmatrix} = \frac{1}{6}\begin{bmatrix} 2u_{AB} + u_{BC} + \sqrt{3}u_{DE} \\ \sqrt{3}u_{BC} - 3u_F \\ 2u_{AB} + u_{BC} - \sqrt{3}u_{DE} \\ -\sqrt{3}u_{BC} - 3u_F \end{bmatrix} \tag{10}$$

When the open-circuit fault occurs in phase F, the phase-to-phase voltages u_{AB}, u_{BC} and u_{DE} are not changed. It is mentioned that only the phase voltage u_F will change after the fault, and the value is changed from the terminal voltage under normal condition to the total induced back-EMF of phase F. Both u_β and u_y will be affected by the change of u_F. So, the key is to derive the voltage difference Δu_F. The expression of phase voltage u_F is given as:

$$u_F = -u_D - u_E = -R_s(i_D + i_E) - \frac{d}{dt}(\psi_D + \psi_E) \tag{11}$$

Therefore, $\frac{d}{dt}(\psi_D + \psi_E)$ is to be calculated at first. According to Eq. (1), the following relationship is obtained:

$$\begin{aligned} \psi_D + \psi_E &= L_{ls}(i_D + i_E) + L_{ms}(\frac{\sqrt{3}}{2}i_B - \frac{\sqrt{3}}{2}i_C + \frac{1}{2}i_D + \frac{1}{2}i_E - i_F) \\ &+[\cos(\theta - \frac{\pi}{6}) + \cos(\theta - \frac{5\pi}{6})]\psi_f + (\psi_{mrD} + \psi_{mrE}) \end{aligned} \tag{12}$$

$$\begin{aligned} \psi_B - \psi_C &= L_{ls}(i_B - i_C) + \frac{3}{2}L_{ms}(i_B - i_C) \\ &+[\cos(\theta - \frac{2\pi}{3}) - \cos(\theta + \frac{2\pi}{3})]\psi_f + (\psi_{mrB} - \psi_{mrC}) \end{aligned} \tag{13}$$

where the ψ_{mrB}, ψ_{mrC}, ψ_{mrD}, ψ_{mrE} are the magnetic reluctance flux of phase B, C, D, E. They can be derived from $\boldsymbol{\psi}_{mr} = L_{mr}[\mathbf{B}]\mathbf{i}_s = [\psi_{mrA}, \psi_{mrB}, \psi_{mrC}, \psi_{mrD}, \psi_{mrE}, \psi_{mrF}]^T$

By considering the current restraints $i_A + i_B + i_C = 0$, $i_D + i_E = 0$ and $i_F = 0$, Eq. (12) becomes:

$$\begin{aligned} \psi_D + \psi_E &= \frac{\sqrt{3}}{2}L_{ms}(i_B - i_C) \\ &+[\cos(\theta - \frac{\pi}{6}) + \cos(\theta - \frac{5\pi}{6})]\psi_f + (\psi_{mrD} + \psi_{mrE}) \end{aligned} \tag{14}$$

Thus, Eq. (13) and Eq. (14) are transformed as:

$$\begin{aligned} &\frac{3}{2}L_{ms}(i_B - i_C) = (\psi_B - \psi_C) - L_{ls}(i_B - i_C) \\ &-\left\{[\cos(\theta - \frac{2\pi}{3}) - \cos(\theta + \frac{2\pi}{3})]\psi_f + (\psi_{mrB} - \psi_{mrC})\right\} \end{aligned} \tag{15}$$

$$\begin{aligned} &\frac{\sqrt{3}}{2}L_{ms}(i_B - i_C) = \psi_D + \psi_E \\ &-\left\{[\cos(\theta - \frac{\pi}{6}) + \cos(\theta - \frac{5\pi}{6})]\psi_f + (\psi_{mrD} + \psi_{mrE})\right\} \end{aligned} \tag{16}$$

By equaling the right terms of Eq. (15) and Eq. (16), the following equation is obtained:

$$\begin{aligned} \psi_D + \psi_E &= \frac{\sqrt{3}}{3}[(\psi_B - \psi_C) - L_{ls}(i_B - i_C)] \\ &+[\cos(\theta - \frac{\pi}{6}) + \cos(\theta - \frac{5\pi}{6}) - \frac{\sqrt{3}}{3}\cos(\theta - \frac{2\pi}{3}) \\ &+\frac{\sqrt{3}}{3}\cos(\theta + \frac{2\pi}{3})]\psi_f + [(\psi_{mrD} + \psi_{mrE}) - \frac{\sqrt{3}}{3}(\psi_{mrB} - \psi_{mrC})] \end{aligned} \tag{17}$$

Since the terms in the second line and the third line are zero on the right side in the equation above, Eq. (17) becomes:

$$\psi_D + \psi_E = \frac{\sqrt{3}}{3}[(\psi_B - \psi_C) - L_{ls}(i_B - i_C)] \tag{18}$$

By taking Eq. (18) into Eq. (11), the faulty phase voltage is obtained as:

$$\begin{aligned} u_{F\_fault} &= -R_s(i_D + i_E) - \frac{\sqrt{3}}{3}[\frac{d}{dt}(\psi_B - \psi_C) - L_{ls}\frac{d}{dt}(i_B - i_C)] \\ &= -\frac{\sqrt{3}}{3}[u_{BC} - R_s(i_B - i_C) - L_{ls}\frac{d}{dt}(i_B - i_C)] \end{aligned} \tag{19}$$

According to Eq. (10), in normal state, $u_{F\_normal} = -\frac{\sqrt{3}}{3}u_{BC}$ by controlling the y-axis voltage to be zero, namely $u_y = 0$. By comparing with Eq. (19), the change in u_F is:

$$\Delta u_F = -\frac{\sqrt{3}}{3}[R_s(i_B - i_C) + L_{ls}\frac{d}{dt}(i_B - i_C)] \tag{20}$$

Based on Eqs. (10) and (20), the change of stator voltages on α-β subspace are adjusted after fault:

$$\begin{cases} \Delta u_\alpha = 0 \\ \Delta u_\beta = \frac{\sqrt{3}}{6}[R_s(i_B - i_C) + L_{ls}\frac{d}{dt}(i_B - i_C)] \end{cases} \tag{21}$$

In order to achieve the same voltage vectors effect under faulty operation, the reference voltage u_{α_ref} needs not to be changed and u_{β_ref} should be added by Δu_β. But the control structure and the switching strategy of the SVM-DTC before fault are unchanged with the proposed fault tolerant control.

It should be noted that the harmonic subspace is also changed after occurrence of open-circuit faults. The single-phase open-circuit fault reduces control dimensions from six to five. Therefore, the harmonic vector can be derived by constructing new five-dimension orthogonal vector matrix. By removing phase F from Eq. (6), the following vector matrix related to α-β subspace and o_1-o_2 subspace is obtained:

$$\begin{bmatrix}\alpha\\ \beta\\ o_1\\ o_2\end{bmatrix}=\frac{1}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 & 0\\ 1 & 1 & 1 & 0 & 0\\ 0 & 0 & 0 & 1 & 1\end{bmatrix} \tag{22}$$

It can be calculated that the four vectors corresponding to α-β subspace and o_1-o_2 subspace are orthogonal to each other. The remaining one-dimension harmonic vector, namely z should be orthogonal to the aforementioned four vectors, which is derived as:

$$[z]=\frac{1}{3}\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2}\end{bmatrix} \tag{23}$$

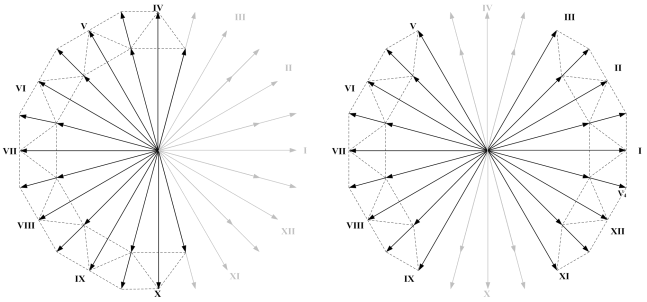
Therefore, the final VSD matrix with open-circuit fault in phase F is obtained, In the fault tolerant scheme, the matrix in Fig. 2 need be modified. By taking Eq. (5) into new five-dimension orthogonal vector matrix, the harmonic voltage u_z is deduced as:

$$u_z=\frac{1}{6}(2u_{AB}+u_{BC}-\sqrt{3}u_{DE}) \tag{24}$$

Comparing Eq. (6) and Eq. (24), it is found that the voltage components u_x and u_z share the same expression under open-circuit fault in phase F. For simplicity, the harmonic dimension is still expressed by x while the component of y dimension is meaningless and ignored under open-phase fault in this paper. The proposed fault tolerant scheme for open-phase fault can be applied in any phase with Eq. (9) to Eq. (24). Different voltage compensation values on α-β subspace and the corresponding one-dimension harmonic vector can be derived for different faulty phases. In case of open-circuit faults in two phases, the voltage of faulty phases can still be compensated by other healthy phases.

V. Fault Tolerant Scheme for Switch Fault

The proposed fault tolerant control scheme for open-switch faults can be divided into two cases: the open-circuit fault occurring in half-bridge switches S_{A1}/S_{A4} and the open-circuit fault in mid-point switches S_{A2}/S_{A3}. The corresponding voltage vector diagrams are shown in Fig. 9.

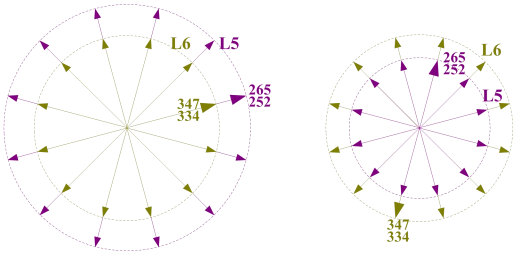


(a) (b)

Fig. 9. Remaining voltage vectors: (a)S_{A1} fault (b)S_{A2}/S_{A3} fault

A. Open-circuit fault in half-bridge switches S_{A1}/S_{A4}

When switch S_{A1} fails in open-circuit fault, the voltage level 2 of faulty leg A is lost. The remaining voltage vectors designed in section III are shown in Fig. 9(a), where the gray parts represent lost vectors. The vectors in the right half of the space vector diagram are almost all lost. Since the lost vectors can not be replaced or synthesized by remaining vectors, the new space vector diagram under faulty conditions are required. The six-phase voltage vector can be regarded as the combination of two three-phase voltage vectors. For instance, the six-phase vector 221211 in ternary is the combination of small vector 221 of phase ABC and small vector 211 of phase DEF. Based on the same principles of selecting vectors, the vectors are selected from remaining primitive vectors, as shown in Fig. 10.



(a) (b)

Fig. 10. Selected voltage vectors: (a) α-β subspace; (b) x-y subspace.

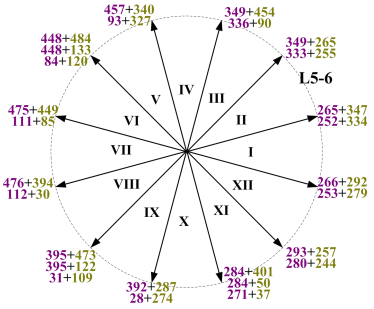


Fig. 11. Harmonic-free vectors on α-β subspace.

As Fig. 10 shows, the vectors of group L_5 and group L_6 with the same directions on α-β subspace are with opposite directions on x-y subspace. The proposed fault tolerant control scheme also adopts the two-step vector synthesis approach mentioned above. In the first step, the vectors with the same direction on α-β subspace of L_5 and L_6 are selected to compose the new group of harmonic-free vectors $L_{5\text{-}6}$, as shown in Fig. 11. Twelve sectors are divided based on new synthesized vectors. The amplitudes of selected primitive vectors and newly synthesized vectors are shown in Table V.

TABLE V
Amplitudes of Vectors

	L_5	L_6	$L_{5\text{-}6}$
α-β	$\frac{\sqrt{6}+\sqrt{2}}{12}U_{dc}$	$\frac{\sqrt{2}}{6}U_{dc}$	$\frac{3\sqrt{2}-\sqrt{6}}{6}U_{dc}$
x-y	$\frac{\sqrt{2}}{6}U_{dc}$	$\frac{\sqrt{6}-\sqrt{2}}{12}U_{dc}$	0

The second step is to select two harmonic-free vectors to compose the reference voltage vector based on the sector and DC link mid-point voltage. Since some positive small vectors are lost, the redundant negative small vectors have to be used to synthesize the voltage reference. But the performance becomes worse in balancing DC link mid-point voltage. For instance, if the reference voltage is located in sector V and the mid-point voltage of DC link is lower than $U_{dc}/2$, primitive vectors 457 (121221), 340 (110121), 448 (121121) and 133(011221)

participate in the synthesis process, as shown in Fig. 11. In the second primary vector 110121, the redundant negative small vector 110 has to be used to replace the lost positive small vector 221 due to fault of S_{A1}. Then, in the fourth primary vector 011221, the three-phase vector 011 is used instead of 122, in such a way that the voltage level transition between 2 and 0 is avoided in phase C within a single switching period.

B. Open-circuit fault in mid-point switches S_{A2}/S_{A3}

When switch S_{A2}/S_{A3} fails, the voltage level 1 of phase A is lost. The remaining voltage vectors are shown in Fig. 9(b). where the gray parts represent the lost vectors. It is found that the vectors on sectors IV and X are all impossible. The uneven distribution of remaining primitive vectors makes it difficult to redesign voltage vector diagram and modulation strategy. Different from selecting the primary vector within the remaining voltage vectors, a fault tolerant control scheme is proposed only for faulty phase in this paper. According to the volt-second balance principle, the dwelling time of lost level 1 in faulty phase is distributed to level 1 and level 0 equally. The lost vector 1XXXXX is actually synthesized by 2XXXXX and 0XXXXX. For instance, the lost vector 120210 is synthesized by vectors 220210 and 020210. By using this fault tolerant control, the system can restore the performance under normal state. But there will be slight increase of harmonics due to the voltage transition between 2 and 0 of the fault phase voltage in one switching period.

VI. Experimental Verification

The experiments are carried out on a laboratory prototype of T-NPC three-level VSI fed asymmetric six-phase PMSM drive to verify the effectiveness of the proposed fault tolerant control scheme. Fig. 12(a) and (b) show the block diagram and photograph of the experimental setup. In the experiments, the DSP (TMS-F28335) performs the control algorithm and generates the 12-channel PWM signals, which are transported into 24-channel complementary PWM signals by digital dead-time generator. The power inverters are built with six T-NPC modules (F3L75R12W1H3_B27) to supply the asymmetric six-phase PMSM machine. A PM generator is coupled to the PMSM machine to work as an electric load. The key parameters of the experimental setup are shown in Table VI. Throughout the experiment, the motor speed, stator currents and DC link voltages are measured by means of sensors. The other variables are derived indirectly based on estimators, which are shown on oscilloscope through DA converters in DSP. In the fault tolerant experiments, the open-switch faults and open-phase faults are emulated by disabling drive signals of specific IGBT and the total phase leg, respectively.

Fig. 13 plots the measured steady-state performance of the proposed DTC scheme based on two-step SVM with 1000-rpm speed and 10-Nm load under normal operation. Fig. 13(a) shows the five-level inverter output voltage waveform of the phase-to-phase voltage. Fig. 13(b) and Fig. 13(c) show the phase current waveforms. By using the two-step SVM and the additional harmonic current controller, the low order harmonics are suppressed effectively as shown in Fig. 13(d). Fig. 13(e) verifies the steady stator flux trajectory is maintained during the operation. Fig. 13(f) shows the mid-point DC link voltage is controlled well.

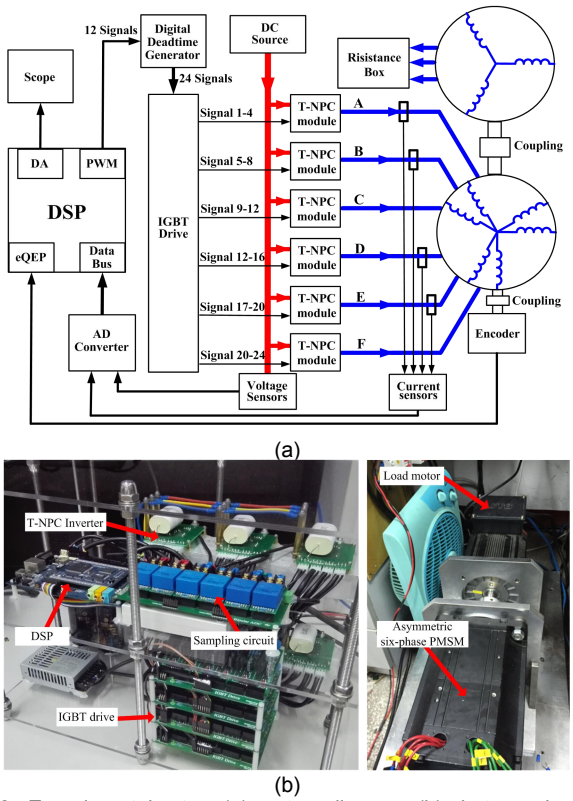


Fig.12. Experimental setup: (a) system diagram; (b) photograph.

TABLE VI
Key Parameters of Experimental Setup

Name	*Value*
Pole pair number	3
q-axis inductance	6.21 mH
d-axis inductance	6.21 mH
PM flux (amplitude)	0.2 Wb
Stator resistance	0.21 Ω
Upper and lower DC link capacitors	1000 uF
Speed reference	1000 rpm
Rated load	10 Nm
Sampling frequency	5 kHz

The dynamic performance of the proposed DTC scheme under normal operation is measured as shown in Fig. 14. The given speed reference switches between 500-rpm and 1000-rpm. The torque reference amplitude is confined between –15-Nm and 20-Nm to ensure the motor work within maximum output torque. It can be observed in Fig. 14(a) that both the torque and the speed can track their reference values accurately and quickly. It verifies the control scheme maintains the fast torque response of DTC. In addition, the stator flux, and harmonic currents on *x*-*y* subspace and the mid-point DC link voltage are controlled well during the dynamic process.

Fig. 15 shows the performance of standard control under open-circuit fault in phase F, where the fault tolerant control is not used. When the fault occurs, large torque ripple appears. The current of phase F is forced zero and other phase currents exhibit sinusoidal waveforms with different amplitudes, as shown in Fig. 15(a) and Fig. 15(b). Due to the change of voltage in β-axis, the corresponding current component becomes abnormal, which results in obvious torque fluctuation.

Furthermore, the copper loss increases with the amplitudes of phase currents. It is observed in Fig. 15(c) that the *y*-axis fundamental current exhibits a sinusoidal waveform, which is caused by the asymmetric phase currents and do not produce harmonic component. The harmonic current component on x subspace can still be controlled almost to be zero as expected, and the harmonic loss does not increase. In addition, the DC link mid-point voltage in Fig. 15(d) remains balanced. Good fault-tolerant performance of proposed two-step SVM based DTC is verified in suppressing harmonic currents and DC link mid-point voltage fluctuation.

Fig. 16. shows the measured performance of the proposed fault tolerant control in section IV under open-circuit fault in phase F. As shown in Fig. 16(a), a small reference voltage difference Δu_β is added to original voltage reference u_{β_ref}, and thus the structure of original DTC is kept for use under faulty condition. Fig. 16(b) and Fig. 16(c) verify that the torque is controlled much smoother with the addition of Δu_β. Fig. 16(d)–(f) verify that the current components on *x*-*y* subspace, the stator fluxes and the DC link mid-point voltage are controlled well with the proposed fault tolerant scheme. In Fig. 17, the dynamic performance of open-circuit fault in phase F is compared between post-fault operation and fault tolerant operation. The torque reference is switched from 5 Nm to 10-Nm. As shown in Fig. 17(a), obvious torque fluctuation appears when the given torque increases under post-fault state. Fig. 17(b) shows that the proposed fault-tolerant scheme can diminish the torque fluctuation under difference load torques effectively. The fast torque response and smooth switching process are retained with the proposed fault tolerant control.

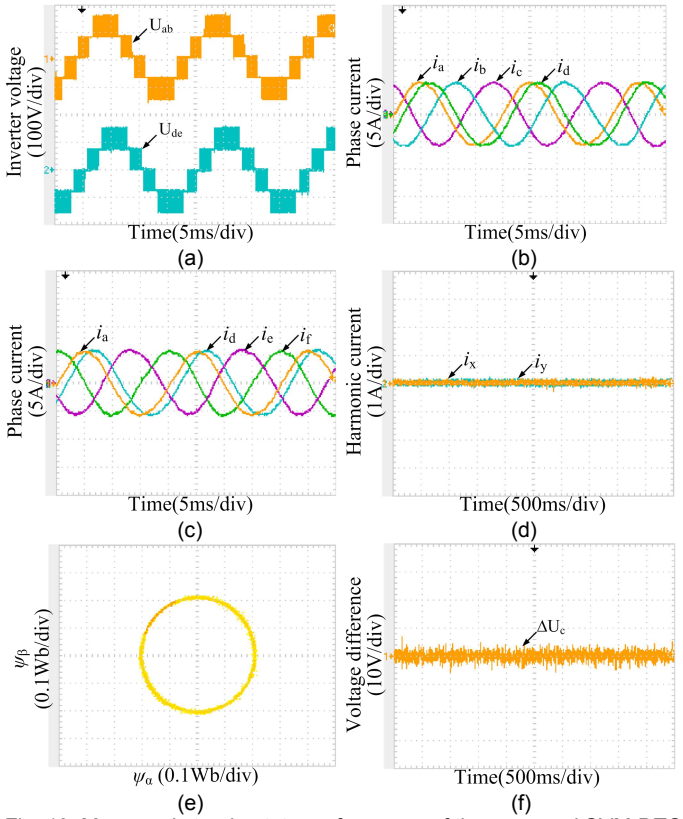


Fig. 13. Measured steady-state performance of the proposed SVM-DTC: (a) inverter voltages; (b) phase currents (abcd); (c) phase currents (adef); (d) current components on *x*-*y* subspace; (e) stator flux trajectory; (f) DC link voltages difference.

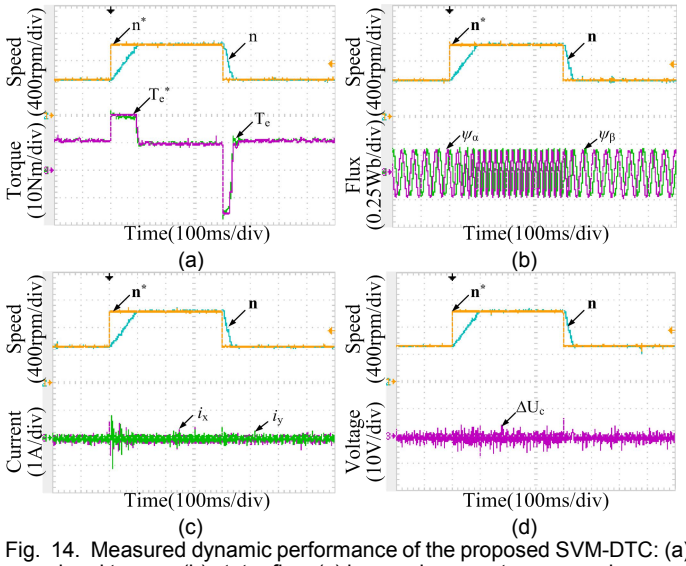


Fig. 14. Measured dynamic performance of the proposed SVM-DTC: (a) speed and torque; (b) stator flux; (c) harmonic currents on *x*-*y* subspace; (d) DC link voltages difference.

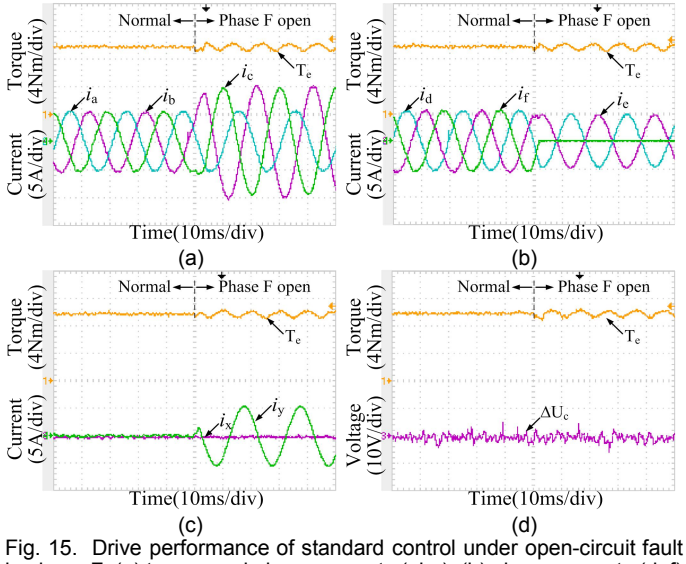
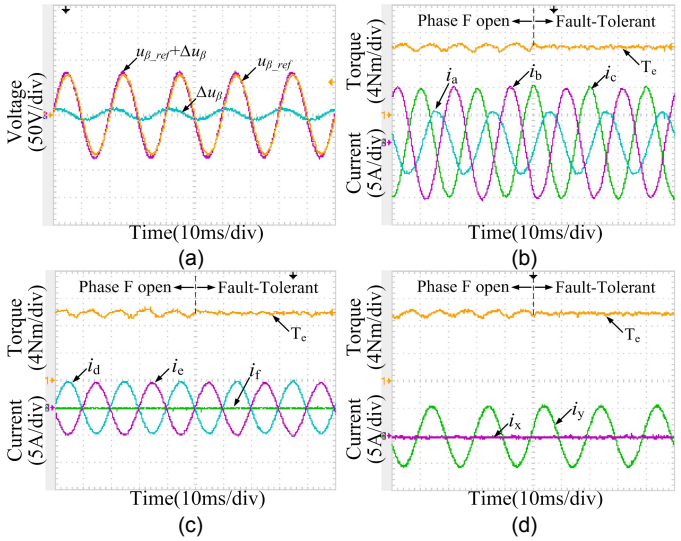


Fig. 15. Drive performance of standard control under open-circuit fault in phase F: (a) torque and phase currents (abc); (b) phase currents (def); (c) current components on *x*-*y* subspace; (d) DC link voltages difference.



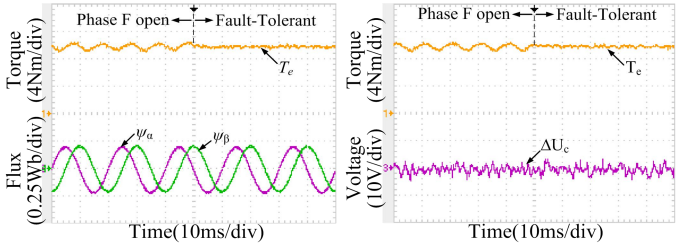


Fig. 16. Drive performance of proposed fault tolerant control under open-circuit fault in phase F: (a) β-axis reference voltage; (b) torque and phase currents (abc); (c) phase currents (def); (d) current components on *x-y* subspace; (e) stator flux; (f) DC link voltages difference.

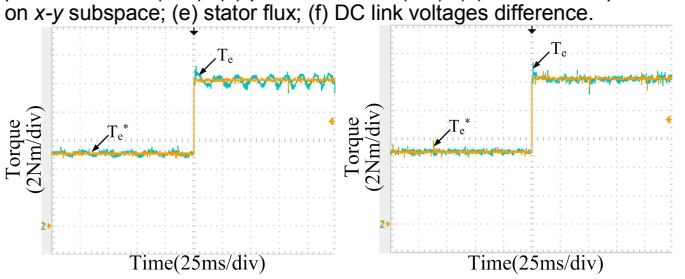


Fig. 17. Measured dynamic performance under open-circuit fault in phase F: (a) post-fault operation; (b) fault tolerant operation.

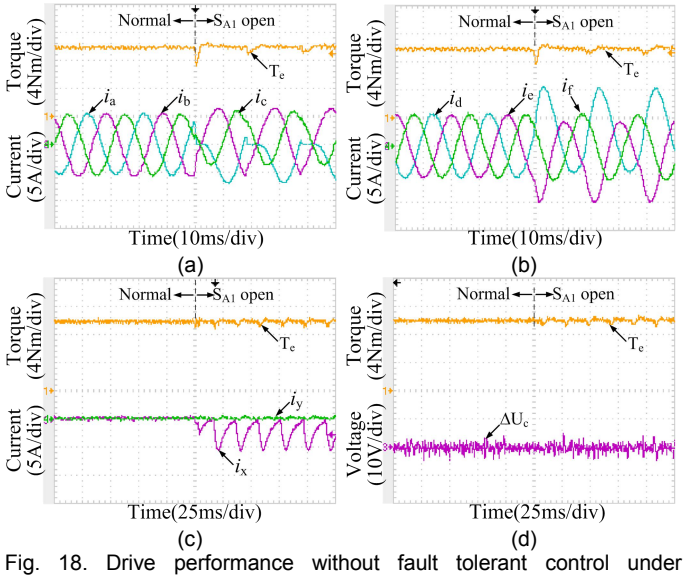


Fig. 18. Drive performance without fault tolerant control under open-circuit fault in S_{A1}: (a) torque and phase currents (abc); (b) phase currents (def); (c) harmonic currents; (d) DC link voltages difference.

Fig. 18 presents the drive performance without fault tolerant control when open-circuit fault occurs in S_{A1} under 1000-rpm speed and 10-Nm load. After fault, the obvious torque ripple appears. The phase-A current is distorted seriously, and the other phase currents also suffer from distortions, as shown in Fig. 18(a) and Fig. 18(b). In addition, the amplitudes of several phase currents have been increased intensively. Fig. 18(c) shows the large harmonic components on x-y subspace. Fig. 19(d) shows that the mid-point voltage in DC link can be balanced well even without specific fault tolerant operation under faulty condition.

Fig. 19 shows the performance of the proposed fault tolerant control scheme of S_{A1} open-switch fault under 10-Nm load. Since the modulation index is reduced in the proposed scheme, the motor speed is decreased to 500-rpm. After the use of fault tolerant control, the torque ripple is eliminated, and the phase currents are almost restored to the normal state, as shown in Fig. 19(a) and (b). The harmonic currents are mitigated in Fig. 19(c). It should be noted that the mid-point voltage has slight deviation in every half fundamental period. The reason is due to that the lost favorable small vectors for stabilizing DC capacitor voltages have to be replaced by undesired ones in the right half of space vector diagram. On the other hand, the mid-point voltage fluctuation is smaller even without using fault tolerant control in Fig. 19(d). The reason lies in that the lost small vector could be forced to another small vector, which still benefit balancing mid-point voltage fluctuations. For example, the original action of the lost vector 221211 will be taken by the vector 121211.

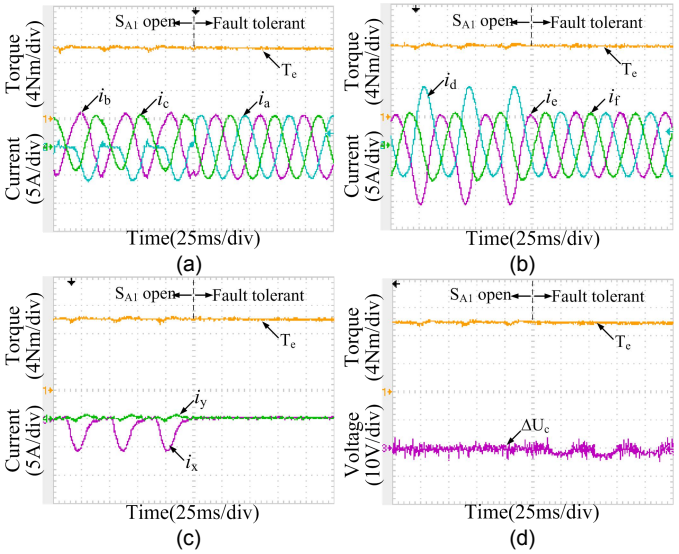


Fig. 19. Drive performance with proposed fault tolerant control under open-circuit fault in S_{A1}: (a) torque and phase currents (abc); (b) phase currents (def); (c) harmonic currents; (d) DC link voltages difference.

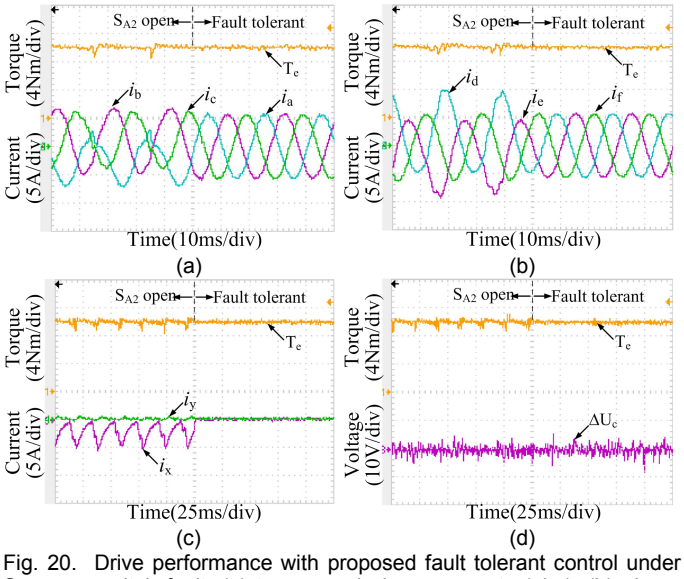


Fig. 20. Drive performance with proposed fault tolerant control under S_{A2} open-switch fault: (a) torque and phase currents (abc); (b) phase currents (def); (c) harmonic currents; (d) DC link voltages difference.

Fig. 20 shows the performance of the proposed fault tolerant control scheme for open-circuit fault in SA2 under 1000-rpm speed and 10-Nm load. Sinusoidal and symmetric phase currents can be provided with the fault tolerant control scheme, which are shown Fig. 20(a) and 20(b).The harmonic currents are suppressed effectively in Fig. 20(c). Also, the mid-point voltage in DC link is balanced well with the fault tolerant scheme in Fig. 20(d).

VII. CONCLUSIONS

In this paper, novel DTC based fault tolerant control schemes are proposed for both the phase winding and the inverter faults in T-NPC three-level asymmetric six-phase PMSM drives. The proposed fault tolerant schemes can provide smooth torque while good harmonic performance for open-phase faults without changing the control structure of DTC. The key is to derive the relationship between the stator fluxes and the stator voltages of all phases after the fault. By this way, a voltage perturbation is deduced and added to the voltage references. The control system of DTC is kept same as that before fault. In addition, a complete tolerant scheme is proposed for open-switch faults of the six-phase T-NPC inverter. Both the faults in half-bridge switches and those in mid-point switches are considered. The experimental results are given to verify the proposed fault tolerant schemes provide good operating performance under fault tolerant conditions.

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