Hafnium Oxide Based Gate Stacks on Germanium and Silicon

Thesis submitted in accordance with the requirements of the University of Liverpool for the degree of Doctor in Philosophy by Sean Mather

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Abstract

Up until 2007 the heart of the metal -oxide-semiconductor-field-effect-transistor (MOSFET) in computer processors was based on the Si-SiO_2-poly Si system. This changed when Intel announced the fabrication of the high-k metal gate MOSFET. This was required because the SiO_2 layer had become too thin so that quantum mechanical tunnelling meant that the leakage current through the device was unacceptably high. As the high quality SiO_2 layer was the main reason for silicon it is now possible for a semiconductor with better electrical properties to be used. The International Technology Roadmap for Semiconductors (ITRS) states that this is due to happen in 2018. Germanium is one of the contending materials due to high carrier mobilities (2x electron and 4x hole enhancement over silicon).

This thesis studies the development of high-k dielectrics deposited by atomic layer deposition (ALD), specifically the dielectric constant enhancement of HfO_2 with the addition of titanium. Different preparation methods were then deployed to create Hafnium based gate stacks on germanium. These methodologies are divided into 4 sections. Firstly, to grow a germanium oxide layer by oxygen plasma with the subsequent deposition of high-k on top. Then Molecular Beam Epitaxy (MBE) of an ultra-thin aluminium layer to create an ultra-thin gate stack with high-k deposited on top to reduce the leakage current through the devices. Then ALD of a thin Al_2O_3 layer with high-k on top

and finishes with sulphur passivation of the Ge interface with high-k on top. These material systems were characterised by both physical (ellipsometry, X-ray diffraction, X-ray photoelectron spectroscopy, Transmission electron microscopy) and electrical (Capacitance-voltage, Current-voltage) means. The dielectric constant of HfO_2 was found to increase from 17 to 35 for the $Ti_{0.5}Hf_{0.5}O_2$ system. This then reduced upon annealing to 27 with a 30 minute N_2 anneal at 500^{o}C and 22 with a 30s spike anneal at 850^{o}C.Growing a germanium oxide layer by oxygen plasma gave reasonable C-V characteristics but the thickness of the layer at 3nm was too large to make it suitable for extremely scaled devices

By giving the germanium a thermal clean in the MBE chamber and depositing an ultra-thin Aluminium layer which was subsequently oxidised a structure with an equivalent oxide thickness of 1.3nm were achieved with low leakage currents of $2x10^{-4}Acm^{-2}$ and low hysteresis of 10mV. The leakage current dropped to $3x10^{-7}Acm^{-2}$ for a sample with an EOT of 1.5nm. The equivalent oxide thickness (EOT) was found to be related to the temperature of the thermal preclean with higher temperatures giving lower EOT's due to a more efficient removal of the native oxide. EOT was also found to reduce for samples after a forming gas anneal which is attributed to densification of the layers and a reduction of the GeO_x interfacial layer.

ALD of a thin Al_2O_3 layer and subsequent plasma ALD of HfO_2 showed that significant regrowth of GeO_x occurs even when 2nm thick Al_2O_3 barrier is

employed. The electrical data is similar to samples without the Al_2O_3 layer which could be due to it not being thick enough to suppress an unwanted interfacial layer forming.

Sulphur passivation gave very good C-V data when Al_2O_3 is used as a dielectric and conduction band offsets were calculated as being 3.3eV for S-passivated samples and 3.61eV without S-passivation. Both of these are well over the 1eV set out by the ITRS to reduce carrier injection from the channel through the device. Device performance was found to be not as good when HfO_2 was used as the dielectric as there is significant regrowth of the GeO_x interfacial layer.

These studies show that there are a number of possible routes available for forming a gate stack on germanium and the control of the interface is the critical performance factor that needs to be controlled.

List of Publications

- **Mather. S**, Sedghi. N, Althobaiti. M, Mitrovic. I. Z, Dhanak. V.R, Chalker. P.R, Hall. S, *"Low EOT GeO_2/Al_2O_3/ HfO_2 on Ge substrate using ultrathin Al deposition*", (2013) Microelectronic Engineering, 109, pp. 126-128

- Werner. M, King. P.J, Hindley. S, Romani. S, **Mather. S**, Chalker. P.R, Williams. P.A, Van Den Berg. J.A, "*Atomic layer deposition of Ti- HfO_2 dielectrics*", (2013) Journal of Vacuum Science and Technology A: Vacuum, Surfaces and films, 31 (1), art. no. 01A102

- Mitrovic. I. Z, Althobaiti. M, Weerakkody. A.D, Sedghi. N, Hall. S, Dhanak. V.R, **Mather. S**, Chalker. P.R, Tsoutsou. D, Dimoulas. A, Henkel. C, Litta. E.D, Hellstrom. P.E, Ostling. M, "*Interface engineering routes for a future CMOS Ge-based technology*" (2014) ECS Transactions, 61 (2), pp. 73-88

- Althobaiti. M, **Mather. S**, Sedghi. N, Dhanak. V.R, Mitrovic. I. Z, Hall. S, Chalker. P.R, "*Hafnia and alumina on sulphur passivated germanium*", (2014) Vacuum, Article in Press, DOI: 10.1016/j.vacuum.2015.03.017

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Acronyms

Symbol	Name	Units
ε_0	Permittivity of free space	Fm^{-1}
Φ	Work function	eV
ALD	Atomic layer deposition	
CVD	Chemical vapour deposition	
CET	Capacitance equivalent thickness	nm
D_{it}	Density of interface states	
EOT	Equivalent oxide thickness	nm
E_f	Fermi level	
E_i	Intrinsic Fermi level	
E_c	Conduction band	
E_v	Valance band	
K	Dielectric constant	
Q	Charge on an electron	C
μ	Mobility	$cm^2V^{-1}s^{-1}$
MBE	Molecular beam epitaxy	
TEM	Transmission electron microscopy	
XPS	X-ray photoelectron spectroscopy	
XRD	X-ray diffraction	

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1. Introduction

1.1 Outline of Thesis

Chapter 1 outlines the technological context for the research presented. This includes MOSFET operation and MOS physics, the rationale for the inclusion of high k dielectrics and high mobility channels and a literature review. Chapter 2 outlines the experimental techniques employed in the fabrication and characterisation of the gate stacks. Chapter 3 presents research into the deposition of high k dielectrics on silicon by ALD. This includes Al_2O_3, HfO_2 and Ti-doped HfO_2. Chapter 4 presents work on germanium with oxygen plasma grown GeO_x layer with an ALD grown HfO_2 cap. Chapter 5 presents work where an ultrathin MBE deposited layer of Al (oxidised to Al_2O_3) with the subsequent deposition of high k by ALD to scale the EOT of MOS devices down. Chapter 6 has similar device structures as chapter 5 but this time with the Al_2O_3 layer deposited by ALD. Chapter 7 presents work where the surface of germanium is passivated by sulphur deposition (via a $(NH_4)_2S$ dip) with high k deposited by ALD on top. Chapter 8 has the conclusion and prospects for future work.

1.2 Technological Context

1.2.1 MOSFET origins and evolution

The metal-oxide-semiconductor-field-effect-transistor (MOSFET) is one of the most important inventions there has ever been. It has enabled the modern computer age which has meant advances in all realms of science and technology. The first transistor (which was a point contact transistor) was made from germanium at Bell laboratories by Shockley, Bardeen and Brattain in 1947 [1]. It was not until a decade later that an integrated circuit (IC), also on germanium, was developed by Kilby at Texas Instruments with silicon IC's following soon after. These early ICs were based on junction transistors and these presented many problems with the junction surfaces which caused significant reliability issues. In 1958 Attala of Bell Laboratories presented work [2] on thermally oxidised silicon and suggested the MOSFET device to make use of this work. Figure 1 shows a schematic of a pMOSFET device.

A semiconductor has the important property that the conductivity of the material can be modified by the addition of dopant atoms in the semiconductor crystal. An undoped semiconductor has an equal number of electron and holes that are created by thermal excitation or by defects in the crystal lattice. If some of the atoms are substituted by a different element, then an imbalance in the number of charge carriers forming a semiconductor with an excess of electrons or holes.

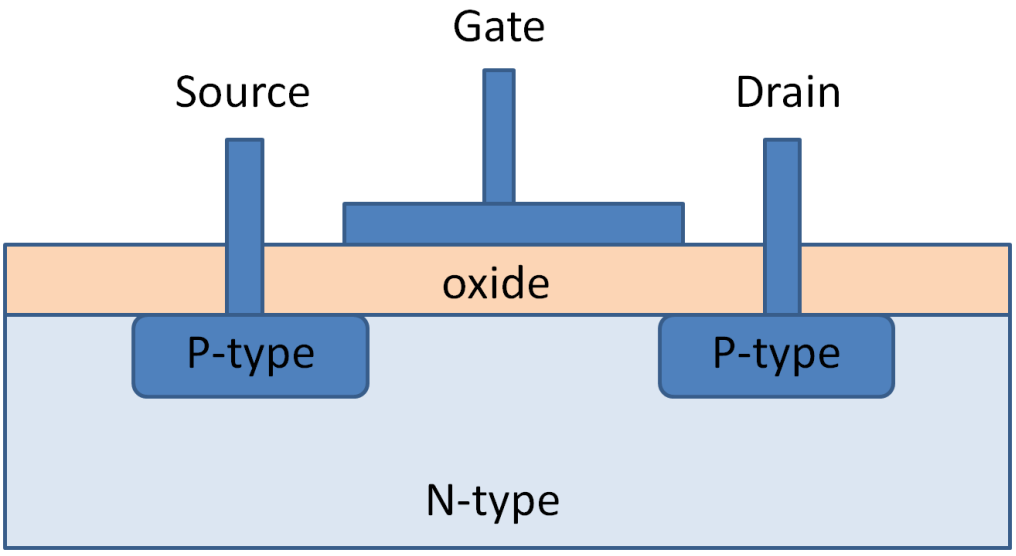

Figure 1. Schematic of a pMOSFET device

An example of this is that if a group IV semiconductor, e.g. Ge, is doped with a group IV element such as Sb. These Sb atoms substitute Ge in the crystal and as Sb has a higher number of valance electrons this means that for every dopant atom there is an extra electron in the lattice that contributes to macroscopic charge transport. This material would then be deemed to be n-type. The analogous argument holds true for if a group III atom is substituted into the lattice then there will be an excess of holes and this is a p-type semiconductor. The doping levels are typically of the order of a few millionths of a percent.

The basic principle of a MOSFET is that when a voltage is applied to the gate the conductivity of the channel is changed. How this conductivity varies with

gate voltage is described in more detail on page 26 but for a description of how a MOSFET works this detail is not necessary. Figure 2 shows a schematic of what is happening to the charge carriers under the gate electrode for different gate biases for an n-type MOSFET.

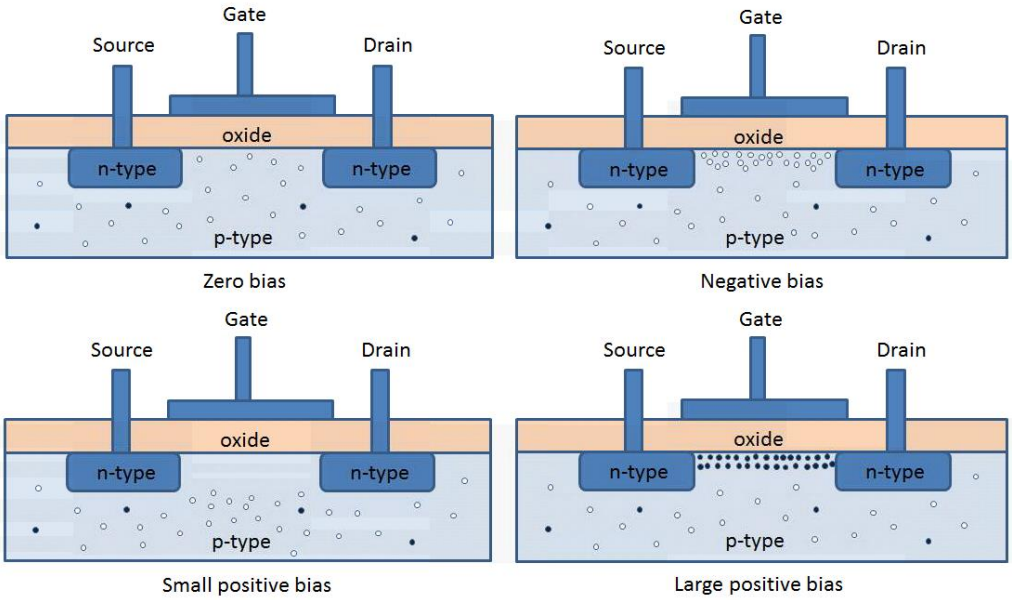

Figure 2. nMOSFET with various gate voltages applied. The white circles representing holes and the dark blue circles representing electrons

When there is no bias applied to the gate in a nMOSFET there is no conduction possible from the source to the drain but as the bias is made more positive the conductivity of the channel changes until the majority charge carrier in the semiconductor under the gate changes to become negative. This then forms a conductive channel from the source to the drain.

1.2.2 Scaling

Gordon Moore made a famous prediction in 1965 that the number of transistors on a chip would double every two years[3]. This prediction became the driving force in improving the manufacturing processes and then became known as Moore's Law. This led to improving the performance of devices by scaling the device dimensions down using constantly developing new fabrication methods. The MOSFET device stayed broadly the same but smaller. For the continued scaling set by Moore's law to continue something had to change as the physical limit of the some of the device materials were being reached. For the area of the gate electrode, A, to be made smaller and for the capacitance, C, to remain the same then according to equation 1 the thickness of the insulating layer, t, must be made smaller or the insulating layer be replaced with a different material with a higher dielectric constant, k as ε_0 is the permittivity of free space and is a constant and therefore cannot be changed.

$$C = \frac{k\varepsilon_0 A}{t} \qquad \text{Eq. 1}$$

As the thickness for SiO_2 is scaled further it becomes possible for electrons to quantum mechanically tunnel directly from the gate to the semiconductor which is known as leakage current. To reduce these high leakage currents the only option is to replace the SiO_2 layer with a layer with a higher κ and have

this layer thicker to reduce the leakage current. The dielectric constant of SiO_2 is 3.9 so this means that if a dielectric had a κ ten times greater than SiO_2 then the thickness of the dielectric can be ten times larger and still have the same capacitance. The equivalent oxide thickness (EOT) is a measure of how thick a layer of SiO_2 would have to be to get the same capacitance as a high κ dielectric and is given by

$$EOT = t_{high\,k}\left(\frac{k_{SiO_2}}{k_{high\,k}}\right) \qquad \text{Eq. 2}$$

Where $t_{high\,\mathrm{k}}$ is the thickness of the high k layer, k_{SiO_2} and $\mathrm{k}_{high\,\mathrm{k}}$ are the dielectric constants of the SiO_2 and the high k layer respectively.

The EOT of a gate stack is not directly measurable from the C-V data. This is due to a contribution to the capacitance from the semiconductor ($C_{channel}$) and the gate metal (C_{metal}) as the accumulation layer cannot exist infinitely close to the interfaces. Equation 3 shows how the total gate stack capacitance (C) is modelled.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{metal}} + \frac{1}{C_{channel}} \qquad \text{Eq.3}$$

This means that the measured capacitance has contributions from the semiconductor and metal as shown in equation 4 where the capacitance equivalent thickness (CET) is the measured value.

$$CET = EOT + t_{metal} + t_{channel} \qquad \text{Eq.4}$$

These electrical thickness contributions from the metal and the channel are intrinsic to the material and the contribution is taken to be 0.3nm so when an EOT value in this thesis is presented it is calculated according to equation 5.

$$EOT = CET - 0.3nm \quad \text{Eq.5}$$

By modelling the device structure as two capacitors in series as shown by

$$\frac{1}{C} = \frac{1}{C_{HK}} + \frac{1}{C_{IL}} \quad \text{Eq.6}$$

where C is the measured capacitance, C_{HK} is the capacitance of the high k layer and C_{IL} is the capacitance of the interfacial layer. From this the dielectric constant of the film can be calculated from equation 7

$$k_{HK} = \frac{t_{HK}k_{IL}}{CET - t_{IL}} \quad \text{Eq.7}$$

where t_{HK} is the thickness of the high k layer, k_{IL} is the dielectric constant of the interfacial layer and t_{IL} is the thickness of the interfacial layer.

For application in MOS technologies this EOT needs to be less than 1nm according to the International Technology Roadmap for Semiconductors (ITRS) and the requirements from the 2013 ITRS report is shown in Figure 3.

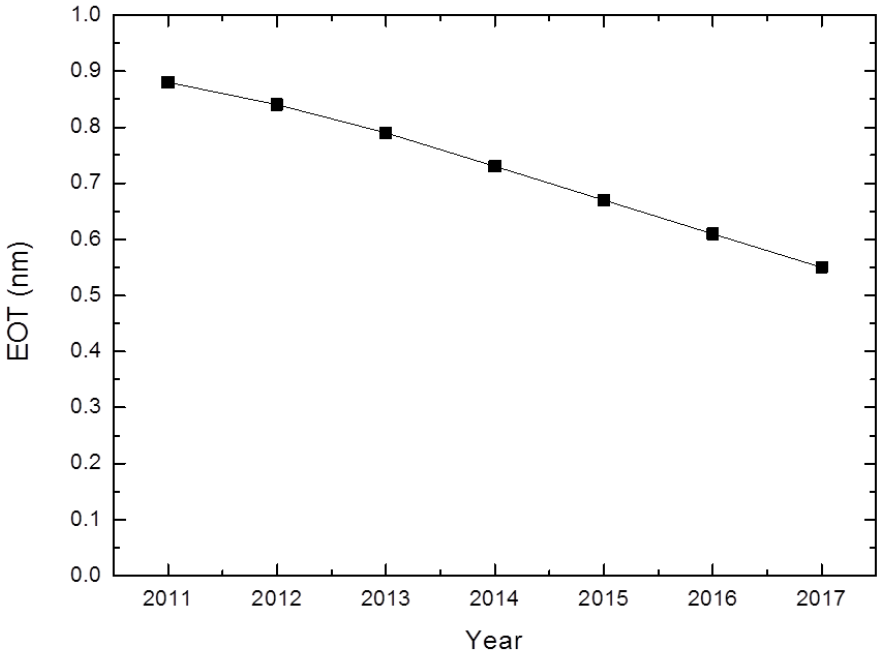

Figure 3. EOT against year of production for bulk planer MOSFET devices [4]

1.2.3 MOS Capacitor physics

The heart of the MOSFET is the MOS capacitor. This is a very useful device in research and development as many of the MOSFET characteristics can be optimised first by fabricating the MOS capacitor. This approach is advantageous as the MOS capacitor is much quicker and simpler to fabricate. Figure 4 shows a typical band diagram of a MOS device.

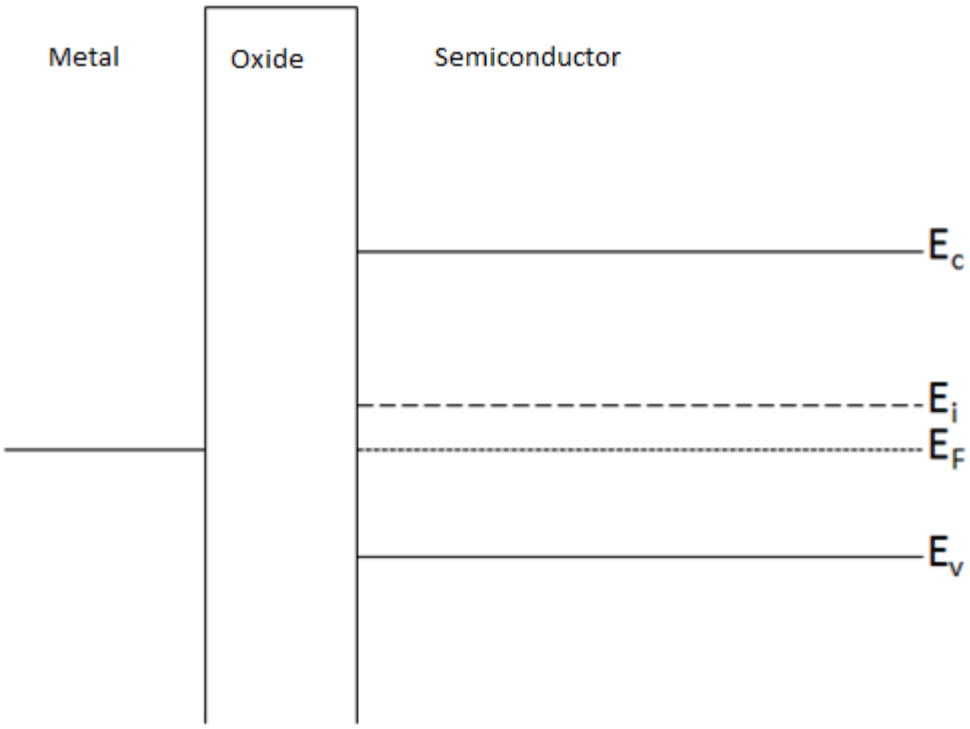

Figure 4. Energy band diagram of a p-type MOS device under flat band conditions where E_c is the conduction band edge, E_i is the intrinsic fermi level, E_F is the fermi level and E_v is the valence band edge. The metal is on the left, the oxide in the middle and the semiconductor on the right

The density of charge carriers (electrons and holes) at the semiconductor-dielectric interface varies as a function of applied gate voltage. This is the most important aspect of how the capacitance in a MOS capacitor changes with the given potential. The carrier density is related to the difference in the Fermi level (E_F) and the intrinsic Fermi level (E_i) and for a p-type semiconductor the concentration of holes is given by

$$p_p = n_i e^{\frac{(E_i - E_F)}{kT}} \qquad \text{Eq.8}$$

Where p_p is the concentration of holes in a p-type semiconductor, n_i is the intrinsic carrier concentration, k is the Boltzmann's constant and T is the temperature.

When a negative bias is applied to the metal gate the bands bend as shown in Figure 5b) and therefore $E_i - E_F$ increases at the surface of the semiconductor and the dielectric which means that the concentration of holes increases as can be seen from equation [eq: carrier density] causing the semiconductor to be in accumulation and therefore the capacitance is at a maximum acting as a standard parallel plate capacitor. The physical process behind this is that the semiconductor already has an intrinsic positive charge and the application of a negative bias to the gate attracts further positive charge from the bulk of the semiconductor whilst also repelling the negative charge that is present when under flat band conditions. The capacitance is measured performing a DC sweep with an AC ripple on it. This accumulation capacitance should be the same across all the frequency range measured (0.1-1MHz) as the majority carriers (holes in this case) are able to respond almost immediately to the changing field.

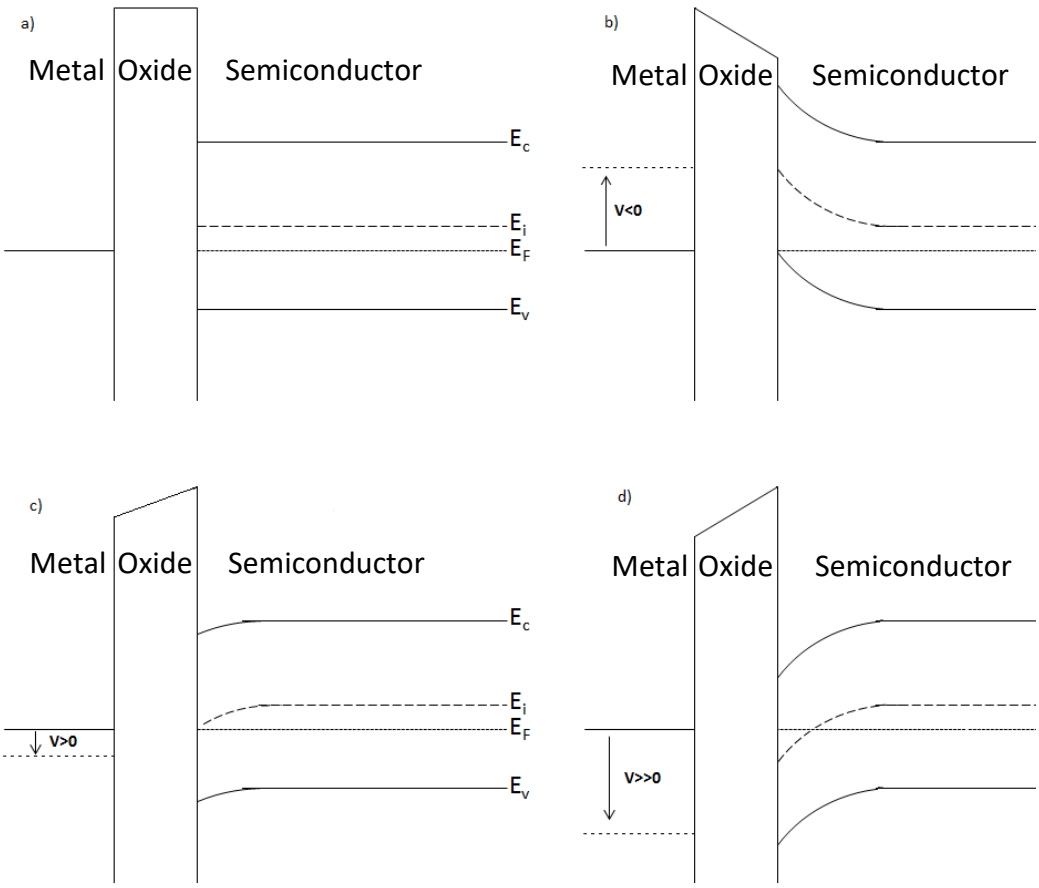

Figure 5. Band Diagrams for a MOS device when in a) flat band b) accumulation c) depletion and d) inversion

When a small positive bias is applied to the gate (as in Figure 5c) the bands start to bend downwards and $E_i - E_F \to 0$ so that $p_p = n_i$. As $n_i^2 = p_p n_p$ where n_p is the electron concentration for a p-type semiconductor, it can be shown that there is no charge present at the surface as shown by

$$n_p = n_i e^{\frac{(E_F - E_i)}{kT}} \qquad \text{Eq.9}$$

due to $p_p = n_p$ causing the device to be in depletion and the capacitance to be at a minimum. If the positive bias is further increased (as in Figure 5d), the bands bend further so that E_i crosses E_F causing p_p to be less than n_i from equation [eq: carrier density]. This now means that n_p is larger than n_i ($E_F - E_i > 0$)so that $n_p > p_p$ causing the device to be in inversion. To explain this from a physical perspective means considering how the minority and majority carriers respond to the applied field from the positive gate bias. If a larger positive bias is applied to the gate, then this will cause the majority carriers (holes) to be repelled from the interface and for the minority carriers (electrons) to be attracted to the interface. These electrons then form a small inversion layer at the interface where they now become the majority carriers. This now acts again like a parallel plate capacitor and the capacitance should be the same as in the accumulation case and this inversion layer is the channel layer in a transistor for switching the transistor on and off. If the frequency is too large then the minority carriers do not have enough time to react to the changing bias and are repelled from the interface and an inversion layer cannot form, when this happens the device goes into depletion. Since there is now no charge present at the interface the capacitance is very low. For even higher frequencies the width of the depletion layer continues to widen as a function of the magnitude of the gate bias and drives the capacitance even lower. These different regimes are shown in Figure 6 figure when measured as a C-V curve.

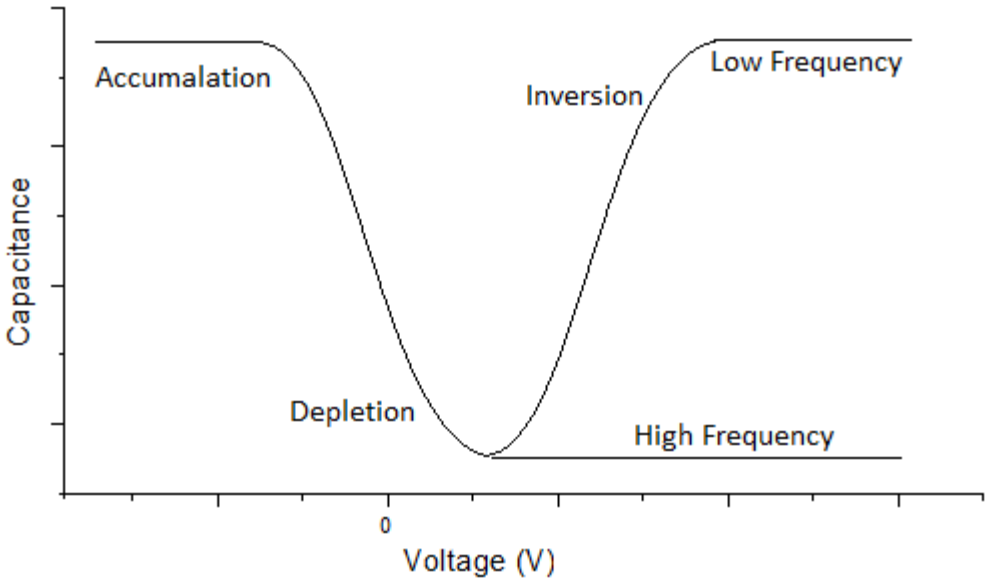

Figure 6. C-V characteristics of a MOS devices

In a real device, there are charges present in the oxide layer and at the interface. These charges can change the C-V measurements. One type of charge is known as fixed oxide charge and these are located near the semiconductor/oxide interface and the effect on the C-V measurements is to translate the graph along the voltage axis but the shape will be unaffected as these charges are not bias dependant. A negative fixed oxide charge will act to shift the measurements to a higher voltage and a positive fixed oxide charge will shift the measurements to a lower voltage. This effect is shown in Figure 7 where the translation along the voltage axis is shown is relation to an ideal device with no fixed oxide charge.

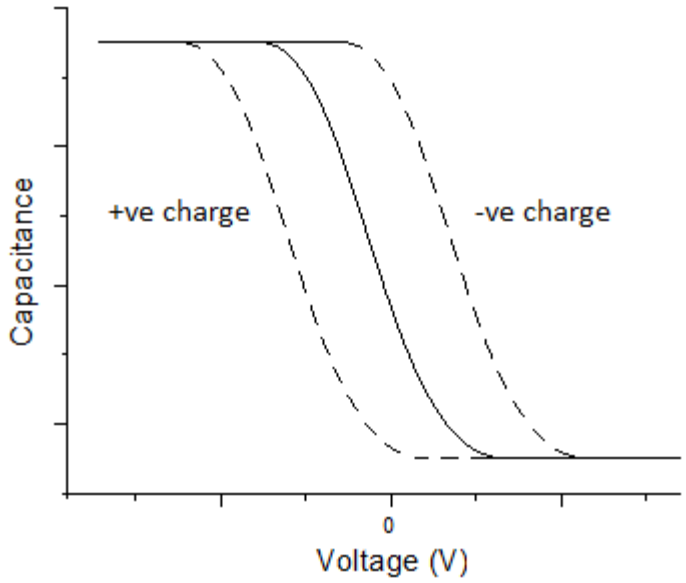

Figure 7. C-V graph showing the effect of fixed oxide charge

This is due to the charges causing band bending at the interface thereby changing the value of $E_i - E_F$. A negative fixed oxide charge will increase this value meaning a larger bias is required to move from accumulation to depletion.

There is another form of charge that is present which is voltage dependant and are known as interface states. These states are present at the interface and their occupation is dependent on their position in the band gap and the position of the Fermi level. Figure 8 shows the position of these states within the band gap.

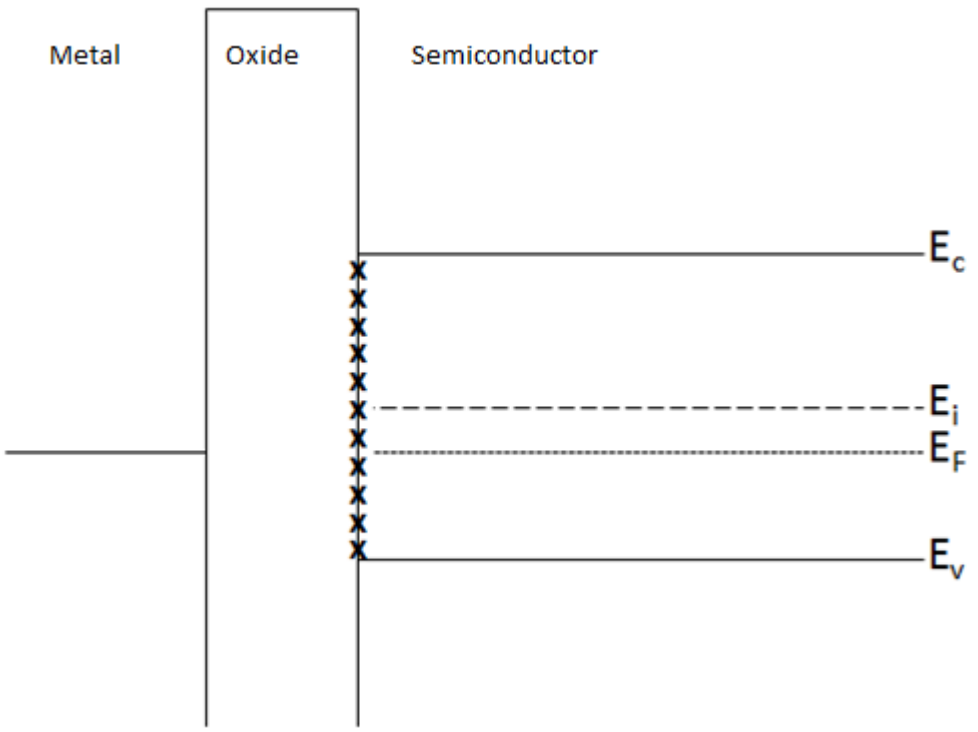

Figure 8. Band diagram under flat band conditions where the crosses denote the position of interface states

There are two kinds of states and these are donor and acceptor like states. Donor like states are neutral when full of electrons and positive when empty. Acceptor like states are negative when occupied with electrons and neutral when empty. As the bias voltage is being swept the band bending at the interface causes these states to fill or empty which changes the overall amount of charge at the interface thereby changing the capacitance being measured. The effect of these interface states on a C-V graph is shown in Figure 9 and the characteristic change in shape known as stretch out.

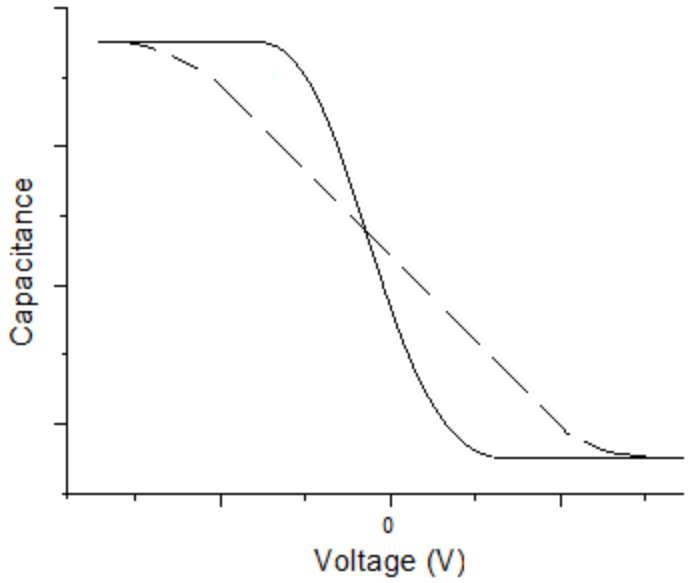

Figure 9. CV graph with the dotted line representing the stretch out effect due to interface states

It is thought that acceptor like states are in the top half of the band gap and donor like states are in the bottom half of the band gap. This means that interface states and fixed oxide charge can be distinguished by measuring at the mid-gap so that all the states are neutral and not contributing to the measurements.

1.2.4 Current Density-Voltage

The J-V characteristics of a MOS capacitor are important for determining properties such as the leakage and breakdown voltage of the device. In an ideal device, there would be no leakage current at all but as the insulating layer in the MOS structure is scaled down the leakage due to quantum mechanical tunnelling becomes a constraining issue. The main conduction

mechanisms are direct tunnelling, Fowler-Nordheim tunnelling and Frenkel-Poole tunnelling. These different tunnelling mechanisms are shown in Figure 10.

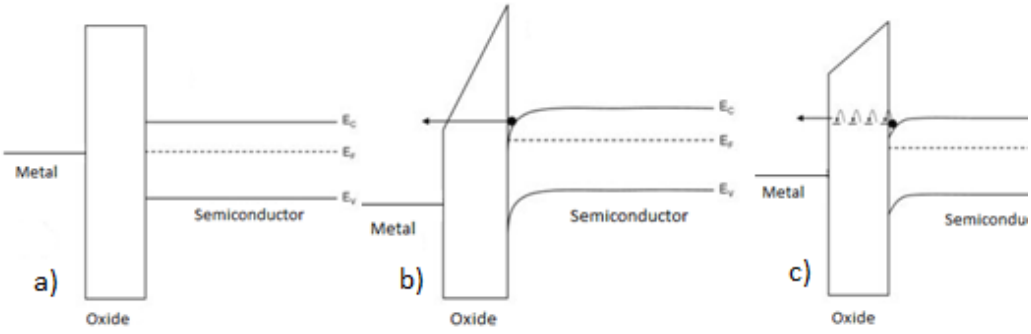

Figure 10. a) shows the system under flat band condition, b) shows Fowler-Nordheim tunnelling and c) shows Frenkel-Poole tunnelling

Direct tunnelling occurs due to a finite probability of an electron appearing on the other side of a potential barrier and for thin films this is unavoidable. Fowler-Nordheim tunnelling is where in the presence of an electric field the conduction band of the oxide forms a triangular potential barrier to conduction which can lead to a shortening of the potential barrier and therefore a higher probability of an electron tunnelling through it.

For dielectric layers that are less than about 3.5nm thick direct tunnelling through the layer plays a dominant role whereas for thicker layers in a Si/ SiO_2 system Fowler-Nordheim tunnelling plays a larger part and the Fowler-Nordheim conduction is given by

$$J_{FN} = C\xi_{ox}^2 e^{\frac{-\beta(\varphi)}{\xi_{ox}}} \quad \text{Eq.10}$$

where J is the current density, ξ_{ox} is the electric field, ϕ is the potential barrier height for electron emission and C and β are given by

$$C = \frac{q^3 m_o}{8\pi h m_{ox}\varphi} \quad and \quad \beta = \frac{8\pi}{3}\frac{(2m_{ox})^{\frac{1}{2}}}{qh}\varphi^{\frac{3}{2}} \quad \text{Eq.11}$$

where q is the charge on an electron, m_o and m_{ox} are the mass of an electron at rest and the effective mass of an electron in the dielectric respectively and h is Planck's constant.

For high κ dielectrics Frenkel-Poole can contribute more to the leakage current. Frenkel-Poole is a bulk-limited effect which is caused by impurities in the dielectric causing Coulombic traps in the band gap of the dielectric. This means that electrons can hop from trap to trap via the conduction band of the dielectric. The governing equations for Frenkel-Poole conduction given in by

$$J = \sigma_o E e^{B(\xi)^{\frac{1}{2}}} \quad where \quad B = \frac{q}{kT}\left(\frac{q}{\pi\varepsilon_0\varepsilon_r}\right)^{\frac{1}{2}} \quad \text{Eq.12}$$

where σ_o is the conductivity, T is temperature and ε_0 and ε_r are the permittivity of free space and the dynamic dielectric constant respectively.

It can be difficult to identify which conduction mechanism is dominant so measuring the conduction at different temperatures can help resolve this due

to the higher temperature dependence of Frenkel-Poole conduction when compared to Fowler-Nordheim conduction.

1.3 High-k dielectrics

1.3.1 Dielectric theory

The dielectric is a material that can be polarised by the application of an electric field. This happens by the slight rearrangement of the charges within the material and the macroscopic polarisation is given by

$$P = N_m \alpha_m E \qquad \text{Eq.13}$$

Where N_m is the number density of microscopic polarisation, α_m is the microscopic polarisibility and E is the local electric field.

The Clausius-Mossetti relation is given by [5]

$$\frac{k-1}{k+2} = \frac{4\pi}{3}\frac{\alpha_m}{V_m} \qquad \text{Eq.14}$$

Where k is the relative permittivity and V_m is the molar volume of the system.

From this the macroscopically defined dielectric constant is related to the microscopic polarisation.

The polarisability of a material occurs typically through three different ways, the permanent, ionic and electronic polarisations. It is assumed that there is

no permanent polarisation in high-k materials and the dominant polarisation mechanism is via ionic polarisation.

1.3.2 Choice of High-k

There are many options to choose from as a high-κ dielectric and some of these are listed in Table 1.

	Dielectric Constant	Band Gap (eV)
SiO_2	3.9	9
GeO_2	5-7	5.8
Al_2O_3	8	6.4
HfO_2	18-25	5.8
$HfSiO_4$	11	6.5
ZeO_2	25	5.8
TiO_2	36-70	3.1
La_2O_3	30	6

Table 1. Potential high-k oxides with their corresponding dielectric constant and bandgap

Some of the key requirements of this dielectric for use in a MOSFET are as follows:

1. It must be insulating by having band offsets to the semiconductor greater than 1eV

2. The dielectric constant must be sufficiently high so that it can be used for several scaling nodes

3. It needs to be thermodynamically stable to withstand high processing temperatures during manufacture

4. It needs to form low defect electrical interfaces with the semiconductor and the metal

The dielectric constant has an inverse relationship with band gap as shown in Figure 11 so that the materials with a very high dielectric constant are not suitable due to small band offsets. This discounts the very high κ materials such as $SrTiO_3$ which has a dielectric constant of ~2000 but a band gap of only 3.2 and also TiO_2[6].

1.4 High Mobility MOSFET Channels

1.4.1 Why are they Necessary?

If the silicon oxide layer is being replaced, then the main advantage of using silicon is now less relevant so this means that the channel material can be replaced by one with better electrical properties.

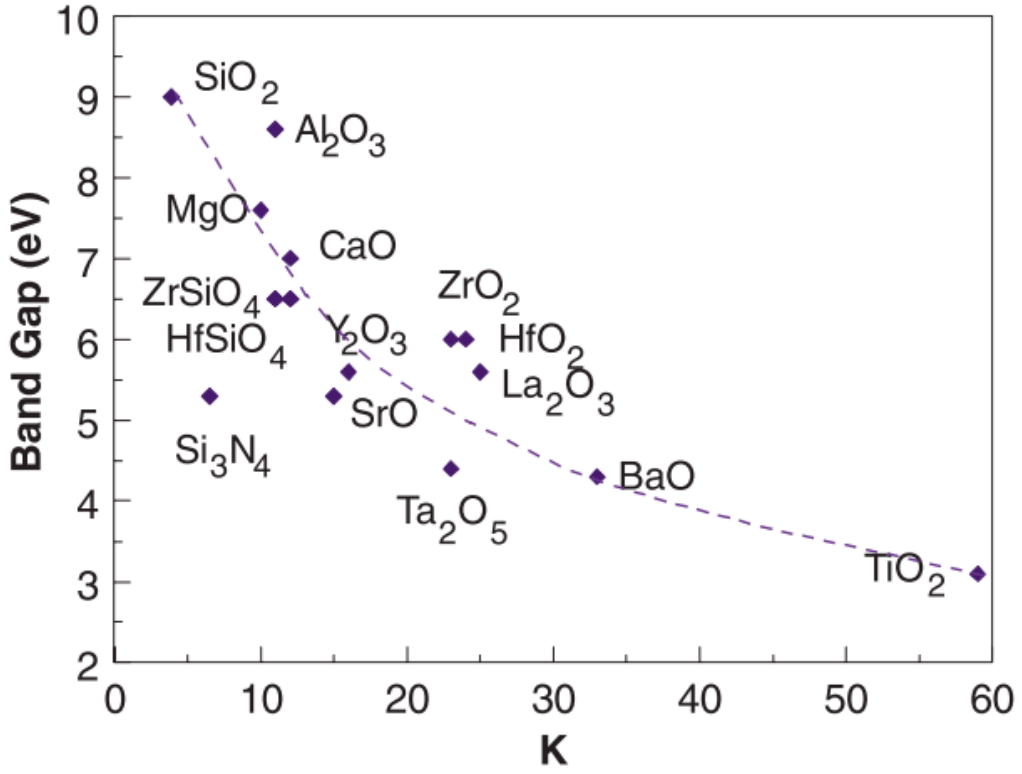

Figure 11. Band gap against dielectric constant, from [7]

The drain current is the current that flows from the source to the drain of a MOSFET and is given by

$$I_D = \frac{W}{L}\mu C_{ox}(V_G - V_T)V_D \qquad \text{Eq.15}$$

where W is the channel width, L is the channel length, μ is the channel mobility, C_{ox} is the oxide capacitance, V_G is the gate voltage, V_T is the threshold voltage and V_D is the drain voltage. Increasing I_D is necessary for improving the device performance. As the terms on the right-hand side of the equation are reduced the drain current will also reduce meaning that the voltages will have

to be increased. This is undesirable for efficiency reasons so increasing the mobility of the channel increases the drain current so that lower voltages can still be used.

1.4.2 Channel Materials

One candidate material for use as the channel is germanium due to its superior electron and hole mobilities (2x and 4x larger than silicon respectively). It is also possible that MOSFETs using germanium for the p-type channel due to its large hole mobility and a III-V semiconductor (such as GaAs) for n-type channel due to their high electron mobility will be integrated on the same integrated circuit. The properties of candidate MOSFET channel materials are shown in Table 2.

	Silicon	Germanium	GaAs
Band Gap (eV)	1.12	0.66	1.42
Electron mobility (cm^2/Vs)	1500	3900	8500
Hole Mobility (cm^2/Vs)	475	1900	450
Intrinsic Carrier Concentration (cm^{-3})	$1.45x10^{10}$	$2.4x10^{13}$	$1.79x10^{6}$

Table 2. Comparison of some of the properties of Si, Ge and GaAs

1.5 Literature Review

For the proper operation of a MOSFET the interface between the semiconductor and the dielectric needs to have a low number of defects and this is referred to as surface passivation. To achieve a well passivated surface a thin passivation layer is required to make a good electrical contact between the germanium substrate and the dielectric as high k dielectrics such as HfO_2 in direct contact with the germanium have a high D_{it} [8]–[10] so are unsuitable for CMOS applications. GeO_2 can be used to pacify the surface of germanium and a review of the problems associated with it and possible solutions will now be discussed. It was initially thought that a problem with employing GeO_2 as the passivation layer was problematic because the GeO_2 layer would degrade in to its sub oxides [10]. A Ge/GeO_2 interface was shown to have improved electrical properties when the Ge surface was oxidised at a high pressure (70 atmospheres) [11]. This improvement in the interface was explained by considering GeO is formed at the Ge/GeO_2 interface and then diffuses through the GeO_2 and then desorbs at the GeO_2 surface. When the oxygen pressure in increased the vapour pressure of the GeO at the surface is reduced thereby suppressing the desorption of GeO. These MOS capacitors showed a significant improvement of electrical properties when compared to Ge/GeO_2 MOS capacitors grown with atmospheric oxygen and had a minimum D_{it} of $2x10^{11}eV^{-1}cm^{-2}$. The thickness of the film was 18.5nm which is too thick to be used in advanced CMOS devices as the EOT is too large.

This mechanism for GeO desorption at the interface by the reaction of Ge and GeO_2 was confirmed by Kita et al who sputtered GeO_2 on to Ge and on Si [12]. These films were then annealed at various temperatures and thermal desorption spectroscopy (TDS) was used to analyse the desorbed species. Figure 12 shows the results of the TDS analysis.

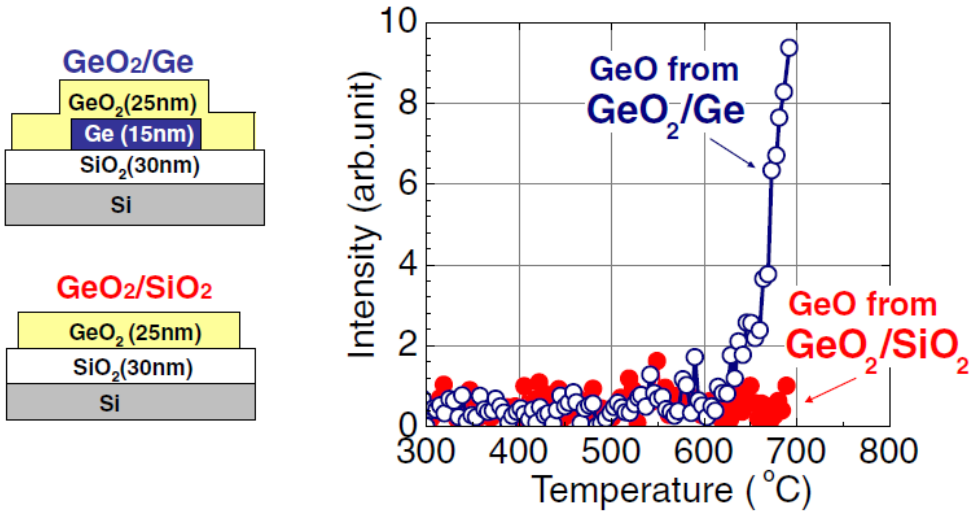

Figure 12. A schematic (left) of the gate stacks fabricated for TDS analysis. The results of the TDS are shown on the right, after Kita et al [12]

The intensity of the signal above 600°C increases for the Ge/GeO_2 system but not the SiO_2/GeO_2 system. The authors conclude that the GeO desorption is driven by the reaction at the interface between Ge and GeO_2 and not from the bulk of the GeO_2 otherwise there would be a GeO signal from both sets of samples. Oniki et al performed similar experiments and also found this desorption of GeO from the interface but with the onset of desorption occurring at a lower temperature of around 400°C [13].

Milojevic et al investigated how the Ge surface changes during an ALD process [14]. This was achieved by interrupting the ALD process in between pulses and then employing in situ XPS analysis. Figure 13 shows the XPS data for deionised water (DIW) etched Ge surface and how it evolves with processing and a Ge surface cleaned by UHV annealing.

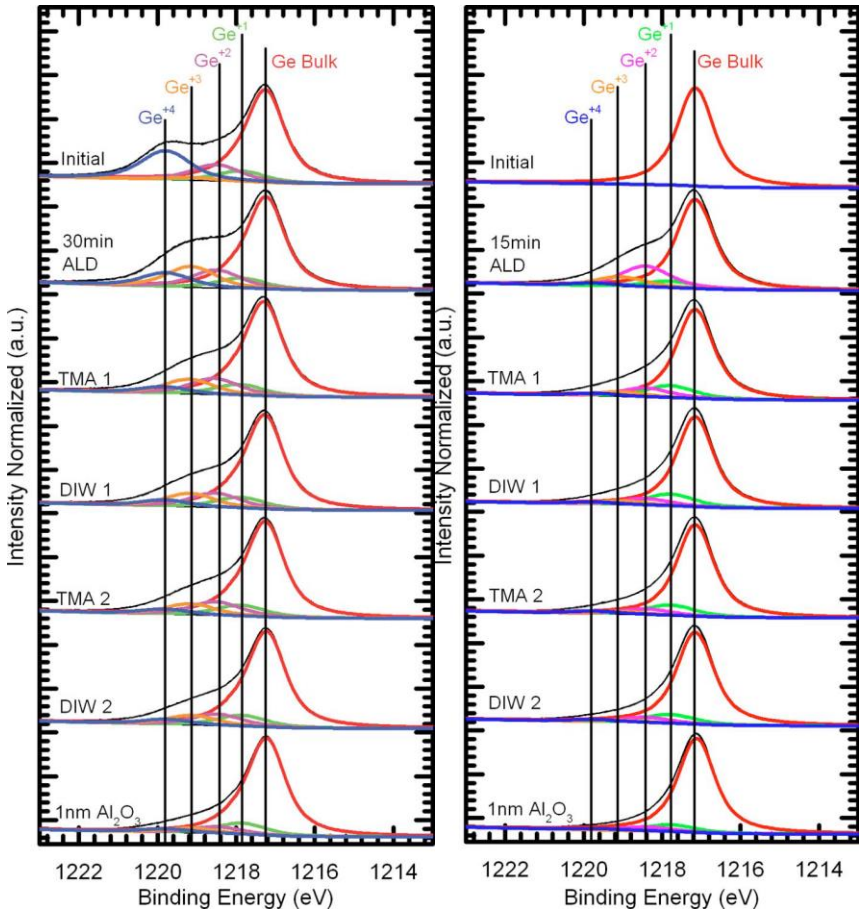

Figure 13. XRD spectrum showing Ge $2p_{3/2}$ of DIW etched germanium (left) and UHV cleaned germanium (right) showing reduction in the germanium oxides after TMA and water pulses. After Milojevic et al [14]

These results show that the surface is very sensitive to the ambient condition in the ALD reactor as after 15 minutes the “clean” Ge grows a thin oxide in the reactor which is then reduced upon successive ALD cycles of TMA and H_2O. DIW etched Ge showed a reduction in the initial oxide surface and a shift to lower oxidation states which were then reduced during the ALD process. These results highlight the difficulty in processing as this initial oxidation will always be present in a commercial ALD tool.

Al_2O_3 has been proposed as a barrier against the desorption of GeO. Zhang et al [15] proposed a method whereby a Ge/Al_2O_3 gate stack was grown by ALD and subsequently given an electron cyclotron resonance (ECR) plasma post oxidation resulting in a Ge/GeO_x/Al_2O_3 gate stack. Figure 14 shows a TEM image of the resulting gate stack.

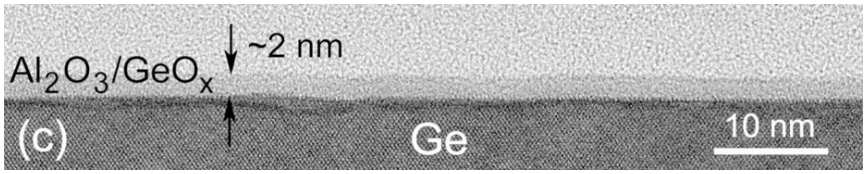

Figure 14. TEM image of a Ge/GeO_x/Al_2O_3 gate stack, after Zhang et al [15]

The thickness of Al_2O_3 was 1nm and after the oxygen plasma treatment the film grew to 2nm. The lack of clarity between the GeO_x and Al_2O_3 was attributed to low contrast in the TEM image between the two layers and that they are extremely small (~1nm). The MOS capacitors showed improved C-V

characteristics after the plasma treatment and had a D_{it} of $5x10^{10}eV^{-1}cm^{-2}$ for p-type and $6x10^{10}eV^{-1}cm^{-2}$ for n-type. Subsequent investigations from the same group [16] showed that the D_{it} has a strong dependence on the thickness of the GeO_x layer which is showed in Figure 15 where the differing thicknesses of the GeO_x was achieved by keeping the plasma treatment the same but changing the thickness of the Al_2O_3 layer. The thicker Al_2O_3 layers reducing the amount of active oxygen species available to form GeO_x.

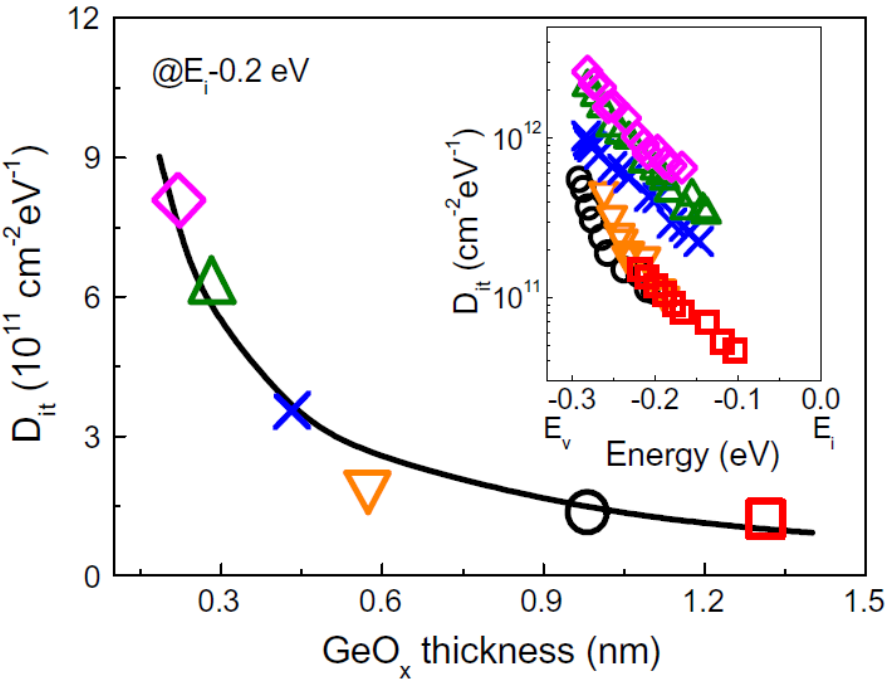

Figure 15. D_{it} at -0.2eV as a function of GeO_x thickness with the corresponding D_{it} distributions in the inset, after Zhang et al [16]

This shows that if the thickness of the GeO_x layer is less than 0.5nm then the D_{it} rises sharply. Using this manufacturing technique to make pMOSFETs the hole mobility was characterised as a function of EOT and is shown in Figure 16.

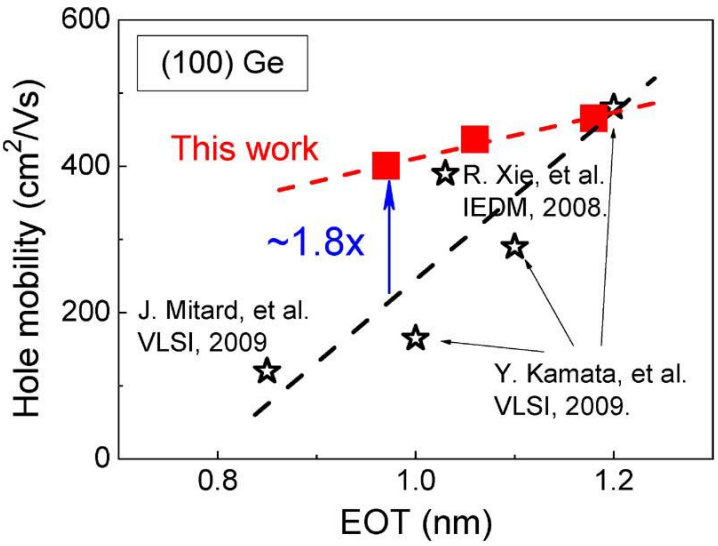

Figure 16. Peak hole mobility as a function of EOT of the pMOSFETs fabricated in [17] *compared with other work in the area, after Zhang et al* [17]

More recent work used the same technique but this time as a $Ge/GeO_x/Al_2O_3/HfO_2$ gate stack so that the thickness of Al_2O_3 could be reduced making it possible to scale down the EOT of the gate stacks. Figure 17 shows how the EOT can be reduced using this tri-layer gate stack whilst maintaining a low D_{it}.

The electron and hole mobilities were also characterised as the plasma oxidation time was varied giving different thicknesses of GeO_x and are shown in Figure 18 [17]. The samples had 2.2nm HfO_2 and 0.2nm Al_2O_3 deposited by ALD with different EOT values corresponding to the different thicknesses of the underlying GeO_x.

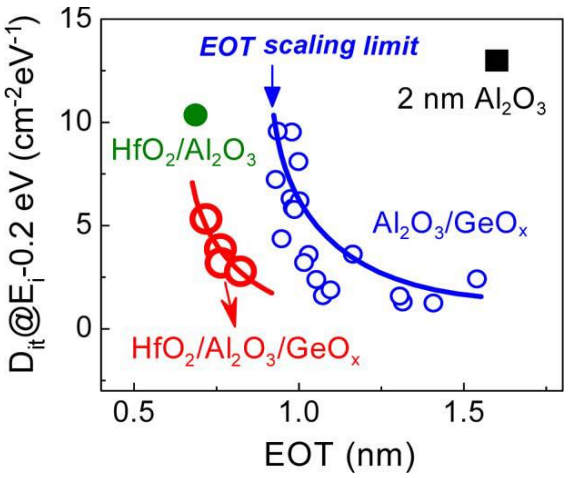

Figure 17. D_{it} as a function of EOT for gate stacks with and without using HfO_2 for lowering the EOT, after [17]

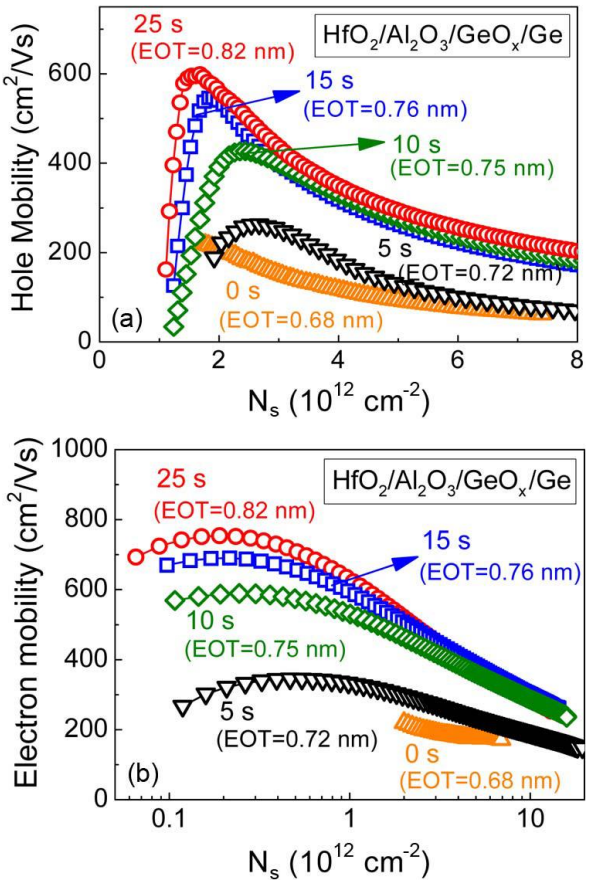

Figure 18. Ge p and n-type MOSFETs giving the hole (a) and electron (b) mobilities for $Ge/GeO_x/Al_2O_3/HfO_2$ gate stacks, after Zhang et al [17]

These MOSFETs showed a peak hole mobility of 596cm^2/Vs and peak electron mobility of 754cm^2/Vs. The authors conclude that these results show the feasibility of applying this technique in high performance CMOS.

One possible route towards creating a gate stack with a low EOT and low D_{it} is to use sulphur to passivate the germanium surface. Merckling et al [18] proposed a method whereby the germanium substrate was heated up to 750^{o}C in a UHV environment to evaporate the surface GeO_2. This surface was exposed to molecular H_2S at a pressure of 2x10^{-6} Torr and underwent subsequent deposition of Al_2O_3 by MBE. Structures with an ultrathin Al interlayer between the H_2S and the Al_2O_3 layers were also fabricated. MOS capacitors were used to characterise the interface after forming gas annealing and the C-V measurements are shown in figure 1.

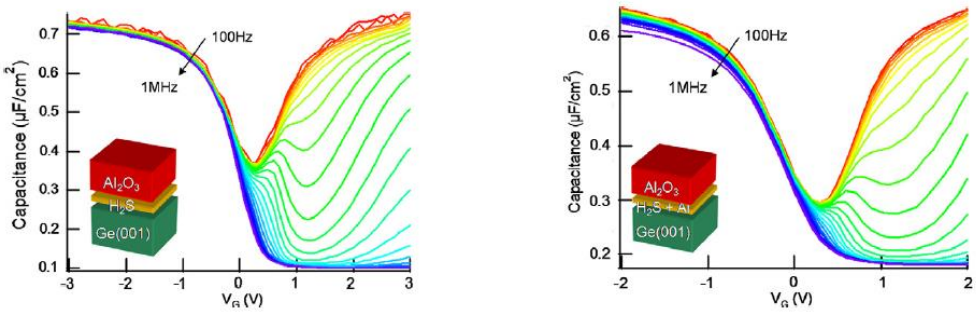

Figure 19. CV characteristics as a function of frequency of Al_2O_3/H_2S–Ge (left) and $Al_2O_3/Al/H_2S$–Ge (right) MOS capacitors measured at RT, after Merckling et al [18]

These show a characteristic C-V curve with very low frequency dispersion in accumulation. In the strong inversion region, the frequency dispersion was attributed to the fast response of minority carriers in the Ge. For the Al_2O_3/H_2S–Ge system, the interfacial state D_{it} values were extracted using the conductance method and estimated to be 5 x 10^{12} $cm^{-2}eV^{-1}$. In the case of the $Al_2O_3/Al/H_2S$–Ge system, the interfacial state D_{it} values were estimated to be low 10^{12} $cm^{-2}eV^{-1}$. The authors assert that the use of an interfacial Al pre-layer has evidently improved the electrical passivation.

Another method of fabricating S-passivated Ge gate stacks is to expose the surface of HF cleaned germanium to ammonium sulphide ex situ. Sioncke et al used this method with subsequent high-k deposition via ALD [19]. Figure 20 shows the CV characteristics of $Ge/S/Al_2O_3$ (8nm).

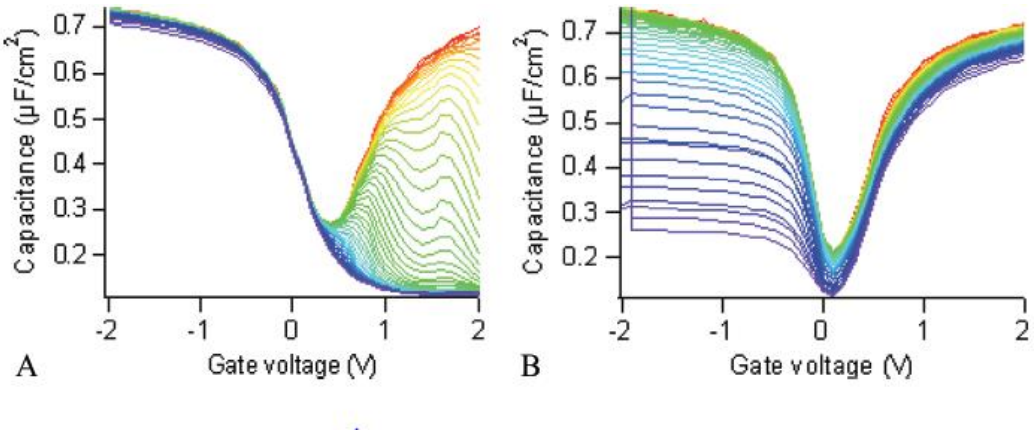

Figure 20. CV as a function of frequency characteristics of $Ge/S/Al_2O_3$ (8nm) with p-type (left) and n-type (right) Ge, after Sioncke et al [19]

Figure 21 shows the D_{it} distribution as a function of position in the band gap for this Ge/S/Al_2O_3 (8nm) system.

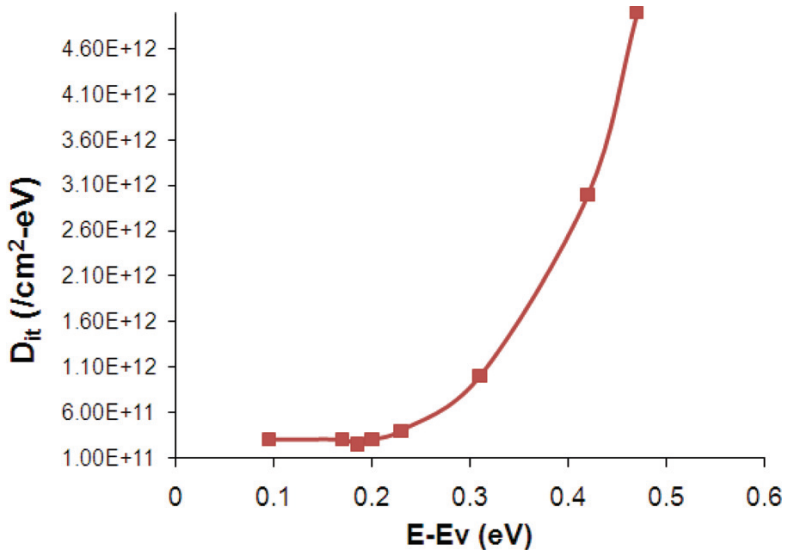

Figure 21. D_{it} distribution as a function of position in the band gap for a Ge/S/Al_2O_3 (8nm) gate stack, after Sioncke et al [19]

As this gate stack has a low D_{it} at the valance band edge it is most suitable for PMOS operation. Gate stacks were also fabricated with HfO_2 and ZrO_2. Figure 22 shows the C-V characteristics for these gate stacks which show that the use of high-k in direct contact with the S-passivated Ge have strongly degraded C-V behaviour.

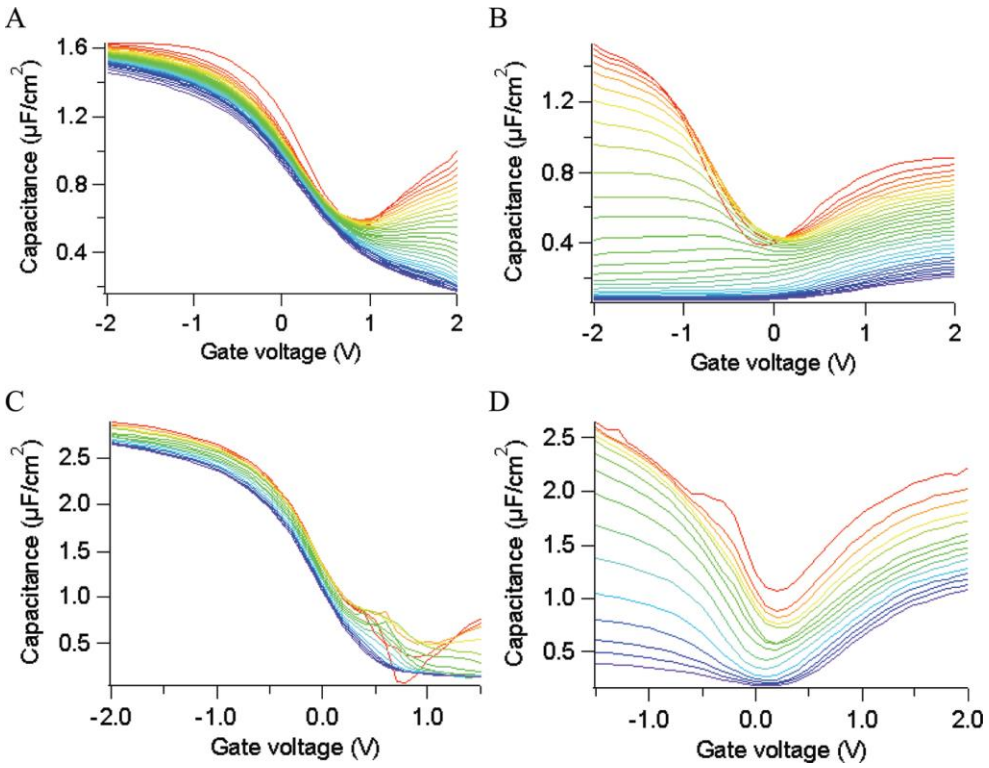

Figure 22. CV as a function of frequency characteristics of $Ge/S/ZrO_2$ (8nm) on p-type (A) and n-type (B) Ge. $Ge/S/HfO_2$ (4nm) on p-type (C) and n-type (D) are also shown, after Sioncke et al [19]

The authors conclude that a bilayer structure with at least 2nm of Al_2O_3 with high-k on top is the best route towards structures low D_{it} and scaled down EOT.

Chellappan et al [20] have performed an XPS study of S-passivated Ge which was achieved by immersion in ammonium sulphide for 20 minutes at room temperature with subsequent deposition of Al_2O_3 by ALD using TMA and H_2O as the precursors. Figure 23 shows the Ge 3d XPS spectra of $Ge/S/Al_2O_3$ and how it varies with anneal temperature.

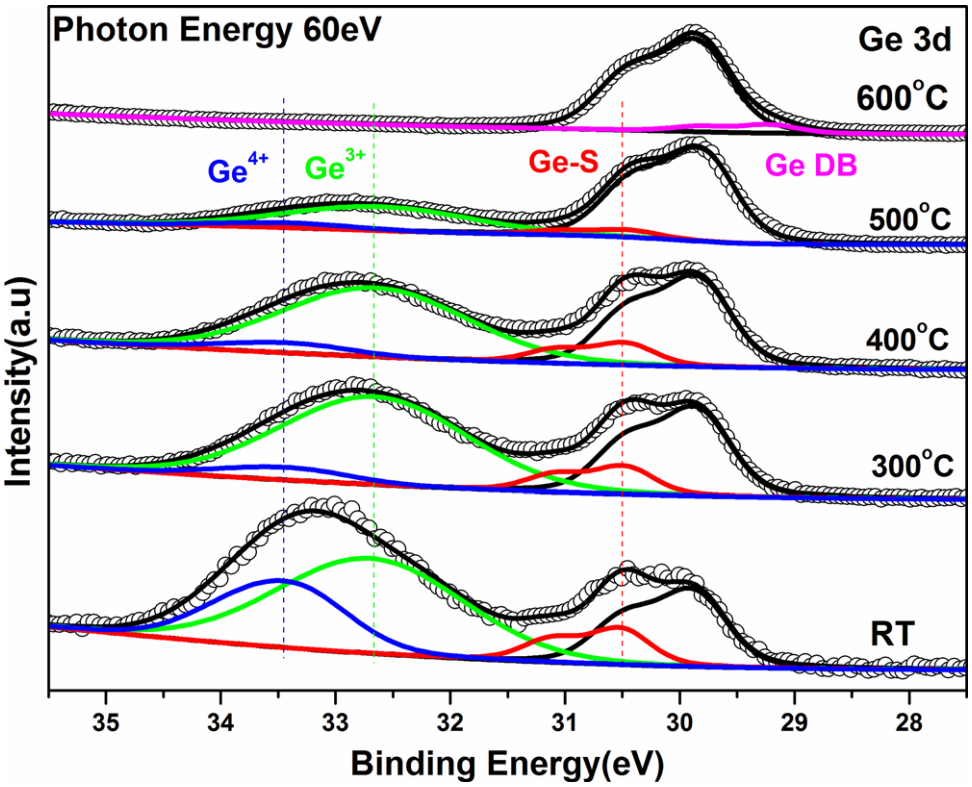

Figure 23. XPS spectrum showing Ge 3d spectre of a Ge/S/Al_2O_3 sample after successive anneal cycles, after Challapan et al [20]

The authors estimate that the oxide component is 0.7nm thick and shows significant reduction upon annealing up to 600°C where it is totally removed and a small new peak 0.53eV below the main peak appears which is attributed to the creation of germanium dangling bonds at the interface. The authors used Kraut's method to calculate the band offsets of the structure after the 600°C anneal and found the valance band offset to be 3.4eV and the conduction band offset to be 2.74eV and conclude that these offsets are an effective barrier against carrier injection across a MOS device.

The same group also performed an XPS study of HfO_2 on S-passivated Ge [21]. Figure 24 shows the thermal stability of the Ge-S bond.

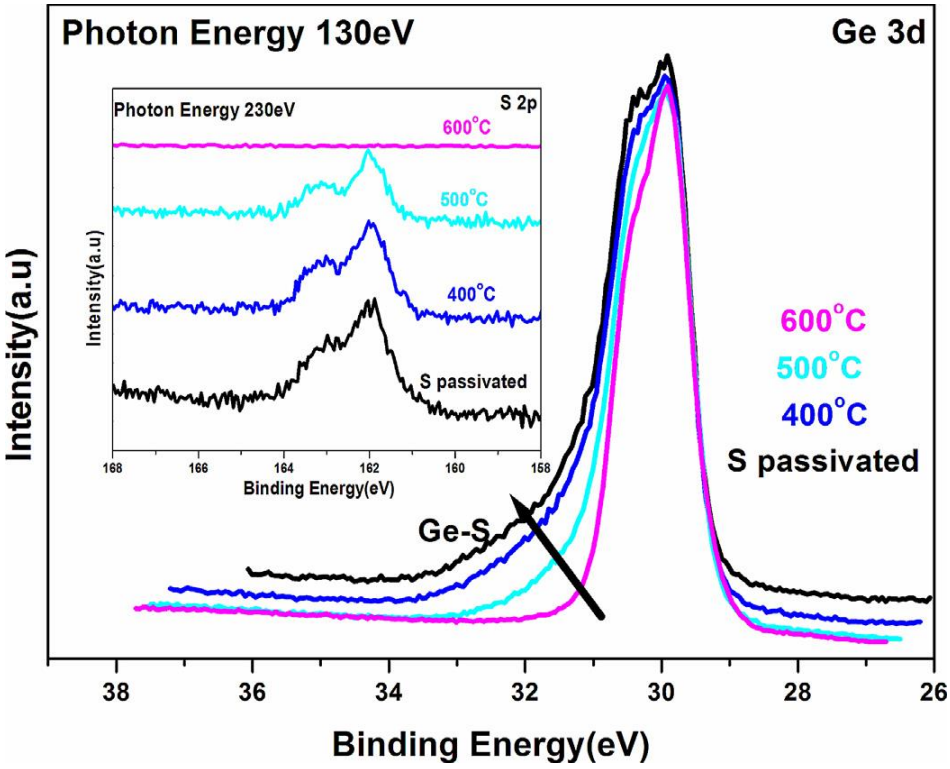

Figure 24. XPS spectrum showing Ge 3d peak and S 2p peak (inset) for S-passivated Ge at various temperatures, After Challappen et al [21]

These results show that the sulphur signal shows no change up to 400°C and decreased to below the detection limit after 600°C annealing. The authors also find that after the sulphur treatment there are no germanium oxide components in the Ge 3d peak profile but after ALD of HfO_2 there is a 1nm thick interfacial oxide which forms either during deposition or following air exposure. The band offsets were also calculated with the valence band offset

as 2.7eV and the conduction band offset as 2.3eV which is sufficient to act as a barrier against carrier injection across a MOS device.

A study by Fleischmann et al [22] shows that the ammonium sulphide treatment saturates after 30s with a maximum sulphur coverage below half a monolayer and that the Ge-S bonds are preserved upon moderate exposure to ambient conditions and after ~2 hours approximately 15% of the sulphur is oxidised from which they conclude that proper control of the time exposed to ambient conditions is crucial to prevent degradation of the surface properties and the electrical performance loss that could be associated with it. Figure 25 shows a XPS spectra of the Ge $2p_{3/2}$ spectre from this study.

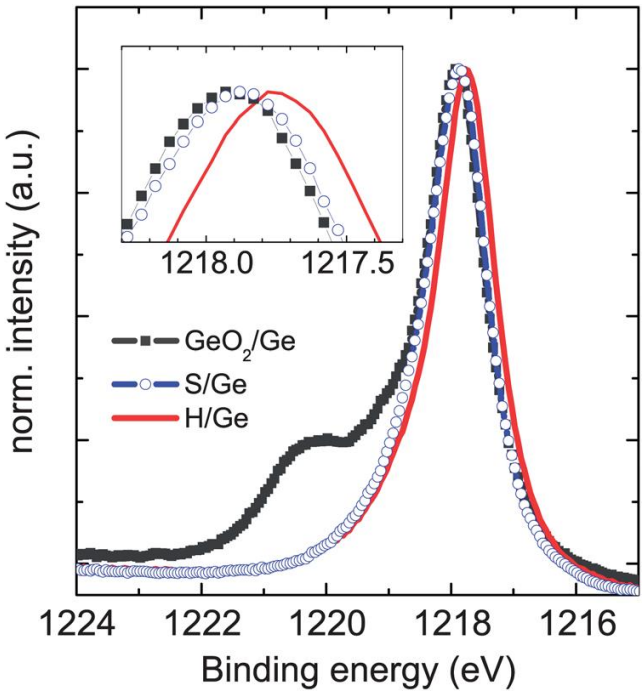

Figure 25. XPS spectrum showing Ge $2p_{3/2}$ with HF cleaned Ge, S treated Ge and an untreated GeO_2/Ge sample. The inset shows a close up of the maximum intensity, After [22]

There is an increase in binding energy of 0.13eV after S-treatment. This coupled with scanning tunnelling spectroscopy (STS) data from the authors shows that the Ge-S have a partial ionic character causing band bending at the interface and a depletion of the majority charge carriers near the surface of the germanium.

Other passivation methods have been used to lower the D_{it} but these have not quite as low as the GeO_2 case. These include nitridation of the germanium surface to form either GeN_x or a GeO_xN_y layer [23]–[29]. These passivation layers are made by plasma nitridation [26], [28], [29] and NH3 exposure [30]. It has been reported that the D_{it} is larger for these devices than a germanium oxide interfacial layer [31].

2. Growth and Processing

2.1 Germanium Substrate Cleaning

An important part of the process when trying to achieve low EOT's is the correct cleaning of the substrate so as to remove all of the native germanium oxide which has a low κ value (4.5-7 depending on growth conditions). There are many ways in which this cleaning can be achieved, e.g. HF [32]–[36], HCl [32], [33], [37], HBr [33], [36], [37], using H_2O_2 as an intermediate step [33], [38]. Cyclic HF cleaning is the most commonly used and the hydrogen coverage of the surface of the germanium is proportional to the concentration of the HF [32]. Using a cyclic H_2O/H_2O_2 (30%)/HF(10%) procedure with nitrogen drying in between each step, Rivillon et al [39] reported an oxide free fully hydrogen terminated surface but has large carbon contamination when exposed to ambient air. Others have reported a small amount of native oxide remaining after HF cleaning [36] but this is often removed by annealing in a vacuum or in a hydrogen environment which removes any carbon contamination associated with the HF clean. HBr cleaning gives a fully bromine terminated surface but upon exposure to H_2O the Ge-Ge back bonds break and then replace the halogen terminated surface with a hydroxyl group which then leaves the surface prone to oxidation in the presence of oxygen [37] and this process occurs for chlorine terminated surfaces as well. As germanium oxide is volatile

at temperatures above 430^{o}C, annealing in a UHV will cause the native oxide layer to desorb from the surface leaving an oxide free surface [9].

For this work the most repeatable method for wet cleaning was found to be a three-minute ultrasonic bath in acetone to degrease the surface followed by a 30s dip in DI water to etch most of the native oxide. This was then followed by exposure to oxygen plasma in the ALD chamber to grow a sacrificial oxide which was then subsequently etched by cyclic HF/DI water rinses. This method was found to be the most consistent at etching the native oxide as other methods would sometimes not uniformly etch across the whole sample when measured by ellipsometry at various points across the sample. If the acetone step is missed, then sometimes the HF dips don't etch the surface at all meaning that this step is important for consistent etching results.

2.2 Atomic Layer Deposition

2.2.1 The ALD Process

Atomic layer deposition is similar to chemical vapour deposition but the film is achieved by a sequential, self-saturating reaction. The method was first used for commercial use by Suntola et al [40] in the 1970's and was then known as atomic layer epitaxy. This use was for creating uniform thin films for use in Thin Film Electroluminescent Displays. The process has since become of great

interest to the semiconductor industry due to the very desirable properties of the films.

It was then later popularised in the semiconductor industry in DRAM fabrication and later when in 2007 it was used for the deposition of the high-k/metal gate stack for microprocessors [41].

These films can be made to be very thin due to the layer by layer approach that the technique uses, the films are highly conformal and pin-hole free.

The basic operating principle is that the substrate (germanium in these experiments) is exposed to a gaseous precursor which reacts with the surface of the substrate in a self-limiting way, i.e. it reacts with every available surface site on the substrate and then stops reacting because the precursor is specially chosen so that it does not react with itself (Figure 26a). The remaining precursor is then purged out of the chamber (Figure 26b). Once all the initial precursor is out, another gaseous chemical is introduced to the chamber (often water) and this then reacts with the new surface on the substrate, again in a self-limiting way so as to create a stable monolayer (e.g. HfO_2) on top of the substrate (Figure 26c). This second chemical is then purged out of the chamber (Figure 26d) and the resulting surface is accommodating to a reaction with the initial precursor which means that the reaction can be repeated so that one monolayer can be deposited at a time giving great control of the

thickness of the film. A schematic illustration of this process is given in Figure 26.

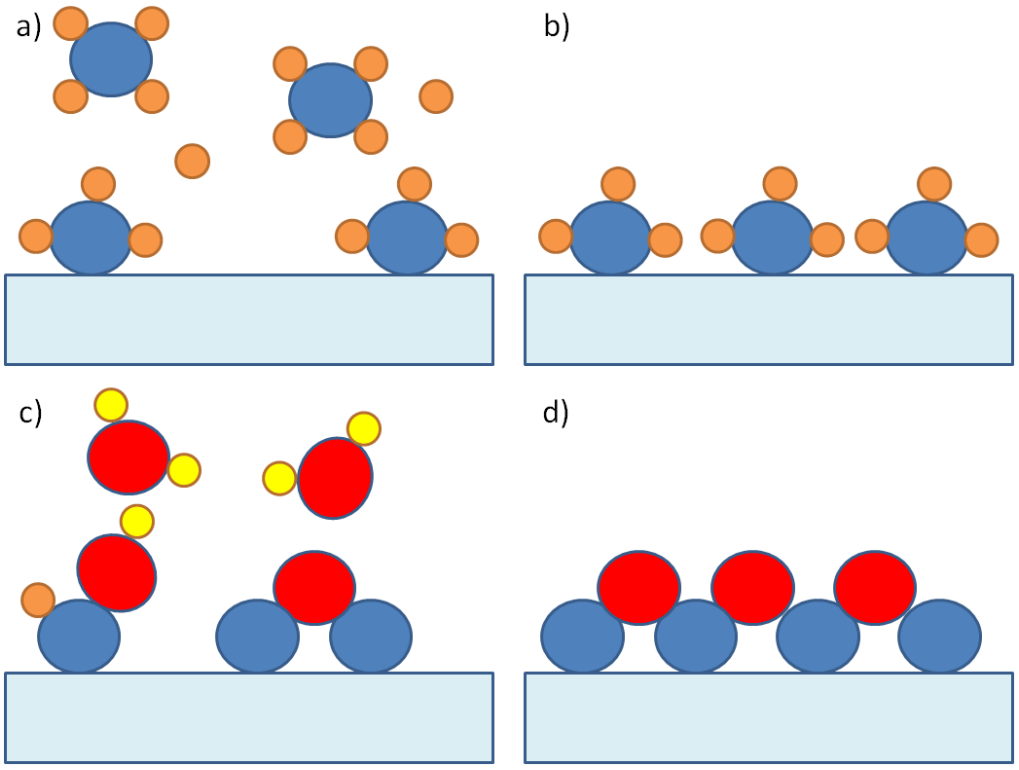

Figure 26. The sequential nature of ALD schematic with a) precursor 1 pulse, b) purge, c) precursor 2 pulse and d) purge leaving a deposited monolayer

This control of the deposition rate gives many advantages over other deposition technologies. The film has a very high degree of conformity due to the fact that the process is self-terminating which means that it can be used for structured surfaces (e.g. trenches). The nature of the process makes it pinhole free which is advantageous for passivation layers and dielectrics. The process is very repeatable and can be scaled up relatively easily which is why it

has become used in manufacturing. The single monolayer deposition per cycle is an ideal case and usually does not happen and the deposition is only a fraction of a monolayer per cycle. The main reason for this is steric hindrance which is where active surface sites are obscured from the reactive precursors by the ligands of adjacent reacted precursor molecules.

The choice of precursors is very important and there are some precursor properties that are essential for ALD growth. The precursors must be volatile because the precursors are delivered to the substrate in the vapour phase. If the precursor has insufficient volatility at room temperature, then it needs to be heated but not to the extent that the precursor thermally decomposes which is one of the reasons that precursor choice and the processing conditions are so important so that high quality films can be fabricated. If the precursor is too thermally unstable then decomposition can occur at the substrate causing impurities in the film which will degrade the film properties. If the precursor is volatile, then the precursor can be delivered to the chamber by vapour draw where the valve to the precursor is opened and the pressure of the precursor means that it will readily come out of the bubbler in a vapour and flow to the chamber. If the precursor is less volatile, then it should be bubbled. This means that the pot containing the precursor has a dip leg in it which an inert gas such as argon flows through. This gas then flows through the precursor and out of the pot into the chamber and it picks up some of the

precursor with it and delivers it to the chamber. The different growth mechanisms are shown in Figure 27.

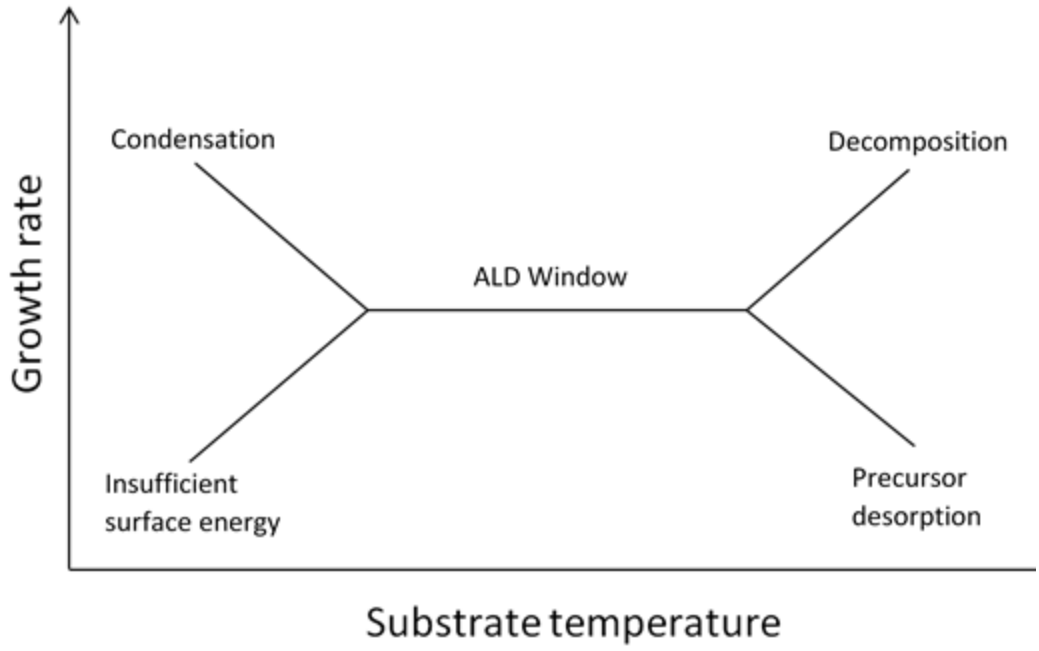

Figure 27. ALD growth rate against *substrate temperature*

If the temperature is too low, then two things can happen:

1. The growth rate is less than expected due to there not being enough surface energy to facilitate to reaction.

2. The growth rate is more than expected due to the precursor condensing on the substrate

There is then a region known as the ALD window where the growth rate remains constant with increasing substrate temperature which is characteristic

of the self-limiting nature of ALD. If the substrate temperature is further increased, then two things can happen:

1. The growth rate rises which is caused by the thermal decomposition of the precursor so therefore causes impurities in the film.

2. The growth rate falls as the precursor desorbs from the surface which makes the process no longer saturative so more cycles are necessary to reach a desired thickness.

The purge time is also an important part of the ALD process as if insufficient time is allowed for all the previous precursor to be removed from the chamber then the next precursor pulse could react with any remaining precursor causing a CVD like reaction allowing less control of the growth rate.

The hafnium precursor used in this study for HfO_2 deposition was $(MeCp)_2Hf(OMe)(Me)$ due to Cp (cyclopentadienyl) based precursors having good thermal stability and low levels of impurities [42]. The precursor bubbler was set to 100^{o}C. Titanium isoproproxide was used as a precursor for TiO_2 deposition due to its extensive use in industry. The bubbler was set to 50^{o}C. Trimethyl Aluminium was used for Al_2O_3 as this is extensively used precursor so is the standard for depositions using aluminium.

2.2.2 The Opal Reactor

These studies use an Oxford Instruments OpAL reactor for ALD depositions and a schematic of the OpAL reactor is shown in Figure 28 [43].

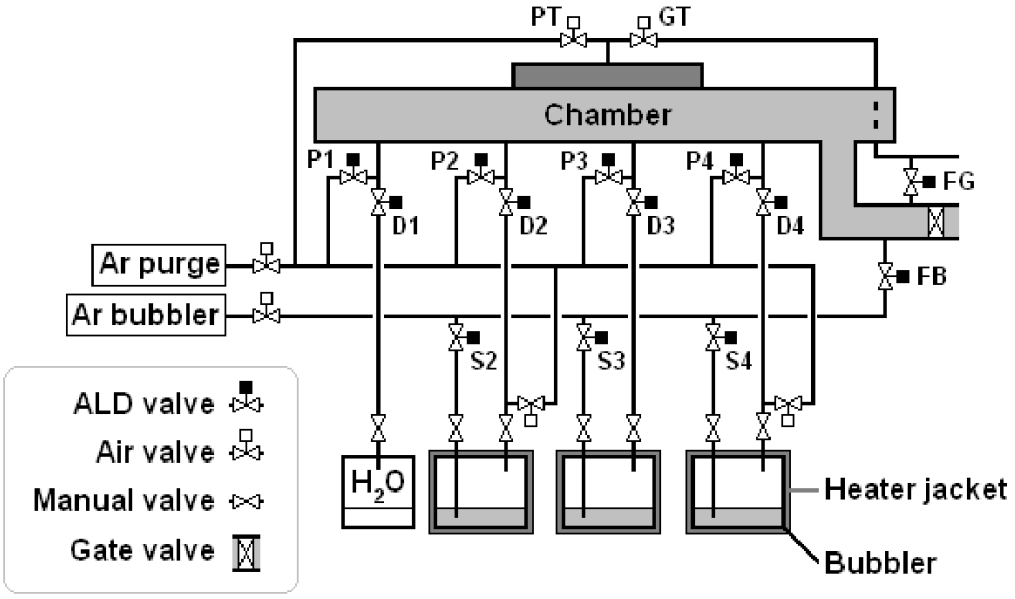

Figure 28. OpAL reactor schematic [43]

2.2.3 Thermal Deposition of Oxides

H_2O can be used as the oxidising species in ALD. As H_2O has a high vapour pressure it can be delivered by vapour draw. The pulse time for TMA was 0.01s and the water pulse was 0.03s and vapour draw was used as the vapour pressure was high enough that bubbling was unnecessary. Both the $(MeCp)_2Hf(OMe)(Me)$ and titanium isoproproxide were bubbled using argon and the pulse was for 3s.

2.2.4 Plasma Enhanced Deposition of Oxides

Another way of delivering oxygen to the film is to use an oxygen plasma. The OpAL reactor uses a remote inductively coupled plasma in a downstream configuration. This is used as it has been reported that films that are grown where the substrate is immersed in the plasma have high levels of plasma induced damage making this method unsuitable for delicate microelectronics where this damage would impact device performance. By using a remote plasma this plasma induced damage is reduced so that it can be used as a method for depositing layers within delicate structures. The oxygen plasma used was at 300W with 60sccm of O_2 flowing for 3s.

2.3 Molecular Beam Epitaxy

MBE is a deposition technique that can achieve very pure and conformal thin films with monolayer resolution and a high degree of control over doping or composition. It is widely used in industry due to its desirable film deposition properties.

MBE uses very pure material sources (e.g. Al) and then heats the source until they slowly sublime. A shutter is placed in front of the source before deposition and the MBE system needs to have an ultra-high vacuum (UHV) because the material being deposited, in this case Al, will be arriving at the target substrate in atomic form and therefore needs a long mean free path so

that it does not interact with any impurities in the chamber. Once the substrate is in the chamber and the requisite vacuum level has been reached the shutter on the Al source is opened for however long is necessary for a certain thickness (typical growth rates are Å/s). This growth is often measured in situ by RHEED analysis so that atomic control of thickness can be attained. MBE was used in this research so that germanium wafers could be cleaned by heating the germanium in UHV leaving an oxide free surface which then had Al metal deposited to try and avoid regrowth of GeO_x when transferring to the ALD reactor ex situ.

2.4 Metal Gate and Back Contact Deposition

To reduce the series resistance of the MOS structure the back of the wafer is coated in Al. First the back is scratched using a diamond scribe and then aluminium is deposited by thermal evaporation to create an ohmic contact. This is performed otherwise the electrical characterisations are effected by essentially having another capacitor in series on the back of the substrate which also creates series resistance. The top gate contact of the MOS device was formed either by evaporating or sputtering of gold through a shadow mask.

2.5 Physical Characterisation

2.5.1 Ellipsometry

Ellipsometry is an optical technique for finding the optical constants of a thin film. The film thickness is also measured. The technique works by comparing the polarisation of light incident on the film and the polarisation of light that is reflected from the film. The polarisation of the light that is reflected from the film depends on the film properties. If light of known polarisation is incident on the film, the reflected light will be elliptically polarised. The ellipsometer measures two values of the reflected light which are Ψ and Δ. Ψ is the ratio of the amplitude of the incident and reflected light, Δ is the phase shift of the reflected light. These values are the used with the Fresnel equations for polarised light. Fresnel's equation is given by

$$p = \frac{r_p}{r_s} = tan\Psi e^{i\Delta} \qquad \text{Eq.16}$$

Where p the polarisation, r_p and r_s are the complex Fresnel reflection coefficients.

The measurements were taken using a Horiba Jobin Yvon spectroscopic ellipsometer which has a wavelength range of 450-750nm with the angle of incidence of 70°. A model was set up using reference materials in the software to fit the Ψ and Δ to measure the thickness of samples. The different material parameters that can be acquired using the spectroscopic ellipsometer are the thickness of the layers, optical properties of the layers, composition, uniformity and surface roughness.

A single wavelength ellipsometer (Rudolph Auto EL-IV ellipsometer) was also used which had to be reprogrammed for use with germanium. The frequency of light used was 632.8nm and the germanium parameters were set with the refractive index as 5.39 and the extinction coefficient as 0.69 for the germanium substrate. The refractive index of the GeO_2 was set as 1.674.

2.5.2 XPS

X-Ray Photoelectron Spectroscopy is a surface sensitive technique whereby the composition of a material can be investigated as well as the nature of the chemical bonding present. The general operating principle behind it is to make use of the photo-electron effect by irradiating a given material with x-rays of a known wavelength and this will cause photo-electrons to be emitted from the surface of the material. These photo-electrons have a specific kinetic energy that is determined from the binding energy of the electron before it was emitted and the energy of the x-ray that liberated it. This binding energy is specific to each energy level within an element and gives off a characteristic spectrum of binding energies. The chemical bonding can also be measured by the changes in the shape and position of a particular binding energy peak.

Band offsets are measured using Krouts method [44] which involves measuring the difference in binding energy of core level peaks and valance band maximum. Equation 17 shows the relationship between these values and how they give the valence band offset for a film on a substrate.

$$\Delta E_V = \Delta E_{CL} + (E_{CL} - E_{VBM})^{Sub} - (E_{CL} - E_{VM})^{Film} \qquad \text{Eq.17}$$

where $\Delta E_{CL}$is the difference in the core level peaks of the substrate and the film, E_{CL} is the core level peak position and E_{VBM} is the valance band maximum.

This means an evaluation of the band structure of a MOS device can be determined and whether the band offsets are sufficient to prevent carrier injection across the structure which would degrade the device performance in the form of high leakage currents.

XPS was used in this study to investigate the surface bonding conditions of germanium and to calculate band offsets according to Krouts method. A correction to the binding energies was used where the XPS scans are calibrated to adventitious carbon at 284.6eV and peak fitting was done using OriginPro 9 software with a Shirley background correction.

2.5.3 XRD

X-Ray Diffraction is a technique that can give information about the crystal phase of a sample as well as various other material properties. The general principal is that an incoming x-ray beam is incident on the sample and these x-rays are scattered by the atoms in the sample under investigation. For a crystalline solid, there is destructive interference of the x-rays in almost all directions but in a small number of directions there will be constructive

interference and these beams of x-rays will leave the sample in very specified and characteristic directions.

If two x-rays are incident on two lattice planes in the crystal, then the maximum signal that is diffracted back from the sample is when the distance between the two planes is an integral number of wavelengths of the incident beam. This relationship is shown in equation 18 which is Bragg's Law.

$$2dsin\theta = n\lambda \qquad \text{Eq.18}$$

Where d is the spacing between the two planes, θ is the incident angle of the x-rays, n is an integer and λ is the wavelength. This equation shows that the unit cell dimensions of the crystal lattice which are used to determine the parameters of the sample. A schematic of the experimental set up is shown in Figure 29.

XRD was used in this study to investigate the crystallinity of deposited films before and after annealing. A Rigaku Miniflex diffractometer was used for the measurements in this study.

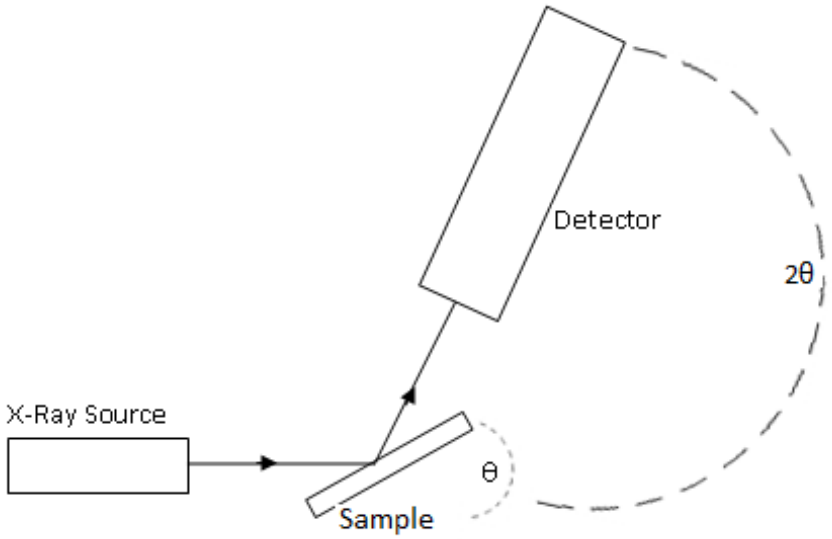

Figure 29. The experimental set up for x-ray diffraction. 2ϑ is the measured angle as the detector moves twice as far as the sample

2.5.4 TEM

Transmission Electron Microscopy is a powerful imaging technique that can give atomic resolution. The microscope works on the same basic principles as optical microscopes but instead of using light to investigate a sample it uses electrons. TEMs have a much better resolution than optical microscopes due to optics that are limited by the wavelength of light whereas TEMs use electrons and these have much smaller wavelengths. The electrons are accelerated towards the sample and are focused using magnetic lenses to form a narrow beam of electrons which are incident on the sample. Cross sectional transmission electron microscopy (XTEM) was carried out on an aberration corrected JEOL 2100 FCs microscope, which used an operating

voltage of 200 kV during the analysis. The sample is prepared by mechanical polishing and then preparing an area by ion beam milling to be electron transparent so that the electrons can pass through and are scattered on to a screen which can detect these electrons and then an image can be deduced from the pattern on the screen. TEM was used in this study to investigate the thickness of deposited films and any interfacial layer between deposited films and the substrate.

2.6 Electrical Characterisation

2.6.1 Capacitance-Voltage

Once the samples have been prepared into a MOS capacitor the capacitance measurements are taken by placing the samples into a probe station when the base is one contact and a needle is placed onto the top metal contact of the MOS device. The measurements are taken by performing a DC voltage sweep which has an AC current superimposed on it. This AC current is set to 50mV and the frequency is varied from 1 kHz to 1MHz. A voltage sweep is performed as a build of charges in the device can be present that would distort the C-V readings. Once this is done C-V measurements are performed by measuring from negative to positive bias and then held at a positive bias for 10s followed by a positive to negative bias sweep. This is to let all the charge be built up or deplete at the semiconductor/dielectric interface so that the measurements are not effected by previous sweeps as it could make it appear that there is a

low frequency response (see Figure 6) when there isn't. The measurements were carried out in a light proof box to minimise any carrier generation through optical excitation which again could cause it to appear to have a low frequency response when there isn't.

These measurements were used to characterise the gate stacks in terms of EOT, frequency dispersion and D_{it}. The measurements were carried out with an Agilent E4980A LCR meter.

2.6.2 Current Voltage

Current voltage measurements were carried out using Kiethley 230B voltage source and Kiethley 617B Electrometer. The MOS capacitor is left at zero bias to begin with until the current reading reaches a minimum so as to let any build-up of charge dissipate from the structure before beginning the measurements. A voltage sweep is then carried out where the voltage is varied in increments with a delay time in between the measurements. The current read off is the leakage current and values are taken at +/- 1V to compare to the literature values and determine if the gate stack structures have a low enough leakage current to be applicable for high performance CMOS technology.

3. Growth of Al_2O_3 and (Ti-doped) HfO_2 on Silicon

The growth of Al_2O_3 and HfO_2 on silicon by ALD was characterised in terms of growth rate. The reason silicon was used is that is much less expensive than germanium as a substrate and the Si/SiO_2 system is well understood which makes the thickness and electrical characterisation more straightforward. The effect of doping the HfO_2 with Titanium was then investigated to increase the dielectric constant of the HfO_2 films to increase the suitability when attempting to scale down the EOT of gate stacks in high performance CMOS. The films were characterised in terms of growth rate, XRD, TEM, CV and IV. All the ALD growths were carried on an Oxford instruments OpAL reactor using TMA as the Al precursor, $(MeCp)_2Hf(OMe)(Me)$ as the Hf precursor, titanium isoproproxide as the Ti precursor and either H_2O or oxygen plasma as the O precursor. The pulse time for Al and H_2O was 0.1s and the pulse time for Hf and Ti was 3s unless otherwise stated.

3.1 Al_2O_3 Growth on Silicon

3.1.1 Thermal Growth Of Al_2O_3

The growth of Al_2O_3 was carried out thermally at various temperatures on silicon to characterise the growth parameters. Figure 30 shows the thickness of the Al_2O_3 for 100 cycles of TMA and H_2O between 150^oC and 300^oC where the thickness was measured by ellipsometry.

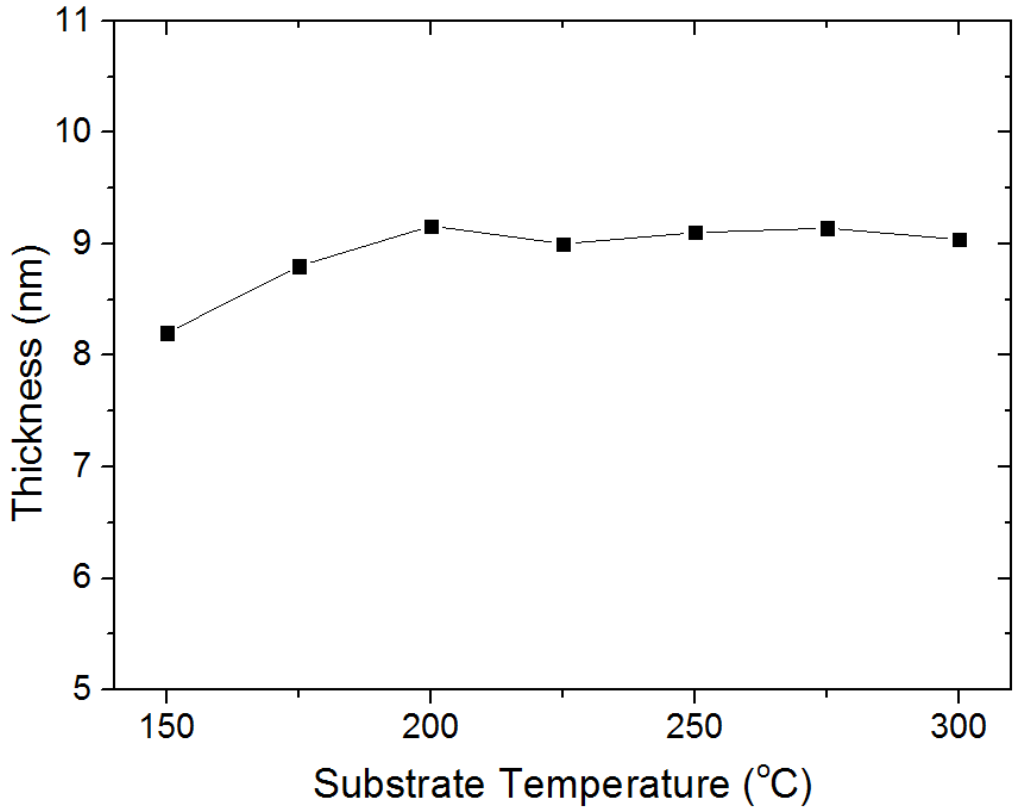

Figure 30. The variation in Al_2O_3 thickness as a function of temperature

This shows that there is an increase in the growth rate from 150°C to 200°C and then the growth rate plateaus up to 300°C. This is expected as there is an increase in surface energy meaning a higher proportion of the surface has sufficient energy to facilitate the ALD reactions until it reaches the ALD temperature window as shown in Figure 27.

3.1.2 Plasma Growth of Al_2O_3

The growth of Al_2O_3 was carried out using an oxygen plasma at various temperatures on silicon to characterise the growth parameters. Figure 31

shows the thickness of the Al_2O_3 layers for 100 cycles between 150°C and 300°C.

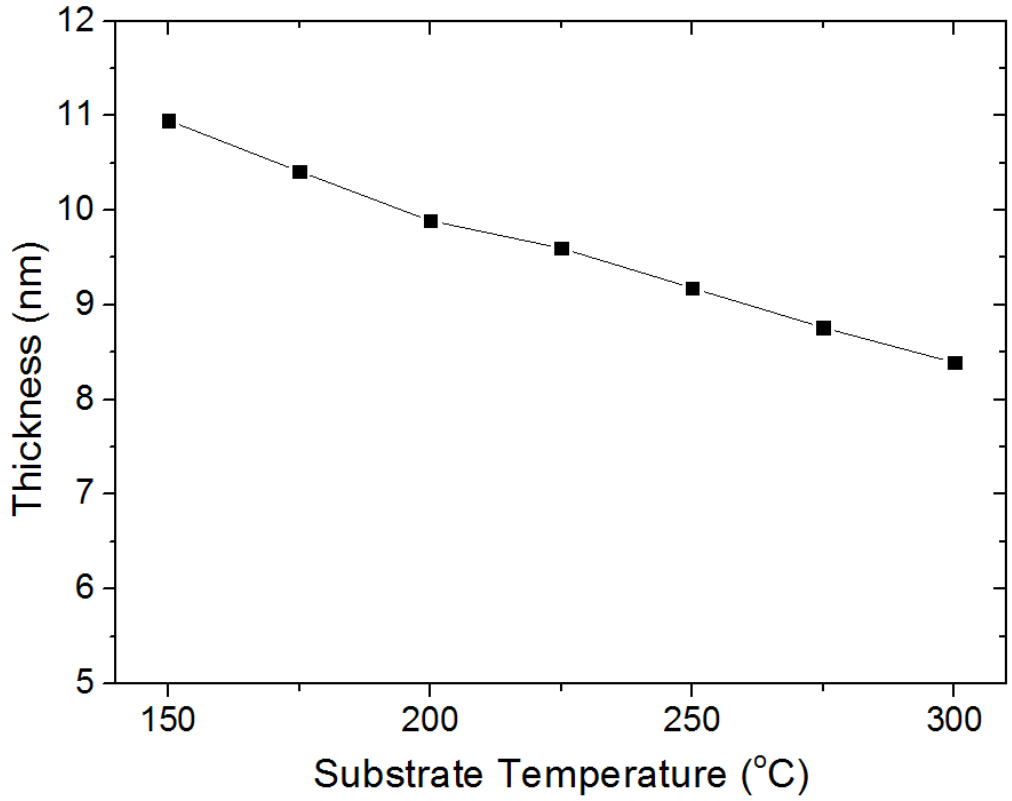

Figure 31. The variation in Al_2O_3 thickness as a function of temperature

This shows a steady decrease in growth rate throughout the temperature range. This could be due to the film becoming denser with an increase in temperature or the plasma process provides more energy which causes the precursor to desorb from the surface therefore lowering the surface coverage.

3.2 HfO_2 Growth on Silicon

3.2.1 Thermal growth of HfO_2

HfO_2 was grown using H_2O as the oxidising species in the ALD process. The pulse length of the hafnium precursor was varied to find the optimum time for a complete cycle to take place but not longer than necessary so as not to waste the precursor. The growth rate against pulse length for HfO_2 is shown in Figure 32 and at various temperatures.

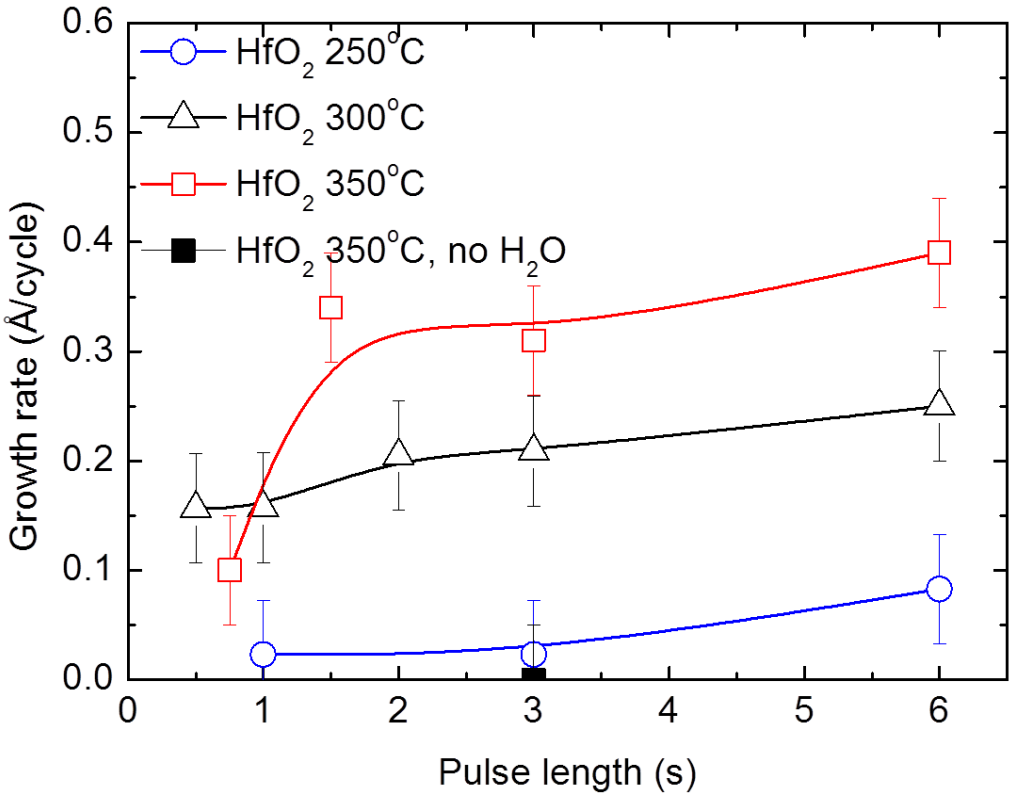

Figure 32. Growth rate against pulse length for HfO_2 at different temperatures

The graph shows that there is very little growth at 250^{o}C meaning that there is not enough surface energy available for the reaction to take place. As the temperature is increased the growth rate increases as well but at 300^{o}C there is a higher growth rate for lower pulse times than at 350^{o}C which then changes around as the pulse time is increased. This is due to the precursor condensing on the surface at 300^{o}C but not at 350^{o}C with the lower growth at 350^{o}C attributed to insufficient precursor being delivered to the sample. The optimum deposition temperature is therefore found to be 350^{o}C and the precursor is seen to be thermally stable because when there was no water pulse there was no growth.

3.2.2 Plasma enhanced growth of HfO_2

Growth against oxygen plasma pulse time is shown in Figure 33. This shows an increase in growth up to 3s after which the growth rate only increases slightly up to 6s. This means that 3s is sufficient for an effective ALD process. The plasma power was varied to see how this effects the growth rate and this is shown in Figure 34.

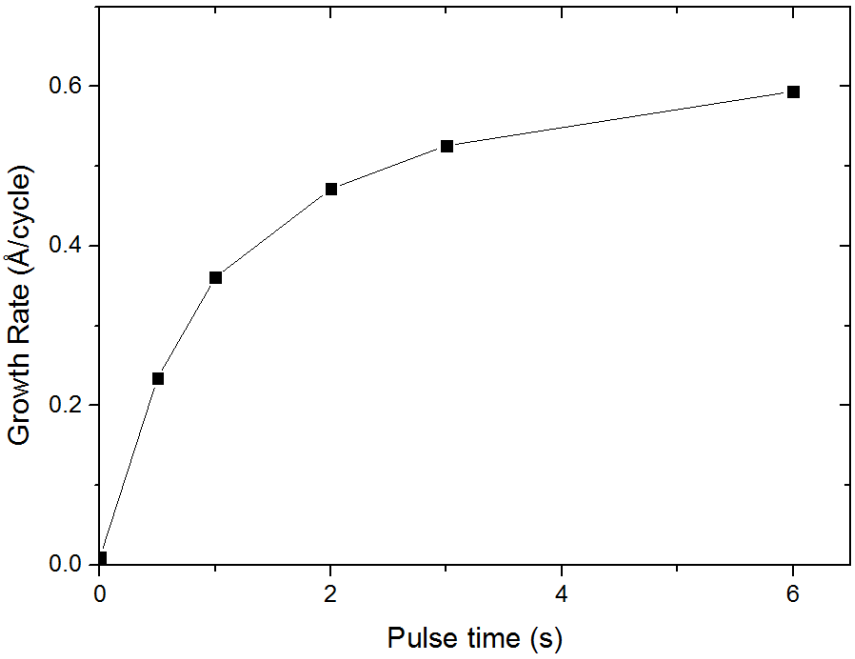

Figure 33. Growth rate against oxygen plasma pulse time for HfO_2 deposited at 250°C

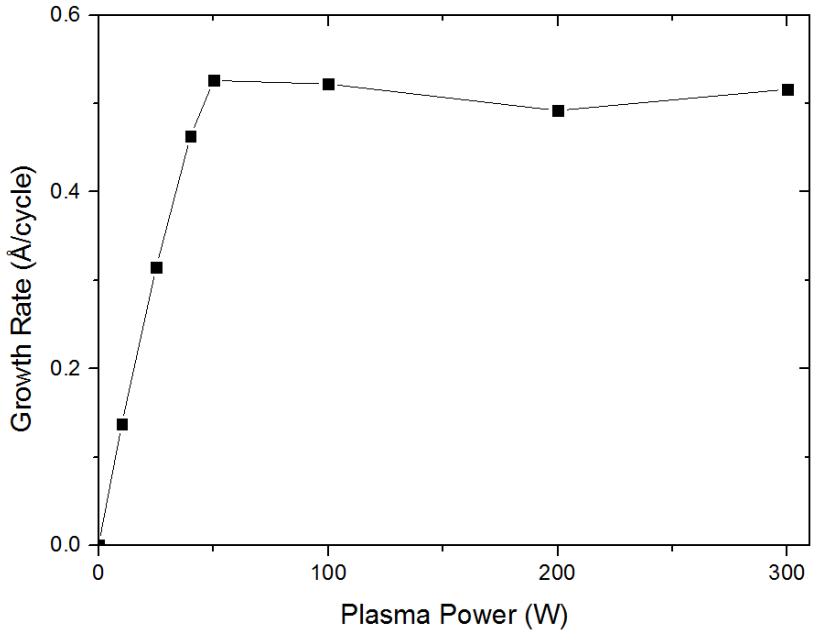

Figure 34. Growth rate against oxygen plasma power for HfO_2 deposited at 250°C

This shows that the growth rate stays fairly uniform above 50W but drops off with a lower plasma power than 50W meaning at least 50W is required for an efficient growth process.

3.3 Ti-doped HfO_2

3.3.1 Growth Characterisation

To improve the dielectric constant of HfO_2, titanium was introduced as a dopant. TiO_2 has a very large dielectric constant of 50-60 [45] but for use on germanium the conduction band offset is very small meaning that the leakage current is high [46]. For this study silicon was used as the substrate with a 2nm native SiO_2 layer. Depositions were carried first for the HfO_2 and TiO_2 separately at a range of temperatures to investigate the growth behaviours. Figure 35 shows the growth rate against pulse length for TiO_2 deposited at a range of different temperatures and from this the optimum deposition temperature was found to be 250^{o}C with a growth rate of 0.17Å/cycle. This is due to the growth staying constant with increasing pulse length which indicates that the film is growing in an ALD manner and any increase in the temperature causes an increase in growth rate due to thermal decomposition of the precursor. Growth occurred even when there was no H_2O present which further confirms the thermal decomposition of the Ti precursor.

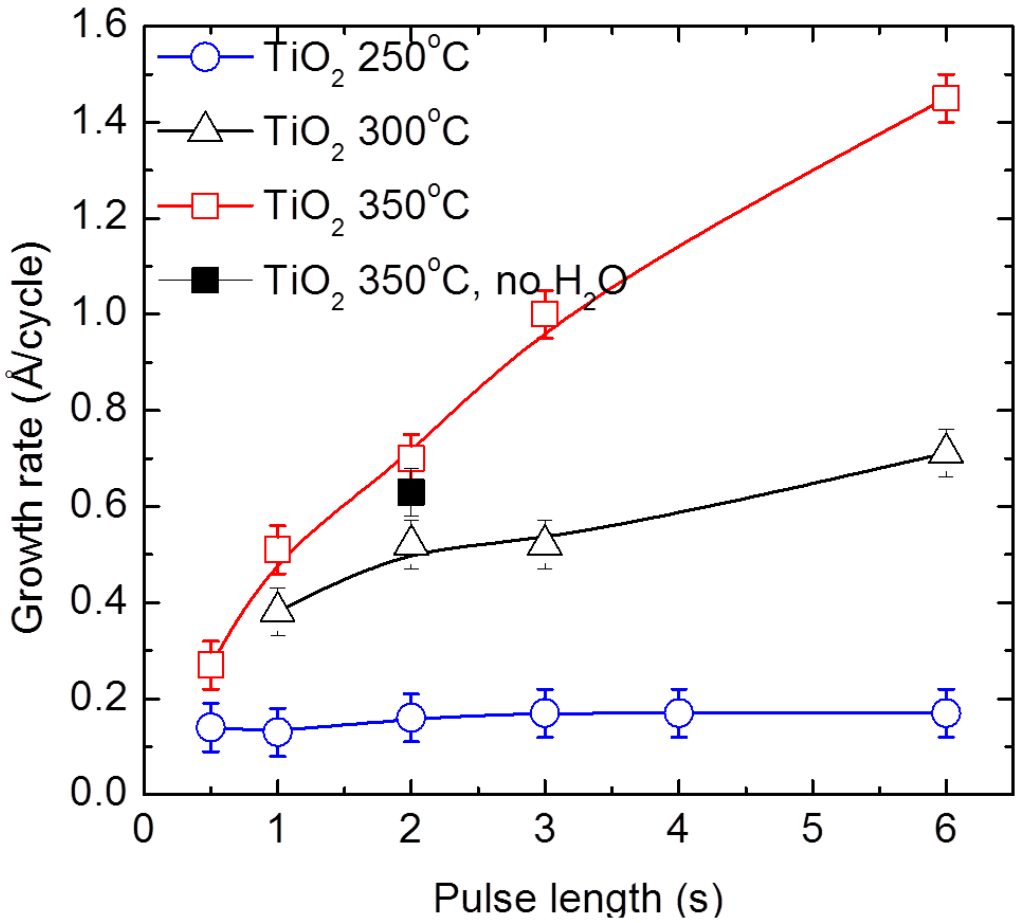

Figure 35. Growth rate against pulse length for TiO_2 at different temperatures

From the data in Figure 32 and Figure 35 a compromise temperature was used at 300°C even though at this temperature there is a chemical vapour deposition (CVD) component to growth from the Ti precursor with a growth rate of 0.52Å/cycle and the growth rate of the Hf precursor is lower than its optimal value at 0.21Å/cycle.

To achieve films with 10% and 50% doping levels of titanium, ratios of (23 Hf ALD cycles):(1 Ti ALD cycle) and (5 Hf ALD cycles):(2 Ti ALD cycles) were used.

These films were given a N_2 spike anneal at 850^oC or a 30 minute anneal at 500^oC to simulate the thermal budget of device processing.

The growth was lower than expected for these films and this is likely to have been from an etching effect due to either the Hf precursor etching Ti-O or the Ti precursor etching the Hf-O. The composition of the films was unchanged (medium energy ion scattering was carried out to confirm this, data not shown).

3.3.2 XRD of (Ti-doped) HfO_2

XRD was carried out to investigate the crystallinity of the films and both films were amorphous when as deposited but the 10% Ti doped samples crystallised under both types of annealing conditions suggesting that the doping has not significantly change the crystallisation properties of the HfO_2 film. The 50% Ti doped samples showed no peaks in the XRD spectre after annealing which means that if there is any crystallite growth then they are small enough so that there is a tendancy towards the film being amorphous and this is shown in Figure 36.

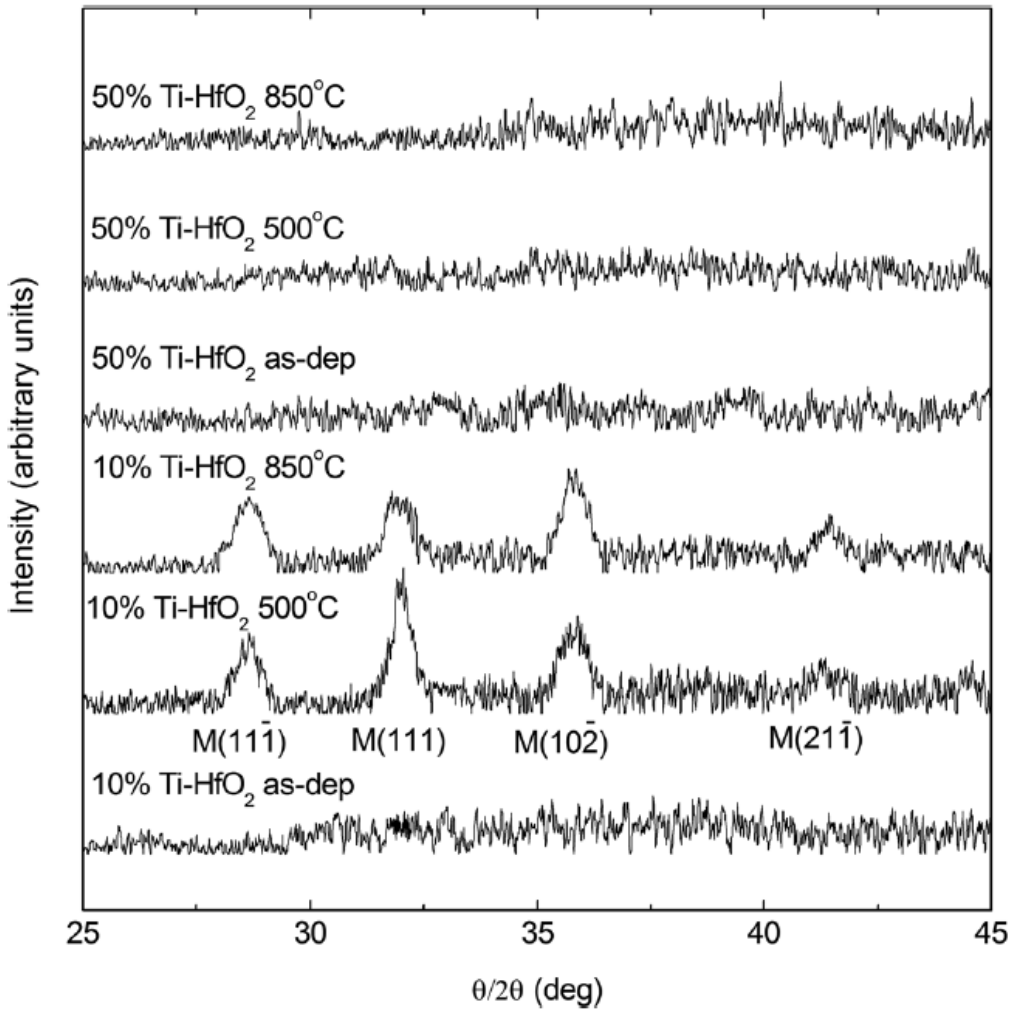

Figure 36. XRD spectra showing the crystallisation of the 10% Ti doped film for both types of annealing in contrast to the 50% doped films remaining amorphous

3.3.3 Electrical Characterisation

Electrical characterisation found that the undoped HfO_2 film had a dielectric constant of 17 and this was raised to 20 for the 10% Ti doped sample and to 35 for the 50% Ti doped sample. Annealing the samples caused the dielectric constant to fall to 27 for the 50% Ti doped sample after a 30 minute 500°C

anneal and to 22 for the 850°C spike anneal both of which are improvements on the undoped HfO_2 films. These characteristics are shown in Figure 37. Leakage current density was also found to be comparable between the 50% Ti doped films and the undoped films as shown in Figure 38 which indicates that the films remain an effective barrier to carrier injection across the structure.

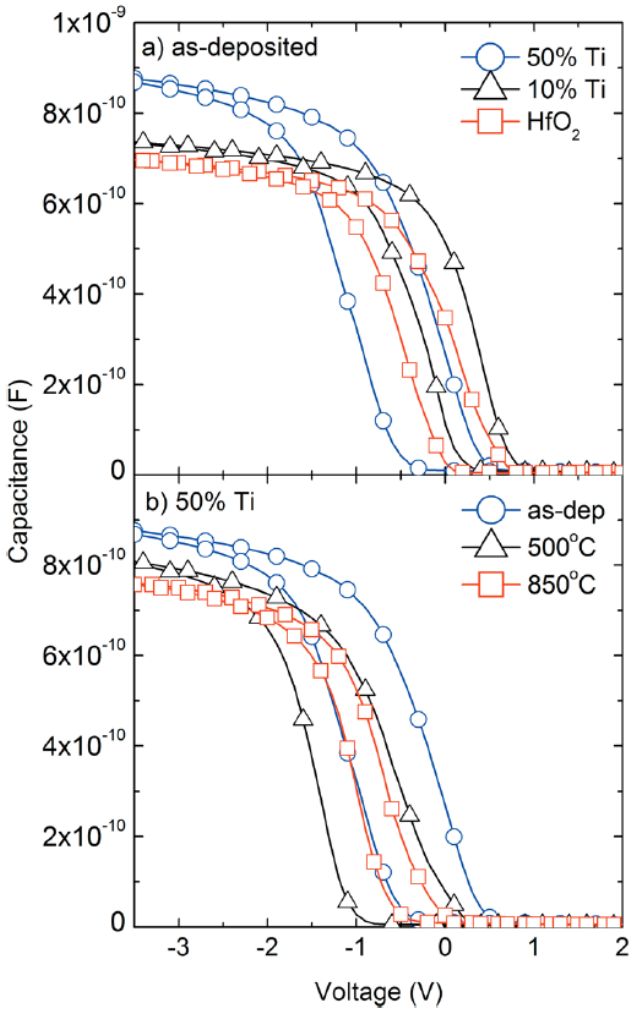

Figure 37. C-V measurements showing the change in capacitance arising from the difference in dielectric constant and the reduction in this (as indicated by lower capacitance) when annealed

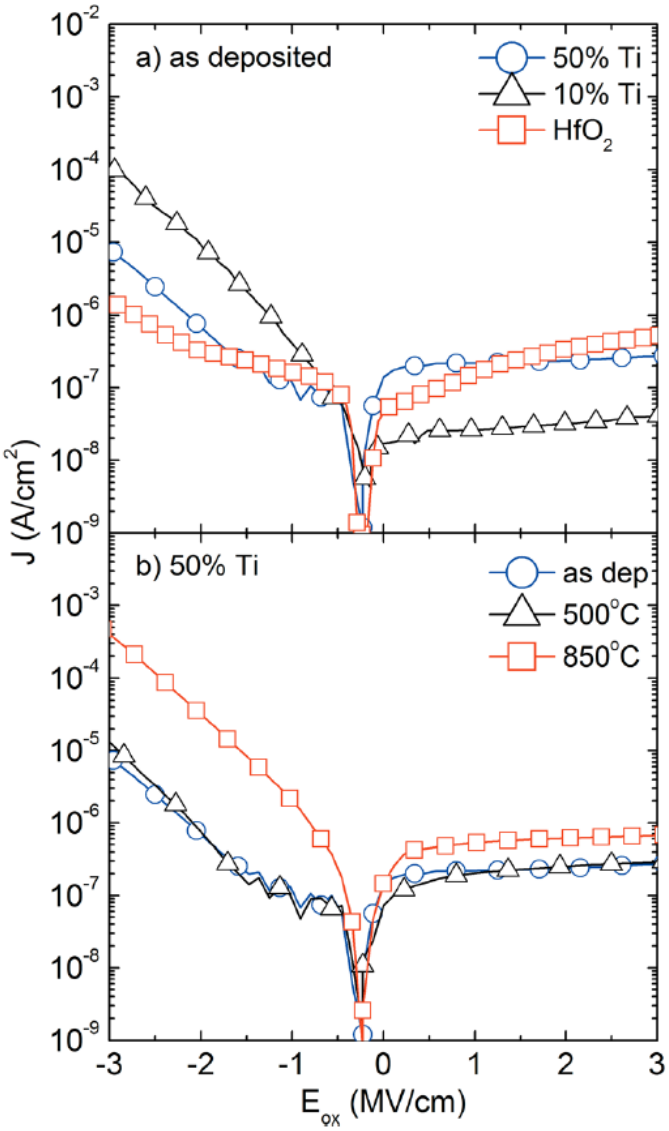

Figure 38. IV leakage measurements for the Ti doped HfO_2 films

3.4 Chapter Summary

Growth was carried out on silicon of Al_2O_3 and HfO_2 to determine the growth characteristics of these films. Ti-doped HfO_2 was investigated to increase the dielectric constant of HfO_2. This was successfully carried out and the dielectric

constant was increased to 35 for the 50% doped sample although this then reduced upon annealing. The leakage current was found to be satisfactory even with this increase in dielectric constant. The inclusion of Ti also caused the film to have the appearance of remaining amorphous after a spike anneal at 850^{o}C. These mean that Ti-doped HfO_2 is a suitable high k dielectric for EOT scaling in CMOS devices. Triyoso et al [47] found that when depositing Ti-doped HfO_2 by ALD (using $HfCl_4$ and $TiCl_4$ as the metal precursors) the Ti prevented the crystallisation of as deposited HfO_2 but after annealing the films poly-crystallised (monoclinic for films with less than 10% Ti content and films with 45% Ti content crystallised to the orthorhombic $HfTiO_4$ phase). It is unclear why there is this difference in crystallisation behaviour.

4. Plasma grown GeO_x with HfO_2 cap

To investigate the passivation of germanium a GeO_x layer was grown on germanium by exposing the surface to an oxygen plasma with a HfO_2 layer on top to protect the GeO_x from moisture in the atmosphere. These gate stacks were characterised by XPS to confirm the growth of GeO_x. CV analysis was used to investigate the effect of employing an Al back contact and the effect of forming gas annealing.

4.1 Growth

P and n type Ge (100) wafers with a resistivity of 0.3-3Ωcm were prepared by a cyclic HF/deionised (DI) water rinse. This consisted of first rinsing in DI water for 30s to remove the native GeO_2 layer, the sub-oxides are resistant to etching by water so the Ge was then rinsed in 4% HF solution for 30s then 30s rinse in DI water. This HF/DI cycle was then repeated five times to try and make sure that the majority of the oxide was removed leaving a sub 0.5nm layer.

The samples were then transported to the ALD chamber whilst submerged in acetone so as to try and avoid re-oxidation before the deposition process. The cleaned samples were exposed to an oxygen plasma at a pressure of 100mTorr at 250^{o}C for either 30mins or 60mins. A control sample without plasma exposure was also prepared. The subsequent HfO_2 deposition was performed at 250^{o}C in an Oxford Instruments OpAL reactor using $(MeCp)_2Hf(OMe)(Me)$ as

the hafnium precursor and an oxygen plasma as the oxidising precursor. The cycle follows the pattern of hafnium precursor pulse, then purge and an oxygen plasma pulse followed by a purge. The timings for these are 3s/3s/3s/2s respectively. Nominally 5 and 10nm thicknesses of HfO_2 were prepared. Aluminium back contacts were deposited by thermal vacuum evaporation and circular Au contacts with a range of diameters (0.25mm, 0.375mm, 0.5mm, 1mm and 2mm) were also deposited using a shadow mask using the same method and all electrical data shown has been measured using the 0.5mm diameter contact unless otherwise stated. Some samples were also given a post metallisation annealing (PMA) in a nitrogen (VLSI grade) or forming gas (10% H, 90%N) environment at 350^{o}C to reduce D_{it}. Table 3 shows the different sample names and the process that they have undergone.

Sample	Oxygen plasma(Temp/ Time)	Annealing(temp/time/atmosphere)	Thickness(GeO_x/HfO_2)
GeW5S3	250/60	350/30/Nitrogen	3nm/10nm
GeW6S2	250/60	350/30/Forming gas	3nm/10nm

Table 3. Table showing the different processes the samples underwent

4.2 XPS of Plasma grown GeO_x

Figure 39 shows the Ge 3d XPS spectrum peak for Ge exposed to oxygen plasma for 5 minutes.

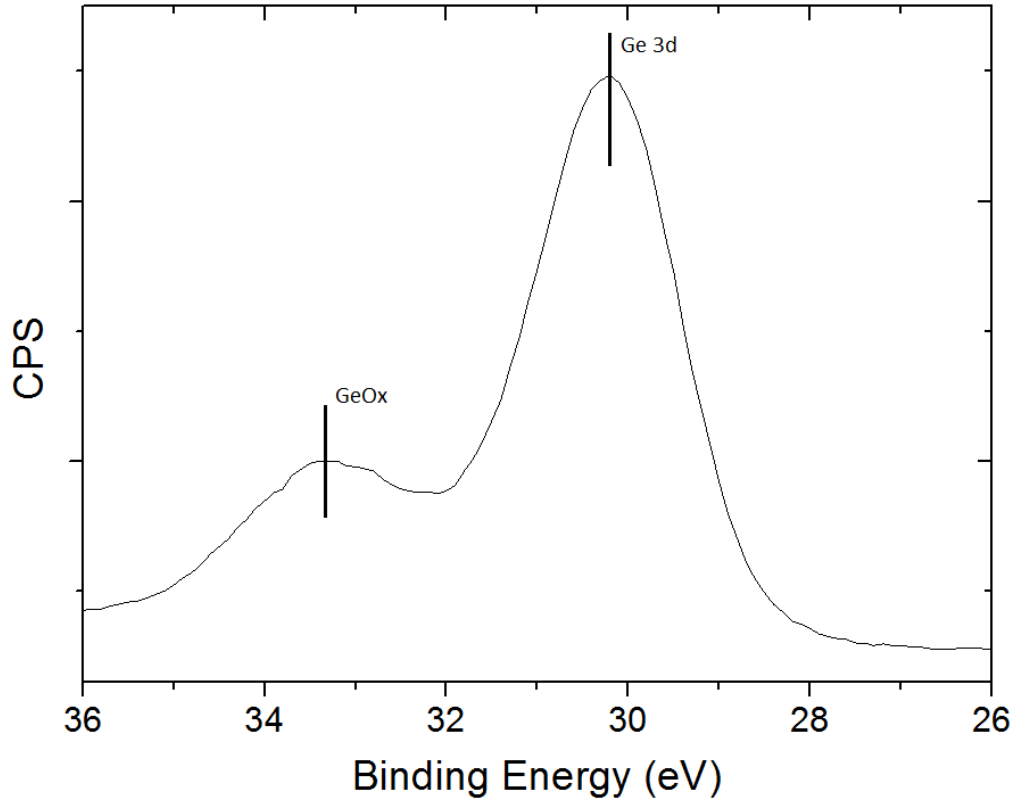

Figure 39. XPS spectrum Ge 3d of plasma grown GeO_x

This shows that there is growth of GeO_x after plasma exposure due to the presence of a peak at a higher binding energy than the main Ge peak. The GeO_x peak is smaller than the Ge 3d peak which suggests that there is not much growth of GeO_x.

4.3 Electrical Characterisation of plasma grown GeO_x/HfO_2 Gate Stack

To investigate the effect of series resistance on the CV measurements, GeW5S3 had the measurements taken before and after aluminium back coating and the results are shown in Figure 40.

As can be seen under positive voltages the frequency dispersion in accumulation is improved as the higher frequency measurements are closer to the lower frequency measurements. This is improved further by a post metallisation anneal in nitrogen shown in Figure 40 e) and f) where the inversion capacitance has also decreased indicating an improvement in the interface quality due to a reduction in the density of interface states. The equivalent oxide thickness (EOT) can be calculated from the CV plot using the lowest frequency (100Hz) in strong accumulation and assuming a dielectric constant of 6 for GeO_2. This EOT was calculated to be 5.6nm and then assuming that the thickness of GeO_2 to be 3nm and the thickness of HfO_2 to be 10nm the dielectric constant of the HfO_2 layer is calculated to be 23. There is some error in this value due to the uncertainty in the thicknesses of the layers.

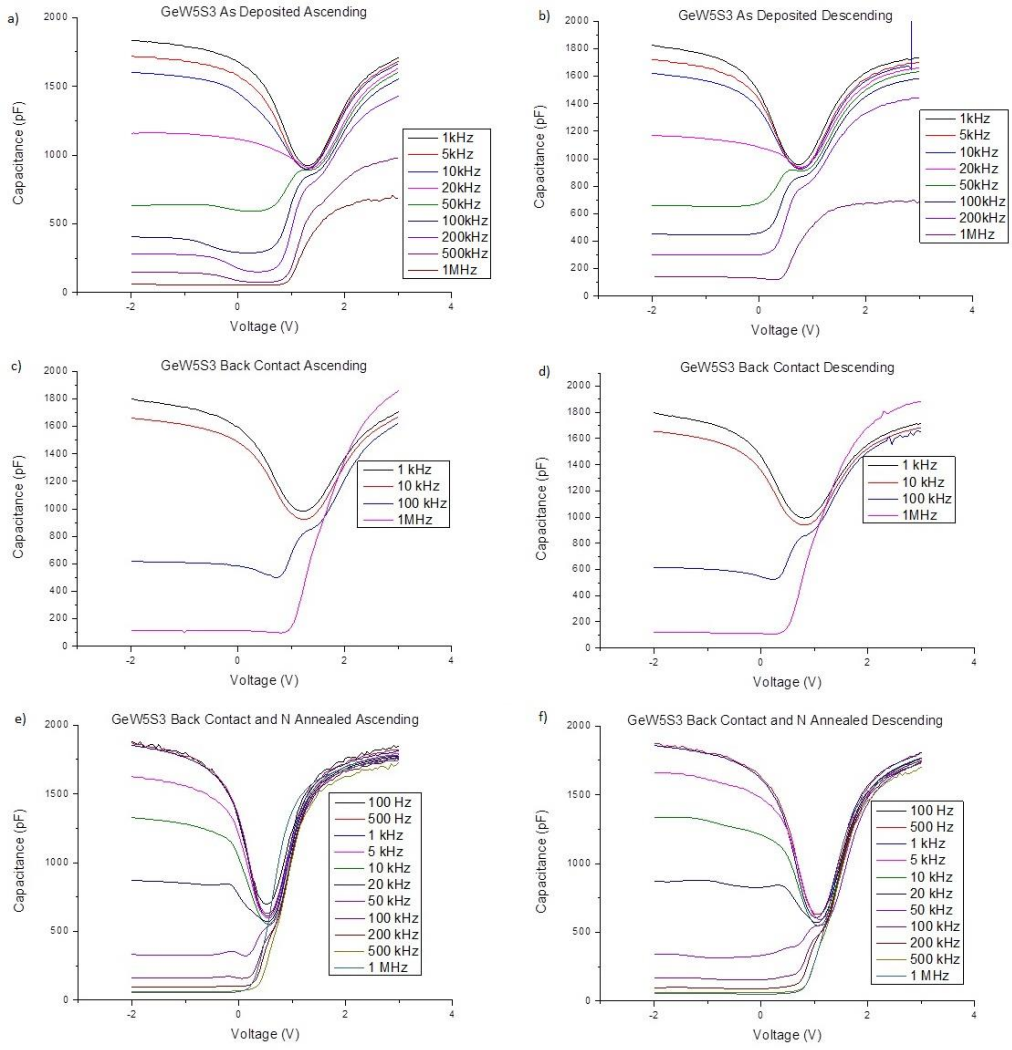

Figure 40. CV as a function of frequency results on GeW5S3 with a) and b) as deposited, c) and d) with an Al back contact and e) and f) after a nitrogen anneal at 350°C for 30 minutes. Ascending indicates the voltage sweep going from negative to positive bias and descending indicates from positive to negative

This experiment was repeated with GeW6S2 with a forming gas anneal instead of nitrogen. The accumulation capacitance both before and after annealing

was lower in this sample than for GeW5S3 which had the same growth procedure and this is likely due to variations in the thickness of the GeO_2 layer. The CV results are shown in Figure 41 for the sample after deposition of an Al back coat and then after a forming gas anneal.

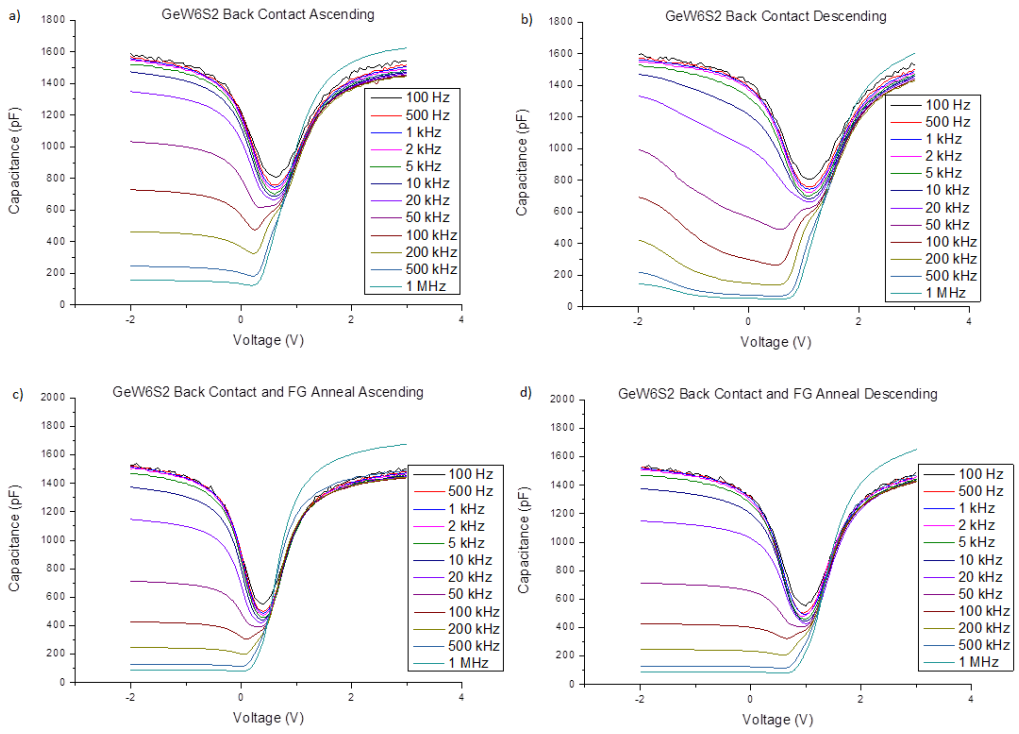

Figure 41. CV as a function of frequency on GeW6S2 with a) and b) as deposited with Al back contact and c) and d) after a forming gas anneal at 350°C for 30 mins. Ascending indicates the voltage sweep going from negative to positive bias and descending indicates from positive to negative

Using the 100 Hz frequency values the EOT can be calculated to be 6.8 and if assuming a GeO_2 thickness of 3nm and HfO_2 thickness of 10nm then the dielectric constant is 15.8 which is probably an underestimate due to the uncertainty in the thickness of the GeO_2. The forming gas anneal also has

greatly improved the CV characteristics when in inversion as they don't saturate at a value before the heat treatment and the inversion capacitance is also reduced which indicates a lower density of interface states.

4.4 Chapter Summary

GeO_x was grown by exposing a clean Ge sample to oxygen plasma. This then had a HfO_2 capping layer. The C-V data showed good characteristics with low stretch out and frequency dispersion in accumulation indicating a low density of interface states. The EOT was found to be too large for CMOS manufacturing due the formation of a ~3nm thick GeO_x layer which has a low (~5-6) dielectric constant. Xie et al [48], [49] found that exposing the germanium surface to an oxygen plasma grew a 1.5nm GeO_2 layer that showed low D_{it} and that O_2 annealing was preferred to forming gas annealing to lower the D_{it} further. This difference in thickness could be due to the different oxygen plasma configurations.

The data shows that using an aluminium back contact reduces the back-contact resistance and that a post metallisation anneal reduces frequency dispersion and lowers the density of interface states which is why it is standard practise to perform these processes on MOS devices.

5. MBE of thin Al with HfO_2 cap

As it has been previously reported that a thin Al_2O_3 layer can be used as a diffusion barrier to stop the desorption of GeO from the interface a method of fabricating a trilayer system using GeO_x/ Al_2O_3/ HfO_2 was investigated. Al_2O_3 as a diffusion barrier has been shown to be effective for use on silicon [50] as well as germanium [15].

5.1 Growth Conditions

Ge (100) wafers with a resistivity of 0.3-3Ωcm with both n- and p-type doping were used in this study. To clean the wafers of the native oxide a thermal cleaning was used by exposing the wafers to an ultra-high vacuum (UHV) ($<10^{-8}$mbar) and heating to 500^{o}C for 10 minutes. At this temperature, the oxide layer is volatile and whilst under UHV conditions will evaporate away leaving an oxide free surface. The samples were then exposed to an aluminium flux for 2s, 5s, and 10s via MBE with an Al cell temperature of 980^{o}C leaving a sub nanometre layer of Al metal. These were then transferred into the load lock of the MBE system and oxidised in air at ambient temperatures. These samples were then transferred to the Oxford Instruments OpAL ALD system where HfO_2 was grown with thicknesses ranging from 1.8 to 7nm using $(MeCp)_2Hf(OMe)(Me)$ as the precursor for hafnium and an oxygen plasma for the oxidising cycle. The temperature for all HfO_2 depositions was 250^{o}C. The ALD timing was 3s Hf pulse/3s purge/3s O plasma/3s purge. Circular gold

contacts were then thermally evaporated to MOS devices with diameters ranging from 250µm to 1000µm using a shadow mask.

These gate stacks were then characterised by XPS, TEM, CV and IV.

5.2 XPS of $Ge/GeO_x/Al_2O_3/HfO_2$

X-ray Photoelectron spectroscopy was carried out on a sample from the Ge wafer that had 10s MBE treatment with 2nm of HfO_2 on top. The results are given in Figure 42 for the aluminium data and in Figure 43 for the germanium 3d data.

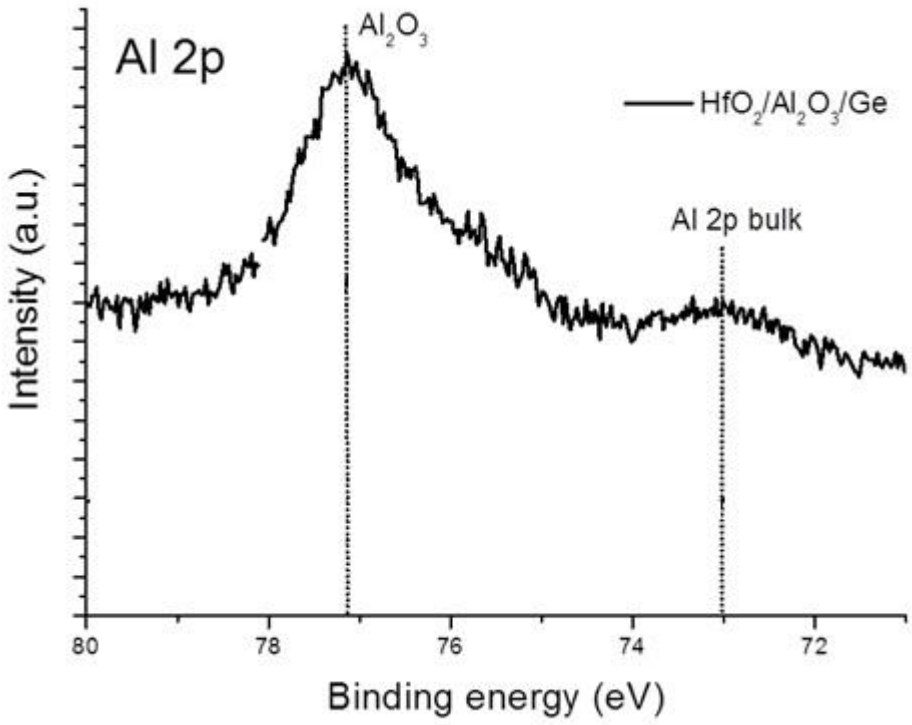

Figure 42. XPS spectrum showing the results centred around Al 2p

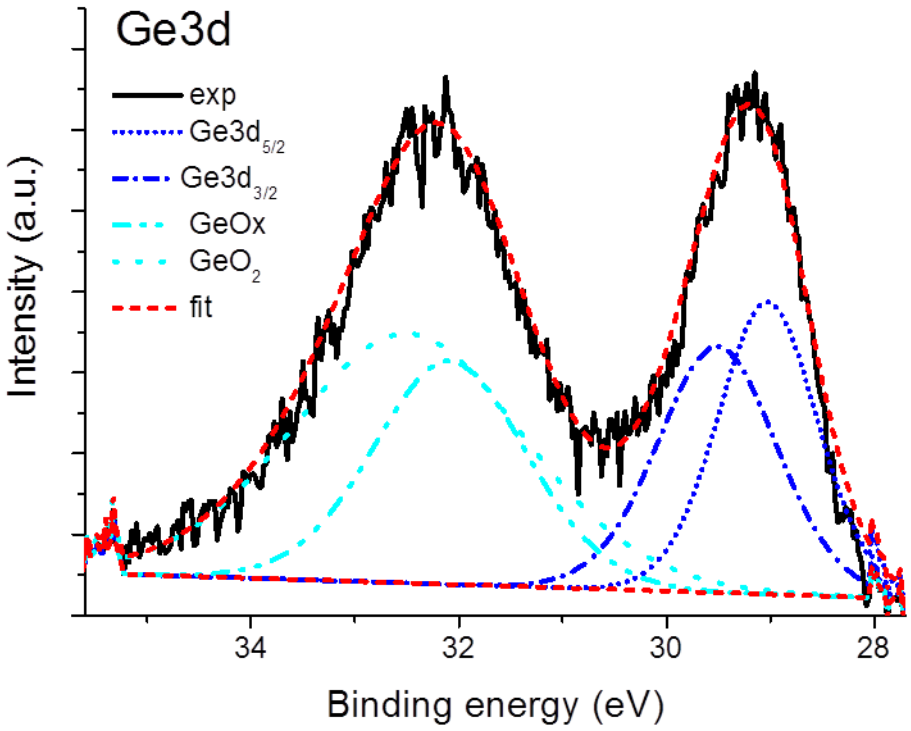

Figure 43. XPS spectrum results centred around Ge 3d

These figures show that aluminium was deposited on the surface but there is still a very strong signal from the GeO_x. Further experimental runs of Al deposition have shown that an incomplete Al layer has been deposited (as shown starting from page 99) meaning that for the set of results from the 10s, 5s and 2s exposure there is not an effective oxygen barrier so that when the samples are exposed to an oxygen containing atmosphere they quickly reoxidise to form a native oxide with some aluminium oxide component remaining as confirmed by the XPS results.

5.3 TEM

Transmission electron microscopy was carried out on this sample to determine thickness values and these are shown in Figure 44.

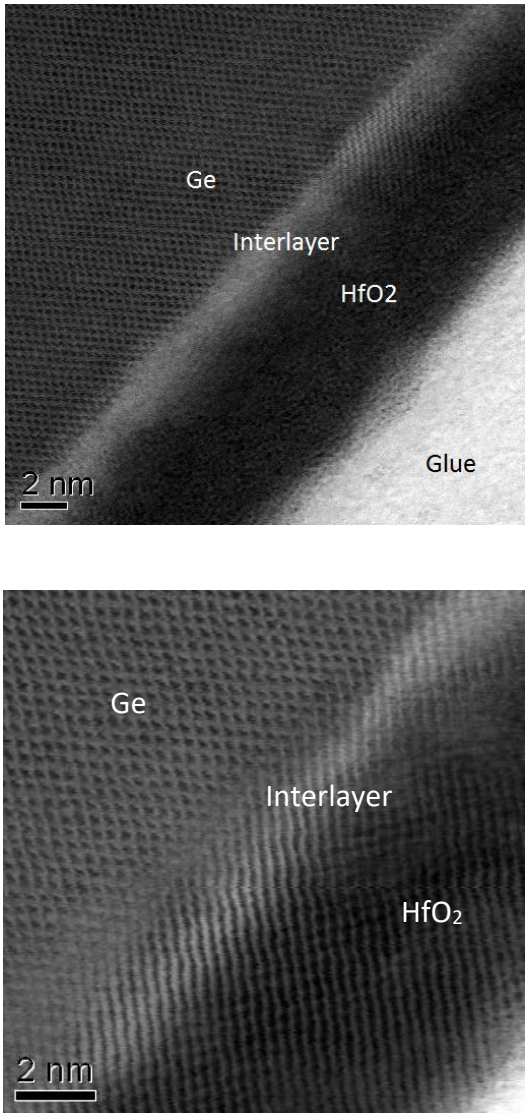

Figure 44. TEM images under x6000k (top) and x10000k magnification (bottom) in bright field mode

From the TEM images it can be seen that there is a 7nm thick layer of HfO_2 with a 2nm thick inter-layer. The CV data would suggest that this inter-layer is GeO_2 when considering the EOT results and the 7nm thick layer of HfO_2.

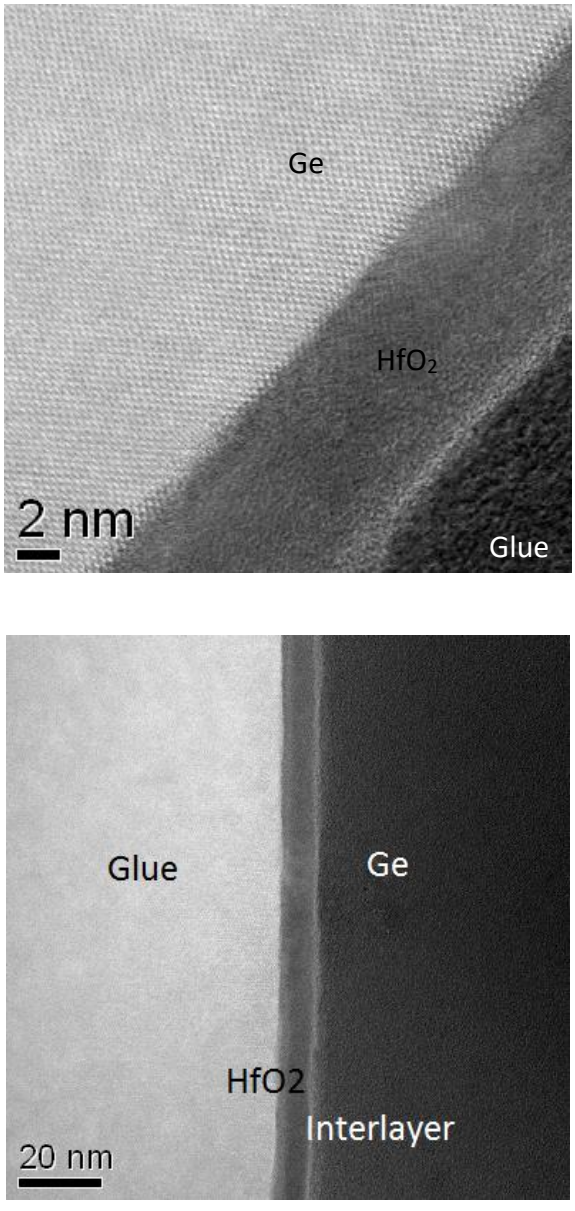

Figure 45. TEM images under x5000k (top) and x1000k (bottom) magnification in dark field mode

TEM data shows that this HfO_2 layer was uniform across the sample investigated because as can be seen in Figure 45 there is no interfacial layer between the germanium wafer and the HfO_2 but in a 1000kx magnification image it is seen that there is a fairly uniform interfacial layer elsewhere on the same sample. This would suggest that the HfO_2 is uniformly deposited but the interlayer is non-uniform but repeatable as the C-V measurements would have a much larger variation in EOT if there were large differences in the thickness of the low-k GeO_x.

5.4 Electrical Characterisation

5.4.1 CV Characteristics

The electrical characteristics were measured before and after a 30-minute forming gas anneal at 350°C. Table 4, Table 5 and Table 6give the CETs calculated from the C-V measurements for 10s, 5s and 2s exposure to the Al flux.

	Thickness of HfO_2		
	1.8nm	3.5nm	7nm
CET As Dep	2nm	3nm	3.6nm
CET FG anneal	1.6nm	2.6nm	3nm

Table 4. CET calculations from CV measurements for 10s Al flux exposure

	Thickness of HfO_2				
	1.8nm	2.2nm	3.5nm	7nm	14nm
CET As Dep	-	-	3.2nm	3.4nm	4.8nm
CET FG anneal	2.3nm	2.6nm	2.6nm	3.5nm	4.8nm

Table 5. CET calculations from CV measurements for 5s Al flux exposure

	Thickness of HfO_2		
	2nm	3.5nm	7nm
CET As Dep	-	3nm	-
CET FG anneal	2.1nm	2.6nm	3.1nm

Table 6. CET calculations from CV measurements for 2s Al flux exposure

Figure 46 shows a typical C-V plot for these samples. This shows low stretch out through depletion and inversion, low frequency dispersion in accumulation and the shape in inversion suggests a low density of interface states. Figure 47 shows the CET against number of cycles for the 5s and 10s Al flux times.

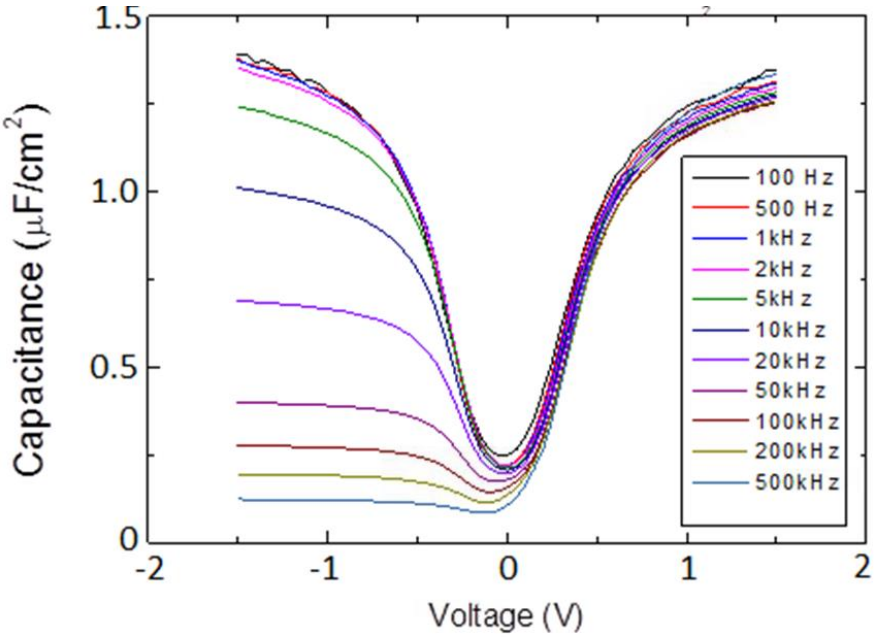

Figure 46. Typical CV as a function of frequency scan for sample with 5s Al flux and 3.5nm HfO_2

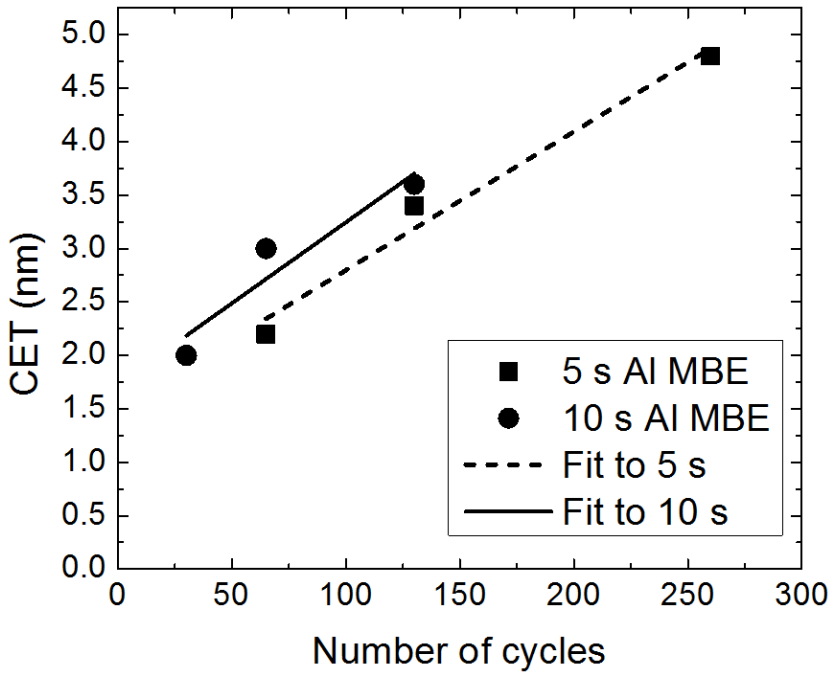

Figure 47. CET against number of ALD cycles for 10s and 5s Al flux times

From a linear extrapolation of this data to the intercept of the CET axis the thickness of the interfacial layer can be calculated. There is a difference in the intercept for the 5s and 10s flux times and this is attributed to thicker Al_2O_3 thickness deposition rate is found to be 0.6nm per 5s and there is a 1.6nm GeO_x layer at the interface.

The lowest CET value is for the sample with 10s Al exposure and 1.8nm of HfO_2 deposited on top. The hysteresis for this sample was very low as shown in Figure 48 for the as deposited measurements but after undergoing a forming gas anneal, significant hysteresis appeared (from ~10mV to 1V). This could be due to an intermixing of the germanium oxide and the hafnium oxide to form a hafnium germanate but for the samples with 5s Al flux exposure the forming gas reduced the hysteresis and for the 2s Al flux exposure there was little difference to the hysteresis. Forming gas annealing did improve the shape of the C-V curves and an example of this is shown in Figure 49.

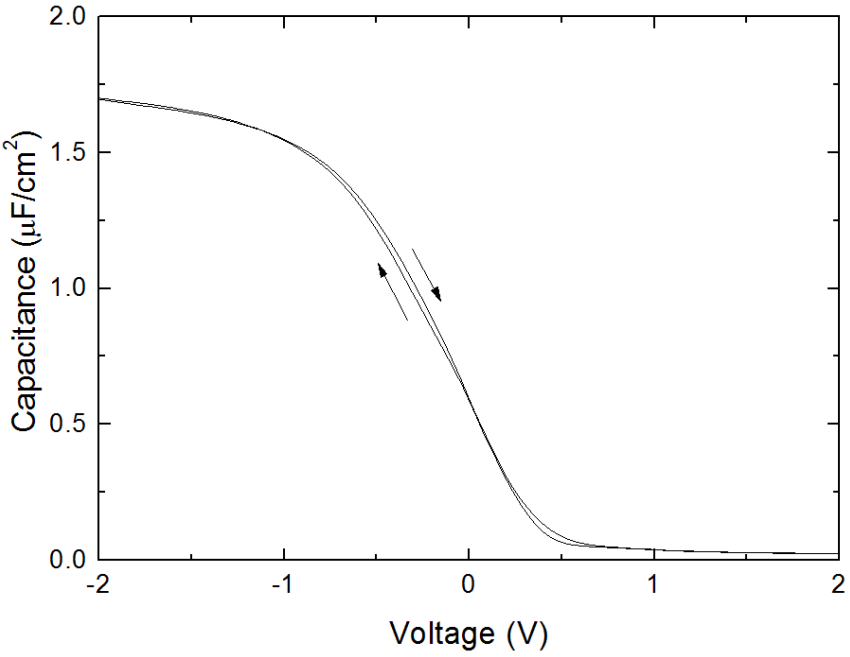

Figure 48. CV data showing the hysteresis of sample with an EOT of 1.7nm measured at 1MHz

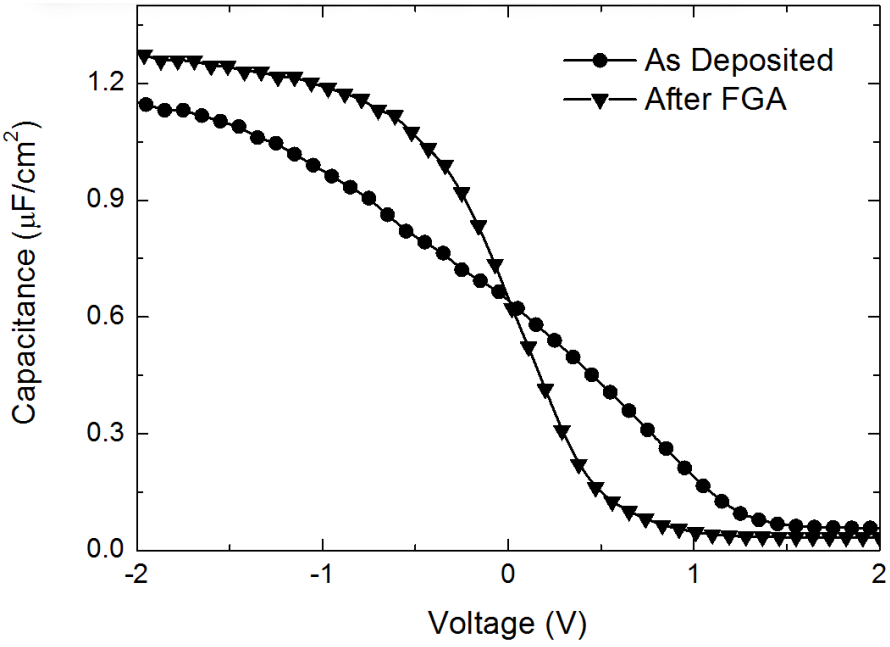

Figure 49. CV data showing an example of the effect of forming gas anneal on the C-V characteristics where the stretched out CV for the as deposited sample indicates a higher D_{it}

As can be seen in Figure 49 the effect of the forming gas anneal is to improve the EOT of the device as indicated by the increase in capacitance at -2V and there is significantly less stretch out indicating a reduction in the density of interface states.

The effect of the thermal preclean temperature can be seen in Figure 50.

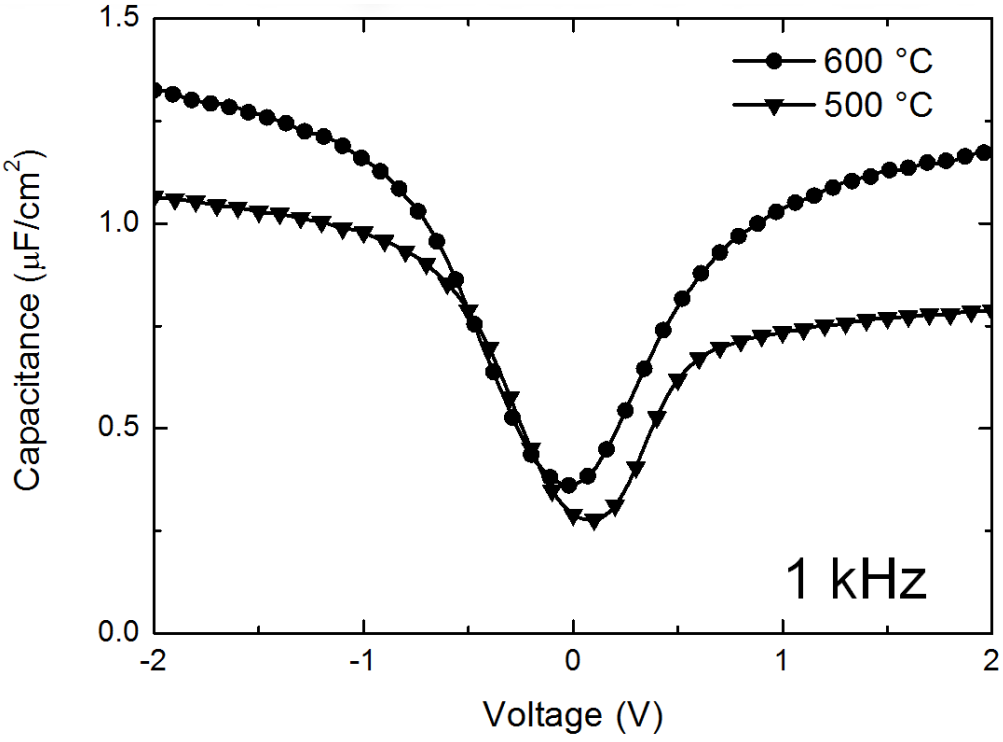

Figure 50. CV data showing the effect of the thermal preclean temperature on the EOT (shown by the increase in the capacitance) of samples with 7nm HfO_2 on p-type germanium

The capacitance in accumulation (-2V) is increased by about 30% with the higher temperature clean meaning the EOT of the devices reduces from 3nm

to 2.3nm for samples with 7nm of HfO_2 deposited. This is attributed to a more efficient removal of the native oxide layer prior to depositions meaning a thinner GeO_x layer in the final devices and this thinner GeO_x layer is estimated to be about 1nm.

5.4.2 I-V Characterisation

The leakage current for the sample shown in Figure 46 is shown in Figure 51.

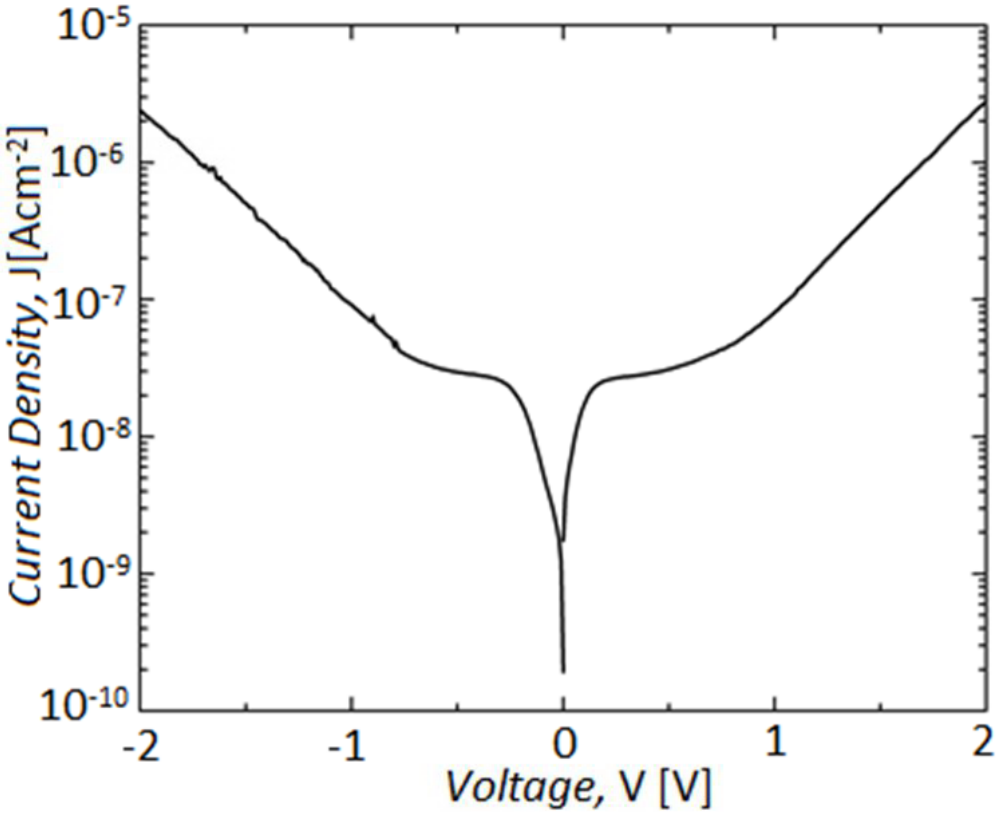

Figure 51. Current density measurements for sample with 5s Al flux and 3.5nm HfO_2

This shows low leakage currents of $3x10^{-8}Acm^{-2}$ at +/- 1V. For a sample cleaned at 600°C with the same 3.5nm HfO_2 the leakage doubled which led to degraded C-V characteristics. For a device with an EOT of 1.5nm the leakage current is shown in Figure 52.

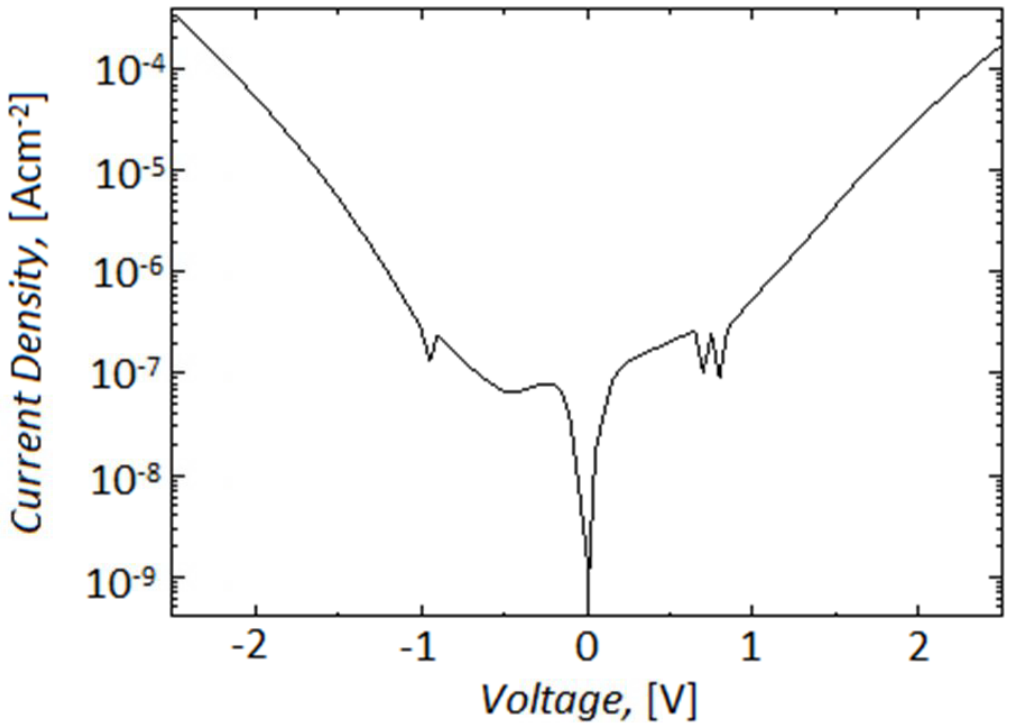

Figure 52. Current density for sample cleaned at 600°C, 15s Al flux and 3.5nm HfO_2 with an EOT of 1.5nm

This I-V data in Figure 52 shows a leakage current of $3x10^{-7}Acm^{-2}$ at +/-1V.

5.5 Chapter Summary

Trilayers of $GeO_x/Al_2O_3/HfO_2$ were fabricated using MBE for ultra-thin deposition of Al and subsequent ALD of HfO_2. It has been shown that shorter exposure times to the Al flux, gave lower EOT's with the lowest value being

1.3nm when combined with a 1.8nm cap of HfO_2 on top. Low hysteresis was observed for as-deposited samples but this increased upon annealing indicating a deterioration of the GeO_x layer and as the EOT was observed to decrease with annealing this hysteresis is attributed to changes in the GeO_x layer creating traps near the interface. The leakage current of these devices was found to be comparable with the state-of-the-art in the literature for this type of scaled devices [17]. The EOT showed a dependence on the temperature of thermal clean of the devices prior to deposition, which is attributed to a more efficient removal of the native GeO_2. Zhang et al [15] showed that when exposing a ALD grown thin (~0.3nm) Al_2O_3 layer to an oxygen plasma a thin GeO_x layer can be formed underneath with very low EOT and D_{it} and HfO_2 could be deposited to further scale down the EOT. These were shown in Figure 14-18. The improvements found by Zhang and co-workers could have been due to their process being entirely in situ thereby reducing any contamination that would degrade the interface properties. The plasma ALD process also grew a thicker GeO_x interlayer thereby hindering EOT scaling. Hidishima et al [61] performed experiments similar to the results presented here in that they also deposited Al metal by MBE but they then oxidised the underlying Ge by annealing in a furnace. They found that increasing the thickness of the deposited Al metal suppressed the thickness of the GeO_x layer grown underneath when annealed and that once the thickness of the Al layer reached 0.8nm the Al could not fully oxidise. Using this

technique they were able to scale the EOT down to 1.2nm but at a much higher leakage current (approaching 1 Acm^2 at -1V) than presented in this study.

6. ALD of Thin Al_2O_3 with HfO_2 Cap

ALD is used in industrial CMOS fabrication meaning that it would be preferential to have a fully ALD process as the fabrication method. For this reason similar structures to the ones described in Chapter 5 were grown by ALD. The growth of these gate stacks were characterised by XPS and CV methods.

6.1 Growth

Samples were prepared by using the preclean method described on page 57 with the subsequent deposition of three ALD cycles of TMA (0.1s)/oxygen plasma (3s) with a 3s purge time using an Oxford Instruments OpAL reactor. Varying thicknesses of HfO_2 $(MeCp)_2Hf(OMe)(Me)$ ((3s)/oxygen plasma (3s)) with a 3s purge time were then deposited by a plasma ALD process and metal contacts were deposited to form MOS structures so that the dielectric constant of the HfO_2 layer could be determined by plotting the CET against HfO_2 thickness.

6.2 XPS Characterisation

Figure 53 shows the XPS scan with 2nm of Al_2O_3 grown thermally followed by 2nm of HfO_2 using oxygen plasma.

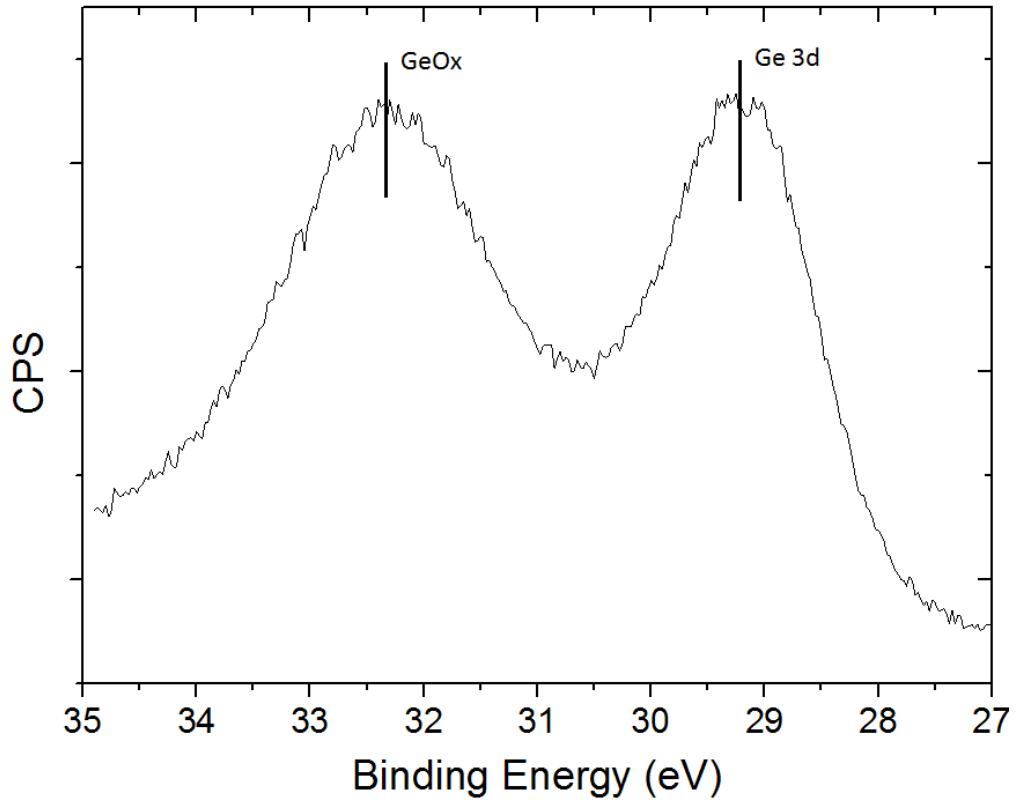

Figure 53. XPS spectrum of Ge 3d when 2nm of Al_2O_3 is grown thermally followed by 2nm HfO_2 grown using oxygen plasma

This shows that there is still very significant regrowth of GeO_x when using a plasma process even if a 2nm thick Al_2O_3 layer is employed as a diffusion barrier. This means that a plasma process is not suitable for scaled devices due to the low dielectric constant nature of the GeO_x (~5) interfacial layer.

6.3 Electrical Characterisation

Figure 54 shows a C-V scan of a sample with the Al_2O_3 treatment with 20nm of HfO_2 deposited on top by the plasma process.

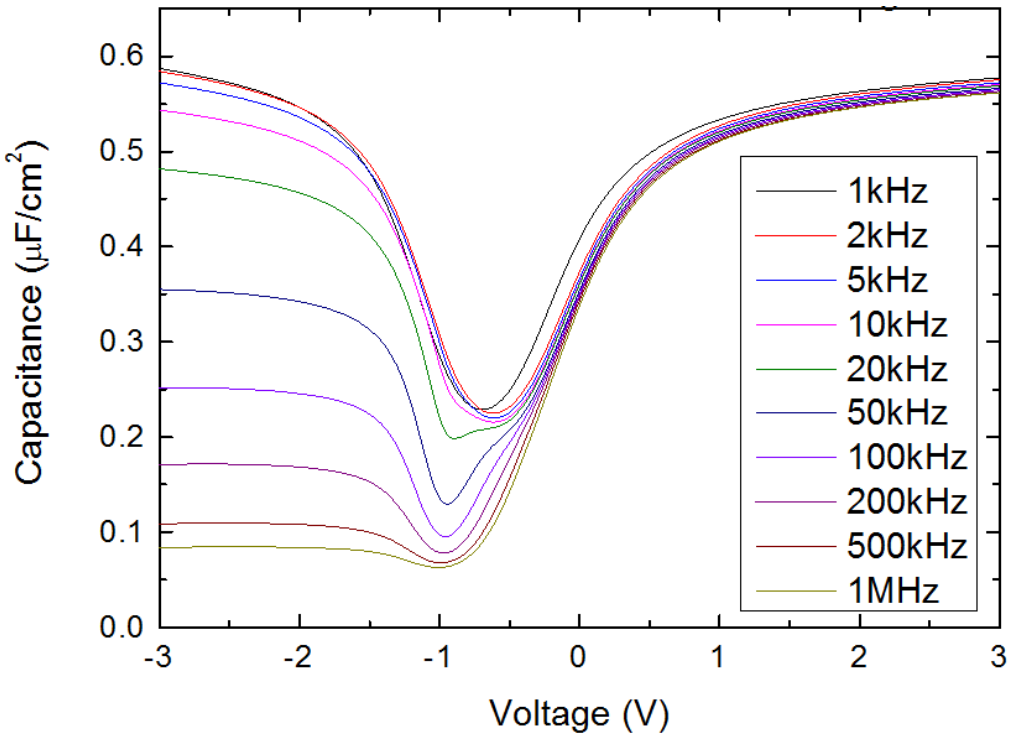

Figure 54. C-V as a function of frequency of 20nm HfO_2 grown using a plasma process on n-type Ge

The C-V data shows well behaved data with proper inversion characteristics.

A plot of CET against HfO_2 thickness is shown in Figure 55. If the dielectric constant used to calculate the CET (SiO_2 is used with a dielectric constant of 3.9) is divided by the gradient of the graph the dielectric constant of the HfO_2 can be found. From the gradient of Figure 55 figure the dielectric constant was determined to be 20.8 (with 18.7 as the lower limit and 23.5 as the upper limit). The intercept of the y-axis gives the CET of the interfacial layer and this was found to be 2.16nm. This equates to an EOT of 1.86nm and assuming a dielectric constant of 5 this means that there is a GeO_x interfacial layer of 1.45mn. The figure will be slightly less than that due to the presence of a small

amount of Al_2O_3 present at the interface. This interfacial layer is unintentionally grown during the ALD process due to the use of oxygen plasma as the oxygen source.

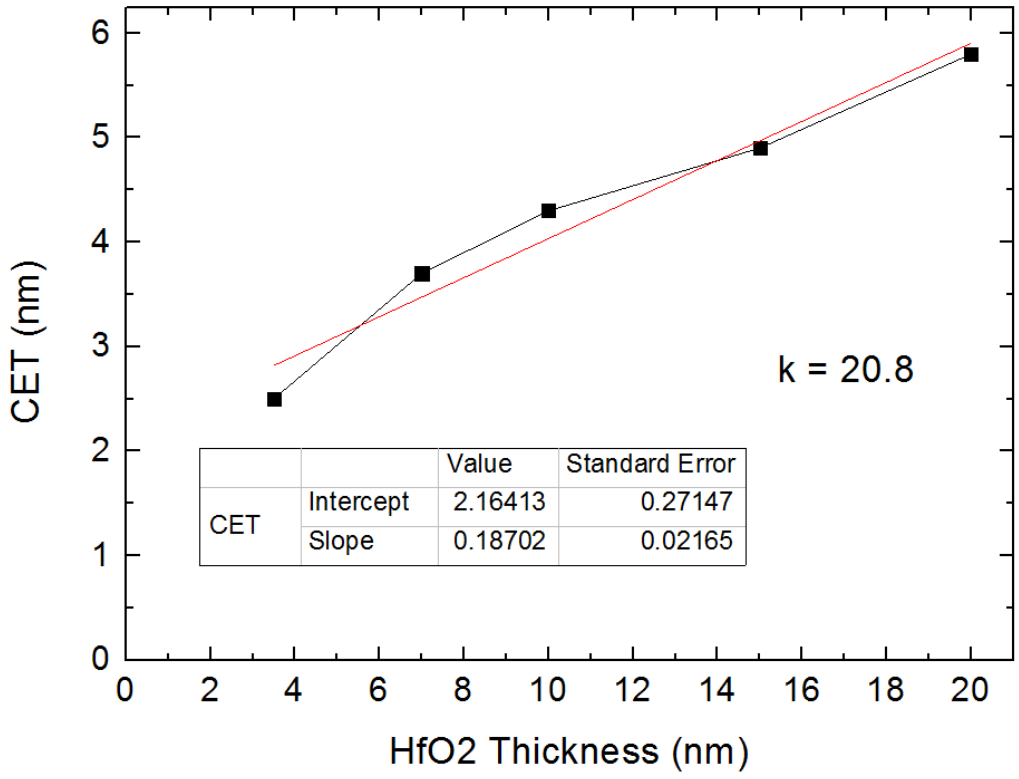

Figure 55. CET against HfO_2 thickness with a line of best fit indicating the y-axis intercept and the slope of the graph

6.4 Chapter Summary

Fabricating the samples using a plasma process creates a ~2nm thick GeO_x interfacial layer which makes scaling the EOT down difficult without using a method to reduce the interfacial layer. This interfacial layer is formed even when a relatively thick (2nm) layer of Al_2O_3 is used as a barrier. The dielectric

constant of the plasma grown HfO_2 was found to be 20.8 which is slightly higher than the value of 17 for HfO_2 grown thermally at 300^oC which could be due to a denser film being deposited. When compared to the structures set by Zhang at al detailed in Figure 14-18 it is clear that the process set out in this study grows too thick a GeO_x layer which makes it EOT scaling difficult. The difference is probably due to the method of oxygen plasma that has been employed.

7. Sulphur Passivation of Germanium

Sulphur passivation has been proposed as a method to for the passivation of Ge [19]. This has the advantage that it can be used as a common gate stack solution if high performance CMOS is realised using Ge and III-V on a silicon substrate [52]. S-passivated Ge gate stacks were fabricated with either Al_2O_3 or HfO_2 as a dielectric on top. These gate stacks were then characterised by XPS to determine the bonding conditions at the interface of the high k and Ge(S) and determine the band offsets. CV analysis was performed to investigate the effect of the S-passivation at the Ge/high k interface.

7.1 Growth Conditions

To investigate the effect of sulphur passivation on germanium the germanium wafer was exposed to ammonium sulphide prior to ALD deposition. The germanium samples were given the clean described on page 57. The samples were dipped in 10% $(NH4)_2S$ for 10 minutes. They were then rinsed in DI water and blown dry in Argon. ALD was performed using an Oxford Instruments OpAL reactor and Al_2O_3 deposition was achieved using TMA (0.1s pulse)/H_2O (0.1s pulse) cycles with 3s purge time in between at 250^oC. HfO_2 depositions were performed using $(MeCp)_2Hf(OMe)(Me)$ (3s pulse) as the Hf precursor and either H_2O (0.1s pulse) or oxygen plasma (3s pulse) as the oxygen precursor with a 3s purge time in between at the stated temperature.

7.2 XPS of (S-passivated) Germanium

Figure 56 shows a XPS scan of Ge 3d after only a HF clean and Figure 57 is after $(NH4)_2S$ treatment. Figure 56 has a small peak at a higher binding energy than the main Ge 3d peak which is attributed to a small GeO_x layer remaining after the HF clean. Figure 57 also has a small peak at higher binding energy that is slightly smaller and at a lower binding energy after S-passivation than without suggesting a more efficient removal of native oxide and replacement with Ge-S bonds.

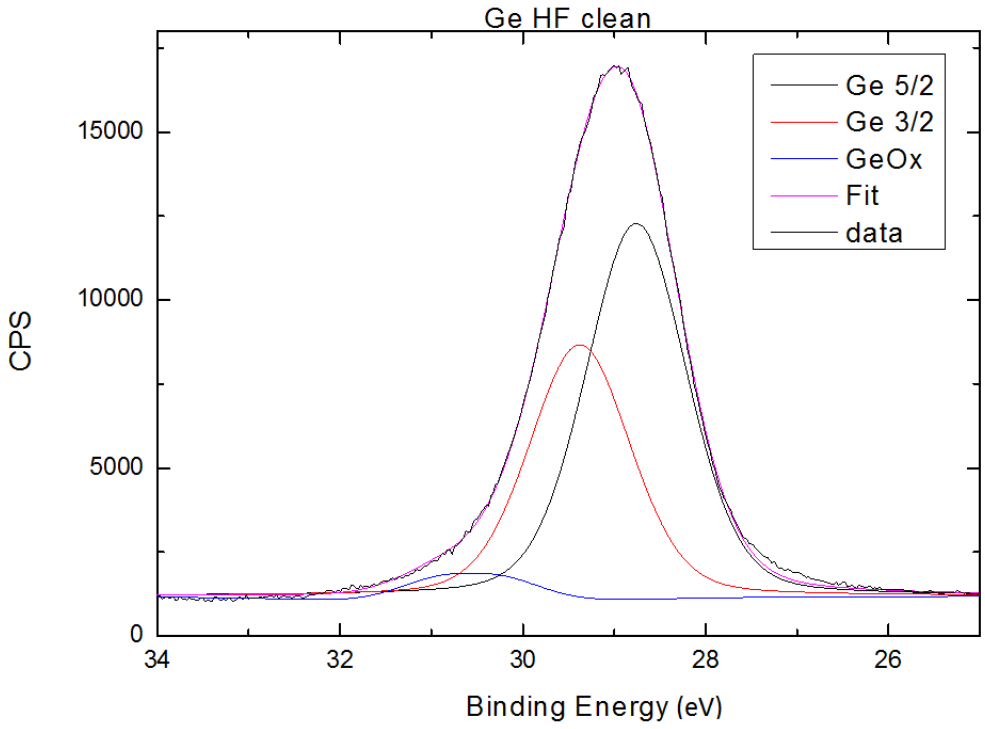

Figure 56. XPS spectrum of HF cleaned Ge3d

In Figure 56 the fit deviates from the data slightly at about 27.1eV. This extra peak is attributed to Ge dangling bonds as shown in Figure 23 by Chellappan et al [20]. The electrical data (page 126) also shows a high D_{it} which supports the presence of dangling bonds at the interface.

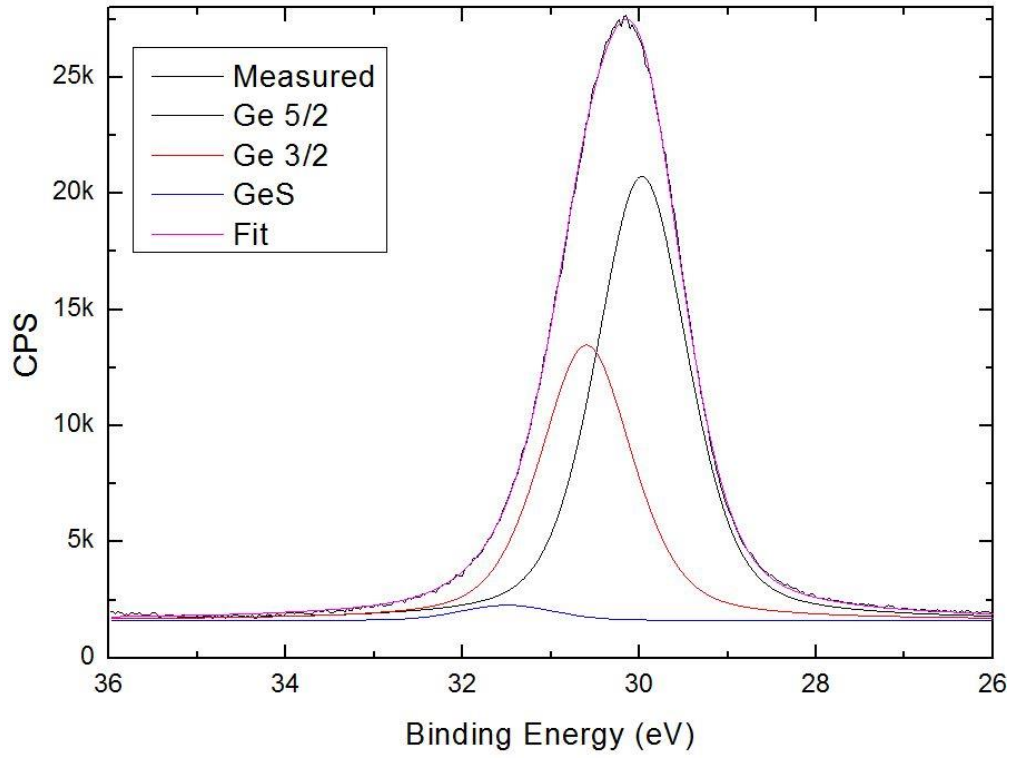

Figure 57. XPS spectrum of S-passivated Ge3d

In Figure 57 the fitted curves lie on the experimental data on the trailing edge of the main peak at lower binding energies which would suggest that there is a significant reduction in dangling bonds when compared with Figure 56. This is evidence that the S-treatment has been successful in passivating the interface which would agree with the electrical data which will be shown on page 126.

A scan of the S 2p region shows that the sulphur has been successfully deposited on to the surface of the germanium as shown in Figure 58.

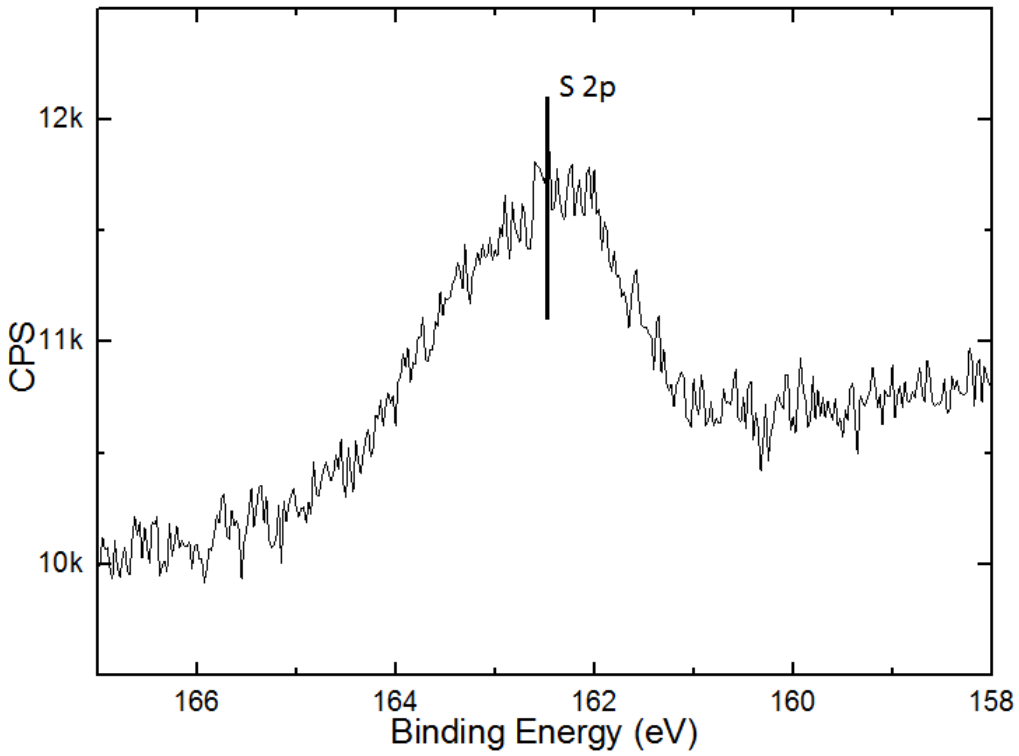

Figure 58. XPS spectrum of S-passivated S 2p

For deposition of Al_2O_3, 20 thermal ALD cycles (TMA/H_2O) were deposited at 250^oC for the thin cap samples as this has been shown to provide a layer that is thick enough so that the island like growth at the initial part of an ALD process has finished therefore providing a closed layer that protects the Ge surface from the atmosphere during transfer to the XPS chamber. By using 20 cycles (~2nm) the layer is still thin enough that the germanium surface can still be seen with XPS. For the electrical measurements, 100 cycles were used so

that the interface could be investigated without detrimental effects due to leakage currents through the device.

For the HfO_2 films grown thermally at 300^oC, ALD nucleation was an issue so that for the HF cleaned sample there was no growth at all but for the S-passivated sample there was a significant reduction in growth. When 325 ALD cycles were deposited, which provided a film of 10nm on a Si sample grown at the same time, the thickness measured by ellipsometry was only 6nm on the S-passivated Ge. For some samples three cycles of TMA/H_2O were used to nucleate the surface making it accommodating to the ALD process after which the HfO_2 films grew as expected compared to a reference samples grown at the same time.

7.3 Al_2O_3 on (S-passivated) Germanium

7.3.1 XPS Characterisation

To see if the surface maintains a Ge-S interface after ALD deposition a XPS scan of Ge3d was acquired after the deposition of 2nm of Al_2O_3 and this is shown in Figure 59.

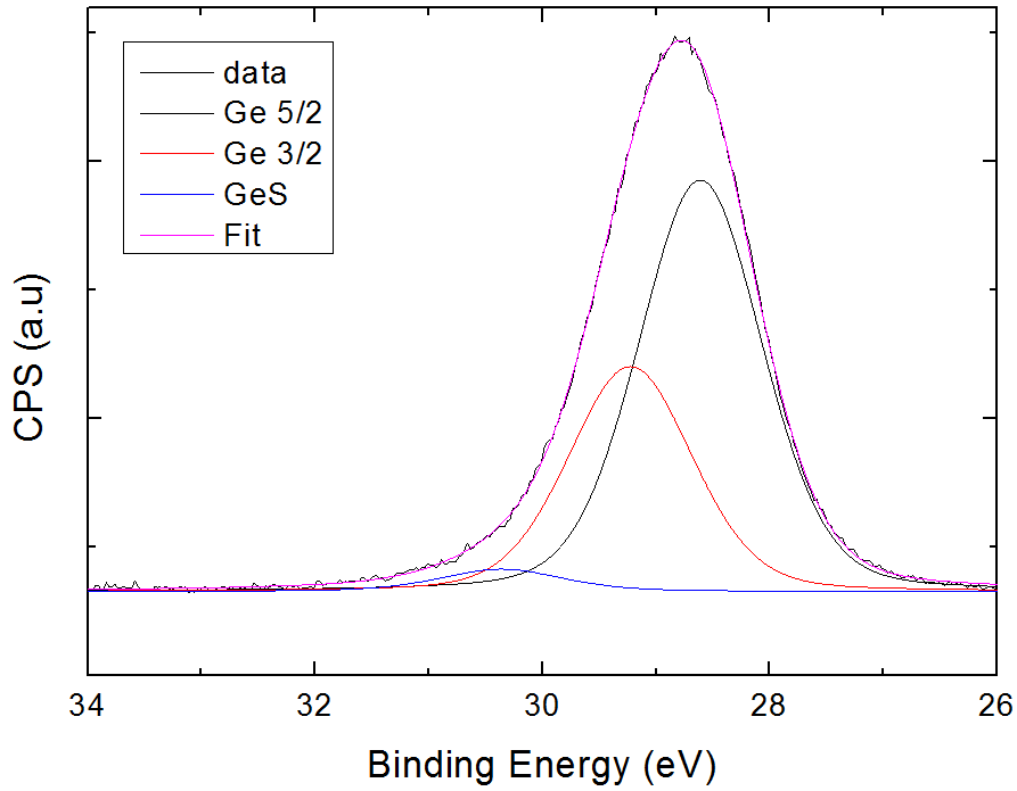

Figure 59. XPS spectrum S-passivated Ge3d with 2nm Al_2O_3 deposited thermally showing the presence of a GeS peak at higher binding energy than the main Ge3d peak

This shows that the germanium/sulphur interface is preserved through the ALD process with very little change in the Ge3d scan when compared to Figure 57 without the Al_2O_3 layer. Figure 60 shows that the sulphur remains after ALD deposition.

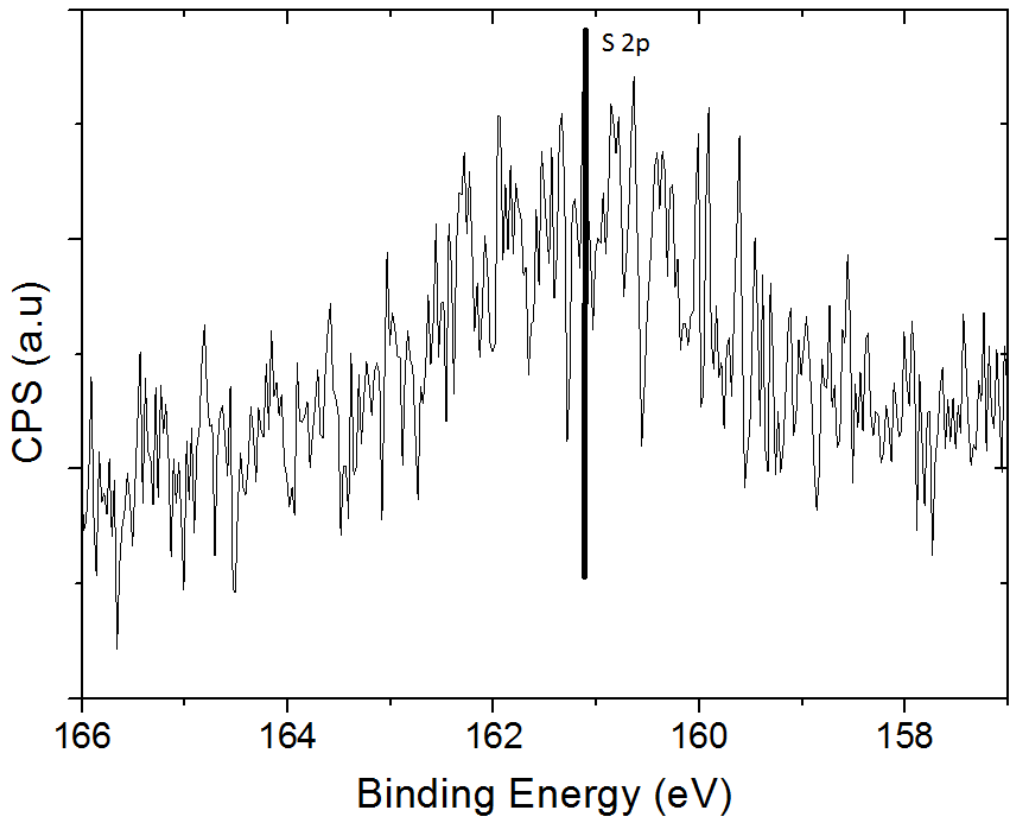

Figure 60. XPS spectrum of S-passivated S 2p with 2nm Al_2O_3

The peak position of the S 2p has shifted significantly (1.25eV) to lower binding energy when compared with Figure 58 after the ALD process. This is caused by a change in the bonding conditions of the sulphur atoms during the ALD process where oxygen is incorporated at the interface. Sioncke et al [53] report that under forming gas annealing these S-O bonds are replaced so the bonding is Ge-S-Al.

Krouts method was applied to calculate the valence band offset of the gate stack from the Ge to the dielectric layer. Figure 61 shows the valence band maximum (VBM) scan for a thick Al_2O_3 layer.

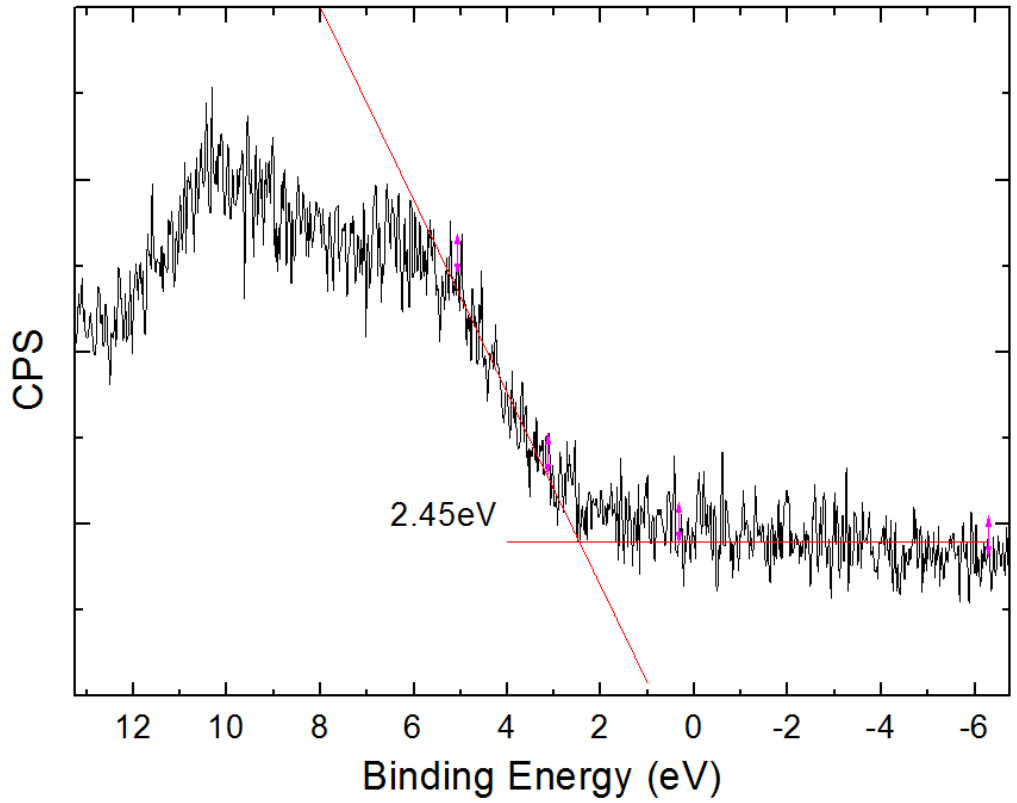

Figure 61. XPS spectrum of valence band maximum of thick Al_2O_3 sample

Figure 62 shows the Al 2p peak for a 20nm thick Al_2O_3 layer. The Al 2p scan of the GeS/2nm Al_2O_3 system is shown in Figure 63. The Al 2p peak value differs from the thick Al_2O_3 by 0.32eV which could be due to some intermixing of the Al_2O_3 layer and the Ge-S interface.

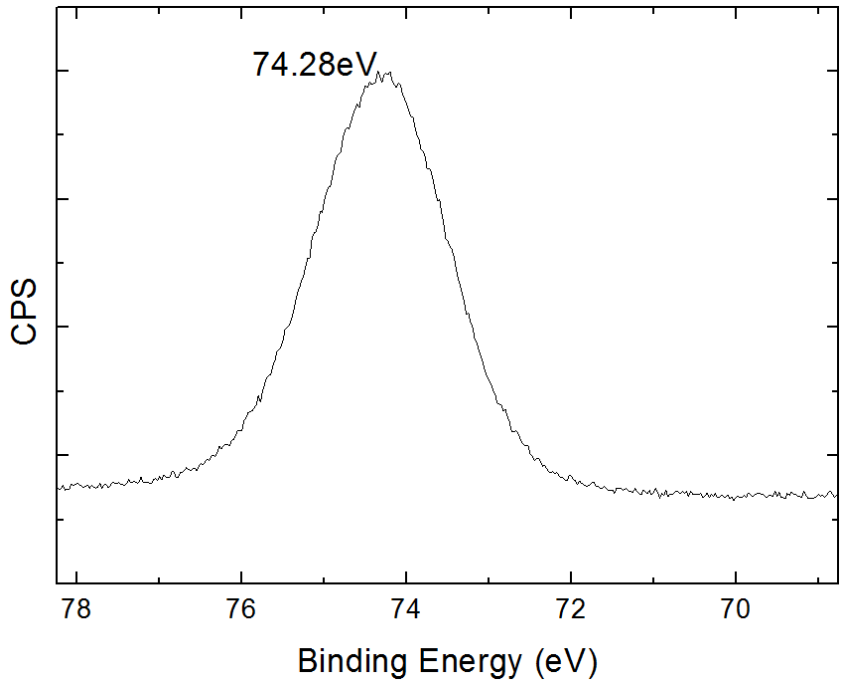

Figure 62. XPS spectrum of Al 2p of thick Al_2O_3 sample

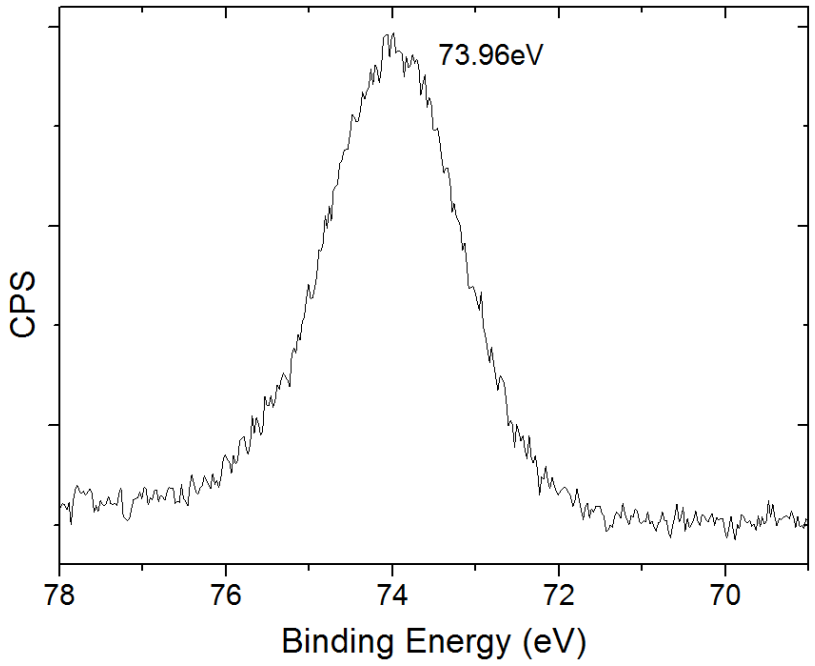

Figure 63. XPS spectrum of Al 2p of S-passivated Ge with 2nm Al_2O_3 cap

From these values and using equation 17 the valence band offset is calculated at 2.84eV. From this and assuming a band gap of 0.66eV for germanium and 6.8eV for Al_2O_3 [20] the band schematic for this structure is shown in Figure 64.

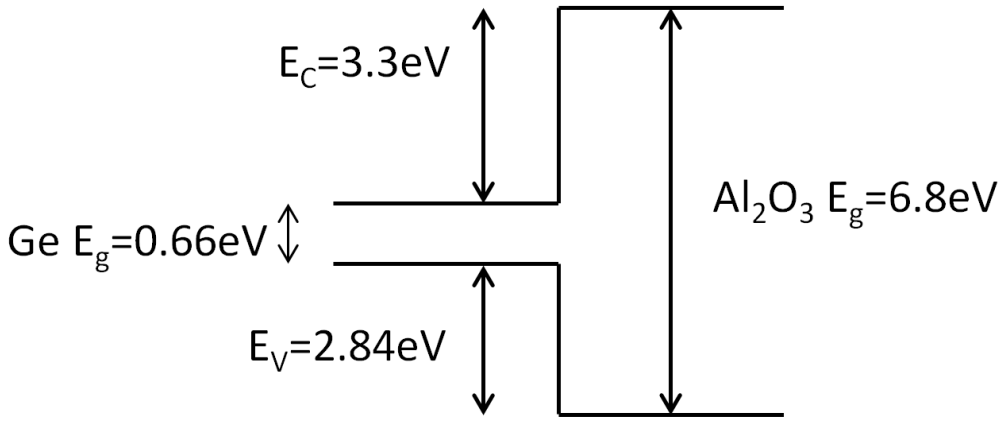

Figure 64. Band schematic of S-passivated Ge with Al_2O_3

This shows that the conduction band offset is 3.3eV. These band offsets are well above the 1eV required to restrict leakage currents across the device meaning that this passivation technique is suitable for CMOS production.

The valence band maximum of a HF clean germanium is shown in Figure 65 and from Figure 56, the Ge 3d peak of a cleaned germanium sample is 28.97eV which is needed for band offset calculations. Figure 66 shows the Al 2p scan for a thin Al_2O_3 cap of HF cleaned germanium.

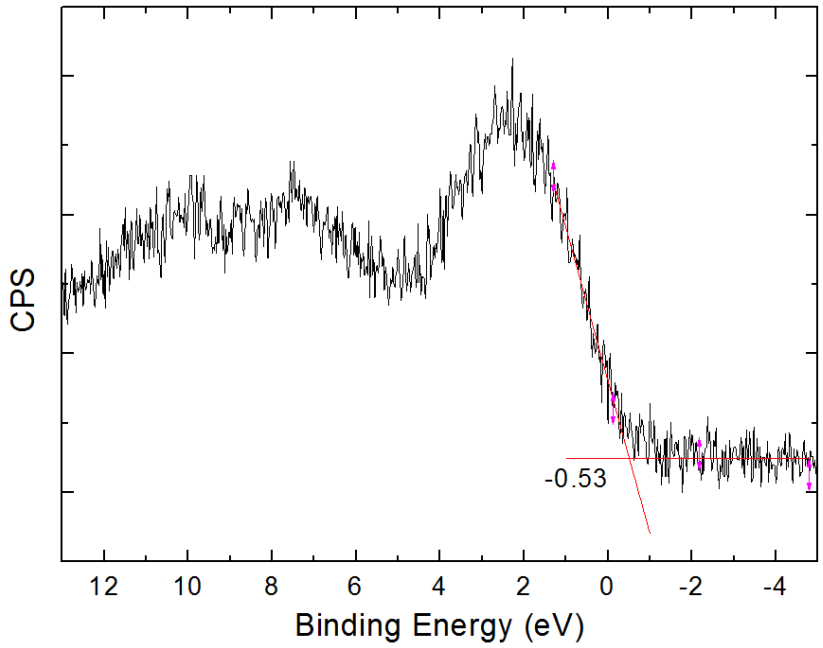

Figure 65. XPS spectrum of valence band maximum of a cleaned Ge sample

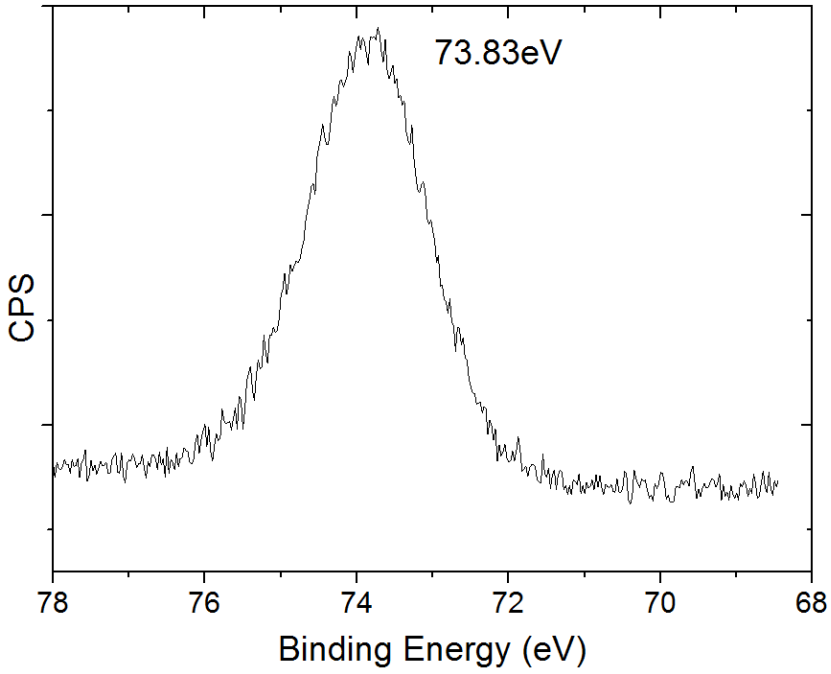

Figure 66. XPS spectrum of Al 2p of HF cleaned Ge with thin Al_2O_3 cap

From this the valance band offset was calculated as 2.53eV. The band schematic for the Ge/Al_2O_3 system is calculated and shown in Figure 67.

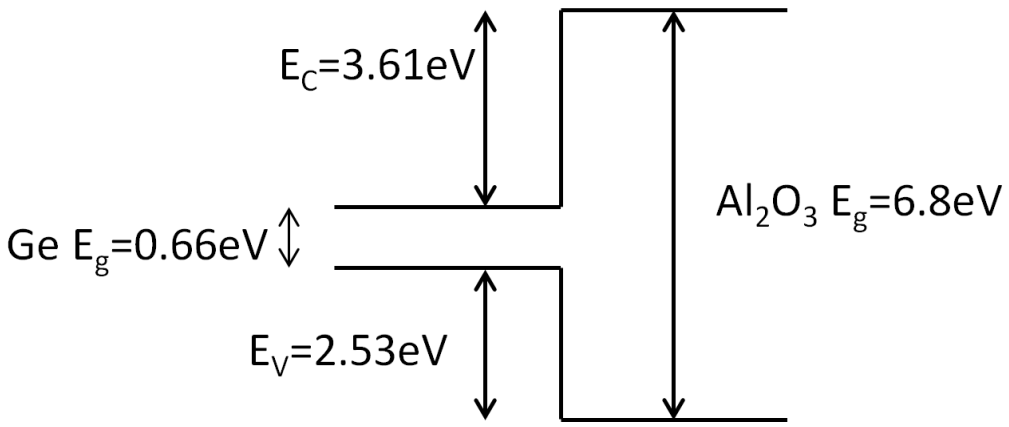

Figure 67. Band schematic of HF cleaned Ge with Al_2O_3

The conduction band offset is therefore shown to be 3.61eV which is larger by 0.31eV than with S-passivation. These band offsets are shown in Table 7 and are well above the required 1eV for state of the art devices.

	Conduction Band Offset (eV)	Valence Band offset (eV)
With Sulphur	3.3	2.84
Without Sulphur	3.61	2.53

Table 7. Band Offsets with and without Sulphur passivation

7.3.2 Electrical Characterisation

To investigate the electrical properties of a S-passivated Ge surface MOS capacitors were fabricated. 100 cycles of thermal Al_2O_3 deposited at 250°C was used as the dielectric first to investigate the effect of S-passivation on the interface and both n-type and p-type substrates were used to see if the passivation occurred throughout the band gap. Figure 68 shows the C-V characteristics on p-type Ge with S-passivation.

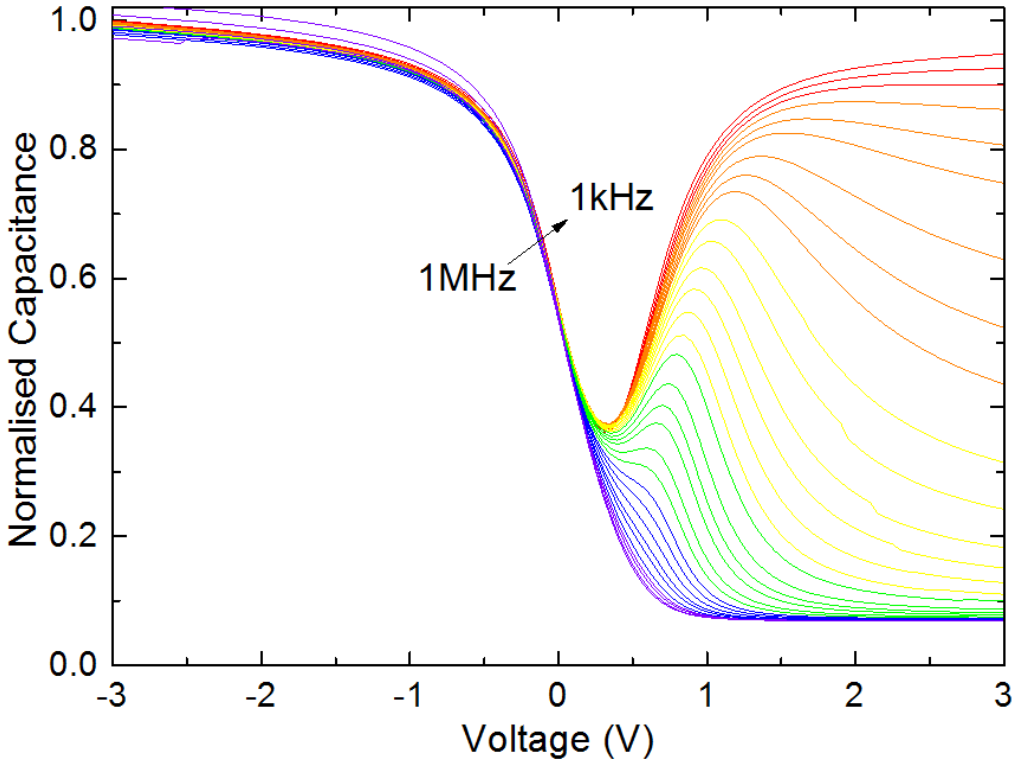

Figure 68. CV as a function of frequency of Al_2O_3 on p-type S-passivated Ge

This shows good CV characteristics with low frequency dispersion in accumulation and into the depletion regime and only the low frequency scans showing inversion indicating a good interface. Figure 69 shows the C-V characteristics of p-type Ge without S-passivation with the Al_2O_3 layer grown at the same time as the sample in Figure 68 to minimise any process differences.

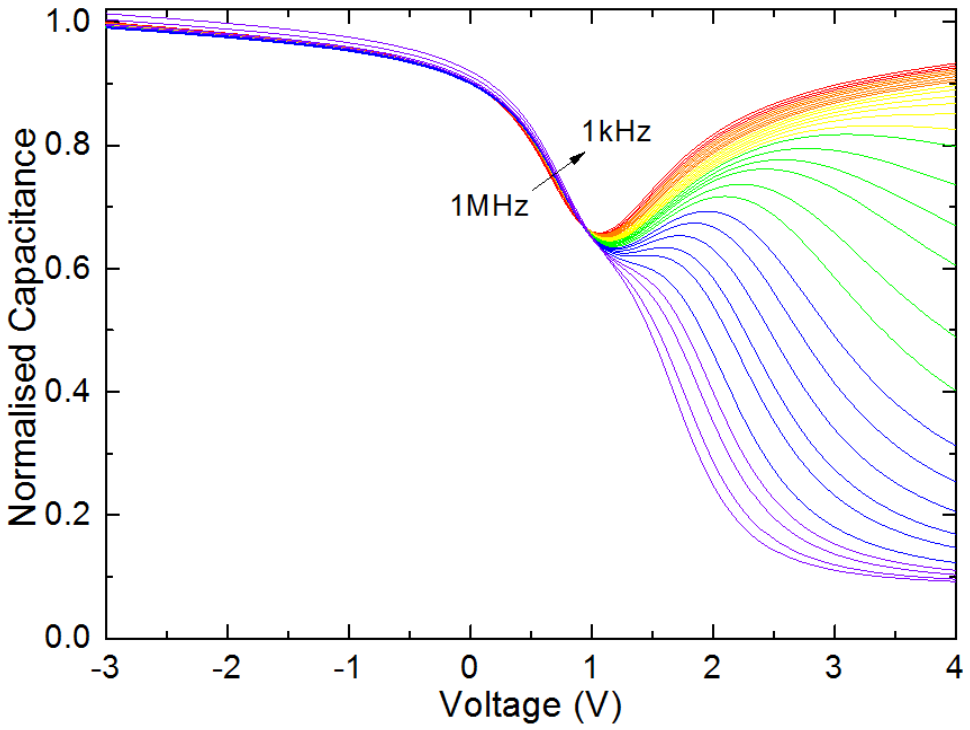

Figure 69. CV as a function of frequency of Al_2O_3 on p-type Germanium

The depletion and inversion characteristics are very different when S-passivation is not employed. A shift to positive voltages (0.65V) is observed when measured at the capacitance minimum for the low frequency curves

which would agree with the XPS finding of downward band bending at the interface. The bump in the capacitance when going in to the depletion regime is indicative of a high density of interface states. Figure 70 shows the transition frequency for the p-type devices. The transition frequency is defined as the frequency at which equation 19 is satisfied and can be used to estimate the relative quality of the gate stack in terms of D_{it}.

$$C_{inv} = \frac{(C_{max} - C_{min})}{2} \qquad \text{Eq.19}$$

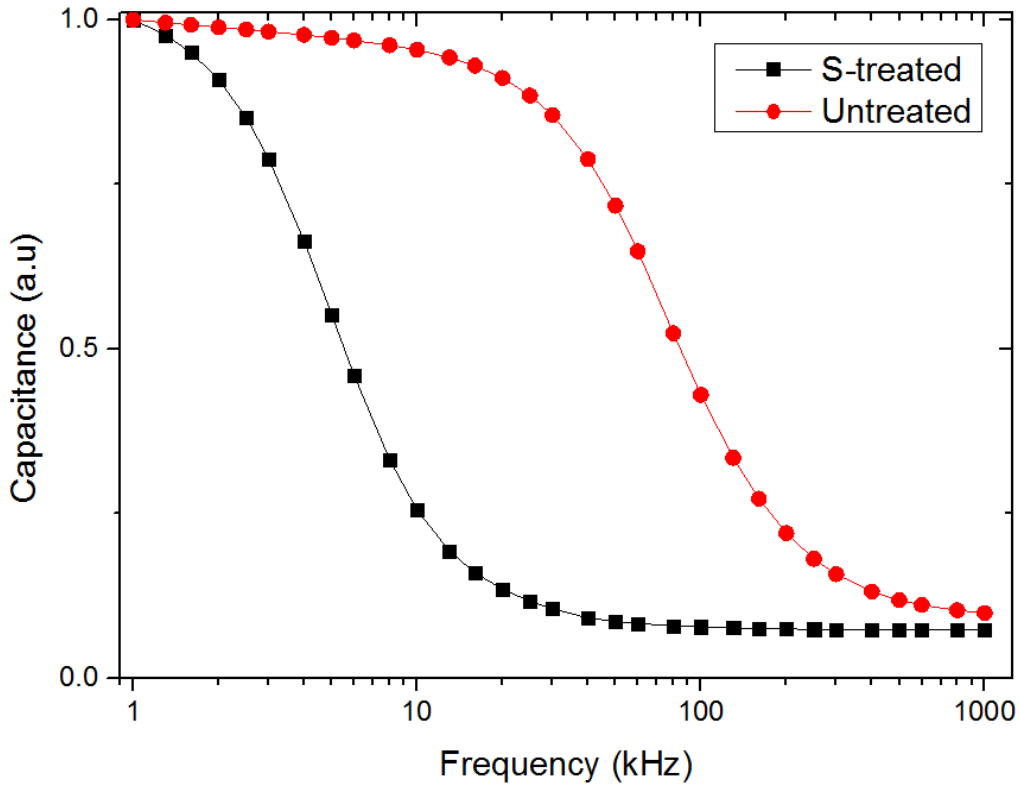

Figure 70. Inversion Capacitance against frequency for p-type Ge with Al_2O_3 with and without S-passivation

The transition frequency for S-passivated samples is 5.5 kHz whereas without S-passivation this raises to 84.2 kHz. This increase in frequency could be explained by considering interface states providing a mechanism for the generation of minority carriers which indicates a higher quality interface for the S-passivated sample.

The C-V data from S-passivated n-type Ge with Al_2O_3 deposited on top is shown in Figure 71.

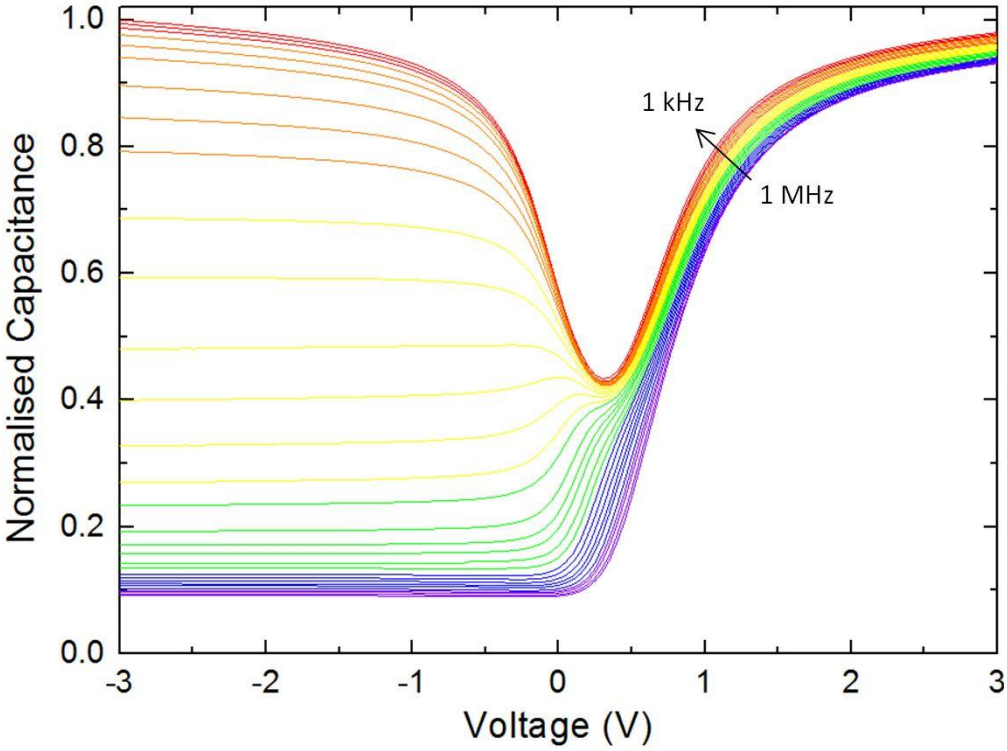

Figure 71. CV as a function of frequency of Al_2O_3 on n-type S-passivated Ge

Figure 72 shows the C-V data on n-type Ge with Al_2O_3 deposited on top without S-passivation.

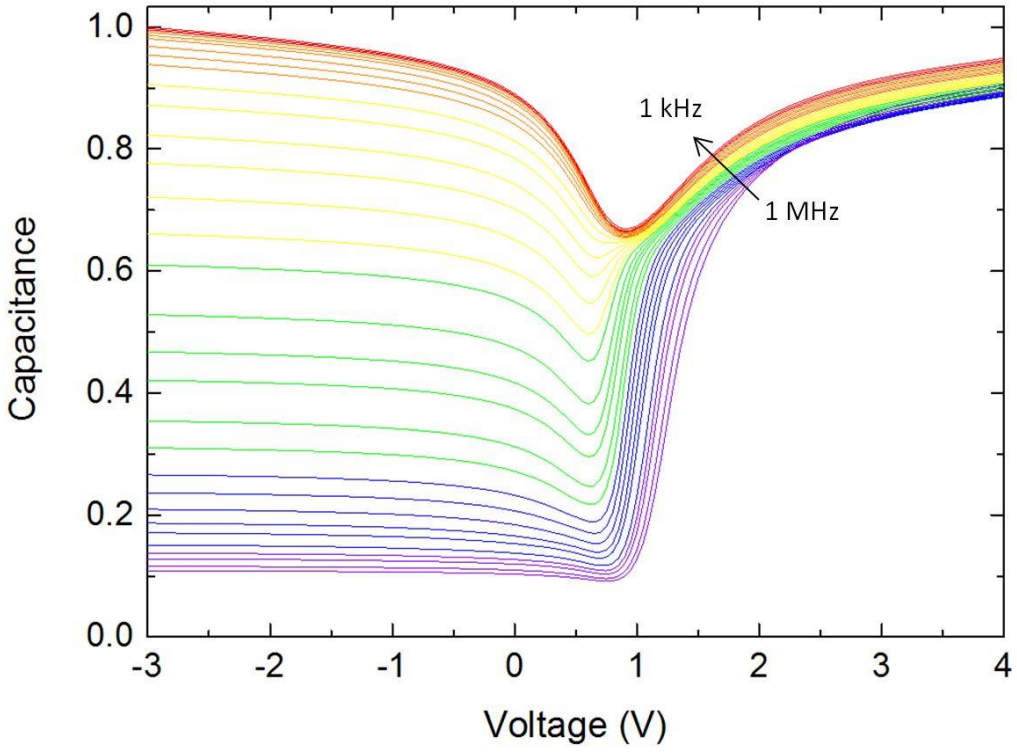

Figure 72. CV as a function of frequency of Al_2O_3 on p-type Germanium

There is again a shift to more positive voltages when measured at the capacitance minimum for the low frequency curves due to the downward band bending at the interface caused by the S-passivation. The transition frequency is plotted in Figure 73.

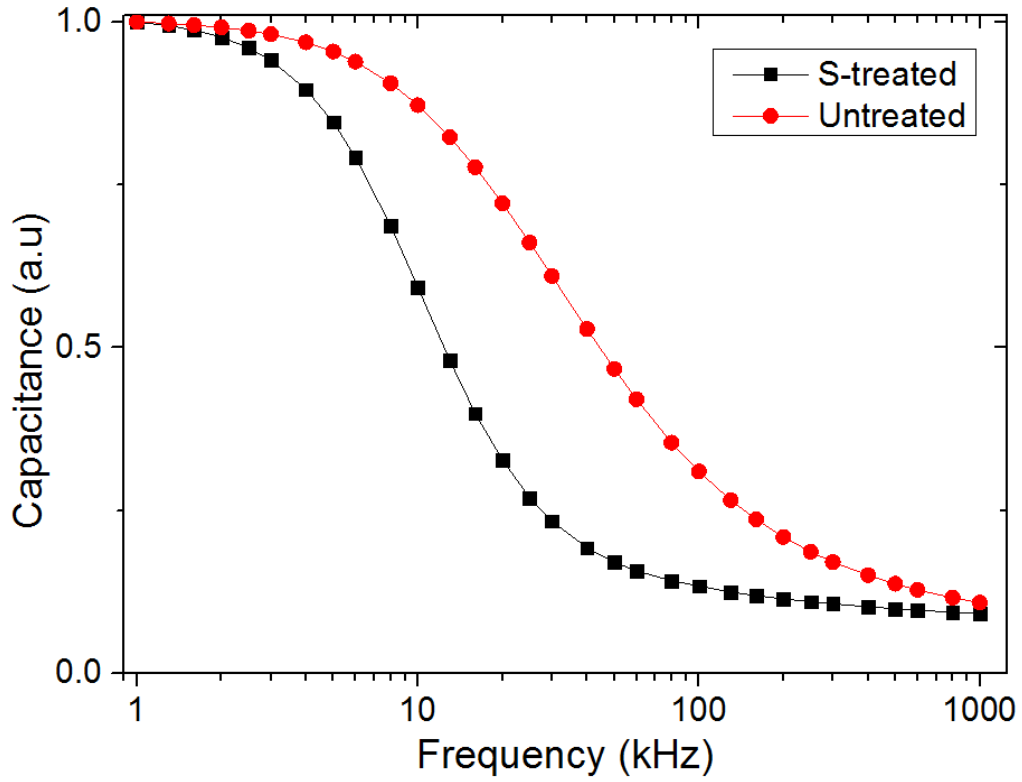

Figure 73. Inversion Capacitance against frequency for n-type Ge with Al_2O_3 with and without S-passivation

The transition frequency for S-passivated Ge is 12.52 kHz whereas without the S-treatment this raises to 44.94 kHz which could indicate a higher density of interface states without S-passivation.

The EOT for both devices measured from the capacitance-voltage measurements were the same which would indicate that the S-passivation does not add to the EOT meaning that it is a promising route for scaled devices.

7.4 HfO_2 on (S-passivated) Germanium

7.4.1 XPS Characterisation

HfO_2 was deposited thermally to see if a good quality Ge interface is maintained with HfO_2 deposited on top of the S- passivated germanium. In an attempt to avoid any growth of an unwanted interfacial layer the samples were loaded in to the ALD chamber at 250^oC as the work on using Al_2O_3 shows that there is minimal growth of a GeO_x layer. The sample then had to be heated up to 350^oC in-situ for deposition of HfO_2. The reactor was then cooled down to 300^oC before the samples were removed.

Figure 74 shows the Ge3d peak for the germanium with and without S-passivation. This shows that the regrowth of an interfacial layer is suppressed by the inclusion of the S-passivation but there is still some GeO_x formed. This could be because the Germanium samples had to be heated in-situ over a period of around 5 minutes in the ALD chamber which is not UHV meaning that there will be some residual moisture in the chamber which could cause a degradation of the interface. This kind of process was illustrated in Figure 13. The position of the S-passivated Ge3d peak in Figure 74 was shifted by 0.16eV to line up with the unpassivated Ge 3d peak. This shift in peak position is consistent with reports showing a shift due to slight band bending occurring at the interface when sulphur is present as shown in Figure 25. This is indicative

that the S-passivation is maintained and that any growth of GeO_x occurs above the S-passivated Germanium.

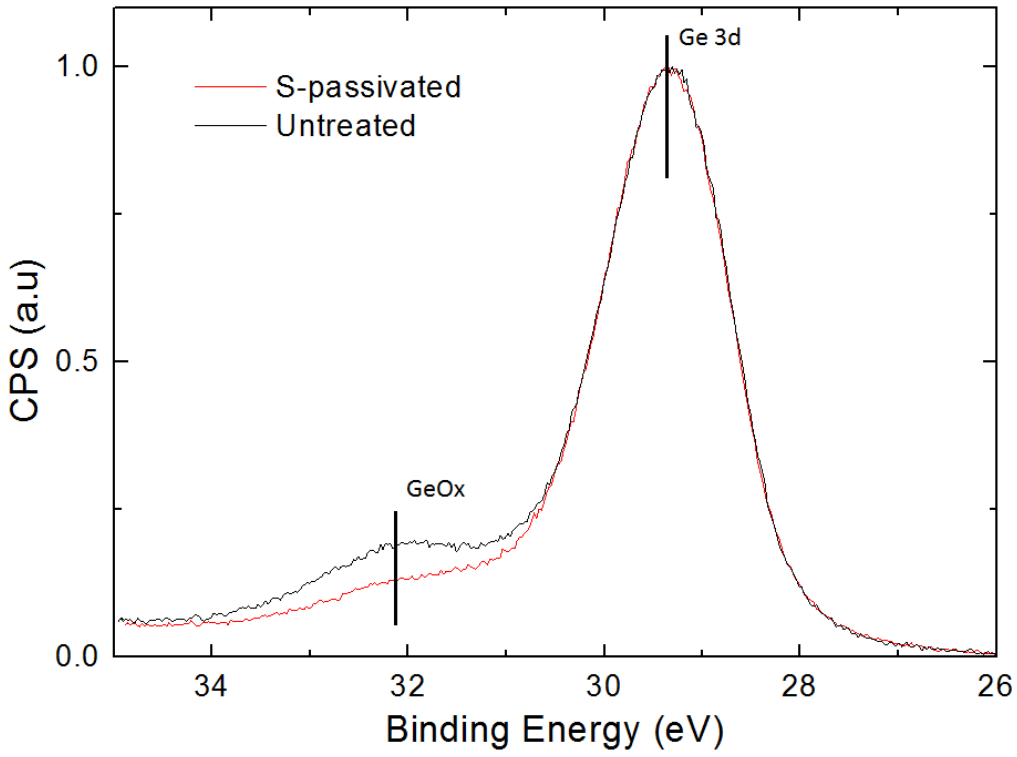

Figure 74. XPS spectrum showing Ge3d of thermal HfO_2 grown with and without S-passivation. S-passivated trace has been shifted by 0.16eV to coincide with untreated sample for clarity

Figure 75 shows the Ge3d when HfO_2 is grown using an oxygen plasma process on Ge with and without S-passivation. The Ge 3d peak coincides for both S-passivated and untreated samples this time. This indicates that the S-passivation layer is affected by the ALD process and the surface has been replaced with a GeO_x/Ge interface regardless of the pre-treatment.

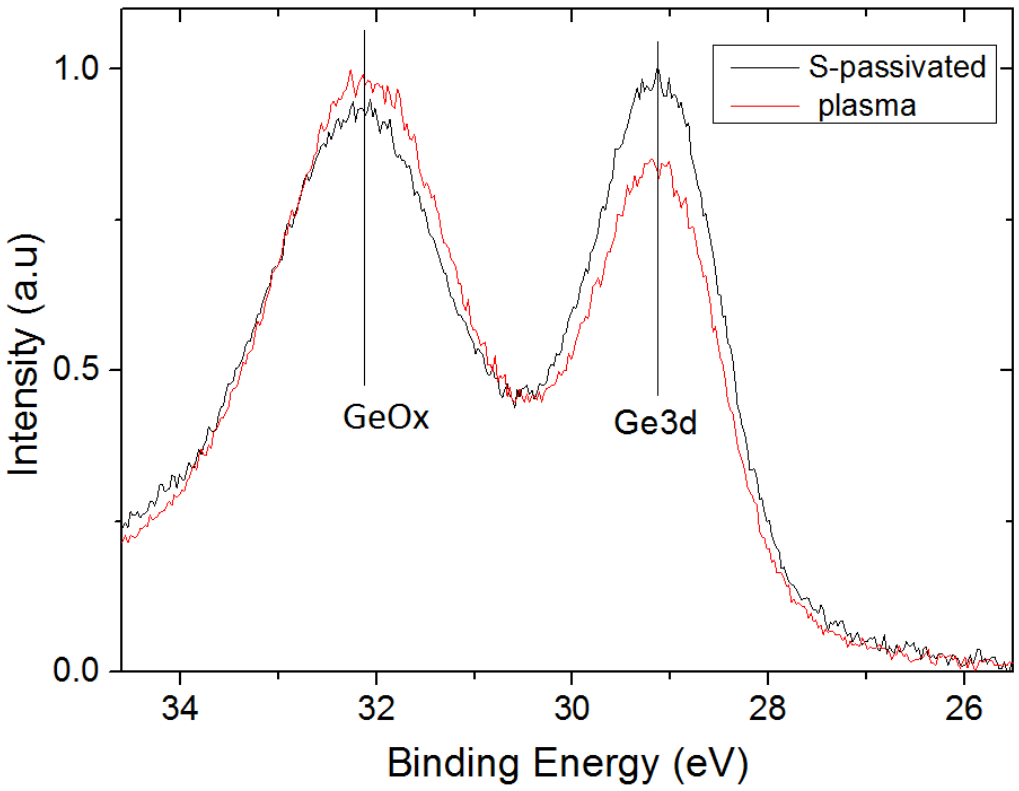

Figure 75. XPS spectrum of Ge3d of plasma HfO_2 grown with and without S-passivation

It can be seen that there is a thicker GeO_x layer formed which is consistent with previous results when a plasma process is employed. The S-passivated sample shows that the regrowth is slightly suppressed when compared to the sample without the sulphur pre-treatment but not enough for it to be used in a scaled CMOS device.

7.4.2 Electrical Characterisation

The C-V data for S-passivated Ge with 13nm HfO_2 is shown in Figure 76.

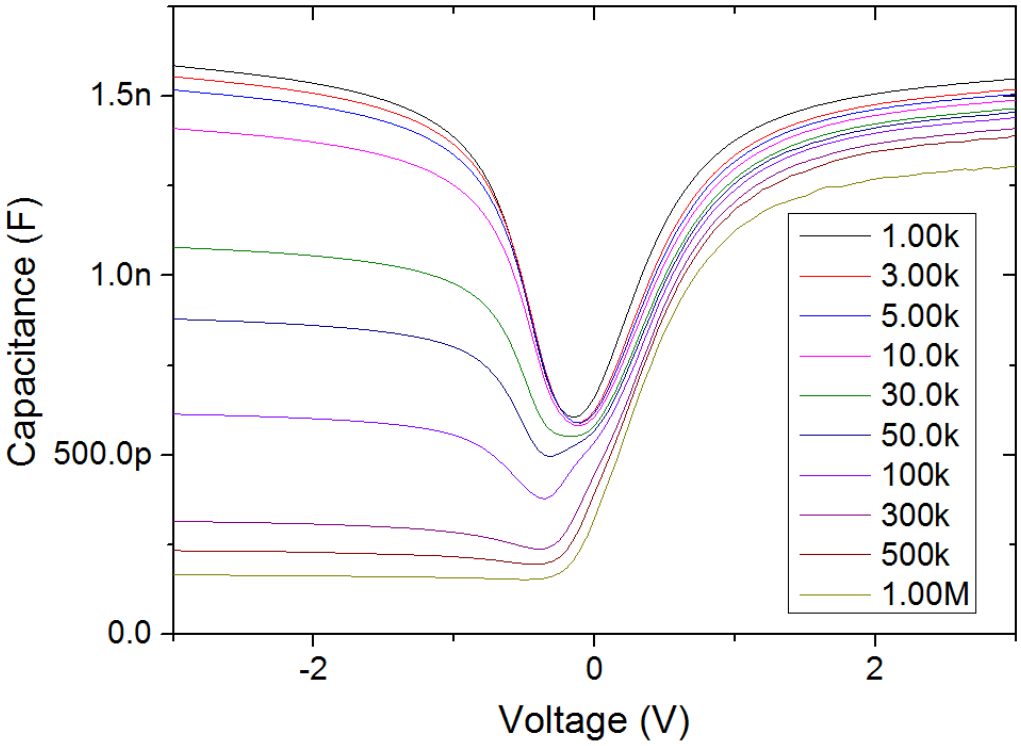

Figure 76. CV data as a function of frequency for S-passivated Ge with 13nm of HfO_2

This shows reasonable C-V characteristics with some frequency dispersion in accumulation and proper inversion characteristics. The EOT of this 4nm and assuming a dielectric constant of 18 for the HfO_2 layer this means there is a contribution to the EOT by the interfacial layer of 1.2nm. This is due to the regrowth of a GeO_x layer during device processing and possible intermixing of HfO_2 with this interfacial layer giving layer with a lower dielectric constant than HfO_2.

7.5 Chapter Summary

In this chapter the effect of sulphur passivation of the germanium surface has been investigated. The influence of S-passivation on the dielectric properties of ALD deposited Al_2O_3 onto the treated semiconductor substrate has been revealed using XPS and capacitance-voltage measurements. It was found that the electrical characteristics of the Al_2O_3-Ge gate stack exhibited lower density of interface states were after S-passivation. The enhanced electrical characteristics were found for both p-type and n-type germanium, implying that the treatment could be used for both nMOSFET and pMOSFET devices. When these samples are compared to the study of Sioncke et al [19] (Figure 20) which employed a similar sample preparation route (the ALD of Al_2O_3 was at 300^{o}C in the reference and at 250^{o}C in this study) the CV characteristics are a comparable. In that study there are features or "bumps" in the CV in the depletion/inversion region which is indicative of interface states for the p-type sample and there is inversion at high frequencies which again is indicative of interface states for the n-type sample. In the study present here, these C-V characteristics are significantly reduced which would indicate a lower D_{it}. As the authors in [19] claim a D_{it} that is in the low $10^{11}cm^{-2}eV^{-1}$ region which is low enough for CMOS operation it can be concluded that the results from this study are also low enough for CMOS operation. The results presented in this study show CV results which are more similar to those presented by Merckling et al [18](Figure 19)in which the S-passivation was achieved under ultrahigh

vacuum conditions using H_2S doses with subsequent in-situ deposition of Al_2O_3 by MBE. An explanation for this could be because the samples in this study (and from Sioncke et al [19]) have both been exposed to air and as shown by Milojevic et al [14] (Figure 13) samples can undergo changes in the ALD chamber but perhaps the sample preparation was better in this study (for example the samples were loaded in the ALD reactor less than 1 minute after $(NH_4)_2S$ treatment and ALD growth was initiated around 1 minute after the ALD reactor had been pumped down) meaning that the sulphur had less time exposed to oxygen (either in the air or in the reactor) which could degrade the Ge-S surface. This cannot be said conclusively, though as the authors in [19] do not state the timings between processes. The same authors (Sioncke et al) also exposed a cleaned Ge wafer to H_2S (at 20Torr) and in situ grew Al_2O_3 on top by ALD [53]. They found that these gate stacks showed different behaviour depending on the oxidant used in the ALD process (H_2O or O_3) with both exhibiting poorer CV characteristics then presented in this study. As ALD is the more technically relevant manufacturing technique for high performance CMOS fabrication this shows that it is important to do these studies using ALD as there are differences in the electrical properties of gate stacks using processes that grow nominally the same gate stack. The conduction band offsets were found to be 3.3eV and 3.61eV for S-passivated and untreated samples respectively which is well above the necessary 1eV for scaled devices but differ slightly from the conduction band offset of 2.74eV reported by

Chellappan et al [20]. The reason for this difference is unclear. The device performances for samples grown with HfO2 were found to be not as good due to the regrowth of an unwanted GeO_x layer at the interface and possible intermixing with the HfO_2. This GeO_x layer could have grown during the time it took to heat the ALD reactor up to 350^oC from 250^oC. Sioncke et al [19] found that high-k oxides (ZrO_2 or HfO_2) degraded the performance of these MOS devices when the high-k oxide is in direct contact with the Ge-S surface even further than the results presented in this study as shown in Figure 22d which also on n-type Ge. The difference is probably attributable to the GeO_x layer formed in this study during processing which the authors in [19] did not report.

8.1 Main Conclusions

Doping of hafnium oxide with titanium was found to be very effective at significantly increasing the dielectric constant of the film with only small differences in the leakage currents. The addition of the Ti also keeps the HfO_2 amorphous after annealing which is preferable as grain boundaries are known to provide leakage pathways through the device.

Three different systems of fabricating gate stacks on germanium were employed. Of these the most promising for producing scaled devices was by thermally cleaning the germanium in UHV and exposing the sample to Al flux to make an ultra-thin Al_2O_3 layer and the subsequent deposition of HfO_2 to reduce the leakage current. This made a lowest EOT of 1.3nm with reasonable leakage current.

S-passivation was investigated and was found to be effective at passivating interface states across the band gap with a conduction band offset of 3.3eV which is well above the necessary 1eV required to be an effective barrier of carrier injection across the device.

Plasma enhanced ALD was found to be unsuitable for a fully ALD process as there is significant regrowth of a GeO_x layer meaning that scaling down the EOT would be problematic due to the low dielectric constant of this interfacial layer.

8.2 Prospects of Future work

Further work on scaling down the EOT of the samples so that they reach the 0.7nm required by ITRS needs to be done. Integration of the higher k $Ti_{0.5}Hf_{0.5}O_2$ is one possible route for this.

Further optimisation of the gate stack using S-passivation could yield an answer to the possible integration of Ge pMOSFETs and III-V nMOSFETs as sulphur has been shown to be effective in passivating interface states for both systems.

Temperature dependent measurements for accurately probing the interface states would give a better indication of the quality of the gate stacks as the density of interface states is known to be overestimated when measured at room temperature.

Putting these gate stacks into a MOSFET would be useful so that device properties such as mobility could be measured and if these were to be on 3D transistor architecture would give an indication of their suitability for future MOSFET iterations.

Other gate stacks such as rare earth in contact with the germanium channel are a promising area for extremely scaled devices as there is no low k interfacial layer meaning devices performance could be dramatically improved.

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