Development of a novel series interconnect for thin-film photovoltaics

M. L. Crozier

Submitted for the qualification of Doctor of Engineering (EngD)

Heriot Watt University

May 2015

The copyright in this thesis is owned by the author. Any quotation from the thesis or use of any of the information contained in it must acknowledge this thesis as the source of the quotation or information.

I. Abstract

Thin-film photovoltaics (TF-PV) offer possible cost savings from reduced semiconductor usage compared to the incumbent crystalline silicon technology. During manufacture TF-PV devices are deposited onto a large glass panel and split into many, series interconnected, cells in order to obtain a useful electrical output. M-Solv has patented a novel process to do this series interconnection in a single step, One Step Interconnect (OSI), after the deposition of all layers. This has a number of benefits compared to the conventional process including, but not limited to, reduced capital cost by ~30%, reduced panel transit time and reduced energy usage.

In this thesis OSI is introduced, the individual processes developed (laser scribing, inkjet printing of insulator and conductor) and working modules manufactured. The electrical performance of the manufactured modules compare favourably with reference material from the same deposition run and modules interconnected in the conventional way. Fill factor (FF) is the principle metric when determining the quality of series interconnection and very high FF, ~80%, have been shown by OSI cells. Preliminary lifetime testing guided by the IEC 61646 specification has been carried out and the results are promising with OSI cells surviving more than double the required number of thermal cycles from -40 to +85°C with no sign of performance degradation.

II. Acknowledgements

I would like to thank everyone at M-Solv for their help and support during this project particularly my industrial supervisor, Adam Brunton, whose enthusiasm for the subject kept me going when things were going wrong and Vijay Tailor for extensive tech support. I am also grateful to my academic supervisor Jon Shephard for his words of encouragement and support throughout.

I would also like to acknowledge the kind support of colleagues at the Centre of Renewable Energy Systems and Technology (CREST), Loughborough University, the Centre for Solar Energy Research (CSER), Glyndŵr University and Colorado State University (CSU) for supplying the PV material that allowed me to do this work. Particular thanks go to Giray Kartopu (CSER) and Piotr Kaminski (CREST). For the excellent SEM/FIB cross sections credit goes to Ali Abbas (CREST).

The EngD has been financially supported by M-Solv Ltd, Oxford and EPSRC. I am grateful to the UK Technology Strategy Board (TSB) for supporting us with 2 years of funding, IMP2, which allowed a lot of this work to take place.

III. Declaration

ACADEMIC REGISTRY

Research Thesis Submission

Name:	Mickey Crozier		
School/PGI:	IDC in Optics and Photonics, EPS		
Version: *(i.e. First, Resubmission, Final)*	First	Degree Sought (Award **and** Subject area)	Engineering Doctorate (EngD)

Declaration

In accordance with the appropriate regulations I hereby submit my thesis and I declare that:

1) the thesis embodies the results of my own work and has been composed by myself
2) where appropriate, I have made acknowledgement of the work of others and have made reference to work carried out in collaboration with other persons
3) the thesis is the correct version of the thesis for submission and is the same version as any electronic versions submitted*.
4) my thesis for the award referred to, deposited in the Heriot-Watt University Library, should be made available for loan or photocopying and be available via the Institutional Repository, subject to such conditions as the Librarian may require
5) I understand that as a student of the University I am required to abide by the Regulations of the University and to conform to its discipline.

* *Please note that it is the responsibility of the candidate to ensure that the correct version of the thesis is submitted.*

Signature of Candidate:	[signature]	Date:	25/09/15

Submission

Submitted By *(name in capitals):*	
Signature of Individual Submitting:	
Date Submitted:	

For Completion in the Student Service Centre (SSC)

Received in the SSC by *(name in capitals):*			
Method of Submission *(Handed in to SSC; posted through internal/external mail):*			
E-thesis Submitted (mandatory for final theses)			
Signature:		Date:	

IV. Contents

I. Abstract i

II. Acknowledgements ii

III. Declaration iii

IV. Contents v

V. List of Publications ix

VI. List of Abbreviations x

Chapter 1 : Introduction 1

1.1 Solar energy 1

1.2 Thin-film PV 2

1.3 Conventional series interconnect 3

1.4 One Step Interconnect (OSI) 4

1.5 References 6

Chapter 2 : Literature Review 8

2.1 Novel interconnects 8

2.2 Laser scribing of thin film PV 12

2.2.1 Laser scribing of thin film silicon (TF-Si) 14

2.2.2 Laser scribing of Cadmium Telluride (CdTe) 23

2.2.3 Laser scribing of Copper Indium Gallium Selenide (CIGS) 24

2.2.4 Summary of laser processing for TF-PV 29

2.3 Fundamentals of inkjet deposition 29

2.3.1 ‘Drop watching’ 33

2.3.2 Effect of voltage waveform on print characteristics 34

2.3.3 Jetable fluids 39

2.3.4 Drop/surface interactions 41

2.3.5 Drop coalescence 47

2.4 Functional inks formulation and processing 48

2.4.1 Formulation of inks 48

2.4.2 Formulation of conductive nano-particle based inkjet inks 49
2.4.3 Post deposition processing of conductive inks 50
2.4.4 Thermal processing of conductive inks.. 51
2.4.5 Photonic Sintering 53
2.4.6 Electrical sintering 56
2.4.7 Plasma Sintering 57
2.4.8 Microwave sintering.. 60
2.4.9 Combined approaches to sintering 65
2.4.10 Chemical sintering and 'self-sintering' inks 67
2.4.11 Summary and conclusions of inkjet deposition for functional materials .. 69
2.5 References 70
Chapter 3 : Laser Processing for OSI 77
3.1 Introduction 77
3.2 Experimental setup for superstrate cells 79
3.2.1 Lasers 79
3.2.2 Optical setup.. 79
3.2.3 Basic procedure for process optimisation 82
3.3 Thin-film Silicon 84
3.3.1 TF-Si 1064nm, film side processing 85
3.3.2 TF-Si 1064nm, through the glass processing 88
3.3.3 TF-Si 532nm, through the glass processing 90
3.4 Electrical verification of laser processes on TF-Si 95
3.4.1 Measuring cell performance using a solar simulator 95
3.4.2 Impact of anneal on TF-Si performance 101
3.5 Cadmium Telluride... 107
3.5.1 CdTe Scribe development on FTO substrates... 107
3.5.2 CdTe Scribe verification test structures 109
3.6 CIGS – substrate cells 117

3.6.1 Lasers for CIGS ... 119
3.6.2 Optical Setup ... 119
3.6.3 1μm scribing of CIGS ... 120
3.6.4 1.5μm CIGS scribing ... 127
3.6.5 Modelling of CIGS scribing process ... 130
3.6.6 CIGS Conclusions ... 133
3.7 References ... 135
Chapter 4 : Inkjet printing for OSI ... 138
4.1 Experimental Setup ... 139
4.1.1 Print Hardware ... 139
4.2 Insulator deposition ... 146
4.2.1 Controlling insulator fill ... 147
4.2.2 Insulator thermal stability ... 149
4.2.3 Summary of insulator deposition ... 152
4.3 Conductor Deposition ... 153
4.3.1 Ink/TCO contact resistance ... 154
4.3.2 Wetting of conductive inks on back contact ... 157
4.4 Matching ink wetting to substrate ... 160
4.4.1 Cracking of conductive inks ... 161
4.4.2 Plasma surface treatment for wetting modification ... 164
4.4.3 Summary of conductive ink deposition ... 167
4.5 Conclusions ... 168
4.6 References ... 170
Chapter 5 : OSI mini-modules on CdTe ... 172
5.1 Mini-module manufacture on CSU CdTe ... 172
5.2 Mini-module manufacture on CSER CdTe ... 181
5.2.1 CSER mini-module ... 182
5.3 Comparison of OSI with the conventional process ... 188

5.4 Accelerated lifetime testing 190
5.4.1 Encapsulation and damp heat testing 191
5.4.2 Thermal cycling 194
5.5 Conclusion 196
5.6 References 198
Chapter 6 : The case for OSI 200
6.1 Benefits of OSI 200
6.1.1 Reduced Line Length 200
6.1.2 Reduced total cost of ownership of interconnect tooling 205
6.1.3 Process advantages 208
6.2 Conclusions and Further Work 208
6.3 References 211

V. List of Publications

B. Maniscalco, P. M. Kaminski, G. Claudio, M. Walls, Y. Yu, D. Mansfield, M. L. Crozier, and A. Brunton, “Characterisation of laser scribes in thin film photovoltaics by coherence correlation interferometry,” 27th Eur. Photovolt. Sol. Energy Conf. Exhib., pp. 2808 – 2811, 2012.

M.L. Crozier, A.N.Brunton, A. Abbas, J.W.Bowers, P. M. K. J.D.Shephard, and J.M.Walls, “One step thin-film PV interconnection process using laser and inkjet,” in 39th IEEE PVSC conference proceedings, 2013.

P. M. Kaminski, A. Abbas, J. W. Bowers, G. Claudio, B. Maniscalco, J. M. Walls, M. L. Crozier, and a. N. Brunton, “Characterization of contacts produced using a laser ablation/inkjet one step interconnect process for thin film photovoltaics,” IEEE 39th Photovolt. Spec. Conf., pp. 1694–1699, Jun. 2013.

M. L. Crozier, A. Brunton, M. Jiang, S. Henley, J. Shephard, A. Abbas, J. Bowers, P. M. Kaminski, and J. M. Walls, “Inkjet and laser hybrid processing for the series interconnection of TF-PV,” in 10th Photovoltaic Science, Applications and Technology (PV-SAT 10), 2014.

M. L. Crozier, A. Brunton, G. Kartopu, and S. Irvine, “A one step process for the series interconnection of thin-film PV,” in SNEC 8th International Photovoltaic Power Generation Conference, 2014.

M. L. Crozier, P. Adamson, A. Brunton, S. J. Henley, J. D. Shephard, G. Kartopu, S. J. C. Irvine, P. M. Kaminski, and J. M. Walls, “Recent developments toward a one step thin-film PV interconnection process using laser scribing and inkjet printing,” IEEE 40th Photovolt. Spec. Conf., vol. 1, pp. 2784 – 2788, 2014.

M. L. Crozier, A. Brunton, S. J. Henley, J. D. Shephard, a. Abbas, J. W. Bowers, P. M. Kaminski, and J. M. Walls, “Inkjet and laser hybrid processing for series interconnection of thin film photovoltaics,” Mater. Res. Innov., vol. 18, no. 7, pp. 509–514, Nov. 2014.

S. D. Hodgson, G. Kartopu, M. L. Crozier, P. Adamson, V. Barrioz, S. Rugen-Hankey, E. Tejedor, D. Dupin, A. J. Clayton, W. S. M. Brooks, D. A. Lamb, A. Brunton, and S. J. C. Irvine, “Performance of EVA Encapsulated CdTe Devices and Micro-Modules Grown by MOCVD under Heat/Humidity Testing,” in 29th European PV Solar Energy Conference and Exhbition (EUPVSEC), 2014, pp. 1840 – 1843.

G. Kartopu, M. L. Crozier, A. Brunton, B. L. Williams, V. Zardetto, V. Barrioz, S. Hodgson, S. Jones, W. M. M. Kessels, M. Creatore, and S. J. C. Irvine, “Comparative study of conventional vs . one-step-interconnected (OSI) monolithic CdTe modules,” in 11th Photovoltaic Science, Applications and Technology (PV-SAT 11), 2015.

VI. List of Abbreviations

ADSA-P - Axisymmetric Drop Shape Analysis – Profile

AM – Air Mass

AR – Antireflection

AZO – Aluminium doped Zinc Oxide

CCD – Charge Coupled Device

CCT – Critical Cracking Thickness

CdS – Cadmium Sulphide

CdTe – Cadmium Telluride

CIGS – Copper Indium Gallium di-Selenide

CREST – Centre for Renewable Energy Systems and Technology

CSER – Centre for Solar Energy Research

CSS – Closed Space Sublimation

CSU – Colorado State University

CTE – Coefficient of Thermal Expansion

CW – Continuous Wave

DMP – Dimatix Materials Printer

DOE – Diffractive Optical Element

DPI – Dots Per Inch

DPSS – Diode Pumped Solid State

EDX – Energy Dispersive X-Ray (spectroscopy)

EL – Electroluminescence

EVA – Ethylene Vinyl Acetate

FE – Finite Element

FF – Fill Factor

FIB – Focussed Ion Beam

FTO – Fluorine dope Tin Oxide

HAZ – Heat Affected Zone

HVFM - Hybrid Variable Frequency Microwave

IEA – International Energy Agency

IEC – International Electrotechnical Commission

IJ – Inkjet

IP – Intellectual Property

IPL – Intense Pulsed Light

IR – Infrared

ITO – Tin doped Indium Oxide

LBIC – Laser Beam Induced Current

LED – Light Emitting Diode

LMIS – Liquid Metal Ion Source

MOCVD – Metal Organic Chemical Vapour Deposition

ND – Neutral Density

NIR – Near Infrared

NP – Nanoparticle

NREL – National Renewable Energy Laboratory

OLED – Organic Light Emitting Diode

OM – Organo-Metallic

OPV – Organic Photovoltaics

OSI – One Step Interconnect

PAA – Poly Acrylic Acid

PDAC – Poly Diallydimethyl Ammonium Chloride

PEN - Polyethylene Naphthalate

PET - Polyethylene Terephthalate

PI – Polyimide

PIJ – Piezo Inkjet

PMMA – Poly Methyl Methacrylate

PRF – Pulse Repetition Frequency

PV – Photovoltaics

PVP – Poly Vinyl Pyrrolidone

R2R – Roll to Roll

RF – Radio Frequency

RMS – Route Mean Square

RTA – Rapid Thermal Annealing

SAM – Self Assembled Monolayer

SEM – Scanning Electron Microscopy

SSA – Specific Surface Area

STC – Standard Test Conditions

SWLI – Scanning White Light Interferometer

TCO – Transparent Conductive Oxide

TEM – Transmission Electron Microscopy

TF-PV – Thin-Film Photovoltaics

TF-Si – Thin Film Silicon

TFT – Thin Film Transistor

TGA – Thermogravimetric Analysis

TIJ – Thermal Inkjet

TLM – Transmission Line Measurement

UV – Ultra Violet

VIA - Vertical Interconnect Access

XRD – X-Ray Diffraction

Chapter 1 : Introduction

1.1 Solar energy

Investment in and uptake of solar energy is directly linked to how cost competitive it is with other methods of electricity generation. During the 2000's as the oil price rose from $20-$30 per barrel up to a peak of almost $150 per barrel [1] investment in solar soared almost 10x [2], total installed solar capacity also increased at a greater rate [3]. Furthermore solar energy is seen as a key part in a renewable mix to help tackle the energy trilemma of energy cost, carbon emissions and energy security.

Price per Watt is used as a guide to the cost of solar to allow comparisons between technologies. As materials and manufacturing costs decline and efficiencies increase, the price per Watt decreases [4]. For wide spread adoption the cost of electricity from solar must reach grid parity i.e. it must cost the same, or less, to generate electricity from solar cells as it does by conventional means. Solar panels are, as standard, guaranteed for 20-25 years and have few running costs associated with them therefore the cost of electricity from solar photovoltaics (PV) is dominated by the initial module and associated infrastructure costs (balance of systems). The cost per Watt is defined as the cost of the panel divided by the nominal power produced when used at standard test conditions (STC) which are 1,000W/m^2 irradiance, air mass (AM) 1.5 spectrum and module temperature of 25°C [5].

The drive for grid parity of solar cells has led to a concerted effort to reduce the price of modules. According to the 2014 International Energy Agency (IEA) Solar Photovoltaic Roadmap module costs have fallen by 5x in the 6 years to 2014 [6]. This reduction in costs has been possible for a variety of reasons but has been dominated by the reduction in silicon price and more cost effective manufacturing processes which use less materials.

As of 2013 86% [7] of the solar PV market was held by the original crystalline silicon technology. Crystalline silicon photovoltaics are mature and well developed with little scope for large improvements in efficiency or cost however the majority of the installation cost is still the panel cost (~60%) of which ~50% is from the cost of the silicon [8]. In order to make a significant impact it is necessary to migrate to the next generation of cell technologies, these include thin-film (TF), concentrator and organic photovoltaics (OPV). Of these technologies TF-PV is the most established with ~10% market share, led by a few large companies such as First Solar, using Cadmium

Telluride (CdTe) [9]–[11] and Solar Frontier, using Copper Indium Gallium di-Selenide (CIGS) [12], [13] semiconductors. The main advantage of thin-film cells compared to crystalline silicon is much reduced material usage. TF uses direct semiconductors (CdTe, CIGS) whereas crystalline silicon is an indirect semiconductor meaning that to absorb the total solar irradiance a crystalline cell must be ~150μm's thick where as a TF cell needs to be 2-3μm's [14].

The work presented in this thesis has focussed on a new manufacturing technique designed to reduce the cost of manufacture of TF modules including CdTe, CIGS and TF-Si, in order to improve their competitive position with respect to crystalline silicon.

1.2 Thin-film PV

There are three established inorganic semiconductors used for TF-PV, Cadmium Telluride (CdTe) [9]–[11], amorphous Silicon (a:Si) [15], [16] and Copper Indium Gallium Selenide (CIGS) [12], [13]. All PV solar cells work in essentially the same way. Solar photons are absorbed by a semiconductor, provided they are of energy equal or greater than the band gap. The absorbed photons promote charge carriers into the conduction band. This creates excess carriers compared to thermal equilibrium and these carriers are free to move. In the presence of a potential barrier, such as a pn junction, charge separation occurs. Provided there is a conduction path current flow results. Therefore the properties required for a PV solar cell are [17]:

- Semiconductor of suitable band gap for the solar spectrum (ideally ~1.5eV [17])
- Charge separation – usually achieved with a pn junction
- Contacts to both sides of the junction to allow charge to flow

TF cells are built up of epitaxial layers with a transparent conductive oxide (TCO) contact on the light collecting side and a thin metallic back contact. These cell are usually configured in one of two ways, either superstrate (CdTe, a:Si) or substrate (CIGS), see Figure 1.1.

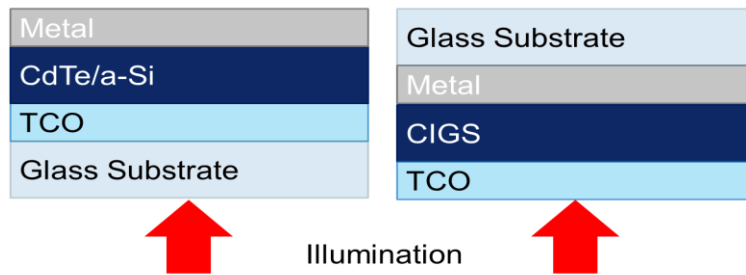


Figure 1.1: Left; a superstrate TF cell, CdTe and thin film Silicon are usually constructed in this configuration. Right; a substrate TF cell, CIGS is constructed in this configuration. Only the main layers are shown. In practice, there are other layers such as Cadmium Sulphide (<100nm) in a CdTe cell used to form the pn junction or window layers used to match electrical or growth characteristics of two of the main layers.

1.3 Conventional series interconnect

The current generated by a PV cell is directly proportional to the amount of sunlight incident on the surface whereas the voltage is governed by the bandgap [18]. This means that for a large area panel (~1 m^2) there would be a large current (~200A) and a low voltage (0.5-1V) however for integration with the grid a lower current (~2A) and a higher voltage (50-80V) is required to avoid resistive losses. To achieve the desired voltage and current output the panel is divided, during the manufacturing process, into many (>100) smaller cells connected in series.

Each of the layers that make up the TF cell are deposited onto a, typically, glass substrate and between each deposition step the layers are scribed either mechanically or more commonly using a laser [11], [17]. Each scribe is offset producing a current path between the TCO of one cell and the metal contact of the adjacent, Figure 1.2. The three scribes are usually labelled P1, P2 and P3.

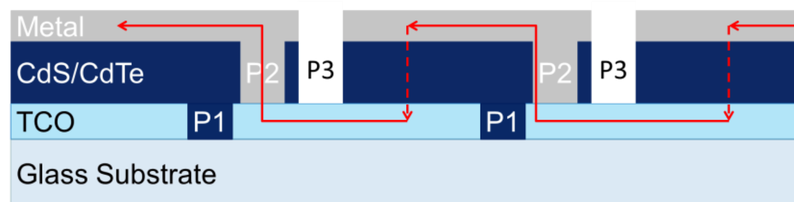


Figure 1.2: The conventional process for the series interconnection of a TF cell. P1 isolates the TCO, P2 provides a connection between the front and back contacts and P3 isolates the metal contact. It is common for these scribes to be made with a laser except in the case of CIGS, discussed in more detail later. The arrows show the current path through the interconnect (solid line) and cell (dotted line).

1.4 One Step Interconnect (OSI)

This thesis presents the development of an alternative manufacturing process for the series interconnection of TFPV. The work has been completed in conjunction with M-Solv UK Ltd, Oxford who hold IP in this area [19]. The M-Solv process, termed 'One Step Interconnect' or OSI, uses a combination of laser subtractive and functional additive manufacture to series interconnect cells in a single pass after the deposition of all layers.

Figure 1.3 shows OSI on a superstrate CdTe cell. Simultaneously 3 lasers scribe 3 lines into the stack; scribe A to the glass and scribes B and P3 to the TCO. Scribe A is in-filled by inkjet with an insulating material. A conductive ink is then deposited into scribe B and bridges across the insulator to the metal contact thus connecting the TCO of one cell to the metal back contact of the adjacent cell.

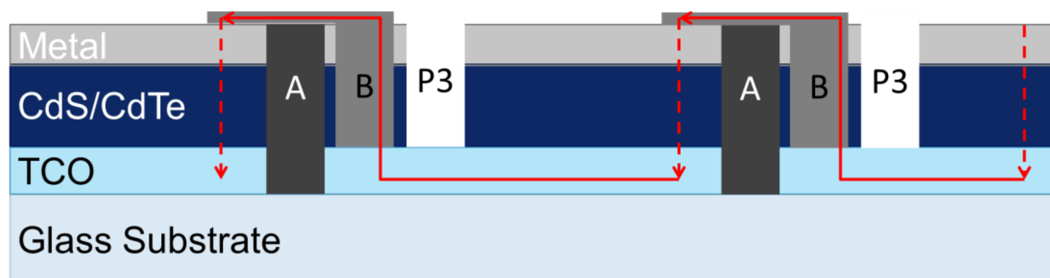


Figure 1.3: The OSI process. All three scribes, A, B and P3 are completed simultaneously; inkjet heads are aligned on the process head to follow directly behind the laser path. As soon as the laser creates the scribes scribe A is filled with insulator and then metal ink connects the TCO of one cell to the metal back contact of the adjacent creating a series connection.

OSI has a number of benefits compared to the conventional interconnect process:

- In OSI the entire interconnect is manufactured in a single pass of a single process head removing the requirement for the alignment steps that have to occur between the P1, P2 and P3 scribes.
- This, in return, allows a decrease in interconnect width, which does not contribute to electricity generation, resulting in increased panel efficiency.
- The material deposition can occur without breaking vacuum, allowing better control over layer interfaces.
- There is a large reduction in capital equipment cost and line foot print since three laser scribing platforms can be removed and replaced with one OSI tool.

- The total temperature change of the panel in transit is reduced due to the removal of the ambient temperature, atmospheric laser processes between each of the three deposition steps.
- The flatter temperature profile reduces energy consumption, lessens thermally induced panel stress and removes the requirement for further capital equipment in the form of heaters and coolers.

The cost of a panel and therefore the cost per Watt are all calculated by taking into account the fixed costs of capital equipment and the overhead rate of the line. Implementing OSI and therefore reducing capital cost and energy consumption directly impacts the cost per Watt for TF-PV.

1.5 References

[1] R. a. Lizardo and A. V. Mollick, "Oil price fluctuations and U.S. dollar exchange rates," *Energy Econ.*, vol. 32, no. 2, pp. 399–408, Mar. 2010.

[2] C. E. Jennings, R. M. Margolis, and J. E. Bartlett, "A Historical Analysis of Investment in Solar Energy Technologies (2000-2007)," *NREL Tech. Rep. NREL/TP-6A2-43602*, no. December, 2008.

[3] SEIA, "US Solar Electric Installations 2000-2010," *http://www.seia.org/cs/research/industry_data*, 2010. .

[4] DECC, "Review of the generation costs and deployment potential of renewable electricity technologies in the UK Study Report," *Report*, 2011.

[5] C. Del Canizo, G. Del Coso, and W. C. Sinke, "Crystalline silicon solar module technology: Towards the 1 € per watt-peak goal," *Prog. photovoltaics Res. Appl.*, vol. 17, no. 3, pp. 199–209, 2009.

[6] IEA, "Solar Photovoltaics Technology Roadmap," 2014.

[7] B. Bakhiyi, F. Labrèche, and J. Zayed, "The photovoltaic industry on the path to a sustainable future — Environmental and occupational health issues," *Environ. Int.*, vol. 73, pp. 224–234, 2014.

[8] F. Z.D. Pan, Q.S. Wei, J.C. Liu, Zheng, "New changes and influences of the international Photovoltaics market and coping strategies of the Chinese Photovoltaic Industry," in *Biotechnology, Agriculture, Environment and Energy*, 2015, pp. 9–13.

[9] P. V Meyers, "DESIGN OF A THIN FILM CdTe S O L A R CELL Summary Cadmium telluride was originally considered for thin film solar cells because of its optimum band gap , high optical absorption coefficient and ability to be doped . Furthermore , it is a stable compound w," vol. 23, pp. 59–67, 1988.

[10] N. Romeo, a. Bosio, V. Canevari, and a. Podestà, "Recent progress on CdTe/CdS thin film solar cells," *Sol. Energy*, vol. 77, no. 6, pp. 795–801, Dec. 2004.

[11] P. V Meyers and C. E. Mark, "FIRST SOLAR POLYCRYSTALLINE CdTe THIN FILM PV," pp. 2024–2027, 2006.

[12] N. G. Dhere, "Toward GW/year of CIGS production within the next decade," *Sol. Energy Mater. Sol. Cells*, vol. 91, no. 15–16, pp. 1376–1382, Sep. 2007.

[13] M. a. Contreras, M. J. Romero, and R. Noufi, "Characterization of Cu(In,Ga)Se2 materials used in record performance solar cells," *Thin Solid Films*, vol. 511–512, pp. 51–54, Jul. 2006.

[14] B. Parida, S. Iniyan, and R. Goic, "A review of solar photovoltaic technologies," *Renew. Sustain. Energy Rev.*, vol. 15, no. 3, pp. 1625–1636, Apr. 2011.

[15] D. E. Carlson and C. R. Wronski, “Amorphous silicon solar cell Amorphous silicon solar cell,” *Appl. Phys.*, vol. 671, no. 1976, pp. 1–4, 1976.

[16] S. Benagli, D. Borrello, E. Vallat-Sauvain, J. Meier, U. Kroll, J. Hötzel, J. Bailat, J. Steinhauser, M. Marmelo, G. Monteduro, and L. Castens, “High-Efficiency Amorphous Silicon Devices on LPCVD-ZnO TCO Prepared in Industrial KAI TM-M R&D Reactor,” in *European Photovoltaic Solar Energy Conference and Exhibition*, 2009, no. September, pp. 21–25.

[17] K. L. Chopra, P. D. Paulson, and V. Dutta, “Thin-film solar cells: an overview,” *Prog. PV Res. Appl.*, vol. 12, no. 23, pp. 69–92, Mar. 2004.

[18] P. Baruch, a. De Vos, P. T. Landsberg, and J. E. Parrott, “On some thermodynamic aspects of photovoltaic solar energy conversion,” *Sol. Energy Mater. Sol. Cells*, vol. 36, pp. 201–222, 1995.

[19] A. Brunton, “Method and apparatus for dividing thin film device into separate cells,” GB24746652011.

Chapter 2 : Literature Review

2.1 Novel interconnects

M-Solv is not the only entity currently interested in novel ways of series interconnecting thin film solar cells. Next generation interconnective laser patterning of CIGS thin film modules [1] and laser micro-welded interconnections in CIGS PV modules [2] have been introduced as a method for interconnecting Copper Indium Gallium Selenide (CIGS). The first step is the standard P1 process where the Molybdenum (Mo) contact is scribed using a 1064 nm laser (Figure 2.1, left). The second step occurs after the deposition of the entire cell and uses a 532 nm laser to metallise the CIGS to create a conductive path between the Mo and the TCO, in this case Zinc Oxide (ZnO) (Figure 2.1, centre). The process is termed laser micro-welding. The final step is the standard mechanical P3 scribe, the current industry standard for CIGS (Figure 2.1, right). The benefits of this process are also common to the OSI process in that there is no need to break vacuum and therefore there is better control of layer interfaces and lower end to end process times.

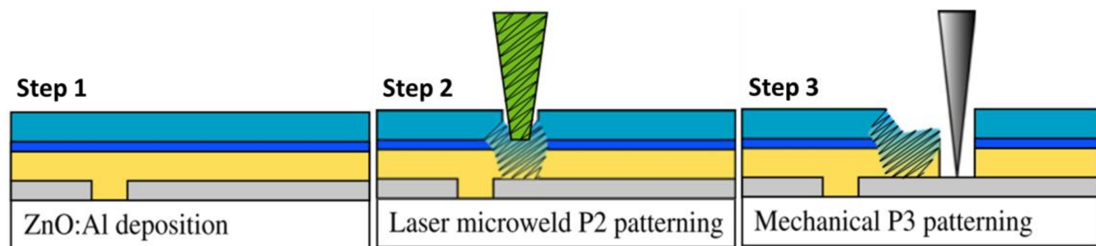


Figure 2.1: The laser microweld process. The P1 and P3 steps are completed as before. Instead of a P2 scribe to connect front and back contacts once all the deposition has occurred a laser is used to locally transform the CIGS into a conductive compound between the two scribes [1].

37 mini-modules ranging in sizes from 37cm^2 to 900cm^2 were produced from different batches of CIGS using different process parameters for the micro-weld. Reference samples were also produced in the standard way for comparison [1].

The initial results look reasonably promising, the majority of mini-modules were comparable in efficiency and fill-factor (FF) with the reference samples and some samples even achieved slightly higher efficiencies, see Figure 2.2. To produce the micro-welds a defocused laser beam with a wavelength of 532 nm was used with a variety of pulse repetition rates (PRF), fluence and beam speeds. The best results were obtained at ~35 μJ, 65 kHz and 17 mm/s. The trend appears to be a slightly lower FF

attributed to a higher than normal series resistance within the micro-weld compared to the standard interconnect.

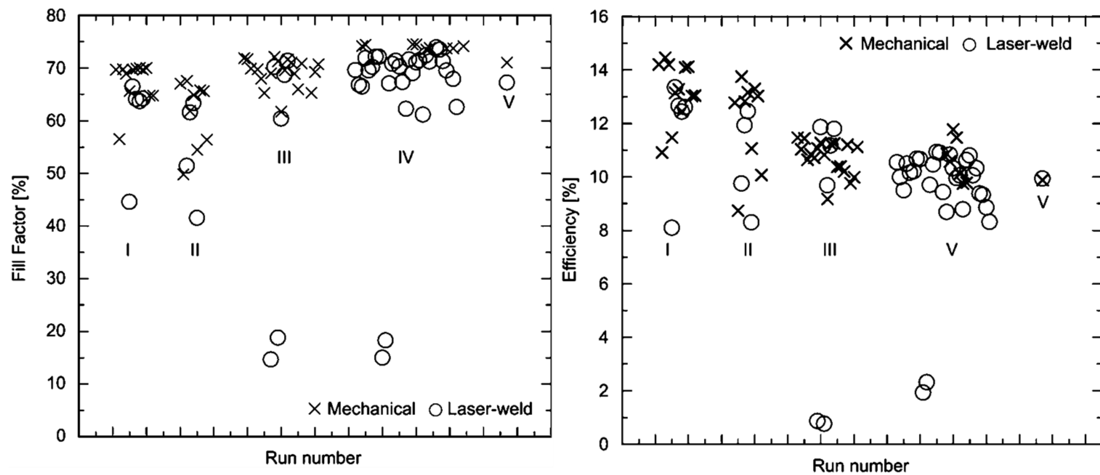


Figure 2.2: Left; plot of fill factor and right; efficiency of the cells created with the standard mechanical process and the laser micro-weld [1].

Building on these results, further analysis of the mechanical properties of the micro-weld was carried out by the same group [2]. For the second round of tests 244 mini-modules were produced using laser micro-welding from two batches of CIGS and both focused/defocused beams were tested along with pulse repetition rates of 20, 50 and 80 kHz using the same 532 nm laser. It was found that the higher pulse energies associated with the 20 kHz rep rate produced complete ablation of the stack before any change in material composition took place and no modules could be manufactured at this PRF. The 50 and 80 kHz results were more successful, with similar electrical results to the original trials. It was found that both the Mo layer and glass were significantly damaged in the best performing micro-welds. Defocusing the laser spot reduced the damage to the Mo layer and it was hypothesised that using beam shaping optics to create a top hat profile could remove the damage to the Mo whilst still achieving good electrical results. The glass damage however seems to be related to the total energy deposited into the material as defocusing had no appreciable effect, see Figure 2.3.

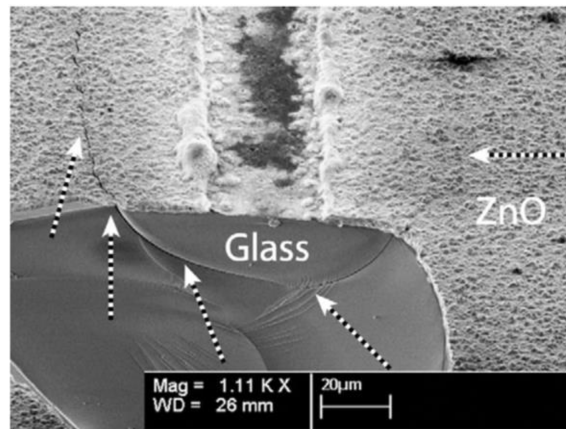


Figure 2.3: SEM image of one of the laser micro-welded interconnects. Note the cracking of the glass substrate [2].

Energy Dispersive X-Ray Spectroscopy (EDX) measurements around the laser micro-weld site were presented in order to identify the material which makes up the micro-weld. Although the data isn't conclusive it appears that the conductive regions are metal rich and selenium poor as perhaps would be expected. The final data set presented is dry heat stability testing of some of the produced modules, these results are far less positive. In the intervening gap between module production (500-1500hours) there was strong performance degradation, up to 50% in some cases. Subsequently, while on test, the performance continued to drop in all but one case. The module that didn't degrade was a less well performing module in which no Mo or glass damage had been observed. Two hypotheses for why the Mo/glass damage created module degradation were put forth. The first is that the damage to the Mo disrupts the circuit causing increased series resistance, the second that cracks in the glass allow atmospheric moisture to enter the samples.

Although the initial results look impressive, the flaws in this interconnect method may result in this process not being practically viable. Firstly, the correlation between good electrical performance and Mo and glass damage will prove a difficult hurdle to overcome. Using beam shaping to create a flat, top-hat, energy distribution will probably eliminate the Mo damage however the glass damage will likely be more difficult to overcome since it is related to total energy. Out of the hypotheses presented for the module degradation it is likely that the ingress of atmospheric humidity into the sample is the principle cause and so without eliminating the glass damage the long term performance of modules manufactured in this way will struggle to meet the requirements of the industry standard 25 year guarantee. The second and possibly more critical problem with this interconnect method is the high laser spot density

required to produce the micro-weld. All of the most successful tests were achieved at frequencies of 50-80 kHz and stage speeds of just 17mm/s. This is far too slow for integration into a commercially viable industrial process. At that rate, with a single beam, it would take about an hour and a half to produce a one full size panel. Alternatively, in order to achieve a beam speed of 1m/s a repetition rate of 3.5MHz is required with the same pulse energy.

A second novel interconnect design has been introduced by Haas et al [3] which is a modification of the standard process. Instead of three scribes, one to isolate the front contact, one to connect front to back and one to isolate the back contact the front and back contacts are only connected by points. In this way the P1 scribe performs the dual function of isolating both contacts over the majority of the interconnect, with an extra P3 scribe around each point contact. This scheme can be seen in Figure 2.4, below.

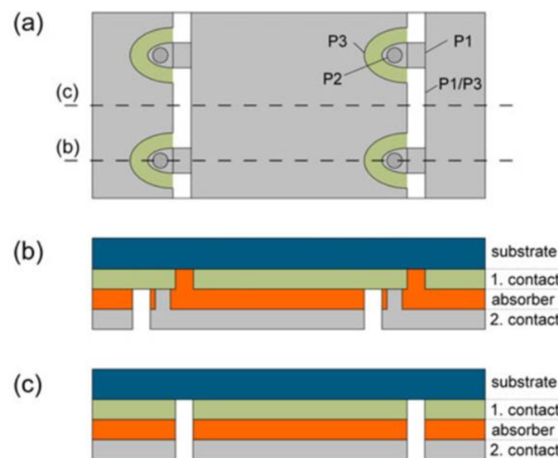


Figure 2.4: Schematic view of the point wise laser interconnect geometry, a) top down view, b) and c) are cross sections at the points noted in a) [3].

This interconnect design results in a massive reduction in dead zone however it is not immediately obvious how large an impact it will have on FF by increased series resistance. This effect has been investigated by Haas; the new interconnection scheme is a trade-off between the Ohmic losses due to the increased contact resistance and the extra active area gained. By taking both these factors into account it is possible to calculate the optimum geometry in terms of cell spacing and spacing between point contacts. Running this theoretical optimisation for three different types of cells a-Si, μc-Si and micromorph Haas calculates that it's possible to increase absolute efficiency by 0.2-0.3%. To test this structure, modules with both the standard interconnect and point interconnects were manufactured. Comparing the standard cell to the point

contact cell the area loss decreased from 5.5% to 2.8%, correspondingly the short circuit current increased by ~3%. This resulted in an average absolute efficiency increase of 0.35%, slightly higher than calculated. The explanation for this is that the cell widths were fixed at 5mm, closer to the optimum width for the point contacts of 4.8mm than for the strips at 6.9mm. This result is very encouraging and although in practice the modified point contact interconnection maybe more difficult to achieve it will probably be worth it for the gain in efficiency for little extra cost.

This interconnection scheme could be integrated with the OSI process very easily. There would have to be an A scribe along the modules length filled with insulator then Vertical Interconnect Access (VIA) to connect the top and bottom contacts and P3 scribes to isolate the VIA, to finish it off short lengths of metal ink could be printed perpendicular to the scribe at each of the VIA points to bridge from the front contact to the back contact. An adapted version of Figure 2.4, the point wise laser contact interconnection can be seen in Figure 2.5 modified using the OSI process.

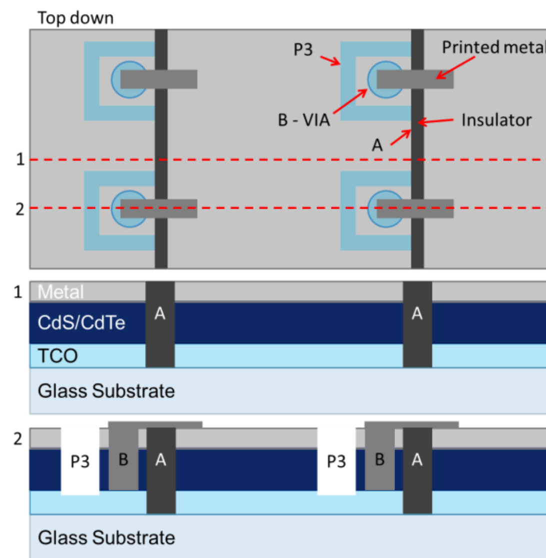


Figure 2.5: OSI applied to the pointwise interconenction introduced by Haas. As before insulator fills the A scribe and metal is printed from the TCO in the B scribe to the metal back contact, the major difference is in this case the B scribe is made of VIAs with short sections of P3 scribe isolating them from the adjacent cell. The figure is an adaption of Figure 2.4.

2.2 Laser scribing of thin film PV

Laser scribing is a key step in the manufacturing process of most TF-PV. The requirements for laser scribing of thin-film Silicon (TF-Si) have been stated [4]

although the general points are applicable to all thin film PV materials. It is stressed that wavelength selection for each of the processes, P1, P2 and P3 is key. The P1 process is usually achieved with the beam incident from the glass side of the glass TCO stack. This is preferable to scribing from the film side as all the energy is absorbed at the layer interface resulting in clean scribe morphology and a lower energy process. The laser wavelength must be transmitted by the glass but absorbed by the TCO. Visible wavelengths are clearly not absorbed by either material since they are both transparent, UV and mid/far IR lasers are not used because glass exhibits strong absorption in these wavelength ranges. Near infra-red sources are ideally suited for the P1 scribe as glass is still transparent but TCO free carrier absorption is increasing meaning that they absorb more strongly [5]. The fundamental of common diode pumped solid lasers such as Nd:YAG or Nd:YVO4 lasers at 1064nm are the ideal choice as the technology is mature, provides compact robust lasers and is relatively cheap and reliable. For selective absorption in the absorber required for the P2 and P3 scribes visible lasers are preferred. A prerequisite of a PV material is the ability to absorb strongly in the visible portion of the spectrum. A visible laser incident from the glass side of the solar cell stack will be transmitted by both the glass and TCO layers and absorbed strongly at the interface between the TCO and absorber. This creates an area of local pressure resulting in an explosive lift off [6] of the absorber which fractures along grain boundaries.

All three scribes must meet several requirements for the process to be optimal, namely they must be:

- Free of defects
- Take up minimum space
- Have good edge quality
- Not limit the takt time (average unit production time) of the production line

Scribe defects could be discontinuities or remaining material. Discontinuities in P1 or P3 create alternative paths for current flow essentially removing that cell from the series connection and reducing the current/voltage accordingly. Remaining material in any of the scribes could again cause alternative paths for current flow or in the case of the P2 scribe a thin layer of remaining semiconductor may increase the contact resistance between the TCO and metal contact resulting in a parasitic loss of current.

The requirement on minimum space is obvious; the area bound by the P1 and P3 scribes is not contributing to the current generation of the cell. Therefore minimising this area increases the overall current, and therefore power, generated by the panel. Current interconnect widths are of the order of a fraction of a millimetre (~0.2-0.5mm). The width of the interconnect can also be linked to the straightness of the scribed line. As each scribe is sequential the second must be aligned to the first leaving enough gap to accommodate any deviation from linear in the first. If all scribes are perfectly straight and well aligned this gap can be minimised thus reducing the total dead zone.

The edge quality of the scribes is important because any defect sites act as recombination centres for the charge carriers and this limits efficiency. Micro cracks or damage caused by thermally affecting the material can increase the defect density and thus reduce the efficiency of the cell. Thermal effects can be reduced by apperturing the beam so that all light incident on the substrate is above removal threshold this then means that the lasers heat affected zone (HAZ) caused by the tails of the Gaussian pulse does not interact with any material. Using a short pulse duration also reduces the amount of thermal damage produced by the laser. Using short pulses (<10 ns) the localised heating produced by the laser doesn't have time to diffuse laterally into the surrounding material and therefore does not cause damage.

The final point, that the process must not limit takt time again is obvious but very important. Takt time is the amount of time that a panel moving through a continuous flow production line spends at each station with the slowest process limiting the throughput. These laser processes are generally low energy and therefore the material can be removed with a single shot. This means that the overlap required to make a continuous scribe is relatively low. In turn this also means that the pulse repetition frequency (PRF) required to move the beam relative to the substrate at a few m/s is fairly modest and can be achieved by most commercially available Diode Pumped Solid State (DPSS) lasers.

2.2.1 Laser scribing of thin film silicon (TF-Si)

Silicon is the most mature of all the PV technologies with the crystalline panels having been around since the 1950's [7]. The drive for ever cheaper solar energy has led to efforts to reduce the amount of material required in a solar cell. Silicon wafers used in

crystalline silicon cells account for over half the cost of manufacture [8]. Crystalline Silicon being an indirect gap semiconductor has a relatively low optical absorption coefficient and so thick layers (>100 μm) are required. To reduce the amount of material required, amorphous Silicon can be used. In its amorphous form silicon becomes a quasi-direct band gap semiconductor with a band gap ~1.8 eV and therefore exhibits a much higher optical absorption coefficient ($>10^5 cm^{-1}$ [9]) compared with crystalline silicon. The benefit of this is that only a few μm's (2-3 μm) of amorphous silicon are required to absorb most of the solar energy reducing the amount of material and the associated costs.

Amorphous silicon initially appears to be the natural choice for a solar material. Silicon is abundant, 27.7% in the earth's crust compared with Cadmium at 0.15 ppm [10], there is already an established electronics industry based on Silicon and amorphous silicon is already used in TFT displays and the deposition equipment used in the display market is suitable for producing a-Si PV [8]. However there have been a number of inherent materials problems with amorphous silicon. Firstly amorphous silicon has many dangling bonds that can act as recombination centres limiting the minority carrier lifetime and therefore the efficiency. It is well known that by incorporating around 10% atomic Hydrogen into the amorphous lattice these dangling bonds can be passivated [11] and the material quality is better suited for use in solar cells. The second problem is that amorphous silicon solar cells exhibit light induced performance degradation via the Staebler-Wronski effect [12]. Although the exact mechanism of the Staebler - Wronski effect is still unclear [9] it appears that exposure to light increases the defect density which increases the number of recombination sites and limits the generated current. In real terms this means that the solar cell efficiency degrades over a period of UV exposure, therefore amorphous silicon cells are specified in stable efficiency i.e. efficiency of the cell after Staebler-Wronski degradation.

Despite these problems amorphous silicon has had a relatively high market penetration [9] of the TF-PV market. Commercially available a-Si modules offered by Kaneka and Oerlikon solar achieve efficiencies of ~10%. The commercial modules use many design tricks to achieve these efficiencies. The e-field in amorphous silicon is naturally quite low due to low minority carrier lifetimes [9] leading to charge separation. In order to get around this a p-i-n structure is used with a-Si as the intrinsic absorber layer and doped micro crystalline silicon (μc-Si) as the p and n materials. μc-Si consists of small crystal grains in an amorphous matrix and can be used as a solar material in its own

right, however it is difficult to grow at high rates and is therefore usually used in small quantities alongside amorphous silicon. The other method that commercial amorphous silicon cell manufacturers use to increase the efficiency is light trapping. The TCO is textured to scatter non absorbed light and thin layers of transparent conductive oxides (TCOs) are layered to trap light. This creates a much higher effective optical path and allows less material to be used having a dual benefit of lowering costs and increasing material stability as thinner layers are less prone to Staebler-Wronski degradation. A schematic of a commercial Kaneka cell can be seen in Figure 2.6.

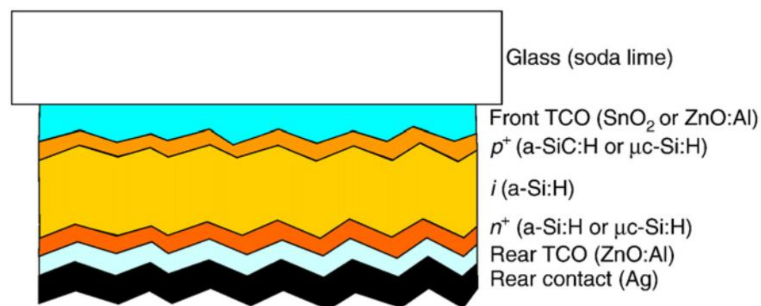


Figure 2.6: A schematic of a commercial a-Si solar cell. Note the roughened surface of the layers to increase light trapping [13].

Now that 10% efficient single junction a-Si cells are available [13] there is little room for improvement without changing the cell architecture [9]. To further increase the efficiency beyond the 10% level multi-junction cells are being investigated. These cells have two, three or more absorber layers with complimentary band gaps. By arranging the absorbers with the largest band gap at the top and decreasing band gaps below the cells effectively dividing the spectrum between themselves so more total light is utilised. One of the main benefits of tandem a-Si cells is that they don't cost much more in time or money than the equivalent single junction cell making them an attractive option for progress.

In amorphous silicon, multi-junctions can be achieved in two ways. Alloying of amorphous silicon with germanium allows the band gap to be tuned from 1.8-1.4eV [9]. By growing layers with progressively higher Ge content a multi-junction cell can be formed. This has allowed the manufacture of cells up to 10.4% efficient [14]. The second method is the incorporation of a layer of μc-Si below the a-Si layer. μc-Si has a band gap of around 1.1eV, much closer to crystalline silicon. However the many grain boundaries in μc-Si means there is a lot of internal scattering of light and a much longer effective path length which creates an effective absorption coefficient about an order of

magnitude higher than crystalline silicon. These amorphous/micro crystalline cells have been termed micromorph cells [9] and have achieved stabilised efficiencies of 12.3% for a tandem cell and 13.4% for a triple junction cell [13]. There are positives and negatives to these two approaches. The benefits of micromorph cells are thinner layers of a-Si which decreases the light induced degradation, higher quantum efficiency and fill factor (FF) and reduced materials costs as the GeH_4 precursor for a-SiGe:H is more expensive than the silane SiH_4 used in micromorph cells. The drawbacks of micromorph cells are thicker intrinsic layers of μc-Si compared to a-SiGe because μc-Si is an indirect bandgap, low deposition rate for μc-Si and slightly reduce Voc. After weighing up both options most of the commercial attention has been focused on the micromorph design with several large companies making these types of cells including Oerlikon solar and Kaneka, see Figure 2.7.

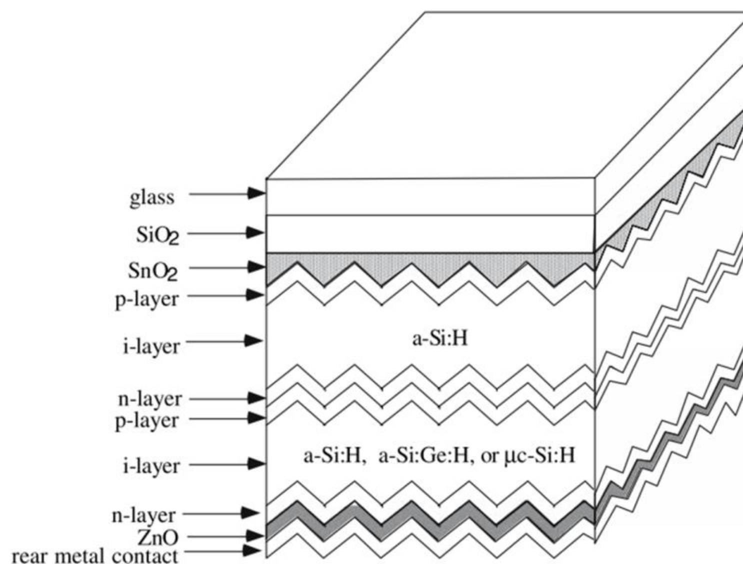


Figure 2.7: Schematic view of a tandem thin film silicon solar cell. The second layer can be either based on Ge compounds or μc-Si [8].

One of the main challenges in fabricating multi-junction cells is matching the amount of current generated in each absorber layer as the lowest current will limit the current of the other cells. In practice it is usually the a-Si that has the thinnest layer and therefore the lowest current so internal reflectors are employed to trap light in this layer to raise the current. This has been described in [15].

The standard process for laser scribing of thin-film silicon is well known. The P1 scribe is usually done with a near IR laser from the glass or film side, film side UV is also possible but generally not used in industry due to higher laser costs. The P2 and P3 scribes are both achieved from the glass side with green lasers. All lasers are Q-

Switched with pulse widths typically of 10's of ns, the most commonly used lasers are DPSS or fibre lasers.

A large array of work on laser scribing of thin film Silicon for the manufacture of solar cells has been published [16]–[18] which confirms that all the processes are usually completed with a Q-Switched DPSS laser operating in single transverse mode (TEM00) with a Gaussian output. The commonly used wavelengths are the first, second and third harmonics of neodymium doped gain media such as Nd:YAG or Nd:YVO4 at approximately 1064nm (IR), 532nm (green) and 355nm (UV).

Of the three processes P1, P2 and P3, the back contact patterning step P3 has been shown to be the most critical [16] with any unablated material or remaining debris potentially leading to shorts in the cells. As such the bulk of the work in the field of TF-Si scribing has been focused on this process step. The main issue with the back contact ablation step, in non-optimised processes, is the formation of flakes at the edges of the scribes [18]. The flakes of metal that are generated are a problem since it is possible that they can shunt between the TCO and the metal contact. The metal flakes can be seen in Figure 2.8.

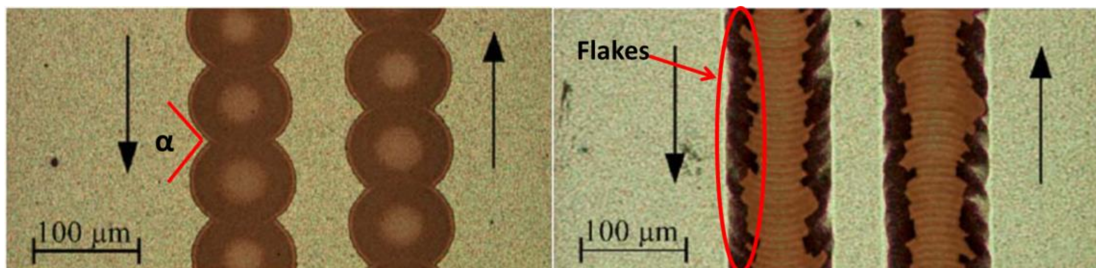


Figure 2.8: Optical images of laser ablation of silicon with a 532nm q-switched laser. Left image is a low overlap, flake free process and the right hand images shows a high overlap process with flakes of metal back contact, indicated [18].

It has been proposed that the flake formation process is dependent on the angle between successive laser pulses. For a Gaussian beam this angle is determined by the spot overlap which in turn is governed by the interplay between the PRF and the beam translation velocity across the sample. The criteria for flakeless ablation was determined to be that the angle between spots (α, see Figure 2.8) must be greater than 90° this is related to the beam speed (v), spot size (d) and pulse repetition frequency (f) in Equation 1 and corresponds to scribes with very low overlap [18].

(2.1) $$Sin\left(90-\frac{\alpha}{2}\right)=\frac{v}{df}$$

(2.2) $$\frac{1}{\sqrt{2}}\leq\frac{v}{df}<1$$

To test this theory Haas generated a square beam using a diffractive optical element (DOE), at 45° to the direction of travel as this always creates an angle between successive spots of 90° [16]. Using this spot geometry flakeless ablation has been observed over a broad range of shot overlaps, this result can be seen in Figure 2.9. This result seems to confirm the theory that the key parameter is the angle between shots.

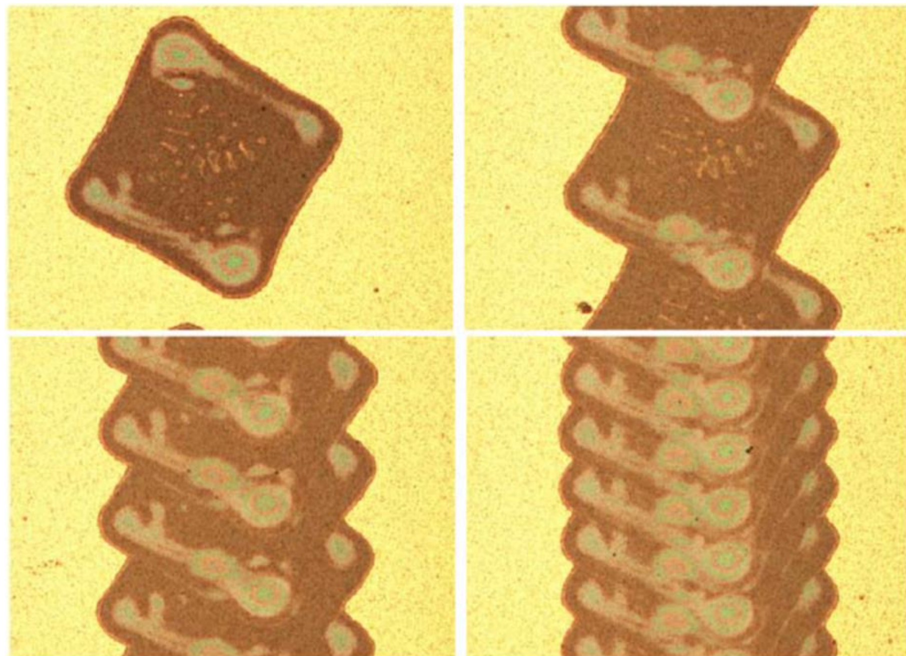


Figure 2.9: Optical images of laser ablation of silicon using a beam with a square, top hat intensity distribution. It can be seen that flake free ablation can be achieved for a wide variety of overlaps [16].

The effect of the back contact patterning process on the dark I/V characteristics has been investigated [16], [18]. A 1cm^2 cell is used and further scribes are added in parallel to the back contact scribe. After each of the scribes the dark I/V characteristics are measured, the scribe geometry and a typical plot can be seen in Figure 2.10.

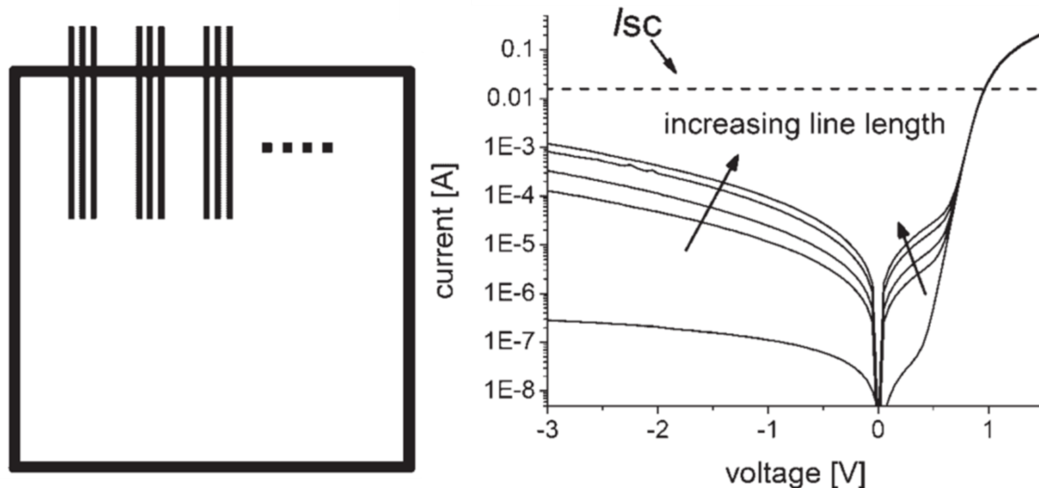


Figure 2.10: Left; A schematic of the structure used to test the effect of the scribes on the dark I/V characteristics. The bold line around the outside defines the 1x1cm2 cell area used for testing, the smaller parallel lines at the top are the scribes to be tested. Right; The effect of the scribes on the dark I/V curve of the cell. It can be seen that with increasing total line length the dark current increases [18].

As each scribe was added it was found that the dark saturation current I_0 increased. This is thought to be because the heat affected zone (HAZ) around the scribes locally affects the material either by increasing the defect density, recrystallization of the silicon or causing diffusion of dopands. The behaviour under reverse and forward bias can be fitted using SPICE to a modification of the one diode model of solar cells.

The one diode model is an equivalent electrical circuit to a solar cell and can be used to model the I/V behaviour of cells. It is made up of a light dependent current generator (I_{ph}), a diode (D) and two resistors to incorporate parasitic shunt and series resistances (R_{sh} and R_{sh}). Under reverse bias the addition of an element with an exponential I/V response (diode $D_{reverse}$) connected with a resistor ($R_{reverse}$) accounts for the observed behaviour. In the forward current regime a single diode connected in parallel recreates the observed characteristics. This modified circuit can be seen in Figure 2.11.

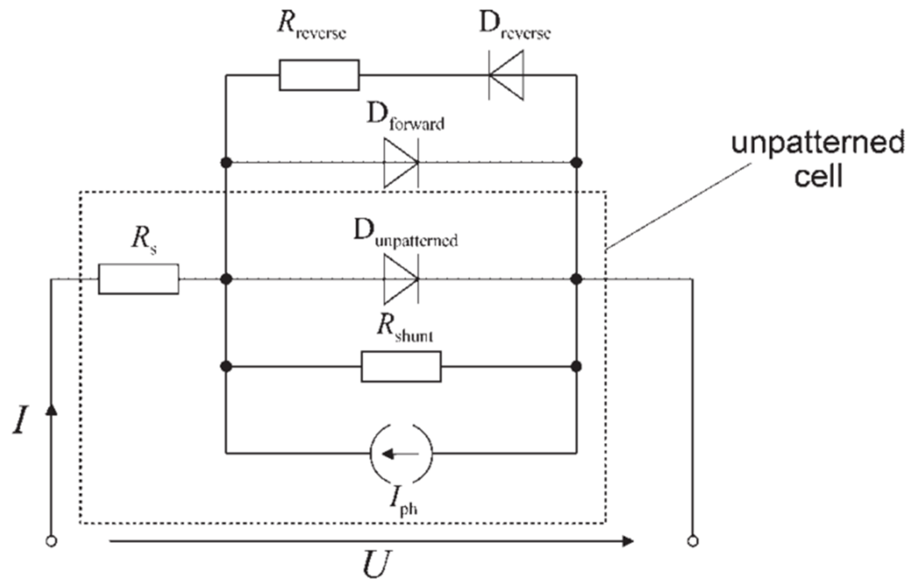


Figure 2.11: The equivalent circuit for a solar cell is the section within the dotted line. The extra scribe lines are modelled by the two diodes $D_{forward}$ and $D_{reverse}$ and the resistor $R_{reverse}$. The model achieved good agreement with the experimental results [18].

Using SPICE to simulate this circuit with $D_{forward/reverse}$ acting proportionally to line length and $R_{reverse}$ being inversely proportional a good agreement has been achieved with the experimental observations. The characteristics of a solar cell under illumination can be thought of as a superposition of the dark current and the photocurrent, thus the length of laser line also effects the illuminated I/V characteristics. Testing the illuminated cell characteristics, a small reduction in both I_{sc} and FF was observed. The reduction in I_{sc} can be explained by the reduction in active cell area and perhaps the short circuit current density J_{sc} would have been a better parameter to have been used in the comparison. The local increase in defect density around the scribe doesn't have any noticeable effect because of the short carrier diffusion length of this type of silicon. The decrease in FF however has been shown to be related to the increase in dark current.

Taking all the effects into account, the influence of the back contact scribing process has been shown to depend on the ratio of scribe length to cell area. Since cell area is cell width multiplied by scribe length, the effect of the laser scribe is only dependent on cell width. This means that when scaling up from mini-modules to full size panels the key parameter to optimise is cell width. In fact under Standard Test Conditions (STC) the effect of the back contact scribe is negligible for cell widths from 0.7-1.0cm as long as the process parameters are optimised. The methodology developed here can be used as a test to electrically qualify P3 scribes.

The two different approaches to scribing the TCO for the P1 process have been compared [17]. The standard process usually uses an IR laser from the glass or film side or UV from the film side [19]. In this work a UV laser incident from the glass side is used. This is thought to have benefits to the afore mentioned processes in that the absorption of TCO at UV is greater and thus more energy is deposited at the glass TCO interface resulting in a cleaner scribe. Samples consisting of two different TCOs (ZnO and SnO_2) are used ranging in substrate thickness from 1.1-3.2 mm, layer thickness 650-1200 nm and covering sheet resistance from 4-14 Ω/sq. It was found that all samples could be ablated without any visible damage to the glass substrates with very low intensities (6-13 μJ) and moderate beam speeds of around 0.3m/s. All scribes achieved good isolation, greater than 20 MΩ and looked clear of material. Although this result is very good in principal with pulse energies approximately 10 times lower for the UV process compared with the comparable IR process it is worth bearing in mind for moving into an industrial setting that the cost per Watt of a UV ns laser compared with an IR ns laser is typically more than 10 times larger resulting in a more expensive process. The process is also likely dependent on the type of glass used as some absorb more strongly than others in UV.

Replacing the green laser currently used for the glass side P2 and P3 processes with a near IR (NIR) laser of 1064nm, again incident through the glass has been investigated. The laser was tested with both a-Si and μc-Si cells and the previously described dark I/V test was used to compare the electrical impact of both scribes. In the case of a-Si the I/V characteristics were heavily affected by the IR laser scribes. The line was visibly of poor quality, the edges were ill defined and Silicon residue could be observed on the bottom of the scribe. The group theorise that the NIR laser results in a poor scribe for a-Si because the photon energy is less than the band gap and therefore the absorption coefficient is lower. This results in the energy being absorbed over a larger volume of material rather than at the TCO a-Si interface resulting in a less clean scribe. In the case of a single junction μc-Si cell the results are much better. The observed change in the dark current characteristics was comparable with the standard process and the corresponding degradation in the illuminated I/V curve was negligible. This is believed to be due to the smaller band gap of micro crystalline silicon compared to the amorphous material. This means the absorption of the NIR laser is much higher at 1064 nm and so the energy is deposited at the interface and the mechanism for ablation is the same as in the green case. Although it is disappointing that the NIR laser is

ineffective at scribing the amorphous silicon cell the result on the micro crystalline cell is promising. Perhaps in the future micromorph/multi junction cells can be manufactured in such a way as to allow ablation with the cheaper NIR laser.

The standard scribing process for a-Si has been extended to micromorph (a-Si/μc-Si:H) tandem cells [20]. Using a 532nm laser for the P2/P3 process has been investigated both through the glass and with the laser incident through the solar materials i.e. film side. The P1 process is completed with an NIR laser as usual. From the film side it was not possible to remove the entire micromorph layer in a single shot even at pulse energies of 1.5mJ, to get a properly scribed cell 7-9 passes were required. Unsurprisingly the cells resulting from these scribes were poor with FF < 50% and V_{oc} losses of the order of 300mV. Micrographs of these scribes show signs of remaining molten material at the edges which would shunt the cell and explain the poor V_{oc}. Using film side scribing the group were unable to produce a good cell, this result is disappointing as film side scribing would be highly preferable for the OSI process. The results through the glass look much more promising, the entire absorber layer can be removed in a single shot and fill factors greater than 70% were achieved which demonstrates the absence of shunts. There was some excess and unnecessary active area loss due to the removal of the back contact along the very edge of the scribe, probably resulting from a similar mechanism as the metal flake formation but analysis by the Laser Beam Induced Current (LBIC) technique didn't reveal any changes in current generation within the HAZ. There was also a change in the surface texture of the TCO. Under SEM it appears that at the centre of the laser pulse where the intensity is greatest the TCO has melted and re-solidified resulting in a smoother surface. None of the results gave any indication that this lowered the quality of the completed cell and in fact a smooth surface may lower the contact resistance of the deposited metal contact.

2.2.2 Laser scribing of Cadmium Telluride (CdTe)

CdTe is a natural choice for thin-film PV as it's band gap of 1.45eV is well suited to the solar spectrum, it is a direct semiconductor and so has high optical absorption coefficients, it has a strong tendency to grow in a stoichiometric way naturally becoming strongly p-type and it forms a p-n hetero-junction with a thin layer of CdS which grows strongly n-type [21]. All this makes it one of the easiest thin-film PV technologies to manufacture having been grown successfully by a large number of

methods including electro-deposition, sputtering and screen printing [22] with the current record cell efficiency held by close space sublimation, evaporation of a granular CdTe source in close proximity to a substrate, at 19.6% [13]. The quality of deposited films is a function of substrate temperature with 400°C minimum and 600°C optimum. After deposition the quality of the films can be greatly increased by treatment with a Chlorine containing compound, usually $CdCl_2$ [21]. For these reasons CdTe has the highest market share of any thin-film technology thanks mainly to American company First Solar who as of 2011 had a manufacturing capacity of 2.3GW per annum [23].

Cadmium Telluride's ease of manufacture also extends to laser processing. It is the easiest of the primary thin-film technologies to scribe and the process is well known [24]. A review of scribing polycrystalline thin films has been published by Compaan [19] . focussing on scribing of all the component parts of CdTe and CIGS solar cells including several different TCOs, both the semiconductors themselves and a handful of metal back contacts. All these materials were tested with 9 different lasers spanning UV-IR wavelengths and pulse durations from 10's of nanoseconds to 250ns. The beam was trialled both incident from the film and glass side as well as with a number of different spot shapes/energy distributions. The findings for CdTe were that it was the easiest of the two semiconductors to scribe, even at 1064nm where it should be transparent and that glass side scribing for CdTe has real advantages including lower threshold for removal, self-depth limiting and better scribe morphology than film side scribes [19]. Work published by Jingquan et al shows the standard laser manufacturing process with the P1 scribe done with 1064nm laser and the P2 and P3 with a 532nm laser [25]. This process is also used in industry [26], [27] and is so well established that there is little novel work going on into laser processing of CdTe solar cells. The only novel work available is about moving from glass substrates to thin (~100μm) flexible substrates of Polyimide or similar but even this transition hasn't required significant modification of the laser process [28].

2.2.3 Laser scribing of Copper Indium Gallium Selenide (CIGS)

CIGS is perhaps the most promising of all the second generation thin film technology. With cell efficiencies currently 19.8% and module efficiencies of 15.7% [13] CIGS has the potential to match or even outperform crystalline silicon in battle for the lowest cost per Watt. One of the drawbacks of CIGS compared to CdTe and a-Si is the complexity

of the absorber layer. CIGS is usually put down via co-evaporation [29] and many different combinations of Cu, In, Ga and Se can be found with different properties. Control of the material gradients over large areas proves to be a challenge [30].

As discussed previously CIGS is usually manufactured in a substrate configuration with the back contact (Molybdenum) deposited on the substrate. This creates a few problems for laser processing for monolithic interconnection. As discussed above glass side scribing usually creates the best results for ablation of thin-film solar cells as all the energy is deposited at the layer interface. Since Mo is opaque to all common laser wavelengths glass side scribing can only be used for the P1 scribe, subsequent P2 and P3 scribes are limited to film side processes. This difficulty has meant that the industry standard P2 and P3 processes are scribing with mechanical styli [30]. Although many modules have been produced with this method, the chipping associated with the mechanical process means that the dead zone between the interconnect has to be larger than the equivalent laser process. Mechanical scribes also suffer from slower scribe speeds and decreasing scribe performance over time due to tool wear, all of which are not problems for lasers [31]. This has meant that there has been extensive work on laser processing for P2 and P3 scribing of CIGS .

In the review of scribing of polycrystalline films CIGS is also tested [19]. It is noted by Compaan that CIGS is consistently more difficult to scribe than CdTe and that ‘considerable effort may be necessary to maintain clear scribe profiles’. This is partly because the glass side scribing which was so beneficial for CdTe can’t be used for CIGS. Despite this there was some success with laser scribing for CIGS. The P1 scribe of Molybdenum was successfully completed with both IR and green lasers and scribing of CIGS for P2 was achieved with relatively long pulse (250ns) IR lasers, however there were a couple of problems with this scribe. Firstly ridges appear at the sides of the scribes due to recoil pressure of the ejected plume on the molten material. Secondly, residue is often left in the scribe which may result in poor electrical contact between the Mo and the TCO. Mini modules were fabricated using all-laser CIGS scribing but the results were inconsistent. The need to ship samples cross country between each scribe or deposition step was cited as the likely problem. Since this review was published in 2000 and as of 2015 this author knows of no company using lasers for both P2 and P3 scribes [32] it could be argued that the inconsistencies in the data were related to the scribing process rather than sample transport. In fact it has been shown [33] that ns

laser ablation of CIGS heavily effects the electrical conversion efficiency of the structured solar cell.

The failure of the usual laser technology, ns Q-switched Nd:YAG lasers and their harmonics, in scribing CIGS has led to research in a number of alternative laser based solutions. As described in Chapter 1.1, novel interconnects, laser micro-welding has been investigated to replace the CIGS P2 scribe [1], [2], [34]. There is also a wide array of research into ultrafast lasers for scribing CIGS [32], [35], [36]. Scribing of CIGS solar cells with ns, ps and fs lasers has been compared by Kim et al [32]. It was found that for ns pulses thermal effects created many problems for P2 and P3 ablation including a large HAZ, interdiffusion of molten CIGS/Mo, cracks in Mo and CIGS and rims of material around the edge of the ablation region. Moving to shorter pulse lengths reduced these thermal effects considerably. Moving from ns to fs pulses improves visible scribe quality and the impact of laser processing on the cell efficiency, resulting with 6.6% efficient cells with fs ablation and only 0.6% with ns ablation [33]. The result with fs lasers is promising but fs lasers are expensive and complex and therefore only tend to be implemented when only fs pulses will do the job. Picosecond laser sources, although still more expensive than ns are more economical than fs. The result of scribing CIGS with ps lasers appears to fall between ns and fs in terms of electrical performance of the PV cell. It is likely that the final solution will be a trade-off between cost and performance and so ps lasers could be a good compromise.

Optimisation of ps laser scribing for CIGS for industry using a 2W, 1064nm High Q laser with 10ps pulse width has been completed [36]. Using this laser source for the P1 ablation of Mo from film and glass side showed much better scribe quality and lower ablation threshold compared to the longer pulse processes. The impressive results for the P1 scribing come from using cylindrical lenses to create an elliptical beam 32um x 350um. Using this beam the team were able to run the P1 process at speeds of up to 4m/s with no adverse results for the isolation of the layer. The group then moved on to the film side ablation for the P2 and P3 processes. Both were completed successfully at speeds of a few 100mm/s and look good from optical microscopy and profilometry. The contact resistance of the picosecond P2 was compared with the mechanical P2 process and it was found that the contact resistance was lower with ps laser ablation. All the results from this work look promising, however in order to be fully confident in the scribes it would be required to prepare full modules and compare their performance to the mechanically scribed counterparts. Questions still remain as to whether the

benefit of the extra speed for the P1 process is worth the extra cost of moving to picosecond lasers rather than the currently used nanosecond lasers. If the P2 and P3 processes are shown to be consistently good, the benefits of laser processing over mechanical scribing, smaller scribes, less dead zone, higher repeatability, higher yield etc. may well warrant the switch to the picosecond laser sources for these steps.

Further work into laser scribing of CIGS has come out of a collaboration between laser manufacturer Pyro Photonics and the National Renewable Energy Laboratory (NREL) in Colorado [31], [37], [38]. Pyro photonics have manufactured a laser with a controllable temporal pulse shape. The pulse can be tailored in 1ns steps to a total pulse duration of 250ns with limits placed on maximum pulse energy (600uJ), maximum average power (25W) and maximum peak power (25kW). Using this laser source it was found that short 2-5ns square pulses successfully scribes the CIGS for both the P2 and P3 processes on NREL samples. A diagram of the temporal pulse shape can be seen in Figure 2.12.

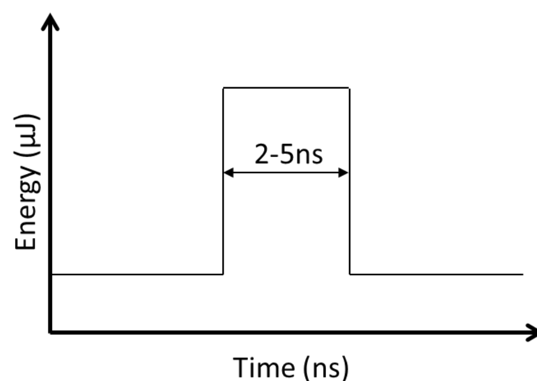


Figure 2.12: The temporal pulse shape used by Pyro Photonics and NREL to successfully scribe CIGS can be seen in the figure. The pulse had a fast rise and fall time and a duration of 2-5ns. The usual pulse shape for a DPSS laser would be Gaussian however the design of this laser allows the temporal pulse shape to be tailored with resolution of 1ns.

Inspection with optical microscopy, profilometry, SEM and EDX shows the scribes to be free of the unwanted melting of CIGS common in ns and to a lesser extent ps laser processing. The profilometry reveals that the edge of the scribe is very clean and the SEM shows clear fracture lines along the length of the scribe. EDX reveals that the material at the bottom of the trench consists of Mo as expected but also has a relatively high concentration of Selenium (Se) residue.

A mechanism was proposed to explain the CIGS scribe process in this pulse regime but not with other ns laser sources. From observations of the scribe walls it appears that the material was fractured along the edge, more closely analogous to the through the glass scribing than film side [37]. The theory is that the laser isn't absorbed by the CIGS and is heavily absorbed at the interface with the Mo, at this point the Se, having the lowest melting and vaporisation temperatures of all the constituents of CIGS is vaporised. This exerts a mechanical pressure on the rest of the stack which is enough to snap it off and eject it. A similar mechanism has been observed in picosecond and femtosecond laser removal [31]. For this mechanism to be applicable in this instance the CIGS has to be transparent to the 1064nm light (1.165eV) and with a band gap of approximately 1.2eV it has been calculated that roughly 80% of the light is delivered to the Mo interface [31]. This model has been extended to include other factors. As the light is incident on the CIGS most of it is transmitted to the interface but any energy absorbed or transferred via heat from the Mo to the CIGS increases the density of free electrons and thus the absorption. After about 5ns the CIGS is completely opaque and all absorption is in the bulk of the material which causes melting and leads to a failure of the brittle fracture mechanism. If the rise time, pulse duration and fall time of the pulse is sufficiently short and the energy delivered is sufficiently high then the laser energy vaporises the Se at the interface before the CIGS temperature is significantly raised becoming opaque and melting, the result is a brittle fracture process from the coating side.

Using the optimised scribes two all-laser interconnected mini-modules were manufactured by shipping samples back and forth between NREL and Pyro Photonics. Simultaneously two modules with mechanical scribes were manufactured, for reference, by shipping them between NREL and an undisclosed German company. A blank reference sample was also manufactured and accompanied the shipped samples, at the end of the trial the blank sample was finished using NRELs standard process. The initial results from the laser scribed modules were poor, with efficiencies of 5.31 and 4.08% respectively, the reason for this was believed to be that the antimony zinc oxide (AZO) TCO was too thin for the 6.5mm cell width and caused a large series resistance. A further 0.38μm coating of AZO was deposited on all modules and subsequent P3 scribes were added. It's worth noting that both sets of modules were edge isolated with Pyro photonics laser scribes. The laser modules and mechanically scribed modules were comparable, η = 7.24 and 8.3% for the laser modules and 7.48 and 6.63% for the mechanical modules. This process shows significant promise and could easily be a

candidate to replace mechanical scribing, although further work is required to produce all laser scribed modules with efficiencies closer to the record efficiency of 15.7%.

2.2.4 Summary of laser processing for TF-PV

OSI requires a combination of laser and inkjet processes therefore the initial focus was on developing the required laser scribes. Two other novel interconnects have been presented. The first, laser micro-welding is applicable only to CIGS and has had some success although there are still some problems. The second, point wise contacts for series interconnection is broadly applicable to all thin-film cells and has been demonstrated for a-Si. This interconnection scheme could in principle complement OSI well.

In the previous section the current knowledge on laser scribing for TF-PV has been investigated. Firstly the general specifications for a laser interconnect have been established, namely;

- The laser process must be robust and free of defects
- The scribes must take up minimum space (minimise the dead zone)
- All scribes must have good edge quality so as to not to introduce shunts
- The laser process must not limit the takt time of the process.

After this, each material has been looked at individually for its particular challenges. CdTe appears to be the easiest and best known process, a-Si requires some work on optimisation of scribes for flake free ablation and could potentially be improved using different laser sources and CIGS has the most work to do as the industry standard is scribing with mechanical styli. There is a lot of ongoing work into scribing with ultrafast and novel lasers to replace the current mechanical process. Implementation of OSI on CIGS will require significant development of laser processes as mechanical scribes are unlikely to be suitable.

2.3 Fundamentals of inkjet deposition

In order to complete OSI, insulating and conductive materials must be placed with high accuracy into laser scribes of ~50μm width and ~3μm depth. For a one step process a

‘direct write’ deposition method is required as opposed to subtractive methods like lithography which take many steps. There are many forms of printing which are able to place both insulating and conductive patterns with relative accuracy such as screen printing, gravure, flexographic and inkjet (IJ) printing [39]. The first three of these methods suffer from limited flexibility, requiring the manufacture of screens or rollers with the printed pattern etched into them. They would also be difficult to integrate into a traditional laser machining system which has a process head delivering the laser which must move with respect to the substrate. The laser pattern is produced by translating the head across the substrate many times, either by moving the head relative to the substrate or the substrate relative to the head. In contrast inkjet printing fits well with a traditional laser system. An inkjet printer is made up of computer controlled stages and print heads capable of placing a very small volume of ink (~10pL) with great accuracy [39]. There are two types of IJ either continuous or drop-on-demand (DoD). DoD printing produces smaller drop sizes with higher accuracy and is therefore preferred for printed electronics applications [40]. In DoD printing the pattern is defined by a digital file which is easily changed.

Modern DoD inkjet technology is broadly split into two types based on the actuation mechanism used to eject the ink droplet; thermal and piezo. Thermal Inkjet (TIJ) uses miniature heaters to locally vaporise a small amount of ink causing a bubble and a corresponding positive pressure, this in turn ejects the ink droplet. TIJ has many benefits: it is easily miniaturised and inexpensive which has led to it being common place in home inkjet printers [41]. In an industrial setting however piezo inkjet (PIJ) dominates for two main reasons: firstly in TIJ the ink must have a relatively high vapour pressure, limiting the variety of suitable inks and secondly with TIJ it is difficult to accurately vary some drop parameters such as velocity and volume [42].

PIJ uses the reverse piezoelectric effect to convert an electrical signal into a mechanical deformation of the inkjet nozzle, the positive pressure from the channel deformation ejects the droplet. In 1984 Bogy and Talke [43] presented an analyses of the effect of inkjet cavity length on optimum drop ejection parameters and from this produced a theoretical treatment of drop ejection based on linear acoustic wave theory. The voltage applied to piezo electric material within the print nozzle causes an expansion of the channel and generates an internal negative pressure wave. The negative pressure wave splits in half, one wave propagates toward the ink supply end and the other towards the

nozzles opening. From acoustic wave theory the acoustic impedance of a channel is given by Equation 2.3 [41]:

$$Z = \frac{\rho c}{A} \quad (2.3)$$

where ρ is the density of the ink, c is the speed of sound in the ink and A is the channel cross-sectional area. The reflection co-efficient of the acoustic wave at domain boundaries such as moving from the channel of the nozzle to either the supply or nozzle ends is given by Equation 2.4 [41]. Where the acoustic wave is moving from domain 1, acoustic impedance Z_1 (i.e. the channel) to domain 2, acoustic impedance Z_2 (either the supply or nozzle ends):

$$R = \frac{Z_2 - Z_1}{Z_1 + Z_2} \quad (2.4)$$

If as in this case the compliance doesn't change the reflection coefficient simplifies to Equation 5 [41] where domain 1 has area A_1 (channel cross sectional area) and domain 2 has area A_2 (either the nozzle or supply ends):

$$R = \frac{A_1 - A_2}{A_1 + A_2} \quad (2.5)$$

The wave incident at the supply end of the nozzle has $R \approx -1$ since the diameter of the supply section, open end in Figure 2.13, is much larger than the channel diameter ($A_2 >> A_1$); in contrast the wave incident at the nozzle, closed end in Figure 2.13, has $R \approx 1$ since the nozzle diameter is much smaller than the channel diameters ($A_1 >> A_2$). Therefore the wave reflecting off the closed nozzle keeps its phase whereas the wave reflecting off the open supply end has its phase reversed. The open time of the piezo actuated nozzle is optimum when, as the two reflected waves meet back in the centre, the channel relaxes back to its resting position producing a positive wave. All three waves interact, the negative pressure wave is annihilated and the positive pressure wave is reinforced, resulting in a large amplitude positive wave moving towards the nozzle end which forces droplet ejection. Figure 2.13 [44] shows a schematic of a typical print nozzle and the movements of the various acoustic waves.

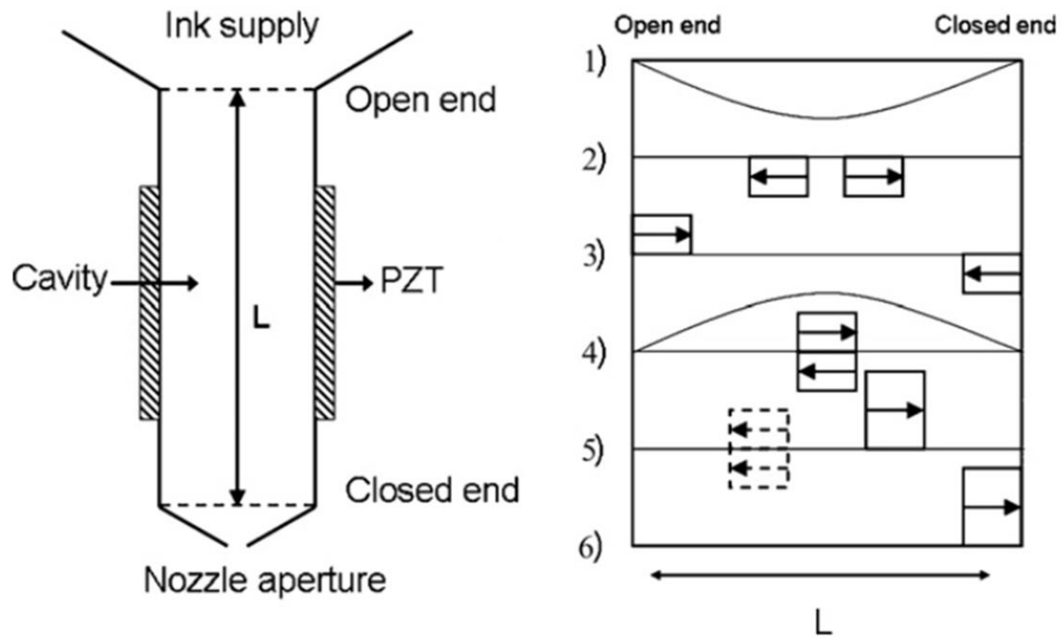


Figure 2.13: Mechanics of drop ejection based on acoustic wave-propagation. a) A schematic of the print nozzle with the piezo elements surrounding the nozzle cavity. b) The propagation of acoustic waves at different times during actuation. 1) shows the deformation of the channel wall caused by the piezo, 2) shows the direction of propagation of the acoustic waves, 3) shows the reflection of the waves off the nozzle and supply ends, 4) shows the two waves meeting in the centre of the channel as the piezo returns to its original shape 5) and 6) show the propagation of the reinforced wave towards the nozzle end which causes droplet ejection [44].

This idealised model is useful to understand the mechanics of drop ejection but in some cases the assumptions do not hold [45]. It was found that the optimum pulse duration, equal to cavity length divided by the speed of sound in the fluid, was actually proportional to *~2.5L* where *L* is half the cavity length compared with *4L* predicted using the simplified model above, if the nozzle end is also modelled as an open end then the predicted value for optimum pulse duration is exactly *2L.* So the actual optimum value is measured to be somewhere between the calculated values for an open ended nozzle and a closed ended nozzle, tending more towards the open ended. An assumption made in the simple model is that the cavity has uniform cylindrical cross-section. A tapered cross-section near the orifice, as found in most inkjet nozzles, leads to an effective cavity length which is shorter than the actual cavity length, thus reducing the optimum pulse duration. A second identified breakdown in the model is the assumption of a 100% phase change in the acoustic wave from the nozzle end which is inaccurate because the open orifice diameter does impact the degree of reflection. It was found that by plotting nozzle diameter against optimum pulse duration a trend became apparent; as the orifice diameter is reduced the optimum pulse duration

increases [45]. Extrapolating this data back to zero opening produces a value close to the ideal value of *4L* calculated using the assumption of a closed nozzle end.

2.3.1 'Drop watching'

Before describing in detail the effect of driving waveform on the drop formation process it is important to understand how the effects are measured. The most common analytical technique applied to inkjet is stroboscopic imaging, also known as 'drop watching'. A camera and light source are setup either side of the print nozzle with the light synchronised to the drop ejection pulse via a delay generator. Typical drop ejection frequencies are a few kHz and each ejection triggers the light source however, since typical camera frame rates are around 25fps, each camera frame contains the average of many drop ejections. Inkjet drop ejection is an inherently repeatable process and therefore this method results in the capture of most of the information however random or probabilistic events will either not be viewable or result in blurring of the image. By controlling the delay between the trigger pulse and illumination the drop can be viewed at any point in its flight from the first movements of the meniscus until the drop travels beyond the field of view of the camera. Quantitative measurement of drop velocity is possible by measuring the change in position of a droplet for a given change in delay. Mass and volume can also be measured by jetting a known number of droplets, usually $>10^5$ into a microbalance [45]. In order to see greater detail this technique can be modified by using a fast camera with the shutter also synchronised to the trigger pulse and a high intensity light source. In this mode it is possible to capture an image of a single drop. A comparison of single images and stroboscopic imaging can be seen in Figure 2.14, below [46].

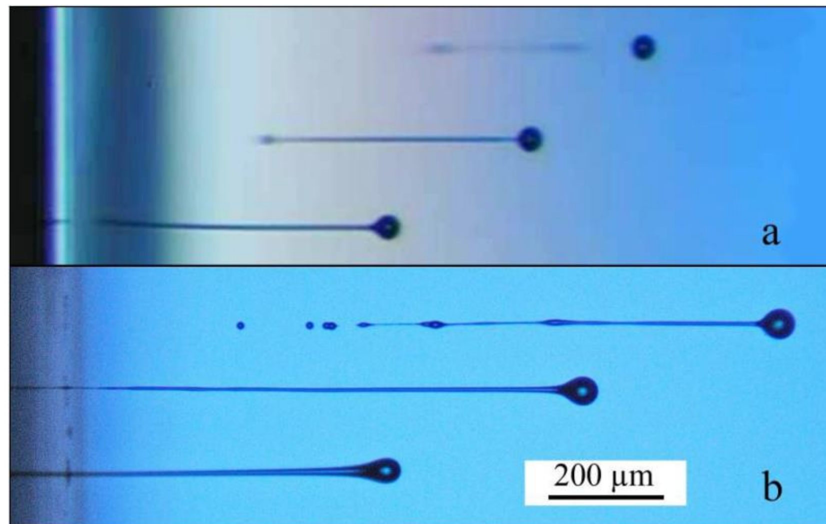


Figure 2.14: a) Stroboscopic imaging is the average of many drops per frame, probabilistic changes in drop formation cause blurring. b) A single flash image of a drop in flight using a fast camera and high intensity light source results in a much clearer image [54].

2.3.2 Effect of voltage waveform on print characteristics

The magnitude, velocity and direction of the piezo actuators movement within the nozzle are dependent on the applied voltage. Optimisation of jetting characteristics requires control of the piezo movement; this is done by altering the voltage waveform applied to the piezo element. By changing this voltage waveform it is possible to control many aspects of drop formation, including velocity, volume and shape, all of which are important for a good quality print. In traditional graphics applications it is desirable to modulate the drop volume on the fly in order to produce different tones of colour by having different volumes of ink per pixel, this on the fly drop modulation also allows printing detailed parts of an image at higher resolutions and blocks of colour at lower resolution thus increasing efficiency and lowering print cost [41]. This technology would also be useful for the deposition of functional materials where tailoring exact volumes of material to specific locations on structures can be critical. This drop volume modulation must be achieved while keeping the velocity stable to keep drop placement errors consistent and can be achieved using correct waveform control. Ideally, in inkjet printing, the drop is spherical when it hits the surface giving a repeatable circular shape on the substrate and again this can be controlled through optimisation of the waveform.

In the most basic case the waveform is a simple trapezoid with a characteristic rise, hold and fall time at a single voltage level [46], see Figure 2.15. Work published by printer manufacturer Océ gives an extremely detailed overview of the mechanisms of drop ejection and formation [41]. Through a combination of finite element modelling using the software package Ansys and experimentation the droplet formation process from the point of droplet ejection is described.

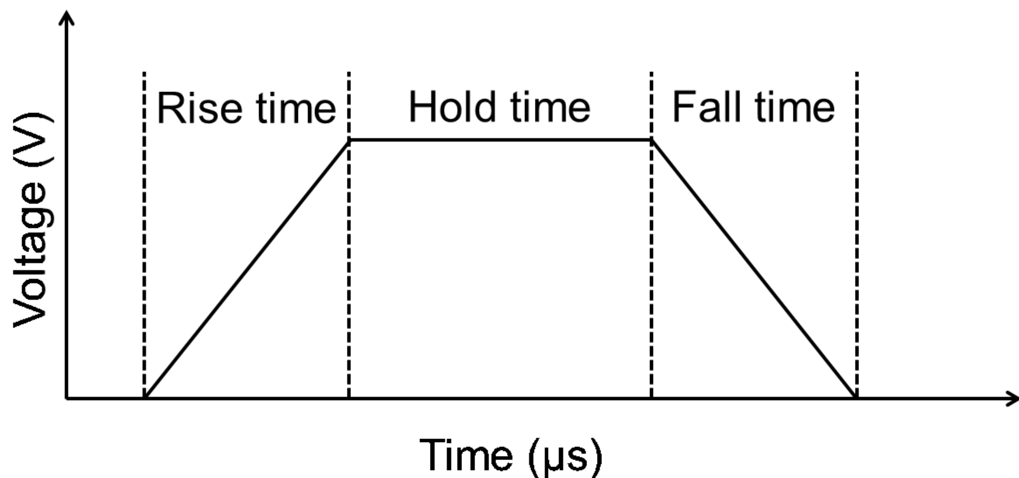


Figure 2.15: The basic shape of the voltage waveform applied to a PIJ print nozzle. Full optimisation of drop formation is achieved by controlling rise, hold and fall times as well as the magnitude of the applied voltage.

As the channel expands at the start of the actuation process the negative pressure causes both the meniscus to retract and an influx of ink from the supply channel. These phenomena lead to the two names given to this type of PIJ actuation, either 'fill before fire' as the channel is filled from the supply end or 'pull-push' which describes the motion of the meniscus at the nozzle end. After the reflection and reinforcement of the positive acoustic wave the meniscus moves outwards with at its maximum velocity, around 20m/s. After the drop is ejected it remains attached to a ligand or tail which slows the drops velocity. The tail length and break-off point are mainly dependent on ink properties such as, surface tension, density and viscosity. When the drop detaches from the meniscus, if the print parameters are optimum the tail will snap back into the main drop, slowing the speed further until it reaches a final velocity around 5-7m/s [41]. Measurements of the drop speed as a function of distance from the nozzle can be seen in Figure 2.16.

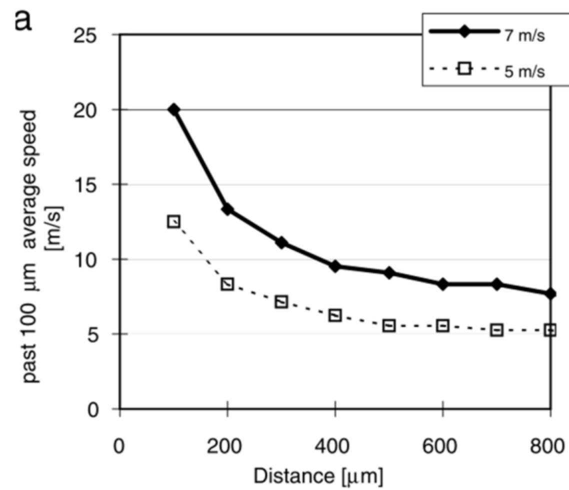


Figure 2.16: Average inkjet drop velocity for the previous 100μm motion measured as a function of drop distance from the nozzle. It can be seen that the drop velocity is not constant during formation but settles toward a final value as the tail joins the main drop. Both plots are using the same fluid and head however the final drop velocity has been modulated by controlling the voltage applied to the piezos to give final drop velocities of 7 m/s (solid line) and 5 m/s (dashed line) [41].

It is critical for print quality to avoid formation of secondary, satellite drops. There are 4 mechanisms of satellite formation; mist of droplets, Rayleigh breakup, fast satellites and slow satellites [41]. All satellite formation mechanisms are related to the drop's tail. A mist of drops is caused by outside noise either mechanical vibrations, thermal, airflow or pressure fluctuations and results in many very fine drops that form randomly, making it impossible to see using stroboscopic imaging. Rayleigh breakup happens because a cylinder of liquid is a fundamentally unstable state [46], as the tail becomes longer small perturbations grow and cause it to collapse into a more energetically favourable form; a number of small drops rather than a long cylinder of ink. Rayleigh breakup is partly random but has a characteristic breakup length so an average of many Rayleigh breakup satellites can be seen using stroboscopic imaging (although they will appear blurred). The final two satellite formation methods are very repeatable and therefore the easiest to image. A fast satellite is formed when the drop has sufficient acceleration that surface tension can no longer hold the droplet together. Finally, slow satellites occur when secondary acoustic peaks are generated within the nozzle. The arrival of the second peak causes a small section of the tail to have lower diameter than the rest. The resultant area of high capillary pressure results in the tail being pinched off at this point [41]. An example of slow satellite formation can be seen in Figure 2.17.

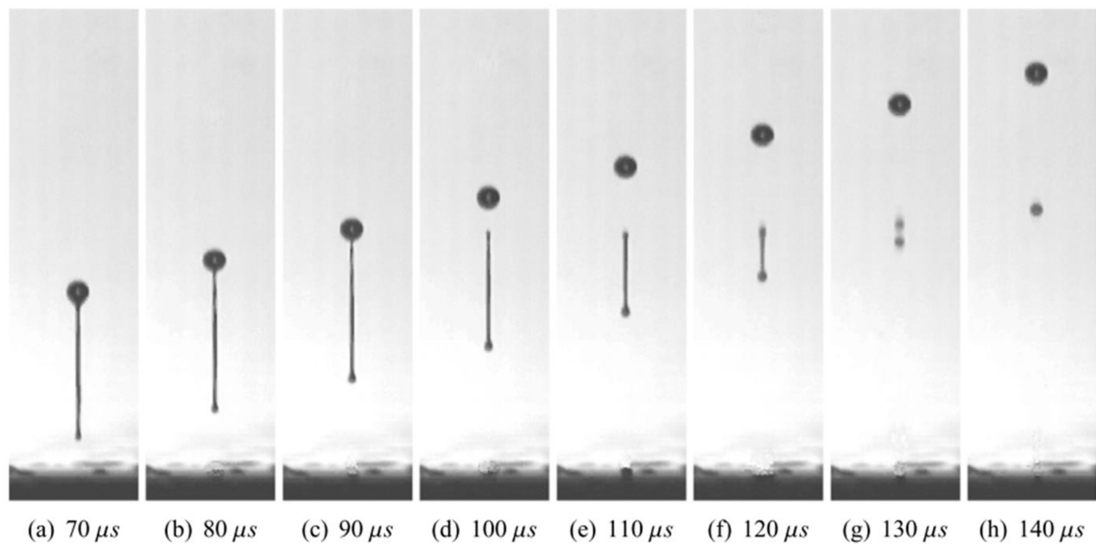


Figure 2.17: Slow satellite formation viewed using a stroboscopic imaging technique. The main drop has a velocity of 7m/s whereas the tail has a velocity of 5m/s, this discrepancy causes the tail to break off (100μs) and form a satellite (140μs) [41].

Drop volume modulation can be achieved through a number of different mechanisms, a standard nozzle with a cavity length of 5mm produces a 10pl nominal drop volume as standard and can be modulated between 7 and 65pl [41]. The simplest way to increase drop size is by increasing the waveform voltage however this is undesirable for a number of reasons. Firstly, increased voltage increases the drop velocity as well as the volume meaning the use of increased voltages in an on-the-fly modulation scheme will cause changes in drop placement for different volumes. Secondly, it is possible to increase the formation of fast satellites by the associated increase in voltage. Figure 2.18 [44] shows the changes in both velocity and drop volume caused by increasing the voltage applied to the piezo actuators within the printhead.

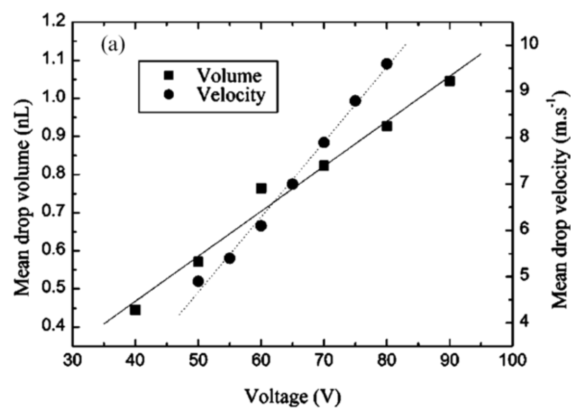


Figure 2.18: Changes in drop volume and velocity with voltage. It is undesirable to change the drop velocity on the fly in active volume modulation schemes since it also changes drop placement accuracy [44].

In order to avoid drop placement issues it is better to increase drop volume by increasing the hold time, this allows more ink to transfer towards the front of the nozzle. However, the detuning of the hold time from the optimum value leads to less reinforcement of the positive pressure wave and therefore a higher voltage is required to achieve the same velocity. This can be seen in Figure 2.19 [41]. In the example of the nozzle with nominal 10pl drop volume this method allows tuning of the volume from 10-16pl.

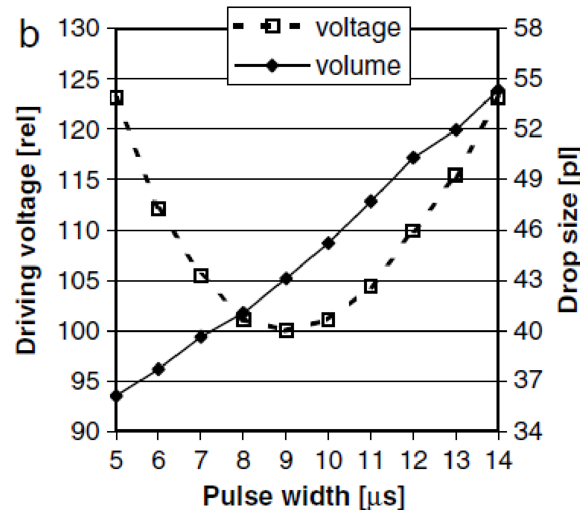


Figure 2.19: Drop size changes linearly with hold time, also called pulse width, however the voltage required to obtain a given drop velocity reaches a minimum at the optimum hold time value. This value corresponds to the time taken for the piezo generated acoustic waves to propagate to the end of the channel and back to the centre [44].

The next technique for extending the drop voltage tuning range is the application of a pre-pulse of around 10% of the nominal driving amplitude. This increases the amount of ink toward the front of the nozzle increasing the tuning range to 10-26pl. The opposite mechanism can also be applied, by selecting a post pulse of around 50% nominal voltage either with the same sign at the half period of acoustic wave oscillation or the opposite sign at the full period of oscillation to hold back some of the ink from the main drop allowing the volume to be tuned from 7-26pl. The final mechanism is an extension to the idea of a pre-pulse where a number of pulses are triggered together to eject a burst of 2-4 drops which agglomerate in flight. This allows high volumes to be achieved but the long duration of the pulse burst places limits on the maximum achievable ejection frequency. Using this scheme the nominal 10pl volume nozzle is able to achieve 7-36pl at a frequency of 40kHz, 7-50pl at 30kHz and 7-65pl at 20kHz. An example of a three drop burst can be seen in Figure 2.20, below.

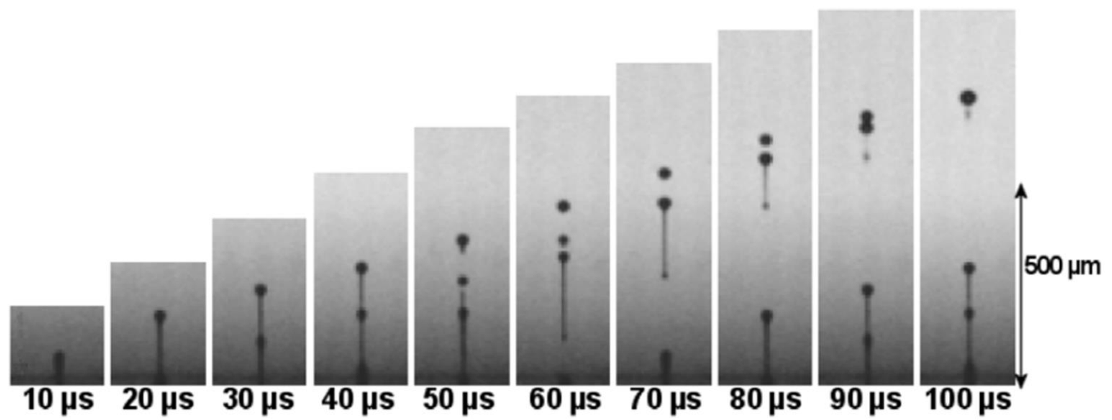


Figure 2.20: Stroboscopic imaging of a three drop burst, the drops agglomerate in flight to form a single drop of high volume before impacting the substrate. The next drop to be ejected can be seen after 70µs [41].

2.3.3 Jetable fluids

Moving from graphics applications to the deposition of functional materials poses a challenge for ink formulation. Graphics ink formulations are concerned primarily with printability and aesthetics resulting in a large formulation space. In contrast functional materials, particularly conductors, often require a high percentage of solids which increases the ink viscosity. In order to formulate suitable inks for inkjet applications and appreciate the limits of ink formulation, it is useful to understand which ink properties affect the ability to jet a fluid. It is possible to characterise inkjetable liquids using dimensionless groupings of physical constants, common place in fluid mechanics; Reynold (*Re*), Weber (*We*) and Ohnesorge (*Oh*) numbers, defined below, where ρ is density, η is viscosity, γ is surface tension, v is velocity and a is a characteristic length in this case given by the print nozzle orifice diameter [47].

(6) $$Re = \frac{v\rho a}{\eta}$$

(7) $$We = \frac{v^2\rho a}{\gamma}$$

(8) $$Oh = \frac{\sqrt{We}}{Re} = \frac{\eta}{\sqrt{\gamma\rho a}} = \frac{1}{Z}$$

The number *Z* can be defined as the inverse of *Oh* and it has suggested that any liquid with Z>2 would be stable while being inkjet printed. This has been investigated

extensively, particularly related to ceramics [1],[4],[8],[9]. Using numerical modelling [45] an adjustment to this range to *1<Z<10* is proposed for stable inkjet printing. It is explained that at low *Z* values viscosity dissipates the induced acoustic wave and prevents drop ejection, at high *Z* the tail of the drop is unstable and easily breaks up into satellites. A further limit on an inkjetable fluid is the requirement to overcome the fluid/air surface tension at the nozzle. This leads to a minimum drop velocity for drop ejection to occur which places a lower limit of 4 on *We* as anything less has insufficient energy for drop formation, see Figure 2.21. This is expressed in Equation 9 where d_n is the orifice diameter.

(9)
$$We = v_{min}\left(\frac{\rho d_n}{\gamma}\right)^{\frac{1}{2}} > 4$$

The final requirement is related to the onset of splashing when the drop hits the substrate, this places a requirement on the fluid that $We^{1/2}Re^{1/4} > f(R)$ where *f(R)* is a function of surface roughness and a typical value of *f(R)* for smooth flat surfaces, R_a<500 nm, is 50. Combining all of these fluid parameter requirements into a single chart with axis of *Re* and *We* the chart in Figure 2.21 is obtained [42].

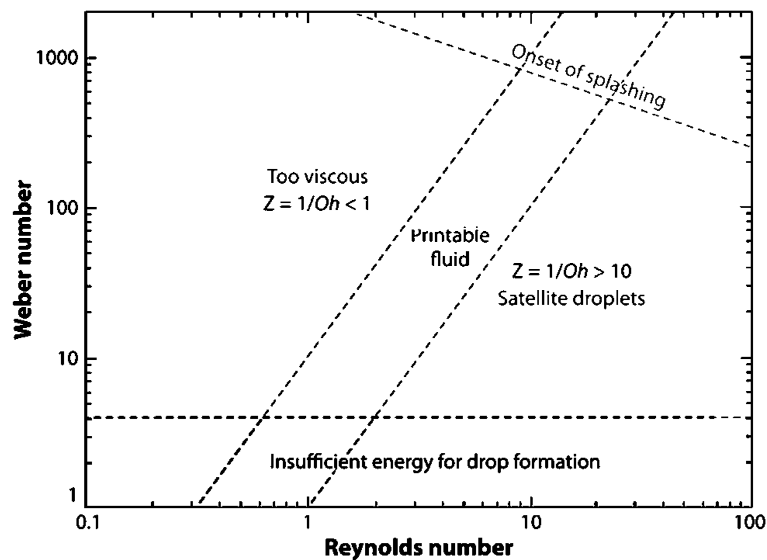


Figure 2.21: The range of printable fluids expressed in terms of Weber and Reynolds number [42].

The above parameter space has been explored for a range of fluids with large percentages of suspended particles [45] and appears to hold up well. Testing a range of fluids of 1<Z<14, it was found that the ejected drop volume, normalised to the channel displacement, was governed by *Z*. This relationship can be seen in Figure 2.22, below.

However, work published in 2009 disagrees with the position of the lower Z limit [50], suggesting that the range should be 4<*Z*<14. It was found that at Z<4 the time between droplet ejection and formation of a single droplet increases, requiring an increase in printer stand-off and an associated increase in drop placement error.

A key relationship first proposed in 1984 [47] has been experimentally verified [58,53]. For a given print head geometry, the drop volume when normalised to actuator displacement is dependent only on the fluid properties, namely the dimensionless grouping Z. Figure 2.22 shows the results of two independent sets of experimental work along with the original prediction. The relationship has been termed a 'master curve' relating drop volume to fluid properties for a given actuator displacement [50]. For OSI this result is of interest since it is likely that inks which fulfil particular criteria, such as conductivity, are likely to have similar Z numbers. It may therefore be the case that there are limits on the range of obtainable drop volumes for conductive inks based on the printhead geometry.

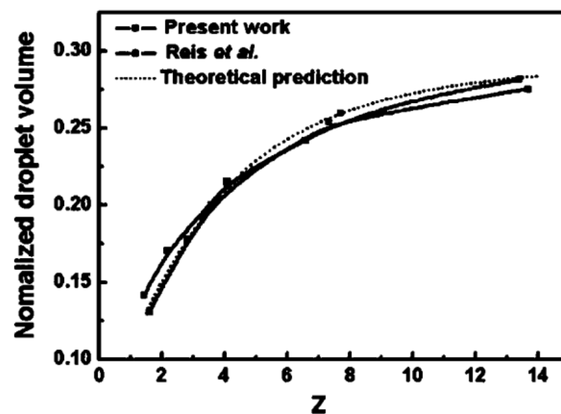


Figure 2.22: The 'master curve' relating ink fluid properties, in terms of the dimensionless constant Z, to droplet volume for a given actuator displacement [50].

2.3.4 Drop/surface interactions

There are three phases of a droplet interaction with a solid surface before equilibrium is reached [51]. Firstly, there is the impact where the drop meets the surface, secondly, there is a rapid expansion of the droplet outwards along the surface and this also includes a rapid fluid flow outwards creating bulges at the contact line, finally there is a period of damped oscillation governed by capillary forces before equilibrium is reached. The dynamics of this process are seen in Figure 2.23 [42], below.

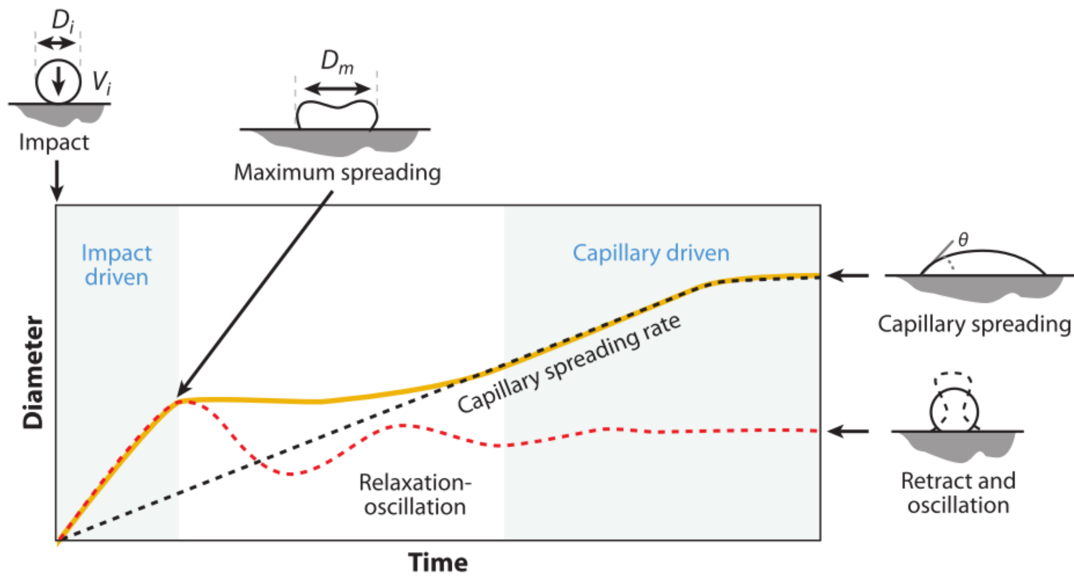


Figure 2.23: The dynamics of inkjet/surface interaction. The impact occurs at t=0, the first period is an impact driven rapid spread. The second period is one of damped oscillation. Finally the drop reaches its equilibrium size determined by contact angle. The red line shows drop evolution for a liquid with high contact angle, the yellow line one with lower contact angle [42].

The drop/surface impact can be classified into one of four regimes depending on the values of the Ohnesorge and Weber numbers [52]. With respect to the Weber number, the interaction is either Impact or Capillarity driven, in terms of the Ohnesorge number the liquid is either highly viscous or almost inviscid [42]. Overlaying the criteria for an inkjetable fluid, Figure 2.21, results in all inkjet surface interactions appearing in the same regime, that of an impact driven interaction with an almost inviscid liquid, Figure 2.24, below. Therefore all inkjet impacts are dominated by the inertia of the drop and there is little resistance to the initial impact driven spreading.

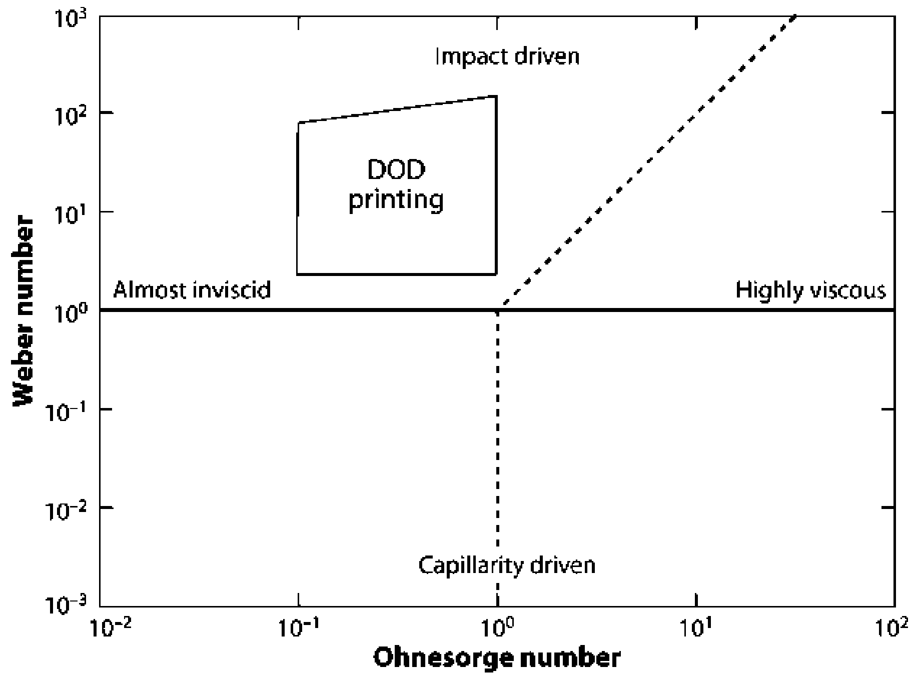


Figure 2.24: Regions of different drop surface interactions, separated according to the Weber and Ohnesorge numbers of the, diagram modified from [52]. The diagram is plit into quadrants, the top shows impact driven drop/surface interactions while the bottom is capillary driven. The left side is an inviscid fluid while the right is highly viscous. The previously described requirements on inkjetable fluids are overlaid, yellow trapezoid, it can be seen that all inkjet liquids appear in the same quadrant that of an impact driven interaction with an almost inviscid fluid [42].

Once the impact energy has been dissipated, capillary forces completely take over and, assuming there is no contact line pinning, dominate the final size of the ink drop on the surface. The final footprint is therefore related to the initial drop diameter, or volume, and the equilibrium contact angle of the drop with the surface according to the relationship in Equation 10, where θ_{eqm} is the equilibrium contact angle, d_0 is the drop diameter in flight and d_{eqm} is the equilibrium drop diameter on the substrate, see Equation 10 [42].

$$d_{eqm} = d_0 \sqrt[3]{\frac{8}{tan\frac{\theta_{eqm}}{2}\left(3+tan^2\left(\frac{\theta_{eqm}}{2}\right)\right)}} \quad (10)$$

This relationship only holds true if gravity can be ignored, i.e. the surface tension of the liquid dominates. The Bond number (Bo) is a measure of the importance of surface tension over gravity, the formula for Bo can be seen in Equation 11. Typically for a system where the effect of gravity is negligible $Bo<1$, inkjetable liquids typically have densities similar to water, around 1000 kg/m^3, surface tensions around 0.1 J/m^2 and drop diameters <100μm resulting in $Bo \ll 1$ [42].

(11) $$Bo = \frac{\rho g a^2}{\gamma}$$

The parameter 'contact angle' has already been used in Equation 10 but it is important to understand what the contact angle is and how it is measured. Once a drop reaches equilibrium, for a given drop volume, the drop diameter on the surface is controlled by the interaction of three forces; solid-vapour surface tension (γ_{sv}), also known as surface energy, solid-liquid surface tension (γ_{sl}) and the liquid-vapour (γ_{lv}) surface tension. After the drop comes in contact with the surface it expands reducing the contact area of the solid-vapour interface, an energetically favourable process, while increasing the contact area of the liquid-vapour interface, an energetically unfavourable process. During this time the solid-liquid contact area also changes which depending on the specific surface tensions, can be energetically favourable or unfavourable. The drop reaches equilibrium when these three forces balance; this is described by Young's equation, where θ_Y is Young's contact angle. See Equation 12 and Figure 2.25, which shows the resolved forces [53].

(12) $$\gamma_{lv} Cos(\theta_Y) = \gamma_{sv} - \gamma_{sl}$$

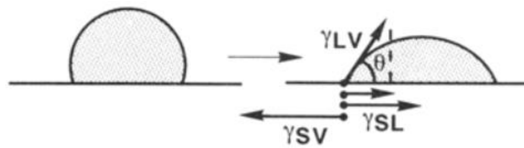


Figure 2.25: The resolved forces applied to a liquid drop on a solid surface, the contact angle θ is determined by the magnitude of the solid-vapour, solid-liquid and liquid vapour surface tensions [53].

Contact angle is often thought of as an easy to measure parameter requiring little skill or knowledge [53] however this view has been disputed [54]. Contact angle can be measured either from the static drop, advancing drop or receding drop. Advancing drop measurements are made while liquid is being added to the drop, receding while liquid is being subtracted and, static where the drop volume is constant. In an ideal surface all three angles would be the same however most combinations of drop and surface exhibit hysteresis between the advancing and receding angles due to contact line pining, in this case the static contact angle is often somewhere between the two values [54].

Young's equation is only valid in an ideal case, one with no hysteresis between advancing and receding contact angles. There are also some implicit assumptions; the

surface is smooth and chemically homogeneous, the liquid is pure as mixtures and surfactants can introduce hysteresis due to preferential adsorption and, the liquid and solid surface tensions are constant i.e. they do not undergo chemical reaction. Although very few surface/liquid interactions show zero hysteresis it has been shown that the advancing contact angle is a good approximation for Young's contact angle even when the surface is chemically heterogeneous [54].

Once a suitable surface and liquid have been chosen there is further difficulty in making the measurements. It has been shown that the conventional method of measuring the contact angle, a goniometer, is not accurate enough. An alternative is image processing using an algorithm such as the automated Axisymmetric Drop Shape Analysis – Profile (ADSA-P) [54], this finds the optimum profile that fits to a drop's image and uses that to calculate the contact angle. Figure 2.26, left, shows multiple measurements for two different liquids using a goniometer, from such plots it has been argued that contact angle is effected by specific molecular forces rather than being a simple relationship. Figure 2.26, right, shows measurements taken for many different liquids using the ADSA-P technique all lying on a 'master curve' linking contact angle with liquid surface tension.

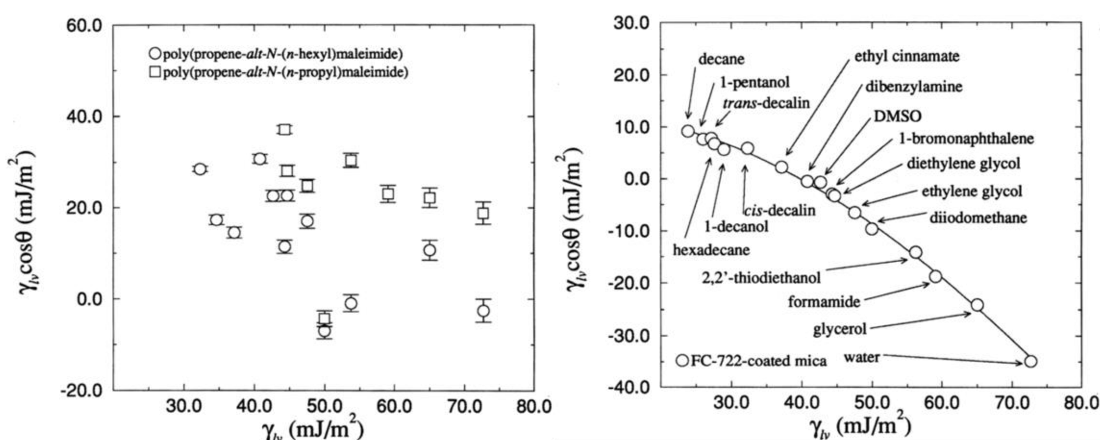


Figure 2.26: Contact angle measurements using a goniometer (left) and the ADSA-P image processing technique (right). The goniometer measurements show no relationship whereas the more accurate image processing technique reveals the underlying relationship between liquid surface tension and contact angle [54].

Based on goniometer measurements of contact angle it has been asserted that contact angle must be a function of more than just surface tensions and that the type of molecular bonding in the liquid has an effect. It is argued that this is the case since interpretation of the contact angle measurements do not come to agreement on the value

of solid-vapour surface tension which should be constant. However, once the more accurate ADSA-P technique is used for the measurement then a pattern emerges with no indication that polar liquids exhibit any different behaviour to non-polar liquids above and beyond the liquid-vapour surface energy [54].

To recap, the conclusions reached about contact angle measurement are threefold; contact angle measurement is non-trivial, contact angle measurement does not contain information on intermolecular forces and, contact angle hysteresis does not stop the measurement from providing useful information but it requires careful experimentation and analysis.

In the case of a rough or porous surface it has been proposed that the variations away from Young's contact angle are due to an increase in the effective contact area [55], [56] thus the effective surface energy. This effect is expected to magnify the original surface properties so that any hydrophobic surface, one with a water contact angle >90°, becomes more hydrophobic and any hydrophilic surface, water contact angle <90°, is expected to become more hydrophilic. The exact description of contact angle on a rough surface is the subject of much investigation [57], [58] and beyond the scope of this review. This change of apparent contact angle with surface roughness has the potential to be a useful tool to obtain features smaller than would naturally occur on a smooth surface.

While developing OSI it is likely that the comparison of two contact angles will be sufficient, however calculations of the free surface energy of the substrate are possible [59]. The most commonly used approach is the measurement of the contact angle of the substrate for at least two liquids of known surface tension. It is then possible to plot the cosine of Young's contact angle against the surface tension. The so called critical surface tension can be determined by fitting a line to the data which is the surface tension where $cos(\theta_Y) = 1$, the contact angle is zero, at this point the surface tension of the liquid is equal to the surface energy of the solid [59]. Proposed extensions to this basic approach include geometric and harmonic mean approach and acid-base theory [60] which again are outside of the scope of this review.

2.3.5 Drop coalescence

Deposition of functional materials is different from graphics printing in that it is usually concerned with depositing continuous lines and tracks formed from the coalescence of many drops. In contrast for graphics printing discreet pixels are desirable. Drops deposited on a substrate will coalesce into a printed track up to a certain maximum drop spacing which is dependent on contact angle, when this drop spacing is exceeded, discreet drops are formed. Assuming that the impact of gravity is negligible i.e. a low Bond number as shown earlier, there is conservation of drop volume from in-flight to forming tracks and there is no evaporation, then the width of a printed line can be calculated by Equation 13 [42]. Where d_0 is drop diameter in flight, p is drop spacing and θ^* is the advancing contact angle.

$$w = \sqrt{\frac{2\pi {d_0}^3}{3p\left(\frac{\theta^*}{\sin^2\theta^*} - \frac{\cos\theta^*}{\sin\theta^*}\right)}} \quad (13)$$

Minimum line width occurs at the maximum allowable drop spacing for coalescence and then increases with reduced spacing. A lower limit on drop spacing is given by the onset of bulge instability. Bulge instability occurs due to flow along the length of a printed track, when the rate of fluid delivery is high i.e. a high nozzle frequency, then flow along the track occurs faster than spreading due to capillary forces [61]. This leads to bulges of material in some locations connected by ridges of liquid at the minimum allowable width for coalescence. The onset of bulge instability is at lower ink arrival volumes for an ink and substrate pair exhibiting a higher contact angle. Printing at the same drop spacing but at lower translation velocities reduces the flow rate due to drop arrival and therefore removes bulge instability. Therefore in order to print a continuous track with constant width there is a maximum combination of drop frequency and print velocity, this may become an issue if trying to form thick continuous layers with well controlled lateral resolution in a production environment where process speed is important. Figure 2.27 [61] shows examples of lines of silver nanoparticle ink printed on polyimide (PI), in both images the translation velocity is constant but the drop delivery frequency is decreased by ~1/3 between image a) and b).

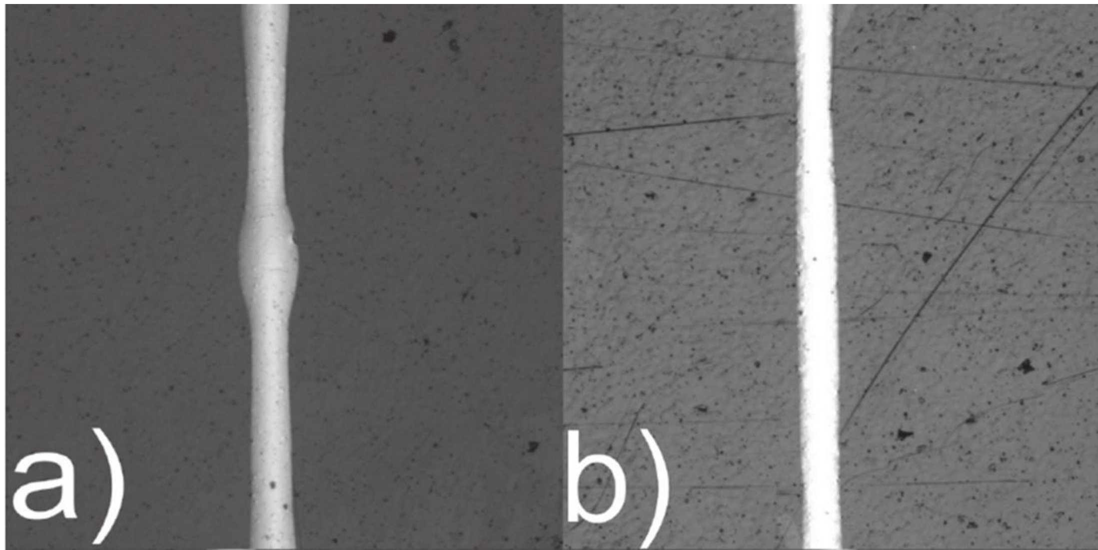


Figure 2.27: Printed tracks of a silver nanoparticle ink on a PI substrate a) a line exhibiting bulge instability at a drop frequency of 75Hz b) a continuous line without bulges at 50Hz, in both images the translation velocity is fixed at 3mm/s [61].

2.4 Functional inks formulation and processing

2.4.1 Formulation of inks

Broadly speaking inks are made up of a functional material in a carrier fluid [62]. The functional material can be suspended or dissolved in water in which case it is known as an aqueous ink or an organic solvent, for example Toluene. In graphics inks the functional material is the dye or pigment used for its colour whereas in printed electronics it is either a conductor, insulator or semiconductor. In most cases other additives are required to modify the inks properties so that it becomes jetable or remains stable [62]. The functional materials used in inkjet printing can be categorised into one of two types depending on the solubility of the active material. Inks are said to be dye based if the active material is soluble in the solvent carrier or pigment based if the functional material is insoluble and so forms a suspension.

Conductive inks are mostly of the pigment variety containing a dispersion of metal nanoparticles, most commonly silver [63]. A similar approach has been shown with semiconductors, such as tin doped indium oxide (ITO) [64]. Insulators are usually dye based inks consisting of a mixture of monomers and oligomers with a small percentage of photoinitiators, UV light catalyses them into polymers such as acrylic [65]. There are however examples of insulating pigment inks based on ceramics [66] and

conductive dye inks using metal salts [67] but both of these are less common. The starting point for OSI is the use of a polymer graphics ink as the insulator and a nano-particle suspension as the conductor. Since graphics inks are well developed they are not discussed in detail here.

2.4.2 Formulation of conductive nano-particle based inkjet inks

A common theme in printed electronics is the desire for a high conductivity track to interconnect parts of a circuit [68] or act as electrodes for TFTs or OPV [64]. To achieve high conductivities metals are the obvious choice, with Silver, Copper and Gold being the most conductive. The cost of raw materials is also an important consideration, Gold is prohibitively expensive, copper is the cheapest and silver is about an order of magnitude more expensive than copper. However the other consideration when choosing which metal to formulate into an ink is ease of handling. Copper nano particles readily oxidise in air making it more difficult to form a stable copper conductive ink [69]. Therefore most conductive inkjet inks in literature are silver based. However as ink formulations are maturing, copper (Cu) as well as nickel (Ni) inks are becoming available [70].

Ideally, an inkjet ink should be highly stable with a shelf life of 1 year or more however this poses a challenge for metal nanoparticle suspensions. Particles naturally want to agglomerate and sediment out of dispersion, this puts an upper limit on particle loading of around 60% [71]. To increase stability additives are used which adsorb at the particles surface preventing close contact [63]. Once printed these stabilising agents must be removed therefore a post deposition treatment, usually heating, is applied after the conductor is printed to produce a conductive network. This serves three purposes; firstly it evaporates any remaining solvents, secondly it removes the stabilising agents which prevent close packing and thirdly, if the temperature is high enough it sinters the particles. This post deposition treatment will be discussed further in the following section.

As well as stabilising agents in pigment inks it may also be necessary to control viscosity and surface tension to both make the fluid jetable and to achieve the desired feature size on the substrate. Viscosity must be in a suitable range, typically 8-15cps for piezo actuated DoD printheads [41], this can be modified by addition of a small

percentage of long chain glycols or high molecular weight polymers [71]. Surface tension can be controlled either by adjusting solvent composition or by altering the ratio of one solvent to the other in a two solvent system. The addition of surfactants can also allow the control of surface tension. Other possible ink additives include humectants to reduce evaporation in the inkjet nozzle so as not to block it and polymeric binders used to increase substrate adhesion. Unfortunately the inclusion of surfactants and polymers can introduce foaming, which prevents reliable jetting so the addition of defoaming agents can also be required.

2.4.3 Post deposition processing of conductive inks

Post deposition a sintering step is required to form continuous conductive tracks from the discreet particles found in nanoparticle inks. Sintering involves the welding of small particles at temperatures below the bulk material melting temperature and comprises three steps. The first step involves necking of the individual particles in which the individual particles become connected by 'necks' of material decreasing the surface area of metal and resulting in porous, connected grains rather than individual particles. During the second stage the necks continue to grow forming larger grains and the original particles become indistinguishable. Finally, full densification occurs, with a corresponding shrinkage of material and a reduction in size and frequency of pores. Figure 2.28 shows the stages of sintering [72]. The final form is close to bulk metal although some remaining porosity and some organic additives, such as adhesion promoters, may remain. For this reason the resistivity of a printed track is never as low as that of the bulk metal. The nanoparticles typically used in inkjet inks exhibit different properties to the bulk material due to the high surface area to volume ratio, a useful result of this divergence from bulk properties is the depression of the melting temperature and therefore sintering temperature [73]. Although sintering is a complex process which has many dependent variables including time, atmosphere and pressure, temperature plays the biggest part in the process. Sintering temperature is typically 60-90% of the melting temperature therefore the smaller particles with the lower melting temperature sinter more easily [62].

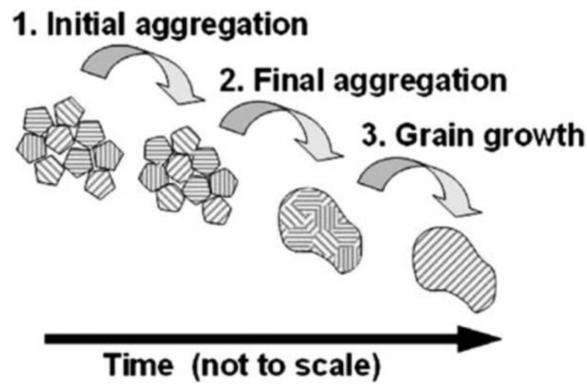


Figure 2.28: The sintering process in nanoparticle inks. Initially capping agents are removed and the particle aggregate, stage 1, upon further heating there is a net flow of material as necking occurs, stage 2. The final stage is grain growth, stage 3 [72].

Resistivity is an intrinsic material property which quantifies a given materials opposition to the flow of electrical current. The resistivity of a printed track can be calculated by the measurement of its resistance using an Ohm meter combined with dimensional information of its length, width and thickness using Equation 14 where R is the measured resistance, l is track length, w is track width and t is layer thickness. Resistivity is a material property and is the reciprocal of conductivity. In the literature both resistivity and conductivity are used, for consistency here all resistivity values are quoted as a multiple of the resistivity of the bulk metal in question, silver is 1.69×10^{-8} Ω.m.

$$\rho = \frac{RA}{l} = Rt\frac{w}{l} \quad (14)$$

The value sheet resistance R_s is a parameter often used when talking about resistance of thin films and has the unit of Ohms/square. It is found by dividing the resistivity of the material by its thickness, see Equation 15. Sheet resistance can be measured directly using a four point probe.

$$R_s = \frac{\rho}{t} \quad (15)$$

2.4.4 Thermal processing of conductive inks

Sintering is a temperature driven process therefore the most commonly used method of sintering conductive tracks is the direct application of heat in an oven [74], [75]. Heating a nanoparticle ink boils off the solvent carrier as well as the majority of ink additives allowing close packing of the metal nanoparticles, typically volatile solvents

and organic stabilisers are used so this is a relatively low temperature process. On application of further heat sintering is initiated. The applicability of inkjet printed conductors relies on the ability to form conductive tracks at temperatures compatible with desired substrates. The goal for most printed electronics is high volume, large area flexible electronics and therefore polymer substrates such as PET, PEN and PI are desired. This leads to the trade-off between resistivity and the melting, softening or glass transition temperature of the substrate. The glass transition temperature is the lowest limiting temperature and is the point where polymer foils undergo irreversible deformation. The glass transition temperatures of PET and PEN are 100-105°C and 125-130°C respectively [76].

Using both 21 nm and 47 nm silver nanoparticles it has been shown that very low resistivities can be achieved at relatively low temperatures [75]. 21 nm nanoparticles reach resistivities of around 19x bulk silver at 140°C whereas the 47 nm particles require 160°C for the same resistivity, it is thought that this onset of conductivity is caused by the onset of necking between the particles. At 200°C both particle sizes have achieved a resistivity of around 2x bulk silver with the difference being predominantly caused by the removal of residual organic components, both solvents and the additive poly vinyl pyrrolidone (PVP). Further treating of these two inks up to 400°C leads to resistivities of 1.7 μΩcm, i.e. 1.1x bulk, for the 21nm particle ink and 1.9μΩcm, i.e. 1.2x bulk, for the 47nm ink. A corresponding densification and grain growth is shown. A plot of temperature against resistivity for the two particle sizes can be seen in Figure 2.29, left [75]. However temperature is not the only important variable, the exposure time to the temperature is also critical [77]. Figure 2.29, right shows a plot of time against temperature at different temperatures for a similar silver nanoparticle ink.

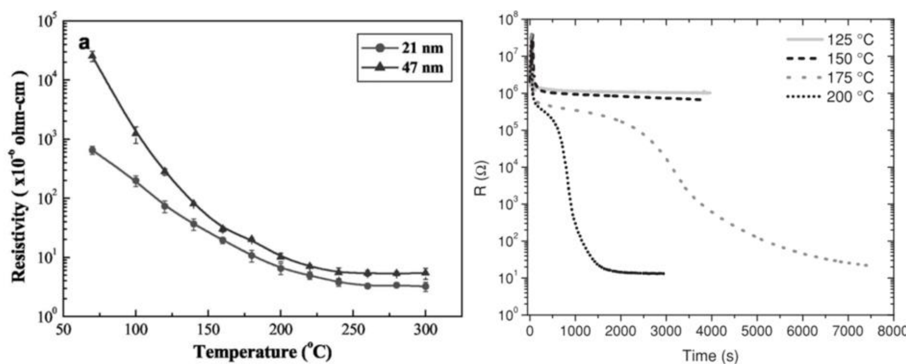


Figure 2.29: Left; the temperature against resistivity relationship for the 47nm and 21nm particle containing inks [66]. Right; the time against resistivity relationship for a similar silver nanoparticle ink at different fixed temperatures [68].

Temperatures of 200°C are too high for many flexible plastic substrates yet resistivities close to bulk are required for many applications. An oven cure requiring anything from 15-60 minutes is also disadvantageous for a production process, requiring batches of product to be stored and loaded into ovens or a very long conveyer oven system. A faster, inline process would be advantageous. There has been much work into alternatives to oven sintering utilising photonic [76], [78], [79], electrical [80], microwave [81]–[83], plasma [84], [85] and chemical methods [86], [87] which are discussed in detail below. Most of these methods have in common the conversion of one form of energy into heating of the metal track in order to begin the sintering process, the notable exception being chemical methods. Benefits of these other methods include the localisation of the heat generation to the metal track, thus sparing sensitive substrates and the ability to perform the sintering more quickly and/or inline with the deposition.

2.4.5 Photonic Sintering

Photonic sintering encompasses both the use of flash lamps, or Intense Pulsed Light (IPL) sintering, and lasers [76], [88], [89]. For flash lamp or IPL sintering a Xenon flash lamp is commonly used where the majority of the emission is in the visible region of the spectrum (if UV filters are used). The principle advantage for printed electronics is that the substrates are typically non-absorbing in the visible whereas the inks as-printed are dark and highly absorbing thus temperature increases are localised to the metal structures. In OSI this isn't the case however the ink is generally printed onto metallic back contacts which are highly reflective and should therefore have similar characteristics. The exception to this is CIGS which has the transparent contact on the top of a photovoltaic absorber which, therefore will be highly absorbing in the visible. This means the IPL sintering is probably not suitable for CIGS. Laser photonic sintering is directional and therefore may be acceptable although it would still present a risk of damage to the cells in the process. The low thermal conductivity of most polymers means that when using a high temperature ink the polymer temperature will only rise significantly at the point which is directly in contact with the track, a side effect of which maybe increased adhesion to the substrate. Again in OSI this isn't the case and the thermally conductive metal back contact could potentially heat up significantly. This potential issue hasn't to date been fully investigated in literature.

It has been shown that an arc plasma fired Xenon flash lamp is able to sinter 5nm copper nano particles [88]. The copper ink was deposited using a micro-pippette and subsequently wet the surface of three different low temperature substrates, polyimide, polyethylene and polypropylene. The Xenon lamp was capable of an energy density of between 20 and 50 J/cm^2 in a 2-10ms pulse duration. The lamp has an electrical to light conversion efficiency of 50% in the range 200-1100nm. Some of the substrates are degraded by exposure to UV therefore lower wavelength light, below 540nm, was filtered out decreasing the optical intensity to 70% of its initial value. Using this intense pulsed light source the achievable copper resistivity was around 3x that of the bulk metal. This result is much lower than the resistivity achieved using a vacuum oven at 325°C for 1 hour which was three times higher. It has been shown through consideration of material properties that the temperature rise is predominantly confined to the copper in which the rise was predicted to be 297°C whereas in the polymer substrate it was only 57°C, furthermore the temperature rise in the polymer is expected to be confined to the area immediately below the copper track and may aid with adhesion. For the sintering of copper this method is particularly beneficial when compared to thermal processes as copper readily oxidises in atmosphere and therefore requires the oven to be in vacuum or a reducing atmosphere. It was shown using X-Ray Diffraction (XRD) that the pulsed light sintering avoids any oxidation even in ambient conditions. One negative of this investigation into pulsed light sintering was the requirement to dry off the majority of solvent before application of the pulsed light, although the sintering step occurred in around 2ms the drying step required 10 minutes at 80°C. It is also not clear that this ink can be made suitable for inkjet printing since in this instance it was deposited with a micro pipette, although other copper nanoparticle inkjet inks are available.

IPL has also been shown to work with silver based nanoparticle inks [76]. A commercially available 20% loaded silver ink was printed before being placed into the elliptical reflector of a 1000W Xenon flash lamp. The lamp created bursts of 32 pulses with a pulse length of 3-8ms, dependent on intensity. A control sample was sintered using a standard convection oven at 130°C for 2 minutes, it took 25s for the printed features to become conductive and a further 10s for the conductivity to increase a few orders of magnitude. After this point the conductivity slowly increased until 2 minutes at which point it levelled out at around 14x bulk resistivity. In contrast the photonic cured sample dropped to 6.3x bulk resistivity in 1s. In this instance a further benefit of

the IPL sintered tracks were narrower features since the ink had less time to spread to equilibrium however the morphology of the final track was less flat. Both the oven sintered and photonic sintered tracks exhibited significant porosity which explains the relatively high resistivities. Although not stated explicitly in this work it is possible that the limit on resistivity of the IPL sintered track is due to the conversion of the ink to a metallic phase with high reflectivity in the visible making it impossible to continue to efficiently supply energy to the printed line. This work postulates that the mechanism behind IPL sintering is photo-thermal and goes on to measure the temperature achieved in the printed tracks. After a single pulse the temperature is quickly raised to around 140°C, a single burst increases the temperature to over 200°C and a number of bursts interspersed with cooling periods further increases the temperature to over 250°C, Figure 2.30. It is therefore likely that the photo-thermal sintering mechanism is correct.

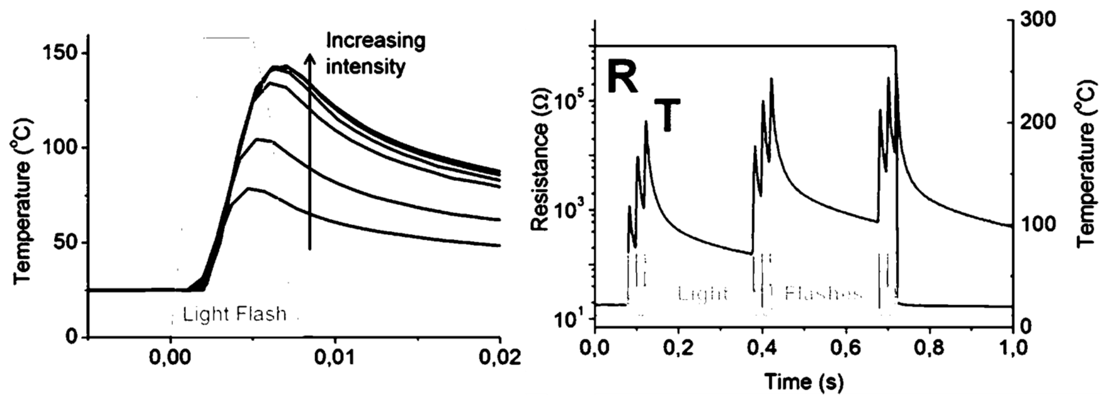


Figure 2.30: The measured temperature profile of silver nanoparticle inks exposed to IPL pulses over time. The temperature reached by the metal ink is similar to sintering temperatures of these types of inks lending credence to the theory that the sintering mechanism is photo-thermal [67].

Laser sintering of metal inks is thought to rely on the same photo-thermal mechanism as IPL but in the case of laser sintering the light is highly localised to the printed track. Use of lasers also offers the ability to improve the resolution of inkjet printed tracks by selectively curing regions and washing off excess inks. The drawbacks to laser sintering are that the curing time increases with pattern complexity since the laser must pass over the entire structure, to some extent this can be mitigated by utilising parallel processing. Continuous wave Argon ion lasers have been successfully used at wavelengths of both 488 and 514nm to cure a gold nanoparticle ink [90]. The ink contained 30% by weight 2-5nm gold nanoparticles carried in Toluene. Laser translation speeds of 2mm/s were used with low laser powers of 50 and 250mW with a 1/e2 beam diameter of 17µm. Using these parameters resistivities of 6x bulk gold,

2.4×10^{-8} Ω.m, were achieved. However, it is worth noting that translation speeds of 2mm/s are not compatible with manufacture of electronics devices, particularly where the entire pattern needs to be covered with a 17μm beam. Work has been done to compare a Continuous Wave (CW) laser with a pulsed laser [91] for laser sintering of metal nanoparticle inks. The ink was a commercially available, 20% silver loaded solution of 30-50nm nanoparticles suspended in ethylene glycol. A near-IR, 940nm, CW diode laser was compared with a pulsed 515nm fibre laser, although the pulse duration was omitted. The cure parameters were optimised in terms of laser spot diameter, translation velocity, laser power and, in the case of the pulsed laser, pulse repetition frequency and shot overlap. Once optimised the resistivities were compared for a given ink volume, for both print volumes the CW laser performed best achieving less than 2.5x bulk for the lower volume film, the pulsed laser achieved around 3x bulk and the oven cured, 220°C for 60 minutes, control sample 3.1x bulk. This work improves on the translation velocity of the previous one by running at up to 100mm/s with good results. Drawing conclusions from the comparison of the CW and pulsed laser is difficult however since they operate at very different wavelengths where different absorption mechanisms may come into play. It might be expected that the CW NIR laser would be better suited to the thermal process of sintering nanoparticles than the visible pulsed laser even if both were CW, however, for a conclusive answer it would be necessary to repeat these experiments using lasers of similar wavelengths.

2.4.6 Electrical sintering

Electrical sintering of conductive tracks has been demonstrated with good results [80]. A commercially available suspension of silver nanoparticles, 34.5% by weight, was printed onto photo paper using a Dimatix Materials Printer (DMP). A dog bone pattern was printed, with two contact pads separated by a narrow line of varying length. A resistor was placed in line with the conductive track to limit the maximum current and therefore stop sample destruction. A constant voltage (U_{dc}), of 50V was applied and the power dissipated in the printed track caused localised heating. The sintering took place extremely rapidly due to the positive feedback in the power dissipated by the printed track, with the bulk of it occurring in the first 2μs. The lowest achieved resistivity was around 1.7x bulk which compared well with a thermal sinter, on a different substrate, using the same ink which achieved around 3x bulk resistivity. The final track

conductivity was determined by the maximum current which can be well controlled through appropriate choice of resistor and voltage level. As an example a decrease from a track resistance of 150kΩ down to 4.3Ω was achieved using a 330Ω resistor and a 50V power supply giving a maximum current of 150mA. Although a powerful technique, there are a few potential drawbacks. Firstly, in OSI the printed tracks are in series with the solar cell and printed on a conductive substrate and it is unclear whether this type of sintering would damage the cell or if it is possible to obtain sufficiently high currents in the printed track. Secondly, the conductivity that the track needs to be at the start of the process is not clearly defined. Finally, it is unclear how easy it would be to make contact to printed tracks in a production manufacturing process. Some inks with different additives/solvents may not allow close packing of the particles before sintering and this could potentially be a limiting factor to the generality of its application.

2.4.7 Plasma Sintering

The use of plasma jets for sintering of silver nanoparticle inks has been investigated in 2009 by Reinhold et.al [84] and 2012 by Wünscher et.al [85]. Plasma is the fourth state of matter after solid, liquid and gas and is made up of ionised gas. In manufacturing, plasma is often used for surface modification, particularly as a technique to increase the surface energy of a solid in order to promote wetting and adhesion [92]. In these applications a plasma jet is formed by directing a pressurised gas, usually either air, oxygen or argon, between two electrodes with a high frequency RF voltage across them in order to ignite the plasma [85]. The first investigation was into the effect of low pressure argon plasma [84] on sintering of nanoparticle inks, subsequently atmospheric argon plasma sintering has also been investigated [85].

The low pressure plasma device consists of an oven like chamber which can be pumped down to pressures of around 0.6mbar. A feed gas, in this case argon is then fed into the chamber, raising the working pressure to 1mbar before ignition of the plasma using between 5 and 100W of RF power at 13.56MHz [84], it was found that 40-80W gave a stable plasma. The ink for curing was a commercially available nanoparticle suspension from Harima chemical, consisting of 30 nm silver particles, 57.4% by weight. The ink was printed with a single, 70µm nozzle Microdrop PIJ print head onto a substrate held at a temperature of 120ºC. Two polymer substrates were tested; polycarbonate with Tg

= 140ºC and PET, Tg = 98°C. Glass microscope slides were used to thermally sinter control samples.

It was found that both the thermal control samples and the plasma sintered samples achieved resistivity of between 2.5 and 3x bulk silver after around 1 hour, this can be seen in Figure 2.31, left. The small difference in final value between the glass substrate, thermally sintered samples and the polymer foil plasma samples is believed to be due to the higher thermal conductivity of the glass. Plasma curing of the same ink on glass required significantly less energy for this same reason. A related drawback to the plasma sintering process is the formation of a skin layer. It was found that printing ever thicker layers resulted in the same line resistivity. This is because the energetic plasma species have a certain penetration depth which limits the thickness able to be cured. A plot of thickness against resistivity can also be seen in Figure 2.31, right, note the deviation from predicted. This was confirmed by removal of the top layer of a thick cured track. The exposed uncured track showed no conductivity until further treatment with the same plasma conditions. This limited penetration depth, along with the slow sintering time make this low temperature plasma technology less attractive than a thermal process for OSI, the only benefit is the ability to use low glass transition temperature polymers.

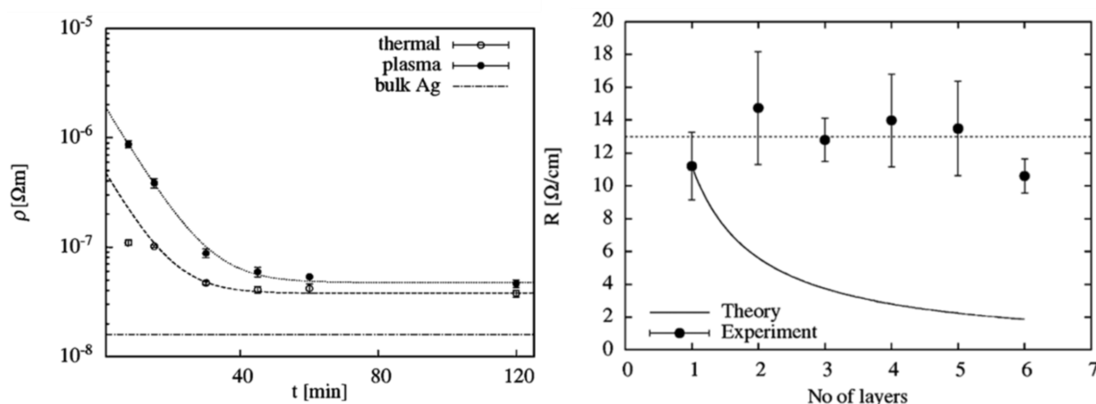


Figure 2.31: Left; resistivity of printed tracks against time for the application of low pressure plasma. Right; predicted resistivity of thicker layers against experimentally measured values, the departure from prediction confirms the creation of a skin layer of cured material with uncured material underneath [74].

Investigation into atmospheric plasma is more promising [85]. The atmospheric plasma is generated within a thin, pen shaped, device with a feed gas, argon in this case, flowing between two electrodes. The pressurised gas is ignited into a plasma by the electrodes and forced out of the end of the ‘pen’ forming a highly localised jet of

plasma. Five substrates were investigated for their susceptibility to plasma, PEN, PI, PMMA, PPHM and PET. Each was placed in a low pressure plasma oven, similar to the one described above, and an etch rate calculated in 30 minute intervals. It was found that the polymer foils with the highest glass transition temperature, PI and PEN, were the least susceptible to etching by plasma. PI and PEN were therefore selected for further testing. Argon was chosen as the feed gas for the atmospheric plasma to avoid surface activation of the polymer foils, which occurs through the incorporation of oxygen. Oxygen incorporation has been linked to increased etch rates [85]. It is noted that the maximum plasma temperature is 60°C, this type of plasma is also called a cold plasma.

Three inks were investigated, the same commercial ink from Harima chemical, 57.4% loaded, 5-10nm Ag nanoparticles, a commercial 20%, 30-50nm silver nano ink from Cabot and a custom ink designed in house with 30% loading of 30nm silver nanoparticles. All three were printed with a DMP using drop pitches of 21.6μm (Cabot), 31.75μm (Harima) and 25.4μm (In house), the difference spacing's depended on the ink properties and were chosen so as to form continuous tracks. The two commercial inks had to be dried on a hot plate for 5 minutes at 60°C, the custom ink for 5 minutes at room temperature before sintering with the atmospheric plasma. It was found, as expected, that smaller plasma stand-offs, slower translation speeds and more passes result in more complete sintering both in terms of resistivity and morphology when viewed under SEM. Sintering can be initiated in as little as 2 minutes at 4mm stand-off and 20mm/s translation. A plot of resistivity against number of passes of the plasma gun can be seen for each ink in Figure 2.32. The Cabot ink achieved 10x bulk resistivity with 2 minutes of atmospheric plasma, 18.8x bulk for 2 minutes of thermal and 8.8x bulk for 60minutes of thermal. The Harima ink achieved 16x bulk resistivity with plasma sintering. It was not conductive after 2 minutes of thermal sintering but obtained 1.9x bulk after 60 minutes of thermal sintering. The custom ink obtained 8.2x bulk resistivity after plasma sintering. It was not conductive after 2 minutes of thermal sintering but obtained a bulk resistivity of 2.9x after 60 minutes of thermal sintering. In all cases the plasma outperformed the equivalent duration thermal process however it never achieved the low resistivities of the longer thermal processing. For OSI this type of plasma would still likely be to slow to use on the tool and the resistivities may not be low enough.

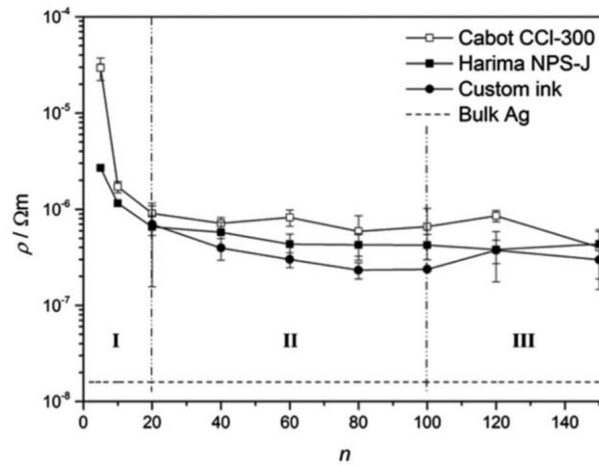


Figure 2.32: A plot of resistivity against number of passes of the plasma head, in all cases the achieved resistivity is significantly larger than the value for the bulk metal [85].

2.4.8 Microwave sintering

Microwave sintering of conductive inks has been thoroughly investigated, both as a standalone technique[81]–[83] and combined with IPL and plasma [77], [78]. Microwave energy can be coupled into solids through two interactions, either via charge carriers or rotary dipoles. Highly conductive metals, with many free carriers have a high absorption coefficient for microwave radiation [82] but can act as reflectors due to their low skin depth [83]. It has also been shown that the absorption of microwave radiation by metal nanoparticles is greater than bulk metal, although this is not fully understood it is believed to be related to Maxwell-Wagner polarization from accumulation of charge at grain interfaces [86]. The low skin depth means that only the first 1.3μm, the penetration depth of silver with 2.45GHz microwaves, directly absorbs the microwave energy. It was postulated that the high thermal conductivity of silver will lead to relatively uniform heating [86]. However this is in opposition to the observation of a skin layer during low pressure plasma sintering, discussed in Section 2.4.7 [84]. It is, however, possible that the temperatures reached in low pressure plasma sintering may not be as high as during microwave sintering which would mean the temperature of the material below the skin depth could be high enough to avoid the formation of a conductive skin. The focus of this work [82], [83] has been on flexible polymer substrates since they are not suitable to a standard thermal cure. The only way for polymers to absorb microwave radiation is through dielectric loss mechanisms related to rotary dipoles. In polymers below the glass transition temperature the

rotational freedom of dipoles is small and therefore the skin depth is close to infinite leading to negligible absorption. This important result means that inkjet printed metal can be selectively sintered on polymer substrates without damaging the substrate.

Microwave curing was tested using a commercial dispersion of 60% silver by weight, 5-10nm silver nanoparticle ink from Harima Inc printed onto a PI substrate [82]. At a temperature of 150°C, a speed of 1.25 mm/s, and with a drop pitch of 100µm continuous printed lines were formed. Additionally, squares and antenna structures were printed. The lines were placed in a microwave reactor with a constant output power of 300W and the electrical conductance was measured at intervals of 30s and found to be approximately constant after 240s, see Figure 2.33. Longer durations did not result in increased conductance but did cause deformation/decomposition of the substrate near to the printed tracks. The final resistivity was around 20x bulk silver which was similar to the value obtained for oven sintering of 60minutes at 220°C. It should be noted that the substrate containing vessel inside the microwave oven reached temperatures of 200°C during the microwave sintering process, similar to the thermal sintering temperature.

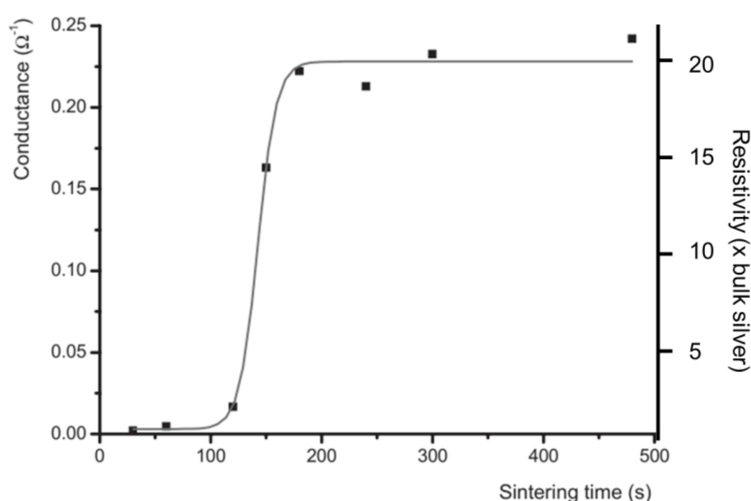


Figure 2.33: A plot of conductance against sintering time in a microwave oven for a silver nanoparticle ink on a PI substrate. After ~240s the resistivity has reached its maximum value, adapted from [77].

The impact of antenna structures on the final resistance value of printed lines exposed to microwave radiation has also been investigated [83]. Simple antenna structures were printed on to a PEN foil and sintered for 60 minutes in a conventional oven at 110°C. A further track was printed between the metallic probes, see Figure 2.34. This line was then placed in an oven at 110°C for 1-5minutes to promote solvent evaporation and close packing of nanoparticles before application of microwave radiation. The initial

resistance values were in the range of 10^8 and $10^2\Omega$. The printed antenna/track structure was then exposed to a 1s burst of microwave radiation at a power of 1W with a directional microwave device and the final resistance measured. The resistance achieved after the microwave flash exposure was dependent on the resistance of the track after solvent evaporation, anything in the range of 10^2-$10^4\ \Omega$ could be decreased to only a few Ohms but with higher starting line resistivities the 1s exposure was insufficient to initiate sintering. An important outcome was that compared to the same line without the antenna the resistance was always 1 order of magnitude lower using the antenna than without. Different antenna surface areas were investigated and it was found that the larger antennas had a greater effect, see Figure 2.34. Application of a 60s burst at the same power of 1W moved the threshold for effective sintering from $10^5\ \Omega$ up to $10^7\ \Omega$. The obtained resistivity values were found to be in the range of 3-10x bulk silver dependent on antenna area and line starting resistance. It should be noted that the antenna structure does not have to be in direct contact with the printed line and can be re-used. The main drawback to this work is that even with the antenna structure the lines had to be dried for 60-300s in an oven before microwave sintering could take place, it is difficult to see a situation where that is acceptable unless the time for drying/pre-sinter can be reduced and integrated into a production line. Throughout this work the microwave sintering has been compared to an oven cure of 60minutes, this isn't in line with the requirements of most inks, particularly those with 5-10nm particle size. It would be expected that such an ink at the 220°C temperature used in the first part of this work would sinter in a quarter of that time however in this case it is limited by the substrate. Therefore the benefit stated of reduction in processing times from 60minutes down to 240s is potentially misleading unless the caveat of on this PEN substrate is added.

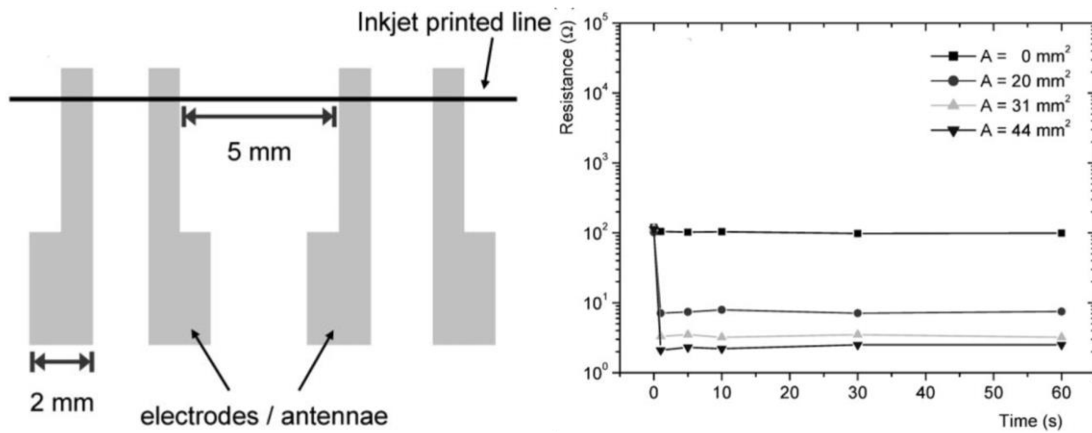


Figure 2.34: Left; a diagram of the antenna structure used to promote microwave absorption in printed tracks. Right; the resistance of printed lines against time for different antenna areas at constant microwave intensity [78].

Further analysis has been undertaken on the microstructure of Hybrid Variable Frequency Microwave (HVFM) sintered printed tracks in comparison to Rapid Thermal Annealing (RTA) [81]. In this study a 20% by weight silver nanoparticle ink with particles of 25-30nm dispersed in polar solvents manufactured by Sun Chemical was printed using a Spectra Jetpac print head, using n-type [100] silicon as a substrate. RTA was conducted in an N_2 atmosphere using a halogen lamp oven manufactured by Jipelec. HVFM curing used a Lambda Technologies MicroCures 2100 oven using a variable frequency mode centred around 6.425GHz, bandwidth 0.75GHz and sweep rate 0.1seconds. Both devices had temperature feedback allowing direct control of temperature in a closed loop configuration. The processes were conducted for 15 minutes at temperatures ranging from 130-300°C with ramps from 0.1°C/s to 150°C/s for RTA and 0.1°C/s-10°C/s for HVFM. After cure the film thickness was found to be 2-3µm. The HVFM sintering was found to create consistently larger grains than the equivalent RTA process. The reason given for this is greater uniformity of heating due to the volumetric coupling of the microwave radiation. Mean grain size is measured to be around 300nm for a 300°C treatment with the maximum ramp rate of 10°C/s using the HVFM, in contrast with the RTA the maximum mean grain size is around 100nm. This is further evidenced by the resistivity values obtained for a given temperature using the two heating methods, HVFM always obtains lower resistivities although at the highest RTA temperature of 300°C the difference is smallest. Achieved resistivity for HVFM was only 1.3x bulk which compares favourably with the 4-5x bulk obtained with the purely thermal processing. Plots of resistivity against temperature can be seen in Figure 2.35. Porosity/grain size is attributed with the difference in resistivities

between the two techniques and this is assessed using the nano-identation technique to measure mechanical stiffness which is related to porosity. It is found that, as expected, the lower conductivity films are more porous, this can be seen in the SEM images in Figure 2.35.

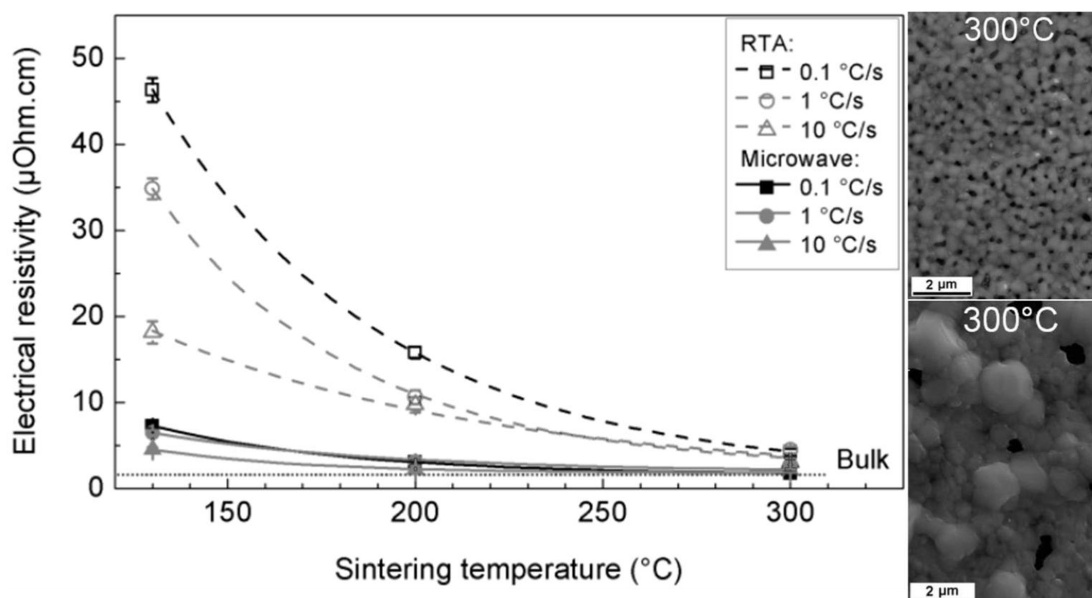


Figure 2.35: A plot of resistivity against temperature for both RTA and HVFM. Right; SEM images of structure obtained with both techniques, top is HVFM and the bottom is RTA [79].

In conclusion it has been found that when measured side by side with RTA microwave curing has benefits in terms of minimum achievable resistivity and material morphology. The second set of work on HVFM shows promise although it still takes 15minutes to fully sinter a printed pattern, it would have been interesting to see the effect of time on the resistivity, this may have revealed a useful regime in terms of both resistivity and time which would also have the benefit of selectively heating the metallic ink while leaving polymer substrates undamaged.

The main drawback to microwave sintering is the requirement of some conductivity before the use of microwave radiation in order to aid absorption. In the previous work this has been achieved with an initial thermal process which evaporates the organic constituents of the ink and allows the onset of conductivity. Combination microwave sintering with both Intense Pulsed Light sintering (IPL) and low pressure plasma has been demonstrated in order to remove this thermal step [77], [78], discussed below.

2.4.9 Combined approaches to sintering

For manufacture based on a roll-to-roll (R2R) mode on a PEN substrate (Tg=120°C) IPL was used as the pre-sinter step for microwave curing [78] replacing the previously reported 10minute bake at 110°C. These tests were performed using a commercially available silver nanoparticle ink Sun Chemical U5603. It was found that there was a trade-off between the total energy input through IPL, the number of flashes, individual flash intensity and the total time. Optimum parameters provided a resistivity of 3.6x bulk silver after only 10s. This was found to be the lower limit with higher energy pulses or longer exposure times leading to substrate damage. The lower limit is believed to be due to the metallic ink becoming highly reflective to the IPL which delivers the bulk of the energy in the visible region of the spectrum. The high conductivity of the IPL pre-sintered films leads to excellent absorption of microwave radiation. On exposure of 1s at a power of 1W, the lowest possible power with the equipment used, the final resistivity value was as low as 2.5x bulk silver. For comparison a similar sample was thermally sintered for 1 hour at 110°C, the maximum temperature allowable with the PEN substrate, and the obtained resistivity after microwave cure was 2.9x bulk. The total process time for this combined IPL and microwave sinter is around 15s, compatible with R2R manufacture. In order to test the applicability to device manufacture a honeycomb pattern often used for OPV/OLED applications was prepared, in R2R mode, and passed through an IPL system consisting of 2 elliptical reflectors, one above and one below the substrate with the substrate at their joint focus. Figure 2.36 shows a diagram of the printed structure and an image of the complete device. The prepared samples were then split into squares and placed in the microwave cure system. They were exposed for 3s at 10W with the previously described antenna pattern used to aid microwave absorption, the higher power is due to the significantly larger volume of material used for these patterns compared to earlier tests on single lines. The final resistivity of this structure was 20x bulk silver, acceptable for some organic electronic applications and total process time was 15s. This result demonstrates the possibility of R2R processing using these techniques but it also highlights one of the drawbacks that the required microwave exposure power is related to the volumes of absorbing material within the system. For OSI where the printed electronic structure is on top of a highly absorbing metallic back contact, this is likely to become an issue.

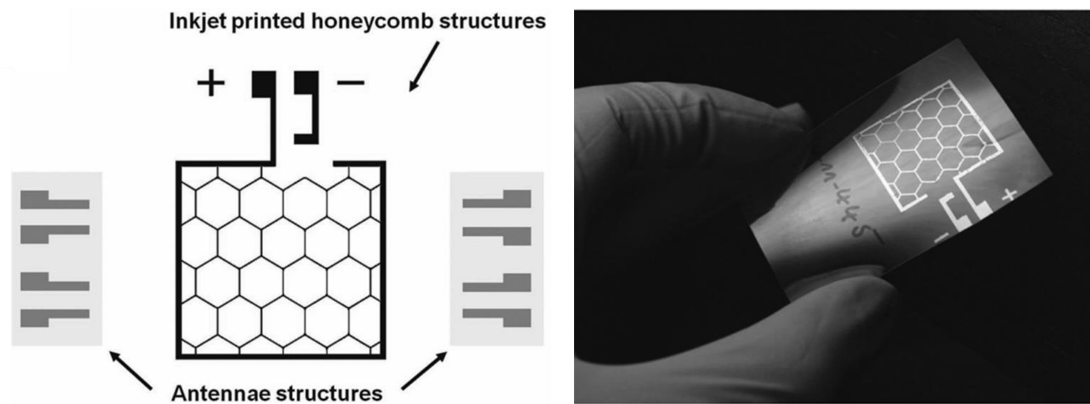


Figure 2.36: Left; a diagram of the printed honeycomb structure showing the positions of the antennas. Right; an image of a complete device manufactured with this combined approach in R2R mode [80].

The other combined approach investigated is the combination of low pressure Argon plasma and microwave sintering using a tailored, aqueous nanoparticle ink containing 20% silver by weight [77]. The behaviour of this ink, when exposed to a standard thermal sintering process, was studied at varying temperatures. As expected the higher temperatures produced the lowest resistivity with the best results at 200°C for 30 minutes being 3.7x bulk. Low pressure argon plasma sintering was found to plateau at a resistivity of 17x bulk after 15-20minutes which is comparable with 30mins at 175°C thermal cure however the substrate temperature was measured to reach only 70°C. Using a plasma duration varying between 4 and 12 minutes combined with an antenna assisted microwave cure of 1s at 1W it was found that the minimum required conductivity to allow microwave curing to take place was 1000x bulk. The final achieved resistivity is heavily dependent on the length of track between the two antenna structures, with an optimum at around 5mm. Using this optimum track length an exceptionally low resistivity of 1.7x bulk was achieved. Achieving the same resistivity with thermal processes alone with this ink required temperatures of >450°C. A flexible Electro Luminescence (EL) device was manufactured using this techniques on a PET substrate, the device was composed of PET, ITO, ZnS:$BaTiO_3$ and the silver printed structure. Upon application of 100V the EL material emitted light only in the locations of the printed silver features. Figure 2.37 shows an image of the manufactured EL device.

Figure 2.37: Electro luminescent printed electronic devices sintered using combined low pressure plasma and microwave flash sintering [68].

2.4.10 Chemical sintering and 'self-sintering' inks

The final technique for sintering of nanoparticulate inks is chemically based sintering at room temperature [86], [87]. It was found that an aqueous, i.e. water based, silver nano particle ink using poly acrylic acid (PAA) as its stabilising agent spontaneously coalesced when mixed with a minimum concentration of poly(dially dimethylammonium chloride) (PDAC) [87]. This was used to print self-sintering tracks on paper, photo-paper and PET by first coating the substrate with a thin layer of PDAC, with the notable exception of photo-paper which was found to already contain a PDAC like molecule. It was found that there was a minimum mass ration of PDAC/Ag of 0.2 to cuase maximum particle coalescence and the changes were irreversible. Printing onto the three substrates resulted in conductive films with resistivities of 4.3x bulk on the photo paper and around 44x bulk on the copier paper. It has been hypothesised that the mechanism is desorption of the PAA stabilising agent resulting in charge neutralisation of the particles, facilitating close packing and coalescence. Again EL devices were fabricated using the same stack on a PET substrate, as in the combined plasma/microwave case, working devices were manufactured.

A self-sintering silver nanoparticle ink has also been developed using a similar chemical reaction [86]. Starting from a similar base of an aqueous silver nanoparticle ink stabilised with PAA with 20% by weight silver it was found that NaCl acts to facilitate desorption of the stabilising agent, in a similar manner to PDAC in the previous work. The onset of this desorption and therefore self-sintering was found to be dependent on

the concentration of NaCl with onset at 50mM with a rapid and significant increase in particle size after this minimum value from 15nm to 0.2-6μm. Figure 2.38 shows a plot of NaCl concentration against average particle size in the self-sintering ink.

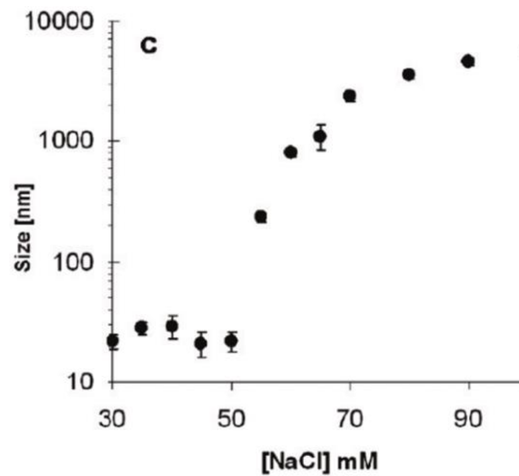


Figure 2.38: A plot of particle size against concentration of NaCl, after a threshold value particle agglomeration takes place increasing the average grain size from around 15nm to 0.2-6μm resulting in reduced resistivity [82].

A self-sintering ink was formulated based on this principle by adding a small amount of NaCl to the base formulation. At low concentrations there is little effect and the formulation is stable however once printed the ink begins to dry by evaporation of the aqueous carrier, increasing the concentration of NaCl until particle coalescence is triggered. A self-sintering ink was printed onto a PET substrate and allowed to dry at room temperature, the resultant track showed a resistivity of 10x bulk silver. It was noted that sintered silver grains were characterised by lattice mismatches, thought to be due to the low temperature sintering process not allowing optimisation of lattice structure which resulted in low density packing of the grains. Printing the standard form of the ink and allowing to dry allowed closer packing of the nanoparticles and then following this with a treatment in HCl vapour resulted in a resistivity of 2.4x bulk silver. In order to achieve such a low resistivity with thermal sintering processes required heating at 320°C for 30minutes. This technique is very promising for printed electronics on flexible substrates. At this time it is unclear whether 10x bulk resistivity is low enough for OSI however with further improvements these ink formulations could become very interesting.

2.4.11 Summary and conclusions of inkjet deposition for functional materials

The principles of piezo actuated DoD inkjet printed have been described. Methodologies for optimisation of drop generation have been introduced including 'drop watching' for visualisation and control of waveform for modification. The dynamics of drop/surface interaction have been introduced and been shown to be dependent on both the surface energy of the substrate and the surface tension of the liquid. Drop coalescence as required to print continuous tracks has been described along with the limitations from so called bulge instability.

The formulation space for inkjet inks in general and functional inks specifically has been briefly examined. It should be noted that formulation of inks with high solid content, as required for conductive nanoparticle suspensions, is more challenging than formulation for typical graphics applications. The post process for converting conductive inks into conductive tracks, thermal baking has been described and it has been noted that it would be difficult to integrate with inline production processes. A range of alternative approaches to post deposition processing have been described, some of which have the potential to be used in continuous manufacturing processes such as OSI.

2.5 References

[1] P.-O. Westin, U. Zimmermann, M. Ruth, and M. Edoff, “Next generation interconnective laser patterning of CIGS thin film modules,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 4, pp. 1062–1068, Apr. 2011.

[2] P.-O. Westin, J. T. Wätjen, U. Zimmermann, and M. Edoff, “Microanalysis of laser micro-welded interconnections in CIGS PV modules,” *Sol. Energy Mater. Sol. Cells*, vol. 98, pp. 172–178, Mar. 2012.

[3] S. Haas, S. Krumscheid, A. Bauer, A. Lambertz, and U. Rau, “Novel series connection concept for thin film solar modules,” *Simulation*, 2012.

[4] C. Dunsky and F. Colville, “Solid state laser applications in photovoltaics manufacturing,” *SPIE Proc.*, vol. 6871, no. Solid State Lasers XVII, p. 687219, 2008.

[5] K. Ellmer, “Past achievements and future challenges in the development of optically transparent electrodes,” *Nat. Photonics*, vol. 6, no. December, pp. 808–816, 2012.

[6] J. Bovatsek, a. Tamhankar, R. S. Patel, N. M. Bulgakova, and J. Bonse, “Thin film removal mechanisms in ns-laser processing of photovoltaic materials,” *Thin Solid Films*, vol. 518, no. 10, pp. 2897–2904, Mar. 2010.

[7] John perlin, “The Silicon solar cell Turns 50,” *NREL Rep. No. BR-520-33947*, 2004.

[8] M. A. Green, “Thin-film solar cells : review of materials , technologies and commercial status,” *J. Mater. Sci. Mater. Electron.*, vol. 18, no. S1, pp. 15–19, 2007.

[9] V. Avrutin, N. Izyumskaya, and H. Morkoç, “Semiconductor solar cells: Recent progress in terrestrial applications,” *Superlattices Microstruct.*, vol. 49, no. 4, pp. 337–364, Apr. 2011.

[10] A. Shah and R. Platz, “Thin-film silicon solar cells: A review and selected trends,” *Sol. energy Mater. Sol. cells*, pp. 501–520, 1995.

[11] M. A. Green, “Crystalline and thin-film silicon solar cells : state of the art and future potential,” vol. 74, pp. 181–192, 2003.

[12] D. E. Carlson and C. R. Wronski, “Amorphous silicon solar cell Amorphous silicon solar cell,” *Appl. Phys.*, vol. 671, no. 1976, pp. 1–4, 1976.

[13] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, “Solar cell ef fi ciency tables (version 43),” no. version 43, pp. 1–9, 2014.

[14] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, “Solar cell efficiency tables (version 39),” *Library (Lond).*, no. version 39, pp. 12–20, 2012.

[15] P. Buehlmann, J. Bailat, D. Dominé, a. Billet, F. Meillaud, a. Feltrin, and C. Ballif, “In situ silicon oxide based intermediate reflector for thin-film silicon micromorph solar cells,” *Appl. Phys. Lett.*, vol. 91, no. 14, p. 143505, 2007.

[16] S. Haas, G. Schöpe, C. Zahren, and H. Stiebig, “Analysis of the laser ablation processes for thin-film silicon solar cells,” *Appl. Phys. A*, vol. 92, no. 4, pp. 755–759, May 2008.

[17] S. Haas, S. Ku, and K. Du, “Patterning of thin-film silicon modules using lasers with tailored beam shapes and different wavelengths,” *Proc. 23rd Eur.*, 2008.

[18] S. Haas, A. Gordijn, and H. Stiebig, “High Speed Laser Processing For Monolithical Series Connection of Silicon Thin-film Modules,” *Processing*, no. November 2007, pp. 195–203, 2008.

[19] A. Compaan, I. Matulionis, and S. Nakade, “Laser scribing of polycrystalline thin films,” *Opt. Lasers Eng.*, vol. 34, no. September, 2000.

[20] A. S. Steve Golay, Johannes Meier, Sébastien Dubail, Ulrich Kroll, “Laser scribing of p-i-n/p-i-n ‘micromorph’ (a-Si:H/μc-Si:H) tandem cells,” *Small*, pp. 3–6, 2000.

[21] L. C. Augustine McEvoy, Tom Markvart, *Practical Handbook of Photovoltaics: Fundamentals and applications*. 2011.

[22] P. V Meyers, “DESIGN OF A THIN FILM CdTe S O L A R CELL Summary Cadmium telluride was originally considered for thin film solar cells because of its optimum band gap , high optical absorption coefficient and ability to be doped . Furthermore , it is a stable compound w,” vol. 23, pp. 59–67, 1988.

[23] First Solar, “First Solar corporate data sheet,” *http://www.firstsolar.com/About-First-Solar/~/media/Files/Corporate/First%20Solar%20Corporate%20Datasheet.ashx*, 2011.

[24] N. Romeo, A. Bosio, A. Romeo, and S. Mazzamuto, “Industrial Upscaling of CdTe / CdS Thin Film Solar Cells E-mail address : Nicola.Romeo@unipr.it (Nicola Romeo). Back contact C d T e,” no. September, pp. 2–5, 2006.

[25] Z. Jingquan, F. Lianghuan, L. Zhi, C. Yaping, L. Wei, W. Lili, L. Bing, C. Wei, and Z. Jiagui, “Preparation and performance of thin film CdTe mini-module,” *Sol. Energy Mater. Sol. Cells*, vol. 93, no. 6–7, pp. 966–969, Jun. 2009.

[26] P. V Meyers and C. E. Mark, “FIRST SOLAR POLYCRYSTALLINE CdTe THIN FILM PV,” pp. 2024–2027, 2006.

[27] D. Cunningham, M. Rubcich, and D. Skinner, “Cadmium telluride PV module manufacturing at BP Solar,” *Prog. Photovoltaics Res. Appl.*, vol. 10, no. 2, pp. 159–168, Mar. 2002.

[28] J. Perrenoud, B. Schaffner, S. Buecheler, and a. N. Tiwari, “Fabrication of flexible CdTe solar modules with monolithic cell interconnection,” *Sol. Energy Mater. Sol. Cells*, vol. 95, pp. S8–S12, May 2011.

[29] M. a. Contreras, M. J. Romero, and R. Noufi, “Characterization of Cu(In,Ga)Se2 materials used in record performance solar cells,” *Thin Solid Films*, vol. 511–512, pp. 51–54, Jul. 2006.

[30] N. G. Dhere, “Toward GW/year of CIGS production within the next decade,” *Sol. Energy Mater. Sol. Cells*, vol. 91, no. 15–16, pp. 1376–1382, Sep. 2007.

[31] R. Murison, C. Dunsky, M. Rekow, C. Dinkel, J. Pern, L. Mansfield, T. Panarello, and S. Nikumb, “CIGS P1, P2, and P3 laser scribing with an innovative fiber laser,” *2010 35th IEEE Photovolt. Spec. Conf.*, pp. 000179–000184, Jun. 2010.

[32] T.-W. Kim, H.-J. Pahk, H. K. Park, D. J. Hwang, and C. P. Grigoropoulos, “Comparison of multilayer laser scribing of thin film solar cells with femto, pico, and nanosecond pulse durations,” *Proc. SPIE*, vol. 7409, p. 74090A–74090A–10, 2009.

[33] J. Hermann, M. Benfarah, G. Coustillier, S. Bruneau, E. Axente, J.-F. Guillemoles, M. Sentis, P. Alloncle, and T. Itina, “Selective ablation of thin films with short and ultrashort laser pulses,” *Appl. Surf. Sci.*, vol. 252, no. 13, pp. 4814–4818, Apr. 2006.

[34] P.-O. Westin, U. Zimmermann, and M. Edoff, “Laser patterning of P2 interconnect via in thin-film CIGS PV modules,” *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 10, pp. 1230–1235, Oct. 2008.

[35] D. Ruthe, K. Zimmer, and T. Höche, “Etching of CuInSe2 thin films—comparison of femtosecond and picosecond laser ablation,” *Appl. Surf. Sci.*, vol. 247, no. 1–4, pp. 447–452, Jul. 2005.

[36] H. P. Huber, M. Englmaier, C. Hellwig, A. Heiss, T. Kuznicki, M. Kemnitzer, H. Vogt, R. Brenning, and J. Palm, “High speed structuring of CIS thin-film solar cells with picosecond laser ablation,” *Proc. SPIE*, vol. 7203, p. 72030R–72030R–9, 2009.

[37] M. Rekow, R. Murison, C. Dunsky, C. Dinkel, J. Pern, L. Mansfield, T. Panarello, and S. Nikumb, “CIGS P1, P2, P3 Scribing Processes using a Pulse Programmable Industrial Fiber Laser,” 2010.

[38] F. J. Pern, L. Mansfield, S. Glynn, B. To, C. Dehart, M. Rekow, R. Murison, T. Panarello, C. Dunsky, N. Renewable, and P. Lasers, “ALL-LASER SCRIBING FOR THIN-FILM CuinGaSe2 SOLAR CELLS,” *Sol. Cells*, pp. 3479–3484, 2010.

[39] A. Blayo, B. Pineaux, L. De Génie, P. Lgp, P. B. P. Saint-martin, and H. Cedex, "Printing Processes and their Potential for RFID Printing," no. october, pp. 7–10, 2005.

[40] B.-J. de Gans, P. C. Duineveld, and U. S. Schubert, "Inkjet Printing of Polymers: State of the Art and Future Developments," *Adv. Mater.*, vol. 16, no. 3, pp. 203–213, Feb. 2004.

[41] H. Wijshoff, "The dynamics of the piezo inkjet printhead operation☆," *Phys. Rep.*, vol. 491, no. 4–5, pp. 77–177, Jun. 2010.

[42] B. Derby, "Inkjet Printing of Functional and Structural Materials: Fluid Property Requirements, Feature Stability, and Resolution," *Annu. Rev. Mater. Res.*, vol. 40, no. 1, pp. 395–414, Jun. 2010.

[43] D. B. Bogy and F. . Talke, "Experimental and Theoretical Study of Wave Propagation Phenomena in Drop-on-Demand Ink Jet Devices," *IBM J. Res. Dev.*, vol. 28, no. 3, pp. 314–321, 1984.

[44] E. Tekin, P. J. Smith, and U. S. Schubert, "Inkjet printing as a deposition and patterning tool for polymers and inorganic particles," *Soft Matter*, vol. 4, no. 4, p. 703, 2008.

[45] N. Reis, C. Ainsley, and B. Derby, "Ink-jet delivery of particle suspensions by piezoelectric droplet ejectors," *J. Appl. Phys.*, vol. 97, no. 9, p. 094903, 2005.

[46] G. D. Martin, S. D. Hoath, and I. M. Hutchings, "Inkjet printing - the physics of manipulating liquid jets and drops," *J. Phys. Conf. Ser.*, vol. 105, p. 012001, Mar. 2008.

[47] J. E. Fromm, "Numerical Calculation of the Fluid Dynamics of Drop-on-Demand Jets," *IBM J. Res. Dev.*, vol. 28, no. 3, pp. 322–333, May 1984.

[48] N. Reis and B. Derby, "inkjet printnig of ceramic suspensions N Reis B Cerby.pdf." 2000.

[49] B. Derby, "Inkjet printing ceramics: From drops to solid," *J. Eur. Ceram. Soc.*, vol. 31, no. 14, pp. 2543–2550, Nov. 2011.

[50] D. Jang, D. Kim, and J. Moon, "Influence of fluid physical properties on ink-jet printability.," *Langmuir*, vol. 25, no. 5, pp. 2629–35, Mar. 2009.

[51] D. B. van Dam and C. Le Clerc, "Experimental study of the impact of an ink-jet printed droplet on a solid substrate," *Phys. Fluids*, vol. 16, no. 9, p. 3403, 2004.

[52] S. Schiaffino and A. a. Sonin, "Molten droplet deposition and solidification at low Weber numbers," *Phys. Fluids*, vol. 9, no. 11, p. 3172, 1997.

[53] G. M. Whitesides and P. E. Laibinis, "Wet Chemical Approaches to the Characterization of Organic Surfaces: Self- Assembled Monolayers, Wetting, and the Physical-Organic Chemistry of the Solid-Liquid Interface," no. 11, pp. 87–96, 1990.

[54] D. Y. Kwok and a. W. Neumann, *Contact angle measurement and contact angle interpretation*, vol. 81, no. 3. 1999, pp. 167–249.

[55] R. Wenzel, “Resistance of solid surfaces to wetting by water,” *Ind. Eng. Chem.*, vol. 28, no. 8, pp. 988–994, 1936.

[56] B. D. Cassie, “wetting of porous surfaces,” no. 5, pp. 546–551, 1944.

[57] H. Search, C. Journals, A. Contact, M. Iopscience, and I. P. Address, “Wetting of rough surfaces,” vol. 445.

[58] G. Palasantzas and J. T. M. de Hosson, “Wetting on rough surfaces,” *Acta Mater.*, vol. 49, no. 17, pp. 3533–3538, Oct. 2001.

[59] W. A. Zisman, “Relation of the Equilibrium Contact Angle to Liquid and Solid Constitution,” *Contact Angle, Wettability, Adhes.*, 1964.

[60] M. Gindl, G. Sinn, W. Gindl, A. Reiterer, and S. Tschegg, “A comparison of different methods to calculate the surface free energy of wood using contact angle measurements,” *Colloids Surfaces A Physicochem. Eng. Asp.*, vol. 181, no. 1–3, pp. 279–287, Jun. 2001.

[61] J. Stringer and B. Derby, “Formation and stability of lines produced by inkjet printing.,” *Langmuir*, vol. 26, no. 12, pp. 10365–72, Jun. 2010.

[62] W. Thomson and Lord Kelvin, “Inkjet printing 1.,” no. 1, pp. 1–21.

[63] A. Kamyshny, J. Steinke, and S. Magdassi, “Metal-based Inkjet Inks for Printed Electronics,” *Open Appl. J.*, vol. 4, pp. 19–36, 2011.

[64] J.-A. Jeong, J. Lee, H. Kim, H.-K. Kim, and S.-I. Na, “Ink-jet printed transparent electrode using nano-size indium tin oxide particles for organic photovoltaics,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 10, pp. 1840–1844, Oct. 2010.

[65] L. Vanmaele and E. Verdonck, “Ultraviolet curable ink consists of a copolymer of acrylic monomer and vinyl ether monomers; and a colorant,” US6310115 B12001.

[66] K. Seerden, N. Reis, J. Evans, P. Grant, J. Halloran, and B. Derby, “Ink-jet printing of wax-based alumina suspensions,” vol. 20, pp. 2514–2520, 2001.

[67] P. J. Smith, D. Y. Shin, J. E. Stringer, B. Derby, and N. Reis, “Direct ink-jet printing and low temperature conversion of conductive silver patterns,” *J. Mater. Sci.*, vol. 41, pp. 4153–4158, 2006.

[68] V. Sanchez-Romaguera, M.-B. Madec, and S. G. Yeates, “Inkjet printing of 3D metal–insulator–metal crossovers,” *React. Funct. Polym.*, vol. 68, no. 6, pp. 1052–1058, Jun. 2008.

[69] S. Jeong, K. Woo, D. Kim, S. Lim, J. S. Kim, H. Shin, Y. Xia, and J. Moon, “Controlling the thickness of the surface oxide layer on Cu nanoparticles for the

fabrication of conductive structures by ink-jet printing," *Adv. Funct. Mater.*, vol. 18, pp. 679–686, 2008.

[70] D. Li, D. Sutton, A. Burgess, D. Graham, and P. D. Calvert, "Conductive copper and nickel lines via reactive inkjet printing," *J. Mater. Chem.*, vol. 19, no. November 2008, p. 3719, 2009.

[71] S. Magdassi, *The Chemistry of Ink jet inks*. 2010.

[72] J. Perelaer and U. S. Schubert, "Novel approaches for low temperature sintering of inkjet-printed inorganic nanoparticles for roll-to-roll (R2R) applications," *J. Mater. Res.*, vol. 28, no. 04, pp. 564–573, Feb. 2013.

[73] P. Buffat and J. Borel, "Size effect on the melting temperature of gold particles," *Phys. Rev. A*, 1976.

[74] H.-H. Lee, K.-S. Chou, and K.-C. Huang, "Inkjet printing of nanosized silver colloids.," *Nanotechnology*, vol. 16, no. 10, pp. 2436–41, Oct. 2005.

[75] D. Kim and J. Moon, "Highly Conductive Ink Jet Printed Films of Nanosilver Particles for Printable Electronics," *Electrochem. Solid-State Lett.*, vol. 8, no. 11, p. J30, 2005.

[76] R. Abbel, T. van Lammeren, R. Hendriks, J. Ploegmakers, E. J. Rubingh, E. R. Meinders, and W. a. Groen, "Photonic flash sintering of silver nanoparticle inks: a fast and convenient method for the preparation of highly conductive structures on foil," *MRS Commun.*, vol. 2, no. 04, pp. 145–150, Dec. 2012.

[77] J. Perelaer, R. Jani, M. Grouchko, A. Kamyshny, S. Magdassi, and U. S. Schubert, "Plasma and microwave flash sintering of a tailored silver nanoparticle ink, yielding 60% bulk conductivity on cost-effective polymer foils.," *Adv. Mater.*, vol. 24, no. 29, pp. 3993–8, Aug. 2012.

[78] J. Perelaer, R. Abbel, S. Wünscher, R. Jani, T. van Lammeren, and U. S. Schubert, "Roll-to-roll compatible sintering of inkjet printed features by photonic and microwave exposure: from non-conductive ink to 40% bulk silver conductivity in less than 15 seconds.," *Adv. Mater.*, vol. 24, no. 19, pp. 2620–5, May 2012.

[79] S. H. Ko, H. Pan, C. P. Grigoropoulos, C. K. Luscombe, J. M. J. Fréchet, and D. Poulikakos, "Air stable high resolution organic transistors by selective laser sintering of ink-jet printed metal nanoparticles," *Appl. Phys. Lett.*, vol. 90, no. 14, p. 141103, 2007.

[80] M. L. Allen, M. Aronniemi, T. Mattila, A. Alastalo, K. Ojanperä, M. Suhonen, and H. Seppä, "Electrical sintering of nanoparticle structures.," *Nanotechnology*, vol. 19, no. 17, p. 175201, Apr. 2008.

[81] R. Cauchois, M. Saadaoui, A. Yakoub, K. Inal, B. Dubois-Bonvalot, and J.-C. Fidalgo, "Impact of variable frequency microwave and rapid thermal sintering on microstructure of inkjet-printed silver nanoparticles," *J. Mater. Sci.*, vol. 47, no. 20, pp. 7110–7116, Mar. 2012.

[82] J. Perelaer, B.-J. de Gans, and U. S. Schubert, "Ink-jet Printing and Microwave Sintering of Conductive Silver Tracks," *Adv. Mater.*, vol. 18, no. 16, pp. 2101–2104, Aug. 2006.

[83] J. Perelaer, M. Klokkenburg, C. E. Hendriks, and U. S. Schubert, "Microwave flash sintering of inkjet-printed silver tracks on polymer substrates.," *Adv. Mater.*, vol. 21, no. 47, pp. 4830–4, Dec. 2009.

[84] I. Reinhold, C. E. Hendriks, R. Eckardt, J. M. Kranenburg, J. Perelaer, R. R. Baumann, and U. S. Schubert, "Argon plasma sintering of inkjet printed silver tracks on polymer substrates," *J. Mater. Chem.*, vol. 19, no. 21, p. 3384, 2009.

[85] S. Wünscher, S. Stumpf, A. Teichler, O. Pabst, J. Perelaer, E. Beckert, and U. S. Schubert, "Localized atmospheric plasma sintering of inkjet printed silver nanoparticles," *J. Mater. Chem.*, vol. 22, no. 47, p. 24569, 2012.

[86] M. Grouchko, A. Kamyshny, C. F. Mihailescu, D. F. Anghel, and S. Magdassi, "Conductive inks with a 'built-in' mechanism that enables sintering at room temperature.," *ACS Nano*, vol. 5, no. 4, pp. 3354–9, Apr. 2011.

[87] S. Magdassi, M. Grouchko, O. Berezin, and A. Kamyshny, "Triggering the sintering of silver nanoparticles at room temperature.," *ACS Nano*, vol. 4, no. 4, pp. 1943–8, Apr. 2010.

[88] H.-S. Kim, S. R. Dhage, D.-E. Shim, and H. T. Hahn, "Intense pulsed light sintering of copper nanoink for printed electronics," *Appl. Phys. A*, vol. 97, no. 4, pp. 791–798, Aug. 2009.

[89] J. Chung, N. R. Bieri, S. Ko, C. P. Grigoropoulos, and D. Poulikakos, "In-tandem deposition and sintering of printed gold nanoparticle inks induced by continuous Gaussian laser irradiation," *Appl. Phys. A*, vol. 79, no. 4–6, pp. 1259–1261, Jul. 2004.

[90] N. R. Bieri, J. Chung, D. Poulikakos, and C. P. Grigoropoulos, "Manufacturing of nanoscale thickness gold lines by laser curing of a discretely deposited nanoparticle suspension," *Superlattices Microstruct.*, vol. 35, no. 3–6, pp. 437–444, Mar. 2004.

[91] T. Kumpulainen, J. Pekkanen, J. Valkama, J. Laakso, R. Tuokko, and M. Mäntysalo, "Low temperature nanoparticle sintering with continuous wave and pulse lasers," *Opt. Laser Technol.*, vol. 43, no. 3, pp. 570–576, Apr. 2011.

[92] E. M. Liston, L. Martinu, and M. R. Wertheimer, "Plasma surface modification of polymers for improved adhesion: a critical review," *J. Adhes. Sci. Technol.*, vol. 7, no. 10, pp. 1091–1127, Jan. 1993.

Chapter 3 : Laser Processing for OSI

3.1 Introduction

The first task in OSI is the development of suitable depth selective laser scribes. There is a requirement for two different scribe depths, the A scribe removes all material down to the glass substrate whereas the B scribe stops on the bottom contact. There are two different cell architectures; superstrate, typical in CdTe and TF-Si and substrate, typical in CIGS. OSI should be applicable to both architectures however the laser processes pose different challenges in each case.

In CdTe and TF-Si the front TCO contact can be any transparent conductor with sufficiently low sheet resistance, some common ones include fluorine dope tin oxide (FTO), tin doped indium oxide (ITO) and aluminium doped zinc oxide (AZO). The metallic back contact can be any metal which forms an Ohmic contact with the semiconductor, which is non-trivial in the case of CdTe but is typically silver, gold or molybdenum. The contacts for CIGS are more limited. Mo is used almost exclusively as the back contact material as it forms a thin $MoSe_2$ layer with the CIGS which forms an Ohmic contact [1]. AZO is the most commonly used transparent front contact for CIGS because of its low, <200°C, deposition temperature and the ability to grow a thin i-ZnO passivation layer followed by a highly doped AZO (aluminium zinc oxide) layer for high lateral conductivity [2].

The schematics in Figure 3.1 show the required laser scribe pattern for OSI and reflect the differences between superstrate and substrate cells. The most common substrate in both cases is thick, ~3mm, glass although flexible substrates are becoming more common, particularly for CIGS which has commercial offerings based on thin metal foils.

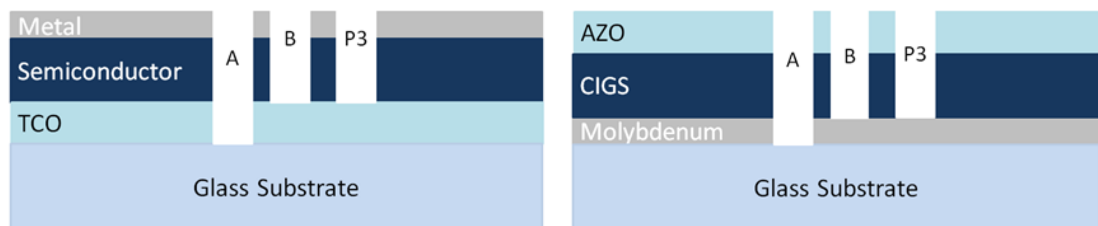


Figure 3.1: Left schematic of a superstrate cell, typically CdTe or TF-Si, the two contacts can be made of a variety of materials, see main text for examples. Right a similar schematic of a substrate CIGS cell, it is most common to use Molybdenum for the metallic contact and AZO for the transparent contact.

The standard industrial process for the interconnect of TF-PV on superstrate cells uses sequential laser scribing [3], [4]. The TCO is deposited and scribed, P1, the semiconductor is deposited and scribed to the TCO, P2, and the metal is deposited and scribed down to the TCO, P3. The P3 scribe process in the standard interconnect and OSI perform the same function, the laser process of the OSI B and P3 scribes is identical to the standard P3 process. This process is well established and produces scribes with good electrical characteristics. The new process for superstrate cells which must be developed is the A scribe which removes all the layers. The laser processing for CIGS is less straight forward and the subject of active research [5]–[7]. The industry standard is a laser to P1 scribe, the molybdenum, but mechanical P2 and P3 scribes using a needle to mechanically scribe the layers [8], this is further discussed in the later section devoted to CIGS scribing.

This chapter will include sections on laser specifications and experimental setup, laser scribing for OSI on superstrate cells and a separate section on the progress of laser scribing on CIGS. The requirements for all OSI laser scribes are the same regardless of material;

Scribe A

- Isolate the front contact
- Suitable morphology for infill with dielectric ink
- No conductive pathways (shorts/shunts) along the edge of the scribe

Scribe B

- Form a low contact resistance interface with conductive ink
- No significant damage to the lower contact (which would cause high series resistance)
- Suitable morphology for infill of conductive ink

P3

- Isolate the back contact
- No significant damage to the front contact (which would cause high series resistance)
- No conductive pathways (shorts/shunts) along the edge of the scribe

3.2 Experimental setup for superstrate cells

3.2.1 Lasers

Laser selection is the most important part of developing an effective scribe process, particularly when layer definition is important. Most industrial thin-film ablation processes use ns lasers as they offer a good compromise between scribe quality and cost [4]. All of the lasers available at M-Solv are solid state, Q-switched ns pulsed lasers operating at IR (~1064nm), green (~532nm) and UV (~355nm), the first, second and third harmonics of the laser gain media used in solid state lasers. All three wavelengths have been used for the development of OSI however the majority of this work has been carried out with IR and green. Table 3.1 lists each of the lasers used during this development and details some of the most important technical specifications. The outputs of all the IR lasers are very similar and for most processes described the lasers are interchangeable. Occasionally one may be selected specifically for a particular feature, such as short pulse duration (IPG) or high pulse energy (SPI, Multiwave), if a parameter was important it will be stated explicitly.

	IR				Green	UV
Manufacturer	*IPG*	*SPI*	*Multiwave*	*Rofin*	*Spectra Physics*	*Coherent*
Model	*YLPM*	*G4S*	*MOPA-DY*	*20E*	*Explorer 2Y*	*Matrix*
Wavelength (nm)	1060	1064	1064	1064	532	355
Pulse duration (ns)	1-10	3-500	10-200	10-50	12	<25
PRF (kHz)	10-600	35-1000	1-500	1-200	1-60	1-100
Max Average Power (W)	18	20	20	20	2	1
Max Pulse Energy (μJ)	60-300	570	600	200	200	20

Table 3.1: Summary of all lasers used for the development of OSI scribes on superstrate cells.

3.2.2 Optical setup

M-Solv have a generic, small scale R&D platform coded MSV101 (101). It is made up of computer controlled 3 axis stages (x,y,z), a granite base and integrated optical breadboard making it easy to customise for any application. The granite is mounted within a laser safe enclosure with access doors to the stages/chuck from the front and the optics from both sides and the rear. Integrated within the enclosure are a monitor and computer for running the stages and other integrated hardware. There are generic 15” rack mounts below the stages to house any controllers or PSUs required for lasers

or other ancillary hardware. CAD models of the base 101 platform can be seen in Figure 3.2.

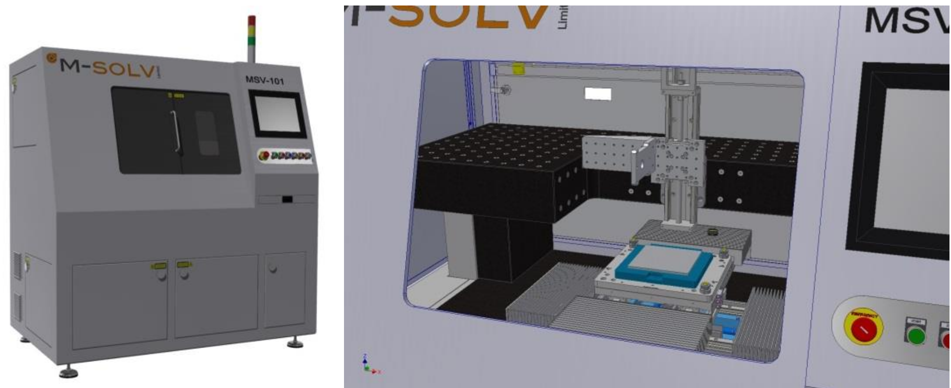


Figure 3.2: An M-Solv MSV101 R&D platform. Left; outside view of laser safe enclosure and integrated monitor. Right; internal view of granite optical breadboard and 3-axis stages.

A 101 was dedicated to development of the OSI process at the start of the project, coded Interconnect Manufacturing Process 101 (IMP101). Two lasers were fitted along with inkjet electronics, two print heads, a camera for alignment/inspection and a fibre fed UV cure lamp. The inkjet side of the setup will be detailed in Chapter 4: Inkjet printing for OSI. For the majority of the project the lasers fitted were the 532nm Spectra Physics Explorer 2Y and the 1μm IPG YLPM. The IR laser was swapped at various points for both the Rofin 20E and the SPI G4 although the optical layout was kept the same. Both lasers were used with fixed optics rather than galvanometer scan heads and scribes were made by moving the substrate on the x,y stages relative to the fixed lenses, the maximum stage speed was 300mm/s. In a number of experiments a 2-8x beam expander made by Linos was placed in the beam path of the IR laser to change the focal spot size. Also, for a number of tests the green laser was imaged through a mask to generate a more uniform energy distribution, this will be discussed in more detail later in the chapter. A schematic of the optical layout within the IMP101 platform can be seen in Figure 3.3. The basic optical setup has two f=100mm plano-convex lenses as the final focusing lenses, anti-reflection (AR) coated for either 1064nm or 532nm.

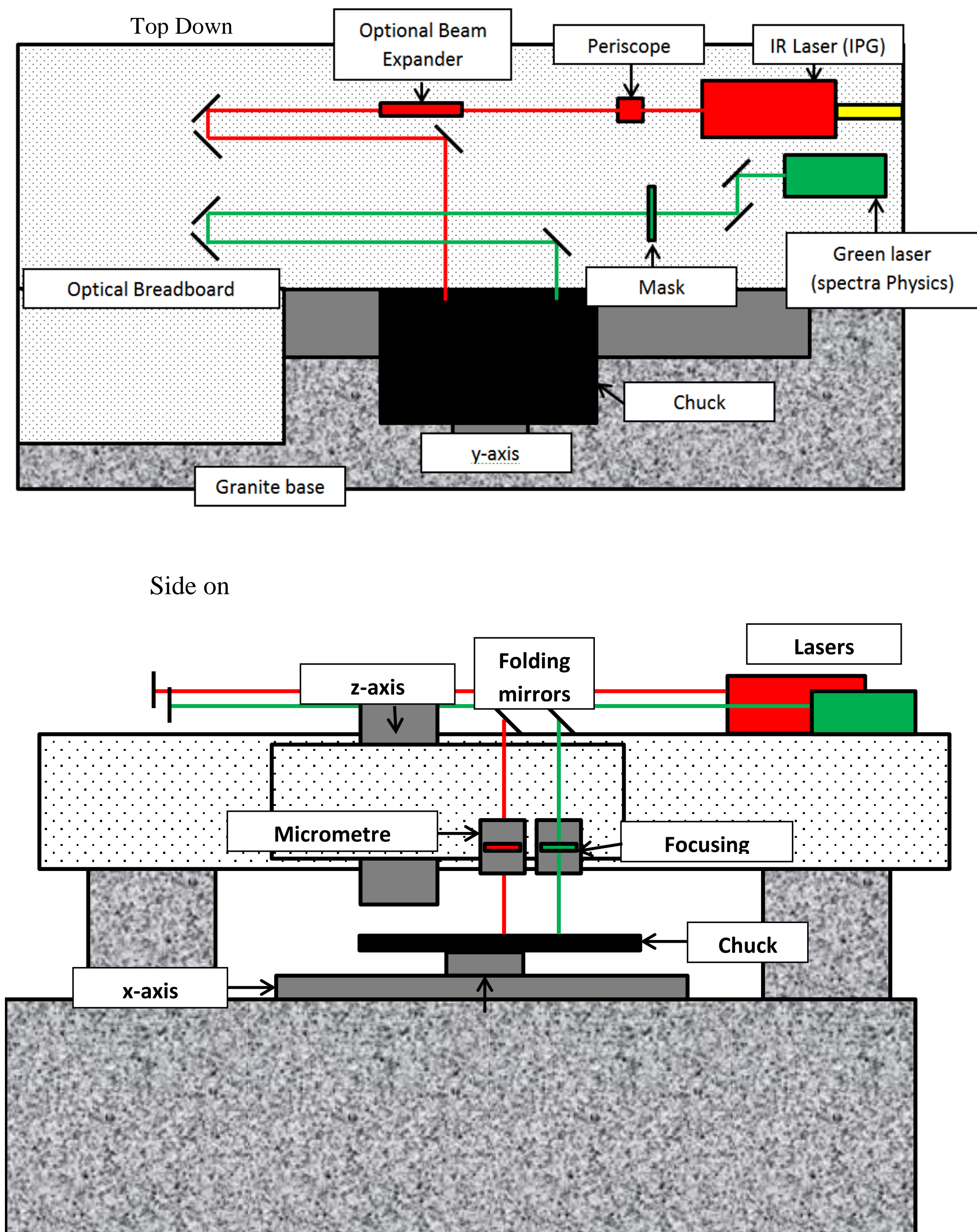


Figure 3.3: (top) top down image of optical breadboard on the IMP101. The two lasers, one green and one IR, feed into separate beam paths. Both have sufficient space for beam conditioning optics before turning mirrors bend the beam down to the substrate. (bottom) front view of the same tool, the two beams are directed through independent focusing lenses mounted on independent, hand controlled, micrometre stage which are, in turn, mounted on a computer controlled z-axis.

3.2.3 Basic procedure for process optimisation

A standard procedure was developed for scribe optimisation on thin film solar materials involving 3 stages; first finding the focal plane in which to operate. In the most basic case this will be the focus of the final lens however for some processes it may be optimal to work out of focus or at the plane at which an image of a mask is formed generating a shaped, uniform beam. Secondly, it is necessary to find the optimum pulse energy for removal of the material. This will be an energy above the ablation threshold of the material to be removed but below the damage threshold of any remaining layers. Lastly, finding the optimum shot overlap for the process, which for a single shot process may require subsequent shots are slightly overlapping to form a continuous scribe. With a normal Gaussian beam this creates a line with scalloped edges, in this case it is possible to identify each laser shot. For some processes it may be optimal to have a high number of shots per area making a straight edged scribe.

In all cases of the following laser development section this methodology is used. A focal scan where a number of lines are separated by 100-300μm was generated each with a different standoff (working distance) of the final lens to the substrate such that it is possible to observe the process through focus. Secondly a ‘power’ scan is run generating a number of lines, separated by 100-300μm, each with a different average power, at a fixed pulse repetition frequency (PRF) equating to a change in pulse energy. It is then possible to monitor the process through the ablation threshold of the layer of interest. Lastly an ‘overlap’ scan is completed again by generating a number of offset lines and either changing the stage speed at a fixed PRF or by changing the PRF while holding the stage speed constant and adjusting the laser diode pump maintain the pulse energy as a constant. This shows what happens to the process as the spot separation is changed. Examples of focal, overlap and power scans can be seen in Figure 3.4, Figure 3.5, Figure 3.6. Developing scribing processes in this way has a further benefit as it is possible to quantify the ‘process window’ i.e. the amount of drift tolerable in the various process parameters, while still maintaining a functional process. This idea is important since it can influence machine specifications, for example the process window with respect to focus can place limits on the accuracy and repeatability of a motorised stage used for a z-axis.

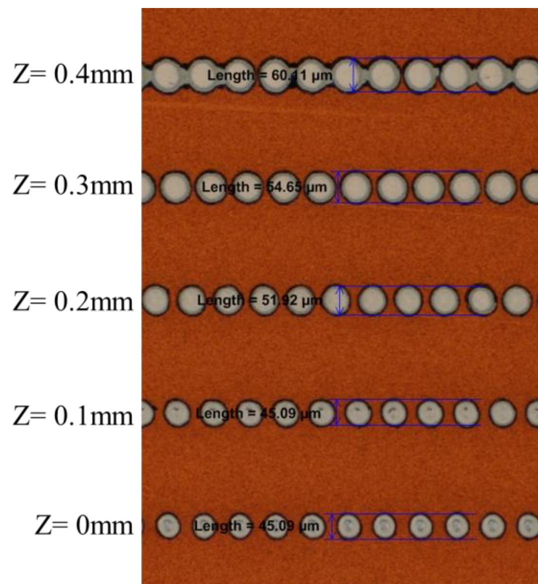


Figure 3.4: An example focal scan, each subsequent line is separated by 100µm in the optical, z-axis. The focus of the lens is the last line and is defined as z = 0mm. As the working distance moves farther from focus the spot becomes larger.

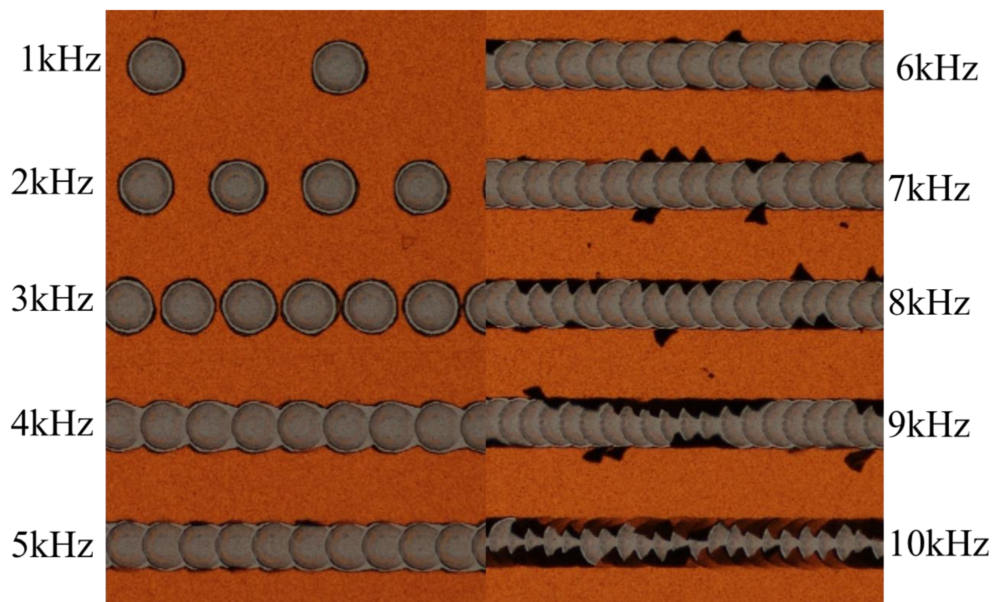


Figure 3.5: An example overlap scan, each subsequent line is an increase of 1kHz to the laser PRF. The beam translation velocity is held constant at 300mm/s and the pulse energy constant at ~22µJ.

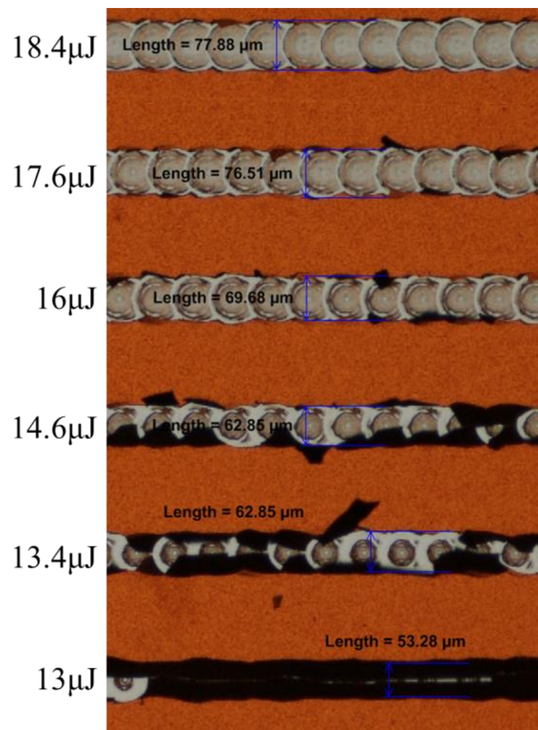


Figure 3.6: An example power scan. Each subsequent line is at increasing pulse energy. The pulse energy step size is small and marked on the image. Threshold is approximately 16-18μJ as that is the enrgy at which the semiconductor is completely removed without damaging the layer below.

3.3 Thin-film Silicon

Samples of thin-film silicon solar panels were obtained for process development from a potential customer of M-Solv. The initial material received was a tandem cell consisting of an aluminium zinc oxide (AZO) transparent conductive oxide (TCO) for the front contact, an absorber layer consisting of both microcrystalline silicon (μc-Si) and amorphous silicon (a-Si) and a silver back contact. Part way through the development process the test samples were switched to a triple junction material thought to contain two layers of μc-Si with different band gaps and one layer of a-Si. The TCO and back contact in the triple junction remained the same material however the thicknesses were changed. Approximate thicknesses for the tandem material were determined using a Zygo new view 200 scanning white light interferometer (SWLI). The thicknesses were 360nm AZO, 2.6μm μc/a-Si and 300nm silver.

3.3.1 TF-Si 1064nm, film side processing

The industry standard approach for Scribe B is to use a green laser incident through the glass however from a machine builder/integrator view point it would be preferable to use an IR fibre laser, like the SPI G4, from the coating side for these processes. This is for two reasons, firstly IR fibre lasers offer a very low cost per Watt, ~£400/Watt of laser power, and are therefore more economical than green DPSS lasers, ~£7,000/Watt, even if the power required for the process is much higher. Secondly having both the laser and inkjet incident from the film side would make it possible to physically align the laser and inkjet on a single head. Therefore the starting point for laser process development was an IR laser, incident from the film side.

Using an IR laser it was possible to process the tandem TF-Si. Processes for both A and B were found at PRF = 40kHz and beam speed = 200mm/s. The pulse energies were 59μJ, for a 28μm A scribe and 20μJ for a 17μm B scribe, higher pulse energies resulted in glass cracking. Although both scribes were to the correct depth neither had suitable morphology for inkjet printing. Scribing from the film side was found to produce ridges, or burrs, of up to 1μm in height along the edge of the scribe. Later it was found that the insulating ink gets stuck in these burrs increasing the height, this morphology creates pinch points for the conductive ink resulting in areas of thin metal and high series resistance.

The formation of burrs is due to the photo-thermal ablation mechanism which occurs when the photon energy is less than the dissociation energy of the bonds within the material, typically 3.5-6.4eV [9], at wavelengths below ~355nm. Photo-thermal ablation is ablation via the conversion of incident light into heat and is characterised by material being melted, vaporised and ejected from the surface. The ejected plume creates a recoil pressure on the molten material, which forces material outwards creating the burrs at the edge of the scribe line [9], see Figure 3.7. Figure 3.8 shows an SEM and a Scanning White Light Interferometer (SWLI) profile of the film side scribes produced with the IR laser on the tandem TF-Si material, the burrs are visible along the edge of the scribe.

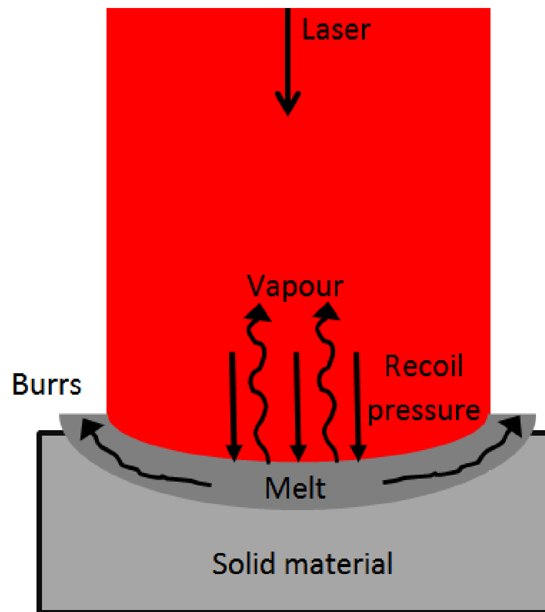


Figure 3.7: Formation of burrs during photo-thermal material ablation. As material is vapourised the recoil pressure forces melted material outwards towards the edge of the scribes where it is recast into burrs.

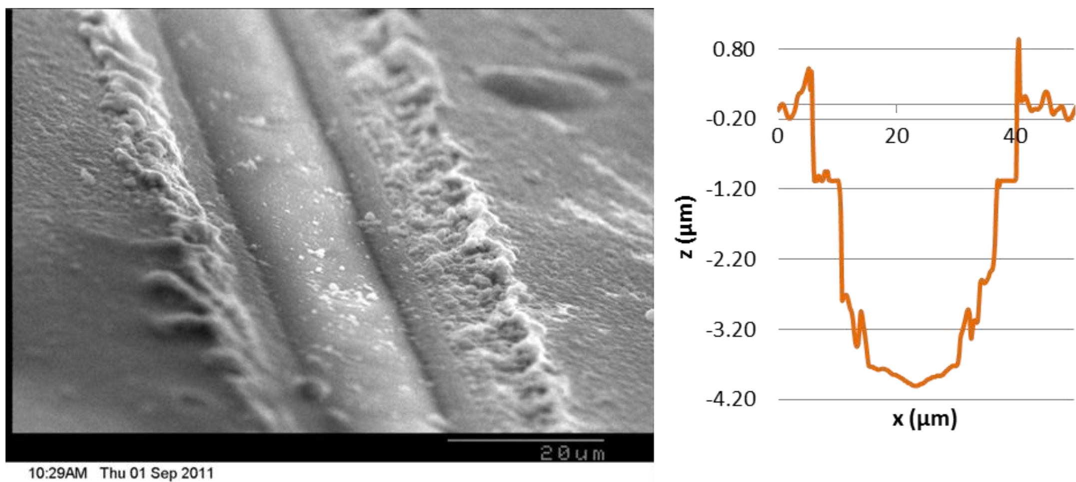


Figure 3.8: Left; SEM of an A scribe made with the Rofin 1064nm laser incident from the film side. Right; An SWLI plot of the same scribe showing the burrs extend more than 800nm above the surface. The scribe was made in the focus of an f=100mm singlet plano-convex lens with a PRF of 40kHz, beam speed of 200mm/s and pulse energy of 59µJ.

It was theorised that a homogenous intensity distribution would reduce the gradient in recoil pressure over the scribe area and thus reduce burr formation. After initially investigating many different ways to achieve a homogenous energy distribution including imaging a mask or square core fibre, bi-prisms, diffractive optical elements (DOEs) and µ-lens arrays, it was decided that mask imaging was the quickest, easiest and most economical for a quick test. The mask imaging setup consists of a 585µm square mask and an f = 100mm lens. The mask is over filled by the laser resulting in a

loss of around 60% of the initial output power but resulting in a more even energy distribution, closer to a top-hat than a Gaussian. A beam profiler wasn't available to verify the energy profile at this time but later in the project a similar imaging setup was used and a beam profile taken, this can be seen in Figure 3.16.

The mask was ~1m back from the lens. It can be calculated using Equation 3.1 that this system has a de-magnification of 0.11 and, therefore, an expected beam size of 65μm on the work piece. From the equation for a thin-lens it can be calculated that the image is formed ~111mm away from lens. A schematic of this mask imaging setup can be seen in Figure 3.9. The results of ablation using the mask image can be seen in Figure 3.10, although the edges are now steeper the burr has in fact increased up to 1.4μm in height.

(3.1) $$M = \frac{f}{f - d_o} = \frac{-d_i}{d_o}$$

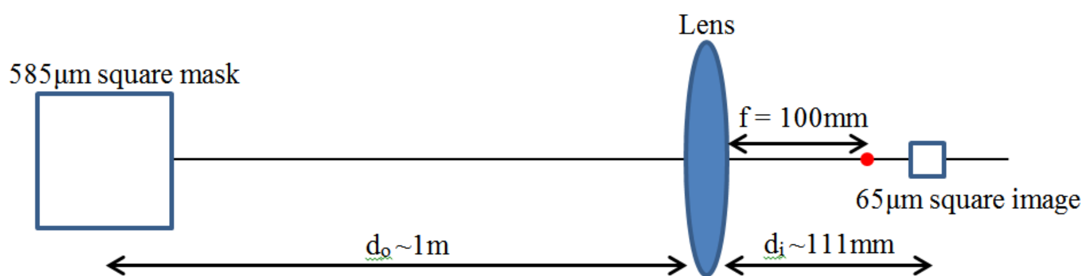


Figure 3.9: A schematic of the mask imaging system used to generate a square top-hat beam. The collimated laser beam over-fills the mask giving a more uniform energy distribution. This imaging system formed an ~65μm square at the work piece.

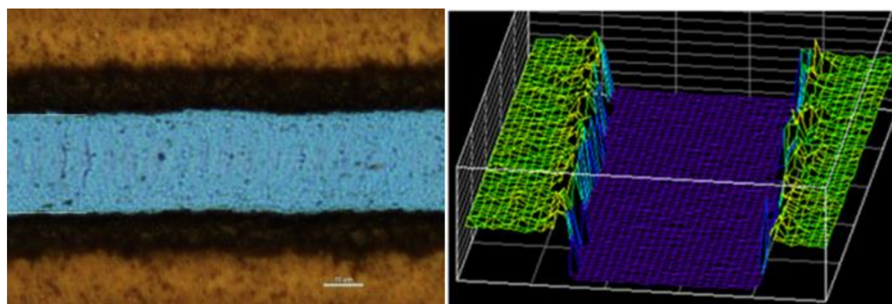


Figure 3.10: High overlap, IR, film side scribing imaging the square mask, left optical image, right 3D plot generated using the Zygo SWLI. The scribe edges are steep and the depth uniform however the burrs remain along the edges up to 1.4μm in height.

Pulse duration was found to have a small effect on creation of burrs with shorter pulse durations tending to create less burr, however the IPG laser capable of running at 1, 5 and 10ns couldn't produce a high enough pulse energy at 1ns or 5ns to remove the material even with significant overlap. Therefore 10ns was selected as the optimum duration however at 10ns the burr still averaged 0.5-0.7µm, this is still an unacceptable process. From these experiments it was concluded that a film side process with suitable scribe morphology was not possible with IR nano-second lasers. It was therefore decided to relax the requirements based on machine architecture and switch to a through the glass process.

3.3.2 TF-Si 1064nm, through the glass processing

Glass side scribing has many benefits, as presented in [10], including better scribe morphology and lower energy requirements resulting from the photo-mechanical mechanism. The glass substrate and TCO are almost completely transparent to the green laser so when the laser light is incident through the glass all the energy is deposited at the interface between layers [4]. This results in a localized vaporisation of material which creates a region of high pressure and mechanical strain. The material then fractures along grain boundaries and the stack is explosively ejected [10] resulting in very clean ablation with little TCO damage. Such glass side scribing is routinely used in industry to make the standard interconnect however it is usual to use a green laser to remove the semiconductor as it is transmitted by the TCO and absorbed strongly by the semiconductor [4], see Figure 3.11. There is some evidence that the P2 and P3 processes can be completed with an IR laser however the results are dependent on the exact material form of TF-Si with a-Si showing poor results but µc-Si having an acceptable process [11].

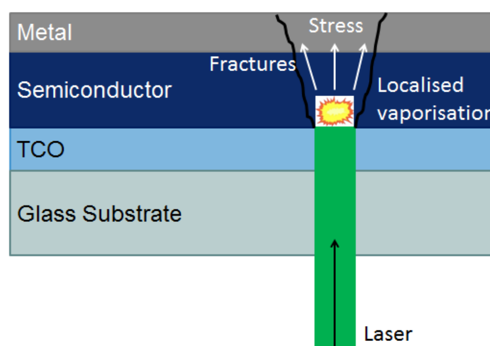


Figure 3.11: A green laser incident through the substrate is transmitted by both the glass and the TCO and is absorbed, largely, by the semiconductor. This causes a localised vaporisation and a corresponding pressure build up along the interface. This causes mechanical stress between layers which leads to the above layers fracturing along grain boundaries and being ejected from the surface.

Testing the IR Multiwave laser at, 10ns, incident from the glass side originally appeared to be promising. It was possible to find processes for both scribes A and B. The fluence was reduced from 25 J/cm^2 and 4 J/cm^2 for scribes A and B respectively to 2 J/cm^2 and 0.9 J/cm^2 a factor of 12.5 and 5 respectively compared with film side ablation. A second benefit of the glass side IR processing was that, as expected, no burr was observed. A new problem however was found; the back contact delaminated away from the semiconductor stack, this problem intensified as the overlap was increased. Optical images of the early glass side IR results can be seen in Figure 3.12, delamination is visible as black strands of material along the edge of the scribes. The delaminated metal appears black since it is reflecting light away from the microscope objective.

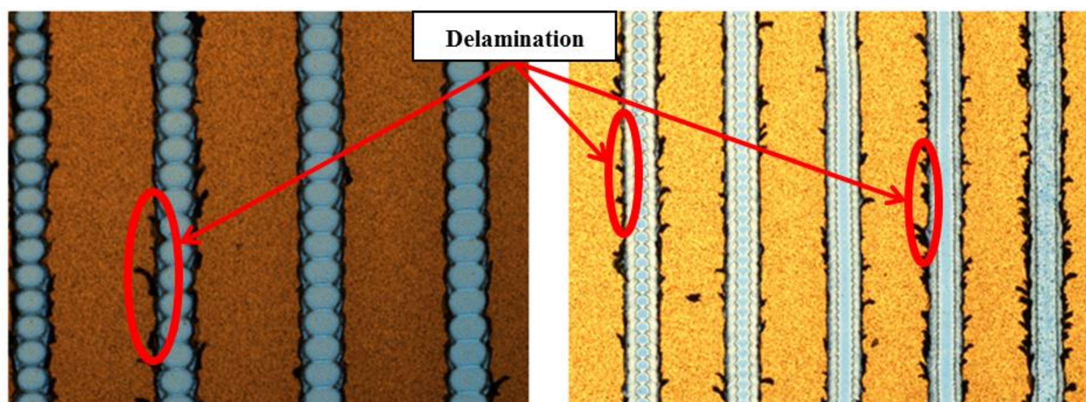


Figure 3.12: IR scribes with the Multiwave laser through the glass. Left; 50kHz, 3.5m/s, increasing laser pump current left to right 50-65%. Right; 10ns, 50kHz, 95% current, 2.5-0.5m/s.

Despite these promising results the customer supplying the samples suggested that using an IR laser through the glass results in shunting of the cell, unsurprising since it is known that some TF-Si configurations are shunted by IR lasers [11]. A quick test was devised to confirm the effect.

The resistances of working, standard interconnects supplied from the manufacturer were measured in the dark. An IR, glass side scribe A was then added adjacent to the interconnect and the resistance re-measured. Figure 3.13 shows the one diode

equivalent circuit diagram of a solar cell with the current path of the measurement in the dark marked in red. By making the measurement with the probe voltage reverse biasing the diode the only current flow is through the two resistors. For a working interconnect the series resistance (R_s) is of the order of a few Ω's and the shunt resistance (R_{sh}) is of the order of 10-100's kΩs therefore the measurement is an approximation of the shunt resistance. Adding the adjacent scribe A is the equivalent of adding a second R_{sh} resistor in parallel. Therefore if the resistance drops significantly it can be assumed that the A scribe is shunting.

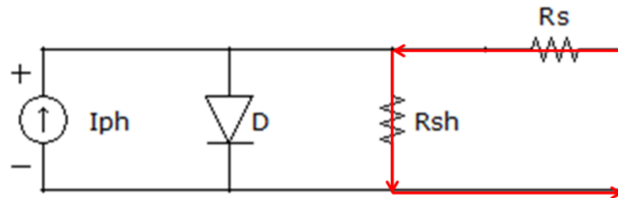


Figure 3.13: The one diode equivalent circuit diagram of a solar cell. The red lines show the current path of a resistance measurement taken in the dark.

This test was completed for both the glass and film side TCO scribe A's and it was found that the IR film side process decreased the resistance from >100 kΩ down to <2kΩ indicating that the process does indeed cause shunting. It is thought that the reduction in shunt resistance due to the film side processing is related to the heat affected zone (HAZ) of the IR laser. A-Si [12] has been shown to recrystallize at temperatures as low as 150°C if the outlying areas are being heated by the HAZ it is possible that the silicon is crystallizing into a more conductive form along the scribe walls introducing a shunt. The approach has therefore been switched to a 532nm through the glass process, similar to that used in industry.

3.3.3 TF-Si 532nm, through the glass processing

Quick tests into film side scribing with the green (532nm), Spectra Physics, laser showed the same morphology, with comparable burr heights as the film side IR scribes. This is expected since the ablation mechanism is still photo-thermal. It has also been shown that film side 532nm scribing of TF-Si results in significant shunting of the cells [13]. Using the green laser for glass side scribing created excellent scribe morphology, with clean edges, free of melt. The initial scribes show some discolouration of the TCO in the centre of the scribe, see Figure 3.14. Scanning White Light Interferometer (SWLI) measurements show a reduction in surface roughness on these discoloured

regions. The TCOs in TF cells are often purposely roughened to scatter light into the semiconductor [14]. The removal of this rough surface is likely due to melting and recasting of the TCO in the centre of the scribes where the laser intensities are highest. A similar reduction in TCO roughness at the centre of the laser pulse has been noted in literature with a 532nm laser incident on a TF-Si stack [13]. Although the effect didn't appear to reduce the cell performance it was decided to try and remove it in the case of OSI, the smoother texture could be brought back at a later date to test the effect.

In order to remove this change in TCO morphology the same mask imaging used previously in the IR beamline system was installed in the green beamline. Increasing the uniformity of the laser profile removed the TCO discolouration; Figure 3.14 shows both Gaussian scribes and those made by imaging a square mask.

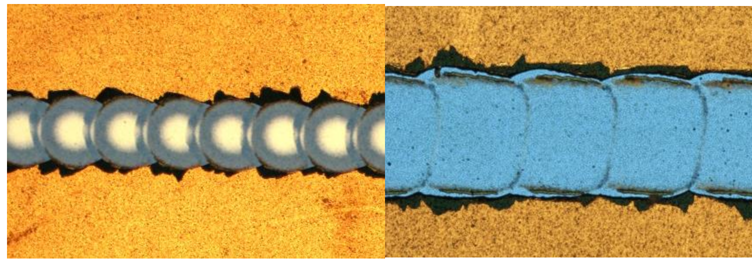


Figure 3.14: Processing through the glass with a green laser having different beam profiles. Left is a scribe made with a Gaussian beam, right is one made with a square top hat. The more uniform energy distribution of the top-hat beams removes the discolouration in the centre of the TCO caused by melting and recasting the TCO into a smoother surface finish.

The back contact delamination observed in the IR glass side scribes is still present in the green scribes even with imaged spots. After searching through the literature it was found that the delamination of the back contact in silicon solar cells with glass side scribing had been documented [11], [15]. Discussed in detail in Chapter 2, a criterion for 'flakeless ablation' was developed stating that the angle, Equation 2.2, between subsequent spots must be greater than 90°. Equivalent to low shot overlap with circular spots. The back contact delamination in these scribes was found to decrease at lower shot overlaps, following the literature criteria, but was not completely removed. Figure 3.15 shows an SEM imaging of a delaminated scribe made with the green laser incident through the glass, with the square mask and a low shot overlap. It can be seen that the delamination is caused by the silver back contact peeling away rather than fracturing. The a-Si is still attached and shows signs of melting where the laser interacts.

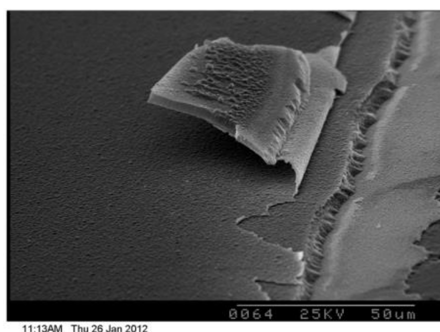


Figure 3.15: An SEM micrograph of a green scribe on amorphous silicon. The green laser is incident through the glass and the energy distribution is made homogenous by imaging a square mask. A delaminated piece of back contact and semiconductor can be seen at the scribe edge.

Discussions with the material supplier revealed that they do not see this problem with their P3 laser process which also used a 532nm laser incident through the glass. In order to find out whether the delamination was a problem with this laser process or specific to these samples one was sent back to the customer for processing with their standard P3 process. Delamination was observed indicating that the problem is caused by the sample shipping and/or handling. It was suggested that adsorption of moisture between layers may modify the adhesion resulting in the delaminated scribes.

The standard test of layer adhesion is the ISO 2409 cross hatch tape test, often used for paints and varnishes. The test involves scratching a cross hatch pattern into the coating then subsequently applying and removing tape to the scratched area in a controlled manner. The level of removal is then compared on a scale from 0 to 5 with 0 being the worst, >65% of coating removed and 5 being the best, 0% of coating removed. The initial result on the samples which flake when laser processed was 0 on the ISO scale indicating that greater than 65% of the back contact had been removed. Implementation of new shipping practices; the samples were sealed in a nitrogen atmosphere and a desiccant was included, they were also annealed for an hour at 150°C before any processing to drive out moisture. Repeating the cross hatch test resulted in a score of 2, not greater than 5% of back contact removed indicating that the adhesion has been greatly improved.

The imaging setup was switched to a circular mask of 750μm giving a spot on the work piece of ~82μm. A Haas Beam Waist Analyser Camera (BWA-CAM™) beam profiler was lent to M-Solv for evaluation. It uses integrated filters to image high energy density beams, close to focus, with a standard CCD detector. A beam profile and intensity plots of the major and minor axis from the working distance of the imaging

system can be seen in Figure 3.16. It can be seen that the energy distribution has much steeper sides and a flatter top than a Guassian beam.

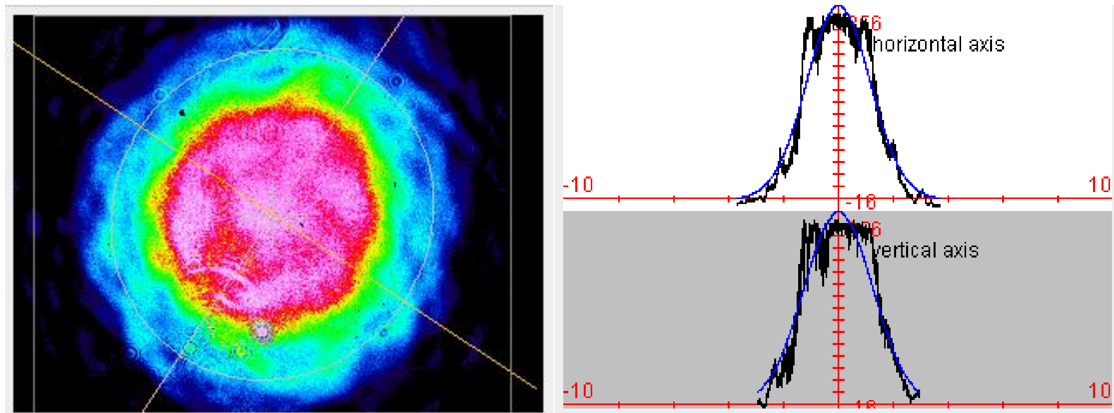


Figure 3.16: beam profile captured from the image plane of the optical system. The intensity profile is flat across the majority of the beam. The profile was taken with a HAAS BA-CAM laser profiler.

Using the circular mask imaging system in combination with the green laser, incident through the glass resulted in B scribes with excellent morphology. Figure 3.17 (right) shows the elimination of the back contact delamination attributed to the new sample shipping and handling procedures compared to the samples shipped without these precautions Figure 3.17 (left).

Figure 3.17: Circular mask imaging with the green laser incident through the glass. Left; Without the new sample handling procedures. Right; the new sample handling procedures increase layer adhesion and remove delamination when scribing.

At this point the customer started supplying their new cell structure, a triple junction TF-Si material, where the thicknesses of each layer were approximately 1μm AZO, 2.5μm silicon layers and 0.5μm of silver back contact. The same approach with a green laser through the glass worked well for the B scribe and the new sample shipping and handling procedures still produced excellent scribes free from delamination.

The remaining process was to develop the A scribe which removes all layers. Since the TCO is almost completely transparent at 532nm, using the large, imaged scribes and the

low shot overlap, required to obtain flake-free ablation, even at the maximum pulse energy of the green laser it is not possible to remove the TCO. It was decided to use the green laser to make a B scribe and follow behind with the IR laser to take off the TCO within the B in a two-stage process. The advantage of this is that there is no need to develop a new process as it is possible to combine the already developed B scribe with the existing P1 process routinely used in industry. It was relatively easy to align the two beams by adjusting the final mirror of the IR laser to bring it in line with the green, a number of iterations of scribing with both lasers, inspection with the on-tool camera and adjusting the mirror achieved alignments within a few microns of one another. Figure 3.18 shows the developed interconnect scribes. The process parameters for the developed scribes are shown in Table 3.2.

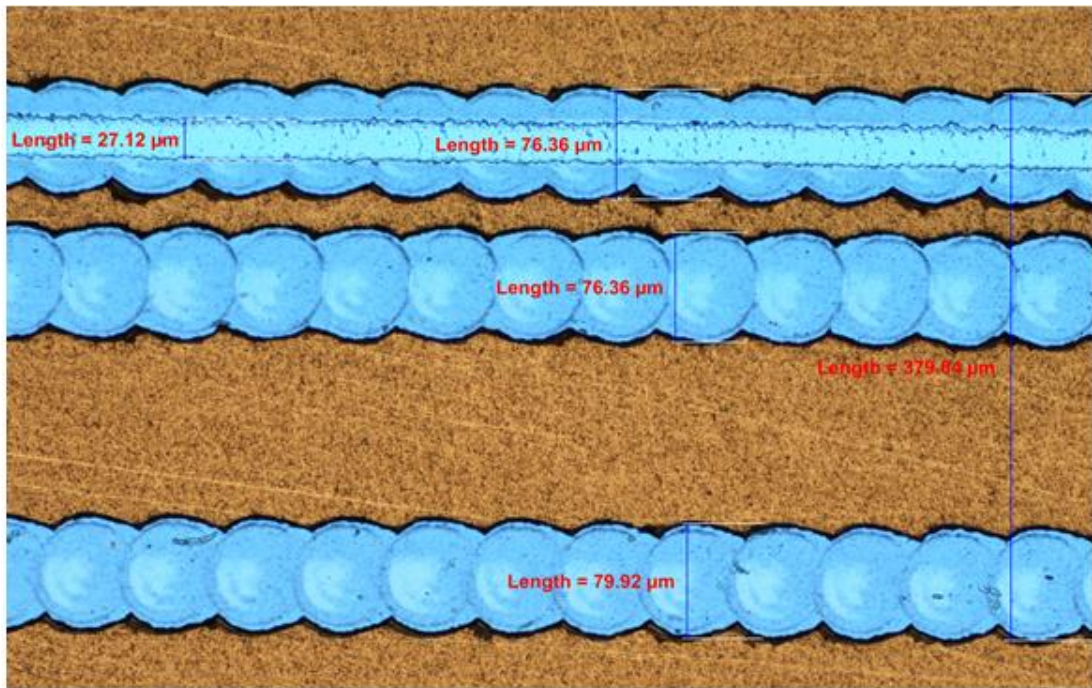


Figure 3.18: An optical micrograph of interconnect all three interconnect scribes (from the top scribes A, B, P3). The scribes were made in two steps; first three sets of scribe B were completed with the green laser through the glass, second an IR laser incident through the glass removed the TCO in scribe A.

Process step	Parameter	Value
Laser - A scribe	Wavelength (nm)	1064
	Fluence (J/cm^2)	8.40
	Spot diameter (µm)	27
	Pulse duration (ns)	10
	Pitch (µm)	10
	Optical setup	Focused Gaussian beam
Laser -B scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	0.42
	Spot diameter (µm)	76.5
	Pulse duration (ns)	<12
	Pitch (µm)	60
	Optical setup	Imaging 750um mask

Table 3.2: Laser parameters for the developed OSI scribes on a-Si

3.4 Electrical verification of laser processes on TF-Si

Solar cells are fundamentally functional, electrical devices therefore laser process optimisation via visual inspection does not ensure a fully functional process. Furthermore thermal processes such as the annealing step to remove moisture may not produce any visible changes however they have the potential to fundamentally alter material characteristics through the migration of dopants or incorporation of oxygen. It is therefore essential to have a method for the measurement of the electrical impact of any process.

3.4.1 Measuring cell performance using a solar simulator

There are standard methods for the measurement of solar cell performance. A solar simulator, as the name suggests, is a light source that mimics solar irradiance both in spectrum and intensity. By illuminating the cell to be tested with the solar simulator and varying the load applied to the cell it is possible to generate a current against voltage curve (I/V curve). From this it is possible to extract cell characteristics such as open circuit voltage (V_{oc}), short circuit current or current density (I_{sc}/J_{sc}), fill factor (FF)

and efficiency (η). V_{oc} and I_{sc}/J_{sc} are fundamental material properties. V_{oc} is a function of the absorbing semiconductors bandgap and recombination pathways. I_{sc} is dependent on carrier density and diffusion length as well as illumination; J_{sc} is I_{sc} per unit area, usually cm^2. FF is the ratio of the power of a solar cell at its max power point (mpp) to the product of V_{oc} and I_{sc}, it can also be thought of as the 'squareness' of the I/V curve. Fundamentally FF is effected by the diode quality and recombination mechanisms within the cell, FF can also however be affected by the introduction of shunt and series resistances an equivalent circuit diagram of a solar cell can be seen in Figure 3.19. The internal cell shunt and series resistances are marked as R_{CSh} and R_{CSer} with the extra shunt and series resistances from the interconnect marked as R_{ISh} and R_{ISer}. Shunt resistance and therefore fill factor are the parameter most sensitive to problems with the laser processes which may introduce extra shunt paths along the side-walls of scribes. Figure 3.19 also shows the possible location of shunts produced by a non-optimal laser process. Finally η is the ratio of the optical power incident on the cell (P_{in}) to the electrical power out, expressed as a percentage and is the most commonly quoted cell characteristic as it is a combination of the other three, Equation 3.1.

(3.2) $$\eta = \frac{V_{OC} I_{sc} FF}{P_{in}}$$

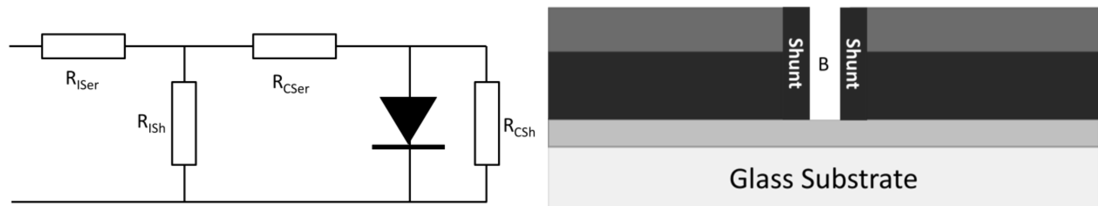


Figure 3.19: Left; an equivalent circuit diagram of a solar cell. The cell itself is represented by the diode while the internal shunt and series resistances are given by R_{CSh} and R_{CSer}. Extra shunt and series resistances will affect FF and may be introduced by a poorly optimised interconnect, these extra resistances are represented by R_{ISh} and R_{ISer}. Right; a diagram showing the location of possible conductive pathways introduced by a poor laser scribe, these pathways decrease the shunt resistance and therefore the fill factor.

The standardisation of solar cell measurements can be the topic of entire conferences however presented here is a brief overview. Cell measurements are sensitive to a number of different variables related to the illumination; the most commonly controlled are spectrum, spatial uniformity and temporal stability. Solar simulators are specified on a scale from A to C in each of the three categories with A being the highest. The

spectrum of the light reaching us from the sun is approximately a black body with a temperature of 5800K but on the earth it is modified by absorption processes within the atmosphere. The Air Mass coefficient (AM) is a way of quantifying the attenuation of the spectrum due to the atmosphere. AM0 is the spectrum in space and is used for characterisation of solar cells for space applications. AM1 is the spectrum generated when the sun is directly overhead however the spectrum most commonly used for measurement of terrestrial solar is AM1.5, which is an average spectrum for a mid-latitude location over the course of a year. It is worth noting that there are significant variations depending on time of day and year as well as location. Figure 3.20 shows AM0 and AM1.5 spectra compared with a 5800K black body normalised with total power density of 1366W/m^2 and 1000W/m^2 respectively [16]. When a solar simulators spectrum is specified in 100nm intervals from 400-1100nm, there are specified percentages of the total output that must lie within that interval. A summary of the three specifications on which a solar simulator is rated can be seen in Table 3.3. Spatial non-uniformity and temporal instability relate to the power output of the solar simulator over the illuminated area and over time.

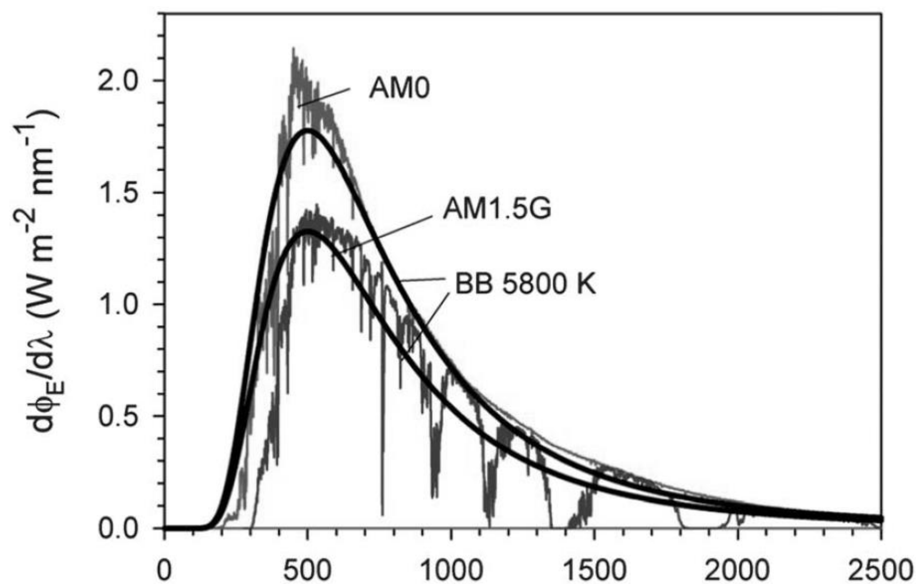


Figure 3.20: The AM0 and AM 1.5 solar spectrums compared to a black body normalised to the same optical intensity. AM1.5 is the spectrum most commonly used for the qualification of terrestrial solar cells and is the average for a mid-latitude location over the course of a year [16].

Classification	Spectral Match (each interval)	Irradiance Spatial Non-Uniformity	Temporal Instability
Class A	0.75–1.25	2%	2%
Class B	0.6–1.4	5%	5%
Class C	0.4–2.0	10%	10%

Table 3.3: A summary of the criteria on which solar simulators are specified.

A second hand Newport Oriel Class ABA simulator was purchased by M-Solv for this project. The system consists of the Newport Oriel light source with homogenising optics and controllers, a chamber for holding the cells and a Keithley 2400 source meter connected to a PC for extracting I/V data. Figure 3.21 is a labelled image of the solar simulator. The cell temperature must also be controlled for repeatable, accurate performance measurements. Each cell material has an intrinsic temperature coefficient which characterises how much the PV performance degrades per 1° temperature increase. The temperature co-efficient is dependent on the type of semiconductor, in the case of multi junction a-Si efficiency is reduced by ~0.48%/°C [17]. Inside the chamber which holds the cell to be tested is a water cooled chuck connected to a chiller for maintaining cell temperature at 25°C during measurement.

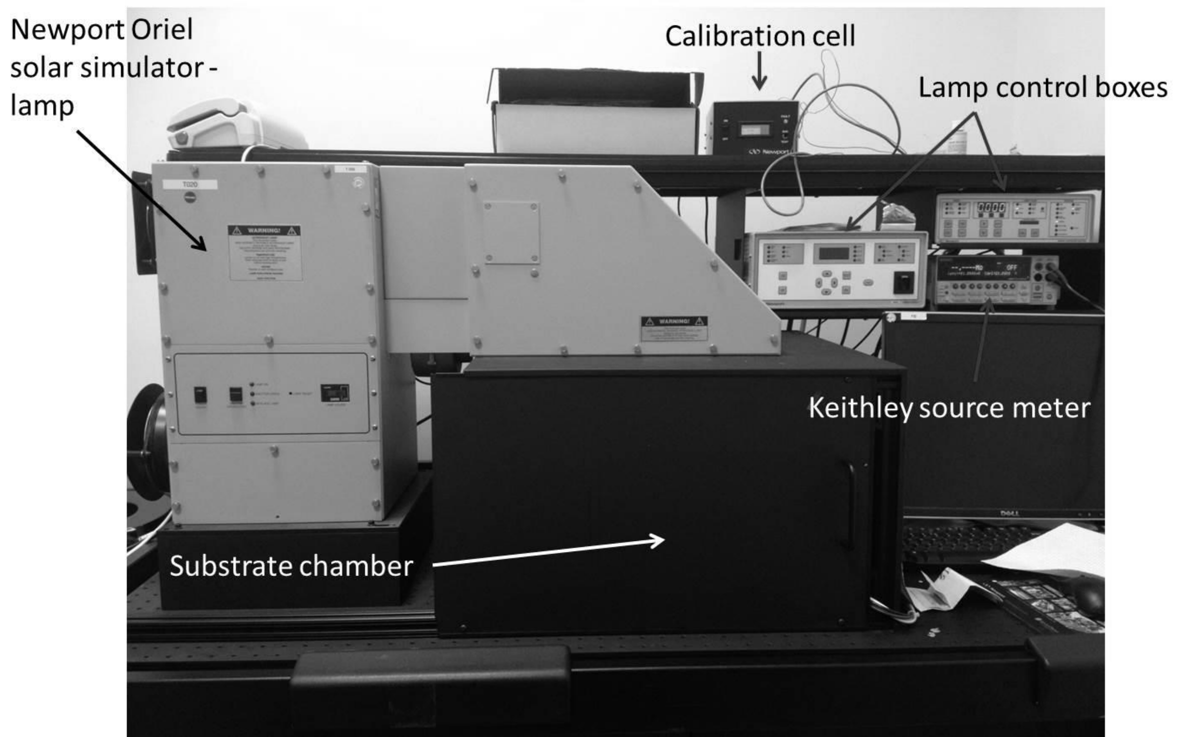


Figure 3.21: Image showing the key components of the solar simulator purchased for this project. It consists of a Newport Oriel light source with controllers, Keithley 2400 source meter and substrate enclosure.

The solar materials used in this project are not supplied with performance data, it is therefore necessary to make comparative measurements with respect to a suitable control, either a measurement of the same material before processing or measurement of similar material at the same time. In this way it is possible to see relative changes brought about by the developed processes without prior knowledge of absolute performance.

Spectral match is dependent on the type of bulb used within the illumination which is constant for all measurements, therefore when considering the error associated with relative measurements spectral match error can be ignored as long as the control has the same spectral response, i.e. is the same type of material. Temporal stability of the lamp is specified to be +/-2% and will be dependent on the electronics control of the lamp, it therefore should be the same as specified. Spatial uniformity of the illumination is dependent on the alignment of homogenising optics within the lamp and could therefore change over time and be adversely affected by shipping and handling. It was therefore decided to quantify the spatial non-uniformity error of the lamp in-situ.

A calibrated reference cell made of crystalline silicon was supplied with the simulator, this was used to check the spatial uniformity by moving it in 2cm intervals in a 5x5 grid across an $8cm^2$ illuminated area. It was found that the illumination intensity was greatest in the centre of the lamp and dropped off in all directions. The greatest total deviation from the centre was 5.4%, a plot of the lamp intensity over the field can be seen in Figure 3.22. Adjusting the values at each point to be a percentage difference from the mean value yielded a variation of +3.4%/-2.0%, within the simulator specification of +/-5%. A 2D heat map of the percentage difference from the mean value can be seen in Figure 3.23.

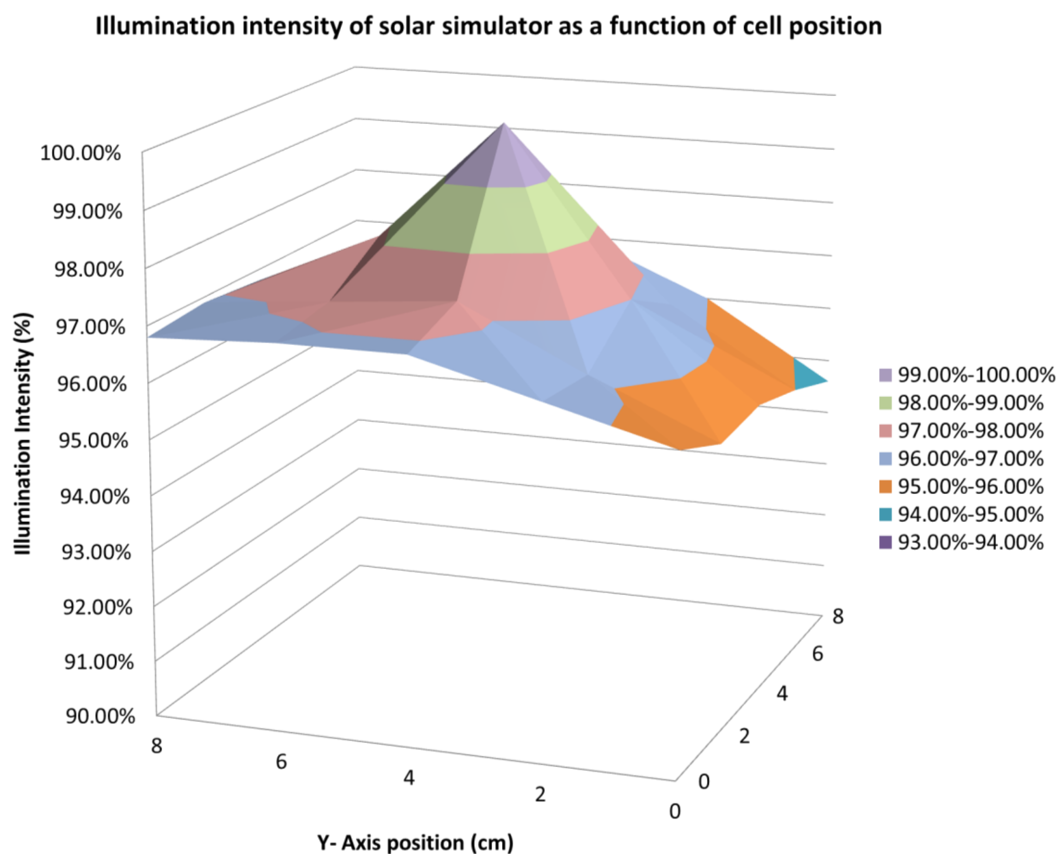


Figure 3.22: A plot of illumination intensity of Newport Oriel solar imsulator as a cuntion of cell popsition as measured with a crystalline silicon reference cell.

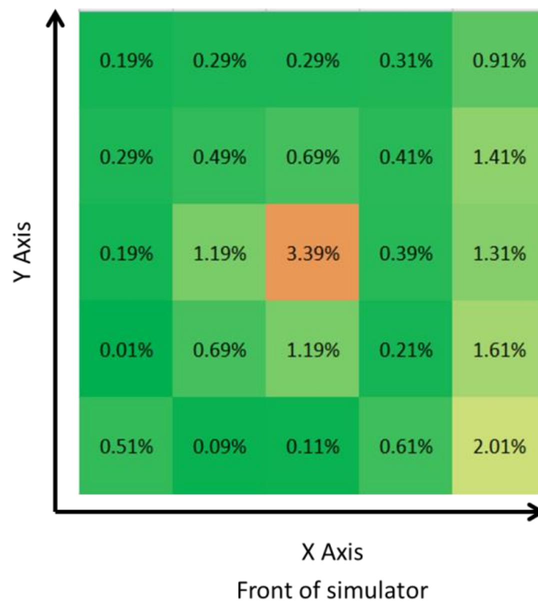


Figure 3.23: A 2D heat map of the difference in intensity measurements from the mean recorded value.

The final potential source of error is temperature drift during measurements. A sequence of measurements was made while measuring the thermo-couple included in the packaged reference cell. The maximum temperature increase after a 2 minute measurement cycle, approximately 12 measurements in quick succession, was found to be ~1°C with the cell mounted on the chiller plate. The maximum increase in a single, 9 second measurement was found to be <0.4°C. It took around 30s for the temperature to settle back to the initial value after the single measurement. The impact on cell efficiency of this temperature rise will be material dependant, example temperature coefficients of the materials used within this work are multi junction a-Si: -0.48%/°C, CdTe: -0.21%/°C, CIGS: -0.36%/°C [17].

3.4.2 Impact of anneal on TF-Si performance

It has been shown above that in order to successfully scribe this TF-Si stack a pre-process anneal is required. Although annealing these samples does not bring about a visible change it is possible that heating may fundamentally alter the solar cell material either by migration of dopants, incorporation of oxygen or changes in crystallinity. It is therefore just as important to qualify this pre-scribe anneal process as the scribe itself.

A test was devised to check the annealing process did not negatively impact the photovoltaic properties of the material. A single sample was split into four pieces, one reference piece was kept at room temperature as a control, the other 3 pieces were

annealed for 1, 2 and 3 hours respectively at 150°C. All four samples had the I/V curves extracted using the solar simulator. All four key performance parameters; η, FF, V_{oc} and Isc were recorded from each cell of each sample; three measurements per sample. The results can be seen in Figure 3.24. The initial anneal improves voltage and fill factor with a corresponding increase in efficiency despite a slightly degraded current output. It has been shown that a 1 hour anneal at 150°C is sufficient to allow scribing and it also appears to improve the material quality with an efficiency improvement of ~1% absolute. A 1 hour anneal was therefore chosen as the baseline process.

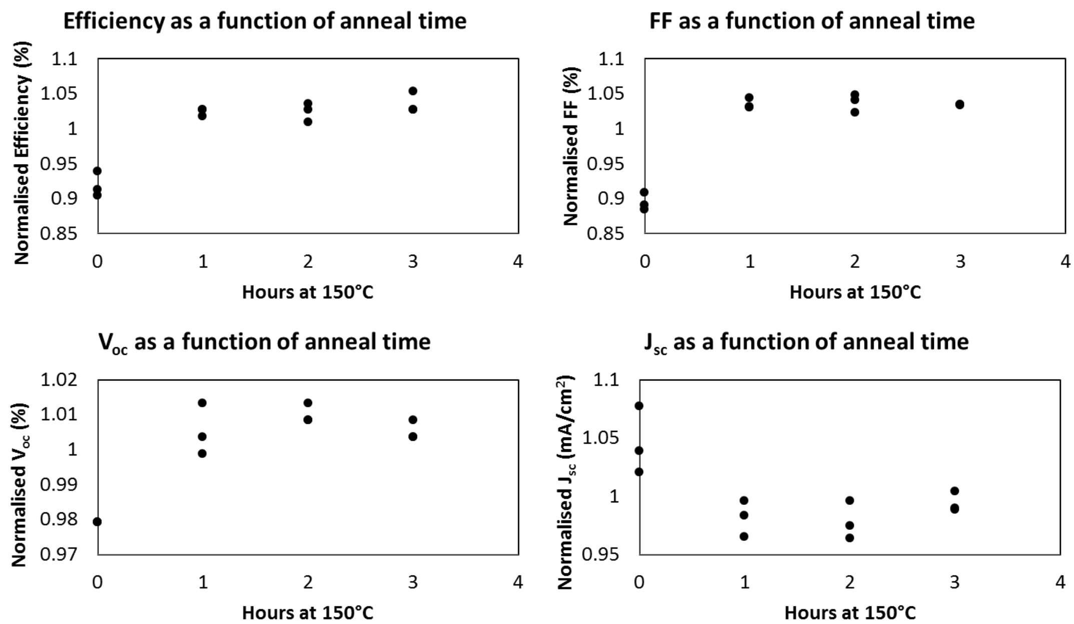


Figure 3.24: A comparison of the four key performance indicators for solar cells against anneal time at 150°C for the triple junction a-Si material. From top left to bottom right; efficiency, fill factor, open circuit voltage and short circuit current.

3.1.5.3 Impact of scribes on cell performance

Scribe B for the OSI process is identical to the P3 scribe for isolating the back contact in the standard process, since the P3 scribe simply defines the edge of the interconnect adding a second one should not have any negative impact on electrical performance of the cell, other than slightly reducing cell active area. In order to remove this effect current density, J_{sc} mA/cm^2, was compared rather than current. However, if the scribe is introducing unwanted electrical issues, such as shunting between the front and back contact via melted material on the scribe wall, the FF will be affected. The Scribe B

parameters from Table 3.2 were tested by adding a second P3 scribe to half of a new mini module (4 out of 7 cells) and comparing the performance of the altered cells to the unaltered ones. Figure 3.25 shows the comparison between the control cells and those cells with extra B scribes, it can be seen that the performance of both altered and unaltered cells is comparable and therefore scribe B has been verified.

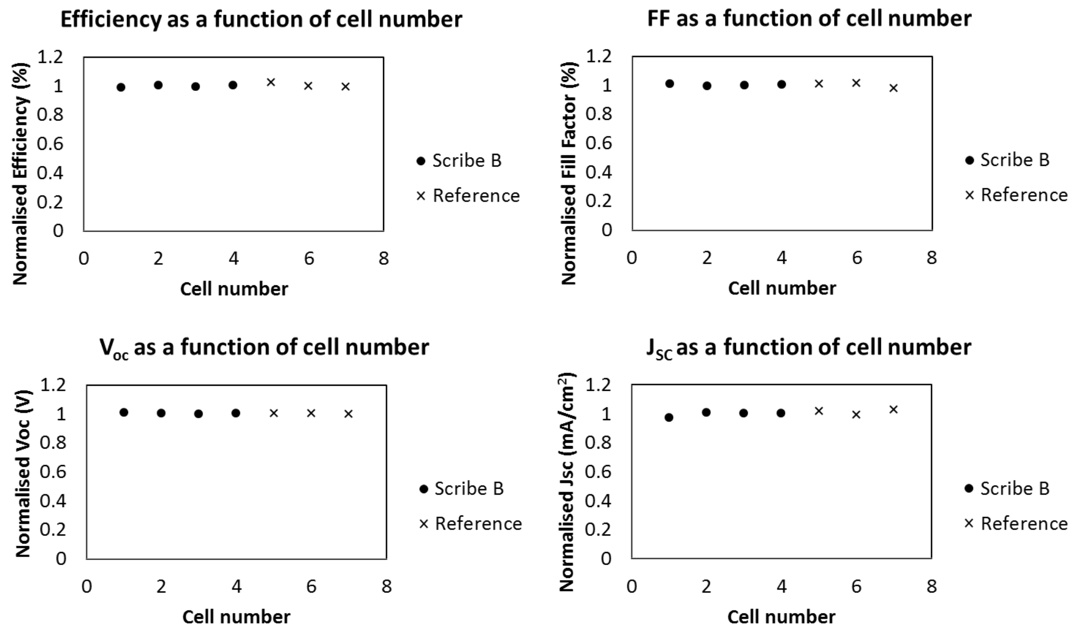


Figure 3.25: A comparison of the standard interconnect and an interconnect with an additional P3 scribe. Both sets of measurements are comparable indicating that the B scribe is not damaging the cell.

In the first instance testing the electrical performance of scribe A was carried out by removing an area of cell down to the TCO using the scribe B settings. It was then possible to perform the IR part of scribe A through the TCO from both glass and film side and check its isolation. A 6cm line was tested, over that distance the resistance of the glass side process was found to be 8MΩ, meeting the requirement of good electrical isolation.

The final test of scribe A was similar to the test for scribe B; an A scribe was used to define a new total cell area by cutting an existing cell in half. Half of a mini-module was modified in this way and half was left as a control, the results of this test can be seen in Figure 3.26. Using these laser processes OSI was sown to work on this TF-Si stack, with excellent electrical performance, FF > 70%, however the exact electrical characteristics are customer confidential and therefore not included.

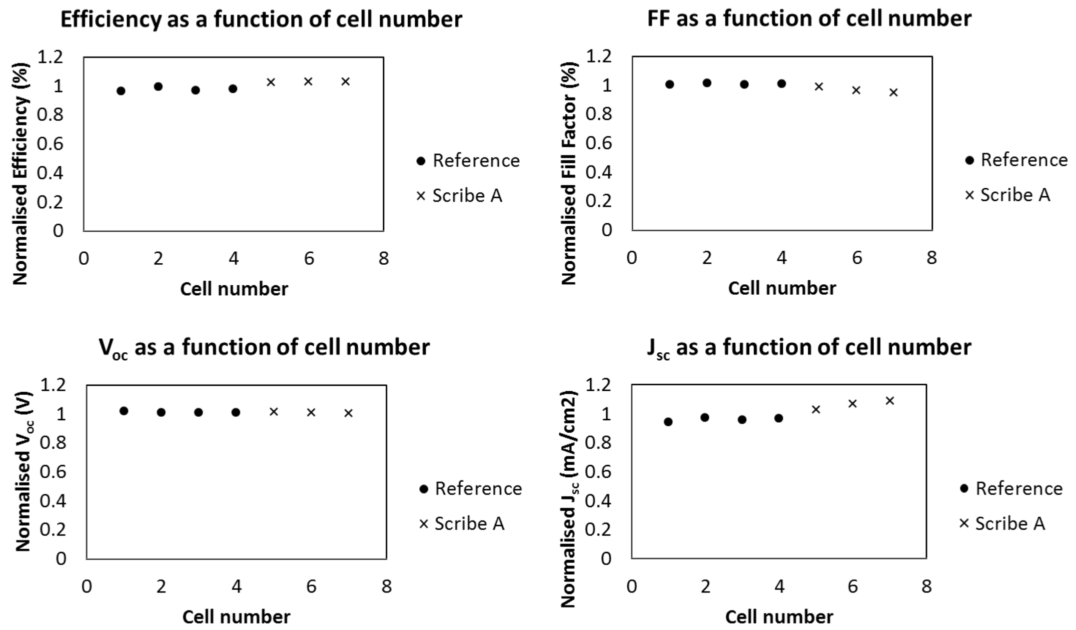


Figure 3.26: Plots showing the 4 key solar cell performance parameters. Reference shows the measurements as received, Scribe A shows the measurements after using the two-stage A scribe to define a new cell area. The cell performance is not negatively impacted indicating that the process is good.

3.1.6 Development of alternative A-Scribes for other TCOs

Different material recipes of TF-Si were received for interconnection by OSI and with minimal modification, adjustment of laser pulse energy, the developed process using the ns green laser through the glass with an imaged spot for the B scribe was fine in all cases. However, the second stage of the two stage A scribe with the ns IR laser removing the TCO was found to be unsuitable and required significant development. In this case the TCO was ~1.8µm of aluminum doped zinc oxide (AZO). The IR laser was unable to adequately isolate the TCO resulting in a resistance of 165Ω over ~6cm line. The results of the scribe A electrical test on the new samples can be seen in Figure 3.27, both FF and Isc are impacted by the poor scribe dropping 22% and 35% respectively due to incomplete isolation.

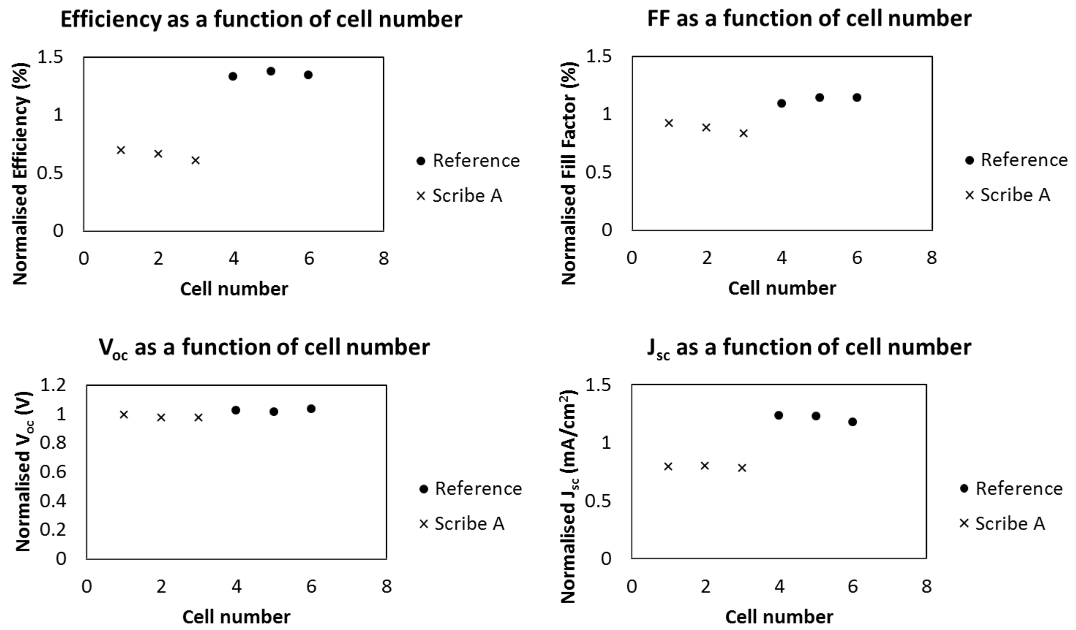


Figure 3.27: The A scribe electrical test for the developed glass side IR process on the material with the new TCO. Not isolating the TCO results in poor electrical performance.

In order to find a viable process different laser wavelengths were tested, both incident from the coating and glass sides making a total of 6 different approaches. The lasers tested were the IPG (1µm), Explorer (532nm) and the Matrix (355nm). Of the 6 approaches 5 produced scribes which, under visual inspection, appeared to isolate, see Figure 3.28. There is no result for glass side ablation using UV since the absorption of the glass prevented sufficient energy to be transmitted to the TCO. Both the UV and IR film side processes isolated the TCO however both were found to shunt the cell, the green film side process didn't isolate and also resulted in some shunting. It was found that the green laser incident through the glass provided both adequate isolation (>5MΩ) and good cell electrical performance. For TCO ablation to occur using a wavelength of 532nm it was necessary to focus the laser down to a small, Gaussian spot (~25µm in diameter), increase the frequency to 40kHz and increase the fluence to 4.9 J/cm^2. TCO absorption at 532nm is, by definition, low, however it has been shown that indirect free carrier absorption can occur in the visible [18] and this maybe the absorption mechanism at high photon densities. Optical images of all approaches can be seen in Figure 3.28 and the electrical results of the 532nm glass side scribe can be seen in Figure 3.29.

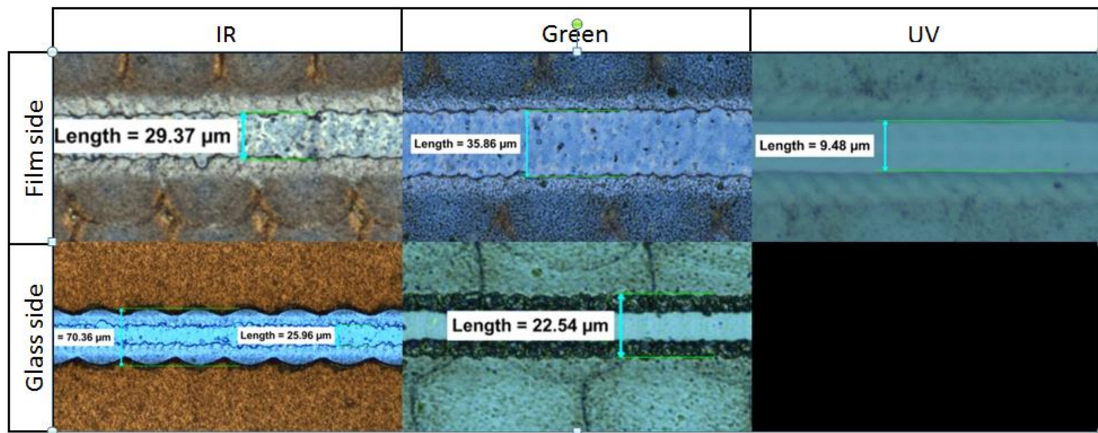


Figure 3.28: A comparison of scribes on the new TCO material at 3 different wavelengths and incident from the film and glass side. The film side IR and UV processes were found to isolate well but shunt the cell while the green film side process didn't completely isolate as well shunting. The glass side IR process was also found to shunt the cell. The only approach which both resulted in good isolation (>5MΩ) and no shunting, confirmed by I/V measurement, was the glass side, green process.

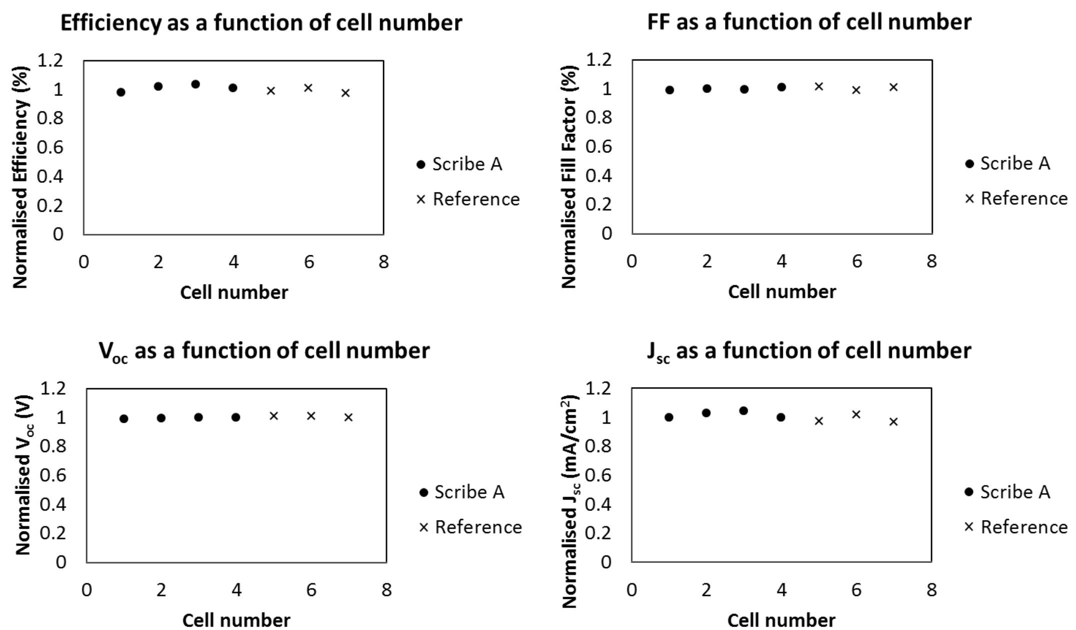


Figure 3.29: The electrical test of the redeveloped 2 stage A Scribe using the green laser for both stages.

The newly developed scribes were shown to be electrically sound and were used to manufacture OSI interconnects on this material also. A methodology for the development and verification of laser processes on PV material has been developed and shown to work on TF-Si. This same approach was applied to laser process development on other thin-film PV materials, detailed below.

3.5 Cadmium Telluride

CdTe cells from two university sources were used for development during the course of this work. The first was from Colorado State University (CSU) in the US. The modules were built on Pilkington NSG TEC10 glass which is a glass substrate coated with 10Ω/sq Fluorine doped Tin Oxide (FTO). A thin layer of n-type CdS, <100 nm, and a thicker p-type layer (~2.5μm) of CdTe is then deposited by Closed Space Sublimation (CSS) to form the absorber layer [19]. The devices then received a copper doping treatment which allows an Ohmic contact to be formed with a metallic back contact. The cells were then sent to the Centre for Renewable Energy Systems and Technology (CREST) at Loughborough University for the deposition of the back contact. Two different back contact materials were tested; nickel and gold.

The second source of CdTe was the Centre for Solar Energy Research (CSER) from Glyndŵr University. Their CdTe is deposited by a novel atmospheric MOCVD process onto the same commercially available NSG TEC10 substrates as CSU [9,10]. The stack consists of 150nm CdZnS and 2.25μm of CdTe, incorporation of Zn into the CdS layer increases its transmission resulting in larger current densities within the device. The CdTe layer has two different dopant densities resulting in an npp^+ structure. The p^+ layer results in a more Ohmic contact for the metallic back contact, which in this case was a thermally evaporated 200nm layer of gold [20], [21].

3.5.1 CdTe Scribe development on FTO substrates

It was decided to use the glass side processing with 532nm ns laser pulses as the basis for CdTe laser process development, informed by the TF-Si development and in line with the industrial process [4]. During laser process optimisation it was found that for both types of CdTe using high overlap scribes does not result in back contact delamination as seen in TF-Si. Moreover, low overlap scribes as used for TF-Si result in poor scribe morphology due to melted remnants of the CdS buffer layer. A high overlap B scribe results in cleaner ablation to the FTO. A comparison of low and high overlap B scribes on the CSER CdTe can be seen in Figure 3.30. The results on the equivalent, TEC 10 based, CSU device were practically identical.

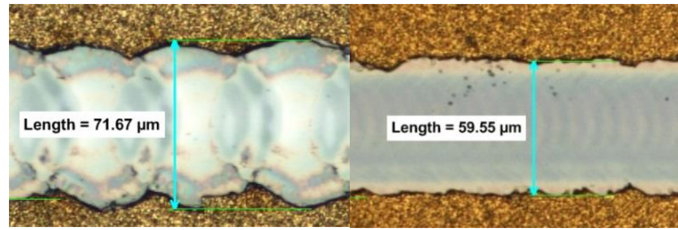


Figure 3.30: Left; low overlap B scribe on CSER CdTe, 7kHZ PRF and 300mm/s beam speed, note the melted/recast CdZnS buffer layer. Right; High overlap scribes, 40kHz PRF and 300mm/s beam speed, showing excellent scribe morphology.

During development of a TF-Si laser process it has already been shown that increasing the fluence of the 532nm laser will remove some TCOs. Since CdTe doesn't exhibit the same requirement to have low overlap scribes in order to avoid delamination of the back contact it was decided to test high fluence, high overlap settings for a single pass A scribe. The resulting scribe was much narrower than the equivalent two stage process and after inspection with the optical microscope it appeared to have good morphology, Figure 3.31.

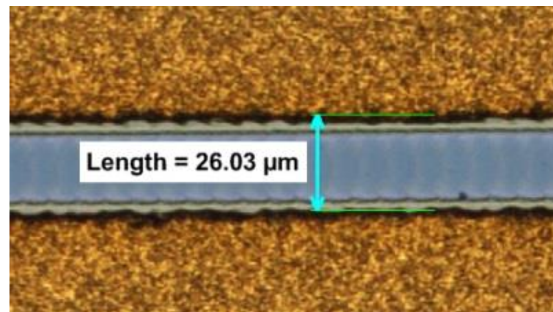


Figure 3.31: A single stage scribe A process on CSER CdTe showing good scribe morphology. Note the width is much less, ~25µm, compared with the equivalent 2 stage process on TF-Si, ~70µm.

Neither University group was able to supply mini-modules with a standard method of series interconnection making scribe verification more difficult. Since it was not possible to add the developed scribes to existing interconnects and look for a change in cell performance as with the TF-Si samples therefore new methods for scribe verification were sought. A series of test structures were devised manufactured and probed to check both scribes A and B. The test structures are detailed below. Both scribes A and B were verified on both CSU and CSER CdTe using these structures.

3.5.2 CdTe Scribe verification test structures

Test structures 1, Figure 3.32, and 2, Figure 3.33, were used to verify the B scribe. Test structure 1 checks for shunting. The result should be a high resistance, on the order of 10's kΩ the value of which depends on the resistivity of the absorber, in this case CdTe and the size of the remaining cell through which the resistance is measured. Predicting the expected value is difficult with the cell resistivity changing depending on the quality and doping of the semiconductor however the test will show up scribes which definitely fail. Resistances as low as 10's Ω have been measured from failed scribes.

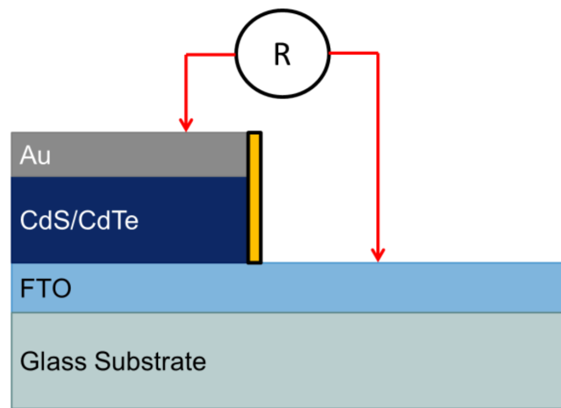


Figure 3.32: Test structure 1, direct measurement of shunt resistance between front and back contact. The potential location of shunts is marked along the scribe edge in yellow.

Test structure 2 checks for damage to the TCO. An area is cleared using the B scribe large enough to measure the sheet resistance of the TCO using a 4-point probe. A significant increase in sheet resistance from the initial value, 10Ω/sq in for these TEC10 modules, would indicate that the B scribe was damaging the TCO.

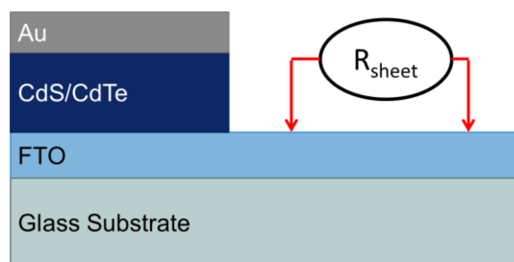


Figure 3.33: Test structure 2, direct measurement of sheet resistance after B scribe.

Test structure 3, Figure 3.34, and 4, Figure 3.35, are used to verify the A scribe. Structure 3 checks for electrical isolation. An A scribe is completed and the area surrounding is cleared with the already verified B scribe. The measurement should be an extremely high resistance, at least in the order of a few MΩ.

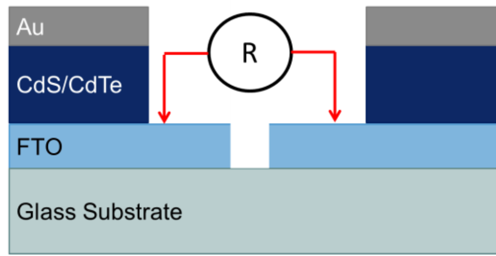


Figure 3.34: Test structure 3, direct measurement of electrical isolation across A scribe.

Test structure 4 checks the A scribe for shunting. An A scribe is used to define an area and a B scribe then clears a section of cell away from the A scribe and the shunting is measured as in test structure 1. The result should not be significantly lower than that measured in structure 1 as this would indicate extra shunting introduced by the A scribe.

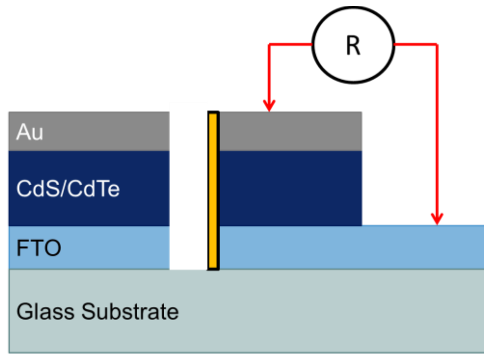


Figure 3.35: Test structure 4 measurement of the decrease in shunt resistance caused by the A scribe.

The results of these 4 tests on CSU CdTe can be seen in Table 3.4, below. Since the CSU CdTe and the CSER CdTe built on TEC glass are similar it was expected that the same scribe settings would produce similar results.

Test structure	CSU
1 (kΩ)	500
2 (Ω/sq)	14
3 (MΩ)	5.8
4 (kΩ)	504

Table 3.4: Results of verified A and B scribe test structures on CSU CdTe samples.

The verified scribes were used for fabrication of OSI mini-modules. Images of the final scribes on CSU and CSER CdTe can be seen in Figure 3.36 and Figure 3.37 respectively. The process parameters for each material were identical and can be seen in Table 3.5. More information on the resulting mini-modules can be found in Chapter 5.

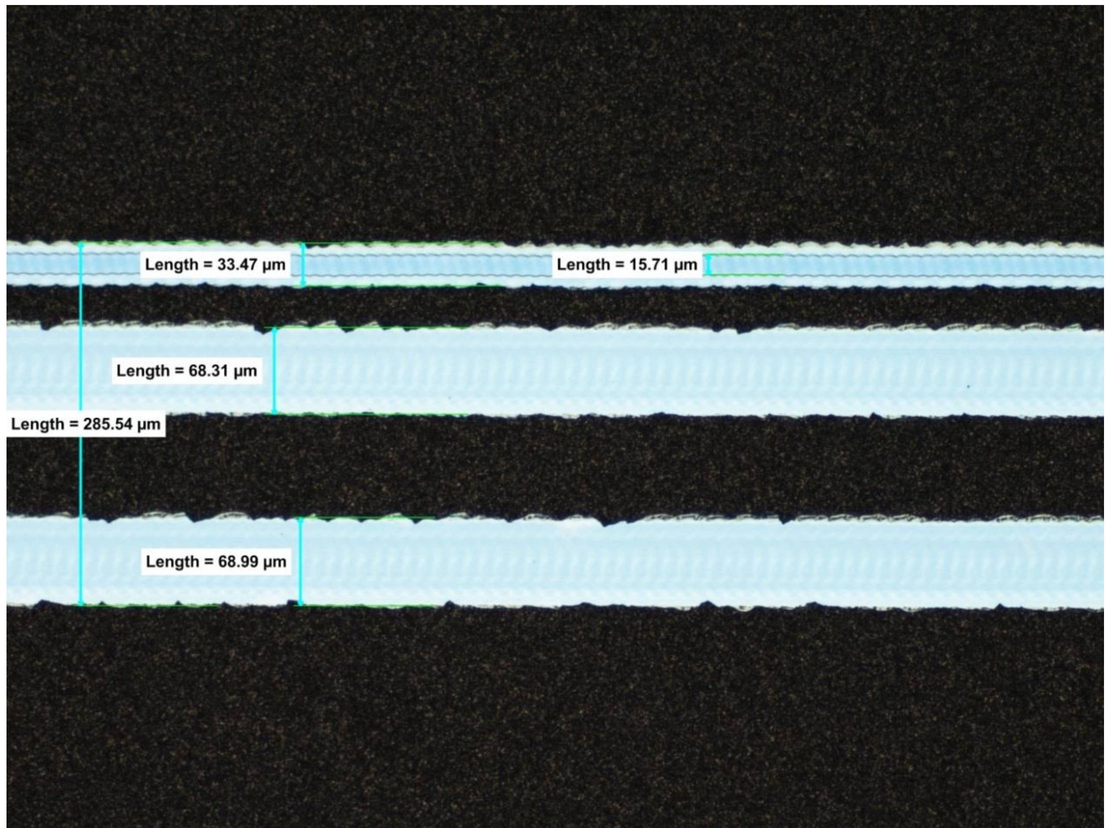


Figure 3.36: OSI scribes A, B and P3 on CSU CdTe.

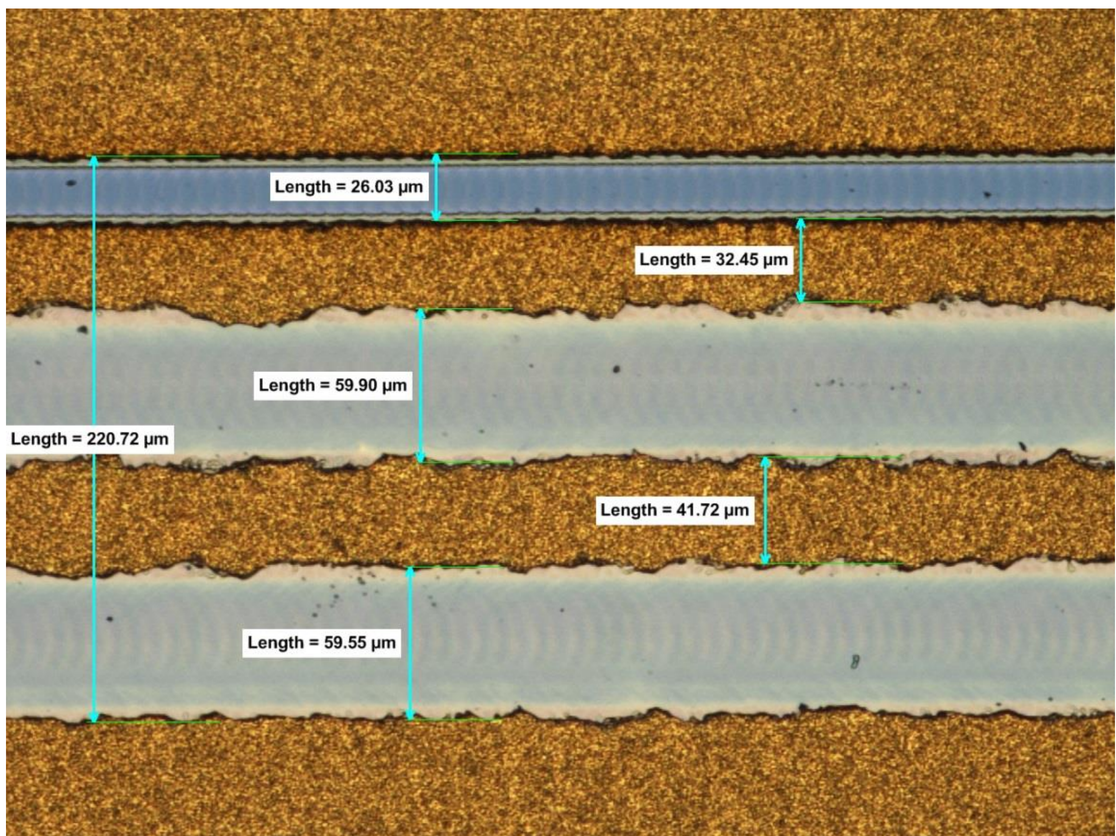


Figure 3.37: OSI scribes A, B and P3 on CSER CdTe.

Process step	Parameter	Value
Laser - A scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	4.50
	Spot diameter (µm)	26
	Pulse duration (ns)	10
	Pitch (µm)	<12
	Optical setup	Focused Gaussian beam
Laser -B scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	0.85
	Spot diameter (µm)	60
	Pulse duration (ns)	<12
	Pitch (µm)	42.9
	Optical setup	Imaging 750um mask

Table 3.5: Laser processing parameters used for both University CdTe samples, CSU and CSER.

3.1.6.3 CdTe devices built on ITO

CSER build their record efficiency devices on a commercially available ITO on thin, ~0.7mm, boroaluminosilicate glass substrate with sheet resistance in the 4-8Ω range. The record for CSER cells on such a substrate stands at 15.3% [22]. There was interest in manufacturing interconnected mini-modules based on these cells with high efficiency using OSI. Therefore a laser process was required on the ITO/CdZnS/CdTe/Au stack. Using the approach which has been shown to work on the equivalent FTO based devices does not work on the ITO based devices. With the explorer 532nm, ns pulsed laser the damage threshold of the ITO is below that of the removal threshold of the semiconductor stack meaning that in all cases the TCO is damaged when the cell is removed. Example scribes around the ablation threshold of the cell can be seen in Figure 3.38. Both low and high overlap scribes were tested using the mask imaging system described previously.

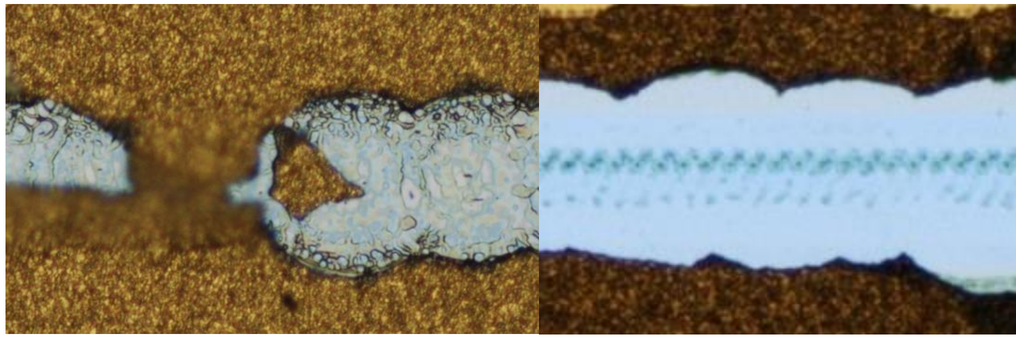


Figure 3.38: Through the glass scribe (532nm) on ITO based CdTe. Left; a low overlap, single shot process. Right; a high overlap process. In both cases the ITO appears to be damaged before the CdTe is fully removed.

IR and UV wavelengths were tested for the B scribe on the ITO based CdTe devices. The substrate used for these experiments is much thinner than most used so far, ~0.7mm compared to ~3mm, meaning that a through the glass UV process is possible. Both through the glass and film side UV and glass side IR have been tested, the results can be seen in Figure 3.39.

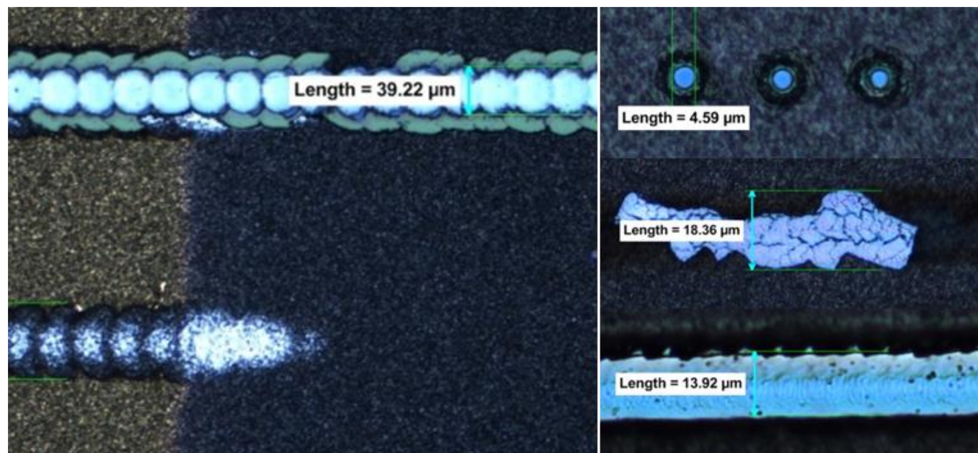


Figure 3.39: Left; through the glass process with 1µm laser, the top line is just above threshold, the ITO has already been cleanly removed, the lower line is just below threshold and shows the metal back contact has been preferentially removed indicating that this CdTe is mostly transparent at 1µm. Right: UV laser processes, top through the glass and in focus results in a very small scribe A, Middle, out–of-focus through the glass results in significant ITO cracking before CdTe is removed. Bottom, film side UV process showing the same poor morphology and melting as seen in IR film side processing.

As is expected it is possible to make very narrow A scribes using UV through the glass, ~5µm in width, which may be of interest at some point for minimising dead area. However, the B scribe process is not possible through the glass with UV as more TCO damage is observed than with the green laser. The film side UV scribes on this CdTe

exhibits the same burrs as all the film side processes tried so far. Scribing with the IR laser through the glass results in either removal of the entire stack or selective removal of the metal back contact indicating that CdTe is largely transparent at 1064nm and neither approach generated a useful result.

Unfortunately, a working scribe process has not been found which causes problems for both OSI and conventional interconnects on this material. The other variable that could be tested is pulse duration, moving to a short pulse duration, ps-fs, results in 'cold' ablation since the laser pulse duration is less than the time it takes for energy to thermalize to the lattice resulting in ablation with no HAZ. It is likely that a film side ultrashort process could be found and this may be worth investigating for generating samples on these university samples. This is especially true since the cost and reliability of ultrashort (ps, fs) lasers are constantly improving and are therefore becoming a viable alternative to nanosecond laser in industrial manufacture. A glass side ultrashort process may be difficult due to nonlinear absorption in the glass when a high e-field is used, this would require investigation to determine whether the ablation threshold of the CdTe is below the threshold for non-linear processes to occur in glass.

3.1.6.4 Simple mathematical treatment of through the glass ablation

It is intuitively obvious that the green laser should work for the B process since the TCO is by definition transparent in the visible and, for instance, that an IR laser should not since the absorption of the TCO is relatively high due to free carrier absorption. However this is not observed, as a viable process when scribing the ITO based CdTe cells with the green laser could not be found. Furthermore it was shown earlier in this chapter that a through the glass IR scribe B process is possible on TF-Si.

The actual situation is less clear and is dependent on the interplay between damage threshold and absorption coefficient of the layers involved. It is possible to develop a simple mathematical relationship between the ablation threshold and absorption coefficients of the materials that will predict the minimum damage threshold that a TCO must have for a through the glass process to be successful at a given wavelength.

In the case of a single laser shot, for ablation to occur the fluence of the incident laser pulse ($E_p, J/cm^2$) must be greater than the ablation threshold fluence ($\emptyset_{TCO}$, J/cm^2) assuming complete absorption, Equation 3.3.

(3.3) $$E_p > \emptyset_{TCO}$$

The TCO by definition does not exhibit complete absorption therefore this expression must be modified by the percentage Absorption (A_{TCO}) which is material quality, wavelength and layer thickness dependent, Equation 3.4.

(3.4) $$A_{TCO}E_p > \emptyset_{TCO}$$

In a two layer system the same expression can be written for ablation of the second layer, in the case of TF-PV the semiconductor, the pulse energy modified by the two absorption coefficients, i.e. the energy reaching the semiconductor, must be greater than the ablation threshold fluence for ablation to occur. Ignoring reflection from interfaces Equation 3.5;

(3.5) $$(1 - A_{TCO})A_{SC}E_p > \emptyset_{SC}$$

Assuming all the energy is absorbed in the semiconductor, as is the case for visible wavelengths in PV materials, then $A_{SC} = 1$. For there to be a process window for the B scribe process, i.e. the semiconductor is ablated leaving the TCO intact then Equation 3.6;

(3.6) $$\frac{\emptyset_{TCO}}{A_{TCO}} > \frac{\emptyset_{SC}}{(1 - A_{TCO})}$$

or,

(3.7) $$\frac{\emptyset_{TCO} - \emptyset_{TCO}A_{TCO}}{A_{TCO}} > \emptyset_{SC}$$

It is possible to plot TCO absorption against pulse energy for a two layer TCO/semiconductor stack. Assuming complete absorption in the second layer and that the TCO has a damage threshold equal to the semiconductors ablation threshold the plot is shown in Figure 3.40. The absorption coefficient of ITO on boroaluminosilicate glass was measured, using a spectrophotometer, by CSER to be 18.41% at 532nm, the glass

substrate without ITO had 7.80% absorption at 532nm therefore the ITO layer had 10.61% absorption. The range of incident fluences which ablate the semiconductor but leave the TCO undamaged at 10.61% TCO absorption are marked on Figure 3.40. It can be seen that there is a process window.

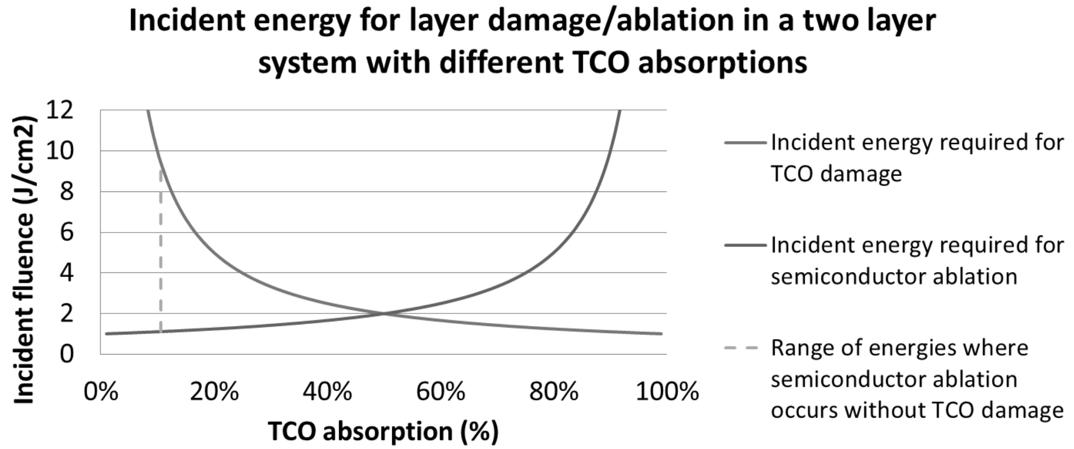


Figure 3.40: Plot of incident laser fluence required for ablation of TCO and semiconductor layers against TCO absorption assuming equal ablation thresholds. The green dotted line marks the range of incident fluences over which the semiconductor is removed without damaging the TCO at the measured absorption of the ITO film. There is a process window of 8.3J/cm^2.

From the experiments above it is clear that in reality there is no process window for this stack at 532nm. Therefore the damage threshold of the TCO must be lower than the ablation threshold of the semiconductor. It can be calculated using Equation 3.7 that for the damage threshold of the ITO to be equal to the ablation threshold of the CdTe that the ITO damage threshold is ~12% of the semiconductor ablation threshold. This situation is plotted in Figure 3.41. It can now be seen that at 10.6% TCO transmission there is no energy where the semiconductor is ablated without damaging the TCO, reflecting reality. In order for there to be a process with this laser the TCO would have to be more transparent at 532nm or have a higher damage threshold. Another approach would be to choose a laser wavelength at which the TCO is more transparent however laser availability precludes this now.

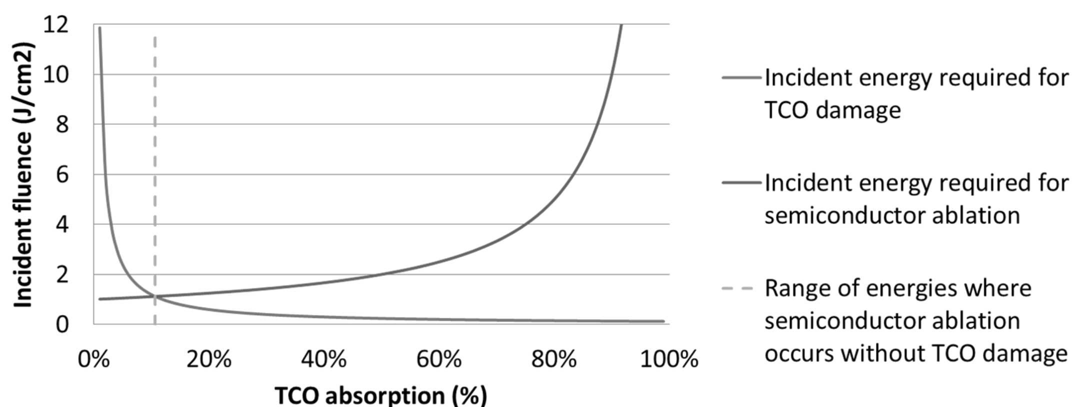


Figure 3.41: Plot showing the laser pulse energy required for ablation of the TCO and semiconductor layers in a two layer system with a TCO damage threshold of 12% that of the semiconductor. The absorption of the real ITO film is marked with the green dashed line, at this value there is no energy which ablates the semiconductor without damaging the TCO. Increasing the TCO transparency would move the green line to the left to a point where there is a process. Increasing the TCO damage threshold would move the crossover point to the right resulting in a process at this absorption.

This simple mathematical treatment demonstrates the situation observed experimentally with the ITO based CdTe devices from CSER. This model ignores the reflection from the air-glass and glass-TCO interfaces and does not deal with the case of incomplete absorption in the semiconductor these would be logical extensions to this simple model. The other effect that isn't investigated is heating of the TCO from absorption in the semiconductor. This would have two effects, firstly if the temperature attained at the interface is high the TCO could experience surface melting or for thin layers crack due to CTE mismatch with the substrate. Secondly the increased temperature in the TCO would increase the free carrier density in the TCO, this would increase the absorption in the TCO making the absorption coefficient both time and energy dependent. Further work in this area could involve a finite element (FE) model to incorporate these factors. This model could be verified experimentally by measuring the two threshold fluences.

3.6 CIGS – substrate cells

CIGS is different to the other TF-PV materials discussed previously in that it is built in a substrate configuration with the metallic contact next to the glass. The substrate configuration makes laser scribing difficult as it is no longer possible to have the laser incident through the glass. This means that the standard series interconnection on CIGS

is made with a laser for the P1 scribe but mechanical P2 and P3 scribes must be used [8]. Mechanical scribes are not currently suitable for OSI as the width is non-uniform due to fracturing at weak points along material boundaries, advanced techniques for mechanical scribing could be investigated with relation to OSI but this is beyond the scope of this thesis.

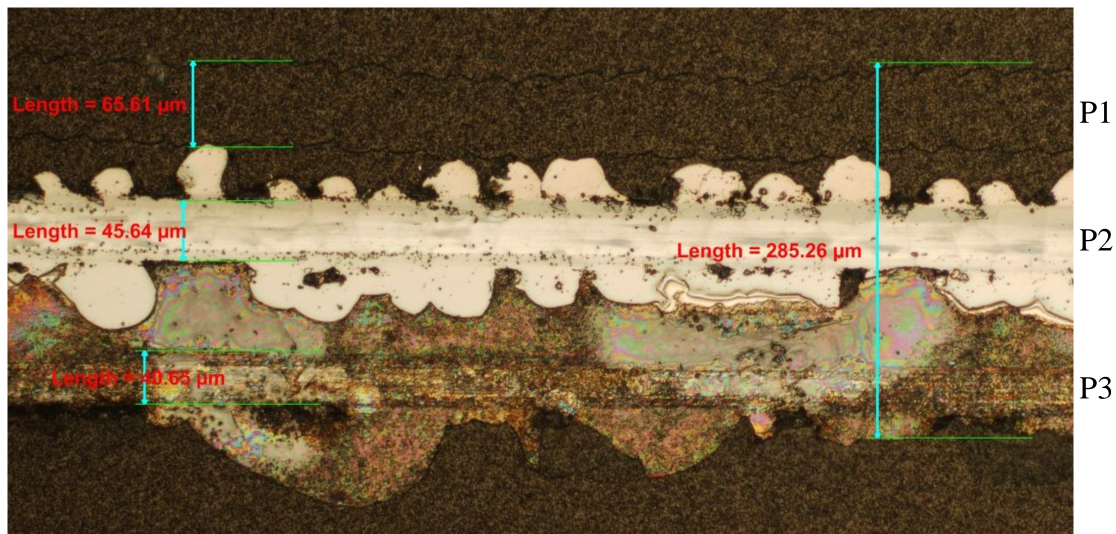


Figure 3.42: Conventional interconnect on CIGS. Laser P1, mechanical P2 and P3, note the inhomogeneous fracture lines caused by the mechanical process, unsuitable for OSI.

A novel ns CIGS scribing process has been developed by Pyro photonics in collaboration with NREL, discussed in detail in Chapter 2. Using a 1µm laser pulse with particular temporal characteristics, 2-5ns pulses with fast rise and fall times, it was found that the CIGS remains transparent long enough to deposit the energy at the Mo/CIGS interface [8–10]. This results in a brittle fracture mechanism, similar to through the glass scribing in superstrate cells. Scribes performed in this way appear to behave well electrically. Longer pulse durations begin to heat the CIGS increasing the density of free carriers and thus increasing free carrier absorption in the IR in an avalanche type process which leads to high CIGS temperatures and melting. It was decided to look more closely at the brittle fracture approach to CIGS scribing.

As well as the general requirements outlined above for OSI A and B scribes CIGS laser P2 and P3 processes would be of significant interest to the wider PV industry. Developing the capability to laser interconnect CIGS would place M-Solv in an advantageous position in the TF-PV capital equipment market. Therefore the P2 scribe is also being investigated. Figure 3.43 shows a diagram of the two processes of interest, P2 and P3/B.

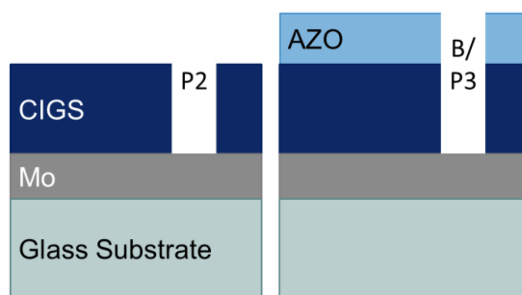


Figure 3.43: The P2 and P3 processes on CIGS. Although the P2 scribe is not used in OSI a P2 laser process would be of general interest to CIGS PV industry placing M-Solv in an advantageous position. Therefore it has also been investigated.

3.6.1 Lasers for CIGS

The 1µm IPG YLPM laser used for some of the development on the superstrate cells is capable of 1, 5 and 10ns pulse duration and was therefore tested for brittle fracture CIGS scribing. It was expected that CIGS would be less absorbing at a longer wavelength, since the bandgap is typically 1-1.2um [24], resulting in more of the energy being delivered to the interface. Multiwave Photonics (now MW-Technologies) lent M-Solv a PFL-1550 laser operating at a wavelength of 1550nm, with pulse durations of <5ns, a summary of the lasers characteristics can be seen in Table 3.6.

Manufacturer	IPG	MW Technologies
Model	*YLPM*	*PLF-1550*
Wavelength (nm)	1060	1550
Pulse duration (ns)	1,5,10	<5
Pulse Repetition Frequency (kHz)	10-600	20-150kHz
Max Average Power (W)	18	1
Max Pulse Energy (µJ)	60-300	>20

Table 3.6: Laser specifications used for scribe development on substrate CIGS cells

3.6.2 Optical Setup

The MW 1550nm laser was integrated onto a temporary system consisting of 2-axis Aerotech controlled stages (x,y), ScanLab intelliScan 14 galvanometer scan head and camera mounted on an optical bench. The scanner interface is handled by an RTC5

control board connected to the same PC as the stage controller, all hardware is controlled through bespoke M-Solv software. The scanner was on a mechanical z-stage for setting focal height. Images of the temporary setup can be seen in Figure 3.44.

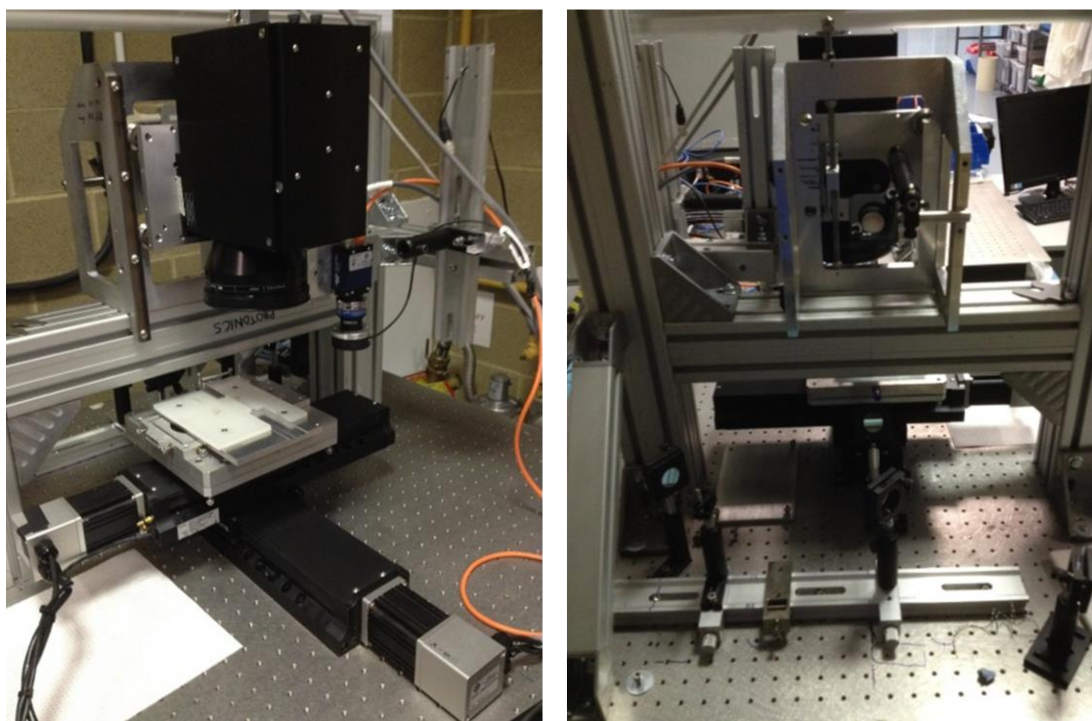


Figure 3.44: Temporary optical bench setup for 1550nm laser used for CIGS scribing. 2-axis Aerotech stages are mounted below an extrusion gantry with a galovonometer scan head mounted above.

CIGS from 3 different suppliers were obtained for process development, 2 potential customers (labelled ‘C1’ and ‘C2’) and samples from the University of Uppsala, Sweden (labelled ‘U1’). C1 and U1 are both built on soda lime glass whereas C2 uses a stainless steel substrate, all three samples use molybdenum and AZO as the contacts. All three CIGS suppliers supplied full stack CIGS for P3/B testing, C1 and U1 also supplied CIGS without the AZO front contact for P2 development.

3.6.3 1µm scribing of CIGS

The conclusion of Pyro Photonics work was that the laser pulse must have a fast rise and fall time and be sufficiently short so as to deposit enough energy at the CIGS/Mo interface without increasing the temperature of the CIGS causing it to melt, the assertion being that their pulse programmable fibre lasers pulse characteristics made it unique in being able to do this process [23]. It was decided to try and recreate the work

done by Pyro Photonics with their pulse programmable 1μm laser using the IPG which is capable of running at 1, 5 and 10ns.

Using the previously described methodology for optimisation of scribes a P2 process was found with the IPG on the C1 P2 samples. A process was found at all three pulse durations. The 10 and 5ns scribe lines were ~35μm wide, whereas the 1ns line was ~30μm. All three lines were produced at 10kHz PRF, with a beam translation speed of ~300mm/s and therefore a low shot overlap of ~10%. The optimum pulse energy for each pulse duration was comparable and in the range of 8-15μJ. The Mo surface at the bottom of the 1ns scribe appears less reflective except at the overlap of individual laser shots and this was attributed to reduced melting at the shorter pulse duration, optical micrographs of each process can be seen in Figure 3.45. The scribe edge quality was inspected with SEM and the optimised scribes at all pulse duration appear to show little melting along the edge and some lift off of the remaining CIGS, see Figure 3.45. This combined with the low pulse energies indicates that the mechanism is brittle fracture. In all cases the process window in energy is extremely small, at most +/-2μJ before either the lines become intermittent or excessive melting is observed.

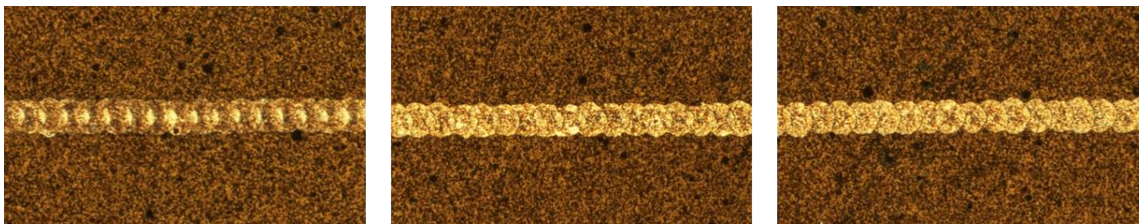


Figure 3.45: A P2 process on CIGS sample C1 at 10, 5 and 1ns pulse duration (left to right). Scribes were made with the IPG YLPM laser. The beam translation velocity was 300mm/s, PRF 10kHz and the pulse energy was in the range 8-15 μJ.

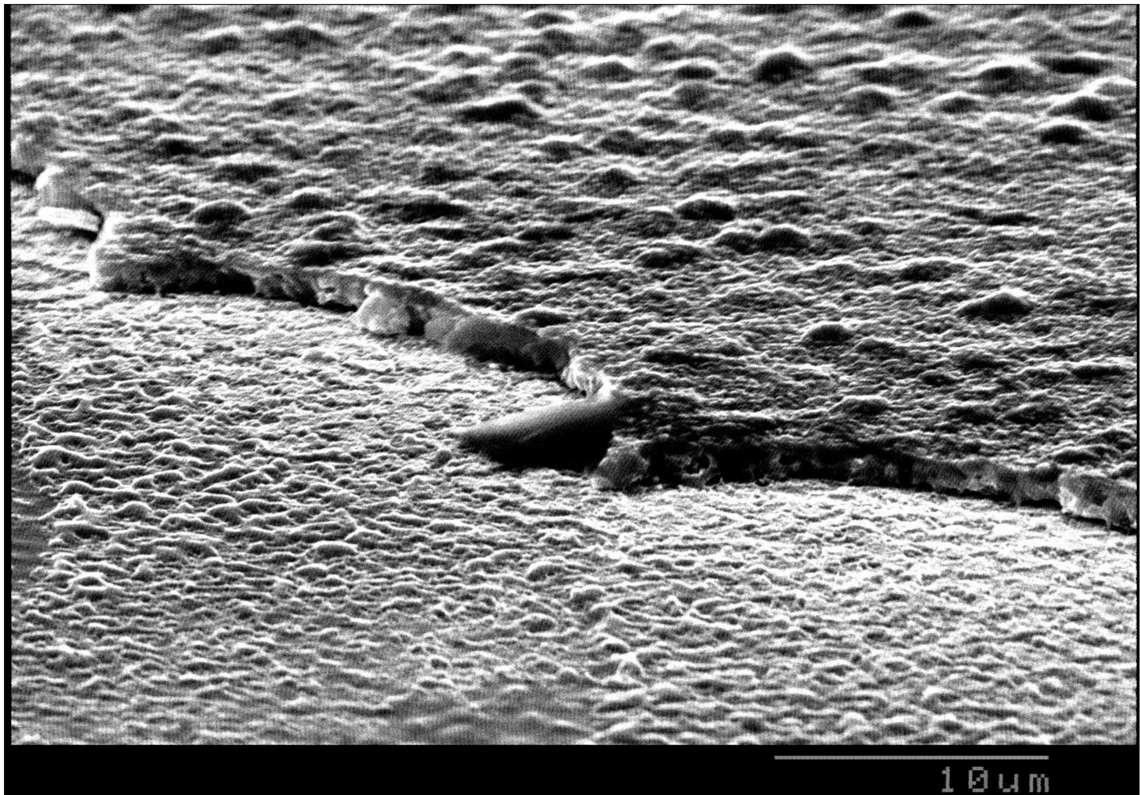


Figure 3.46: SEM image of a P2 scribe on CIGS made with the IPG laser. The scribe edges appear largely free from melt.

These C1 P2 samples were taken to CREST at Loughborough University for EDX measurements in order to determine the composition of the scribe bottom Figure 3.47. The textured surface appears to be composed of Mo and Se perhaps indicating that the $MoSe_2$ layer which forms between the contact and semiconductor [1] is intact. The smoother regions are Mo with lower Se content indicating the laser has dug deeper into the contact removing the $MoSe_2$ layer. For comparison a spectrum of the CIGS was also taken showing that the molybdenum signal is obscured by the CIGS.

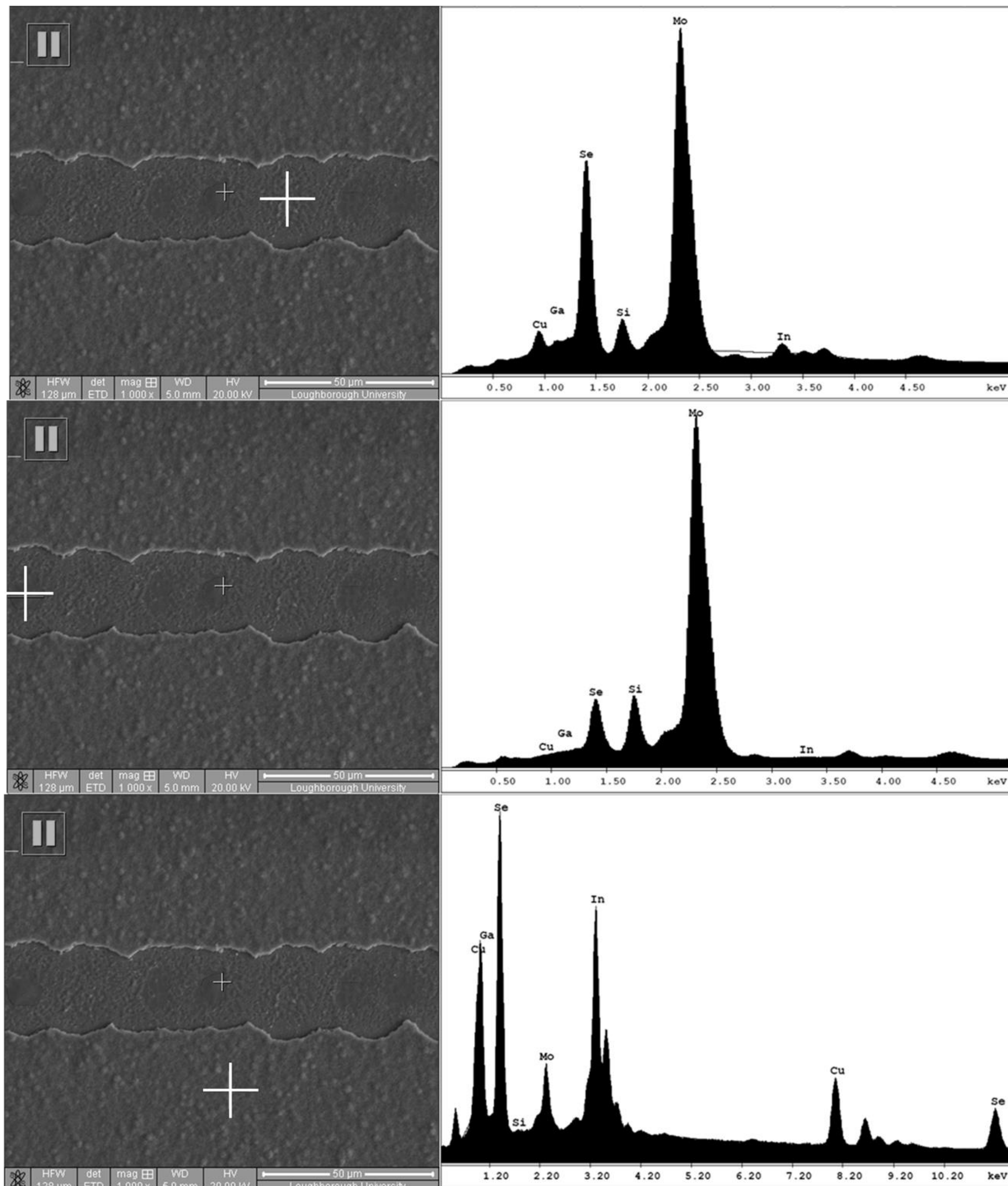


Figure 3.47: EDX of CIGS P2 scribes, large white cross marks the location that the spectra was taken. Top; Spectra from the bottom of the scribe on the 'textured' region. The composition is primarily Mo and Se, perhaps indicating the MoSe2 layer that forms between the back contact and the semiconductor is intact. Middle; spectra from smooth overlap region, the composition is primarily Mo with less Se indicating the laser has dug deeper into the contact in the overlap region. Bottom; a spectra from the bulk semiconductor for comparison, the main constituents are Cu, In, Ga and Se as expected with a small signal from the Mo beneath.

The P3/B scribe was also tested using the IPG laser on the C1 samples. No viable process was found for at 10 or 5 ns. At 1ns pulse duration no process was found with the ~30 μm spots, as tested for the P2 scribe, however moving to a larger spot diameter ~65 μm produced an intermittent process. This is likely due to the requirement that in order establish a minimum pressure to fracture the semiconductor, a minimum amount

of material must be vaporised corresponding to a minimum spot size over which the removal mechanism must occur. The increased minimum spot size for ablation indicates that the AZO layer is strengthening the stack thus requiring increased pressure to cause fracture. The process window in energy is still very small. Figure 3.48 shows a series of scribe B scans at 10 kHz using the IPG laser with 1 ns pulse duration on the C1 material. The step in pulse energy between lines was ~2 µJ which corresponded to an increase in laser diode current of 1%. The top line, which is closest to an optimised process, was at a pulse energy of 24.5 µJ.

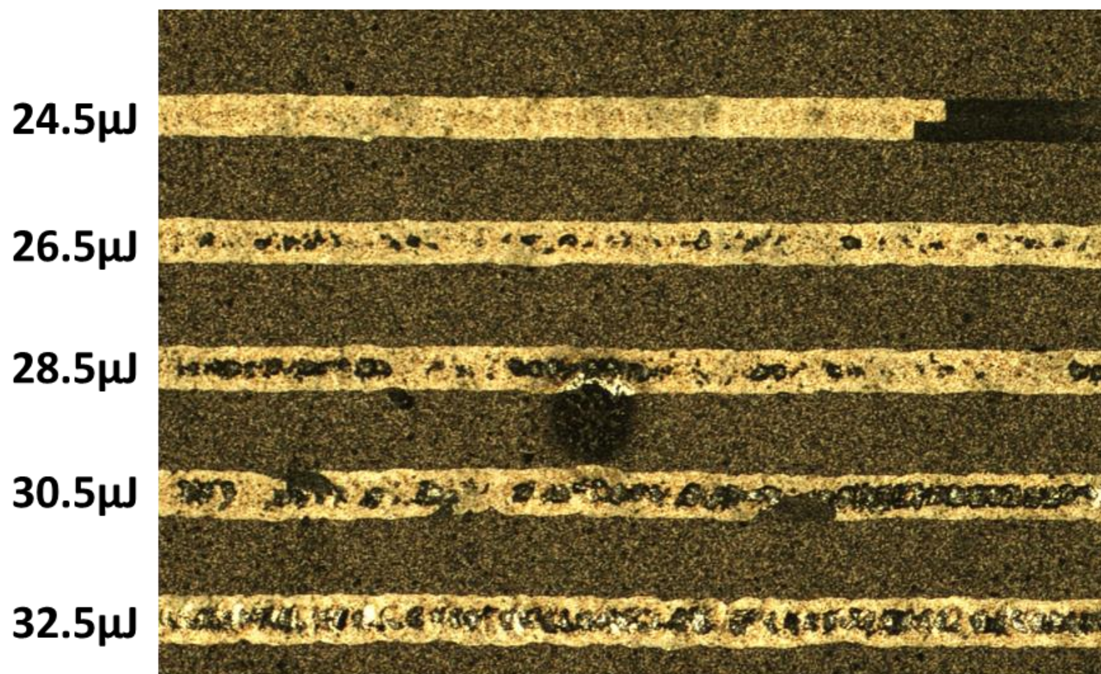


Figure 3.48: A Scribe B power scan on C1 CIGS. The pulse energy step between subsequent lines is ~2 µJ with the top line being 24.5 µJ. The beam translation velocity is 300mm/s, the PRF 10kHz and the nominal spot size ~65µm giving an overlap of 54%.

In the work from Pyro Photonics it was noted that this process works less well at higher shot overlaps, >50% [23], which might explain the intermittent process. It was not possible to achieve both the larger spot size and the low shot overlap with the experimental setup since the minimum laser frequency was 10kHz and the maximum stage speed was 300mm/s. It is likely that a more reliable process could be found with this laser using faster stages or a scanner system capable of high beam translation speeds, >4m/s, however at this time it was not possible to remove the IPG laser from the set-up due to on-going requirements with other materials.

The U1 samples were subjected to the same tests with the IPG laser with different results. At both 5 and 10ns pulse duration only melting of the CIGS is observed

however at 1ns an intermittent process with very low pulse energies with an extremely narrow process window was observed. The closest value to an optimum process is at 3-4 µJ, 10 kHz, 300 mm/s with a 30 µm spot. However, increasing the pulse energy to ~5 µJ results in a mostly melted scribe line with a few instances of brittle fracture, Figure 3.49 shows scribe lines at increasing pulse energy. The inconsistent process could be for two reasons, either the material is non-uniform and therefore reacts differently to the laser or the process window is so narrow that the laser pulse energy stability, quoted as <2% RMS, is not stable enough to find a reliable process. The second reason could well be exacerbated by running the laser at close to threshold diode current to achieve the low pulse energies as this tends to make the output less stable. An external attenuator made up of either ND filters or a thin film polariser and polarisation dependent beam splitter could have been used to obtain low pulse energies at higher diode currents making the laser more stable. This wasn't done as polarising elements were not available at the appropriate wavelength however it would be a logical next step for this work.

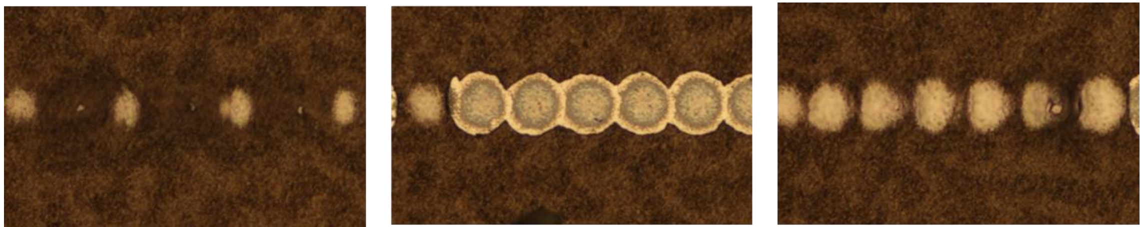


Figure 3.49: The effect of increasing pulse energy on the P2 process on U1 material with the IPG laser running at 1 ns pulse duration. The pulse energy is increasing left to right in steps of ~1 µJ from 3 – 5 µJ. The process works at 4 µJ, middle image, but is unstable.

The P3 process was tested on the U1 samples and all power levels, spot sizes and overlaps used resulted in heavily melted CIGS, Figure 3.50. The conclusion is that either the AZO or one of the buffer layers between the CIGS/AZO is highly absorbing at 1064nm causing a build-up of heat which is melting the CIGS.

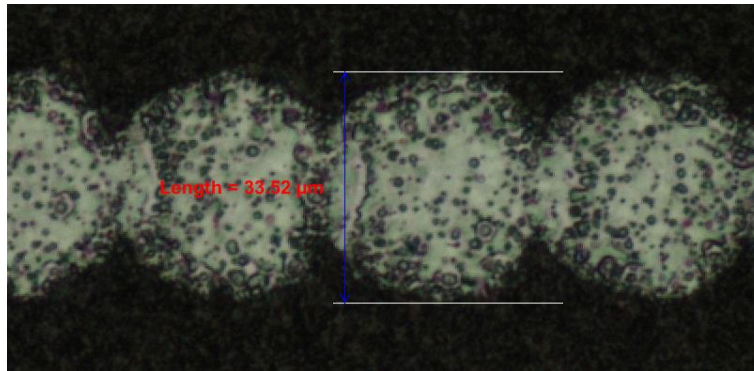


Figure 3.50: P3 process with the IPG at 1 ns. At all process parameters melting results indicating that one of the new layers, likely CdS buffer, i-ZnO, AZO, are absorbing at ~1µm.

The final samples, C2, were tested for the brittle fracture P3 process with the IPG laser. The material response was excellent with a reliable process found with a small spot, ~35µm, at PRF 10kHz and pulse energy ~10µJ at both 1 and 5ns, see Figure 3.51.

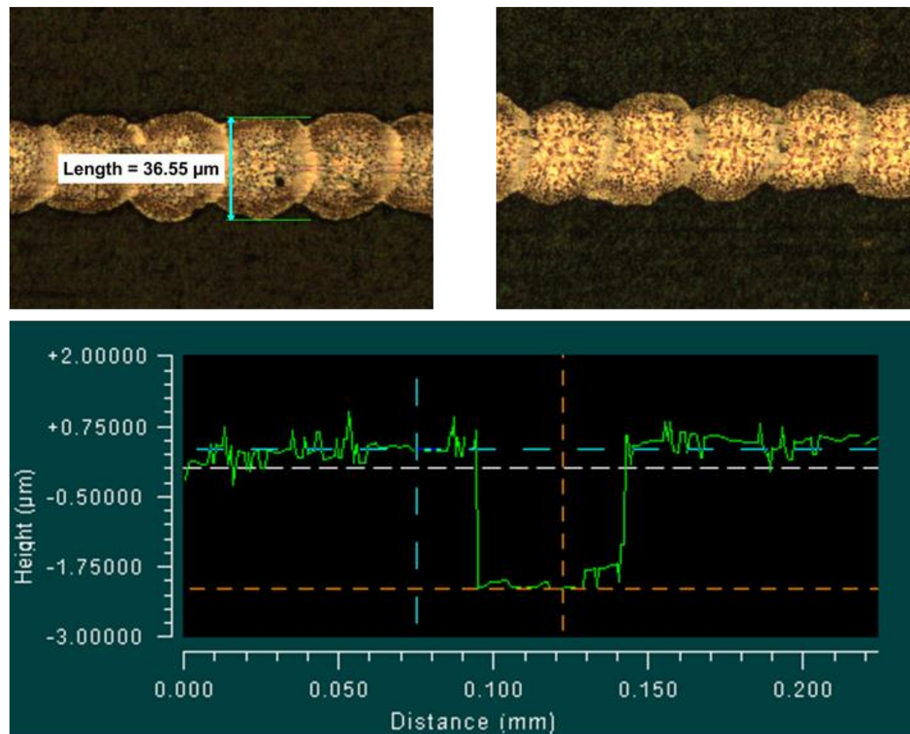


Figure 3.51: Top; optical images of the P3 process with the IPG at 1 ns (left) and 5 ns (right). There is a robust process at both puls durations. Bottom; an SWLI plot of the scribe line showing sharp edges and a scribe depth of ~2 µm.

In conclusion, it has been shown that the brittle fracture process developed by Pyro Photonics for the laser scribing of CIGS can be recreated with the IPG YLPM laser. This shows that the results are not unique to their pulse programmable laser and indicates that the process is perhaps less sensitive to pulse rise/fall times as claimed by Pyro Photonics. Unfortunately the process appears to be highly dependent on the exact

phase of the CIGS stack to be scribed. It is likely that small compositional changes are sufficient to move the bandgap so that it becomes less transparent at the 1µm laser wavelength. Consequently, a more universally applicable scribing process is desirable as discussed in the next section.

3.6.4 1.5µm CIGS scribing

A method for increasing the reliability and universality of the brittle fracture scribes on CIGS was sought. It was thought that by moving to a longer wavelength where CIGS is likely to be more transparent, the process may become more reliable since more energy can be deposited at the Mo/CIGS interface with less heating of the bulk material. A longer wavelength nanosecond pulsed lasers was sought and found at Multiwave Photonics (now MW Technologies) who produce the PLF-1550 laser, principally for LIDAR applications. It was expected that the wavelength of 1550 nm and a pulse duration of <5ns would be ideal for CIGS processing. M-Solv obtained a loan system for the initial tests along with a 1550 nm scanner from Scanlab.

Using the 1550 nm laser a robust process for both P2 and P3 processes on sample U1 was found over a range of spot sizes, ~30-60 µm, with a large range of overlaps and wider process window in terms of pulse energy, 4-8 µJ. Figure 3.52 shows what happens above and below the process window in energy, left 3µJ, centre 5 µJ, right 9 µJ, it can be seen that, as the energy increases, the process goes from one which is not energetic enough to fracture the CIGS, through an optimised process and finally to a process which deposits melted material in the centre of the scribe. At the optimised pulse energy, 7 µJ, it was possible to scribe at a range of shot overlaps. With a fixed PRF of 50 kHz a continuous scribe was formed at beam speeds of 1-1.8m/s with the upper limit being the formation of single shots, see Figure 3.53. These beam speeds are highly compatible with industrial processing making this a promising result.

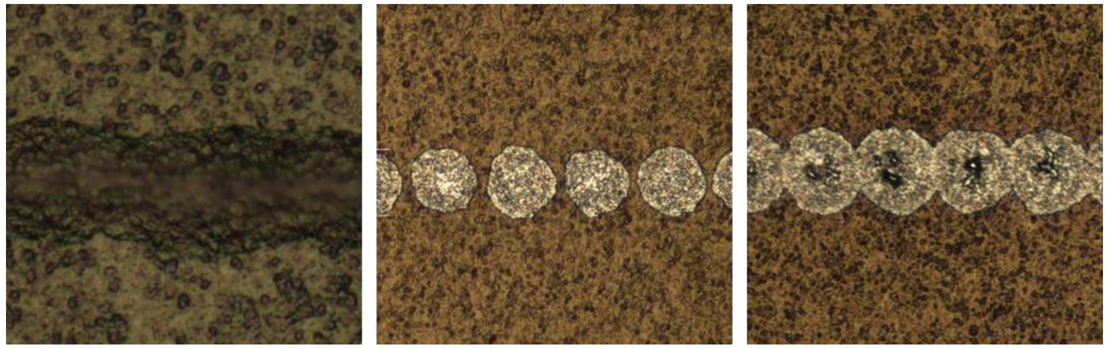


Figure 3.52: The effect of changing pulse energy on the P3 scribe of C1 CIGS. Left; 3 μJ, below threshold energy there is insufficient pressure to fully fracture the stack. Middle; 5 μJ, optimum pulse energy with a reliable process, 31μm spot. Right; 9 μJ above the process window melted material begins to be deposited in the centre of the scribe, 40μm spot.

Figure 3.53: The effect of increasing beam translation velocity on the P3 process, in all cases the spot size is ~32μm. The beam speeds were 1.1, 1.4 and 1.7 m/s giving shot overlaps of ~35, 20 and 5% respectively. This demonstrates that there is a robust process at a range of overlaps.

Using the test structures developed for verification of the scribes on the CSU CdTe samples the 1550nm B scribe on C1 CIGS was also verified. The results can be seen in Table 3.7, and indicate that the scribe was not shunting or damaging the Mo.

Test Struture	**C1**
1 (kΩ)	200
2 (Ω/sq)	1.4

Table 3.7: Electrical results of scribe B test structures for C1 CIGS. The resistance is high between the front and back contacts indicating that the scribe is not shorting whereas the metal contacts sheet resistance is low indicating that all insulative material is being removed without damaging the layer.

Sample U1 was also tested for both P2 and P3 scribing with the 1550 nm laser. Using the optimised settings determined for sample C1 no viable process was found, see Figure 3.54. Sweeping through a range of pulse energies and shot overlaps it was not possible to find a process with ~30μm, spots.

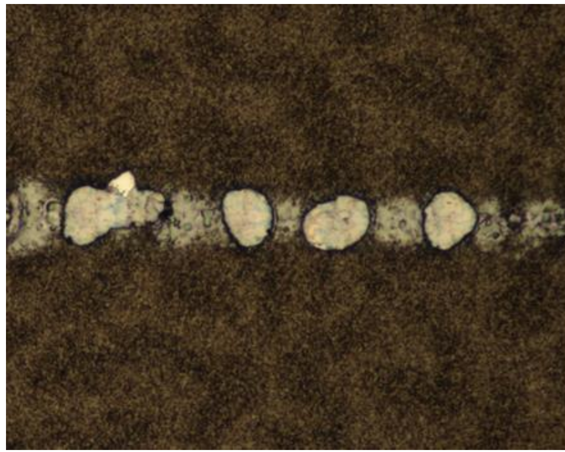


Figure 3.54: The result of scribing U1 CIGS with the parameters developed on sample C1. There is an intermittent process connected by regions of melting. This is the closest to a working process that was found after scanning a large range of parameters with a ~30 µm spot size.

Increasing the spot size to ~50 µm an intermittent process was found which removes material up to ~70 µm wide with clean edges suggesting a brittle fracture mechanism. At no point is the process consistent across the sample, the best pulse energy was 12µJ, Figure 3.55. Decreasing the pulse energy the process fell below threshold and increasing pulse energy began to make the Mo bubble and crack. Changing shot overlap also had no positive effect with increased overlap melting the CIGS and decreased shot overlap resulting in local inhomogeneity's in the scribe line, similar to the 30 µm scribe above.

Figure 3.55: Increasing pulse energy of a P2 process on U1 CIGS with a larger spot, nominal size ~50 µm. There is no process which produces consistent acceptable results.

The P3 process on U1 CIGS produced unexpected result where the TCO appears to be removed with a brittle fracture mechanism, Figure 3.56. At a spot size of ~40µm, PRF of 50kHz and a beam speed of 1.5m/s the optimised scribe is at a pulse energy of ~10µJ. There was some evidence of melting in the shot overlap which can be seen more clearly at higher pulse energies, Figure 3.56.

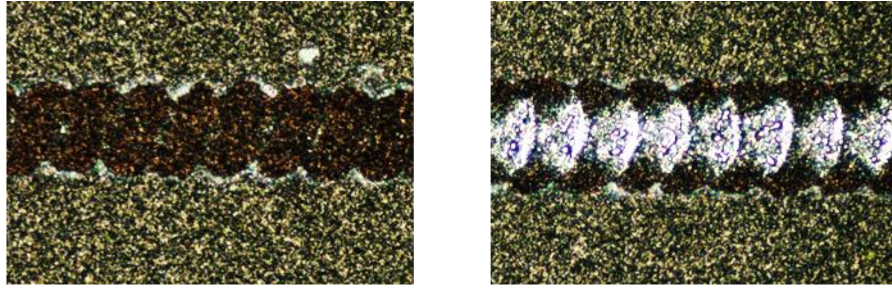


Figure 3.56: Brittle fracture of AZO on full stack U1 samples with the 1550 nm laser. Left; optimised scribe with little CIGS melting (~10 μJ), Right; higher energy scribe showing melting in overlapping regions. This process was unexpected and appears to be some absorption at 1550 nm between the AZO and CIGS it is likely to be in either the i-ZnO or buffer layer.

SEM images were taken of both the optimised scribe and just below threshold, Figure 3.57. Again there is some evidence of melting at the shot overlap, even when optimised. The image taken just below threshold seems to demonstrate that this is a brittle fracture process with partial lift-off of the remaining AZO. The scribes were electrically tested using test structure 4, the measured resistance was in the order of a few 10's Ω which indicated that they were shunting the CIGS probably due to the melting. Furthermore these scribes, although okay as a P3 scribe for the conventional interconnect would not be a suitable B scribe for OSI.

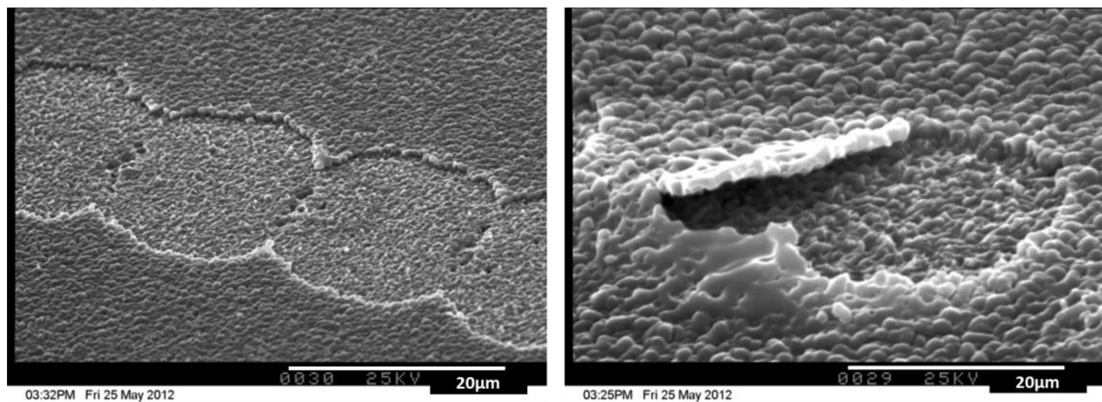


Figure 3.57: SEM images of the unusual P3 process on U1 CIGS with the 1550 nm laser. The TCO is cleanly removed from the top of the stack, the mechanism appears to be a brittle fracture type process.

3.6.5 Modelling of CIGS scribing process

It has been demonstrated that the brittle fracture process at 1 and 1.5μm can be performed with a <5ns pulsed laser, however the process is not universally applicable to all phases of CIGS and can have a small process window. A simple finite element

model was made with COMSOL multi-physics to show the heat distribution generated by this type of 'through the CIGS' scribing process. Taking into account parasitic losses from reflection at interfaces and absorption in the CIGS the laser was modelled as a Gaussian heat source both spatially and temporally. The model was setup for the 1μm, P2 laser process on a glass substrate since absorption coefficients for the various layers were more widely available at 1μm and glass substrates are most common. Layer thicknesses of 340nm Mo and 2μm CIGS were chosen as these values are similar to the experimentally tested materials.

Initially the material stack is at thermal equilibrium at 293K. The modelled laser parameters were chosen based on the experiments with the IPG laser and were 1ns pulse duration and 10μJ pulse energy, only a single shot is modelled since all investigated CIGS brittle fracture processes have been shown to work best at low shot overlap, <40%. An important difference between the model and reality is that the modelled absorption coefficients are not temperature dependant, including this temperature dependence would be a logical next step for the model [25].

Figure 3.58 shows the temporal evolution of the molybdenum temperature at the CIGS/Mo interface in this model. It is interesting to note that the maximum attained temperature of ~920 K is close to the vaporisation temperature of selenium, 958K. In some CIGS cells it has been common to have a Se rich layer next to the Mo, it has been postulated that it is perhaps the Se layer which is vaporised causing the brittle fracture. This also explains why it is easy to shunt the CIGS by melting since the vaporisation temperatures of the Cu, In and Ga are much higher (>2000°C) hence it is easy to remove the Se and leave a metal complex.

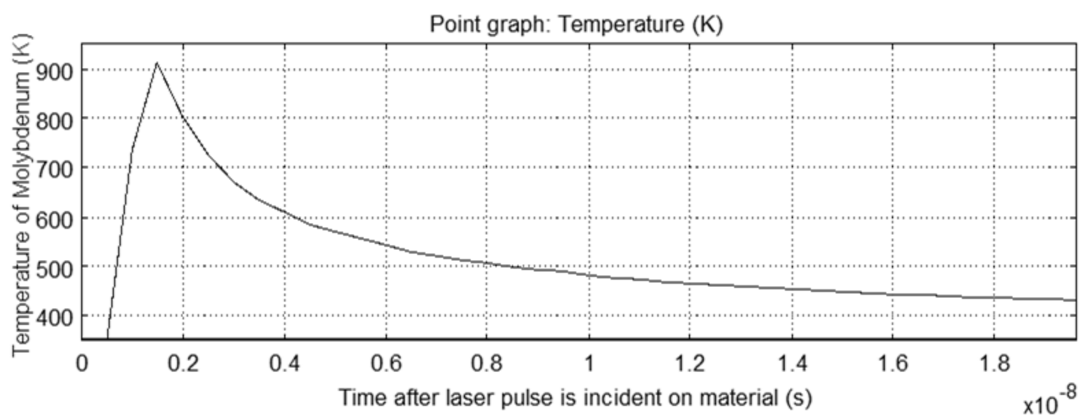


Figure 3.58: Temperature evolution at Mo/CIGS interface during illumination by a 1ns laser pulse at a wavelength of 1μm. It can be seen that the maximum achieved temperature is similar to the vapourisation temperature of selenium.

In contrast Figure 3.59 shows the equivalent temperature evolution in the centre of the CIGS layer, it can be seen that due to the low absorption the temperature stays relatively low, <400K. This is where the model breaks down however because a temperature increase will cause a higher free carrier density and thus increase the absorption coefficient in the IR which is primarily due to free carrier absorption [26], [27].

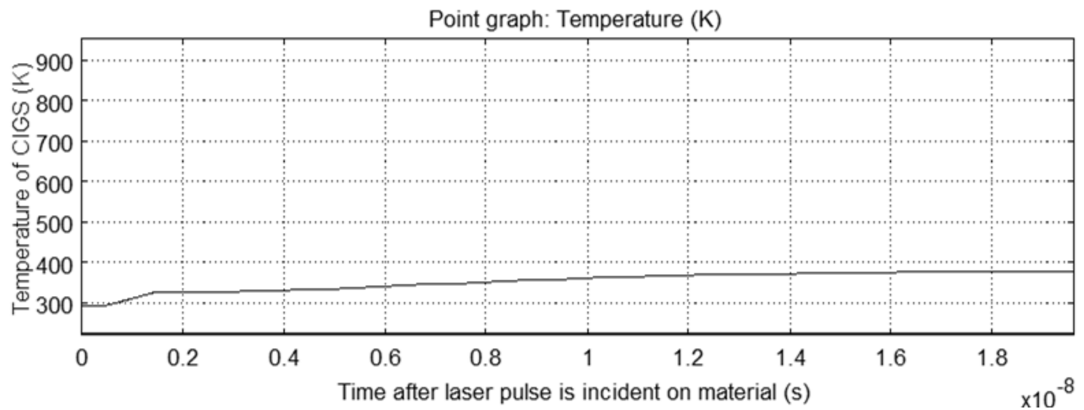


Figure 3.59: Temperature evolution of bulk CIGS during illumination with 1 ns, 1μm laser pulse. The temperature rise is small due to the low absorption coefficient of CIGS at this wavelength.

The 2D plots in Figure 3.60 show the temperature evolution from steady state for the first 3ns after the laser is incident. It can be seen that all of the absorption is at the Mo/CIGS interface and that the thermal diffusion is into the CIGS layer rather than into the glass but, as noted above, the temperature reached by the bulk CIGS is low. The peak temperature is attained at the Mo/CIGS boundary as expected.

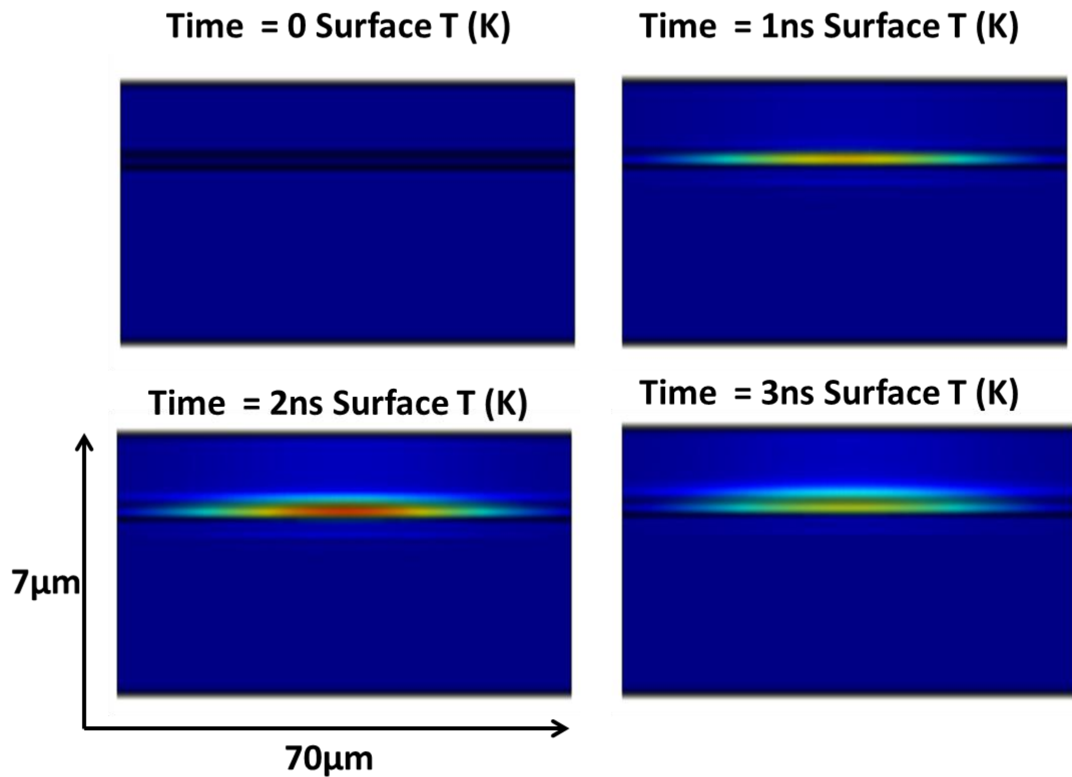


Figure 3.60: 2D diagrams of the glass/Mo/CIGS stack from the FE model. The temperature evolution immediately after the pulse is shown to be predominantly at the Mo/CIGS boundary with some thermal diffusion into the CIGS.

3.6.6 CIGS Conclusions

Laser processes for CIGS have been found at both 1µm and 1.5µm, however at both wavelengths the process is dependent on the exact phase of the CIGS. It has been shown with some simple modelling that a brittle fracture 'through the CIGS' process is possible. There are many possible extensions to this work both experimental and modelling. The next step experimentally would be to form a close collaboration with a CIGS manufacturer who could produce many phases of CIGS which can be tested to see if they work with these laser processes. This would allow the process window in terms of CIGS composition to be defined and through cross referencing with absorption spectra in the near IR of all the materials, allow a clearer picture to be built up of the dependencies of this process. In terms of modelling there are many ways of extending this simple beginning. Firstly, including the AZO and any buffer layers would allow modelling of the P3 process. It would also be useful to include the temperature dependence of the absorption coefficient and perhaps include mechanical modelling to

determine stress and strain in the films and see how that varies with temperature. Furthermore it would be interesting to model what happens at 1550nm and perhaps further into the infrared although this would require collection of data on absorption coefficients of all layers at those wavelengths.

It is worth noting that shortly after this work was carried out, supplier C1 changed their CIGS recipe and the brittle fracture process with both the Pyro Photonics, IPG and MW lasers stopped working. It is speculation at this stage but it could be due to a move to a graded band-gap type device which has become more common in high efficiency CIGS [28].

3.7 References

[1] M. Bär, S. Nishiwaki, L. Weinhardt, S. Pookpanratana, W. N. Shafarman, and C. Heske, “Electronic level alignment at the deeply buried absorber/Mo interface in chalcopyrite-based thin film solar cells,” *Appl. Phys. Lett.*, vol. 93, pp. 13–16, 2008.

[2] N. Naghavi, D. Abou-Ras, N. Allsop, N. Barreau, S. Bücheler, a. Ennaoui, C. H. Fischer, C. Guillen, D. Hariskos, J. Herrero, R. Klenk, K. Kushiya, D. Lincot, R. Menner, T. Nakada, C. Platzer-Björkman, S. Spiering, a. N. Tiwari, and T. Törndahl, “Buffer layers and transparent conducting oxides for chalcopyrite Cu(In,Ga)(S,Se)2 based thin film photovoltaics: Present status and current developments,” *Prog. Photovoltaics Res. Appl.*, vol. 18, no. April, pp. 411–433, 2010.

[3] K. L. Chopra, P. D. Paulson, and V. Dutta, “Thin-film solar cells: an overview,” *Prog. PV Res. Appl.*, vol. 12, no. 23, pp. 69–92, Mar. 2004.

[4] C. Dunsky and F. Colville, “Solid state laser applications in photovoltaics manufacturing,” *SPIE Proc.*, vol. 6871, no. Solid State Lasers XVII, p. 687219, 2008.

[5] P.-O. Westin, U. Zimmermann, M. Ruth, and M. Edoff, “Next generation interconnective laser patterning of CIGS thin film modules,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 4, pp. 1062–1068, Apr. 2011.

[6] F. J. Pern, L. Mansfield, S. Glynn, B. To, C. Dehart, M. Rekow, R. Murison, T. Panarello, C. Dunsky, N. Renewable, and P. Lasers, “ALL-LASER SCRIBING FOR THIN-FILM CuinGaSe2 SOLAR CELLS,” *Sol. Cells*, pp. 3479–3484, 2010.

[7] M. Rekow, R. Murison, C. Dunsky, C. Dinkel, J. Pern, L. Mansfield, T. Panarello, and S. Nikumb, “CIGS P1, P2, P3 Scribing Processes using a Pulse Programmable Industrial Fiber Laser,” 2010.

[8] N. G. Dhere, “Toward GW/year of CIGS production within the next decade,” *Sol. Energy Mater. Sol. Cells*, vol. 91, no. 15–16, pp. 1376–1382, Sep. 2007.

[9] N. Dahotre and S. Harimkar, *Laser Fabrication and Machining of Materials*. 2007, pp. 55–59.

[10] J. Bovatsek, a. Tamhankar, R. S. Patel, N. M. Bulgakova, and J. Bonse, “Thin film removal mechanisms in ns-laser processing of photovoltaic materials,” *Thin Solid Films*, vol. 518, no. 10, pp. 2897–2904, Mar. 2010.

[11] S. Haas, G. Schöpe, C. Zahren, and H. Stiebig, “Analysis of the laser ablation processes for thin-film silicon solar cells,” *Appl. Phys. A*, vol. 92, no. 4, pp. 755–759, May 2008.

[12] D. Britton, a. Hempel, M. Härting, G. Kögel, P. Sperr, W. Triftshäuser, C. Arendse, and D. Knoesen, “Annealing and recrystallization of hydrogenated amorphous silicon,” *Phys. Rev. B*, vol. 64, no. 7, pp. 1–8, Jul. 2001.

[13] A. S. Steve Golay, Johannes Meier, Sébastien Dubail, Ulrich Kroll, “Laser scribing of p-i-n/p-i-n ‘micromorph’ (a-Si:H/μc-Si:H) tandem cells,” *Small*, pp. 3–6, 2000.

[14] V. Avrutin, N. Izyumskaya, and H. Morkoç, “Semiconductor solar cells: Recent progress in terrestrial applications,” *Superlattices Microstruct.*, vol. 49, no. 4, pp. 337–364, Apr. 2011.

[15] S. Haas, S. Ku, and K. Du, “Patterning of thin-film silicon modules using lasers with tailored beam shapes and different wavelengths,” *Proc. 23rd Eur.*, 2008.

[16] P. K. Nayak, G. Garcia-Belmonte, A. Kahn, J. Bisquert, and D. Cahen, “Photovoltaic efficiency limits and material disorder,” *Energy Environ. Sci.*, vol. 5, p. 6022, 2012.

[17] A. Virtuani, D. Pavanello, and G. Friesen, “Overview of temperature coefficients of different thin film photovoltaic technologies,” in *25th European Photovoltaic Solar Energy Conference and Exhibition*, 2010, pp. 4248 – 4252.

[18] H. Peelaers, E. Kioupakis, and C. G. Van de Walle, “Fundamental limits on optical transparency of transparent conducting oxides: Free-carrier absorption in SnO2,” *Appl. Phys. Lett.*, vol. 100, no. 1, p. 011914, 2012.

[19] D. E. Swanson, R. M. Geisthardt, J. T. McGoffin, J. D. Williams, and J. R. Sites, “Improved CdTe Solar-Cell Performance by Plasma Cleaning the TCO Layer,” *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 838–842, Apr. 2013.

[20] G. Kartopu, A. . J. Clayton, W. S. M. Brooks, S. D. Hodgson, V. Barrioz, A. Maertens, D. A. Lamb, and S. J. C. Irvine, “Effect of window layer composition in Cd1-xZnxS/CdTe solar cells,” *Prog. Photovoltaics Res. Appl.*, vol. 22, no. 1, pp. 18–23, 2014.

[21] G. Kartopu, A. A. Taylor, A. J. Clayton, V. Barrioz, D. A. Lamb, and S. J. C. Irvine, “CdCl2 treatment related diffusion phenomena in Cd1-xZnxS/CdTe solar cells,” *J. Appl. Phys.*, vol. 115, p. 104505, 2014.

[22] S. L. Rugen-Hankey, a. J. Clayton, V. Barrioz, G. Kartopu, S. J. C. Irvine, J. D. McGettrick, and D. Hammond, “Improvement to thin film CdTe solar cells with controlled back surface oxidation,” *Sol. Energy Mater. Sol. Cells*, pp. 1–5, Jan. 2015.

[23] R. Murison, C. Dunsky, M. Rekow, C. Dinkel, J. Pern, L. Mansfield, T. Panarello, and S. Nikumb, “CIGS P1, P2, and P3 laser scribing with an innovative fiber laser,” *2010 35th IEEE Photovolt. Spec. Conf.*, pp. 000179–000184, Jun. 2010.

[24] M. Contreras, L. Mansfield, B. Egaas, J. Li, M. Romero, S. Ag, E. Rudiger-voigt, and W. Mannstadt, “Improved Energy Conversion Efficiency in Wide-Bandgap Cu (In , Ga) Se2 Solar Cells Preprint,” no. July, 2011.

[25] G. E. Jellison and D. H. Lowndes, “Optical absorption coefficient of silicon at 1.152 ?? at elevated temperatures,” *Appl. Phys. Lett.*, vol. 41, no. 1982, pp. 594–596, 1982.

[26] J. PankoveI., *Optical processes in semiconductors*. 1971.

[27] D. K. Schroder, R. N. Thomas, and J. C. Swartz, “Free carrier absorption in silicon,” *IEEE Trans. Electron Devices*, vol. 25, pp. 180–187, 1978.

[28] K. Decock, J. Lauwaert, and M. Burgelman, “Characterization of graded CIGS solar cells,” *Energy Procedia*, vol. 2, no. 1, pp. 49–54, 2010.

Chapter 4 : Inkjet printing for OSI

The second process which required development for OSI is inkjet deposition of the two functional materials, insulator and conductor. The purpose of the insulator is to prevent shorting of the A scribe which would shunt the cell, where as the conductive ink forms a bridge connecting the front and back contacts in scribe B. The two processes are the same for superstrate and substrate cells. A diagram of the OSI interconnect in the substrate case can be seen in Figure 4.1.

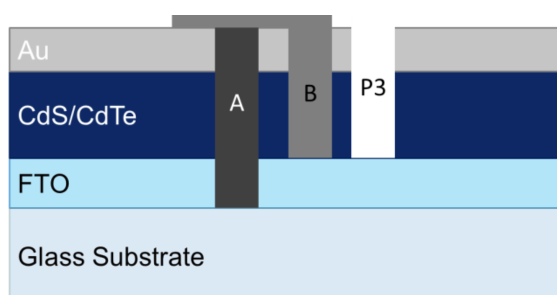


Figure 4.1: The complete OSI interconnect on a substrate cell. The two inkjet processes fill in scribe A with an insulative ink and bridge from the B scribe to the back contact with a conductive ink.

Inkjet deposition is capable of depositing drops of ink in a repeatable manner and with high accuracy (exact specifications are given in the experimental section below). It is however important that the interaction of the inks with the substrate is favourable and for a process to be possible, the inks must meet the following criteria:

Insulator

- Be jetable with industrial inkjet heads at high speed (>0.5m/s)
- Form a solid, non-permeable barrier to the conductive ink
- Be confined within the A scribe

Conductor

- Be jetable with industrial inkjet heads at high speed (>0.5m/s)
- Form a continuous track between the front and back contact
- Have a low total resistance so as not to impact on the cells fill factor

This chapter includes experimental setup, ink qualification and specific sections on processes for insulating and conducting inks.

4.1 Experimental Setup

4.1.1 Print Hardware

The same M-Solv R&D platform, coded MSV101, with the 3-axis stages, on which the lasers and optics were mounted also housed the inkjet hardware. The print system consists of two Fujifilm Dimatix Sapphire QS-256/xx AAA drop on demand (DoD) piezo actuated print heads where xx is the nominal drop volume in pL and 10, 30 and 80 pL heads are available. 256 is the number of nozzles per head, each nozzle is spaced by 254μm giving a native resolution of 100dpi. Figure 4.2 is an image of one of the printheads connected to an M-Solv made electronics printer.

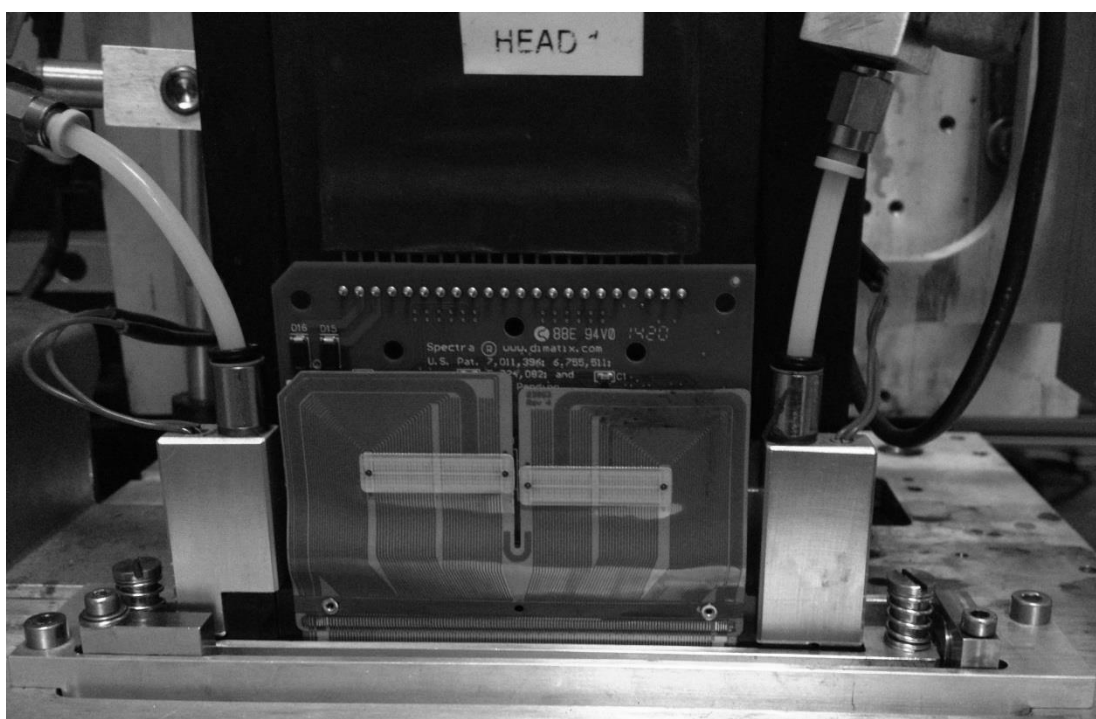


Figure 4.2: A Fujifilm Dimatix Sapphire printhead. The head is high accuracy and capable of running at drop ejection frequencies of up to 30kHz allowing printing at high speed.

The key reason for choosing the Dimatix Sapphire was high drop placement accuracy, which is <10μm at 0.5mm head standoff. The printheads were driven by electronics manufactured by Global Inkjet Systems (GIS). The drive electronics consist of 1 print manager board, 2 head personality boards and an amplifier, this combination allows both heads to be operated simultaneously with different drive voltage profiles and different drop ejection frequencies.

As well as the printheads an Omnicure S2000 fibre fed UV mercury lamp was integrated for inline curing of the insulating inks. The fibre is positioned between the

two printheads allowing inline insulator deposition, cure and conductor deposition in a single pass.

4.1.2 Drop Watching

In order to jet a new ink it is necessary to develop the voltage waveform applied to the piezo within the printhead. The basic waveform is a trapezoid with 4 parameters to vary, rise, hold and fall times and voltage, Figure 4.3.

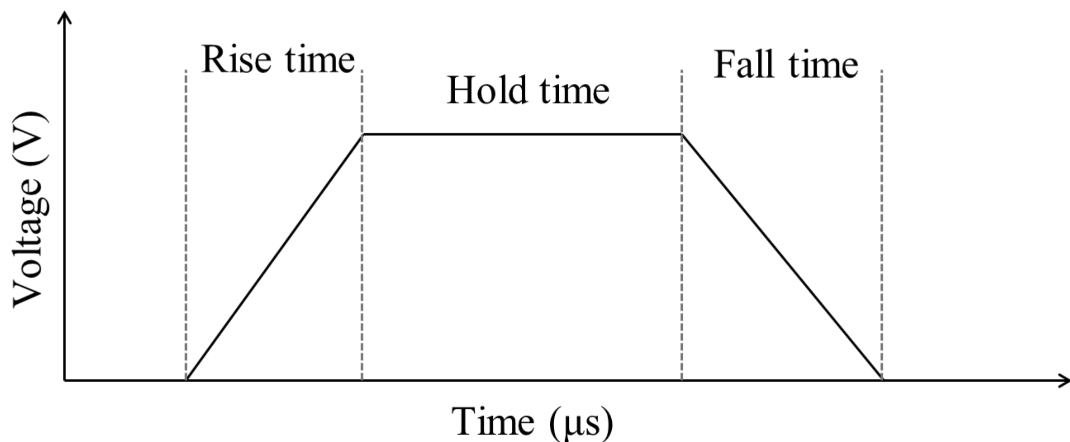


Figure 4.3: The basic waveform applied to the piezo actuators within the Sapphire printhead. The optimum values are dependent on the head geometry and the fluid properties.

The methodology for optimising the waveform uses a technique called 'drop watching' in which a light source was synchronised to the drop ejection and used to illuminate the bottom of the nozzle plate which was then recorded with a camera. Typical drop ejection frequencies are 1-20kHz and the frame rate of the camera is typically ~30FPS therefore each frame contains the average of many drops. Since inkjet is highly repeatable the result is a clear image of the droplet ejection. Drop watching is discussed in more detail in Chapter 2. By varying the applied waveform and watching the resulting change to the droplet ejection it is possible to optimise the waveform. The waveform is dependent on the internal printhead geometry and therefore the same type of head must be used for both drop watching and printing. The dynamics of inkjet printing are further described in Chapter 2. The drop watching setup built at M-Solv uses an overdriven LED light source with pulse durations of <1µs and Matrox smart camera, an illustration of the setup can be seen in Figure 4.4. The trigger signal for the

LED is fed from the inkjet electronics via a delay generator which allows the drop to be visualised at different points after droplet ejection.

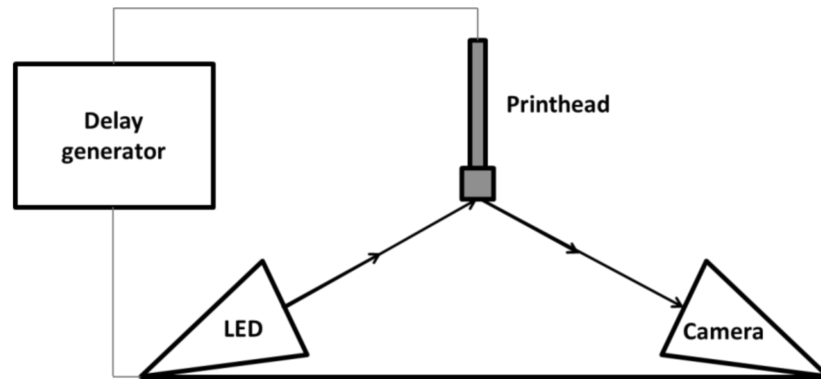


Figure 4.4: A schematic of the drop watcher built at M-Solv. The print signal is fed through a delay generator and used to trigger the LED so it flashes at a defined time after droplet ejection. The camera captures the image using the LED, each frame contains the average of many drops. By varying the delay applied to the trigger signal it is possible to image the droplet at different positions during formation and flight.

Finding the optimum waveform for droplet ejection can be broken down into a standard process flow. Firstly the hold time was optimised. The optimum hold time corresponds to approximately twice the travel time for an acoustic wave to propagate the length of the nozzle channel, as discussed in Chapter 2. The wave is generated in the centre of the channel, propagates in both directions to the ends of the channel where it is reflected and then meets in the middle where it is reinforced by the channel relaxing, see Chapter 2 for more details. The optimum hold time generates the fastest moving drop or at the same delay between fire signal and strobe the drop that travels the furthest from the nozzle plate. A plot of drop location against hold time for a test ink can be seen in Figure 4.5, the optimum in this case is ~3.25μs.

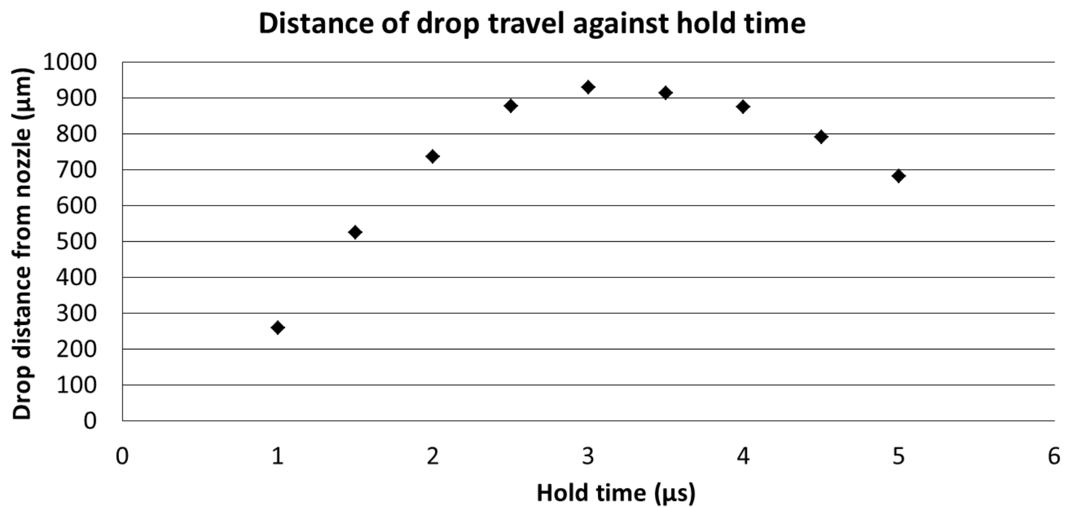


Figure 4.5: A plot of drop distance from the printhead against hold time. The optimum hold time produces the fastest moving drop which is equal to the maximum distance travelled from the head for a fixed delay. In this case the optimum hold time is ~3.25μs.

The next step is optimisation of the voltage to achieve the desired drop volume. The drop volume is proportional to the displacement of the piezo within the printhead, a larger displacement causes a larger droplet to be expelled. Measuring drop volume directly is difficult but using a high solid fraction ink, such as a UV cure dielectric which is ~95% solids by volume, the drop volume from the head can be estimated. Plotting the voltage against the impacted drop diameter, for drops deposited on a constant surface with all other waveform parameters being held constant reveals information about the volume of ink. A plot of voltage against drop diameter can be seen in Figure 4.6.

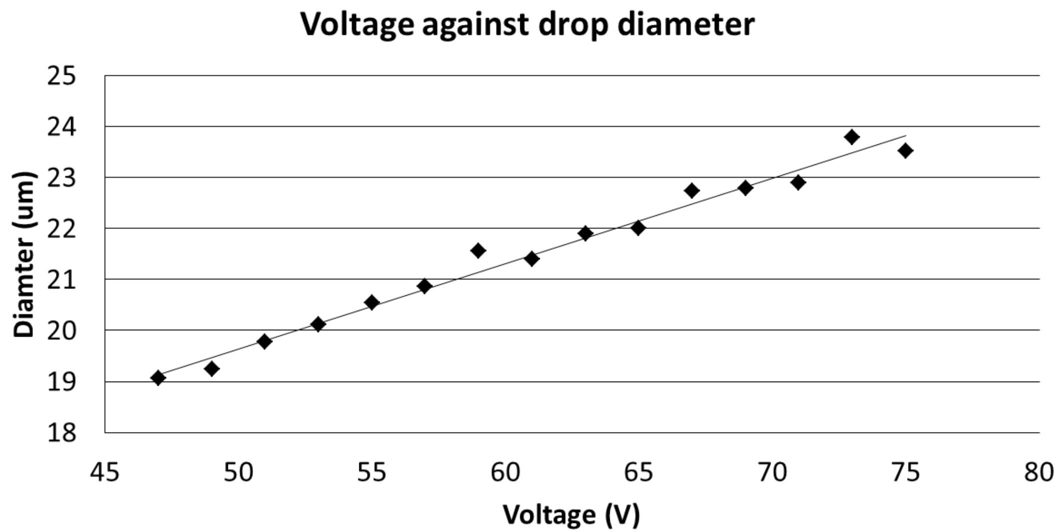


Figure 4.6: A plot of drop diameter on a planar substrate against waveform voltage. It can be seen that the drop diameter varies linearly with the applied voltage.

Modelling the drop as a spherical cap the volume can be calculated by measuring the drop height using the Zygo white light interferometer. Figure 4.7 and Equation 1 show how to calculate the volume of a spherical cap.

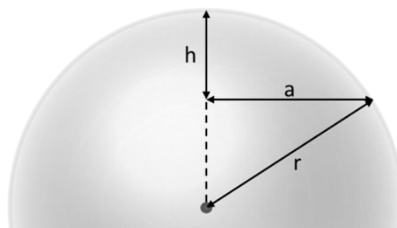


Figure 4.7: The dimensions used to calculate the volume of a spherical cap used to determine the drop volume from the printhead.

(1) $$V = \frac{\pi h}{6}(3a^2 + h^2)$$

This was done for the largest and smallest drop diameters, assuming that the linear relationship holds and compensating for the 95% of solids remaining after cure gives the relationship between voltage and drop volume.

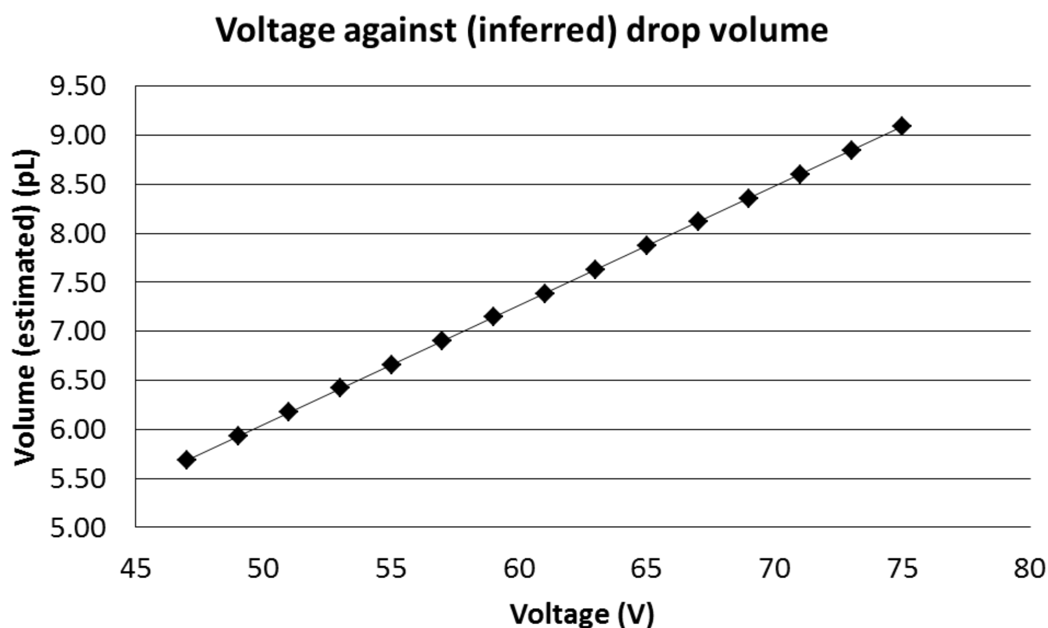


Figure 4.8: Plot of voltage against calculated drop volume.

This shows that the drop volume varies according to the voltage applied to the print head. To calculate drop volume for a low solid loading ink such as the conductive nanoparticle suspensions it is possible to jet a known (in the order of $1x10^6$) number of drops into the pan of an accurate scale and determine the volume from the weight and density however the equipment required for this was not available at M-Solv. Fortunately the drop volume of the conductive ink is less critical as the requirement is to form a continuous film rather than to accurately fill a scribe. The voltage also affects the average velocity of the ejected drops so for the low solid loading inks the voltage was optimised by obtaining the maximum drop velocity, or highest voltage, that allowed jetting without satellite formation corresponding to the maximum drop volume which is optimum for area coverage. Figure 4.9 shows the effect of increasing drop voltage on the jetting of a conductive nanoparticle suspension. The maximum voltage which allowed good drop formation was selected.

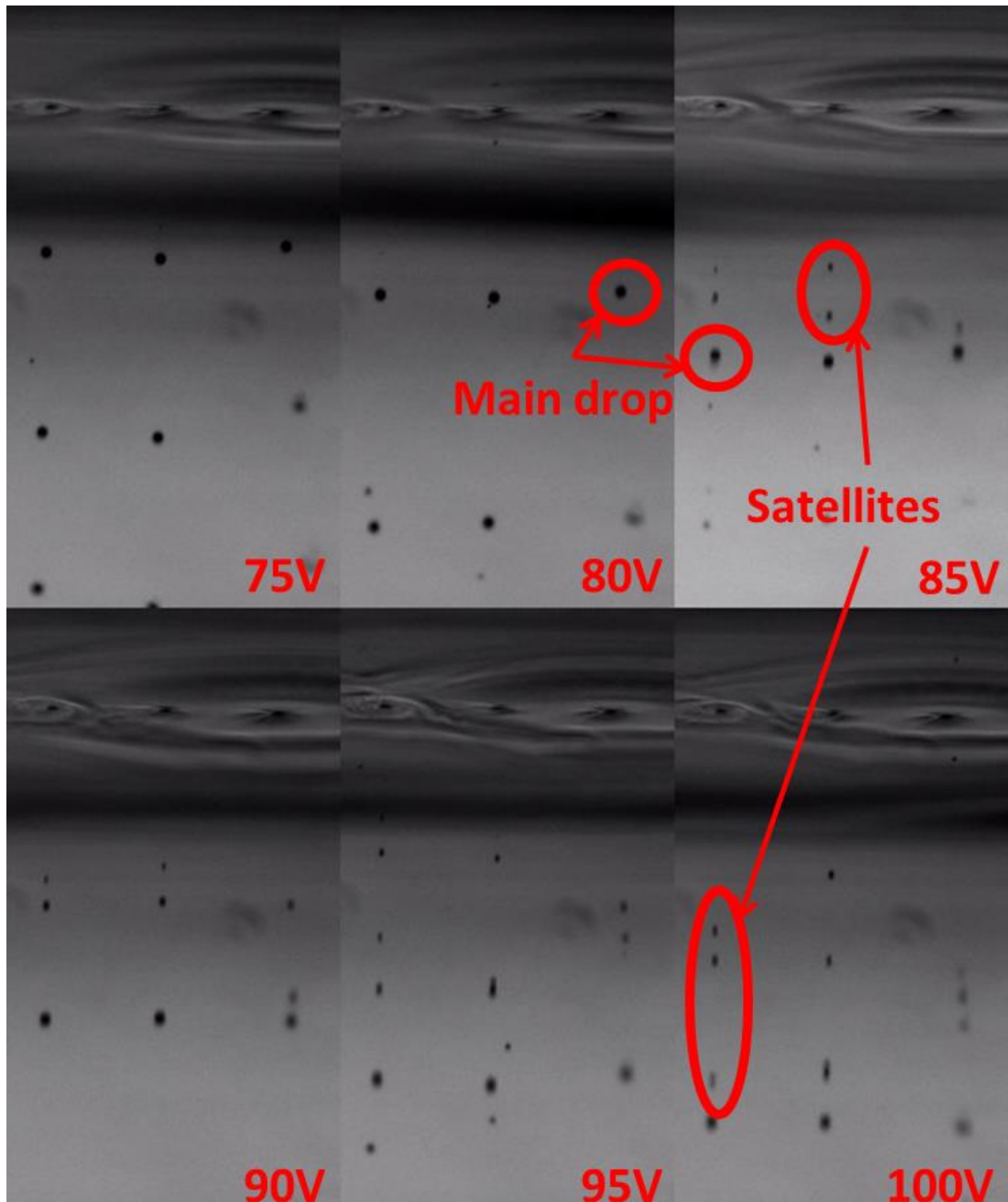


Figure 4.9: The effect of increasing drop volume on the jetting of a conductive nanoparticle ink. Satellite formation occurred at higher voltages and can be seen in the image as trailing, smaller drops behind the main drop. The maximum voltage which allowed jetting without satellite formation was ~80V.

Rise and fall time are the last to be optimised and are used to reduce satellite formation by reducing the distance the drop travels before becoming spherical. As the times increase the drops have less energy, form shorter tails and therefore less satellites. However at the upper limit drop velocity decreases and ejection becomes unstable. An optimum must be found with good drop shape and reliable jetting. Figure 4.10 shows the rise and fall times being increased together in 0.5μs steps. The optimum value was determined to be between 3.5-4 μs.

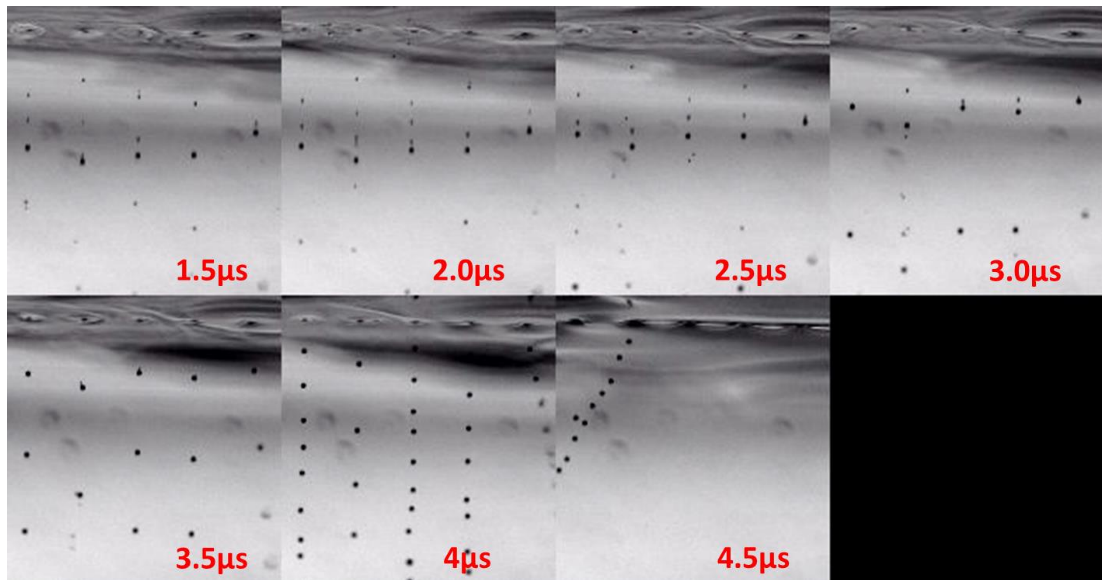


Figure 4.10: The effect of increasing rise/fall times on the jetting of a conductive nanoparticle suspension, the optimum rise/fall time was chosen to be 3.75 µs.

Before testing an ink for OSI it goes through drop watching to ensure reliable jetting and good drop formation. The final print however is not guaranteed to be of acceptable quality just because the waveform produces consistent spherical drops without satellites however, the final print is also heavily dependent on the surface cleanliness, homogeneity and surface energy as will be seen in the following sections.

4.2 Insulator deposition

The first functional ink required for OSI is an insulative material to infill the A scribe in order to stop the conductive bridge from shorting the cell. The primary types of ink identified as suitable were a range of graphics inks made up of acrylate monomers which undergo free radical polymerisation when exposed to UV light [1]. The benefits of such inks are high solid content (90-95% by volume), they are well suited to inkjet, there is an abundance of manufacturers and formulations and they are relatively cheap (~£100 per litre). These inks are used for graphics printing on substrates where aqueous inks are not suitable. The ability to UV cure in place after printing allows the formation of small discreet drops on the surface which is suitable for high resolution images and for OSI where the ability to cure inline is a requirement as the conductive ink needs to be deposited immediately.

Many different manufacturers make these types of inks, the two which were primarily used during development were manufactured by Sun Chemical Corp. and Inktec Corp. although others were tested.

4.2.1 Controlling insulator fill

It has been demonstrated above that it is possible to control the deposited drop volume by controlling the waveform however there is another way of controlling amount of ink deposited which is easier to implement and that is changing the drop pitch. In graphics printing it is common to refer to the resolution of an image in dots per inch (DPI) (i.e. number of inkjet drops in an inch long line). A higher DPI gives a higher volume of ink per unit length. In the inkjet control software the drop density was set by specifying a DPI however within this work DPI will not be used but rather drop pitch which is equal to 25.4mm (or 1”) divided by DPI.

The insulative inkjet deposition within the A scribe forms a surface which subsequently receives the conductive ink. The morphology of the insulator filled scribe is therefore important for the quality of the conductive print. If the insulator is under filled the conductor tended to pool in the centre of the scribe leading to thin layers along the scribes edges. If the insulator overfills the scribe then conductor tended to run off from the peak and leave a thin layer in the centre. Continuous thin areas of conductor cause high series resistance. It is therefore important to optimise the volume of insulator deposited so as to just fill the scribe. Figure 4.11 shows examples of different insulator fill depths measured with a Zygo scanning white light interferometer (SWLI).

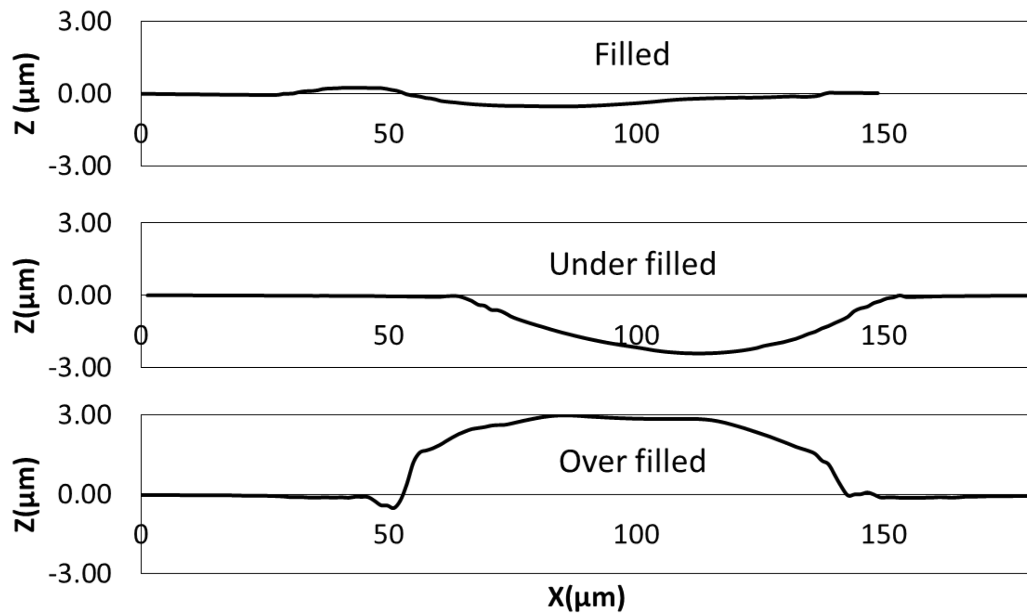


Figure 4.11: Examples of surface profiles measured with a Zygo white light interferometer of different insulator fill depths.

It is relatively straightforward to calculate the volume of insulator required to fill a scribe since all dimensions are known. Drop volume can be measured and the solid content by volume is known it is possible to calculate the required drop pitch for a complete fill. Figure 4.12 shows both calculated and measured drop pitch against scribe fill depth with the scribe height marked. The measured values are low compared to the calculated ones at low drop pitch because the ink is no longer contained by the scribe and runs onto the surrounding surface. There is also some error in the measured value caused by non-flatness in the print, the average height has been judged from the interferometer plots with an associated error.

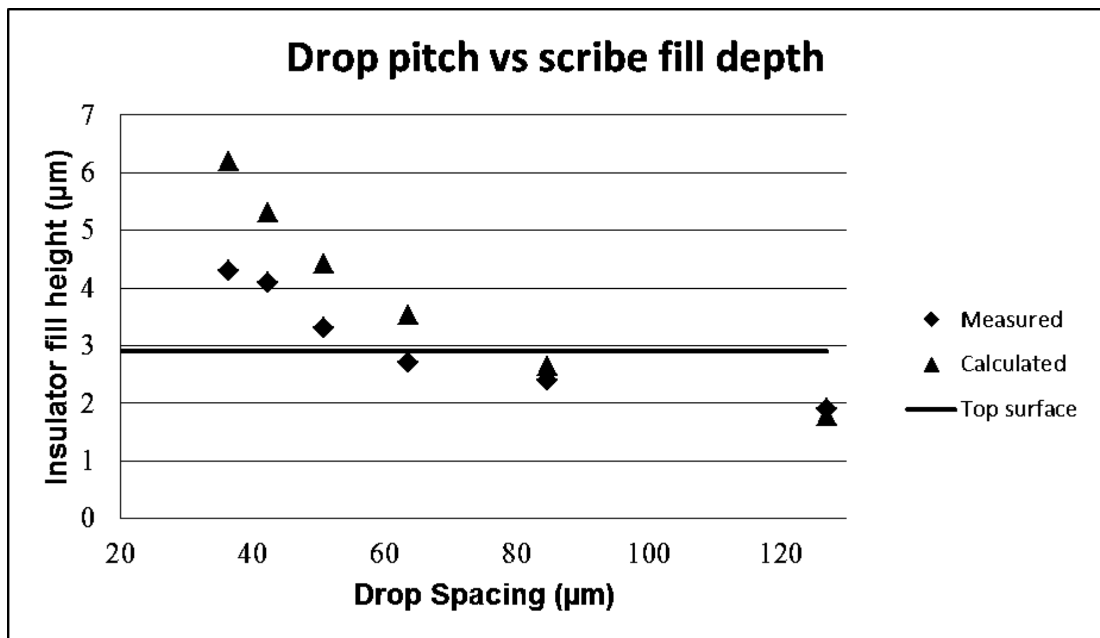


Figure 4.12: Plot of measured and calculated fill height against drop pitch. The top surface of the scribe is shown in red. At lower drop pitches, or higher volumes, the two values diverge. This is due to losing some ink onto the surface in the measured case.

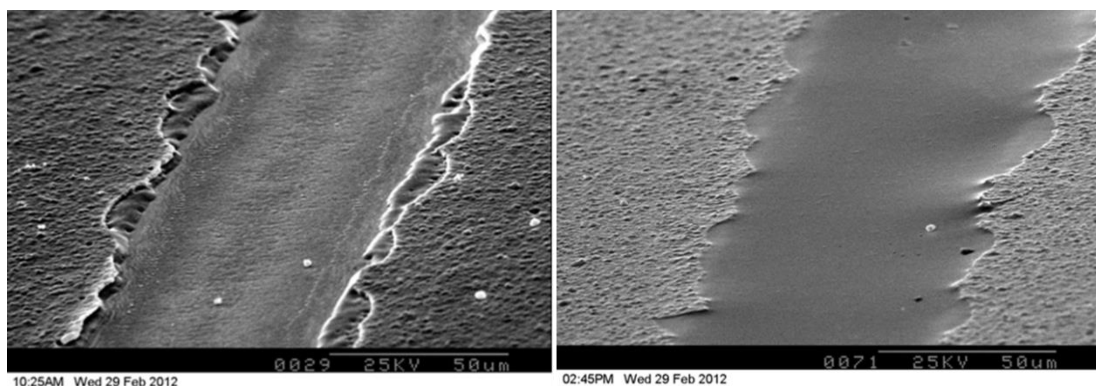


Figure 4.13: SEM images of Left; empty and Right; filled scribes on a customer's TF-PV stack.

4.2.2 Insulator thermal stability

The ink initially used for development of OSI was supplied by Sun Chemical (U7878 - a black acrylic based UV cure graphics ink). The black colour is due to the addition of a carbon black filler. After the first round of testing it was found that the volume of the insulator changes during sintering of the conductive ink, 250°C anneal for 15minutes. This volume change was detrimental to the mechanical stability of the conductive print. SEMs of the conductive coating appear to show some micro-cracks which were thought to be due to the insulator volume change, see Figure 4.14.

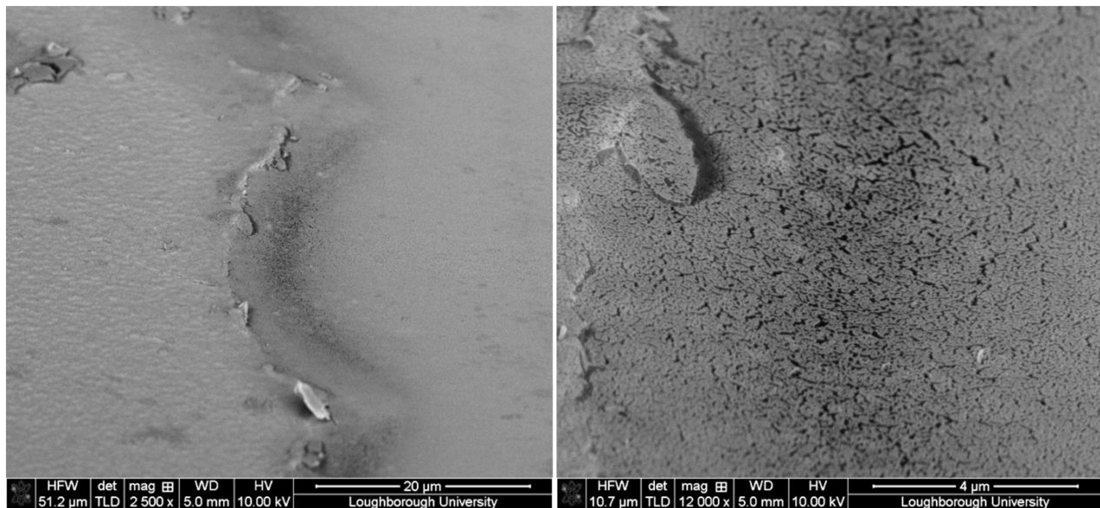


Figure 4.14: SEM image of micro-cracks in the conductive print. It is thought that these were related to the insulator moving during the conductive sintering process.

The total volume change was measured using the SWLI to inspect the same locations before and after the thermal treatment, the change in volume was calculated as the reduction in height of the insulator at predefined points between the two measurements. The average of three points was taken per scribe. U7878 was found to reduce in volume by ~22% after the thermal treatment. Figure 4.15 shows interferometer plots of a filled scribe both before and after a bake at 250°C for 15minutes, the volume reduction is clear.

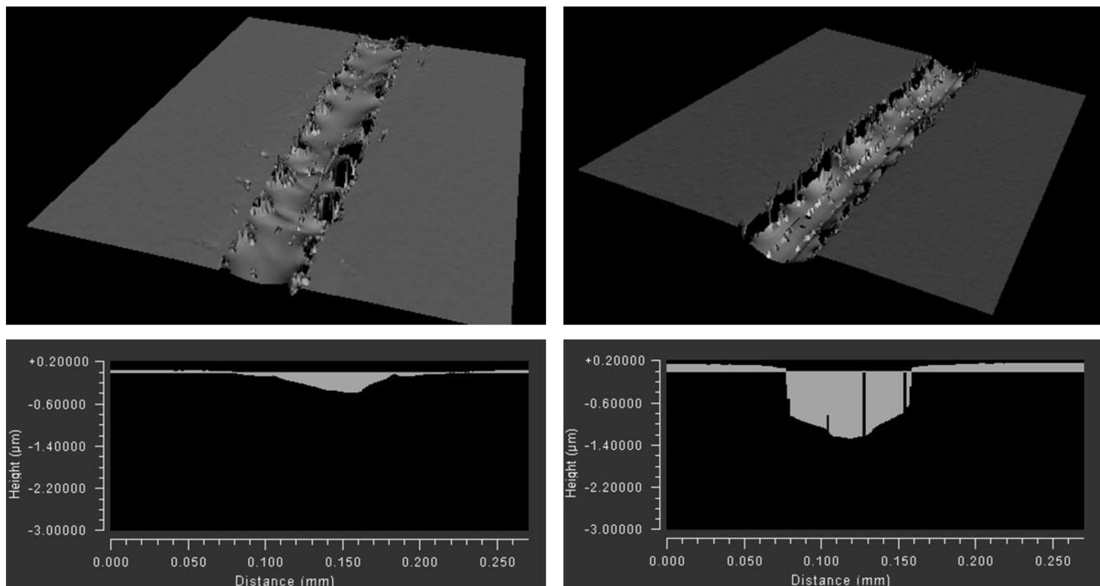


Figure 4.15: White light interferometer plots of an insulator filled scribe before and after the thermal treatment required to sinter the conductive ink.

Two other inks from Sun Chemical Corp. were also tested to see if they exhibited similar behaviour. The first was U6145 which was a clear acrylic UV cure ink, the

chemistry was the same as U7878 without any the additional carbon black filler. This ink was chosen to determine if the volume loss was from removal of the pigment or the base ink. The second ink tested was U8517 which is a white UV cure acrylic ink, again the base material is the same but the white ink is loaded 20% by weight TiO_2 which gives the white colour. Both exhibited volume loss during the thermal process of differing percentage volumes, the clear ink ~30% and the white ~15%.

There are two mechanisms that could be responsible for the reduction in volume, either mass loss through evaporation of volatile material or an increase in density due to improved crosslinking. Both mechanisms were thought to be possible therefore Thermogravimetric Analysis (TGA) was used to measure the mass loss during the sintering treatment. TGA involves heating a small amount of a material on an accurate balance and measuring the change in mass. Samples of each of the three inks were deposited and cured in the usual way and sent to the University of Surrey for TGA. The result of all three inks can be seen in Figure 4.16. At 250°C the black has lost 16.4% mass, the white 10.9% and the clear 6.5%. From this, assuming that the remaining volume change is due to increased crosslinking and therefore an increased density, the amount of volume change due to density increase was calculated. The results for all three inks can be seen in Table 4.1.

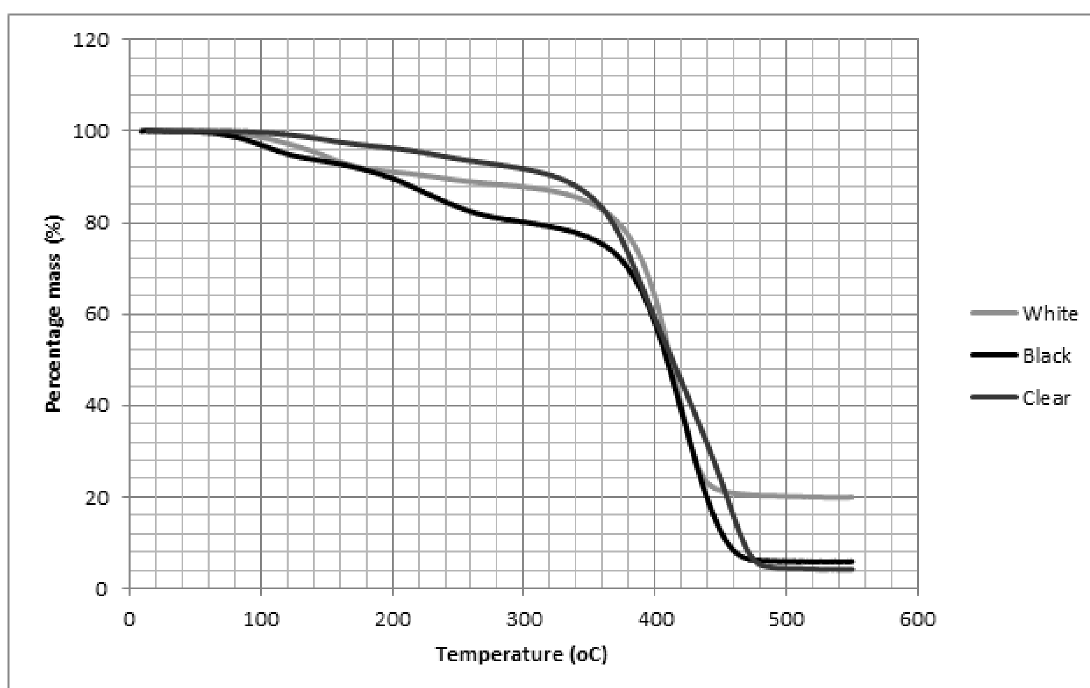


Figure 4.16: TGA of three insulative inks made by Sun Chemical. All three inks use the same acrylic base, the black and white inks contain pigments of carbon black and TiO_2 respectively.

Ink	Δ Volume (%)	Mass Loss (%)	Shrinkage (%)
Black	22	16.4	5.6
Clear	30	6.5	23.5
White	15	10.9	4.1

Table 4.1: A summary of the total volume reduction of three Sun Chemical Corp. inks.

According to the manufacturer the clear ink is expected to be the most reactive and therefore exhibits the highest crosslink density which explains the high degree of volume loss with the clear despite the low mass loss. The pigmented inks are less reactive hence the mass loss is greater since the polymer is less well bound. The supplier suggested that a higher solid content version of the white ink, 40% by weight may be beneficial for lower total volume reduction. This ink was manufactured and tested but the high solid content made it difficult to find good jetting parameters. In parallel other ink suppliers were sought with more stable formulations, the best one found was a black UV cure ink from Inktec, IUSSLB01, with a total volume loss of 11% measured with the SWLI. Inktec did not allow TGA of their ink therefore it was not possible to do the full analysis to determine the percentage mass/volume loss of their ink. Although 11% change in volume was not optimum it was decided to continue OSI development using Inlktec Black, IUSSLB01, since no better ink was available.

4.2.3 Summary of insulator deposition

A number of insulating inks were optimised for jetting and tested for OSI. Good control of total volume of ink deposited is demonstrated by adjusting the droplet pitch. A further issue was highlighted with respect to temperature stability with all UV cure inks which showed a propensity to lose volume when undergoing a thermal process equivalent to the maximum temperature requirement for sintering conductive inks. However, there are inks which can be sintered at lower temperatures based on organo-metallic complexes, discussed below. Nevertheless, the ink with the greatest thermal stability was the Inktec Black IUSSLB01 and was selected as the preferred ink for OSI development.

4.3 Conductor Deposition

The final stage of OSI is deposition of the conductive track which bridges the two cell contacts. Inkjet printing has again been chosen as the deposition method. Conductive inks are available from a number of manufacturers including Sun Chemical Corp., Inktec Corp., Advanced Nano Products Co. (ANP) and DuPont Ltd. There are two chemistries widely used for conductive inks, the first is a suspension of metal nanoparticles in a carrier fluid [2], typical commercial loadings are 20-40% by weight (~2-5% by volume). The second chemistry uses an organometallic complex to carry the metal which is then reduced leaving a metallic coating, equivalent to a loading of ~12% by mass [3]. During this work both chemistries have been used for OSI however nanoparticle suspensions have formed the majority of the work. Both types of ink require a post deposition thermal treatment in order to become fully conductive. Processes for this curing step which are compatible with production lines and digital manufacture such as laser, electrical and chemical curing have been demonstrated in literature and are discussed in detail in Chapter 2.

The drop watching procedure is used initially on each ink to find optimised jetting parameters. The high solid content of the nanoparticle inks make jetting more difficult but achievable in most case. This problem is compounded by the widespread use of Dimatix Materials Printer (DMP) in printed electronics research which has a wider jetting range, 2-30cps, than industrial printheads such as the Dimatix Sapphire, 8-14cps. Many inks formulated for use with the DMP for printed electronics applications are not optimal for jetting by industrial heads leading to poor performance. This has led to the requirement to work closely with ink manufacturers to further develop their product. Despite this, a number of inks have been successfully jetted and tested for OSI.

Importantly, as well as being jetable, the conductive inks must also form a low resistance pathway between the two contacts. The total resistance comprises of two parts, bulk resistivity of the ink and contact resistance with the front and back contacts. Bulk resistivity is specified by the ink supplier in units of Ω.m or a number of times bulk metal. The most commonly used metal is silver for its combination of low intrinsic resistance and stability. The contact resistance between the ink and the metallic back contact should be Ohmic as long as they are in close contact since both materials are metal. The contact resistance between the conductive ink and the transparent back contact may not be Ohmic since the TCO is a wide bandgap (>3 eV)

highly doped semiconductor [4]. Therefore part of the procedure for conductive ink characterisation for use in OSI has been measurement of the ink TCO contact resistance.

4.3.1 Ink/TCO contact resistance

The Transmission Line Measurement (TLM) technique is commonly used to measure metal/semiconductor contact resistance [5]–[7]. TLM applies a series of metal lines to the semiconductor at different spacing (d), the resistance (R) is measured between lines and then plotted against line spacing. The geometry has been manufactured by inkjet printing a number of lines of sufficient thickness (L) to probe with a multimeter, >500µm. The long lines are divided up into discreet widths (W) using a laser to isolate both the TCO and the printed metal. In this way it is possible to make a number of identical structures all of which are probed and the resistance value averaged to improve the accuracy, in all cases >5 measurements were taken per gap. A typical TLM pattern and plot can be seen in Figure 4.17.

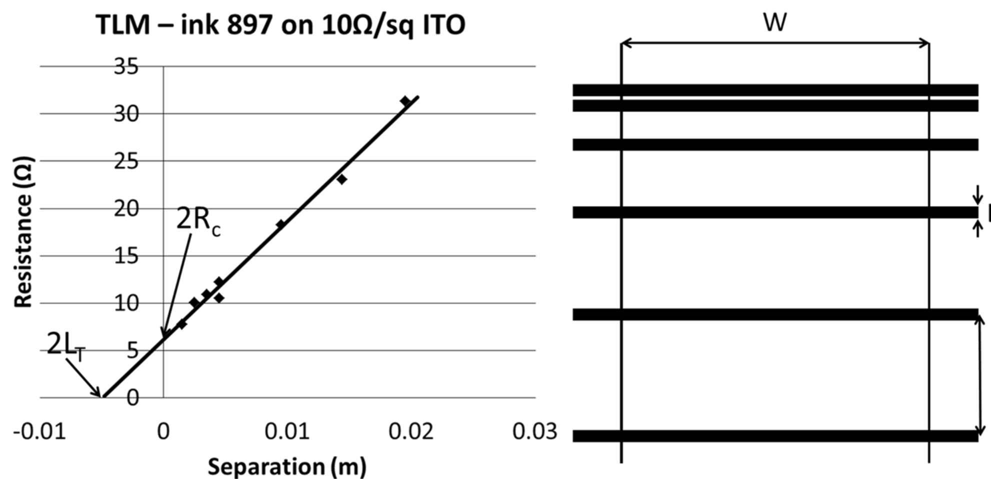


Figure 4.17: Right; A schematic of a TLM pattern for the measurement of metal/ink contact resistance. Left; plot generated from TLM pattern which is used to calculate R_c.

In all cases the data must be processed by fitting a trend line to the plot of resistance (R) against separation (d).

(2) $$R = md + c$$

The gradient (m) of the trend line is directly proportional to the sheet resistance (R_s) of the TCO with the proportionality factor being the line width (W).

(3) $$R_S = mW$$

The contact resistance (R_c) is given by twice the intercept (c) since there are two contacts per measurement.

(4) $$R_C = \frac{c}{2}$$

The transmission length (L_T) is the average length that an electron (or hole) travels in the semiconductor below the printed track before flowing into the metal.

(5) $$L_T = \frac{c}{2m}$$

Contact resistance is specific to the measurement geometry but can be generalised to specific contact resistivity (ρ_c) by multiplying through the contact area. The whole contact length L is not used for current transport, assuming $L>2L_T$, therefore the specific contact resistance uses L_T to determine the effective contact area.

(6) $$\rho_c = R_C L_T W$$

This measurement was made with a number of different ink/TCO pairings, a summary of which can be seen in Table 4.2. In the table ink type is either nanoparticle suspension (NP) or organometallic complex (OM) and the numbers denote different suppliers/formulations.

Measurement No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Ink Type	**NP1**	**NP2**	**NP2**	**NP3**	**OM1**	**NP4**	**NP1**
TCO	**ITO**	**FTO**	**ITO**	**ITO**	**AZO**	**NW**	**NW**
Expected TCO sheet resistance (Ω/sq)	50	10	10	10	?	100	100
Measured TCO sheet resistance (Ω/sq)	52	9	10	12	16	97	96
ρ_c (mOhm.cm^2)	7	35	42	764	624	71	121

Table 4.2: A summary of ink/TCO contact resistance measurements for OSI.

Measurements 1-3 were made as reference standards as these inks have been used to make OSI interconnects with good electrical properties. Measurements 4 and 5 were taken as part of a fault finding process as the interconnects made with these inks showed high series resistance. Measurements 6 and 7 were taken from in house, spray deposited, silver nanowire films as an investigation on the applicability of OSI with next generation transparent conductors.

From these measurements it can be concluded that most nanoparticle inks form a good contact with inorganic TCOs. NP3 was an R&D ink and showed high contact resistance. It also had problems with solid aggregation which also lead to a bulk resistivity of 11x bulk silver, approximately 2x that specified by the manufacturer. A low solid loading in the as-jetted ink may have meant a higher proportion of non-conductive organic filler in the as-cured track, which would explain the high contact resistance. Further optimisation with this ink manufacturer is on-going to address these problems. The contact resistance values on the silver nanowire samples appear to be in the correct order for good electrical quality OSI which is promising for applications involving flexible and/or organic TF-PV.

The organometallic ink, OM1, showed high series resistance which was also observed in the I/V curve of OSI interconnects manufactured with this ink. In order to verify that the contact resistance was causing the high series resistance a larger TCO/ink contact area interconnect was tested. Increasing the contact width from the standard width of 70µm to 140µm resulted in a ~10% drop in series resistance which increased the fill factor of the interconnect by 3.2% absolute. Figure 4.18 shows images of the normal and larger contact area interconnects with the organometallic ink.

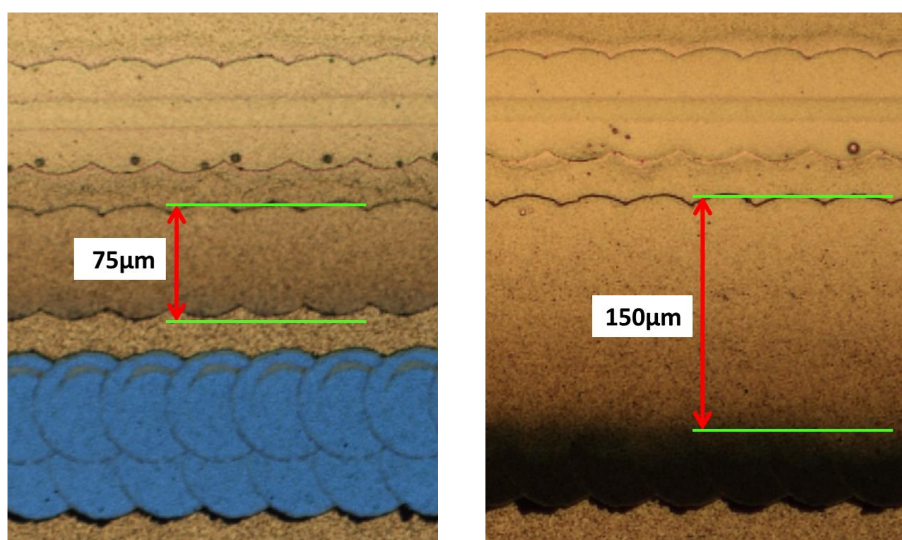


Figure 4.18: The impact of ink/TCO contact resistance was tested by measuring the change in series resistance with change in contact area. Left; 75µm wide region of metal/TCO contact, right; 150µm wide contact. Increasing the contact area showed a decrease in series resistance indicating that the contact resistance of the interface was negatively impacting the cells electrical performance.

Organometallic inks require lower temperature processing to form conductive tracks, ~120°C compared to ~200°C for nanoparticle inks. They are therefore still of interest

for applications requiring low temperature processes such as organic PV however the high contact resistance meant focussing on nanoparticle inks for the rest of the project. Further work is required to determine whether the high contact resistance is a feature of all OM inks or just OM1.

It is recommended that the measurement of contact resistance using TLM should be used to pre-screen inks for suitability for OSI. Based on the collected data it appears that specific contact resistivities $<100m\Omega.cm^2$ are required for all future inks.

4.3.2 Wetting of conductive inks on back contact

Wetting is the amount of spread on a substrate by a liquid and is governed by the interplay between liquid surface tension and substrate surface energy. Wetting can be quantified by contact angle which is the angle that a droplet of liquid makes with the solid surface at equilibrium. Contact angle can be measured using suitable apparatus, described in detail in Chapter 2. In the case of ink wetting the back contact of a TF-PV cell the ink tends to wet the metal well since metals surface energies are large, silver is $\sim 1200mJ/m^2$ [8] compared with the surface tensions of organic solvents $\sim 20\text{-}80mJ/m^2$ [9].

For OSI it was found to be important that the ink does not extensively wet the back contact as significant ink spreading results in a thinner layer over the interconnect which leads to areas of high series resistance and local discontinuities. OSI has been tested on a large number of different back contact metals and the degree of spread varies widely between different back contacts. Figure 4.19 shows the same ink wetting two back contacts made by the deposition of a thin layer of silver, despite the material being the same the ink behaves very differently on each of the samples. After a clean in IPA to remove any organic contaminants the difference in contact angle between the two samples, A (left) and B (right), was measured with DI water to be 11°, 64° and 53° respectively which has corresponded to an increase in contact width of 180µm or 2.5x.

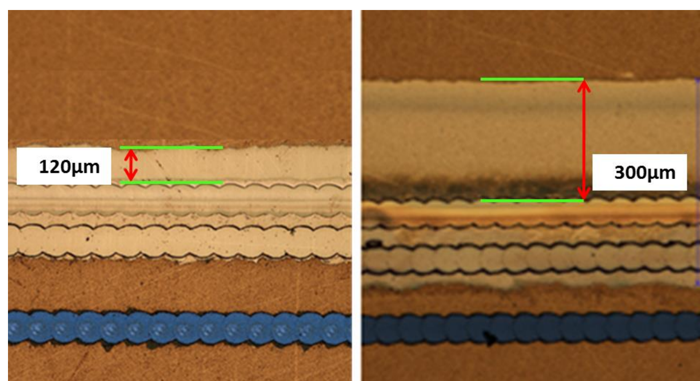


Figure 4.19: The same ink printed with the same drop pitch onto different silver back contacts. The ink spreads 120µm on back contact 1, left and 300µm on back contact 2, right. This clearly demonstrates that the substrate plays a large part in ink wetting. The contact angle of DI water with the substrate on the left is 64°, the right 53°.

The variation in the wetting is attributed to the dependence of the contact angle on surface chemistry. To achieve suitable conductive ink wetting it is therefore required to either match the ink to the substrate or find a way of normalising the substrate. In pursuit of surface normalisation a group of sulphur containing, organic chemicals known as thiols or mercaptans were investigated. The general formula is R-SH, where R is any carbon chain; in this case R was an alkane with chain length C5 to C10. The sulphur end of the thiol binds selectively to most common back contact metals including, silver, gold and molybdenum, forming a self-assembled monolayer (SAM) [10] see Figure 4.20. The remaining organic chain then points away from the surface which decreases the effective surface energy. The length of organic chain determines the magnitude of wetting reduction. Thiols of chain length 5-10 were initially chosen for further investigation by applying thin layers of the volatile liquid to the surface and allowing the bulk to evaporate off naturally. It was found that Thiols with chain lengths greater than C10 were no longer liquid but were solid and so could not be applied in this way.

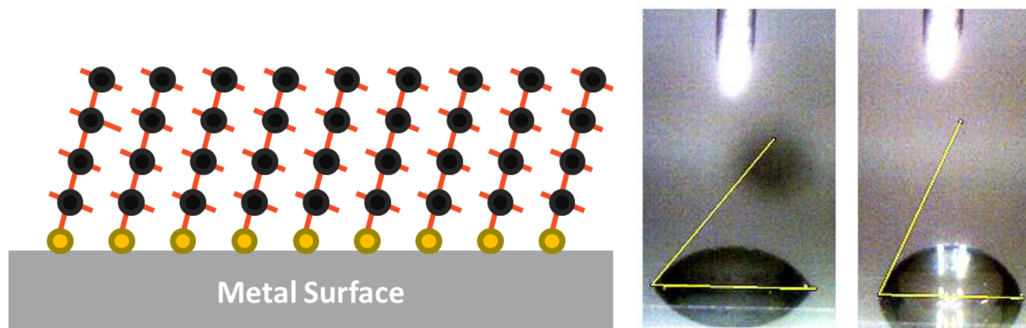


Figure 4.20: Left; an illustration of a thiol SAM on a metal surface. The sulphur end of the chain (yellow) binds to the metal and the carbon ends point upwards in a regular arrangement. Right; the impact of applying a thiol coating to a metal surface note the increase in contact angle.

Using this approach increased the contact angle of substrate B in Figure 4.19 from 53° to 67° which allowed good control of the conductive ink deposition. A notable feature of the interconnects formed with the pentanethiol was the formation of a ‘hard’ barrier ~55µm away from the top of the A scribe, marked at the top of Figure 4.21. This allowed deposition of a large volume of ink without increasing the track width. Figure 4.21 shows interconnects manufactured using a pentanethiol treatment at both ~36µm and ~13µm drop pitch on the same substrate. Mini-modules manufactured in this way were found to have excellent electrical performance with fill factors as high as 78% for a 10 cell module.

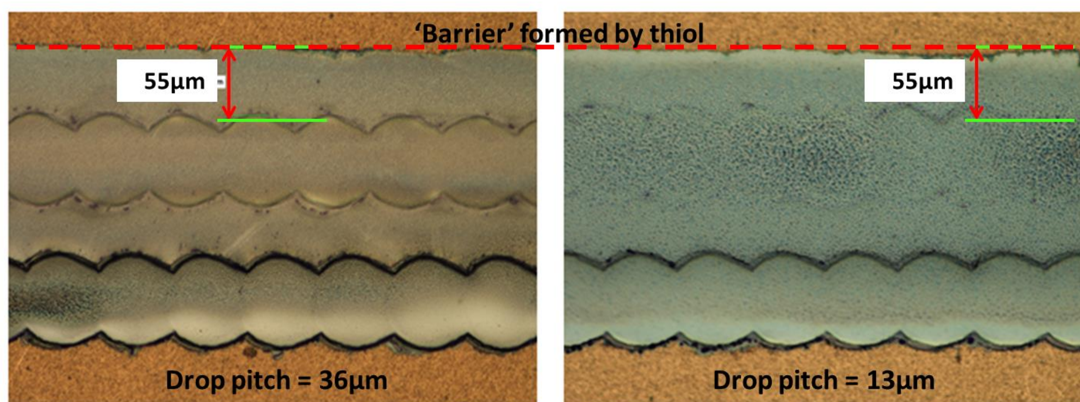


Figure 4.21: Interconnects formed using pentanethiol to control the ink. Left image 36µm, right image 13µm drop pitch. Despite the increased ink volume in the 13µm case the ink spread is limited to ~55µm.

This approach to chemical surface modification allowed the fulfilment of a short-term project goal of demonstrating OSI on a particular customer cell stack however it was abandoned for two reasons. Most importantly it is difficult to see how this approach can be used in a production environment without significant extra cost and process time from the added wet chemical steps. Secondly the odour of the sulphur containing thiols

was both offensive and pervasive resulting in the process not being suited to areas where other persons are in the proximity (as in the case for the laboratories at M-Solv).

4.4 Matching ink wetting to substrate

Rather than normalising the surface with chemical treatment a portfolio of inks was sought which wet suitably on different back contacts without modification. One of the most promising ranges of inks were from Sun Chemical Crop. coded 5714 and 8025. Both had a high surface tension and therefore didn't wet the back contact completely, interestingly the wetting on the insulator was also similar. The ink formed a thin, ~60µm wide, track regardless of substrate. Although this is not suited for production, when the complete interconnect must be formed in a single pass, it made R&D extremely easy with the ink remaining where it was deposited. Complete interconnect coverage could be achieved by stepping the stage in small increments and building up the required layer in multiple prints. Images of ink 5714 can be seen in Figure 4.22.

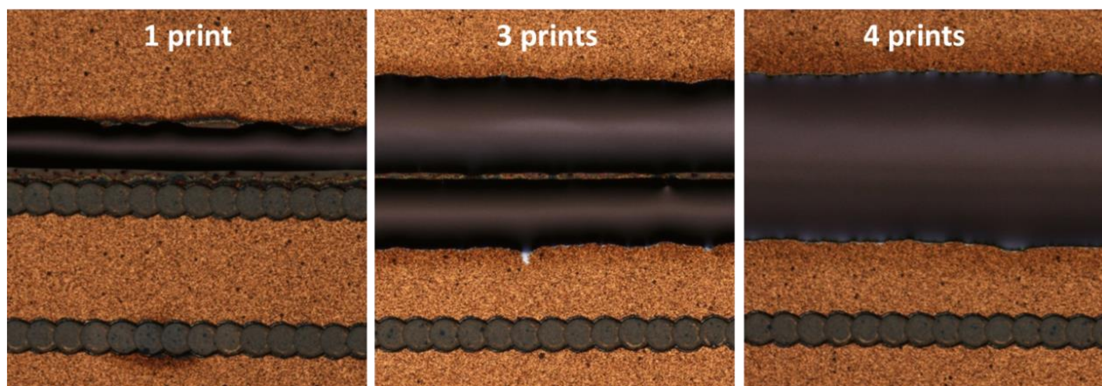


Figure 4.22:Sun chemical silver nanoparticle ink 5714. The ink spread is independent of surface making it easy to build up an interconnect with multiple prints.

This ink enabled the formation of interconnects which functioned electrically on multiple different back contacts. The performance was not as good as expected because of the appearance of two new problems which were back contact dependent. On CdTe samples with gold back contacts produced by CSU/CREST and some commercial silver a-Si back contacts the conductive ink cracks during drying. On other commercial silver a-Si back contacts from a different supplier the ink de-wets the insulator leaving holes. Both effects can be seen in Figure 4.23. The two problems were investigated separately, see following sections.

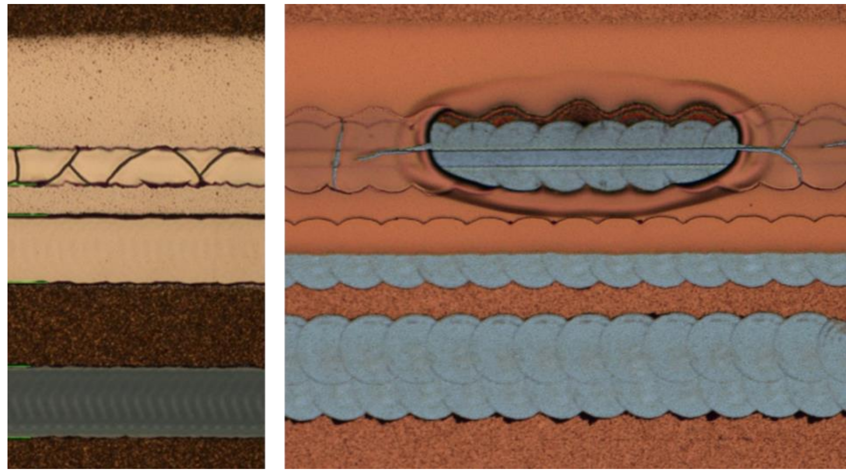


Figure 4.23: The two problems seen with the conductor deposition. Left: the ink selectively cracks over the insulator during thermal processing. Right: the ink de-wets off the insulator forming a hole.

4.4.1 Cracking of conductive inks

From the above images it is obvious that the cracking of the conductive ink is, at least partially, due to the substrate upon which it is deposited as the cracking only occurs over the insulator. The first thought was that the cracking was due to a mismatch of the coefficient of thermal expansion (CTE) of the two different substrate materials. Tests were run to determine the temperature at which cracks occur with the expectation that if it were due to CTE mismatch then cracking would occur at high temperatures.

The solvents in the ink were not very volatile therefore a hotplate at 50°C was used for low temperature drying of the ink without sintering. It was found that the metal ink cracks at 50°C long before CTE mismatch would cause significant differences in expansion of the insulator and metal. Figure 4.24 shows cracks forming at 50°C and the same section after sintering at 250°C. Furthermore this effect wasn't seen with a previous metal ink, IJ031 from Inktec which was also a silver nanoparticle suspension therefore another reason was sought.

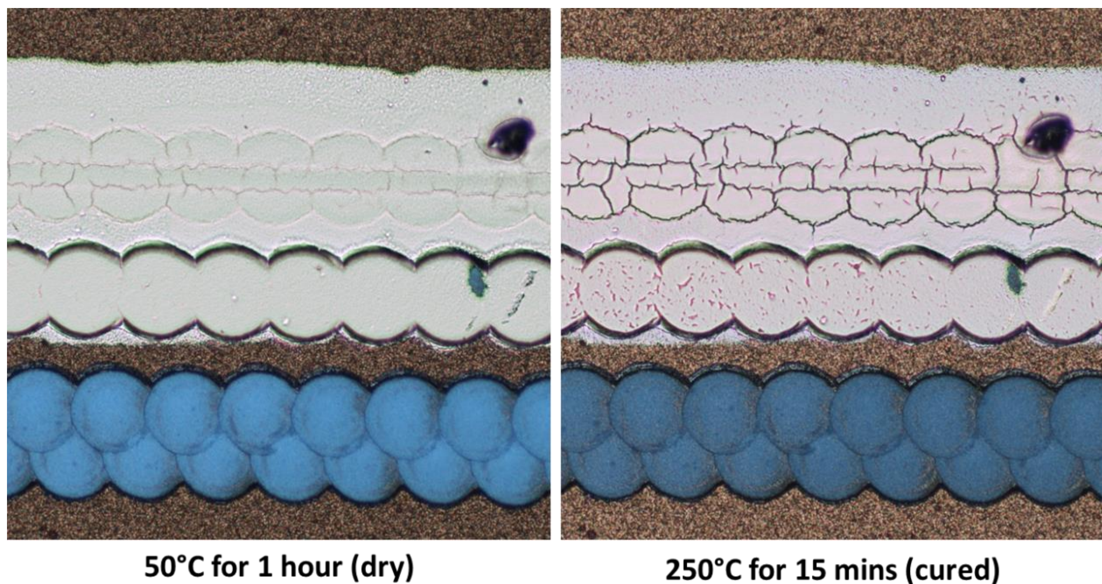


Figure 4.24: Conductive ink cracks during drying at 50°C for an hour, the cracks open up further during sintering at 250°C.

The cracking in colloidal dispersions is a topic well understood by the paint industry, consequently, looking at relevant literature, provided a potential mechanism for the observations seen with the conductive inks [11]–[13]. During drying, capillary forces between the small particles in the suspension cause a compressive force on the layer. If the compressive force is greater than the film strength then cracks are formed. Smaller particles, like the metal nanoparticles in the ink produce a larger compressive force due to narrower capillaries.

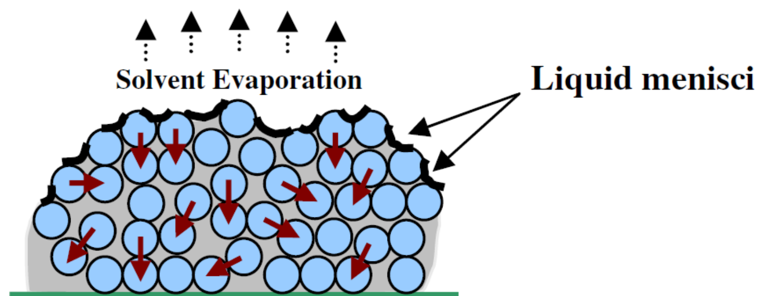


Figure 4.25: Capillary forces during drying of particle suspensions. The magnitude of the capillary forces is increased for smaller particle sizes [11].

All colloidal suspensions have a critical cracking thickness (CCT) which is the maximum layer thickness before cracking occurs. CCT is dependent on the specific surface area (SSA) of the particles (i.e. surface area per unit volume) with high SSA causing a lower CCT [14]. Higher substrate affinity, or better adhesion between the suspension and substrate increases CCT. Drying time also affects CCT when the

particles are large with slower drying increasing CCT however this effect is lessened for smaller particles. Figure 4.26 shows a plot of CCT against SSA. The SSA of a 50nm sphere in a solution loaded 40% was calculated to be ~$10^7 m^2/cm^3$.

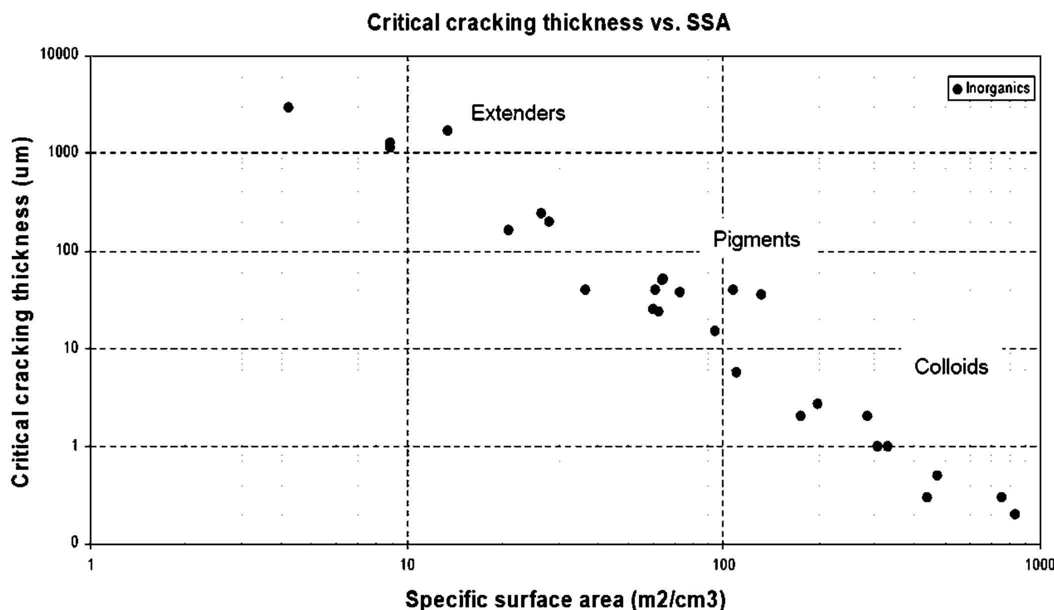


Figure 4.26: A plot of specific surface area against critical cracking thickness [14].

From this it is possible to explain why the previous ink, IJ031, formed layers without cracks. Firstly it wet the back contact much better resulting in thinner layers, below the CCT. Secondly it contained an adhesion promoter, epoxy particles, designed to aid bonding to the substrate. This will have had two effects, firstly the SSA will have been increased due to the presence of the larger epoxy particles and secondly the increased adhesion to the substrate will have increased the layer strength both resulting in less propensity to crack.

To verify this theory a test was devised using a long conveyer oven with the ability to control the temperature ramp between discreet sections. Introducing a thermal ramp it was possible to reduce the viscosity of the ink before evaporating off the volatile solvent within the ink, holding the ink in place. By experimenting with ramp profile a regime was found where the ink could be made to spread further on the back contact reducing the layer thickness and, as expected based on the proposed mechanism, this did indeed remove the cracking. Figure 4.27 shows the same volume of the same ink deposited on the same substrate but controlled with a thermal ramp to decrease layer thickness and remove cracking. This verifies the existence of a CCT for conductive inks on insulator substrates however the extra spreading from the ramped thermal

profile would make it difficult to stop the conductive ink from shorting the P3 scribe. Since CCT is also linked to ink/substrate affinity it was apparent that cracking and the dewetting of the insulator observed previously may be related.

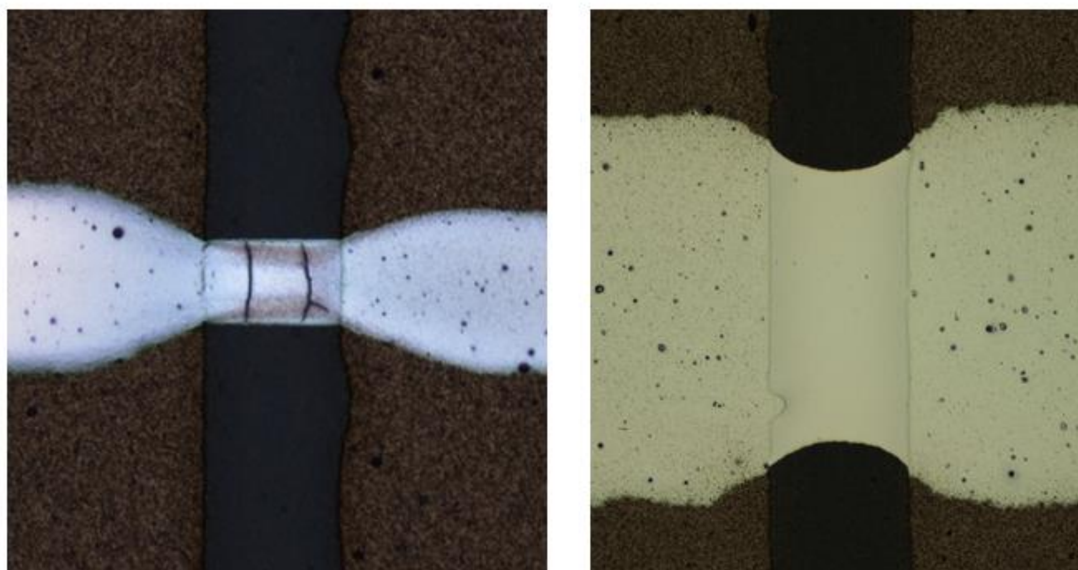


Figure 4.27: Wetting of conductive nanoparticle ink over inkjet printed insulator. The same volume of ink is deposited in both images the spread is controlled by controlling the profile of the thermal treatment.

4.4.2 Plasma surface treatment for wetting modification

It has been shown that some inks de-wet the insulator because of preferential wetting on the metal back contact. The metal back contact has a higher surface energy than the polymeric insulator so to some extent all conductive inks will have a propensity to flow from the insulator to the back contact. This wasn't observed with the previous ink IJ-031 because it was also highly volatile meaning that the solvent evaporation occurred before the ink moved on the surface. The inks from Sun Chemical are less volatile and therefore have more time in the liquid phase in which to flow.

In order to preferentially increase the conductive inks affinity for the insulator without over-wetting the back contact a plasma treatment was investigated. Plasma treatment involves passing a gas between high voltage electrodes which ignite a plasma, this is then directed at the surface, plasma treatments have been discussed for the sintering of conductive inks in Chapter 2. The plasma activates the polymer insulator by incorporation of oxygen and increasing the density of dangling bonds which aids wetting [15]. On the metal back contact the plasma has little effect beyond cleaning off

any organic contamination but even this can result in a significant increase in ink spread. Plasma processes are widely used in the printing industry to increase the adhesion of UV cure inks to plastic substrates.

An atmospheric, air plasma nozzle was purchased from Dyne Technologies and mounted on a 6 axis robot for testing, see Figure 4.28. The plasma nozzle ignites a clean, dry compressed air source into an atmospheric plasma using high voltage electrical discharge [16], the air pressure is 5-6 Bar. The plasma is passed over the surface of the module with a stand-off of ~5mm after the deposition of the insulator. The nozzle is small enough to consider mounting one on the OSI process head if required and the plasma treatment works at high enough translation velocities, >1m/s, to be compatible with manufacture. Figure 4.29 shows the impact of the plasma treatment on the wetting of conductive tracks over insulator.

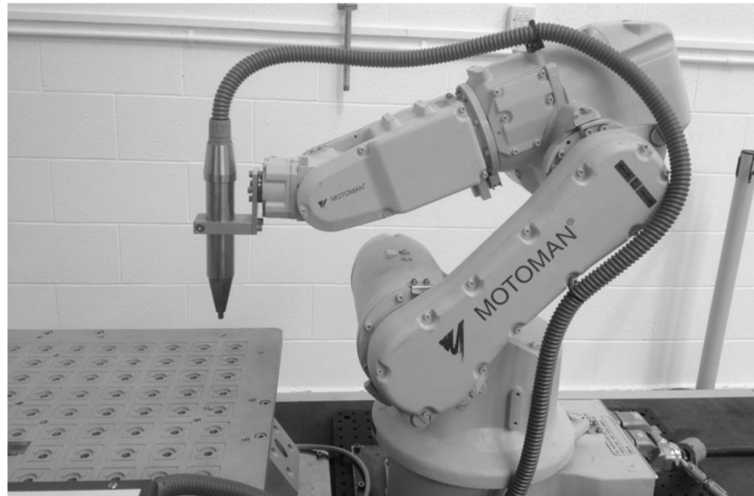


Figure 4.28: Atmospheric plasma nozzle attached to a 6 axis robot. The plasma is ignited in a jet of compressed dry air using high voltage electrical discharge.

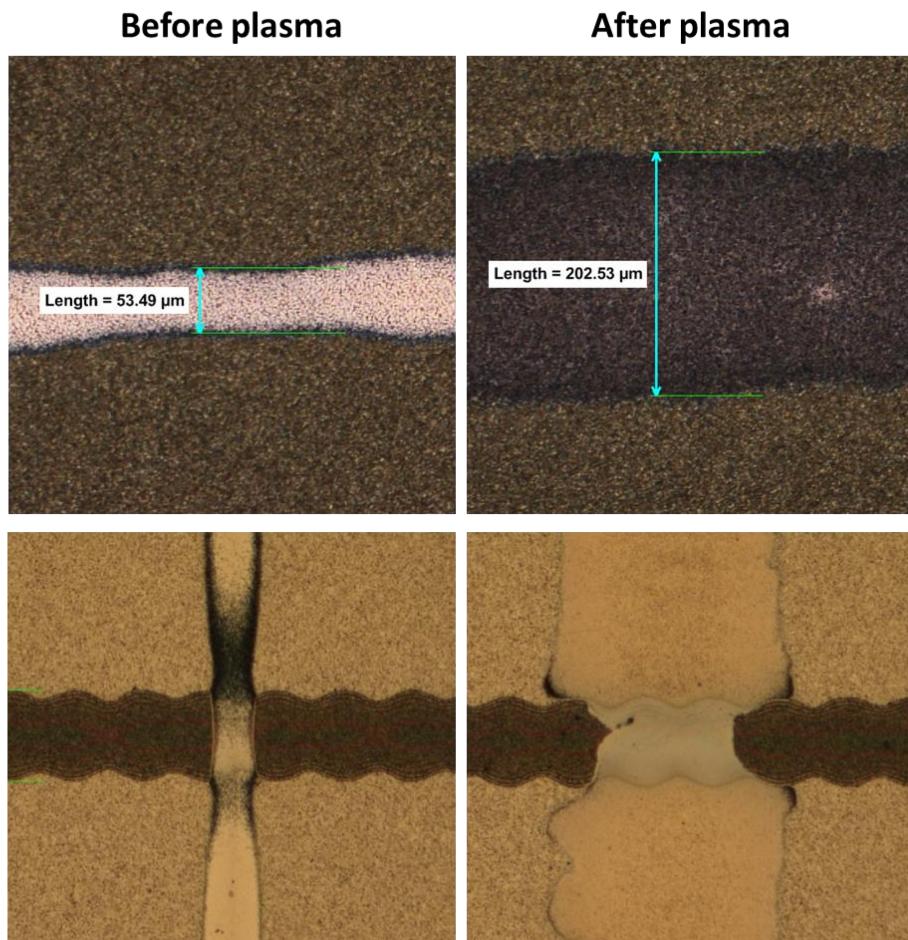


Figure 4.29: The plasma surface treatment increases the wetting of the conductive inks on both back contacts and over inkjet printed insulator.

After introducing the plasma treatment along with reducing the deposited volume of conductive ink to a minimum to obtain good area coverage of the interconnect it was possible to completely remove the dewetting and reduce the crack formation to a minimum on a-Si and almost no cracking on CSER modules, see Figure 4.30. This has allowed manufacture of test cells on CdTe devices from CSER that are suitable for publication and lifetime testing.

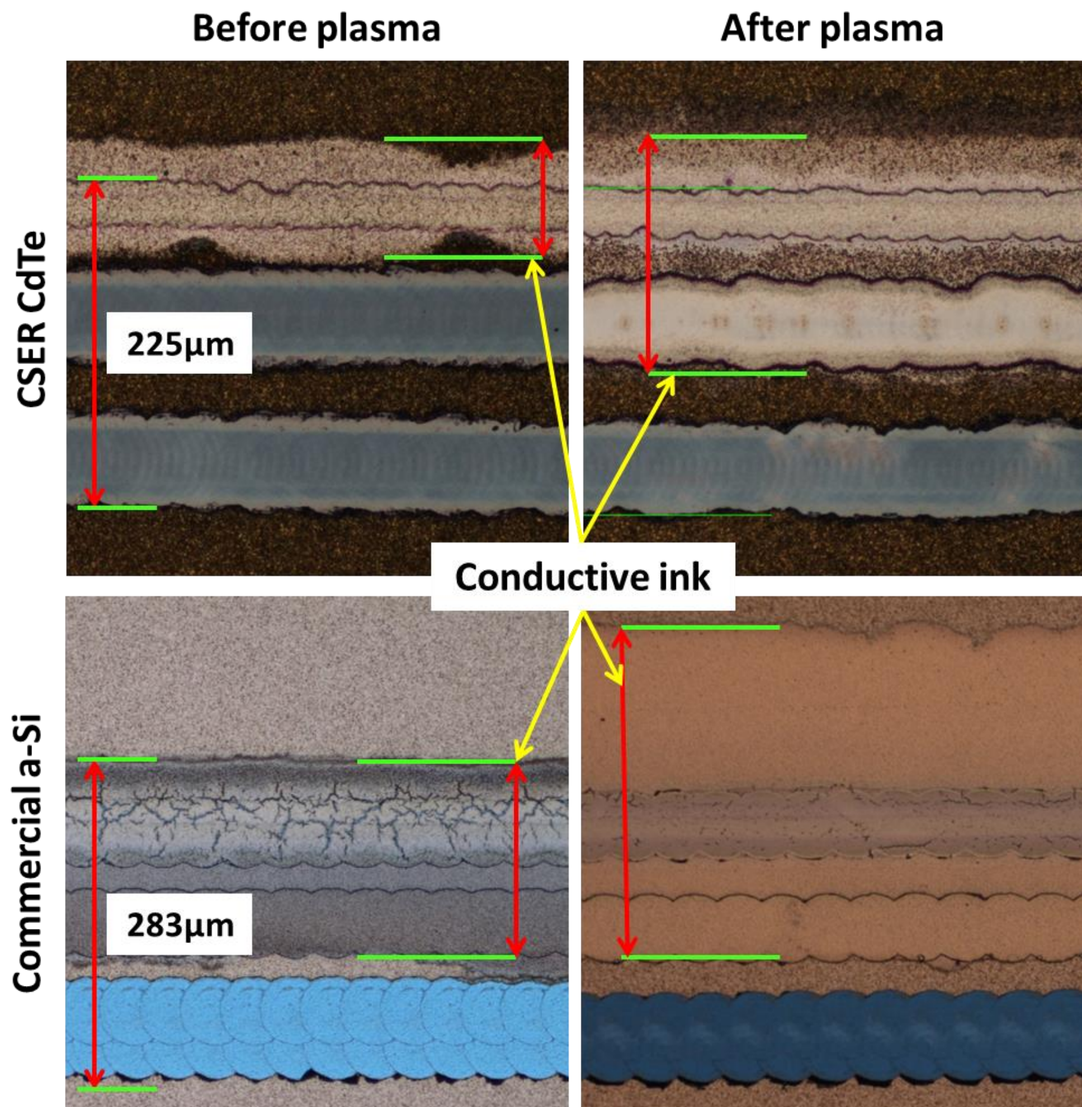


Figure 4.30: The plasma treatment increases the wetting of conductive ink over interconnects on CdTe and reduces the amount of cracking on a-Si.

4.4.3 Summary of conductive ink deposition

It is desirable to completely remove the cracking on all cell structures and to allow the deposition to occur in a single pass. A pair of inks with appropriate wetting for a well-controlled interconnect either with or without plasma is still being sought. During testing of alternative insulator/conductor pairs many unusual wetting behaviours have been observed. Figure 4.31 shows a selection of some of these behaviours. This serves to demonstrate the challenge in finding a well matched ink pair and also shows that there is still work to be done in order to fully understand this behaviour.

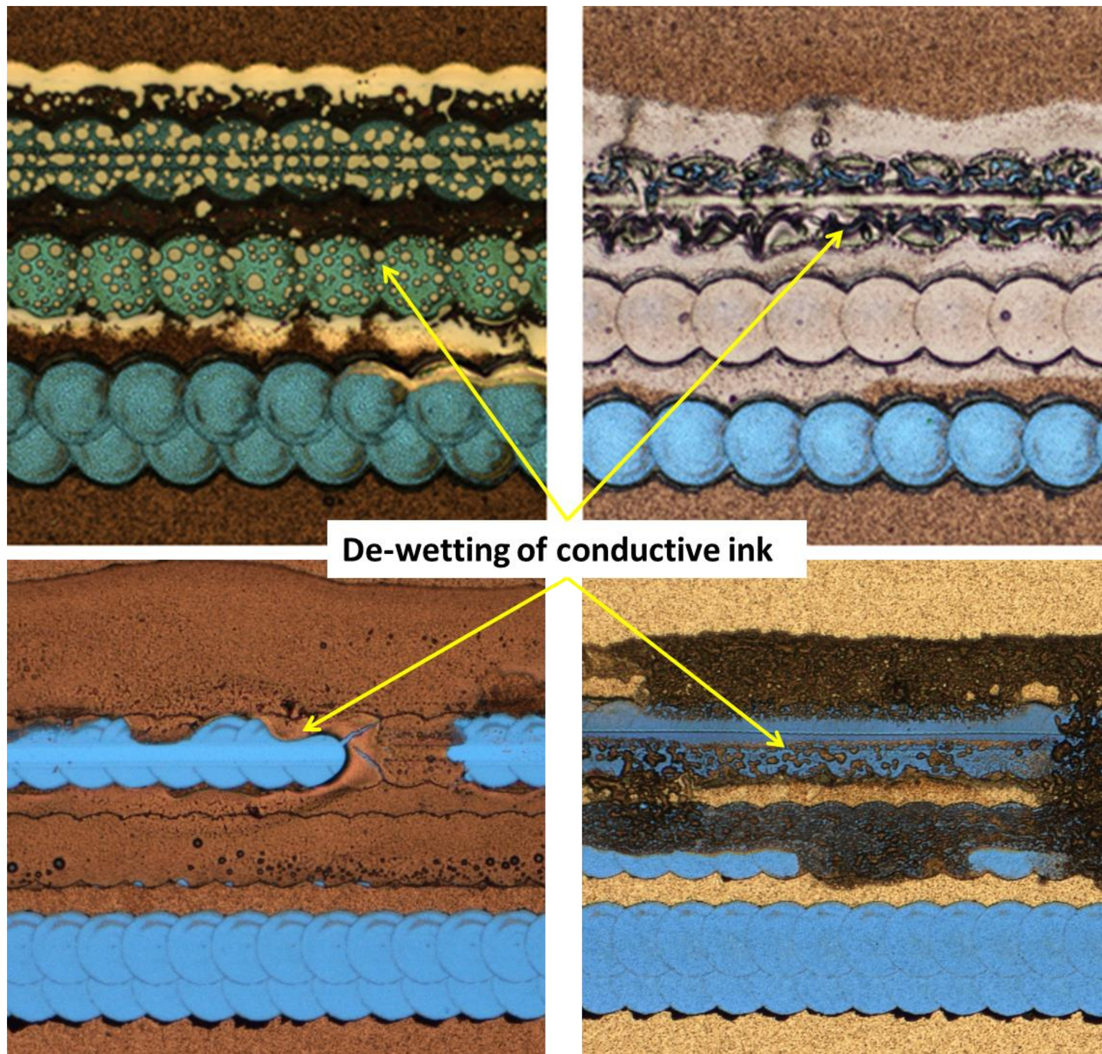


Figure 4.31: Examples of unusual de-wetting behaviour of various conductive inks tested while searching for a suitable ink for OSI. The de-wetting of the different inks occurs at different length scales giving rise to either large holes in the coating, bottom left, or individual beads of ink, top left. Or combinations of the two, right.

4.5 Conclusions

Controlled deposition of a number of insulating inks has been demonstrated. It is relatively easy to obtain good morphology from the insulator fill with the caveat that the thermal stability of the polymer ink should be monitored. The conductive ink presents more of a challenge as it must be well matched to both the insulator and the back contact metal. This is made easier in the R&D environment by the availability of surface modification either by chemical methods, thiol treatment or physical methods such as plasma treatment. The thiol treatment is not compatible with industrial manufacture however plasma treatment could be integrated into a production process.

Controlled conductive ink deposition has been shown in some cases with the aid of surface treatments which has allowed the manufacture of test modules. There is an on-going challenge in finding a combination of inks which work on some surfaces.

Further work includes the investigation of localised deposition of viscous conductive pastes which do not show the problems of cracking or dewetting and which have a deposited line width which is independent of surface energy. This work is at an early stage but shows promise as an alternative to inkjet printing of the conductive track.

4.6 References

[1] L. Vanmaele and E. Verdonck, "Ultraviolet curable ink consists of a copolymer of acrylic monomer and vinyl ether monomers; and a colorant," US6310115 B12001.

[2] A. Kamyshny, J. Steinke, and S. Magdassi, "Metal-based Inkjet Inks for Printed Electronics," *Open Appl. J.*, vol. 4, pp. 19–36, 2011.

[3] P. J. Smith, D. Y. Shin, J. E. Stringer, B. Derby, and N. Reis, "Direct ink-jet printing and low temperature conversion of conductive silver patterns," *J. Mater. Sci.*, vol. 41, pp. 4153–4158, 2006.

[4] H. Peelaers, E. Kioupakis, and C. G. Van de Walle, "Fundamental limits on optical transparency of transparent conducting oxides: Free-carrier absorption in SnO2," *Appl. Phys. Lett.*, vol. 100, no. 1, p. 011914, 2012.

[5] R. Jackson and S. Graham, "Specific contact resistance at metal/carbon nanotube interfaces," *Appl. Phys. Lett.*, vol. 94, no. 2009, pp. 10–13, 2009.

[6] J. Klaer, R. Klenk, A. Boden, A. Neisser, C. Kaufmann, R. Scheer, and H.-W. Schock, "Damp heat stability of chalcopyrite mini-modules: evaluation of specific test structures," *Conf. Rec. Thirty-first IEEE Photovolt. Spec. Conf. 2005.*, 2005.

[7] B. Van Zeghbroeck, "Principles of electronic devices," University of Colorado, 2011, pp. 3–6.

[8] L. Vitos, a. V. Ruban, H. L. Skriver, and J. Kollár, "The surface energy of metals," *Surf. Sci.*, vol. 411, pp. 186–202, 1998.

[9] M. Gindl, G. Sinn, W. Gindl, A. Reiterer, and S. Tschegg, "A comparison of different methods to calculate the surface free energy of wood using contact angle measurements," *Colloids Surfaces A Physicochem. Eng. Asp.*, vol. 181, no. 1–3, pp. 279–287, Jun. 2001.

[10] G. M. Whitesides and P. E. Laibinis, "Wet Chemical Approaches to the Characterization of Organic Surfaces: Self- Assembled Monolayers, Wetting, and the Physical-Organic Chemistry of the Solid-Liquid Interface," no. 11, pp. 87–96, 1990.

[11] K. Singh and M. Tirumkudulu, "Cracking in Drying Colloidal Films," *Phys. Rev. Lett.*, vol. 98, no. May, pp. 1–4, 2007.

[12] M. S. Tirumkudulu and W. B. Russel, "Cracking in drying latex films," *Langmuir*, vol. 21, no. 4, pp. 4938–4948, 2005.

[13] W. P. Lee and A. F. Routh, "Why do drying films crack?," *Langmuir*, vol. 20, no. 23, pp. 9885–9888, 2004.

[14] M. Murray, "Cracking in coatings from colloidal dispersions: An industrial perspective," 2009.

[15] E. M. Liston, L. Martinu, and M. R. Wertheimer, "Plasma surface modification of polymers for improved adhesion: a critical review," *J. Adhes. Sci. Technol.*, vol. 7, no. 10, pp. 1091–1127, Jan. 1993.

[16] E. Stoffels, a J. Flikweert, W. W. Stoffels, and G. M. W. Kroesen, "Plasma needle: a non-destructive atmospheric plasma source for fine surface treatment of (bio)materials," *Plasma Sources Sci. Technol.*, vol. 11, pp. 383–388, 2002.

Chapter 5 : OSI mini-modules on CdTe

CdTe mini-modules were fabricated based on material from two sources. Colorado State University (CSU) supplied material for initial module fabrication, the results of which were presented at the 39th IEEE Photovoltaics Specialist Conference (PVSC), Tampa [1] with further details given at the 10th Photovoltaic Science and Technology (PVSAT) conference, Loughborough [2]. More recently, further CdTe has been supplied by the Centre for Solar Energy Research (CSER), Glyndwr University, primarily for the purposes of lifetime testing. Electrical results were presented at the SNEC 8th International Photovoltaic Power Generation Conference & Exhibition, Shanghai [3]. Accelerated lifetime testing data was presented at the 40th IEEE-PVSC conference, Denver [4] and the 29th European PV Solar Energy Conference and Exhibition (PVSEC), Amsterdam [5].

This chapter describes the parameters used to construct these mini-modules and reports the results obtained. A description of the accelerated lifetime testing program at M-Solv is included, along with the results of these tests on OSI manufactured CdTe mini-modules.

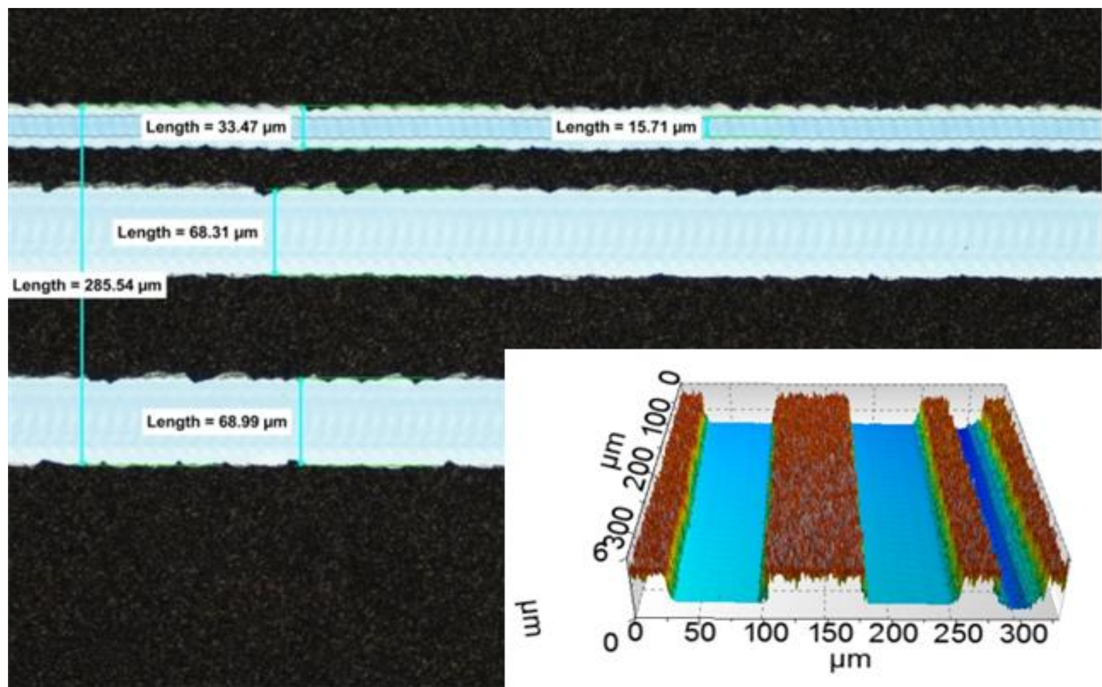
5.1 Mini-module manufacture on CSU CdTe

Two CdTe mini-modules were manufactured by CSU. The modules were built on Pilkington NSG TEC10 glass which is a glass substrate coated with 10 Ω/□ Fluorine doped Tin Oxide (FTO). A thin layer of n-type CdS, <100 nm, and a thicker p-type layer (~2.5 μm) of CdTe is then deposited by Closed Space Sublimation (CSS) to form the absorber layer [6]. The devices then received a copper doping treatment which allows an Ohmic contact to be formed with a metallic back contact. The two cells were then sent to the Centre for Renewable Energy Systems and Technology (CREST) at Loughborough University for the deposition of the back contact. Two different back contact materials were tested; nickel and gold. Both samples were shipped to M-Solv for series interconnection by OSI. The same process parameters were found to be suitable for both types of back contact. Details of the process parameters can be seen in Table 5.1.

Process step	Parameter	Value
Laser - A scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	2.95
	Spot diameter (µm)	37
	Pulse duration (ns)	<12
	Pitch (µm)	10
	Optical setup	Focused Gaussian beam
Laser -B scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	0.73
	Spot diameter (µm)	69
	Pulse duration (ns)	<12
	Pitch (µm)	12
	Optical setup	Imaging 750um mask
Clean	Solvent	IPA
	Duration (s)	300
	Plasma	No
Insulator IJ	Ink manufacturer	Sun Chemical
	Identifier	U7878
	Drop pitch (µm)	63.5
	Nominal drop volume (pl)	10
Insulator Cure	Lamp type	Mercury
	Dose (mJ/cm^2)	151
Conductive IJ	Ink manufacturer	Sun Chemical
	Identifier	U8025
	Metal type	Nanoparticle
	Material	Ag
	Loading (% by wt)	40
	Drop pitch (µm)	25.4
	Nominal drop volume (pL)	30
	Number of passes	5
Conductive sinter	Time (minutes)	15
	Temperature (°C)	230

Table 5.1: Process parameters of mini-modules fabricated on CSU CdTe

Optical images and white light interferometer profiles of different stages of the OSI process can be seen below. Figure 5.1 is the complete OSI scribe pattern and Figure 5.2 is the same set of images after the A scribe has been filled with an insulative polymer ink.



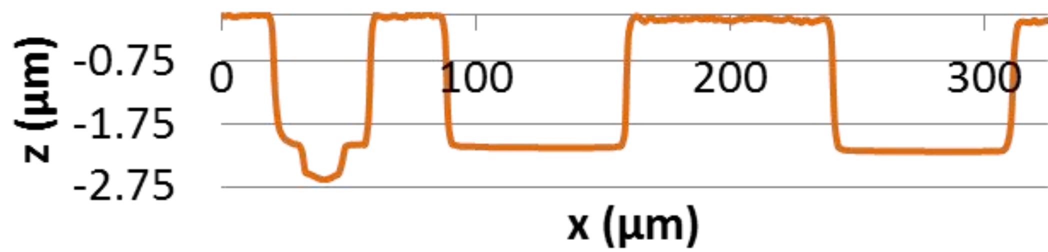


Figure 5.1: Scribe pattern for OSI interconnects with (inset) 3D height map from scanning white light interferometer and (below) line profile across the scribes.

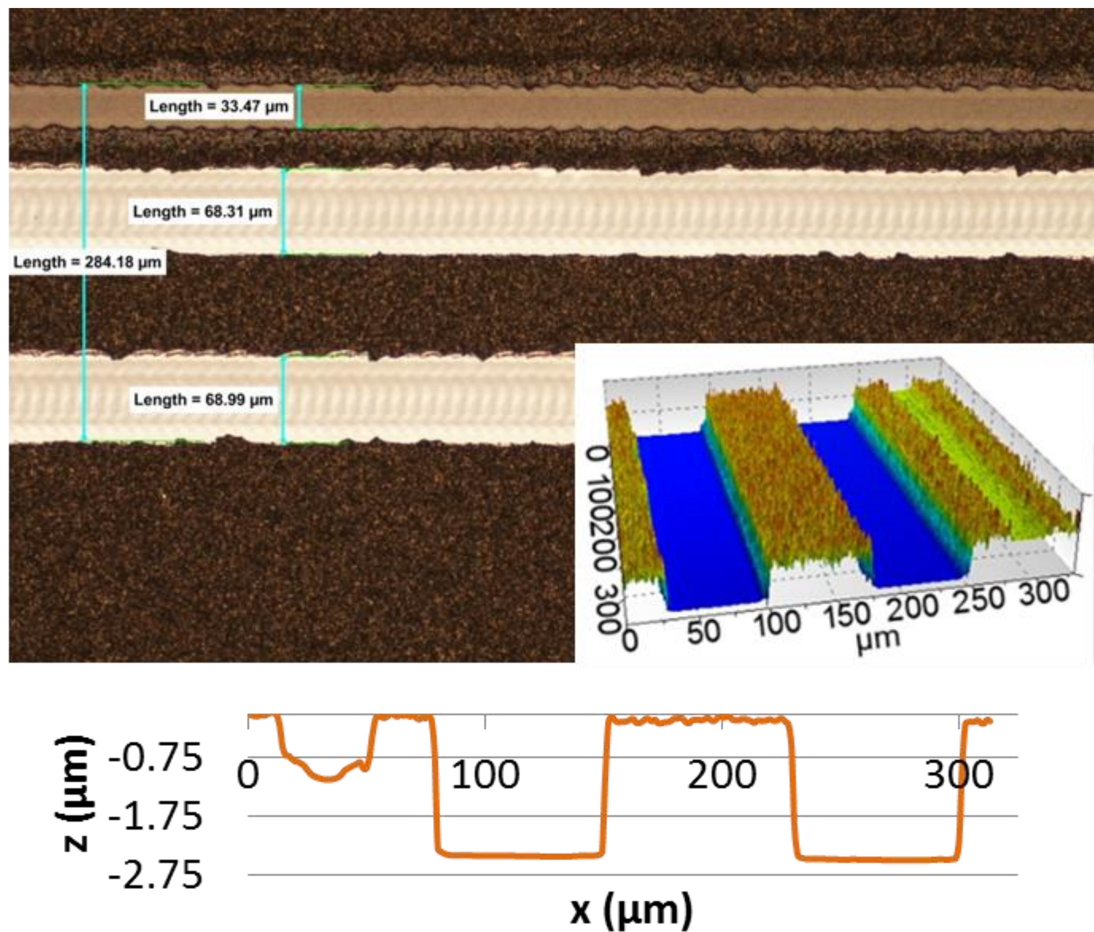


Figure 5.2: Scribe A is in-filled with Sun Chemical U7878 acrylic ink and UV cured inline. (main image) Top down optical micrograph, (inset) 3D height map and (below) line profile from scanning white light interferometer.

The final step for completion of OSI on CdTe is the printing of the conductive bridge. In this case the ink used was a 40% by weight silver nanoparticle suspension from Sun Chemical, coded U8025. The ink was printed in 3 passes at 1500dpi per pass; this is calculated to give a dry film thickness of 1.13µm assuming a nominal 30pL drop volume from the printhead. The measured film thickness is ~1.3µm in the B scribe and averages ~1.0µm on the back contact, in good agreement with the calculated value. As shown in Chapter 4 thick layers of metallic ink have a propensity to crack across the insulator and this was the case on both the gold and nickel back contacts. This work was completed before the plasma treatement was available at M-Solv, inclusion of the plasma treatment process would likely have reduced the extent of the cracking. Figure 5.3 shows the complete OSI interconnect on CSU CdTe with cracking observed across the insulator.

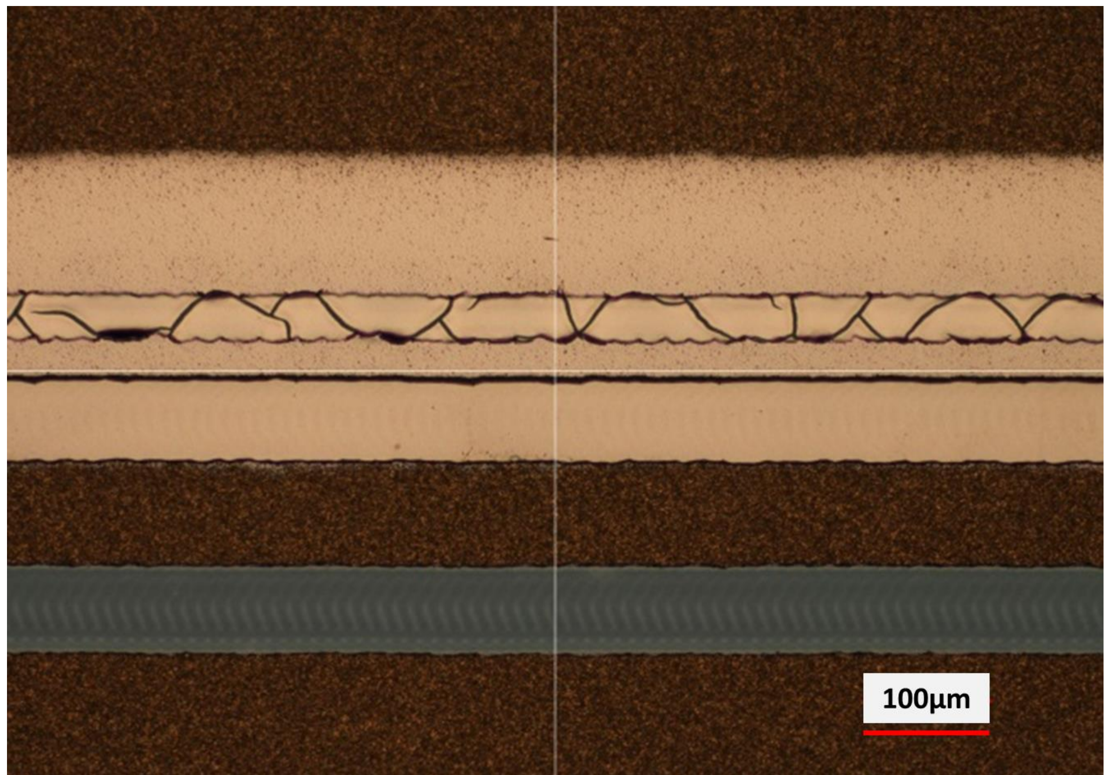


Figure 5.3: The completed OSI interconnect on CSU CdTe, cracking is observed across the insulator. These interconnects were manufactured before the plasma treatment was available, plasma treatment would likely have reduced the extent of the cracking.

Visually the ink behaviour was identical on both back contact materials, however the nickel back contact exhibited poor electrical performance. The nickel sputtering process was not optimised and it is believed that the deposition parameters resulted in both high contact and sheet resistances which gave rise to a low cell fill factor of ~32%. As the nickel back contact sample was defective it was decided to conduct mechanical analysis using a focussed ion beam (FIB) to cut cross-sections across the interconnect for imaging with SEM. This allowed the verification of the mechanical integrity of the interconnect, showing that the reason for the poor electrical performance was the defective cell stack and not the interconnect.

The FIB is built into the SEM and utilises Liquid Metal Ion Sources (LMIS), usually gallium (Ga) because of its low melting temperature, volatility and vapour pressure [7]. Ga ions are accelerated towards the samples using high electric fields, 10^{10}V/m at the FIB tip. Ga ions interact with the substrate in a number of processes, both elastic and inelastic, the most important of which for micro-milling is a collision-cascade interaction [7] in which the incoming ion is able to displace one or more substrate atoms due to transfer of energy exceeding the binding energy from the collision. This

sputtering of target atoms allows the micromachining of very small, ~10nm, features in substrates which are traditionally difficult to pattern. This technique is often used for the preparation of very thin samples for Transmission Electron Microscopy (TEM) but can also be used to cut cross sections across substrates for imaging with SEM. When using FIB to mill cross-sections it is often beneficial to first deposit a thin layer of platinum, by low energy FIB, in order to avoid surface damage of the substrate due to ion implantation or amorphisation of crytallinity within the target [8].

A cross section was cut using FIB along the width of an OSI interconnect on the Ni back contact sample for inspection with SEM. A layer of platinum, ~1µm thick, was deposited to protect the top surface of the material. A low magnification, 250x, SEM micrograph of the section milled with the FIB can be seen in Figure 5.4. Higher magnification, 25,000x, SEM micrographs were taken at regular intervals along the edge of the interconnect, 124 images in total. Figure 5.5 shows 4 such images from key points in the interconnect which are representative of the entire structure.

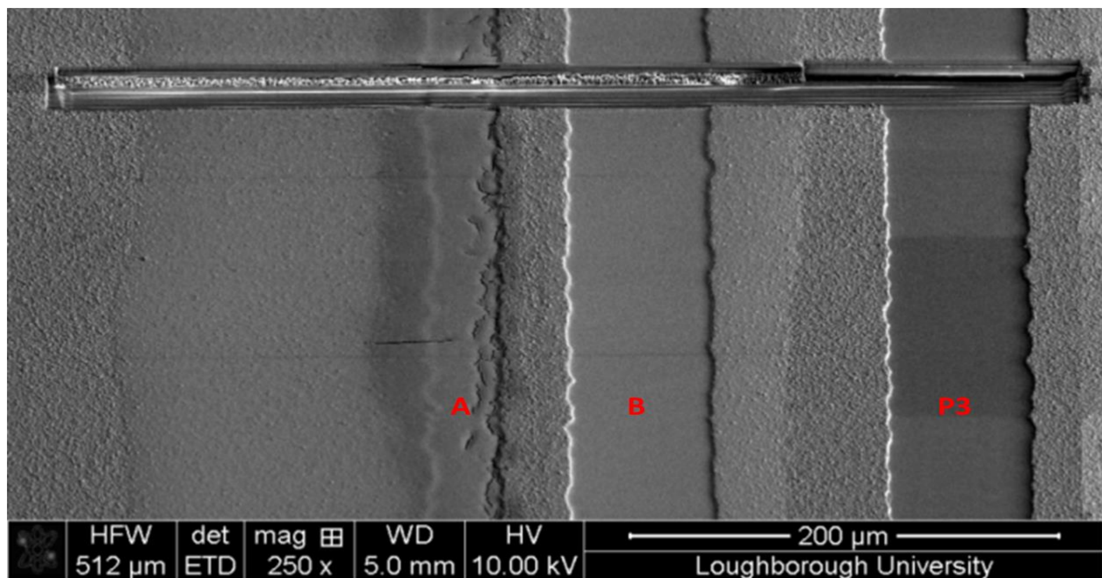


Figure 5.4: An SEM micrograph of OSI on CdTe supplied by CSU. Left to right scribes, A, B and P3 are visible. A cross section has been machined at 90° to the scribes using a gallium FIB in order to inspect the mechanical integrity of the interconnect.

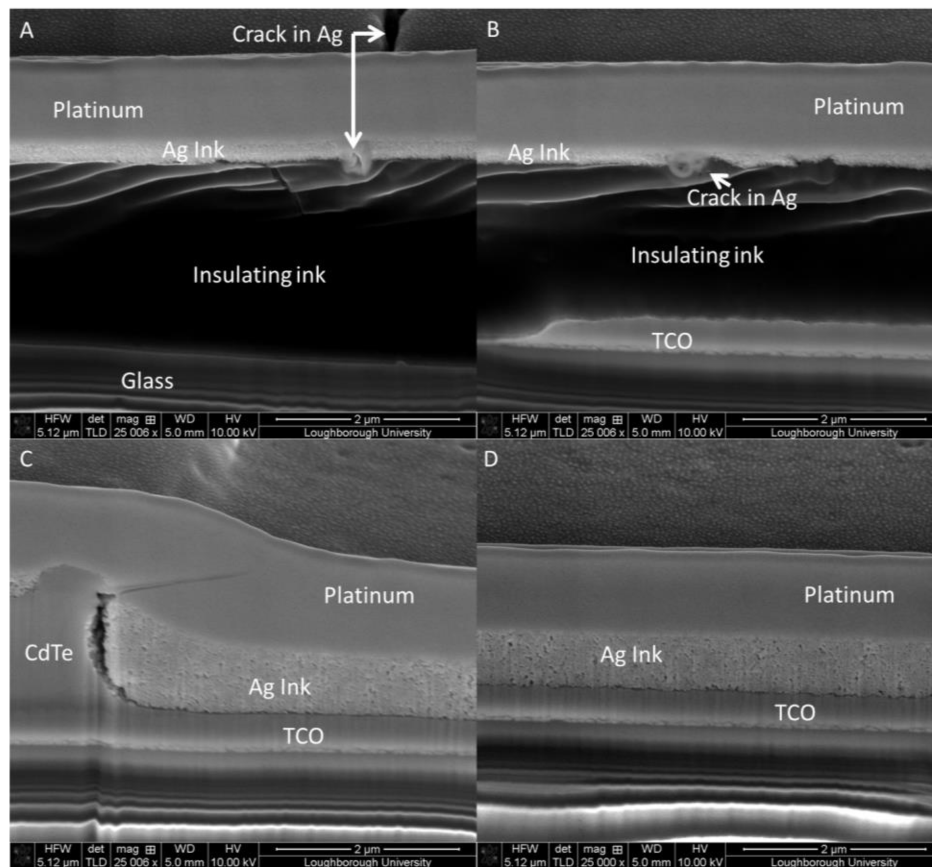


Figure 5.5: High magnification SEM micrographs. Image A; the sintered silver ink over the insulating ink, an extensive crack can be seen at the top of the image. Image B; insulator meeting the edge of the TCO with silver ink flowing over the top, smaller cracks in the silver are labelled. Image C; the edge of the B scribe, it can be seen that there is a void in the silver at the scribe edge. Image D; shows the silver ink making good contact with TCO.

Figure 5.5A shows the metallic silver flowing over the insulator with some cracks in the layer. Figure 5.5B shows the insulator fill within the A scribe, there are no leakage paths for silver ink through the insulative material. In both Figure 5.5A and B the cracks in the metallic ink can be seen however it is also noted that they do not propagate continuously along the length of the scribe, there are still pathways for current flow. Figure 5.5C shows a void in the silver ink at the edge of the scribe. Figure 5.5D shows the thick layer of silver ink in the B scribe and shows that the interface between the ink and the TCO is free of defects.

The CdTe cells had dimensions of 5x7.5 cm, OSI was used to define 6 active cells along the short axis of the sample with a pitch of 0.75 cm. It was decided to use the laser to divide the mini-module into an array of 24 cells with a length of 1cm each giving an active cell area of 0.75 cm. A diagram showing the cell layout with the measured cells highlighted and the failed cell marked in red can be seen in Figure 5.6. When deposited

the material grows preferentially at the centre of the sample, therefore the best performance is found in the central 2cm. Electrical cell performance data was collected from the 12 cells in the central 2 regions. Out of the tested 12 cells 11 of them worked, while 1 cell, designation 3.3 failed because of a short across the P3 scribe due to a change in wetting of the silver ink. A summary of the 12 cells performance data can be seen graphically in Figure 5.7 and is summarised in Table 5.2.

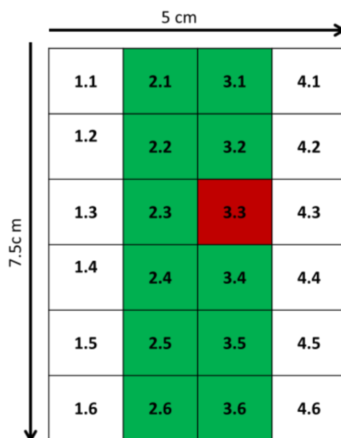


Figure 5.6: Diagram of cell layout of OSI cells manufactured on CSU CdTe.

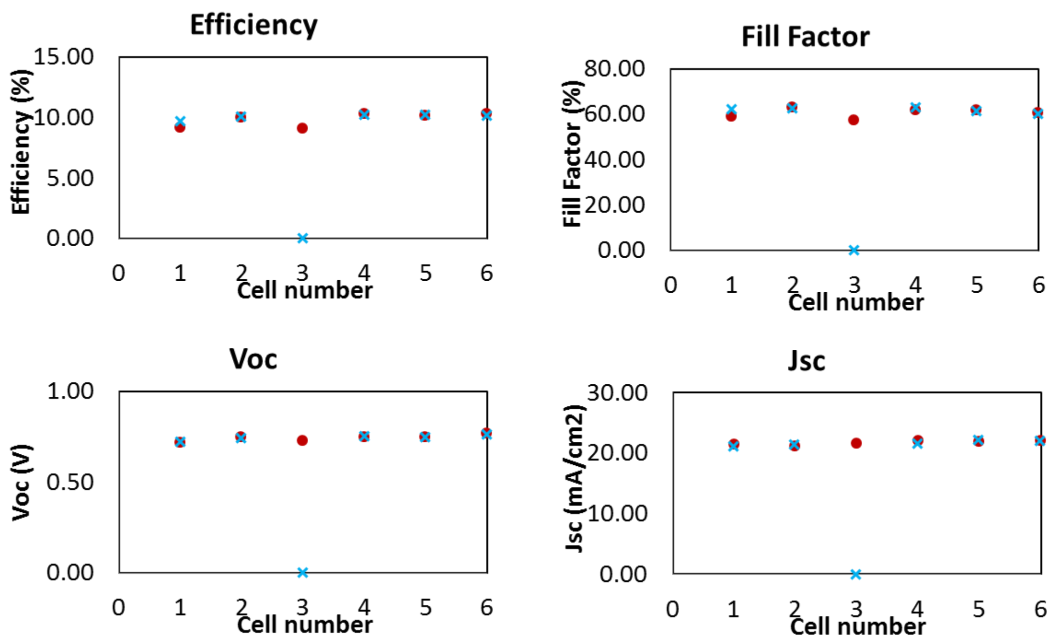


Figure 5.7: Graphical representation of electrical performance characteristics efficiency, fill factor, open circuit voltage and short circuit current density of 12 manufactured OSI cells on CSU CdTe. The cells were made in 2 columns of 6 cells each, column 1 is denoted by red circles, column 2 by blue squares. Cell 3 in column 2 was faulty.

	Best	Average	Standard deviation
Voc (V)	0.75	0.74	0.01
Jsc (mA/cm2)	21.55	21.62	0.35
FF (%)	62.64	61.07	1.65
Efficiency (%)	10.18	9.91	0.40

Table 5.2: Summary of the electrical performance of the 11 working OSI cells, the standard deviation of the measurements is small indicating consistent performance between cells.

The 11 working cells show an efficiency of around 10% which is known to be consistent with the cells produced by CSU at that time. The lack of comparable reference data is unfortunate but further experiments are described later with comparison to reference cells. In an effort to further confirm the quality of the OSI process strings of cells were tested from column 1. Any negative effect that the interconnect may have on fill factor would be cumulative therefore if strings of cells show no degradation in fill factor it is a good indication that OSI is functioning correctly. Figure 5.8 shows the I/V curves of 1, 3 and 6 cell strings of OSI interconnected cells on CSU CdTe. The average fill factor of the 6 cells in column 2 was 60.6% with in all cases the fill factor a standard deviation of 2.1%. The fill factor of the multi-cell strings is always within one standard deviation of the average constituent cell, leading to the conclusion that the interconnection process does not impact cell performance.

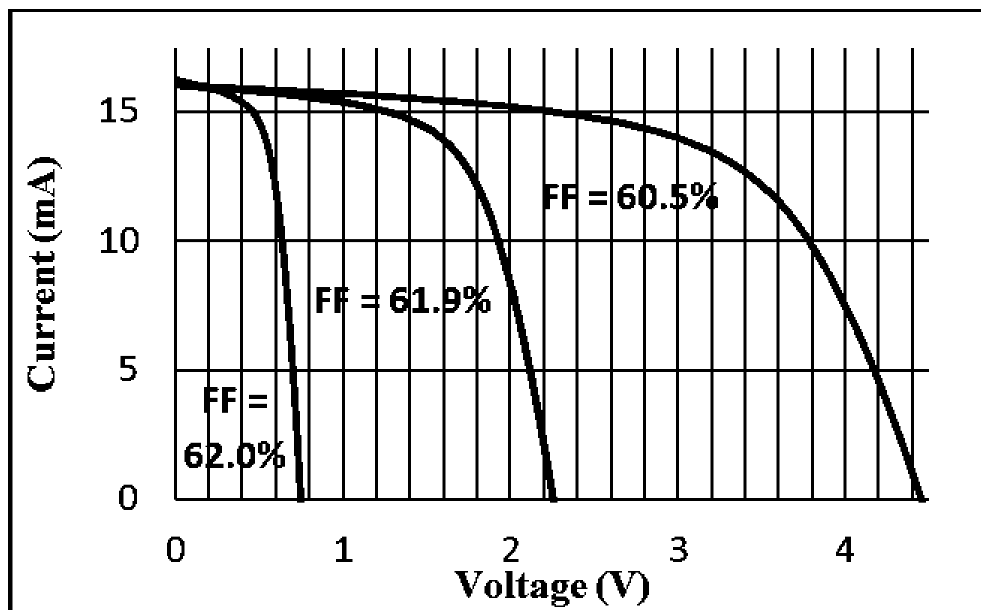


Figure 5.8: I/V curves of 1, 3 and 6 cell strings of OSI cells on CSU CdTe. The performance of a cell string is never less than 1 standard deviation away from the average of its constituent cells.

5.2 Mini-module manufacture on CSER CdTe

CSER deposit CdTe by a novel atmospheric MOCVD process onto the same commercially available NSG TEC10 substrates as CSU [9,10]. The stack consists of 150 nm of CdZnS and 2.25 μm of CdTe, incorporation of Zn into the CdS layer increases its transmission resulting in larger current densities within the device. The CdTe layer has two different dopant densities resulting in an npp^+ structure. The p^+ layer results in a more Ohmic contact for the metallic back contact, which in this case was a thermally evaporated 200 nm layer of gold [9], [10].

A device was manufactured with this structure and shipped to M-Solv for interconnection via OSI. The process parameters used can be seen in Table 5.3. The key differences between the processing on CSU and CSER material are:

- The same laser frequency is now used for both A and B scribe, it was found that it was not detrimental to performance and is preferable due to the experimental setup. It is not currently possible to automatically adjust the laser frequency mid-process therefore using the same frequency allows full automation of the laser processing step with the different spot sizes obtained by shifting focus using a motorised z-axis.
- The insulating ink was swapped from Sun U7878 to Inktec IUSSLB01 as it was found to be more stable at high temperatures.
- Plasma surface treatment is used as it was found to reduce cracking of the metal.
- The nominal drop volume of the conductive ink is now 10pl compared to 30pl in the CSU work. The printhead had to be replaced due to malfunction and a 10pl nominal drop volume head was all that was available.

Process step	Parameter	Value
Laser - A scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	4.52
	Spot diameter (µm)	26
	Pulse duration (ns)	<12
	Pitch (µm)	10
	Optical setup	Focused Gaussian beam
Laser -B scribe	Wavelength (nm)	532
	Fluence (J/cm^2)	0.88
	Spot diameter (µm)	59
	Pulse duration (ns)	<12
	Pitch (µm)	12
	Optical setup	Imaging 750um mask
Clean	Solvent	IPA
	Duration (s)	300
	Plasma	Yes
Insulator IJ	Ink manufacturer	Inktec
	Identifier	IUSSLB01
	Drop pitch (µm)	63.5
	Nominal drop volume (pl)	10
Insulator Cure	Lamp type	Mercury
	Dose (mJ/cm^2)	151
Conductive IJ	Ink manufacturer	Sun Chemical
	Identifier	U8025
	Metal type	Nanoparticle
	Material	Ag
	Loading (% by wt)	40
	Drop pitch (µm)	25
	Nominal drop volume (pL)	10
	Number of passes	5
Conductive sinter	Time (minutes)	60-90
	Temperature (°C)	170

Table 5.3: Process parameters of mini-modules fabricated on CSER CdTe

5.2.1 CSER mini-module

Optical images and white light interferometer profiles of all three stages of OSI on sample 1 of the CSER material can be seen in Figure 5.9.

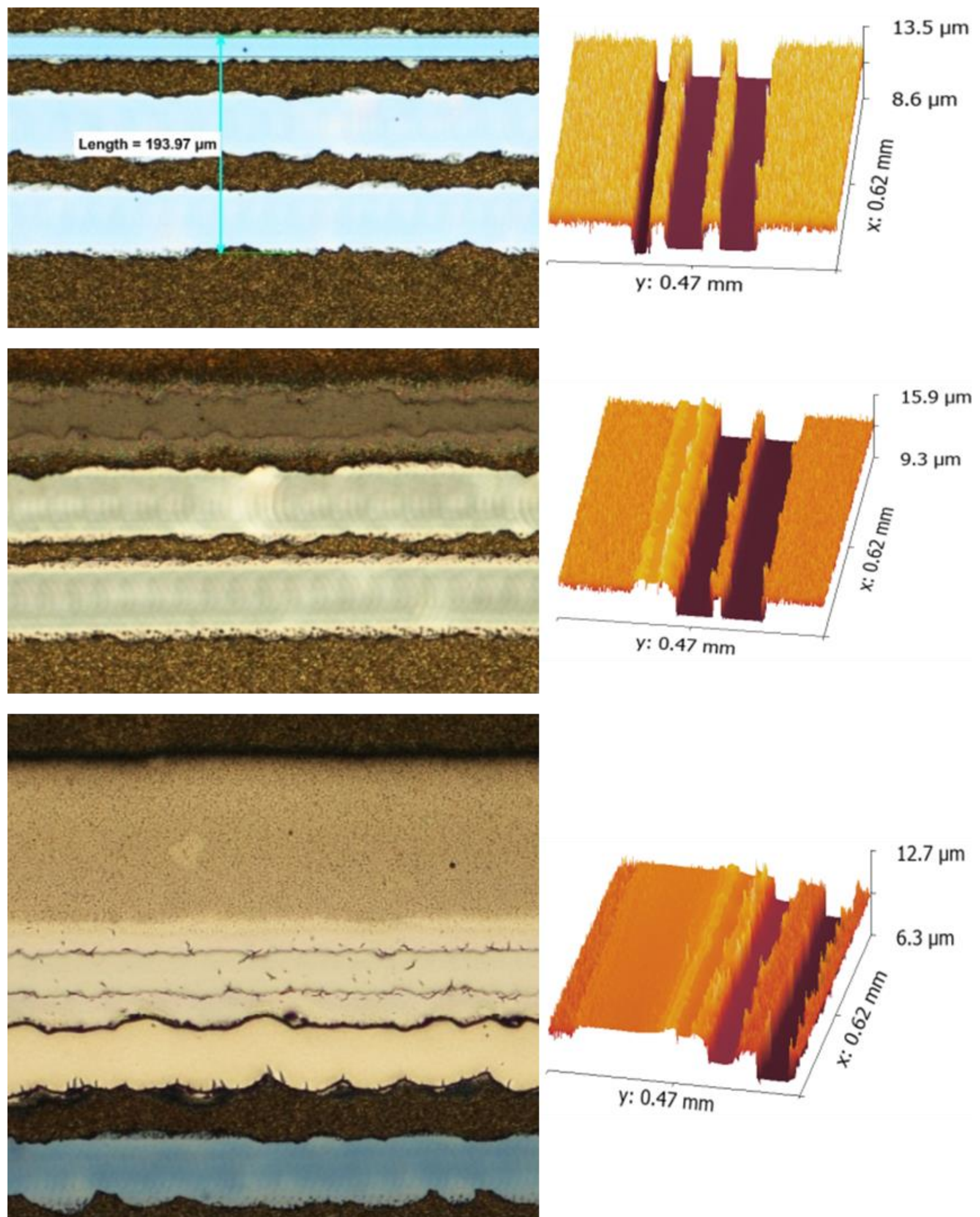


Figure 5.9: Optical images and white light interferometer plots of the three stages of the OSI process on sample 1 of CSER CdTe. Top left laser scribes, top right after insulator fill, bottom completed interconnect

The silver ink deposited on the CSER samples has reduced cracking compared with the CSU samples, Figure 5.9, this was attributed to the inclusion of the plasma surface treatment. A cell pitch of 0.5 cm was chosen with 12 cells per sample, each cell was approximately 3 cm wide leading to a cell area of 1.5 cm. Sample 1 had a printing defect in an approximately semi-circular section in the bottom right of the sample which caused silver ink to short cells 9 and 10 an optical microscope image of the printing defect can be seen in Figure 5.10. It is believed that the printing defect was caused by improper sample handling, as it is approximately thumb shaped, a diagram of the affected area can be seen in Figure 5.10. Cell 12 was too close to the bottom edge to test, giving a total of 9 cells on sample 1. The electrical results of sample 1 can be seen in Table 5.4

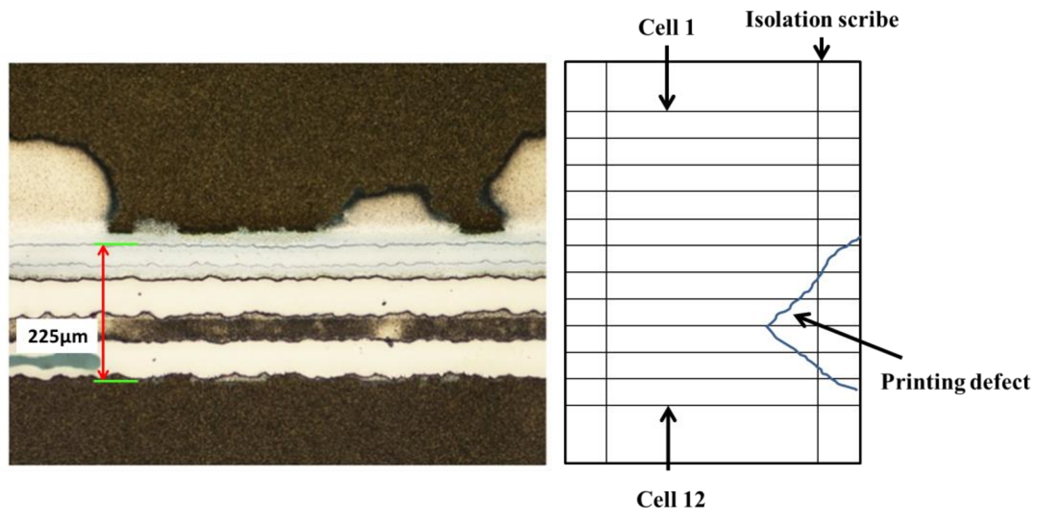


Figure 5.10: Left; An example of the printing defect found in a localised area of sample 1, the conductive ink has shorted the P3 scribe. Right; a diagram of the location affected by the printing defect.

Cell	1	2	3	4	5	6
Efficiency (%)	11.42	11.13	11.03	10.66	11.05	10.64
Jsc (mA/cm2)	23.31	23.06	23.05	23.17	23.04	22.79
Voc (V)	0.72	0.72	0.71	0.70	0.71	0.70
FF (%)	67.72	66.99	67.00	65.57	67.59	66.40

Cell	7	8	11	Average	SD
Efficiency (%)	10.48	10.86	11.43	10.97	0.32
Jsc (mA/cm2)	22.62	22.57	21.93	22.84	0.40
Voc (V)	0.69	0.70	0.71	0.71	0.01
FF (%)	66.80	68.37	73.38	67.76	2.13

Table 5.4: Electrical characteristics of CSER sample 1 after OSI processing; each cell is 0.5x3cm.

CSER also deposited small, 1cm^2 reference samples at the same time as the main mini-module, processed by OSI. The reference cell area is defined by a shadow mask used during sputtering of the gold back contact. There is no interconnection on the reference cells, instead an area of TCO is left exposed for direct contact to be made. 2 reference cells were manufactured at the same time as sample 1. CSER cells require a post deposition anneal to reach maximum performance, the samples for OSI were left without this anneal so that the thermal ink sintering step could occur while keeping the total thermal budget the same between OSI and reference samples. The initial ink sintering bake was 170°C for 60 minutes. A comparison of the average OSI cell and the 2 reference cells can be seen in Table 5.5.

Cell	Average OSI	Reference 1	Reference 2
Efficiency (%)	10.97	12.34	11.93
Jsc (mA/cm2)	22.84	25.77	25.66
Voc (V)	0.71	0.71	0.71
FF (%)	67.76	67.50	65.81

Table 5.5: Electrical characteristics of two $1cm^2$ reference cells deposited at the same time as sample 1. Both the reference and OSI cells underwent the same thermal processes. Although the efficiency of the OSI cells is lower than the reference the average FF is actually slightly higher. The lower current density has been attributed to the coating uniformity over the larger samples.

On first inspection the performance of the OSI cells is poor in comparison with the reference cells however the reduction in performance is due to a low current density. Current density is an intrinsic material property which should not be affected by the series interconnection. The average fill factor is actually slightly higher than the reference cells which indicates good series interconnection. The origin of the reduction in current density is attributed to lateral coating non-uniformities of the deposited photovoltaic stack. The smaller $1cm^2$ cells are square and use only the centre of the device whereas the larger OSI cells are 3cm long and so use material from the edge of the device. Evidence of coating non-uniformity can be seen in two ways. Firstly, variations in film thickness can be seen using a white light interferometer. At the centre of the sample the CdZnS/CdTe stack measures ~3.1 µm whereas at the edge, approximately 2 cm from the centre, the stack measures ~2.8 µm. Secondly, further evidence for coating non-uniformity can be seen when plotting cell characteristics as a function of cell number, see Figure 5.11. As the location of the measured cell changes in the long axis of the sample, the intrinsic electrical characteristics of current density and voltage decrease linearly. Assuming a similar variation along the direction of the interconnect scribes would explain the reduction in cell performance from incorporating longer devices. A conclusive way to determine if this is the case would be to run isolation scribes at 1 cm intervals perpendicular to the OSI interconnects and measure them as 3 separate cells. Although this would provide insight into the cause of these performance differences the complete mini-module was judged to be more valuable as a baseline from which to examine life-time stability of OSI interconnects, see later in chapter.

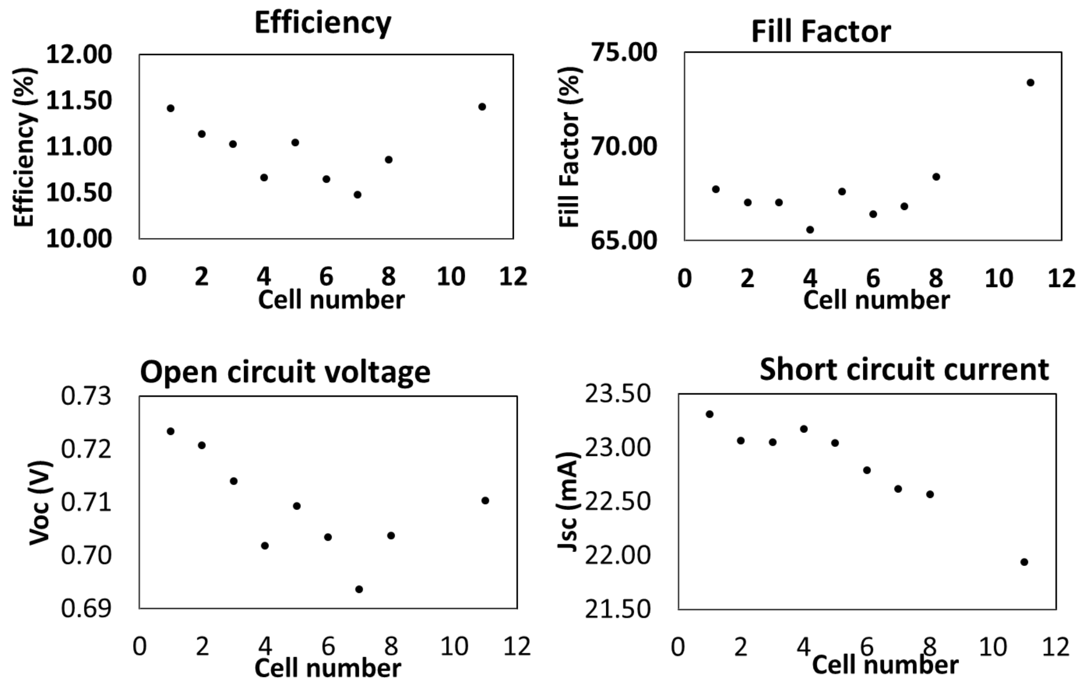


Figure 5.11: Plots of efficiency fill factor, open circuit voltage and short circuit current of 9 OSI interconnected cells on CdTe deposited by CSER. The steady decline in current density and voltage along the device is evidence of coating non-uniformity.

Feedback from CSER indicated that the performance of the OSI cells was not as high as expected. A further anneal of 170°C for 30 minutes was suggested, bringing the total up to 90 minutes. This was found to improve all of the electrical characteristics of the OSI cells except for V_{oc}. The change in electrical performance can be seen in Table 5.6. Current density has improved however is still low compared to the reference cells. The increased fill factor is predominantly due to a decrease in series resistance from 2.3Ω to 1.7Ω which can be explained by an increase in conductivity of the conductive ink due to the extra thermal processing, this indicates that the original bake was not optimum for sintering of this ink. The fill factor is now significantly higher than the references cells, something which may be attributed to the increased shunt resistance from having a highly resistive dielectric material in the A scribe. The decrease in voltage is not fully understood but could be related to appearance of pinholes throughout the cells which have been attributed to the conductive tape used to connect the source meter of the solar simulator, ripping off areas of cell with poor adhesion. Examples of these pinholes can be seen in Figure 5.12.

	Before anneal	Change	After anneal	Reference 1	Reference 2
Efficiency (%)	10.97	+0.42	11.38	12.34	11.93
Jsc (mA/cm^2)	22.84	+0.30	23.13	25.77	25.66
Voc (V)	0.71	-0.01	0.70	0.71	0.71
FF (%)	67.76	+3.03	70.79	67.50	65.81

Table 5.6: Average change in electrical characteristics brought on by an extra 30 minute anneal at 170 °C.

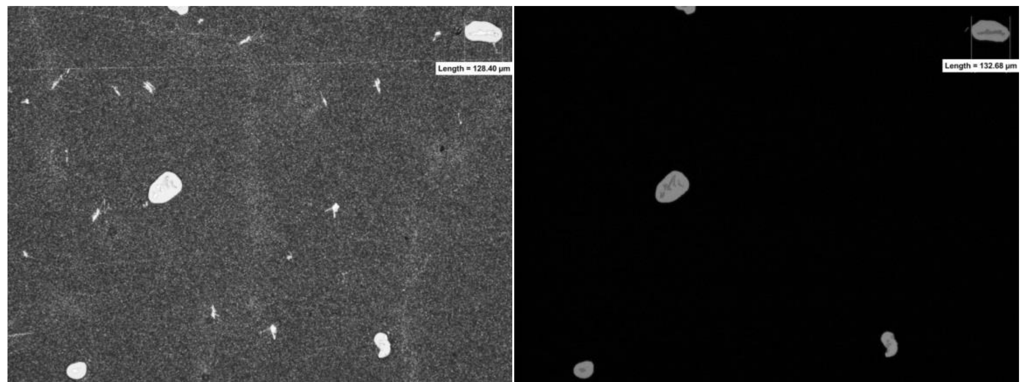
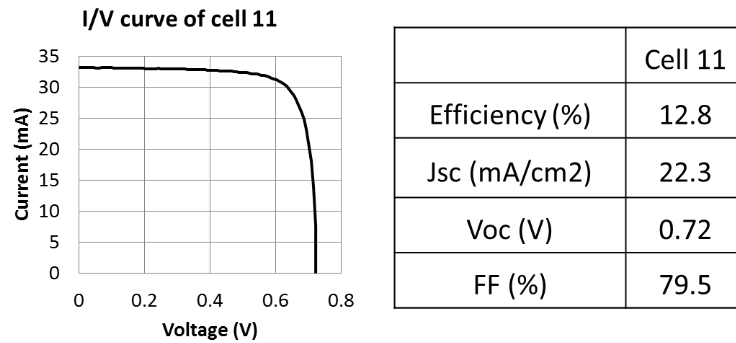


Figure 5.12: Optical images of pinholes caused by removing conductive adhesive tape used for connection to the solar simulator probes. Left; top down lighting. Right; the same section with backlight only. It can be seen that the pinholes are down to the TCO.

After the further anneal it should be noted that although the average cell performance is still behind that of the reference cells, the best OSI interconnected cell, cell 11, has an efficiency of 12.82% which is around 0.5% absolute higher than the best reference cell. The electrical characteristics and I/V curve for Cell 11 can be seen in Figure 5.13. The principal reason for the higher efficiency is an extremely high fill factor of 79.5 %; the voltage is also slightly higher at 0.72 V. If the current density, which as stated previously is believed to be low due to coating non-uniformity were at the same level as the best reference cell, 25.77mA/cm^2 then the efficiency would be ~14.8% which would be a very respectable CdTe efficiency, close to the maximum achieved by Glyndwr on small reference cells, ~15.5%. This shows a straight forward route for further material development.



	Cell 11
Efficiency (%)	12.8
Jsc (mA/cm2)	22.3
Voc (V)	0.72
FF (%)	79.5

Figure 5.13: I/V curve and electrical characteristics of cell 11. The efficiency is higher than the reference cells made during the same deposition run, even though the current density is significantly lower. The good efficiency is mostly due to the high fill factor.

5.3 Comparison of OSI with the conventional process

All indications from the previous section are that OSI is working well however a direct comparison to a conventional module would be more conclusive therefore it was decided to manufacture one. Fluorine dope Tin Oxide (FTO) substrates were received at M-Solv for P1 scribing. It was found that the highest isolation values and the lowest number of scribe defects resulted from glass side, 532 nm scribing of the FTO. The cell pitch was 0.5 cm.

In CdTe modules grown on soda lime glass, it is required to modify the conventional process with an insulative plug in the P1 scribe to avoid Na diffusion from the glass interfering with the CdTe crystallisation [11]. The process flow for the industrial process must therefore be modified to stop this Na leaching [12], [13]. The modified process is deposit FTO, CdS and CdTe then laser scribe P1, to the glass. A uniform coating of a UV curable photoresist is then coated over the panel and the resist is exposed through the glass so it is cured only in the P1 scribes [13]. The panel is then P2 scribe and returns to the normal process flow of activation, back contact deposition and P3 scribe. The resulting structure can be seen in Figure 5.14. Samples grown without this photoresist deposition step delaminate around the P1 scribes where Na contamination occurs.

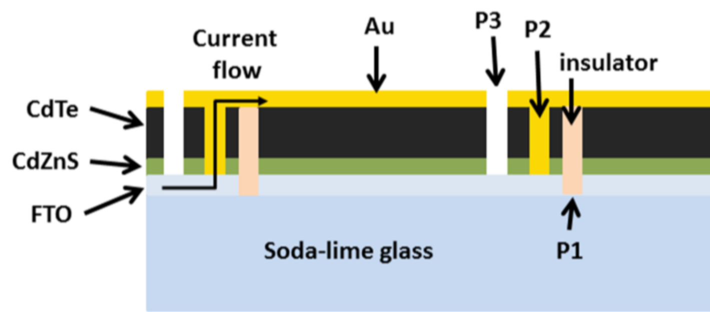


Figure 5.14: [11] The structure resulting from the modified conventional interconnect process used to stop Na diffusion from the glass exposed during the P1 scribe interfering with CdTe growth. The resist is deposited uniformly on the panel after the CdTe deposition, it is then exposed through the glass curing the resist only where there are holes in the CdTe.

In order to manufacture comparable modules inkjet was used to selectively infill the P1 scribes leaving the same structure as the modified conventional process, Figure 5.14. I/V curves of a 7 cell mini-module manufactured in this way and one manufactured with OSI can be seen in Figure 5.15. It can be seen that the efficiency of the OSI mini-module is ~0.4% higher than the conventional process, due mainly to an increased current density. This is likely not related to OSI but due to batch to batch variation in the grown CdTe. The FF of the OSI module however is also higher than the conventional which could be related to the interconnect. The main reason for the increased FF appears to be a lower series resistance of 3.17 Ω/cell for OSI compared to 4.02 Ω/cell for the conventional process. This is a good indication that OSI is working at least as well as the conventional process.

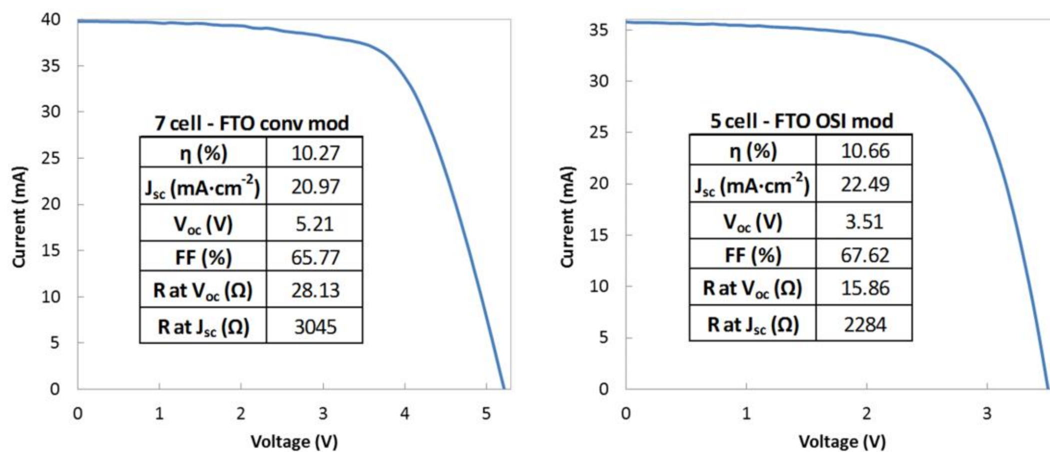


Figure 5.15: Comparison of conventional and OSI CdTe mini-modules grown on FTO substrates. The efficiency of the OSI module is higher due to higher current density and higher fill factor. The OSI modules fill factor is higher due to a lower series resistance which is a good indication that OSI is working well.

5.4 Accelerated lifetime testing

An important consideration for photovoltaics is longevity. Panels are typically warranted for 10-25 years. For example First Solar offer a warranty for their CdTe modules covering materials and workmanship for 10 years, 90% power output for the first 10 years and 80% power output for 25 years [14]. Therefore an interconnect technology like OSI must be long lasting to be accepted by panel manufacturers. The International Electrotechnical Commission (IEC) publish standards for all electrical and electronic technologies, the one relating to thin-film PV is "IEC61646: Thin-film terrestrial photovoltaic (PV) modules – Design, qualification and type approval" [15]. This standard is one that all thin-film modules must pass to be certified for use in most EU countries. The IEC qualification procedure is detailed in Figure 5.16 it includes tests designed to characterise the material, such as measuring performance at standard test conditions (STC) and temperature coefficients as well as module design and structure, for example; hail test, mechanical load test or robustness of termination. Not all of these tests are applicable to OSI however there are two key tests that are useful; humidity freeze and thermal cycling. Since the IEC test protocols are designed to be used at the end of a production run with complete, full sized modules it is difficult to follow the entire test procedures exactly however they will be used to guide this initial accelerated lifetime testing.

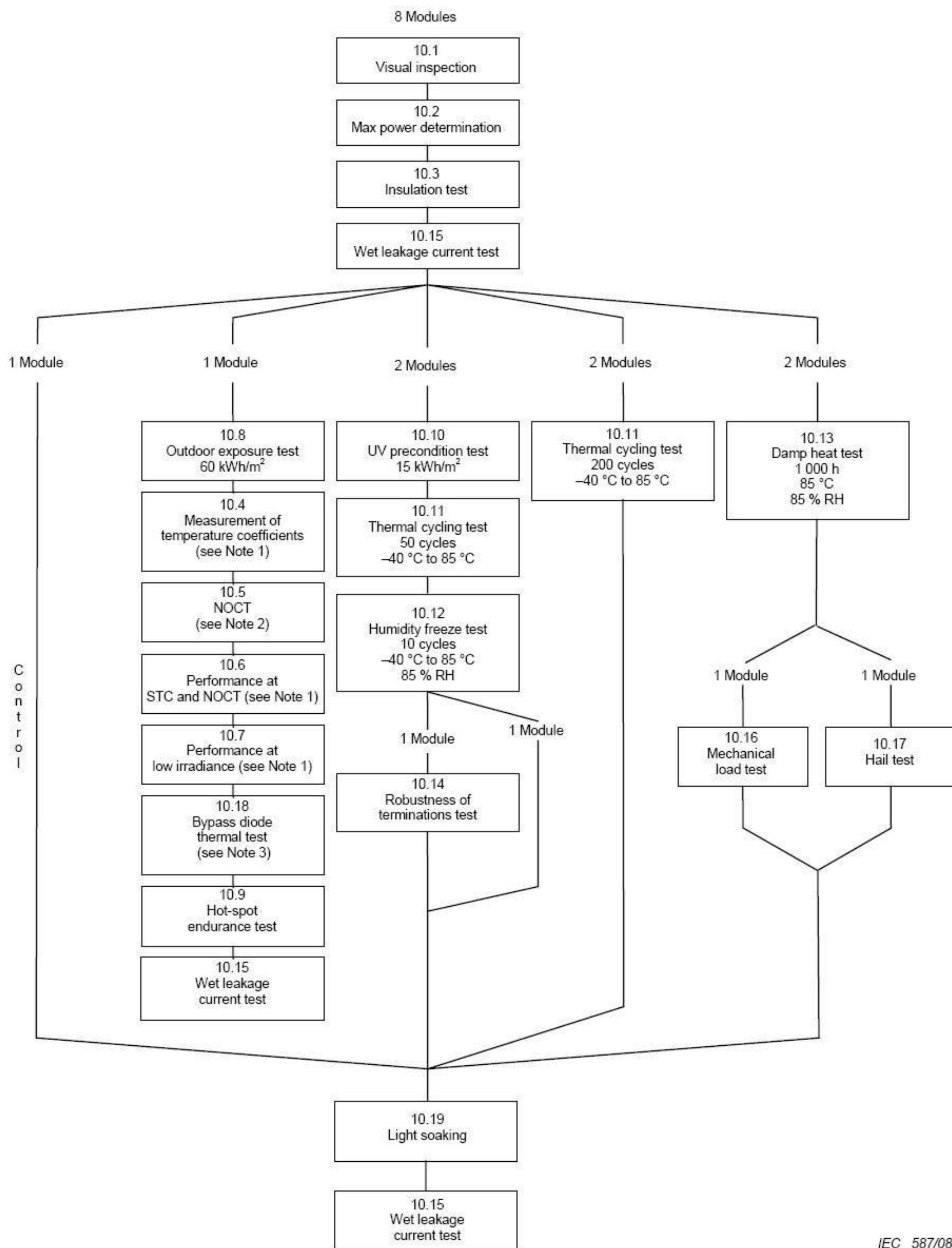


Figure 5.16: The IEC61646 standard testing protocol for the certification of thin-film PV.

5.4.1 Encapsulation and damp heat testing

The industry standard encapsulation for thin-film modules involves a second piece of glass being bonded to the film side of the glass substrate at a pressure of 1-5 bar and a temperature around 80-150 °C using an interlayer made of a transparent polymer material, the most common being Ethylene-vinyl acetate (EVA) [16]. During the bonding process the area between the two pieces of glass is evacuated to remove all air

and moisture. This, so-called, glass-glass lamination is widely accepted to be robust enough to prevent moisture ingress which damages cell performance [17], [18], some manufacturers use an extra edge seal to further decrease moisture permeation [19]. A PVLAM 1.0 laminator was purchased by M-Solv from EETS, Pontypridd, South Wales. Using the PVLAM 1.0 a lamination process similar to industry was developed using glass to glass and an EVA interlayer.

The humidity freeze test evaluates the encapsulation integrity, particularly resistance to water ingress. It is important that the encapsulation be resistance to moisture since any it degrades device performance through oxidation or by allowing migration of dopants. Humidity freeze testing involves the cycling of temperature from -40°C to +85°C at a relative humidity of 85%. This mechanically stresses the module in the presence of moisture which would result in ingress if it were not properly sealed. This portion of lifetime testing was undertaken by CREST at Loughborough University and due to restraints imposed by the available equipment it was necessary to change the humidity freeze testing to damp heat testing. Damp heat testing holds the module at 85°C/85% relative humidity, although the module will be less stressed by damp heat than humidity freeze it is still thought that the damp heat test will give a good indication of packaging integrity.

In order to separate the two questions of encapsulation integrity and OSI cell performance it was decided to use a conventionally interconnected mini-module for this test. A thin-film silicon module from a well-established manufacturer was chosen since it was easily available. The module was laminated at M-Solv using the previously developed EETS laminator and EVA process. The module is heated to 153°C for 150 seconds, the chamber is then pumped to vacuum and held there for 420 seconds, still at a temperature of 153°C. In preparation for encapsulation a strip of material, 1cm wide, is removed from the edge of each module. This process, termed ‘edge deletion’, uses many A scribes next to each other to remove all the active layers, allowing the EVA to bond glass to glass rather than to any of the active layers, resulting in better adhesion. To allow electrical connection to the encapsulated module tabs of 3M Charge Collection Tape, 3007, are stuck to the back contact of the first and last cells. This tape is made of tin-plated copper foil with a pressure sensitive, conductive adhesive for electrical contact and is designed for use in PV manufacturing processes. An example of an encapsulated mini-module can be seen in Figure 5.17.

Figure 5.17: A mini-module encapsulated at M-Solv for damp heat testing. Two pieces of glass sandwich the active layers, a 1cm boarder has been laser edge deleted around the perimeter of the module to aid adhesion. 3M charge collection tape allows electrical connection.

The cells performance was measured straight after lamination and placed into a damp heat chamber. Measurements were taken regularly for the first 2 weeks, around every 2 days, after two weeks further measurements were taken at 3, 4 and 6 weeks. Total test time was ~1000 hours; a graph of efficiency against test time can be seen in Figure 5.18. After the 1000hours damp heat there was no visible sign of water ingress and no degradation in device performance. The results are not as clear as hoped though since the module efficiency continues to rise. The mechanism for this is the, well documented, Staebler-Wronski effect [20]. In hydrogenated a-Si, as used in TF-PV, certain recombination pathways of photo-generated electron-hole pairs result in breaking of Si-H bonds, allowing migration of hydrogen. This mobile hydrogen can form metastable defects which degrade cell performance. Annealing of the same a-Si material forces the Hydrogen back into the original positions and thus restores cell performance.

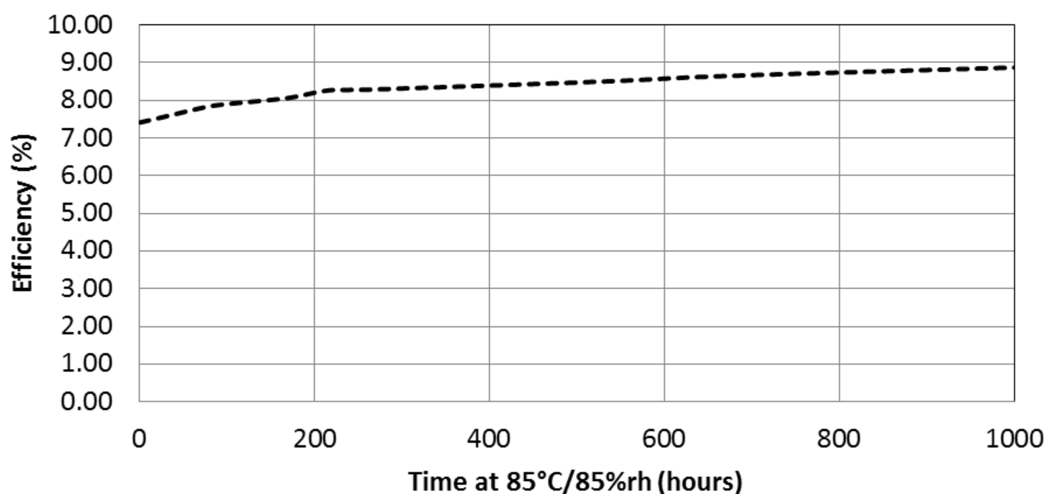


Figure 5.18: Plot of mini-module efficiency against time in damp heat. The rise is due to annealing of defect states, the Staebler-Wronski effect.

The a-Si used in this test was stored in a well-lit laboratory for around 6 months before this test and would therefore have been expected to have degraded due to the Staebler-Wronski effect. Typical values for the amount of degradation are expected to be 8-15% of the starting value which corresponds to a rise of ~18% due to annealing, consistent with the results of the damp heat test which shows a rise of ~20%. The electrical results combined with the fact that there were no visible signs of water ingress or packaging damage indicates that the package integrity is good. The same encapsulation process can therefore be used to assess the robustness of encapsulated OSI interconnected mini-modules.

5.4.2 Thermal cycling

Thermal cycling, as the name suggests, involves periodic changes in temperature of the encapsulated modules. The IEC standard is temperature cycles from -40°C to +85°C for 200 cycles. A Binder MK53 environmental chamber was used for running temperature cycling tests on OSI samples. A complete cycle lasts ~2.5 hours and humidity is controlled during ramp up to prevent condensation forming on the sample. CSER mini-module 1 described above was used for these tests. A ~30% drop in efficiency was observed after encapsulation attributed to the formation of more pinholes from further removing and reapplying conductive tape to the back contact of the module, again described above. Cell 3 was damaged so much as to become non-functional and the edge deletion removed cell 1 and part of cell 2, leaving cells 4-8 and

11 functional. After encapsulation a measurement was taken and this was used as the 0 cycle measurement for comparison purposes. The average efficiency after encapsulation was 8.2%.

Since performance of the individual cells was highly variable, ±1.9% about the average value, it was decided to add contact strips to each cell so they could be individually monitored. Mini-module 1 was placed into the environmental chamber and removed every 1-3 days for measurements to be taken. A total of 422 cycles were completed, more than double the requirement for IEC certification. The results are shown in Figure 5.19.

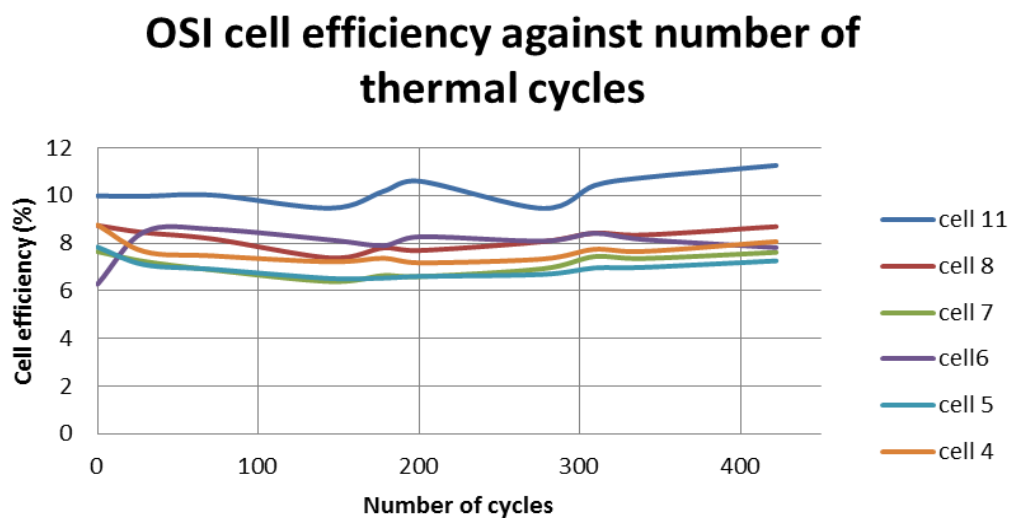


Figure 5.19: Efficiency of OSI interconnected cells against number of temperature cycles from -40°C to +85°C.

The pass criterion for IEC certification is that the panel is not less than 90% of the minimum specified by the manufacturer after 200 cycles. Interpretation of the data with this criterion in mind is difficult. There were no catastrophic failures brought on by thermal cycling, at all measurement points the average of the 6 cells is always >90% of the starting values and after all 422 cycles all cells are >90% of their starting values. Using these factors only it can be said that the result of the thermal cycling is positive. However looking at the trend over time it is less clear cut. At 200 cycles 4 of the 6 cells are <90% of the starting value, the large initial rise in cell 6 compensates for this and on average all cells are only 4% down. It can be argued that if these cells were a connected in series as in a complete mini-module then the performance would average out and the results would look much more positive, an average of all cells can be seen in Figure 5.20. These initial accelerated life-time experiments are promising, there are no

obvious failures and they look to be broadly in-line with the IEC specification but it should be highlighted that further testing is required to conclusively determine whether OSI is adequately robust for production.

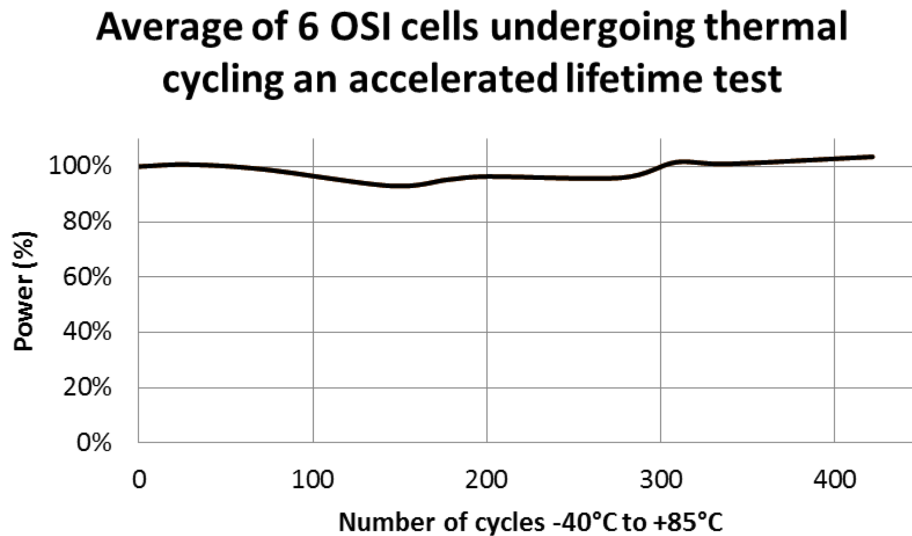


Figure 5.20: Average cell performance of the 6 OSI cells undergoing thermal cycling. At all time points the average cell performance is greater than 90%.

5.5 Conclusion

OSI has been taken from an idea, through the development cycle to proof of concept. Although the process development has been time consuming and relatively difficult this chapter demonstrates that OSI can work as a module interconnection technology and can provide comparable if not better results than the incumbent process. The initial lifetime testing data is extremely positive with no failures found and it gives an indication that OSI can pass the IEC qualification process. However there is still a long way to go until OSI is production ready. Currently all mini-modules are manufactured in discrete stages with the laser, insulator and conductor deposition steps happening independently with some intermediate steps required such as cleans or surface treatments and the manufacture of single mini-modules taking anywhere up to a full week of work.

The biggest hurdle to true OSI is currently the machine architecture of the small development rig which has been used for all tests to date since it is limited to laser and inkjet from the same side of the substrate. The next step is the design and build of a dedicated, true OSI machine to show that this concept can work in a production mode.

This is currently happening at M-Solv. Once the new machine is online, OSI can be taken to the next stage of development which will include the manufacture of multiple interconnects at once and at process speeds compatible with PV production lines. This will allow many mini-modules to be made so that statistical data can be gathered on performance and a full range of accelerated lifetime testing can be performed.

5.6 References

[1] M.L.Crozier, A.N.Brunton, A. Abbas, J.W.Bowers, P. M. K. J.D.Shephard, and J.M.Walls, "One step thin-film PV interconnection process using laser and inkjet," in *39th IEEE PVSC conference proceedings*, 2013.

[2] M. L. Crozier, A. Brunton, M. Jiang, S. Henley, J. Shephard, A. Abbas, J. Bowers, P. M. Kaminski, and J. M. Walls, "Inkjet and laser hybrid processing for the series interconnection of TF-PV," in *10th Photovoltaic Science, Applications and Technology (PV-SAT 10)*, 2014.

[3] M. L. Crozier, A. Brunton, G. Kartopu, and S. Irvine, "A one step process for the series interconnection of thin-film PV," in *SNEC 8th International Photovoltaic Power Generation Conference*, 2014.

[4] M. L. Crozier, P. Adamson, A. Brunton, S. J. Henley, J. D. Shephard, G. Kartopu, S. J. C. Irvine, P. M. Kaminski, and J. M. Walls, "Recent developments toward a one step thin-film PV interconnection process using laser scribing and inkjet printing," *IEEE 40th Photovolt. Spec. Conf.*, vol. 1, pp. 2784 – 2788, 2014.

[5] S. D. Hodgson, G. Kartopu, M. L. Crozier, P. Adamson, V. Barrioz, S. Rugen-Hankey, E. Tejedor, D. Dupin, A. J. Clayton, W. S. M. Brooks, D. A. Lamb, A. Brunton, and S. J. C. Irvine, "Performance of EVA Encapsulated CdTe Devices and Micro-Modules Grown by MOCVD under Heat/Humidity Testing," in *29th European PV Solar Energy Conference and Exhbition (EUPVSEC)*, 2014, pp. 1840 – 1843.

[6] D. E. Swanson, R. M. Geisthardt, J. T. McGoffin, J. D. Williams, and J. R. Sites, "Improved CdTe Solar-Cell Performance by Plasma Cleaning the TCO Layer," *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 838–842, Apr. 2013.

[7] C. A. Volkert, A. M. Minor, G. Editors, and B. May, "Focused Ion Beam Micromachining," vol. 32, no. May, pp. 389–399, 2007.

[8] S. Reyntjens and R. Puers, "A review of focused ion beam applications in microsystem technology," vol. 287, 2001.

[9] G. Kartopu, A. . J. Clayton, W. S. M. Brooks, S. D. Hodgson, V. Barrioz, A. Maertens, D. A. Lamb, and S. J. C. Irvine, "Effect of window layer composition in Cd1-xZnxS/CdTe solar cells," *Prog. Photovoltaics Res. Appl.*, vol. 22, no. 1, pp. 18–23, 2014.

[10] G. Kartopu, A. A. Taylor, A. J. Clayton, V. Barrioz, D. A. Lamb, and S. J. C. Irvine, "CdCl2 treatment related diffusion phenomena in Cd1-xZnxS/CdTe solar cells," *J. Appl. Phys.*, vol. 115, p. 104505, 2014.

[11] G. Kartopu, M. L. Crozier, A. Brunton, B. L. Williams, V. Zardetto, V. Barrioz, S. Hodgson, S. Jones, W. M. M. Kessels, M. Creatore, and S. J. C. Irvine, "Comparative study of conventional vs . one-step-interconnected (OSI) monolithic CdTe modules," in *11th Photovoltaic Science, Applications and Technology (PV-SAT 11)*, 2015.

[12] M. Rekow, R. Murison, C. Dinkel, T. Panarello, S. Nikumb, and W. S. Sampath, "Selective removal of TCO stack layers for CdTe P1 process with a tailored pulse laser," *Conf. Rec. IEEE Photovolt. Spec. Conf.*, pp. 002813–002819, 2011.

[13] B. M. Basol and B. McCandless, "Brief review of cadmium telluride-based photovoltaic technologies," *J. Photonics Energy*, vol. 4, p. 040996, 2014.

[14] First Solar, "FS Series 3 TM Black PV Module Product Datasheet," 2014.

[15] IEC, "IEC Standard 61646: Thin-film terrestrial photovoltaic (PV) modules – Design, qualification and type approval," 1998.

[16] A. Plessing, "Method for producing photovoltaic thin film module," US 20030029493 A12003.

[17] a. W. Czanderna and F. J. Pern, "Encapsulation of PV modules using ethylene vinyl acetate copolymer as a pottant: A critical review," *Sol. Energy Mater. Sol. Cells*, vol. 43, pp. 101–181, 1996.

[18] F. . Pern, S. . Glick, and a. . Czanderna, "EVA encapsulants for pv modules: Reliability issues and current R&D status at NREL," *Renew. Energy*, vol. 8, pp. 367–370, 1996.

[19] P. E. Meeks, "Method for edge sealing barrier films," US 6866901 B22007.

[20] A. Kołodziej, "Staebler-Wronski effect in amorphous silicon and its alloys," *Opto-electronics Rev.*, vol. 12, no. 1, pp. 21–32, 2004.

Chapter 6 : The case for OSI

The PV industry is cost driven. If a new technology offers a lower cost per Watt manufactured then it will be implemented. The question is then: Does OSI offer a significant saving over the incumbent process? This will be addressed briefly in this Chapter.

6.1 Benefits of OSI

There are many benefits of OSI and they can be separated into two categories. Cost benefits, anything which directly reduces the cost of manufacturing of a panel and include aspects such as reduced capital expenditure to setup a production line. The second category are process benefits, anything that has an indirect effect on the cost per Watt, things like increasing efficiency or lifetime. Some of the main benefits are explored in more detail in the following sections.

6.1.1 Reduced Line Length

One of the key selling points of OSI is replacing three laser scribers with one OSI tool thus shortening the production line. Other ancillary equipment can also be removed since the deposition processes do not need to be interrupted for scribing. Detailed line information was obtained from an industrial collaborator which allowed estimation of the impact of OSI on line length for a CdTe manufacturing process. Figure 6.1 shows the production line with the conventional process, this differs from some other CdTe manufacturing flows in that the TCO is ITO and deposited in house rather than buying NSG, FTO coated, TEC glass as the substrate on which to deposit the PV stack.

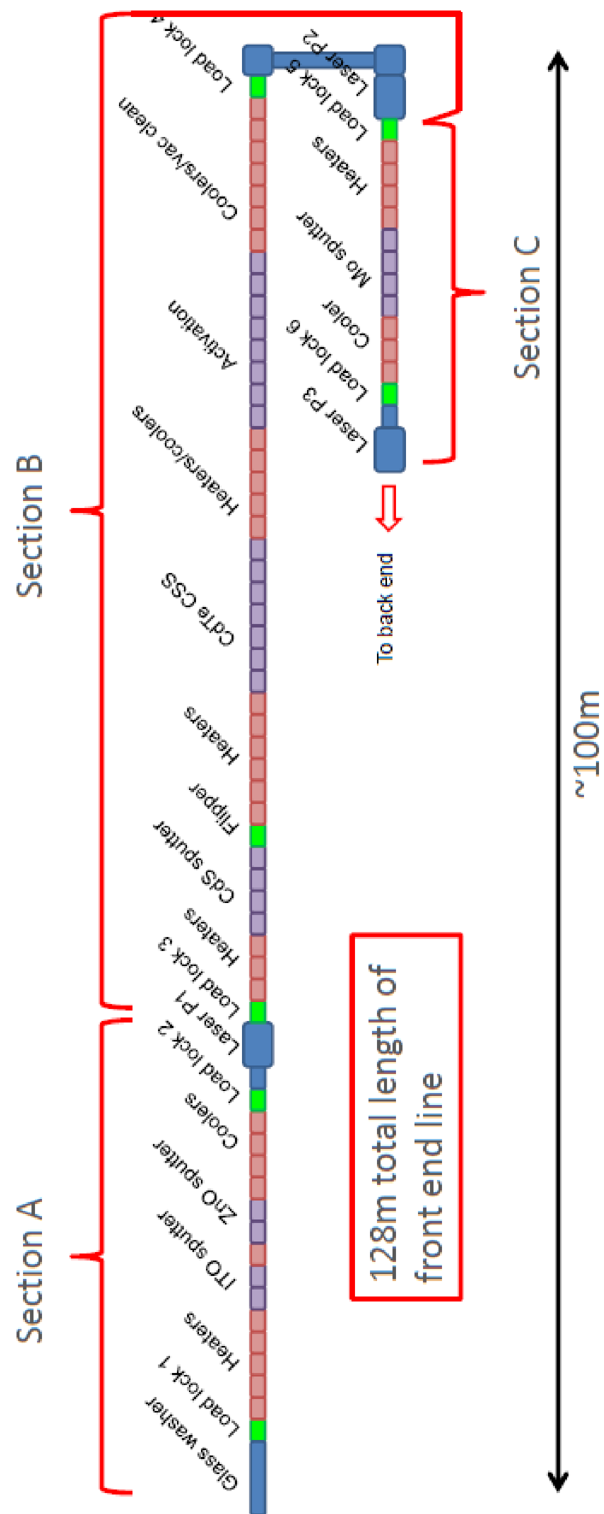


Figure 6.1: A CdTe production line using the conventional interconnect process. Section A is the TCO deposition and P1 scribe, section B the junction deposition, activation and P2 scribe and section C the back contact deposition and P3 scribe.

This production line can be used as a case study to assess the impact of OSI. The obvious change is the removal of the ‘Laser P1’ and ‘Laser P2’ stations and ‘Laser P3’ is changed to an ‘OSI tool’. The deposition must occur at defined temperatures:

- TCO (ITO/ZnO(buffer)) – 400°C
- CdS – 250°C
- CdTe – 500°C
- Activation ($CdCl_2$) treatment – 400°C
- Back contact (Mo) – 250°C

The quality of the deposition is critically temperature dependent. The glass panel can only be heated/cooled at a defined rate so as not to overly stress the glass which can result in breakages, in this line the temperature slew is ~75°C per station. The laser processes must happen in ambient conditions to avoid contamination of vacuum equipment with laser debris and the vacuum/air transitions occur at room temperature again so as not to stress the glass. Taking all these things into account produced an OSI modified production line seen in Figure 6.2.

Removing the laser scribing steps and the associated air/vacuum and temperature transitions also allows the removal of many heating/cooling stations and load locks further simplifying the line. The total length has been reduced by ~25% by incorporating OSI.

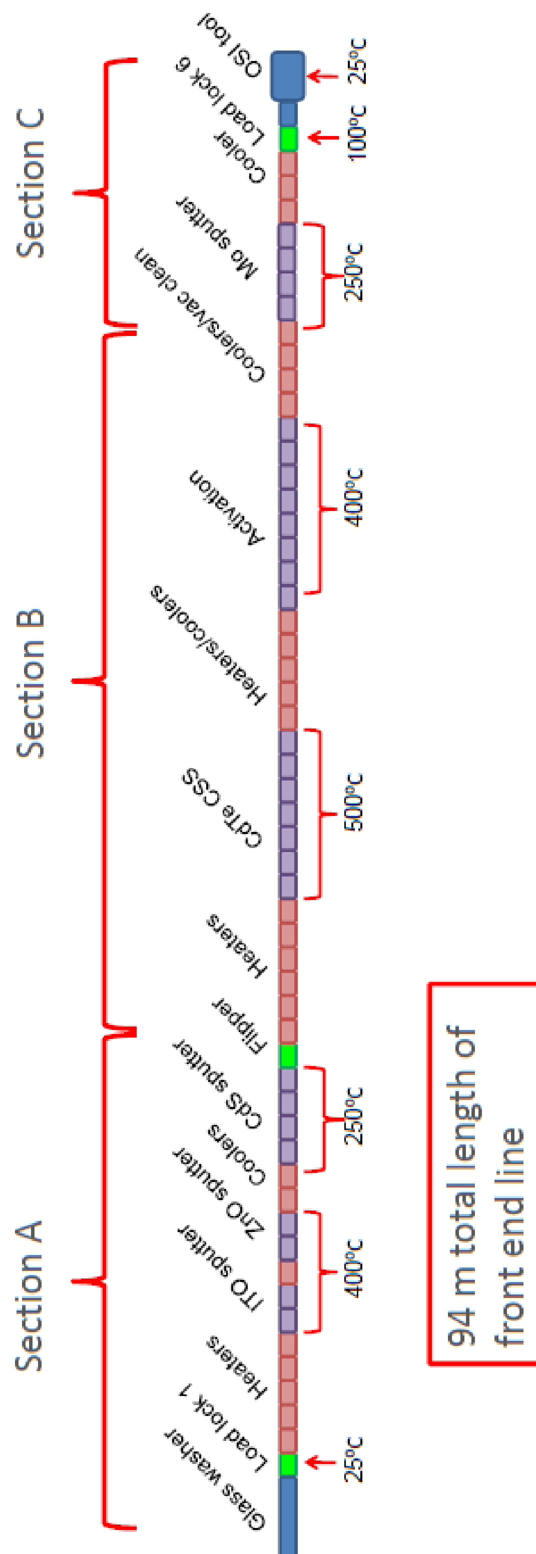


Figure 6.2: The same CdTe production line modified by the incorporation of OSI. Many heating and cooling stations can be removed since the panel does not have to leave vacuum for scribing processes.

The reduced line length has a number of benefits. Firstly the factory foot print is smaller which allows the use of a smaller factory which may reduce the rental overhead. The transit time of a panel through the line is reduced since there are less processing

steps. A reduced number of process steps should also translate to less equipment to breakdown increasing production line uptime. The temperature profile of the glass as it transits the line is also flatter which means the manufacturing process should be less energetic, reducing energy overheads for heating/cooling and reducing thermal stress in the glass. Less thermal stress should reduce the number of glass breakages and potentially reduce strain in the active layers. The reduced thermal budget of the manufacturing process has been modelled and the total temperature change experienced by the panel is reduced from Δ1500°C to Δ1100°C a reduction of ~25%. The temperature profiles of the panel during the conventional and OSI processes can be seen in Figure 6.3.

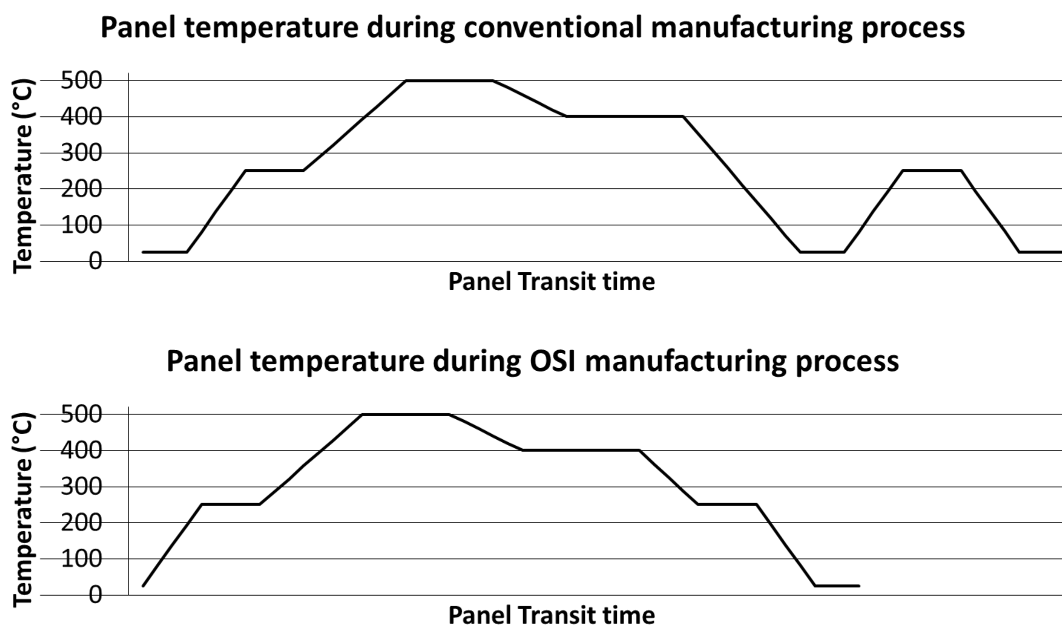


Figure 6.3: The temperature profiles experienced by the panel as it transits the production line with the conventional process (top) and the OSI process (bottom). The total reduction in panel temperature change is 400°C or ~25% by incorporating OSI.

The OSI benefits described above are a combination of process and cost benefits but the actual impact on cost is difficult to quantify as it is a reduction of unknown overheads and perceived benefits. The next section deals with a direct cost benefit, the cost of ownership (CoO) of the interconnect tooling and a model has been developed to quantify this.

6.1.2 Reduced total cost of ownership of interconnect tooling

The most direct cost benefit of OSI is the reduction in CoO of the interconnect tooling. The total CoO of the processes is calculated from the depreciation of the capital equipment, the dominant factor, and the cost of any consumables or required regular maintenance. M-Solv as a machine supplier is in a position to estimate this CoO as the costs of the tooling can be calculated internally.

The conventional process CoO is made up of three parts; depreciation of capital equipment, refurbishment cost of lasers after their lifetime is reached and replacement cost of optics as each beamline requires refurbishment. The cost of the equipment has been estimated internally and cannot be shared here but it is assumed that the equipment is written off over a 5 year period.

Assumptions made about the panels are as follows. The cell efficiency of the material is a rather modest 13.5%, the panels are 1.2x0.6m, the interconnects are on a pitch of 10mm and have a width of ~300µm. Using these assumptions the panel aperture efficiency is 12.71% due to the reduction in active area and negating resistive losses. Assuming a process speed of 0.5m/s, an achievable level of multiplexing and an uptime of 90% the process time per station or takt time is ~50s. This means that the production line outputs one panel every 50s and 1 conventional scribing tool processes ~52MW of panel per year assuming 90% uptime.

It is assumed that there is one laser per tool and that it has a lifetime of 15,000 hours of usage before needing refurbishment. It is also assumed that each of the multiple beamlines optics will need refurbishment on the same time scale. Making these assumptions the depreciation of the capital equipment dominates the CoO making up 73% of the total. The CoO normalised to the total cost can be seen in Figure 6.4.

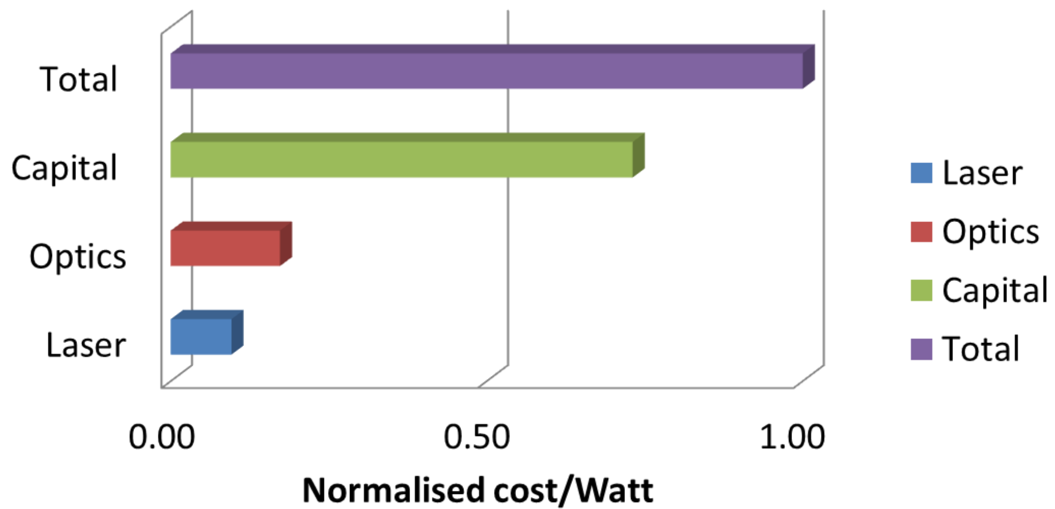


Figure 6.4: Breakdown of cost of ownership of the conventional process normalised to total cost.

The same type of model was setup for the OSI process. For OSI the CoO is made up of the same categories as the conventional process plus extra ones for printheads, inks and UV cure lamps. The same cell and panel assumptions are made as in the conventional process but the interconnect width is reduced to 220μm since all process steps are aligned on one process head. This reduction in interconnect width means that the panel efficiency is increased by 0.12% which although doesn't sound like much equates to an extra MW of output per tool per year for a total of 53MW making the same assumptions about process speed and multiplexing. The optics head designed for OSI is more efficient and therefore has a reduced cost of beamline refurbishment.

The OSI process has extra consumables both from lasers and optics and print hardware. There are 2 lasers per tool rather than 1 in the conventional process. Print hardware in the form of printheads and UV cure bulbs have to be replaced, the heads after 100 billion actuations and the bulbs after 2,000 hours. It is assumed that the ink geometry is optimum in terms of fill and spread and that 10% is wasted in priming and maintenance cycles. Taking all of these things into account the total is still dominated by capital equipment cost at 52% with the ink making up 27%. A breakdown can be seen in Figure 6.5.

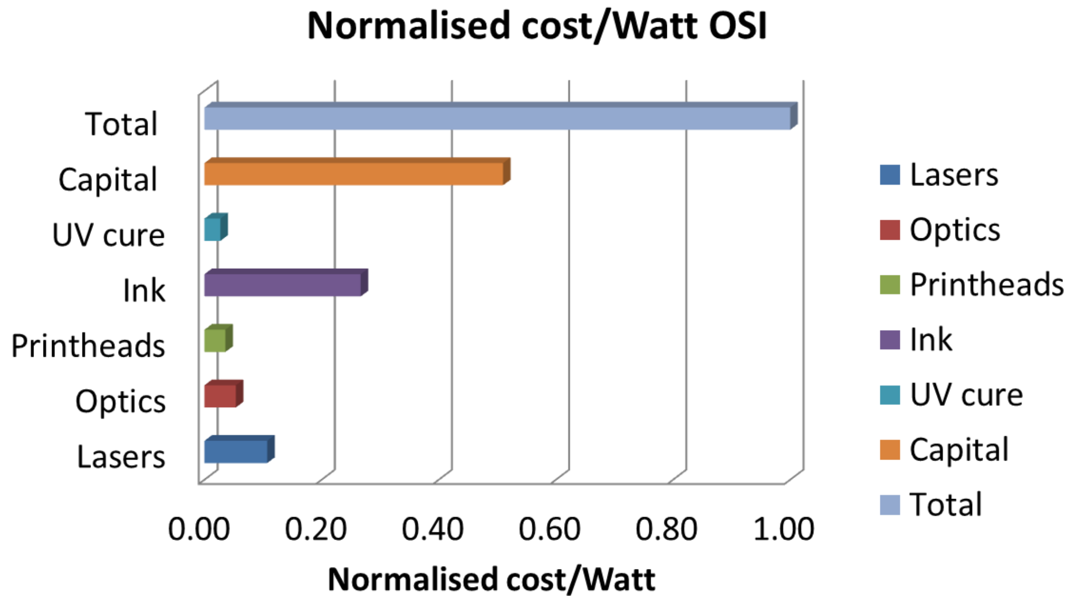


Figure 6.5: A breakdown of the cost of ownership of the OSI process incorporating more consumables in the form of inks and print hardware. Capital cost still dominates.

For both processes the cost of capital equipment dominates and by implementing OSI only one machine needs to be purchased compared to three for the conventional process. This means that as long as the cost of the OSI machine is not significantly more than a laser scriber the OSI process has a cheaper CoO. The sale price of an OSI tool has been calculated internally, again making some assumptions about the type of lasers required and the platform geometry but all based off the work done within this project. Comparing the cost of ownership of one OSI tool with the 3 laser scribers required for the conventional process shows that the total cost of OSI is ~30% less than the conventional process. A normalised comparison of the two processes can be seen in Figure 6.6.

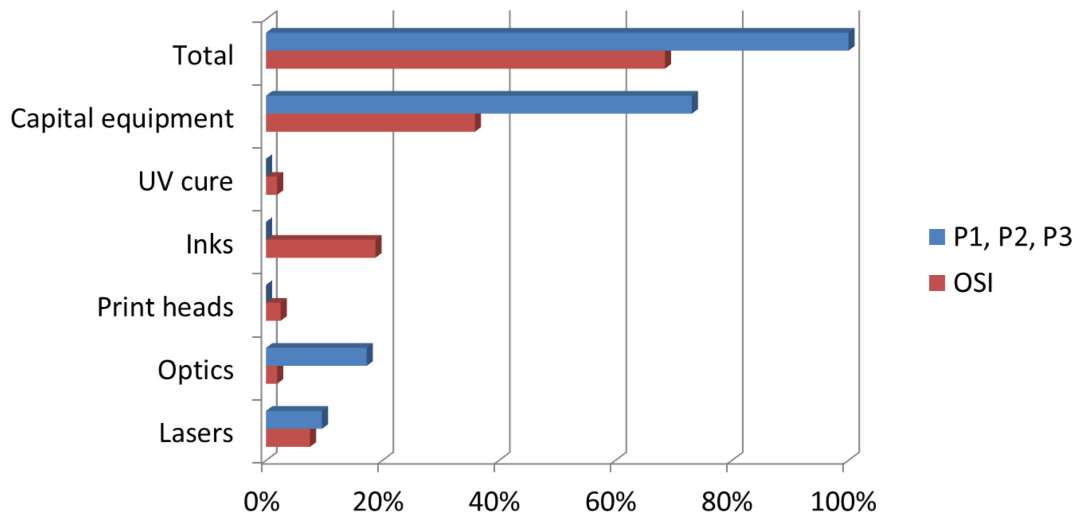


Figure 6.6: Comparison of the two processes normalised to the total cost of the conventional process. OSI works out ~30% less expensive than the conventional process.

6.1.3 Process advantages

Some process advantages such as the flatter panel thermal profile and narrower interconnect have been discussed above. Another process advantage is the ability to deposit all layers without breaking vacuum. This means that the interfaces between layers can be better controlled as they are not exposed to air, preventing incorporation of defects. This may lead to lower recombination rates as defects can be reduced which should result in higher panel efficiencies.

The final process advantage is the presence of a high resistivity material in the P1 scribe in OSI. A similar process is already used for the manufacture of CdTe modules where the P1 and P2 scribes are completed after the deposition of the CdTe junction and the P1 is then infilled with a photoresist and cured through the glass plugging the P1. This prevents sodium diffusion from the glass forming impurities which damage the electrical properties of the module [1]. OSI natively fills in the A scribe with a dielectric in a similar manner without the extra processing steps.

6.2 Conclusions and Further Work

In summary, OSI a proprietary interconnect process for TF-PV, has been introduced and taken to proof of concept. Robust laser processes have been developed for CdTe and

a-Si and shown to be electrically functional. A novel scribing process for CIGS has been developed. This scribing process is currently material dependant but works well in some instances, a basic FE model has been used to show that the ablation mechanism is likely to be 'brittle fracture' similar to a process developed with a pulse programmable 1 μm fibre laser [2]. The next steps in this work on CIGS scribing are to test a range of laser sources with longer wavelengths for the P2 process, and discussions are underway to access such lasers. In parallel the FE model could be extended to include the P3 process with the aim of identifying a wavelength regime suitable for 'brittle fracture' P3 scribes. The main barrier to extending the FE model is the availability of absorption spectra into the near IR. Measurements for this could be taken with FTIR as long as permission is sought from the material supplier.

In terms of material deposition it has been shown that insulative, UV cure polymer inks can be deposited and well controlled using inkjet technology and that they can electrically isolate the back contact from a deposited metal bridge. The polymeric inks suffer from poor thermal stability although functioning interconnects have been made. The next steps for insulator deposition could be testing of inorganic insulative nanoparticle inks made of alumina [3] or similar.

Conductor deposition has been demonstrated although the optimum 'R&D' ink has been discontinued due to material supply issues. There are difficulties in achieving optimum wetting of the conductive ink on the substrates, two methods have been investigated to modify the surface for the ink. The first deposition of a self-assembled monolayer showed limited success but again was substrate dependent, it is also not suitable for a production environment. The second, using an atmospheric plasma, has also shown limited success but not to the point where any conductive ink can be used with any substrate. The next steps in conductor deposition are the investigation of different deposition techniques such as syringe deposition [4] or aerosol jet [5] which allow the use of more viscous inks. The higher viscosity inks should make the deposited line width less dependent on surface chemistry.

Despite the challenges with conductor deposition OSI has been proven to work with electrical results comparable and in some ways better, than the base material, the maximum measured FF of an OSI cell is ~80%. Early indications are that the interconnects can hold up to the IEC standard lifetime testing criteria after surviving over 400 cycles of -40 to +85°C with little sign of performance degradation.

After a robust conductor deposition technique has been found the next step is proving that the process can be run at both production speeds and with a high yield. All the current processes are capable of running at production compatible speeds individually, >0.5m/s, therefore demonstrating the entire process at these speeds should be possible. The question of yield can only be answered after running large volumes of samples and undertaking statistical analysis on failure mechanisms. To this end a pilot production tool capable of running all processes simultaneously at production speeds is being designed and built at M-Solv and is expected to be online by the end of Q2 2015.

6.3 References

[1] B. M. Basol and B. McCandless, “Brief review of cadmium telluride-based photovoltaic technologies,” *J. Photonics Energy*, vol. 4, p. 040996, 2014.

[2] M. Rekow, R. Murison, C. Dunsky, C. Dinkel, J. Pern, L. Mansfield, T. Panarello, and S. Nikumb, “CIGS P1, P2, P3 Scribing Processes using a Pulse Programmable Industrial Fiber Laser,” 2010.

[3] K. Seerden, N. Reis, J. Evans, P. Grant, J. Halloran, and B. Derby, “Ink-jet printing of wax-based alumina suspensions,” vol. 20, pp. 2514–2520, 2001.

[4] M. Popischil, M. Kuchler, M. Klawitter, C. Rodriguez, A. Padilla, R. Efinger, H. Gentischer, M. Konig, M. Horteis, L. Wnede, O. Doll, F. Clement, and D. Biro, “Ultrafine front side metallization on silicon solar cells by industrial dispensing technology,” in *29th European Photovoltaic Solar Energy Conference and Exhibition*, 2014, no. September, pp. 1304–1306.

[5] B. H. King and M. J. Renn, “Aerosol Jet® Direct Write Printing for Mil-Aero Electronic Applications,” *WHITEPAPER - Optomec*, 2008.