Laboratory Demonstration of Closed Loop 30kW, 200V/900V IGBT-based LCL DC/DC Converter

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***Abstract*-- The inductor-capacitor-inductor (LCL) DC/DC converter has been extensively studied for high power and stepping ratio because of elimination of internal transformer, lower footprint/weight, higher efficiency, and most importantly providing DC fault isolation from both DC sides. This paper presents a two-channel, two-layer controller including two inner current loops, which is symmetrical for each bridge of LCL DC/DC. The real-time implementation of control scheme and its performance in normal conditions and during transient DC faults at both sides are studied on a 30kW 200V/900V 1.7 kHz prototype. The prototype development is presented in some depth. The experimental results show that the converter with closed loop control operates well at full power and under fast power reversal. Further DC fault testing concludes that there is no need for blocking since the internal voltage and current variables are within the rated values. Detailed study of converter losses is performed and results show that full power efficiency is around 93.4%.**

***Index Terms*—DC/DC converter, HVDC Transmission, Insulated-Gate Bipolar Transistor (IGBT), DC Fault isolation.**

I. Introduction

DC/DC converter is an important enabling component for developing offshore DC systems, including applications with wind turbine (3-6 MW) [1],[2], subsea compressor (6-80 MW) [3]-[4], and DC transmission grid (>100 MW) [5]-[8] technologies. Cigre uses two DC/DC converters in the DC transmission grid test system [7], and it is considered in several ongoing B4 working groups related to DC grids.

High efficiency, high stepping ratio, low weight/footprint, DC fault tolerance, and bidirectional power regulation are considered as most important specifications for a high power DC/DC converter [5],[6].

The dual or single active bridge DC/DC converters with internal AC transformers can achieve large stepping ratios (transforming both voltage and current) which results in good switch utilization [8]-[10]. It also provides galvanic isolation which facilitates flexible grounding in grid applications. However, designing a medium frequency, high-power transformer with a high stepping ratio, small footprint/weight, low transformer core losses, and avoiding core saturation are most challenging issues [11].

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On the other hand, transformerless DC-DC converter topologies have been studied for high power applications because of advantages in size/weight and possible higher frequency operation [12]-[18]. LCL dual active bridge, transformerless approach achieves high stepping ratios and good switch utilization (as if internal transformers are used) and also benefit of zero reactive current flow through either of the two bridges [15]. Since air-core inductors are used, passive components pose no limitation on operating frequency. For an offshore application, converter volume/weight has priority over switching losses [17]. An additional advantage over isolated topologies, is that LCL circuit can inherently limit the fault current [15][16], which is very important for high-power DC grid requirements. The studies in [17] indicate that 500 Hz, 1GW, LCL DC/DC with Modular Multilevel Converter (MMC) bridges is expected to achieve efficiency of 96-97%.

There has not been much reported kW/MW-size hardware prototyping of DC/DC targeted to transmission applications. In [4], a 10 kW multilevel buck/boost DC/DC converter has been built and tested as proof of concept for high power application. Excellent efficiency of 96.7% is reported, but the operating frequency of 20kHz may not be achievable in MW-size applications. A 9kW, 1kHz, 300V single-active bridge, isolated DC/DC demonstrates 96% efficiency in [10]. Since diodes are used, the switching losses at high-voltage side (prototype uses 1:1 ratio) are lower but at the expense of unidirectional operation and inability to actively operate for DC faults. Similarly, 1kW, 300V DC/DC prototype of resonant non-isolated MMC in [12], has simple structure, flexible stepping ratio and achieves good efficiency, but lacks bidirectional operation and tolerance to DC faults. A 30kW 200V/900V transformerless, thyristor-based DC/DC converter prototype, has been developed and tested in [14]. Despite all the advantages of this topology, both high and low voltage side switches should be rated for high voltage level (low switch utilization ratio) which restricts applications to moderate stepping ratio. In addition, reverse recovery losses impact efficiency and limit maximum operating frequency to 580 Hz.

The design, development, and open loop testing of a 30kW 200V/900V 1.7 kHz LCL DC/DC prototype has been reported in [16]. It confirmed inherent DC fault responses but closed loop control is not reported.

In [18] the initial results with closed loop controller for 30kW LCL IGBT DC/DC prototype were presented, although

full power operation was not possible. The DC faults are not studied and also efficiency analysis is not reported either.

This paper reports on continued development of controller from [18], and details the hardware implementation challenges and experimental testing of the 30kW 200V/900V 1.7kHz IGBT LCL DC/DC at the Aberdeen HVDC laboratory.

The goal is to develop and test real-time feedback controller which enables fast power reference tracking, minimises losses and achieves DC fault ride through from both sides. The details on the controller hardware implementation and converter component development will be reported.

The converter losses will be investigated in depth using the theoretical loss model and compared with hardware measured efficiency. Finally, design and performance of the LCL IGBT DC/DC converter will be compared against a similarly sized thyristor-based LCL DC/DC converter which has been previously developed and tested in our laboratory [14].

II. LCL DC/DC Converter

A. LCL IGBT DC/DC Converter Topology and Design

The 2-phase topology of the LCL DC/DC converter is shown in Fig. 1 and the design is discussed in depth in [15]. It consists of two single-phase VSCs bridges with an internal LCL circuit. Tuned LCL provides voltage stepping ensuring good utilization of bridge semiconductors as if transformer is used, and also fault current limiting. With a proper control angle, LCL also ensure current is in phase with voltage at each bridge. The two active bridges can be designed based on 2 level pulse width modulation (PWM) or MMC.

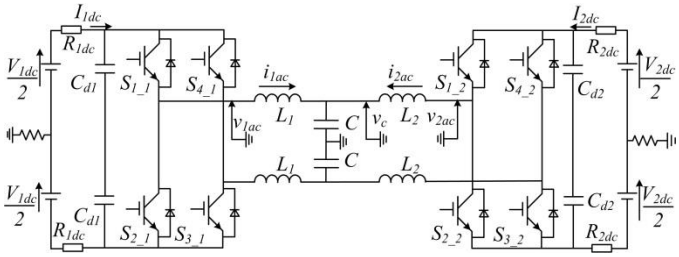


Fig. 1. IGBT based LCL DC/DC converter.

B. Basic Circuit Equations

The converter model is studied in the rotating *dq* coordinate frame linked with the central capacitor voltage V_c as shown in Fig. 1. In time domain, the two bridge AC voltages are:

$$v_{iac} = \sqrt{2}V_{iac}\cos(2\pi f_o t + \alpha_i) \quad i = 1,2 \tag{1}$$

where V_{iac}, f_o, and α_i are the AC voltage main harmonic RMS, the operating frequency, and the phase angle of v_{iac}.

The AC voltages are expressed in the phasor domain as:

$$\overline{V_{iac}} = V_{iac}\angle\alpha_i = V_{iac}\cos\alpha_i + jV_{iac}\sin\alpha_i, \quad i = 1,2 \tag{2}$$

$$V_{id} = V_{iacm}M_i\cos\alpha_i = V_{iacm}M_{id} \quad i = 1,2 \tag{3}$$

$$V_{iq} = V_{iacm}M_i\sin\alpha_i = V_{iacm}M_{iq} \quad i = 1,2 \tag{4}$$

where M_i is amplitude modulation index, M_{id} and M_{iq} are *d-q* components of control signal and $V_{iacm}=0.5V_{idc}$ is the maximum value of V_{iac}. The AC current phasor is obtained as:

$$I_{id} + jI_{iq} = \frac{V_{iq} - V_{cq}}{\omega L_i} + j\frac{V_{cd} - V_{id}}{\omega L_i} \quad i = 1,2 \tag{5}$$

Given that the *dq* frame is aligned with the central capacitor voltage $V_c=V_{cd}$, (3), - (5) result in:

$$I_{id} = \frac{M_{iq}V_{iacm}}{\omega L_i} \quad I_{iq} = \frac{V_c - M_{id}V_{iacm}}{\omega L_i} \quad i = 1,2 \tag{6}$$

Equation (6) shows that I_{id} and I_{iq} can be independently controlled by M_{iq} and M_{id} respectively, which is exploited for developing inner current control loops.

III. Converter Controller Design

The controller design aims are:

1. Symmetrical structure (identical control at each port),
2. Power regulation and optimal current (current in phase with voltage) at each bridge at all loadings.
3. Permanently running inner current control loops.

A. Active Power Management

The complex power of the two bridges is obtained as:

$$\begin{aligned} S_i = P_i + jQ_i = (V_{id} + jV_{iq})(I_{id} - jI_{iq}) = \\ V_{id}I_{id} + V_{iq}I_{iq} + j(V_{iq}I_{id} - V_{id}I_{iq}) \quad i=1,2 \end{aligned} \tag{7}$$

By considering (3)(4) and (6) and replacing into (7):

$$P_i = \frac{1}{\omega L_i}(V_{iq}V_c) = V_c I_{id} \qquad i = 1,2 \tag{8}$$

Equation (8) shows that active power at each bridge can be controlled by *d* component of the corresponding *AC* current. This result along with previous conclusion from (6) reveals that bridge power is controlled using M_{iq} signal.

B. Power Balance Indicator

Considering Fig. 1 the central capacitor current is:

$$j\omega C\overline{V_c} = I_{1d} + jI_{1q} + I_{2d} + jI_{2q} \tag{9}$$

Substituting (6),(8) into (9), and rearranging gives:

$$\begin{aligned} K_c V_{Cd} V_{Cq} = P_1 + P_2 \\ K_c = \left(\frac{1}{\omega L_1} + \frac{1}{\omega L_2} - \omega C\right) \end{aligned} \tag{10}$$

The sum active power, P_1+P_2, must be equal to zero and therefore V_{Cq} will be indicator of power balance and should be kept at zero. Note that keeping V_{Cq} to zero is precondition for

all the equations in the previous section and it is requirement for independent active power flow control using M_{iq}.

The reactive power balance equation is obtained using (9):

$$\omega V_c C = \frac{V_c - M_{1d} V_{1acm}}{\omega L_1} + \frac{V_c - M_{2d} V_{2acm}}{\omega L_2} \tag{11}$$

C. Reactive Current Control

It is postulated that losses strongly depend on current magnitudes, using experience from [14]. To minimize losses, the reactive currents in the coordinate frames linked with the AC voltages of each bridge will be regulated to zero. Fig. 2 shows the relationship between the coordinate frame aligned with AC voltages (*DQ* frame) and the one aligned with central capacitor voltage V_C (*dq* frame). The current relationship is:

$$I_{iD} = I_{id}\cos(\alpha_i) + I_{iq}\sin(\alpha_i) \tag{12}$$

$$I_{iQ} = -I_{id}\sin(\alpha_i) + I_{iq}\cos(\alpha_i) \tag{13}$$

These equations are employed in the original controller in [18], and difficulties were experienced with real time implementation on FPGA hardware because of use of 3 different coordinate frames. Considering (13),(3) and (4), and to achieve I_{iQ} =0:

$$I_{iq} = I_{id}\tan(\alpha_i) = I_{id}\left(\frac{M_{iq}}{M_{id}}\right) \tag{14}$$

Equation (14) uses only variables in the central coordinate frame which is of benefit in reducing real-time computations.

D. Steady-state, closed-loop solution

If the converter parameters (C, L_1, L_2, V_{1acm}, V_{2acm}) and desired power (P_1=P_2) are given, it is possible to calculate 5 variables (M_{1d}, M_{1q}, V_c, M_{2d} and M_{2q}) that define operating point with the above controls. The 5 equations are as follows:

- Two power equations for each port from (8),
- Reactive power balance on V_c in (11),
- Two equations for zero reactive current at each bridge, obtained replacing currents from (6) in (14).

E. Controller Structure

The proposed controller block diagram is shown in Fig. 3. The reference angle, θ, (used for the firing logic and all single-phase *dq* transformations at both bridges) is obtained from a voltage-controlled oscillator (VCO), $\theta = 2\pi f_o t$. The coordinate frame speed is same as operating frequency (f_o=*1.7kHz* in the prototype). No Phase Locked Loop is required since coordinate frame is aligned with V_c as long as V_{cq}=*0*.

The external loops consist of active power regulation to a reference P_{ref} and V_{cq} regulation to zero. Because of bidirectional operation, the average of the powers measured at two bridges is regulated. The output of each external loop is applied at both bridges to ensure equal control sharing, which is important for bidirectional operation and during faults.

The inner current loops are essential if this technology is to be scaled to higher powers. They ensure that semiconductor current is limited under all conditions including DC faults and during saturation of external loops.

The design equation (10) shows that V_{cd} must be positive, and thus M_{1d} and M_{2d} would be positive in any operating condition too. Therefore, a lower limit of 0.01 is imposed on M_{id} controller to avoid any singularity in q-axis reference current calculation in (14). It is worth mentioning that M_{1q} and M_{2q} correspond to active power flow balancing and it is crucial to avoid their saturation. Otherwise, severe overvoltage or voltage collapse may occur on central capacitor which would be detrimental to DC/DC converter operation. In this way, the priority is given to active power loops while reactive current controllers are functioning only if the modulation index is below 1, as shown in Fig. 3. Note that such override might happen only during faults.

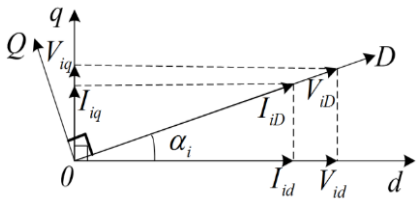


Fig. 2. Relationship between local and central coordinate frames.

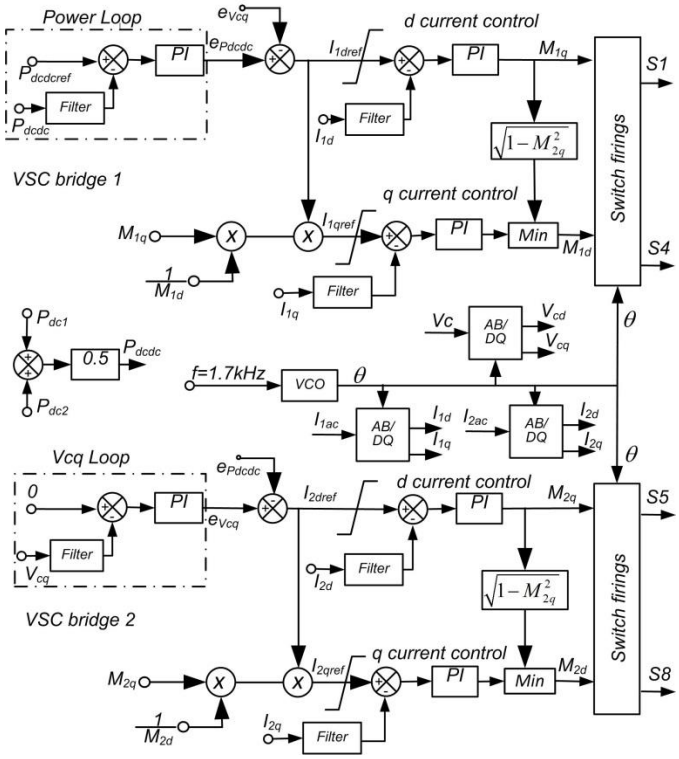


Fig. 3. The proposed controller for LCL DC/DC converter controller.

F. Controller dynamics

The controller topology ensures some decoupling but reactive current control loops are non-linear and coupled with active power control as seen in (14). The controller gains are tuned in PSCAD in the other of their speed of response:

1. Inner d current and power balancing simultaneously, since converter can not operate unless power is balanced. M_d is kept constant initially.

2. Reactive current control loops.
3. Final tuning of filters and all gains. The feedback filters are of second order (ζ=*0.8*, and f_c=*300Hz*). The performance of power balancing has priority.

IV. LCL DC/DC Converter Prototype and Laboratory Test Platform

A. 30 kW 200V/900V DC/DC Converter Development

Fig. 4 (a) shows a photograph of the developed DC/DC converter and the main technical aspects are summarized:

- AC operating frequency of 1.7 kHz is selected, which is a compromise between the weight/size and losses [16].
- Litz wire is used for LCL inductors to mitigate skin effect at the selected operating frequency.
- To decrease the total inductor size, weight, and loss the two pole inductors are closely wound back-to-back with a small gap in between as seen in Fig. 4(a).
- The selected WIMA film capacitors have 1.2kV DC voltage rating which rapidly reduces with frequency down to 250V at 1.7 kHz. The required 48µF per pole is obtained using two 96µF banks in series. Each bank is a parallel array of 2×30 µF, 1×20µF, 3×5µF, and 1×1µF capacitors.
- The low frequency modulation ratio, m_f=3 is used for both bridges as AC power quality is of less interest compared to the efficiency. A new method of PWM pattern generation is employed, which reduces losses by forcing switchings at low or zero current as described in [16].
- VCO, PWM pattern generation, Analog-to-Digital Converter (ADC) signal conversion, single-phase *dq* transformations, control loops of both bridges, and DC/DC converter protection logic are implemented on a SBRIO-9606 National Instrument single FPGA board.
- Single-phase *dq* transformation is facilitated by using an artificial quadrature axis, which is synthesized by delaying the measured signal by 1/4 of the period.
- The protection interlock is activated by: over voltage, and over current at AC and DC side, as well as driver level short circuit, and capacitor voltages asymmetry detection.
- The FPGA board is configured to run the VCO function at 1 MHz using its high frequency internal clock, while the remaining functions are run at 100 kHz frequency.

B. Laboratory test platform

A simplified schematic of the developed platform for testing is shown in Fig. 4 (b) and more details of the initial version are given in [14]. A 30kW, two-level, 10kHz, PWM controlled VSC provides 200V DC, while another 30 kW, 1.5kHz VSC provides 900V DC. The two VSCs control their DC voltages while DC/DC converter regulates power flow between the two VSCs. Subscript labels “200” and “900” are used with all prototype variables corresponding to “1” and “2” in the previous section.

The extreme faults at DC terminals are emulated with special fault hardware consisting of high-current IGBTs and fault impedances (R_{f900} = 1 Ω, and R_{f200} = 50 mΩ). The corresponding VSC is replaced with a resistive load which gives 30kW (26Ω for 900V side and 1.5Ω for 200V side).

Due to pole asymmetries in AC inductors, AC capacitors, and switching pulses, some circulating currents flow through the ground connections in the DC platform. This impacts the converter efficiency but can be minimized by increasing the ground loops impedance. Therefore, the midpoints of the two VSCs are grounded through 10 Ω resistors whereas the central capacitor of DC/DC is solidly grounded, as seen in Fig. 4 (b).

V. Experimental Results

A. Adjusting the LCL parameters

The initial converter design using theoretical study of [15] failed to achieve full power operation. Some control variables were in saturation, and power reversal would lead to saturation of different variables. This was a consequence of high current magnitudes, which in turn resulted from controller inability to minimize reactive current. Ultimately this is attributed to the internal losses which are around 7%, and were not considered in theoretical modeling.

Theoretical design with additional resistances was very challenging because of different impacts in each power direction and because of lack of accurate values for resistances (some vary with operating point and temperature change).

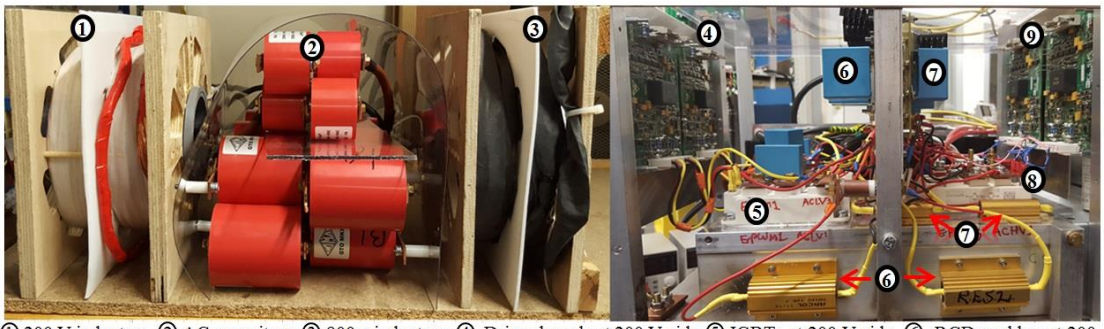
The final LCL parameters are adjusted using PSCAD simulation and hardware testing. In practice, only inductor values can be adjusted to tune the LCL circuit. Fig. 5 shows the controller variables and currents in steady-state depending on values of LCL inductors. For example, if the tests show that M_{200} is in saturation, then we should reduce L_{200} or increase L_{900} according to Fig. 5 c) and d). The adjustment will be made on either L_{200} or L_{900} depending on the current magnitude on the two sides, considering Fig. 8 a) and b). It is also seen that the circuit is quite sensitive to L_{200} variation, since 3% L_{200} change leads to *20%* current change and 40% M_{200} change. Further testing shows that if only one power direction is desired, then circuit can be adjusted for over *35kW* average power.

The capacitance of LCL capacitor is directly linked with the maximal power transfer, and we used around 10% larger than the theoretical value to account for the internal loss. The operating frequency can also be adjusted to tune the LCL circuit but it has not been varied in this study. The final parameters are shows in Table I, where the values in brackets represent the original theoretical values for comparison.

B. DC/DC response to power reference step changes

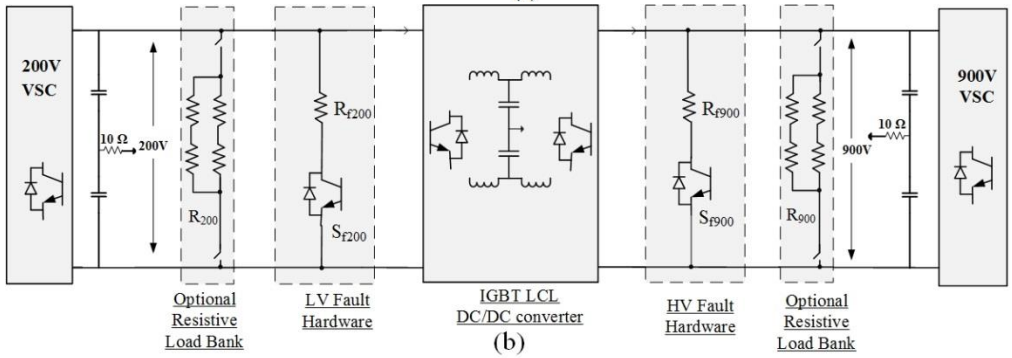
Fig. 6 shows the closed loop converter response in step-up and step-down modes, with two fast power reversals applied at t=1.0 s and 2.0 s. Before t=1.0 s, the DC /DC converter exports 27.5 kW from 200V to 900V side (step-up mode). At t=1.0 s active power reference is changed from 27.5 kW to -26.5 kW within 200 ms to demonstrate fast power reversal capability. Between t=1.0 s and t=2.0 s the DC /DC transfers 26.5 kW from 900V to 200V VSC operating in step-down mode. At t=2.0 s, the active power reference is again changed from -26.5 kW to 27.5 kW within 200 ms.

Fig. 6 (a) and (b) show the outer loops performance. V_{cq} is



① 200 V inductors, ② AC capacitors, ③ 900 v inductors, ④ Driver boards at 200 V side, ⑤ IGBTs at 200 V side, ⑥ RCD snubber at 200 V side, ⑦ RCD snubber at 900 V side, ⑧ IGBTs at 900 V side, ⑨ Driver boards at 900 side.

(a)



(b)

Fig. 4. Laboratory built DC system a) Developed DC/DC converter, b) Test rig schematic.

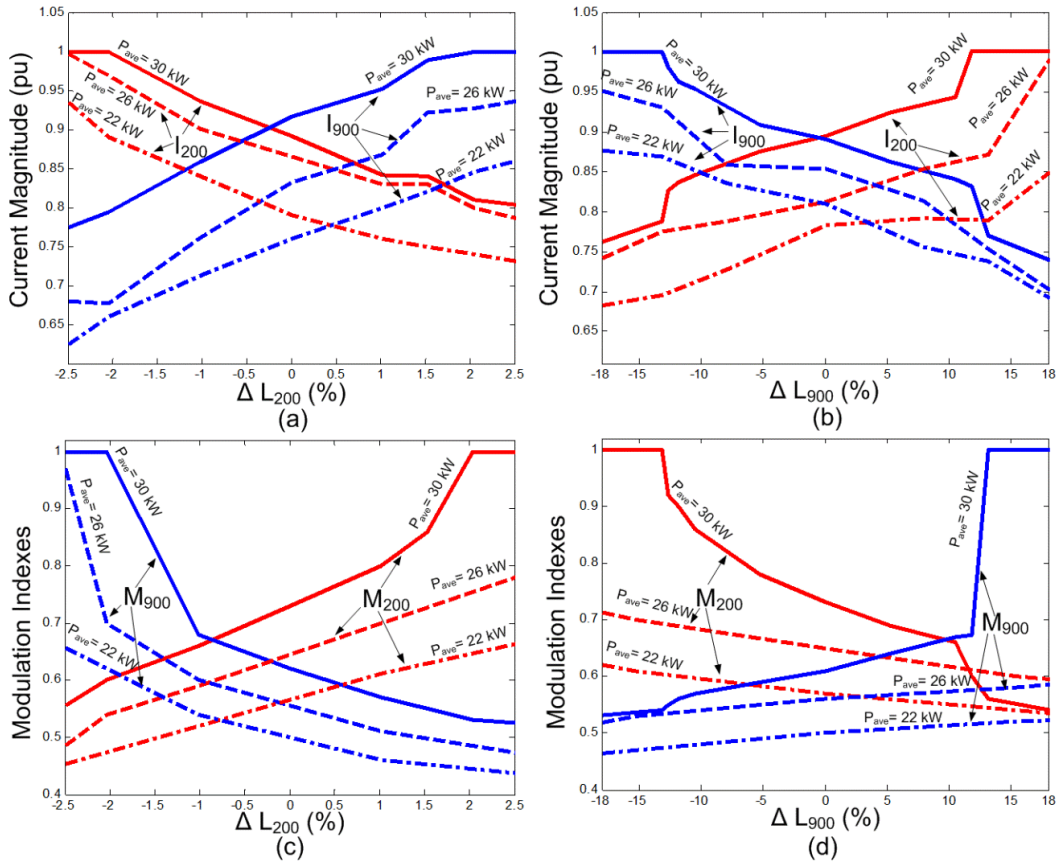


Fig. 5. System variables versus LCL inductor variations a) current magnitudes for 200V side inductor variation, b) current magnitudes for 900V side inductor variation, c) modulation indexes for 200V inductor variation, d) modulation indexes for 900 V side inductor variation.

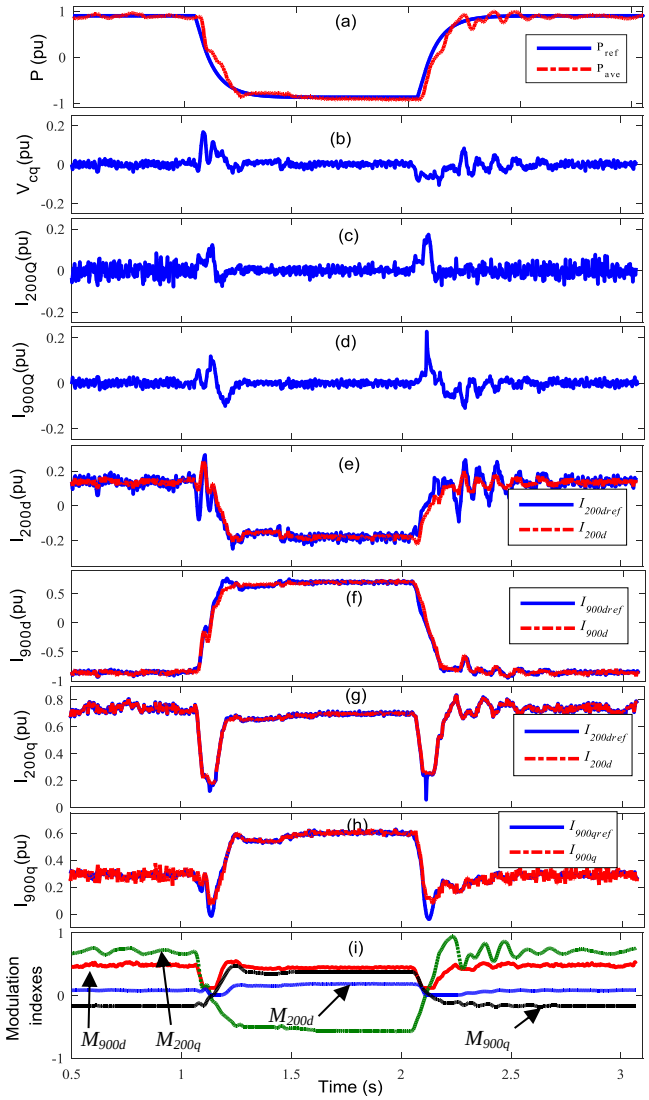


Fig. 6. Experimental results P_{Base}=30 kW, $I_{200\text{-}Base}$= 282 A, $I_{900\text{-}Base}$=63 A.

firmly regulated to zero which facilitates decoupled active power control. Fig. 6. (c) and (d) show AC current Q- axis components in the DQ frames linked with the voltages of each VSC bridge, demonstrating reactive current regulation to zero at each bridge. It is seen that the converter shows satisfactory tracking of active power reference while keeping reactive current at zero. Figures 5 (e) to (h) depict tracking of the four inner current control loops. Note that these currents are shown in the coordinate frame linked with the central capacitor and consequently *q* components are not zero. Fig. 6 (i) shows modulation indices of both bridges and demonstrates that none is saturated during transient or steady state conditions.

The obtained transient response is not of highest quality and deviates from performance observed in simulation (not reported due to lack of space). This has been investigated and it is concluded that the quality of 200V and 900V DC bus voltages control by the external VSCs is an issue. There is a ±10% DC voltage swing for the tests in Fig. 6, and it was not possible to further improve DC voltage control on the sources.

The steady-state AC voltages and currents at both bridges, obtained for two different power levels in each direction, are shown in Fig. 7. As it can be seen, the voltage and current fundamental components are in phase at both bridges. It is also observed that at higher powers, the AC voltage tends to pure square wave profile which results in lower switching losses.

C. DC Fault Responses

The controller responses are monitored for DC faults at each side and Table I presents the steady-state values of the most important variables during fault conditions. The following conclusions are made:

- At faulted side the modulation index does not affect the LCL variables as its DC link voltage is practically zero.
- M_d of the non-faulted bridge saturates at 0. This indicates that reactive current regulation cannot be maintained during DC faults. This is of no concern due to short interval of such event.
- The outer power loop cannot track the reference power and therefore the inner *d*-current reference saturates. This implies that V_{cq} control loop is also ineffective during the fault since it operates on the active power signal. Thus, some non-zero V_{cq} results, and the control signal on non-faulted side will reach saturation.
- The DC/DC converter becomes an open loop system and responds similarly as reported in [15] and [16]. Current on non-faulted side naturally reduces whereas the current at faulted side marginally increases.
- In the worst case (step-down mode and fault at 200V side) central capacitor voltage increases by 20 % which is well below AC capacitor voltage rating.

Fig. 8 (a) shows the DC and AC voltages when a DC fault is applied at 900V DC bus for 1.0 s while in step-up mode. The results demonstrate that the fault is not transferred to 200V side. Fig. 8 (b) shows the AC currents and voltages. It is also seen that the AC current at the 200V side decrease while at the 900V side it marginally increases. The central capacitors show no overvoltage during such extreme disturbance.

Fig. 8 (c) shows the converter AC and DC voltages when a DC fault is applied at 200V side for 1.0 s while operating in step-down mode. Similar to the previous results, the fault is not transferred to 900V side. Fig. 8 (d) shows that 200V side current and central capacitor voltage marginally increase, while the non-faulted side current decreases.

As we can see in both tests, the faulted DC link voltages are restored after fault clearance which demonstrates the capability of the proposed controller in providing fast recovery at post-fault condition.

D. Efficiency Analysis

The converter efficiency is analysed using a loss model developed as follows:

Conduction losses of power switches are calculated by inserting a voltage V_U (representing the voltage drop), and a resistor R_{ON} (representing the current dependency), in series with the IGBTs in the converter model in PSCAD. V_U and R_{ON} can be extracted from the IGBT's datasheet

Switching losses are calculated employing the switching currents, dc link voltage and switching frequency in the detailed converter model in PSCAD, and using turn-on and

turn-off energy curves from IGBT's datasheets.

The equivalent resistance of the LCL inductors is obtained considering selected Litz wires details, number of layers, number of turns and geometry of the air cores.

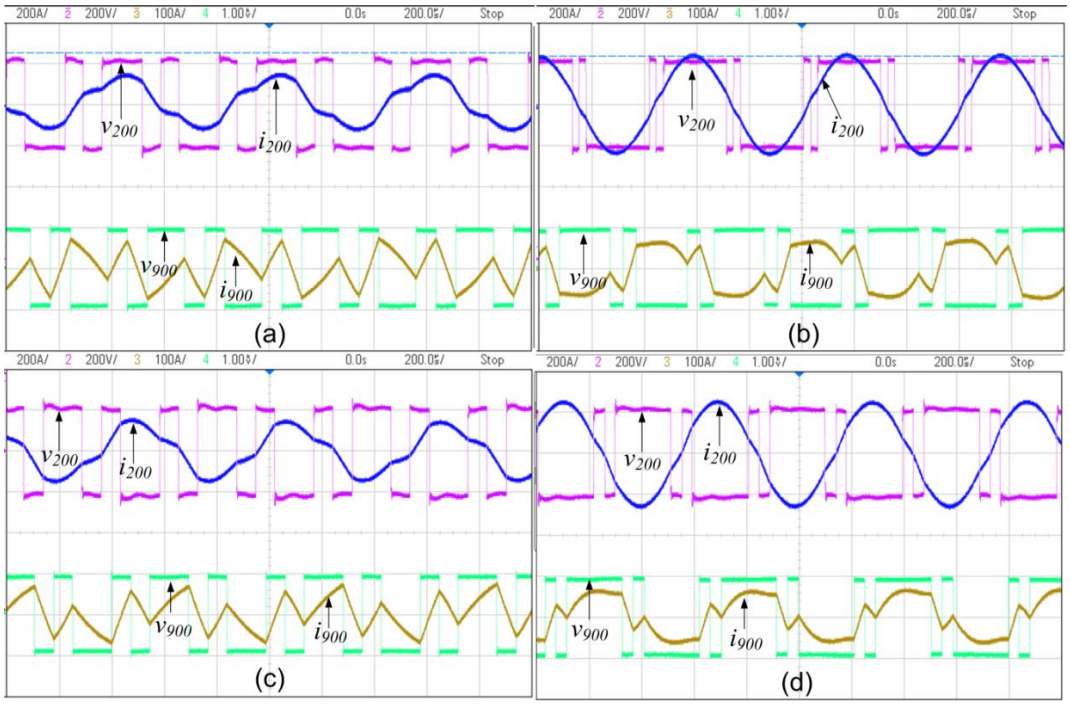


Fig. 7. 200 V and 900 V AC voltages and currents in step-up and step-down modes a) P_{ave}=7.6 kW, b) P_{ave} =27.5 kW, c) P_{ave}=-7.6 kW, d) P_{ave} =-26.5kW.

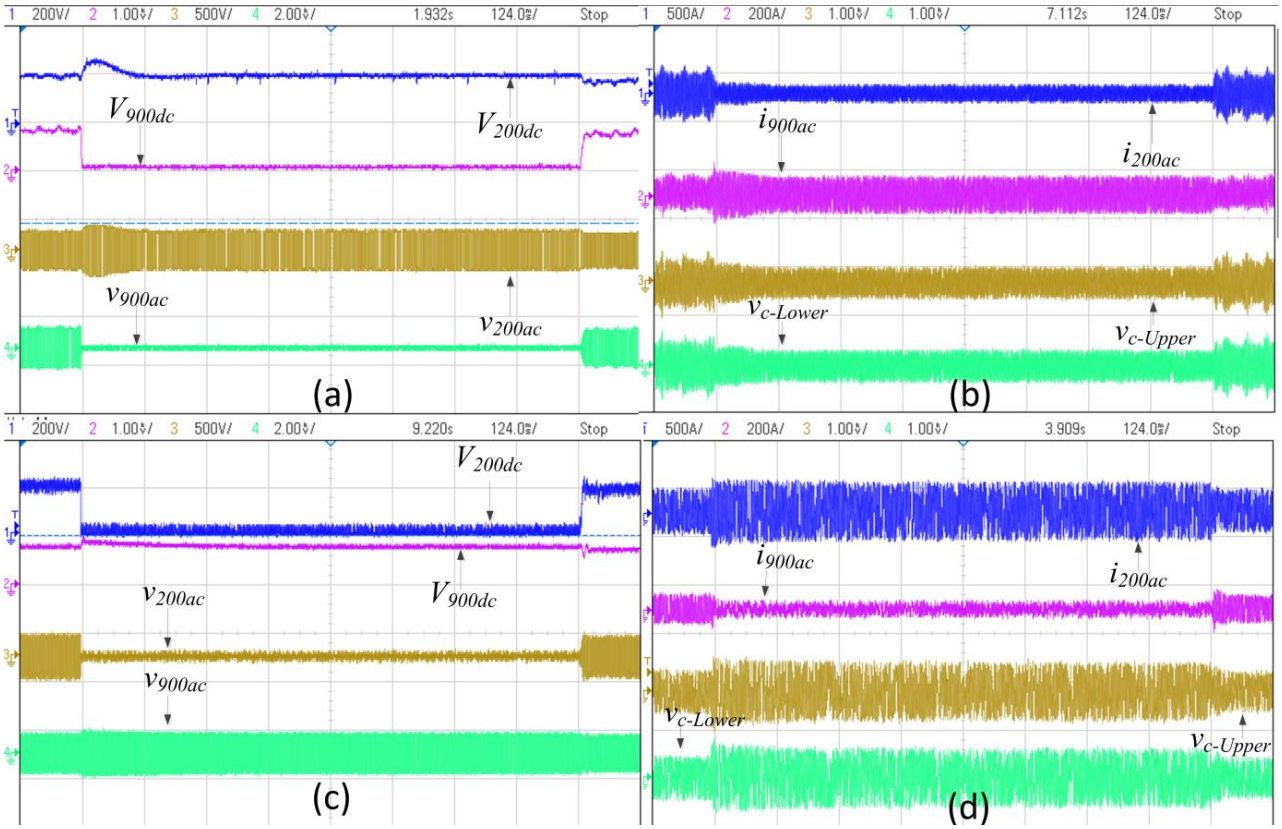


Fig. 8. DC fault experimental results: (a) and (b) 900V side fault when the converter works in step up mode, (c) and (d) 200V side fault in step down mode.

Table I: Converter variable during DC faults

Mode	Fault at 200V side					Fault at 900V side				
	M_{900d}	M_{900q}	$I_{200ac}(pu)$	$I_{900ac}(pu)$	$V_c(pu)$	M_{200d}	M_{900q}	$I_{200ac}(pu)$	$I_{900ac}(pu)$	$V_c(pu)$
Step-up	*0*	*-1*	*1.22*	*0.43*	*1.2*	*0*	*1*	*0.32*	*1.13*	*0.55*
Step-down	*0*	*1*	*1.16*	*0.43*	*1.15*	*0*	*-1*	*0.3*	*1.14*	*0.53*

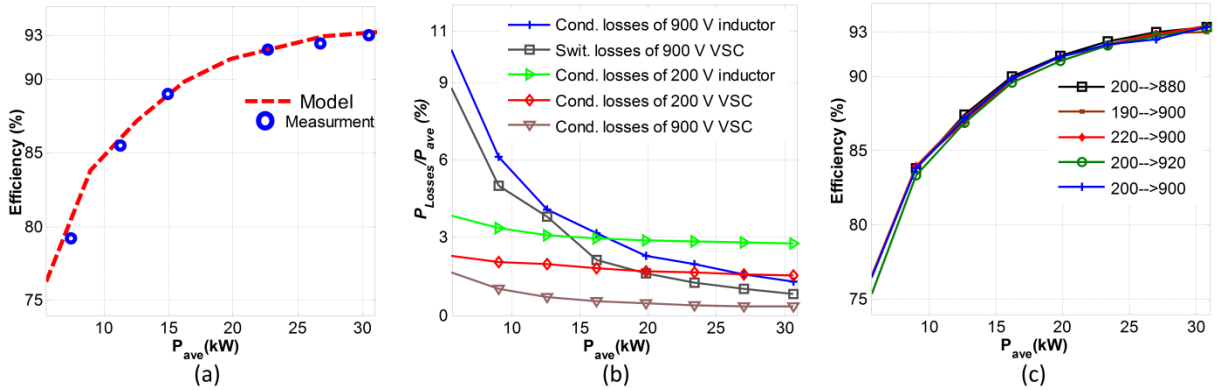


Fig. 9. The DC/DC converter efficiency: a) Efficiency versus power. b) Loss distribution versus power, c) Efficiency with different stepping ratios.

Table II: Comparison between IGBT LCL DC/DC converter and thyristor LCL DC/DC converter

Specification	30 kW IGBT LCL DC/DC Converter	30 kW thyristor LCL DC/DC Converter [14]
200 V Inductor (2 required)	*194 µH,180A, 0.02Ω, 7kg, 0.00736m^3 (205 µH)*	*500µH,175 A,0.03Ω,13 kg, 0.01227m^3*
900 V Inductor (2 required)	*380µH,40 A, 0.052Ω,3.7kg, 0.002m^3 (360 µH)*	*224µH,37 A,0.0375Ω,2 kg, 0.001m^3*
AC capacitor (2 required)	*48 µF,540 V, 12.5 kg, 0.00398 m^3 (45 µF)*	*140 µF,707 V,12 kg, 0.0037 m^3*
Power Switches	*4×IGBT (600 V,300 A) +4×IGBT (1700 V, 120A)*	*8×Thyristor ((1.8 kV, 270 A) + 8×Thyristor ((1.8 kV, 50 A)*
Operating Frequency	*1700 Hz*	*0-580 Hz*
Power Density	*2.25 kW/L*	*1.76 kW/L*
Specific Power	*1.29 kW/kg*	*1.11 kW/Kg_*
Inductor losses at 200V side	*840 W (estimated)*	*1368 W (estimated)*
Inductor losses at 900V side	*415 W (estimated)*	*120 W (estimated)*
Switching losses at 200 V side	*Negligible (estimated)*	*216 W (estimated)*
Switching losses at 900 V side	*190 W (estimated)*	*72 W (estimated)*
Conduction losses at 200 V side	*430 W (estimated)*	*456 W (estimated)*
Conduction losses at 900 V side	*105 W (estimated)*	*72 W (estimated)*
Measured efficiency (%)	*93.4% (estimated total loss is 1980 W)*	*92% (estimated total loss is 2304 W)*

The RCD snubber losses are ignored since they are small.

The efficiency of the developed prototype is also measured for few power levels and close agreement is observed with the estimated efficiency as is shown in Fig. 9. The converter efficiency at full power is around 93.4% which is a promising value for nominal power of 30kW.

The loss components versus loading are shown in Fig. 9 (b). It is seen that the 200V side switching loss is small because of switching around zero current. The Total Harmonic Distortion (THD) of current is high due to low frequency modulation index of 3, which is particularly pronounced at 900V side and at lower power as seen in Fig. 7. The harmonic circulation increase losses. The design options allow some change in parameters, and studies indicate that larger 900V side inductor may improve efficiency, despite increased inductor resistance.

The dominant loss component at high power is conduction loss of 200V side inductor. This loss can be readily reduced by increasing cross section of L_{200} Litz wire. If we use 270 strands of 0.45mm Litz wire instead of currently used 135 strands of 0.63mm, the efficiency will reach over 94.5% with 22% increase in inductor weight.

We have also studied the converter efficiency when the converter is exposed to different DC voltage levels, considering that LCL is tuned for a particular stepping ratio. Fig. 9 (c) shows that design is robust against modest changes in stepping ratio and almost same efficiency is obtained.

E. Comparison with 30kW LCL thyristor DC/DC design

Table II compares the power switch characteristics, power density, specific power, operating frequency, loss components, and efficiency between 30kW IGBT LCL and 30 kW thyristor LCL DC/DC converter [14]. As it can be seen, IGBT design requires lower inductors and capacitors. The capacitance of AC capacitor is reduced but the weight and volume of this capacitor bank is increased slightly. This has been unexpected practical result, which is caused by capacitor voltage rating deterioration with frequency which demands more series-connected units. However, power density and specific power for IGBT-based DC/DC converter have been improved by 27% and 16% respectively. The LCL IGBT topology needs lower number of power switches (8 IGBT against 16 Thyristors), lower rating of the power switches and can achieve faster and more reliable power reversal. The switching losses of thyristor converter are lower at 900V side because of discontinuous operation but this loss component is small. Overall, the IGBT LCL design shows better efficiency, faster control response, with lower volume and weight, and is a favored candidate for offshore DC applications.

VI. Conclusion

This paper firstly presents analytical background of a

feedback controller for LCL IGBT DC/DC and it is concluded that the alignment of coordinate frame with the central capacitor voltage enables decoupled control of active and reactive current. The proposed controller architecture is suitable for implementation on FPGA with high sampling frequency of 100kHz. The inner current regulators are provided with the view of scaling converter to higher powers.

The main challenges of practical implementation of 30 kW, 200V/900V, 1.7 kHz, IGBT LCL DC/DC converter are analyzed. Because of the internal LCL circuit losses, it is essential to finalize the LCL parameters on the prototype and a systematic method of parameter tuning is demonstrated.

Experimental testing concludes satisfactory steady-state operation and fast power reversals. Experimental DC fault tests at full power demonstrate that internal voltages and currents are kept within the safe range and the controller achieves fast recovery after fault removal.

The efficiency studies show that while 900V side switching and conduction losses are dominant at low power, while the 200V side inductors are the main source of losses at high power range. An efficiency of 93.4% is obtained at full power but it drops at partial loading. The possible drawbacks with high-power, high frequency AC capacitor size are highlighted.

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IX. BIOGRAPHIES

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