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Silicon nitride nanotemplate fabrication using inductively coupled plasma etching process

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In this work, we have investigated the fabrication of ordered silicon nitride nanohole arrays as part of an overall process aimed at producing organized silicon nanocrystals. The authors have demonstrated that it is possible to use inductively coupled plasma etching systems in order to etch nanometric layers, despite the fact that these systems are designed for deep and fast etching. A stable process is developed for shallow etching of silicon nitride nanoholes. The influence of different plasma etching parameters on silicon nitride nanohole properties is analyzed. 30 nm deep nanoholes of approximately 30 nm diameter, near vertical sidewalls and a good control of the selectivity are achieved. The overall process provides a simple and reproducible approach based on shallow inductively coupled plasma etching to obtain high quality nanosized silicon nitride templates. A suitable process for organized arrays of 10 nm diameter silicon nanocrystals realized by electrochemical etching is shown. © *2011 American Vacuum Society*.
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I. INTRODUCTION

The organization of silicon nanocrystals has been a topic of interest in recent years due to their potential application for future large scale integration of nanoelectronic devices such as single electron transistors (SET)[1] and nonvolatile memories (NVM).[2] The fabrication of nanocrystals with excellent control over size, location and spacing remains a key requirement to obtain reproducible properties for these nanoelectronic devices.[3,4] Many research efforts have been focused on nanocrystal organization using nanopatterned surfaces as templates. Among the approaches studied, the organization of nanocrystals on artificial prestructured surfaces is a promising option.[5–7] This consists of creating a periodic pattern with high-resolution lithography combined with etching techniques. These prepared surfaces present a periodic regular array which serves as a mask for nanocrystal organization. This type of approach has the advantage of being very precise for nanocrystal localization and can achieve a good resolution providing good control of size, location, density, and spacing between nanocrystals. In our work, this approach was elaborated to fabricate silicon nitride nanohole arrays used as masks for the organization of silicon nanocrystals fabricated by electrochemical etching.

Recently, electrochemical etching became a new alternative compared to other common techniques for silicon nanocrystal fabrication.[8–10] This technique consists of anodizing the surface of monocrystalline silicon wafers by using short single pulses of current in a low concentration of hydrofluoric acid electrolytes and using a current density in a specific anodization regime situated between pore formation and electropolishing.[11,12] This electrochemical etching has the advantage of being a fast and relatively low-cost technique. Depending on the type of substrates, their doping level and the anodization parameters (time, HF concentration, and current density), high quality silicon nanocystals can be obtained with controlled and reproducible morphologies.

However, to organize these silicon nanocrystals on nanopatterned silicon nitride layers (Si_3N_4), the Si_3N_4 nanoholes properties and the silicon (Si) surface quality after template fabrication are crucial for the accomplishment of this fabrication process.

The main possible approaches to fabricate nanometer scale templates are based on direct etching by using focused-ion-beam (FIB) or electron beam lithography (EBL) combined with dry etching process. FIB etching is done directly on the sample leading to template fabrication in a single step. Nevertheless, this technique is far too slow and thus too expensive for template fabrication. In addition, good etch selectivity of Si_3N_4 over silicon is difficult to achieve by using FIB and there is a high likelihood of ion implantation in the substrate.[13] EBL combined with dry etching process is faster and seems to be more appropriate to obtain good reproducibility and nanohole quality. The reactive ion etching achieves anisotropic etching, but can also induce damage on the silicon surface due to the high levels of ionic bombardment that are

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inherent to this technique. Since the electrochemical etching that governs the nanocrystal formation is highly sensitive to the surface quality, ICP systems are potentially more adapted to this process. The advantage of the ICP etching relative to standard RIE is that the RF platen power controls the energy of the ions bombarding the wafer surface independently from the flux of ions in the plasma. It is well known that ICP systems produce a high density plasma enabling the achievement of high aspect ratio structures with high etch rates, vertical sidewall angle and a good control of selectivity over the resist mask. However, the design of the ICP systems (chamber geometries, RF source power, gas fluxes, chamber pressure,…) is more adapted to deep etching than thin film etching.[14,15] For this reason, there are only a few studies in the literature on ICP etching of nanometer scale ultrathin films.

In this work we demonstrate a controllable and reproducible ICP etching of shallow Si_3N_4 nanohole templates, leading to near vertical sidewalls with a good control of the etching rate and the surface quality. A suitable ICP process for fabricating organized silicon nanocrystals by electrochemical etching is developed. In previous work,[16] we have shown that 30 nm Si_3N_4 nanoholes are required to obtain a single 10 nm silicon nanocrystal per each nanohole by electrochemical etching.

In the first section of this paper, we present the required nanohole properties. The second part is then devoted to the description of the fabrication process and the study of the influence of the ICP etching parameters (RF platen and coil powers, chamber pressure) on Si_3N_4 nanohole quality.

II. REQUIRED NANOHOLE PROPERTIES

A robust process to realize organized silicon nanocrystals by electrochemical etching on Si_3N_4 nanohole arrays requires specific nanohole properties. Indeed, the etching properties such as selectivity of Si_3N_4 over silicon, anisotropy, and the control of nanoholes size play an important role to insure the success of silicon nanocrystal fabrication. On the one hand, high etching selectivity of Si_3N_4 over silicon is required in order to stop at the Si_3N_4/Si interface and to avoid silicon etch. Even minor changes or damage occurring in a few nanometers of the superficial silicon layer has a major impact on electrochemical etching in view of the fact that silicon nanocrystals are formed on the silicon surface. It is then primordial to have a quasi-virgin silicon surface for the success of the process. On the other hand, Si_3N_4 nanohole sidewall shape is a very important parameter considering that electrochemical etching is driven by the electric current which can only pass through the Si_3N_4 openings. Since the current lines will follow the trajectory according to the geometrical shape of nanohole sidewalls, near vertical profiles are necessary to produce a good homogeneity of the electrochemical etching. Nanohole size represents also a key parameter for the nanocrystals formation considering that the applied current during electrochemical etching depends on the exposed silicon surface area. Thereafter, Si_3N_4 nanohole size must be precisely controlled to obtain reproducible results for the size and density of silicon nanocrystals.

III. NANOHOLE ARRAYS FABRICATION PROCESS

The main steps of our process are EBL and an inductively coupled plasma etching to fabricate templates in a Si_3N_4 thin film. A layer of about 30 nm thick Si_3N_4 was deposited using low pressure chemical vapor deposition (LPCVD) on a *p*-doped (100)-oriented silicon substrate with a resistivity of 1–10 Ω cm. The LPCVD process used the reaction of dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) with respective flow rates of 30 and 54 standard cubic centimeters per minute (sccm) at a temperature of 800 °C and a pressure of 200 mTorr. In order to prepattern the surface, a layer of ZEP520 resist diluted in anisole was spin-coated to a thickness of approximately 100 nm on Si_3N_4 layers. ZEP520 is a positive *e*-beam resist, consisting of copolymers of a-chloromethacrylate and a-methylstyrene that has high resolution, sensitivity and contrast as well as relatively good dry etch resistance.[17] Samples were then annealed at 180 °C for a few minutes. EBL was performed by means of a LEO1530 scanning electron microscope externally controlled by a computer equipped with lithography software using the nanometer pattern generation system (NPGS). The electron beam energy was fixed at 20 keV and the beam current was varied from 20 to 30 pA. In order to obtain nanoscale holes, a single point exposure scheme was used for each point. In this work, a point dose of 2 fC/point was used to write a field of 200 μm × 200 μm. After exposure, the development of the resist was completed using ortho-xylene, rinsed in methyl isobutyl ketone (MIBK) and dried in a nitrogen gas flow. This resist template is used as a mask for plasma etching. The Si_3N_4 holes were etched using STS advanced oxide etch inductively coupled plasma system in a gas mixture of $CF_4/He/H_2$. H_2 and He were added to the chemistry of Si_3N_4 plasma etching to improve the selectivity and the anisotropy of the process.[18,19] The chemistry and plasma etching parameters (pressure, RF coil, and platen powers) of the ICP system were optimized in order to obtain adequate etch rates for shallow nanostructures leading to a better control of the selectivity. Therefore, a gas mixture of $CF_4/He/H_2$ with respective flow rates of 16/140/14 sccm was used. The quality of Si_3N_4 nanoholes was studied under various plasma conditions for RF coil power varying from 100 to 200 W RF platen power from 15 to 150 W, and chamber pressure from 2 to 12 mTorr.

After Si_3N_4 etching, the resist was stripped using an oxygen plasma cleaning to remove any residual organics. This latter step is essential and very critical for our process since without proper cleaning, electrochemical etching does not produce repeatable nanocrystals. Generally, organic residuals and contaminations are removed by oxygen plasma cleaning. However, plasma O_2 conditions must be well optimized to avoid silicon surface damage. In this work, some samples were electrochemically etched just after oxygen plasma cleaning under different conditions. SEM observation of the Si surfaces after O_2 plasma treatment revealed no obvious change, but the electrochemical etching of silicon failed after oxygen plasma cleaning for power exceeding 100 W and for durations longer than 7 min. This is probably

due to the damage of the silicon surface caused by the oxygen plasma cleaning beyond these conditions. Several research groups[20,21] have studied the effect of plasma processing and it was demonstrated that plasma treatment can cause damage, structural change and defects of the superficial layer as a result of the energetic particle bombardment. This damage increases with increasing power and exposure time. Therefore, in this work we have optimized the cleaning process for a power of 100 W and a duration of 5 min to thoroughly clean samples before electrochemical etching without damaging the silicon surface.

IV. RESULTS AND DISCUSSION

All observations and measurements presented here were conducted by scanning electron microscopy. Two series of samples were used for each type of measurement in order to ensure reproducibility of the results.

Figure 1 shows the etch rates and selectivity for the three materials used in our process (Si_3N_4, ZEP520, and Si) as a function of RF platen power and pressure. The effect of RF platen power at fixed RF coil power of 100 W and chamber pressure of 4 mTorr is shown in Fig. 1(a). For RF platen power between 15 and 50 W, the etch rate of ZEP520 increases slightly; however, the etch rate of Si_3N_4 increases considerably. Therefore, the selectivity of Si_3N_4 over ZEP520 is increased. For a RF platen power of 50 W, this selectivity exhibits a maximum value greater than 5. Beyond 50 W, the etch rate of ZEP520 increases much faster whereas the Si_3N_4 etch rate increases much slowly. This involves the reduction of the Si_3N_4/ZEP520 selectivity. The strong increase of the ZEP520 etch rate beyond 50 W can be related to the temperature increase which accompany the increase of the RF platen power. Indeed, it was shown that ZEP520 is very sensitive to temperature.[22] While for silicon, the etch rate remains slow and almost constant compared to the etch rates of Si_3N_4 and ZEP520. Therefore, the Si_3N_4/Si selectivity increases significantly from 1 to 18 when the RF platen power is increased from 15 to 150 W.

The effect of the pressure at fixed RF coil power of 100 W and RF platen power of 50 W is shown in Fig. 1(b). The etch rate of Si_3N_4 increases significantly from 2 to 12 mTorr; however, the etch rate of ZEP520 deacreases slightly by increasing the pressure. Therefore, the selectivity of Si_3N_4 over ZEP520 increases with pressure. While for silicon, the etch rate remains almost constant by increasing the pressure from 2 to 12 mTorr; consequently, the selectivity of Si_3N_4 over silicon also increases. The variation of selectivities with pressure is as excepted for deep etching.[23]

Finally the obtained values of selectivities as a function of RF platen power and pressure provide an acceptable selectivities for this process considering the low thickness of Si_3N_4 layers to etch.

As shown in Fig. 2, by increasing the RF platen power from 50 to 150 W, the Si_3N_4 nanohole diameter increases and the sidewall angle approaches 90°. Increasing RF platen power enhances the directional ion bombardment, resulting in anisotropic etching. This behavior is as expected for deep etching. An example of cross-section SEM images of the profiles of one Si_3N_4 hole fabricated at respectively 50 and 150 W of RF platen power are shown in the inset in Fig. 2.

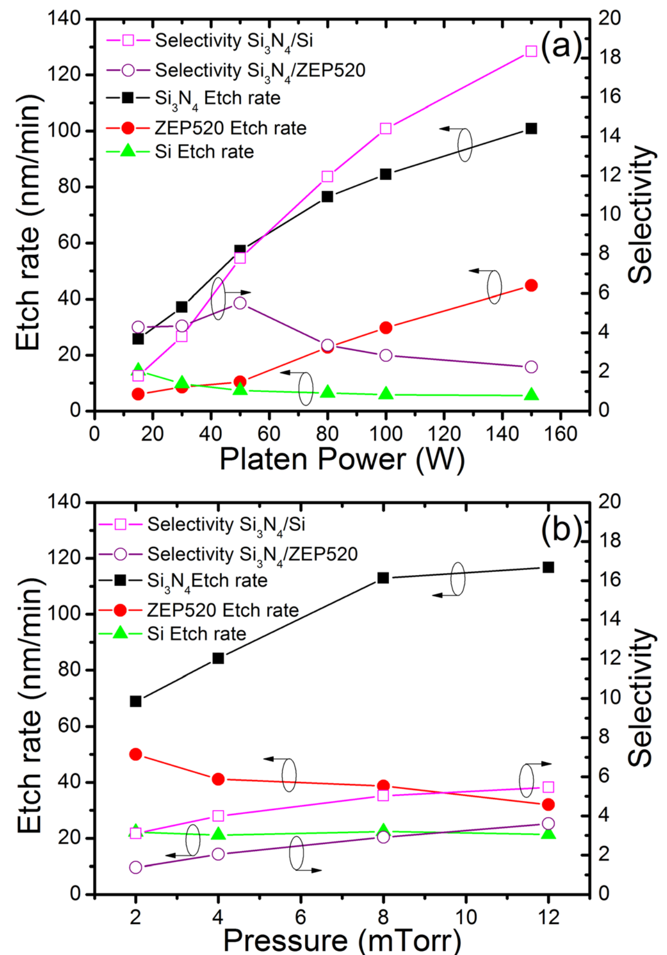

FIG. 1. (Color online) (a) Etch rates and selectivity of Si, Si_3N_4 and ZEP520 as a function of RF platen power. (b) The etch rates and selectivity of Si, Si_3N_4 and ZEP520 as a function of pressure.

The effect of the RF coil power on nanohole diameter and sidewall angle is illustrated in Fig. 3. At fixed RF platen power of 50 W and chamber pressure of 4 mTorr, Si_3N_4 nanoholes become larger up to a doubling of the diameter with increasing the RF coil power from 100 to 200 W and sidewall angles approach a straight vertical profile within a few degrees.

As depicted in Fig. 4, the pressure variation between 2 and 12 mTorr does not affect the nanohole diameter on surface at fixed RF coil and platen powers of respectively 100 and 50 W. However, the sidewall angle was found to be more sensitive to pressure variations. Indeed, by increasing the pressure from 2 to 12 mTorr, the sidewall angle increases and a nearly vertical sidewall profile can be achieved. This behavior was also observed by other researchers.[24]

With the optimized parameters, we thus precisely control the influence of the plasma conditions on Si_3N_4 nanohole properties (silicon surface quality, verticality, and nanohole size). By choosing proper ICP etching conditions, a good compromise between size, anisotropy and selectivity can be achieved in order to obtain high quality Si_3N_4 nanoholes

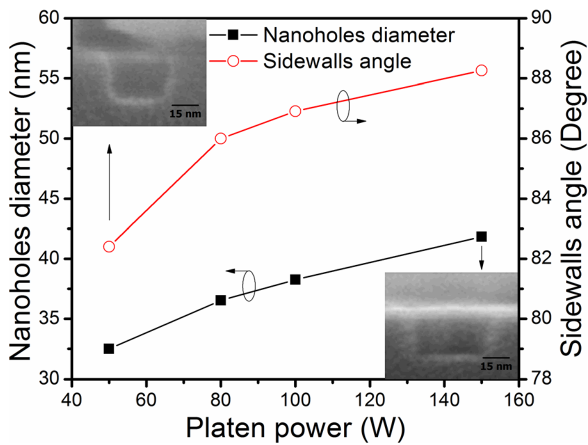

FIG. 2. (Color online) Si_3N_4 nanoholes diameter on surface and sidewalls angle as a function of RF platen power.

well adapted to be used as a mask for silicon nanocrystal organization.

This etching process is limited by the lithography resolution. For ZEP520 electroresist, the resolution can reach 20 nm.[25] However, in this work, we have optimized the ICP process in order to obtain organized 10 nm silicon nanocrystal arrays realized by electrochemical etching through Si_3N_4 templates. Since the obtained nanocrystal size and density depends on the nanohole surface area for an electrochemical etching process, a nanohole diameter of 30 nm is required to obtain a single 10 nm diameter silicon nanocrystal per each hole.[16]

Figure 5 presents a typical example of organized silicon nanocrystals obtained by using the developed process of ordered Si_3N_4 nanohole arrays. Figure 5(a) shows a SEM image on the surface of nanohole arrays obtained in Si_3N_4 layers by EBL and ICP etching. Holes of ~30 nm diameter and 200 nm spacing were obtained in Si_3N_4 layers with a good control of the selectivity of Si_3N_4 over Si and a reasonably near-vertical profile. Ordered arrays of homogenous silicon nanocrystals localized in these prepatterned Si_3N_4 nanoholes could then be obtained by a short electrochemical

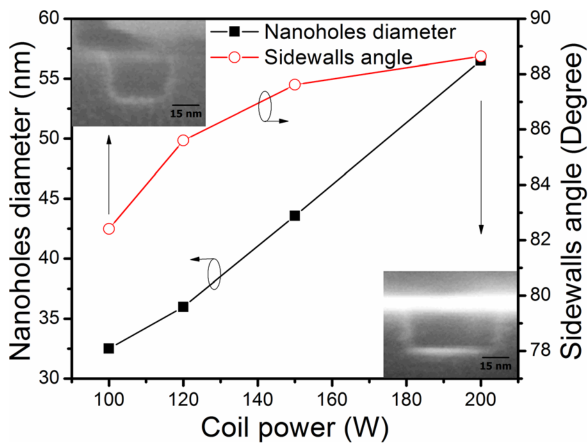

FIG. 3. (Color online) Si_3N_4 nanoholes diameter on surface and sidewalls angle as a function of RF coil power.

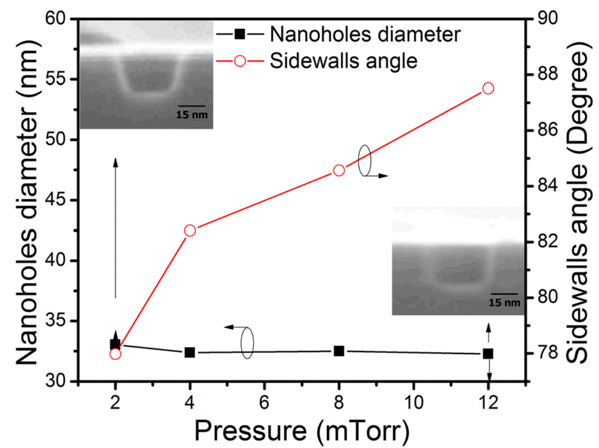

FIG. 4. (Color online) Si_3N_4 nanoholes diameter on surface and sidewalls angle as a function of pressure.

etching current pulse. An example of the obtained nanocrystals with a single silicon nanocrystal per each hole is shown in Fig. 5(b). These nanocrystals have a diameter of approximately 10 nm and a height of 4 nm with a conical shape with the same crystallographic orientation as the silicon substrate.[16]

V. SUMMARY AND CONCLUSIONS

In summary, we have developed a process for Si_3N_4 nanohole templates fabrication. We have demonstrated that ICP systems which are rather designed for deep and fast

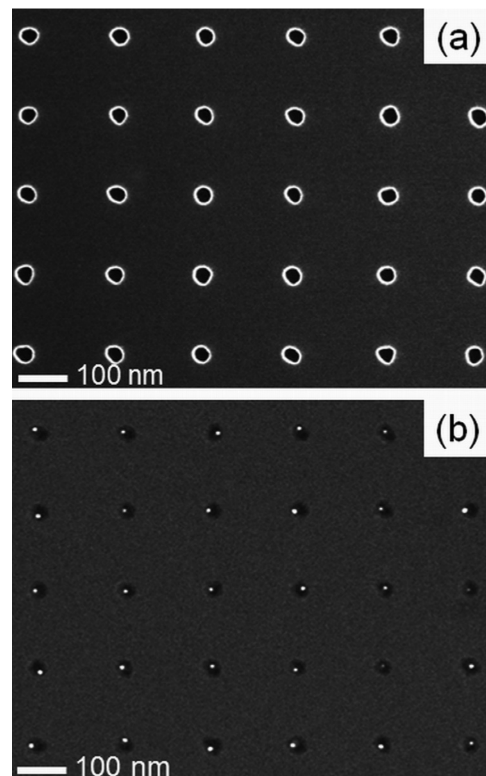

FIG. 5. (a) Si_3N_4 nanoholes array obtained by EBL/ICP. (b) Array of localized Si nanocrystals after electrochemical etching through Si_3N_4 nanoholes.

etching can be used for shallow nanostructure etching (about of 30 nm thick). High quality Si_3N_4 nanohole templates have been successfully demonstrated through the use of EBL and ICP. The influence of ICP parameters (the chamber pressure, the RF coil and the platen powers) on Si_3N_4 nanoholes quality has been discussed. A good compromise between size, anisotropy and selectivity can be achieved to obtain optimal Si_3N_4 nanohole templates compatible with the subsequent fabrication process for the organization of silicon nanocrystals formed by an electrochemical etching technique. These results thus show the high value of ICP system for the fabrication of high resolution of nanoscale patterns in very thin Si_3N_4 films. This process is very promising for many applications and especially for organization of silicon nanocrystal realized by electrochemical etching which can be used in future for large scale fabrication of single electron devices.

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