Hindawi
Journal of Nanomaterials
Volume 2017, Article ID 8613571, 8 pages
https://doi.org/10.1155/2017/8613571

Hindawi

Research Article

A Fabrication Process for Emerging Nanoelectronic Devices Based on Oxide Tunnel Junctions

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Received 28 June 2016; Revised 30 September 2016; Accepted 12 October 2016; Published 23 February 2017

Academic Editor: Li Ji

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We present a versatile *nanodamascene* process for the realization of low-power nanoelectronic devices with different oxide junctions. With this process we have fabricated metal/insulator/metal junctions, metallic single electron transistors, silicon tunnel field effect transistors, and planar resistive memories. These devices do exploit one or two nanometric-scale tunnel oxide junctions based on TiO_2, SiO_2, HfO_2, Al_2O_3, or a combination of those. Because the *nanodamascene* technology involves processing temperatures lower than 300°C, this technology is fully compatible with CMOS back-end-of-line and is used for monolithic 3D integration.

1. Introduction

The microelectronic industry has been able to drastically increase the computing performance while reducing the cost-per-chip over the years. To keep this performance pace, system innovations considering architectures, interconnects, and packaging were required in addition to traditional CMOS scaling [1]. This tendency to increase performances in every aspect of the devices, circuits, systems, and packaging has led to power densities of assembled modules that are reaching levels where standard air cooling is not adequate anymore [2]. In parallel, low-power and ultra-low-power devices and circuits have been required for the ever-increasing demands of mobile applications such as smartphones or tablets and for autonomous systems that could be used for Internet of Things applications. In both ways, the power consumption has become one of the predominant factors for introducing new devices or systems to complement CMOS and add functionality or increase performances.

Tremendous efforts have been deployed to increase the number of devices by mm^2 through 3D integration at the chip or package level. To achieve 3D integration, heterogeneous and monolithic approaches can be pursued. The heterogeneous integration has been developed to stack several chips coming from different technology platforms and to connect them using wafer bonding and through-silicon-vias (TSVs) [3]. More recently, a 3D monolithic integration technology has been proposed by the CEA Leti [4]. With their fabrication process they have been able to integrate on a single technology platform two levels of advanced CMOS transistors on top of each other using different substrates that have been bonded at low temperature. The two levels of transistors

have been connected using mature microelectronic copper interconnects.

We propose to integrate nanoelectronic devices in the back-end-of-line (BEOL) of CMOS technology in a 3D monolithic fashion using a single substrate and standard microelectronic industrial processes. We present four functional devices that are fabricated using the versatile *nanodamascene* platform: (i) metal/insulator/metal (MIM) capacitors; (ii) metallic single electron transistors (SET); (iii) silicon nanocrystal tunnel field effect transistors (TFET); and (iv) planar nanometric resistive random access memories (RRAM). All the proposed devices exploit single or double nanometric tunnel junctions based on oxides that have been grown or deposited. They differ from one another mainly by their dielectric junction dimensions and material and thus the associated conduction mechanisms. A first integration of a SET in the BEOL of a 32 nm CMOS technology is presented in the last section.

2. The Nanodamascene Process

We have developed the *nanodamascene* process that can produce extraordinarily small capacitance tunnel junctions with an accurate control on the oxide junction area. This process that can be realized on any types of flat surface is described in more detail in [5]. This method is similar to an industry damascene technology; however three aspects are particular to the *nanodamascene* process: (i) the possibility to create single, double, or multiple dielectric junctions in a single CMP step; (ii) the planarization of very narrow structures, down to 20 nm in width, together with larger 2 μm microstructures; and (iii) the depth of the nanostructures, z dimension, is precisely controlled down to the nanometer range and can be tuned in-process as no etch stop layers are used to control the planarization. Figure 1 shows a schematic of a typical *nanodamascene* process flow used for the fabrication of SETs with the top down view on the left and the related cross section on the right.

A trench in silicon oxide layer is formed (step 1 of Figure 1) using electron beam lithography in positive resist followed by a −20°C CF_4 inductively coupled plasma oxide etch to precisely control the trench depth, reach almost vertical sidewalls, and minimize line edge roughness to less than 1 nm [6]. The patterning of the center electrode can be achieved using either a metal lift-off step or, to increase fabrication yield, a metal deposition followed by lithography and etching [7] (step 2 of Figure 1). The Al_2O_3 oxide barrier (step 3 of Figure 1) is deposited on the entire surface using atomic layer deposition (ALD). TiO_2, SiO_2, and HfO_2 oxide junctions, as presented in the devices section, have been deposited by means of physical vapor deposition (PVD) or grown using plasma oxidation. ALD allows subnanometer thickness control, highly conformable deposition, and reproducible dielectrics quality and can be used for multiple material crested barriers [8], while plasma oxidation is a simple, low-cost process that leads to a single material junction that is the metal island oxide. A thick metal layer, approximately 2 times the trench depth, is deposited by PVD to ensure good conformity and void-free trench filling [5] (step 4 of Figure 1). Finally, chemical mechanical planarization (CMP) is used to first planarize the sample surface, remove the excess metal, and then control the device height with a nanometric resolution (step 5 of Figure 1). The electrical characterization of a nearby metallic nanowire that is less than 20 μm away from the fabricated nanoelectronic device allows measuring precisely, in-process, the remaining thickness of metal in the trench and adjusting the CMP step, if needed.

Figure 2 shows the main fabrication steps results of SETs with two different layouts. The silicon oxide trenches (Figure 2(a)) illustrate step 1 of Figure 1. They are 20 nm deep and 20 nm wide. Figure 2(b) SEM picture represents a 20 nm TiN line used to define the device central island (step 2 of Figure 1) that has been obtained with an HSQ based electron beam lithography step and chlorine etching plasma [7]. Figures 2(c) and 2(d) show a scanning electron microscopy (SEM) and atomic force microscopy (AFM) picture of a fabricated device after final planarization. The AFM measurement demonstrates that the achievable flatness after CMP planarization is better than 5 nm.

3. Nanodamascene Devices Fabrication

Our approach is to exploit the *nanodamascene* process to fabricate different nanoelectronic devices such as MIM capacitors, metallic SETs, nanocrystalline silicon TFETs, and planar nanometric RRAMs. This implies numerous CMP process developments to adapt the nanofabrication to the various geometries, dimensions, and many materials of the different devices proposed. Moreover, the *nanodamascene* process has a low thermal budget and materials are fully compatible with CMOS back-end-of-line (BEOL) technology. The aforementioned low-power nanoelectronic devices can then be fabricated above CMOS integrated circuits using a 3D monolithic technology. This paves the way for low-power logic, memory, and/or new functionalities such as sensors, while the CMOS devices will be used for high-performance logic and memory and I/O signals restoration.

3.1. Metal/Insulator/Metal Capacitors. The MIM junction is the building block of the different nanoelectronic devices proposed in this paper, and the MIM oxide capacitors that are essential passive devices widely used in the microelectronic industry integrated circuit fabrication. They can be exploited for more fundamental research purposes such as dielectric or dielectric stacking [8, 9] permittivity and barrier height extraction at the nanometer scale. Finally, as it will be shown here, they are excellent devices to evaluate the effect of the fabrication procedure, materials, and deposition methods on the junction and characterize its aging and performance before using it in a circuit.

The fabrication of a MIM tunnel junction is very similar to the process described in Figure 1. However, instead of the two tunnel junctions, one wants to obtain a single dielectric junction. Therefore, the first metal electrode goes all the way to the contact [9]. Figure 3 presents the I-V characteristic of two Ti/TiO_2/TiN/Ti MIM tunnel junctions with 40 nm and 100 nm width at three different consecutive CMP steps: t_0 + 10 s, t_0 + 20 s, t_0 + 45 s (step 5 of Figure 1), where t_0 is

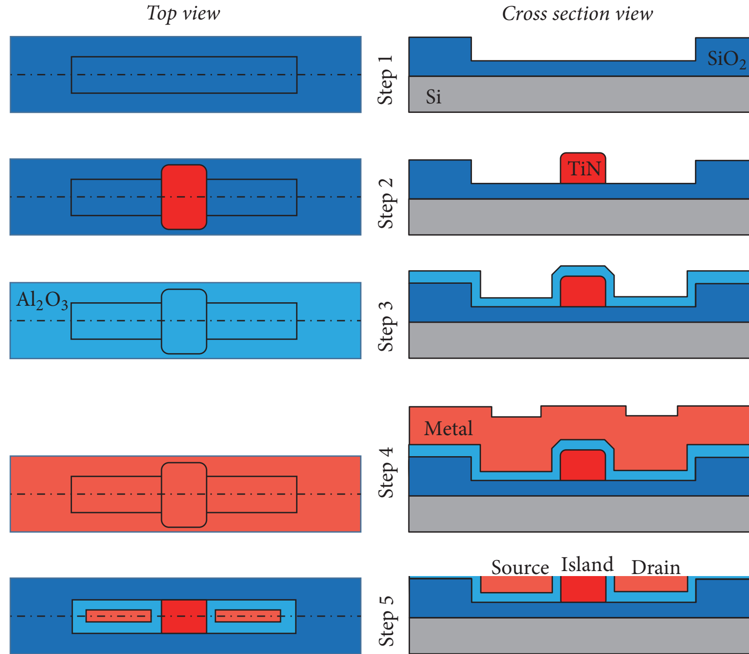

FIGURE 1: *Nanodamascene* process flow, illustrated for the fabrication of a SET device. Left: top down view. Right: cross section view. From top to bottom: trench formation in dielectric layer; metal line definition by lift-off or etching step; dielectric deposition by ALD or PVD; blanket metal layer deposition; CMP planarization step.

the time at which no more metal stands on the surface but only in the etched structures. The TiO_2 tunneling dielectric has been obtained by controlled plasma oxidation of the first Ti electrode [10], and the TiN serves as a capping film. The device thicknesses have been extracted using a four-probe resistance electrical measurement on nanowires close to the MIM junctions [6]. When CMP is further processed after t_0, metal electrodes and dielectric junction depth are reduced, and so is the tunneling current. In Figure 3 the current is not decreasing linearly with the device thickness. This is explained by two factors that have been deducted from electrical characterization on multiple MIM devices with different dielectric materials and dimensions: (i) the electrode metal resistivity is not constant anymore but increases exponentially when the metal thickness is lower than the electrons mean free path, approximately 20 nm in this case; (ii) due to CMP selectivity the junction depth is slightly smaller than the electrode depth and this is exacerbated as the device becomes very shallow.

The *nanodamascene* process allows the fabrication of planar MIM tunnel junctions of nanometric sizes and attofarad capacitances. Theses junctions can be used for fundamental characterization of dielectric materials and stacking of materials, evaluation of MIM capacitors performances and aging, and the fabrication of nanoelectronic devices as it will be shown in the following sections.

3.2. Metallic Single Electron Transistor. Single electron transistors have attracted high interest in the past due to their unique coulomb blockade effect, periodic I_{ds}-V_{gs} characteristic, ultra-small devices dimensions, and very low-power consumption [11]. However, two major hurdles have prevented SET to be integrated in modern circuits and systems: room temperature operation and very low current drive. To work at room temperature, a SET needs very low tunnel capacitances, together with high transparency for a sufficient current drive. This leads to extremely miniaturized dielectric junctions with a low dielectric permittivity material to minimize the island total capacitance C_Σ. With the *nanodamascene* platform we have the tools to overcome these two hurdles. The metallic SET fabrication can be carried out in the CMOS BEOL to integrate SET-CMOS hybrid circuits and benefit from both the high CMOS current drive and SET novel functionalities [12].

Figure 4 shows a SET diamond plot that is the drain current I_{DS} as a function of the source-drain voltage V_{DS} and gate voltage V_G. The device has been fabricated using the process described in Figure 1. In order to demonstrate the full fabrication process feasibility, the SET dimensions have been relaxed. Titanium is used for the device island and electrodes, while the junctions are composed of TiO_2 grown by plasma oxidation and a TiN capping layer deposited by PVD. The electrical characterization has been carried out at 1.5 K in a variable-temperature-insert cryostat. The device physical dimensions have been extracted from SEM and AFM characterizations. The island is 23 nm long and 28 nm wide. The island and electrodes depth after CMP is 10.5 nm and is extracted from nanowire resistance measurements, while the TiO_2 tunnel junction is 2.5 nm thick. The lateral control gate is 39 nm away from the SET island, and the gate dielectric is silicon thermal oxide. Figure 2 shows a SEM and an AFM picture of SETs similar to the one characterized here.

The capacitances of the device presented on Figure 4 are C_S = 35.6 aF, C_D = 39.1 aF, C_G = 0.62 aF, and C_Σ = 75.3 aF.

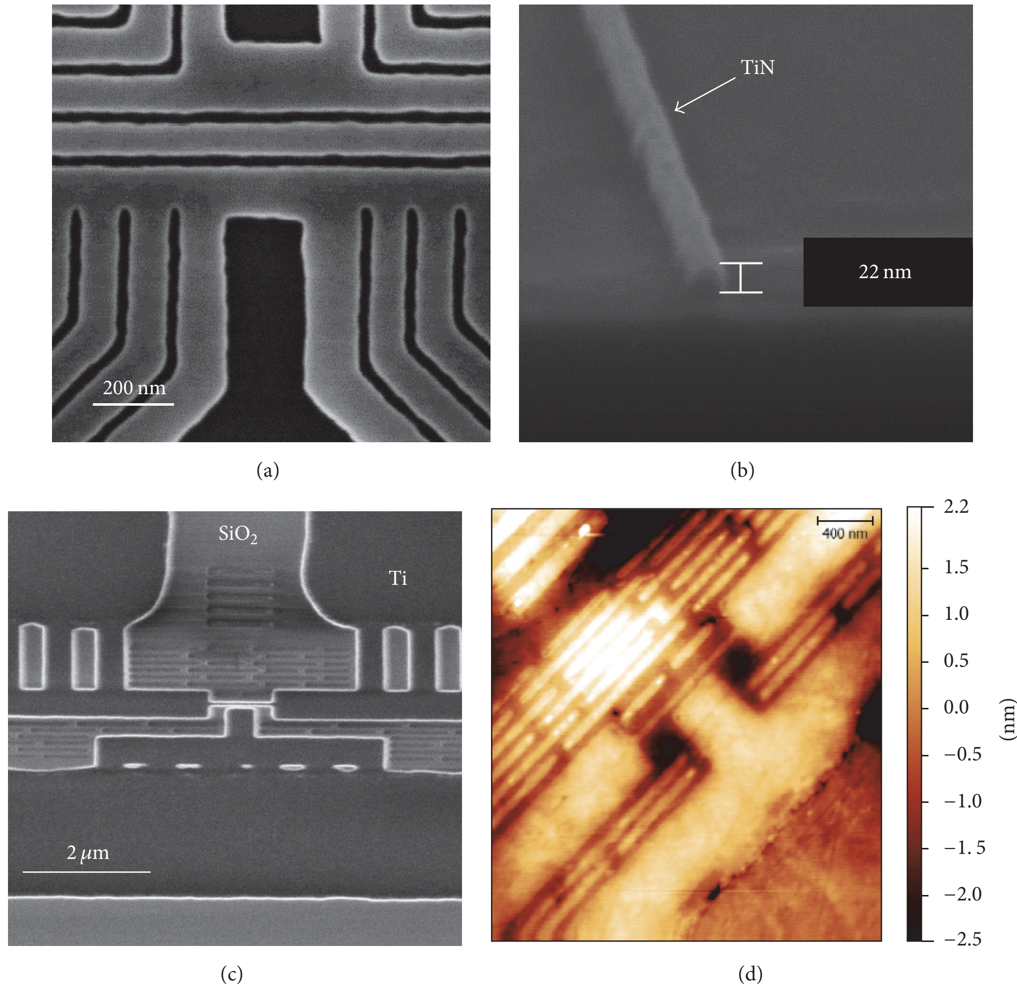

Figure 2: In-process SETs fabrication micrographs: (a) trench formation in silicon oxide using ZEP520 resist; (b) patterning of the central island in TiN using HSQ resist; (c) top down view of completed device after the CMP step; (d) AFM view of the planarized surface.

These values have been extracted from the negative and positive slopes of the diamonds for the source and drain capacitances, C_S and C_D, respectively, the pitch of the Coulomb blockade regions for the gate capacitance, C_G, and their sum for the total island capacitance, C_Σ. Capacitances have been modeled using a finite element method (FEM) to be able to design future devices and junctions with proper materials and stacking without the need to go through many fabrication runs. In this model, the Poisson equation $\nabla^2 V = -\rho/\varepsilon$ is solved to extract the charge density ρ from the fabricated device physical dimensions, applied voltages (V), and the material dielectric permittivity (ε_r). The capacitance is then calculated through the $C = Q/V$ relation [13].

SET room temperature operation requires very low tunnel and island capacitances, almost one order of magnitude smaller than the one obtained with the relaxed dimensions device proposed here. The temperature dependence of the SET Coulomb blockade has been measured and a maximal operating temperature of ~5 K is found. This is explained by the device dimensions which increase the total capacitance of the island and decrease the charging energy. Monte-Carlo simulations [14], using the above calculated capacitances, fit the data in a straightforward way with ε_r for the tunnel oxide of ~18. The development of the FEM modeling, together with the devices Monte-Carlo simulations, is another tool of the *nanodamascene* platform that would help to design room temperature nanoelectronic devices with proper dimensions and junction dielectrics or stacking [15]. Reducing the tunnel oxide ε_r, increasing its thickness, and reducing the junction cross section would increase the charging energy to reach room temperature operation [16]. For that purpose, the tunnel oxide permittivity can be tuned using barrier engineering and ALD [8]; the tunnel junction width can be decreased combining more aggressive lithography and trench filling using ALD, while the island thickness can be reduced to few nm with CMP as in [5].

3.3. Silicon Nanocrystal Field Effect Transistor. Tunneling field effect transistors are promising devices for the beyond CMOS era due to their potential sub 60 mV/decade subthreshold slopes (SS) and low-power consumption [17]. Typical TFETs have source, channel, and drain doping that form a

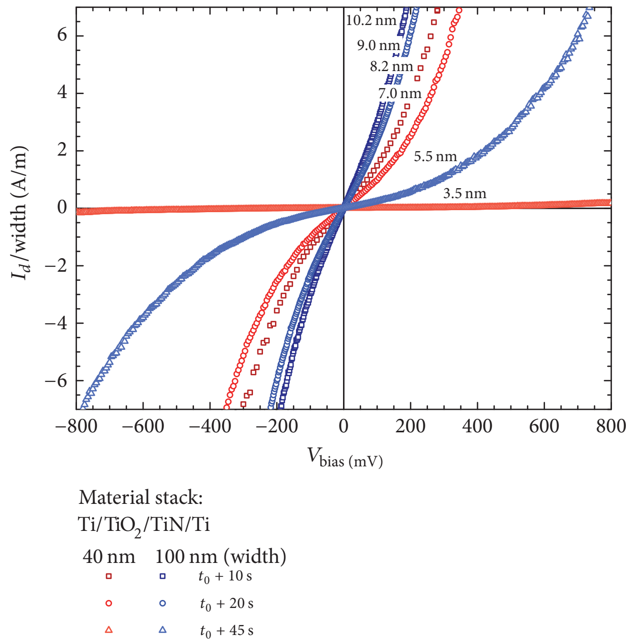

Figure 3: Measured I-V characteristic of a 40 nm and a 100 nm wide Ti/TiO_2/TiN/Ti tunnel junction as a function of device thickness (numbers given on the different curves) for t_0 + 10 s, t_0 + 20 s, and t_0 + 45 s. The device thickness has been extracted with four-point probe resistance measurement on close-by nanowires.

p-i-n junction with very abrupt doping profiles to get almost atomically sharp junctions. Here we propose a nanocrystal field effect transistor (ncFET) with metallic source and drain that sandwich an intrinsic silicon nanocrystal. Its conduction mechanism relies on the gate-induced modulation of a tunnel barrier that can, in principle, reach sub 60 mV/decade SS and extremely low leakage current [18].

The ncFET electrical characteristics shown on Figure 5 are obtained from a device with an architecture that is similar to a SET architecture. It has an island formed of nonintentionally doped silicon nanocrystal separated from the Ti source/drain leads by a thin native silicon dioxide layer. The island is formed by plasma etching of an amorphous silicon (a-Si) island that conformably filled the SiO_2 trench. This island was then annealed to form polycrystalline silicon. The SiO_2 tunnel junctions are prepared by first deoxidizing the polycrystalline silicon and then letting a natural oxide layer form with a thickness estimated to be 0.5 nm. Ti metal leads are deposited by PVD. The final CMP step only leaves a single Si nanocrystal that is connected to the Ti source/drain and isolated in the nanometric trench that was previously patterned. More fabrication details can be found here [18]. The device has been measured at room temperature and down to 1.7 K. It can be seen that the electrical characteristic is ambipolar and there is no visible temperature dependence which are indications that the current is driven by a tunneling effect. An 86 nm thermal oxide gate dielectric was standing between the metal gate and the silicon island which explains the poor electrostatic control and high gate voltages needed. However, it has shown excellent I_{off} current (30 pA/μm) with a 10^4 on/off ratio [18]. As it has already been demonstrated for TFETs [16, 19] and Schottky barrier FETs [20], the use of thinner high-K dielectrics, coupled with thinner and shorter Si channel, and a properly aligned gate would drastically improve the transistor performances in terms of SS and $I_{\text{on}}/I_{\text{off}}$ ratio and make it a very suitable candidate for a low-cost BEOL integration. Adding a state-of-the-art ALD high-k dielectric gate stack could reduce the equivalent oxide thickness from 86 nm to below 1 nm. This would correspond to scaling of the gate voltage from 30 V to 0.35 V and of the subthreshold slope from 4500 mV/decade to below 52 mV/decade, making it useful for low-power applications.

3.4. Planar Nanometric Resistive Memory. Resistive memories are promising devices that could be part of the memories catalog or eventually replace nonvolatile flash memory in the future [21, 22]. Among all competing technologies for the next generation of solid-state memory, RRAM combines all the virtues requested by industry [1], which explains the tremendous research efforts that have been carried out by research groups in both universities and microelectronic industries. In addition to their low-cost fabrication, RRAM can compete with other memories in terms of performances: more than 10^6 cycles' endurance, 50-nanosecond switching speed, and being able to sustain 2×10^4 hours' operation at 250°C [22]. Device scalability is another asset of RRAM. In a crossbar configuration, $4F^2$ cell footprint can be attained, F being the minimum feature size of a technology node [23].

In traditional RRAM, a resistance switching cell is a vertical two-terminal device, consisting of two electrodes, which sandwiches a resistance switching material. The first electrode is patterned, the switching materials are deposited on the whole surface, and the second electrode is patterned perpendicularly to the first one. The resulting device is a vertical structure where the surface is controlled and limited by the lithography resolution and where the covering of the dielectric and second metal electrode on the first electrode sidewalls may be problematic. Here we propose, for the first time, a planar RRAM structure where both electrodes and the junction are in-plane (inset of Figure 6) and the junction surface/depth is controlled precisely in the nanometer range by the planarization step. As mentioned previously, the junction material can be either deposited by PVD or ALD for better thickness and conformability control or obtained through plasma oxidation. Figure 6 shows the electrical characterization of a planar Ti/HfO_2/TiN/Ti RRAM device fabricated using a tailored *nanodamascene* process. The switching dielectric is a 12 nm thick PVD HfO_x, and the junction surface is $180 \times 40\,\text{nm}^2$. The schematic in the lower left inset illustrates the device with the two contact pads used for electrical characterization.

The I-V characteristic demonstrates the switching mechanism with clear SET and RESET. The DC voltage sweeps have been applied to the active Ti electrode, while the passive TiN electrode was grounded. The electrodes resistance, mainly due to the dimension of the electrodes, has been measured at 8 kOhms, using a nearby Ti nanowire. Taking into account this contact resistance, the RRAM $R_{\text{ON}}/R_{\text{OFF}}$

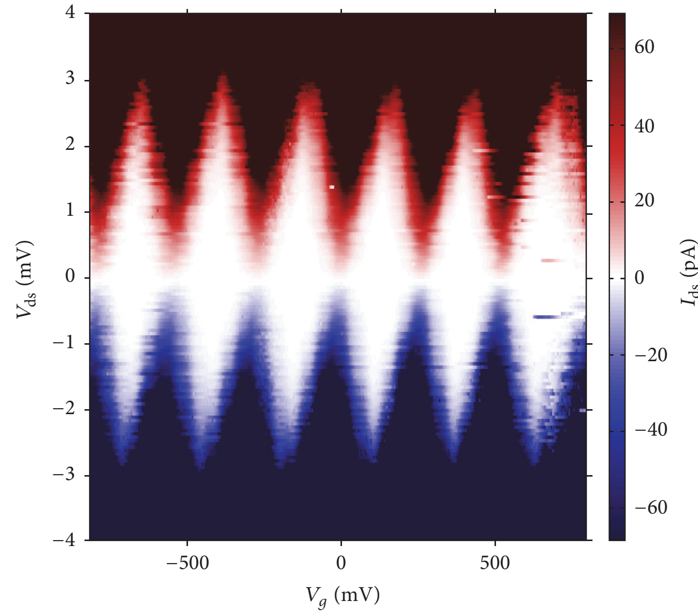

Figure 4: Ti/TiN/TiO_2/Ti/TiO_2/TiN/Ti single electron transistor V_{GS}/V_{DS} diamond plot measured at 1.5 K.

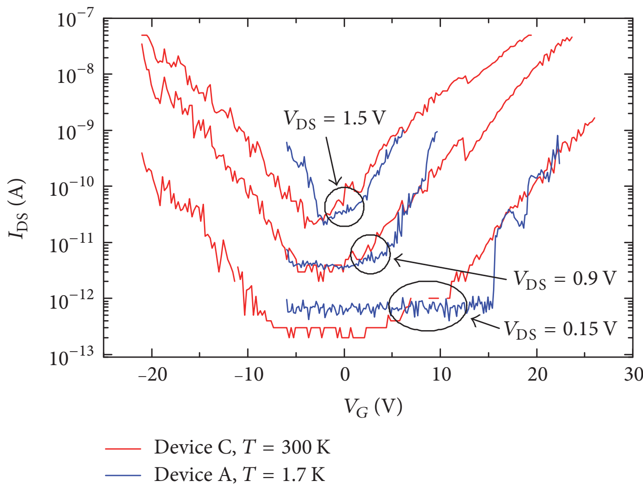

Figure 5: I_{DS}-V_{GS} electrical characteristic of a fabricated Si TFET at 300 K and 1.7 K, for three different source/drain V_{DS} bias.

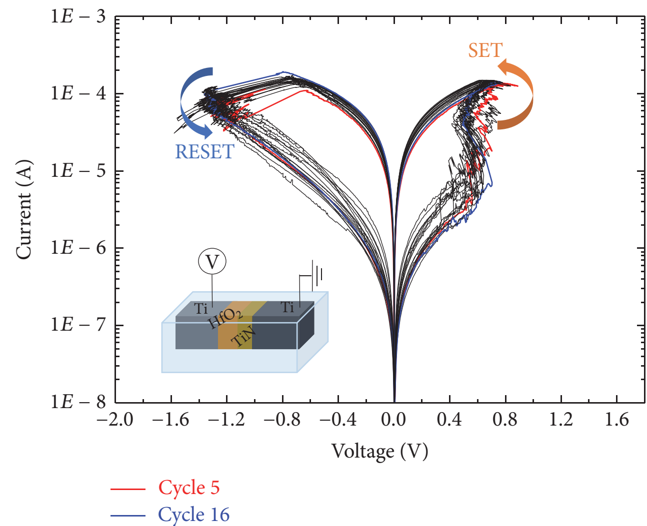

Figure 6: I-V switching electrical characteristic of a 180 × 40 nm^2 Ti/HfO_2/TiN/Ti fabricated planar RRAM device with a 12 nm HfO_x switching junction. The schematic represents the planar device, while the smaller on the right plot gives the R_{ON}/R_{OFF} ratio.

ratio is 150. The device has been cycled 20 times with identical operating voltages and RESET current and was still fully functional with very small deviations, despite the fact that no transistor was used to limit the current in the device (1T/1R configuration). The red and blue curve on Figure 6 highlight the small deviation between the measurement cycles 5 and 16, respectively. Figure 7 shows an Energy Filtered Transmitted Electron Microscope (EFTEM) cross section of a Ti/HfO_x/TiN switching junction after CMP and before electrical characterization. The integrity of the interfaces is confirmed and both HfO_x and TiN sputtering depositions are conformal on the first patterned Ti electrode. The junction is 22 nm high, with a 6 nm thick HfO_x layer. Multiple devices have been fabricated using identical process and materials and showed reproducible characteristics with an electroforming voltage distributed around 5 V, SET and RESET voltages lower than 2 V, and a RESET current about 100 μA [24, 25].

4. Monolithic 3D Integration

3D integration paves the way for increased devices density and performances. As system-on-chips (SOCs), it allows the integration of different technologies and/or applications in a

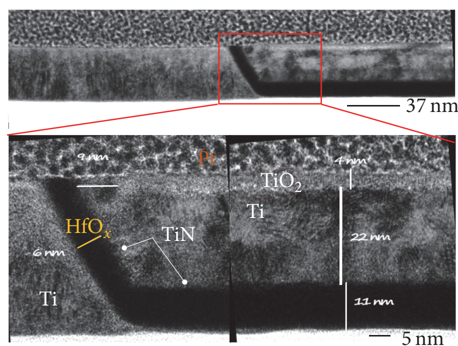

Figure 7: EFTEM cross section of a Ti/HfO_x/TiN junction after CMP. Interfaces are clearly defined and HfO_x and TiN depositions are conformal on the Ti left electrode.

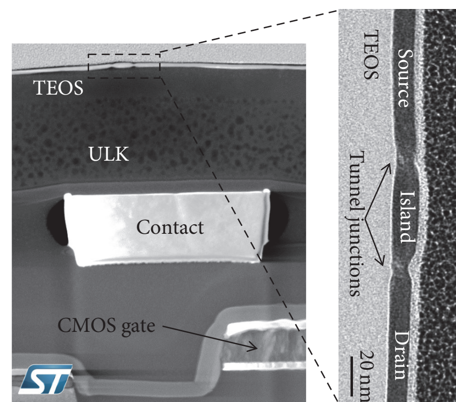

Figure 8: TEM cross section images of a SET fabricated in the BEOL of a 32 nm CMOS circuit. The CMOS gate and first BEOL metal contact are clearly identified in the lower image, while the top cross section shows a magnified image of the SET device.

single module and thus increases the chip functionality. The shorter interconnects of 3D systems improve the bandwidth and greatly diminish the power consumption by reducing the interconnect RC losses. Among 3D integrations, many technologies are already exploited. The first one is the heterogeneous integration at the packaging level. The different chips are stacked on each other and/or integrated on an interposer to adapt the I/O pitch from the chip to the printed circuit board. This technology is the most mature but has a high cost of fabrication. It needs through-silicon-vias (TSVs), multiple chips, silicon interposers, adapted designs, and many added fabrication steps and masks.

On another hand, monolithic integration proposes to integrate the stacked transistors on a single silicon chip. Leti proposed recently [4] a 3D monolithic system with two layers of high-performance silicon transistors. A Si wafer is bonded on a processed and functional CMOS substrate at low temperature and the devices are fabricated on this second substrate giving rise to two levels of CMOS circuits [26]. The main challenges of this technique reside in the ability to process a high-performance top transistor at temperatures lower than 600°C and to be able to design proper high density contacts for the two levels of transistors. This for sure comes with a cost and is limited to two levels of transistors to date.

Among monolithic 3D integration technologies, the BEOL integration has the great advantage of being the lowest cost 3D technology. It is, however, limited to standard microelectronic materials, metallic devices, or lower performance semiconductor devices as it necessitates low thermal budget processes. When those limitations are respected there are almost no limitations to the number of layers that can be stacked. With the *nanodamascene* process and the 4 different applications proposed above, we are able to fabricate devices on top of CMOS without degrading the CMOS devices and circuits lying underneath. Figure 8 illustrates this type of 3D BEOL monolithic integration. A Ti/TiO_2/Ti/TiO_2/Ti SET has been fabricated on top of a 32 nm CMOS circuit [26]. The CMOS physical integrity has been verified with transmission electron microscopy (TEM) characterization. The 32 nm transistors have been electrically measured before and after the BEOL fabrication and no performance degradation has been revealed. With this 3D technology, one can imagine that SETs could be used for gas sensing due to their extreme charge sensitivity, or RRAMs for high density memory, while the front-end-of-line CMOS serves as signal amplification and input/output (I/O) to other chips or systems.

5. Conclusion

The *nanodamascene* process has been used for successful fabrication of fully functional nanometric oxide junctions based MIM, metallic SETs, silicon ncFETs, and for the first time planar nanometric RRAMs. The *nanodamascene* process is a versatile technique that can be toggled for the fabrication of diverse nanoelectronic devices. There are almost no limitations for the oxide materials that can be used for the junctions as long as they can be deposited by PVD, ALD, or low temperature CVD. The MIM and SET modeling and simulation tool using FEM coupled with Monte-Carlo simulation is another asset of the *nanodamascene* platform that can be used for design purposes. A 3D monolithic BEOL integration of a SET on top of a 32 nm CMOS circuit has also been demonstrated. Due to its low thermal budget and the use of microelectronic materials, this fabrication technique can be exploited for the fabrication of 3D chips with increased functionality and/or performances.

Competing Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Acknowledgments

This work was supported by Natural Sciences and Engineering Research Council of Canada and Fond de Recherche Nature et Technologie du Québec.

References

[1] ITRS—International Technology Roadmap for Semiconductors, ITRS Organisation. Executive Summary.

[2] B. Meyerson, "Echoes of DACs past: from prediction to realization, and Watts next?" in *Proceedings of the 47th IEEE Design Automation Conference (DAC '10)*, Anaheim, Calif, USA, June 2010.

[3] S. S. Iyer, T. Kirihata, and J. E. Barth, "Three dimensional integration—considerations for memory applications," in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC '11)*, San Jose, Calif, USA, September 2011.

[4] M. Vinet, P. Batude, C. Fenouillet-Beranger et al., "Monolithic 3D integration: a powerful alternative to classical 2D scaling," in *Proceedings of the SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S '14)*, IEEE, Millbrae, Calif, USA, October 2014.

[5] M. Guilmain, T. Labbaye, F. Dellenbach, C. Nauenheim, D. Drouin, and S. Ecoffey, "A damascene platform for controlled ultra-thin nanowire fabrication," *Nanotechnology*, vol. 24, no. 24, Article ID 245305, pp. 1–8, 2013.

[6] M. Guilmain, A. Jaouad, S. Ecoffey, and D. Drouin, "SiO_2 shallow nanostructures ICP etching using ZEP electroresist," *Microelectronic Engineering*, vol. 88, no. 8, pp. 2505–2508, 2011.

[7] B. Lee Sang, M.-J. Gour, M. Darnon et al., "Selective dry etching of titanium nitride nanostructures with chlorine-based inductively coupled plasma," in *Proceedings of the 40th International Conference on Micro- and Nano-Engineering (MNE '14)*, Lausanne, Switzerland, September 2014.

[8] K. G. El Hajjam, M. A. Bounouar, N. Baboux et al., "Tunnel junction engineering for optimized metallic single-electron transistor," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2998–3003, 2015.

[9] G. Droulers, S. Ecoffey, M. Guilmain, A. Souifi, M. Pioro-Ladriere, and D. Drouin, "Damascene planar metal-insulator-metal tunnel junctions," in *Proceedings of the 14th IEEE International Conference on Nanotechnology (IEEE-NANO '14)*, pp. 884–887, Ontario, Canada, August 2014.

[10] G. Droulers, A. Beaumont, J. Beauvais, and D. Drouin, "Spectroscopic ellipsometry on thin titanium oxide layers grown on titanium by plasma oxidation," *Journal of Vacuum Science & Technology B*, vol. 29, no. 2, Article ID 021010, 2011.

[11] K. K. Likharev, "Single-electron devices and their applications," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 606–632, 1999.

[12] S. Mahapatra, V. Vaish, C. Wasshuber, K. Banerjee, and A. M. Ionescu, "Analytical modeling of single electron transistor for hybrid CMOS-SET analog IC design," *IEEE Transactions on Electron Devices*, vol. 51, no. 11, pp. 1772–1782, 2004.

[13] G. Droulers, S. Ecoffey, M. Pioro-Ladriere, and D. Drouin, "Quantum cellular automata: design and fabrication with the nanodamascene process," in *Proceedings of the 41st International Conference on Micro- and Nano-Engineering (MNE '15)*, The Hague, The Netherlands, September 2015.

[14] C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON—a simulator for single-electron tunnel devices and circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 9, pp. 937–944, 1997.

[15] G. Droulers, S. Ecoffey, D. Drouin, and M. Pioro-Ladriere, "A manufacturable process for single electron charge detection, a step towards quantum computing," in *Proceedings of the 46th European Solid-State Device Research Conference (ESSDERC '16)*, Lausanne, Switzerland, September 2016.

[16] C. Dubuc, J. Beauvais, and D. Drouin, "A nanodamascene process for advanced single-electron transistor fabrication," *IEEE Transactions on Nanotechnology*, vol. 7, no. 1, pp. 68–73, 2008.

[17] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, 2011.

[18] P. Harvey-Collard, D. Drouin, and M. Pioro-Ladrière, "A silicon nanocrystal tunnel field effect transistor," *Applied Physics Letters*, vol. 104, no. 19, Article ID 193505, 2014.

[19] K. Boucart, A. M. Ionescu, and W. Riess, "A simulation-based study of sensitivity to parameter fluctuations of silicon tunnel FETs," in *Proceedings of the European Solid State Device Research Conference (ESSDERC '10)*, pp. 345–348, Sevilla, Spain, September 2010.

[20] J. Knoch, M. Zhang, S. Mantl, and J. Appenzeller, "On the performance of single-gated ultrathin-body SOI Schottky-barrier MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1669–1674, 2006.

[21] L. Baldi, R. Bez, and G. Sandhu, "Emerging memories," *Solid-State Electronics*, vol. 102, pp. 2–11, 2014.

[22] Y. Ji, J. Hu, and M. Lanza, "A future way of storing information: resistive random access memory," *IEEE Nanotechnology Magazine*, vol. 9, no. 1, pp. 12–17, 2015.

[23] C. Zitlaw, "RRAM in IoT," in *Proceedings of the Flash Memory Summit*, Santa Clara, Calif, USA, 2014.

[24] M. Labalette, S. Ecoffey, and D. Drouin, "Fabrication of nano planar Resistive RAM devices using the nanodamascene process," in *Proceedings of the 17th Canadian Semiconductor Science and Technology Conference (CSSTC '15)*, Québec, Canada, August 2015.

[25] M. Labalette, S. Ecoffey, S. Jeannot, A. Souifi, and D. Drouin, "HfOx complementary resistive switches," in *Proceedings of the IEEE Nanotechnology Materials and Devices Conference (NMDC '16)*, pp. 1–2, Toulouse, France, October 2016.

[26] N. Jouvet, M. A. Bounouar, S. Ecoffey et al., "Recent developments on 3D integration of metallic set onto CMOS process for memory application," *International Journal of Nanoscience*, vol. 11, no. 4, Article ID 1240024, 2012.

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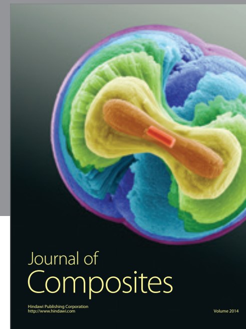
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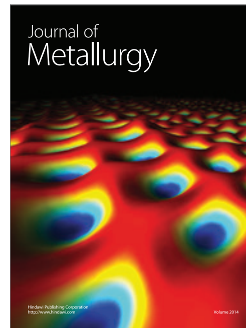
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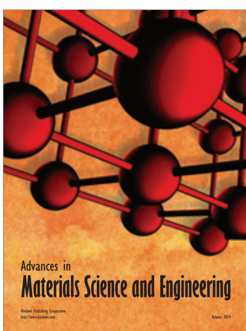
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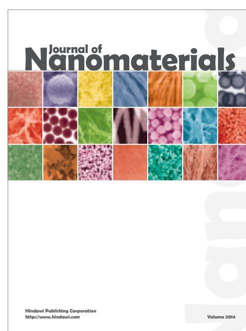
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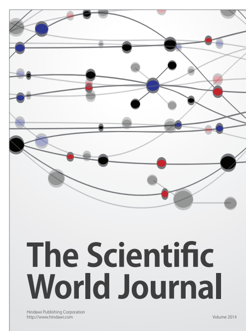
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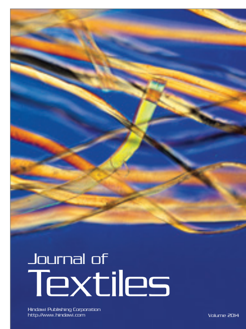
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