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Method for fabricating submicron silicide structures on silicon using a resistless electron beam lithography process

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A novel resistless lithography process using a conventional electron beam system is presented. Metallic lines with widths of less than 50 nm were produced on silicon substrates. The process is based on localized heating with a focused electron beam of thin platinum layers deposited on silicon. It is demonstrated that silicide formation occurs at the Pt-Si interface. By using a dilute solution of *aqua regia*, it is possible to obtain a sufficient difference in etch rates between exposed and unexposed regions of the platinum thin film to selectively remove only the unexposed areas. [S0003-6951(97)q3122-7]

The fabrication of ultra-small scale electronic devices requires efficient high resolution lithography techniques. Much of the work being carried out in fabricating these devices is performed with resist-based lithography processes. Poly(methyl methacrylate) (PMMA) is the most widely used polymer as a resist for electron beam lithography applications.[1,2] This type of lithographic process, however, suffers from several limitations that can become extremely constraining in sub-100 nm device fabrication. These include proximity effects in the resist and resolution limits imposed by the size of the polymer molecules. Proximity effects occur when exposed patterns are within the range of backscattered electrons. These electrons are primary electrons that suffer a high angle collision in the substrate and escape from the surface with a high energy in an area that may be considerably larger than the electron beam diameter. These high energy electrons expose the resist in an undesirable region. Current research efforts in lithography techniques include several resistless processes for defining patterns.[3,4] The process described here is a novel direct write resistless lithography technique for producing metallic structures on a silicon surface with achievable linewidths below 50 nm. The method consists of very localized heating of a thin metal layer deposited on a silicon surface using a focused electron beam. The metal must be able to react with silicon to form a silicon compound (silicide).

The formation of a silicide layer is usually carried out by annealing samples of thin metal layers on silicon substrates in a conventional furnace with a controlled atmosphere of N_2-H_2. This technique of annealing needs several minutes to convert the metal film into silicide.[5–8] New techniques involving rapid thermal annealing (RTA) improve the process of silicide formation. RTA silicide films are significantly better than those formed by conventional annealing[9] due to a shorter processing time.[10] More recently, several techniques of silicide formation have arisen. These processes involve heating of metal-silicon interfaces with photons, electrons and ion beams.[11–13] The main thrust of all these methods is to form the silicide with localized heating near the interface. But none of these techniques is intended as a lithography process, since heating occurs over the entire surface of the sample.

Details of the method presented here will emphasize the particular case of platinum silicide. The activation energy to first form Pt_2Si is around 1.4 eV and the temperature range for complete transformation of Pt into Pt_2Si is from 200 to 350 °C.[14] The growth of PtSi takes place only when all the Pt is transformed into Pt_2Si, the activation energy in this case is increased to 1.6 eV and the range of temperature formation is 300–450 °C.[15] It is possible to reach this temperature range using a standard (SEM) system.

Platinum layers of several thicknesses (20 nm–50 nm) were evaporated onto clean n-type high resistivity silicon ⟨100⟩ substrates using an electron gun deposition system with an evaporation rate of 0.5 nm/s.[16] The electron beam lithography system consists of a JEOL JSM-6300 SEM equipped with a tungsten filament and a beam blanker that is controlled with the NPGS[17] lithography software. Exposures were carried out at several low energies (1 keV–3 keV) and the unexposed platinum was removed from the silicon surface using an *aqua regia* solution of H_2O:HCl:HNO_3=8:7:1. An etch time of 4 minutes was used. The difference in etch rates for the unexposed Pt and the silicide is sufficient for obtaining a selective etch. However, prolonged etching may remove the silicide structures.

Figure 1a shows an Auger electron spectroscopy (AES) depth profile of a 50 nm Pt thin film as deposited. As ex-

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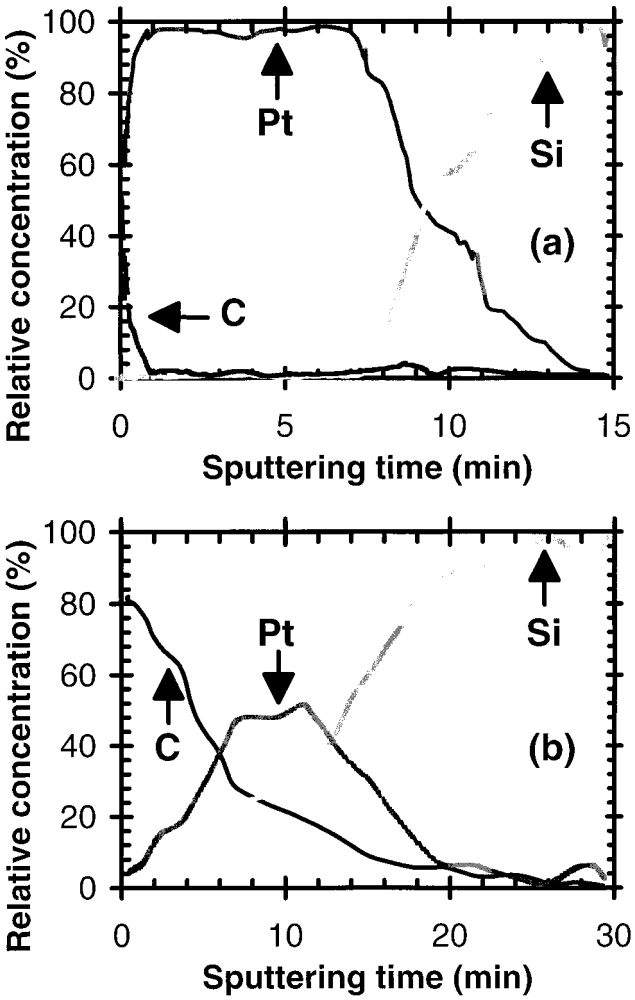

FIG. 1. Auger electron spectroscopy depth profile of 50 nm of Pt on a silicon substrate. (a) As deposited and (b) annealed with the electron beam.

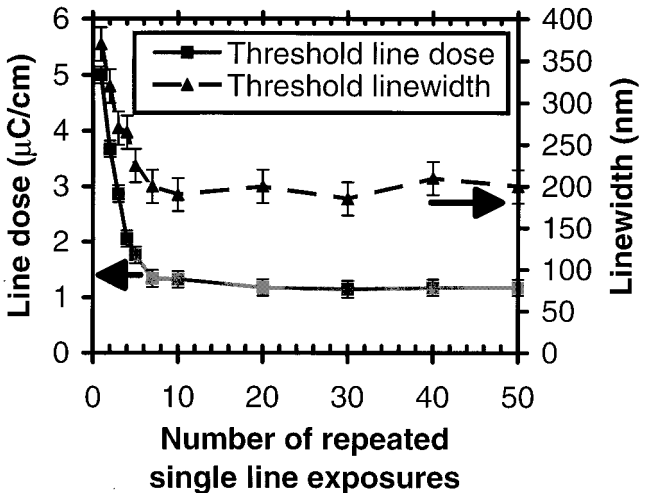

FIG. 2. Threshold line dose and linewidth vs the number of repeated single line exposures.

pected, a smooth transition from the deposited layer to the substrate can be observed. In Figure 2b, the analyzed sample consists of a $20\mu m \times 20\mu m$ structure exposed with the electron beam. The line dose used to produce the square was 17 μC/cm. The surface of the sample is contaminated with carbon which originates in the SEM chamber. A plateau can be observed corresponding to a Pt_2Si region. From this spectrum it is clear that the heating effect of the focused electron beam is sufficient to enable the diffusion of silicon through the metal layer[18] and form platinum silicide which has a slower etch rate than pure Pt. This difference in etch rates provides a means by which to pattern the metal layer with submicron resolution.

The formation of the silicide depends on several factors. The thickness of the deposited metal layer determines the values of the electron accelerating voltage to be used. Better results have been observed when the maximum dissipated energy of the electrons occurs in the metal layer near the junction with silicon. Another important factor that determines the temperature rise is the current density. Experiments have been carried out with a tungsten filament and the current density is approximately 100 mA/cm^2 for a 1 keV electron beam.[19] This value decreases slightly for currents less than 100 pA. Also, the current density increases with the electron beam energy due to the smaller probe size. A higher current density increases the heating at the interface. The last parameter that influences the silicide formation is the electron beam exposure time or the line dose. A threshold line dose is required to form the silicide; when the exposure is less than the threshold value, the pattern will not resist the wet etching.

Figure 2 shows the threshold line dose versus the number of repeated single line exposures. The experimental parameters are as follows: 1 keV electron beam, 100 pA current and a 20 nm Pt film. We obtain the threshold line dose from the minimum total exposure required to form a continuous silicide line after etching. In order to reduce the carbon contamination and the local charging effects, the complete dose was achieved by multiple line exposures. The effect of carbon contamination is to absorb some of the electron energy, thus reducing the amount of energy lost in the metal layer and decreasing the temperature rise. This technique of multiple exposure reduces the total line dose required for threshold by reducing the rate of carbon deposition.[20] From Figure 2 it is seen that the total minimum dose is around 1.2 μC/cm and is obtained with more that seven exposures. Multiple repetition also significantly decreases the linewidth at the threshold. For a given line dose, multiple repetition implies a series of shorter exposure times for the pattern. In this case, the temperature required for silicide formation may only be attained in the center of the beam due to its gaussian profile, thus creating the silicide in a region that is narrower than the beam diameter. When using a 3 keV electron beam under the same conditions, the undesirable effect of carbon contamination should be reduced. Carbon deposition is still present, but at 3 keV the energy loss by the primary electrons in the carbon layer will be less significant. This implies a reduction in the number of multiple exposures required to obtain the threshold dose.

As an example, Figure 3 shows a nanostructure fabricated with this technique. The letters are about 1 μm in height and some lines have widths of less than 50 nm. The experimental conditions used in this case are 100 pA electron beam ($\approx$200 mA/cm^2), 1.5 μC/cm dose and 3 keV accelerating voltage.

After wet etching, the unexposed area may still be con-

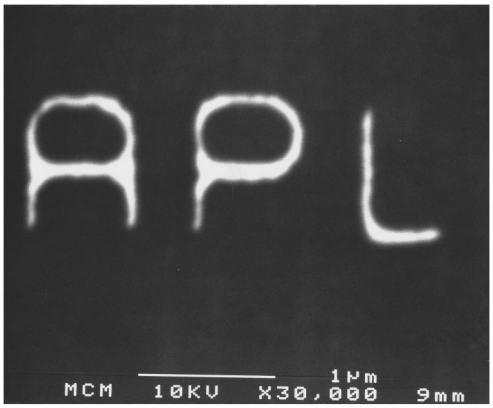

FIG. 3. SEM micrograph of a microstructure.

taminated with Pt. In fact, the first few nanometers of evaporated Pt can react with silicon at room temperature to form a silicide of about 2 nm (Ref. 21) in thickness, thereby decreasing the surface resistivity of the silicon. The surface resistivity in the unexposed area was restored to its original value by using a second etch step consisting of 6 minutes in H_2O:HNO_3:HF=50:49:1. Also, to remove the surface carbon contamination due to the prolonged beam exposure in the SEM chamber, the surface can be exposed to an oxygen plasma etch for 20 minutes.

Proximity effects are reduced dramatically with this method. In fact, proximity effects with this process were observed only within the range of the electron beam diameter. So, by using a high performance SEM (for example a field emission gun), the beam diameter will be reduced and the current density will be increased. A finer structure with relatively insignificant proximity effects will then be achievable using an even smaller line dose.

A second important point to note is that no liftoff is required here unlike the case of resist-based processes. Such lift-off processes can significantly reduce resolution and reduce the yield.

In summary, we have presented here a novel resistless fabrication technique to produce sub-50 nm metallic lines for use as thin conducting structures or even as etching masks on silicon substrates. This process should reduce the proximity effects present in resist-based lithography, and while the resolution limit has not been determined clearly, it should be superior to the 50 nm linewidth obtained using a tungsten filament SEM.

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