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Single-electron transistors with wide operating temperature range

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Single-electron transistors are fabricated with a planar self-aligned process using chemical mechanical polishing. The method is demonstrated with Ti/TiO_x junctions and resistless lithography. The device characterization showed Coulomb blockade up to 433 K. High temperature data allowed one to calculate the impact of the process variations on the charging energy and thus on a realistic operating temperature. It is found that single electron devices can have an operating temperature range similar to conventional silicon transistors, opening the door to hybrid designs. These approaches are promising because advanced functionality is created by an optimal combination of both technology strengths. © *2007 American Institute of Physics*.
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Single electron transistors (SETs) have been around for more than two decades and their potential as extremely high density devices has already been established as well as their unique characteristics for niche markets.[1,2] The nanometer scale dimensions of these transistors have represented an important fabrication challenge and still remain a major hurdle to their widespread utilization. Room temperature demonstration was an important milestone in SETs history, but it is not clear whether it is a sufficient condition for their integration into advanced applications. Like any other electronic device, SETs need to operate properly over a wide range of conditions. More specifically, SETs require an acceptable operating temperature range that will guarantee a sufficient tolerance to normal fabrication process variations and operational heat dissipation. A wider utilization of SETs also supposes a fabrication process that can be transferred into mass production methods.

Many SET processes compatible with the manufacturing environment were presented over recent years.[3,4] While some exhibited relatively high charging energy, few were characterized above room temperature, providing very little data on SETs actual tolerance for operation in real environment. Hybrid approaches,[5,6] where SETs and conventional silicon field effect transistors (Si-FETs) are used in combination on the same substrate, are attractive because these circuits can take advantage of both device's strengths to create advanced functionality. Again, this approach requires SETs with an operational temperature range similar to Si-FETs which has not been specifically demonstrated in previous work.

Here we present a SET concept and its related fabrication that was used to produce devices with a wide temperature range. It is based on a damascene approach using electron beam lithography (EBL) and chemical mechanical polishing (CMP), both technologies which are already in use in the manufacturing environment. The fabricated prototypes have sufficient built-in tolerance to sustain fabrication process variations and still function within a temperature range similar to other conventional devices such as Si-FETs. A very unique tunnel junction creation method is used to control exactly the dielectric thickness and the junction locations. The demonstration is made with metallic SETs using the Ti/TiO_x system at the junctions.

The fabrication process begins with high resolution patterning of a silicon wafer coated with a thermally grown SiO_2 layer. We have selected an EBL process that does not use organic resist for patterning. Inorganic layers such as SiO_2 are good candidates for sub-10 nm imaging[7] and simplify the CMP process. The electron beam directly irradiates the SiO_2 layer, modifying its density[8] and, as a consequence, its etch rate in a dilute acid solution. The irradiated areas etch faster than the background, leading to trench formation. The trenches are not designed to reach the silicon substrate and the underlying oxide ensures electrical isolation from the substrate. When this isolation layer is reduced to a few tens of nanometers in thickness, it can also be used as a back-gate dielectric layer. The shape of the device after this step is a narrow trench in the oxide less than 15 nm wide by 25 nm deep, as shown in Fig. 1(a). The depth of the trench is entirely controlled by the lithography exposure dose and can be precisely adjusted according to design needs.

Figure 1(b) shows how the SET island is created by patterning a Ti line perpendicular to the oxide trench. The line is oxidized in pure oxygen to grow 2 to 12 nm of TiO_x depending on oxidation time and temperature. This TiO_x on the Ti line sidewalls constitutes the tunnel junction dielectric layer. The width of the Ti line will determine the length of the SET island and contributes to its self-capacitance. This line can be patterned with reduced resolution requirements without compromising the total SET capacitance C_T, which must meet the subattofarad target required for wide range temperature operation. This relaxation of the resolution requirement is due to the fact that the tunnel junction capacitances of this process are extremely small as a result of the self-aligned fabrication technique. This represents a key element of this SET concept. In this work, EBL combined with a lift-off technique was used for patterning the Ti lines, with a resolution ranging from 50 to 75 nm.

In the last process step, a Ti layer called the blanket layer is deposited over the entire device area, as shown in Fig. 1(c). The substrate is fixed to a polishing jig and put face down on a turning polishing pad for chemical mechanical polishing. This planarization process will eliminate all material located above the surface of the thermally grown SiO_2

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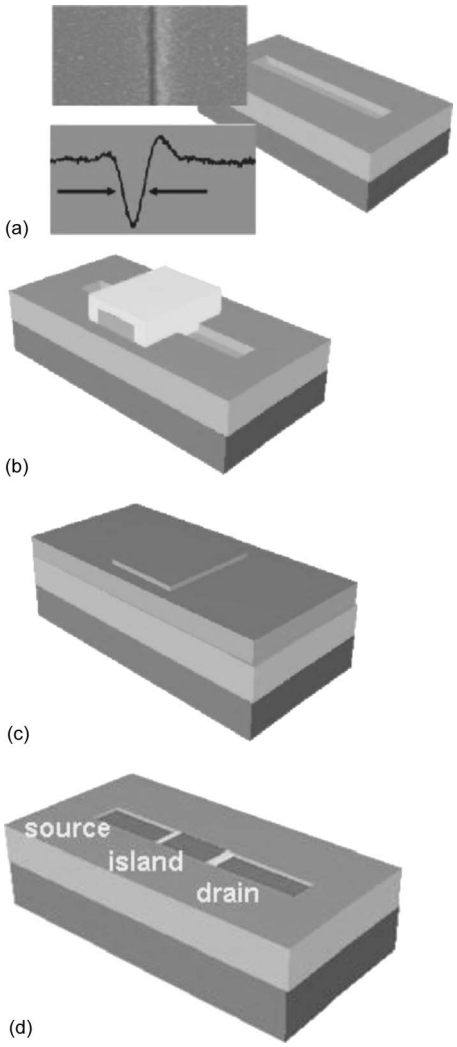

FIG. 1. Wide temperature SETs process overview. (a) View of the trench in the oxide layer and its top down SEM picture including the intensity profile showing where the linewidth is measured. Below the oxide layer is the silicon substrate used as a back gate. (b) The island formation. The open end drawing of the perpendicular Ti line shows the TiO_x layer grown on the future island. (c) The titanium blanket layer is deposited. (d) End result after CMP.

layer. The top of the island is thus removed but its TiO_x sidewalls continue to isolate it from the rest of the thin line, which is now embedded in the SiO_2. The end result is presented in Fig. 1(d). The CMP process is stopped when test structures placed next to the SETs begin to disappear. This is because they intentionally received a lower exposure dose and are thus a few nanometers shallower that the SETs trench. We are investigating the use of stopping layers to improve the polishing accuracy, but with the current method, this optical end point strategy was quite easy to detect and control. The CMP process leads to the simultaneous formation of the source, drain, and island of the SETs with a thickness of only 2– 3 nm. Depending on the specific design of the devices, larger source and drain electrodes can then be deposited to facilitate the electrical characterization of the SETs.

The source-drain current I_{DS} measured at room temperature is presented in Fig. 2(a) for two different back-gate bias values turning the device on and off. The inset of Fig. 2(a) shows the SET characteristics under a wider V_{DS} range. The behavior of the I_{DS}-V_{DS} curves is strongly nonlinear for both

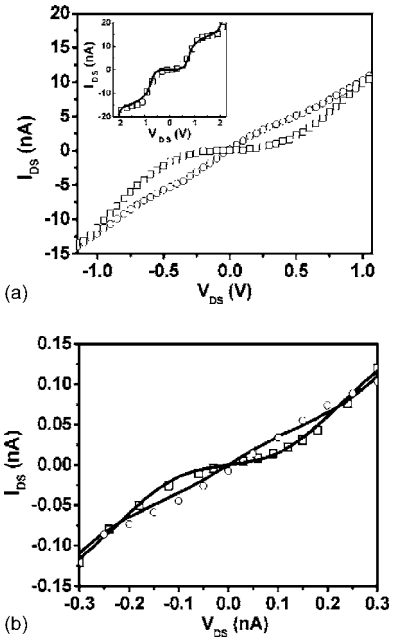

FIG. 2. Electrical characterization at room temperature. (a) Asymmetrical SET data with V_{GS} at 0 V (□) and at 0.3 V (○). The inset shows a wider V_{DS} range (□). The line represents the model calculations with $C_S=C_D=0.06$ aF, $R_S=1.7\times10^7$ Ω, $R_D=3.5\times10^6$ Ω, and $C_{GS}=0.23$ aF. (b) Symmetrical SET data with tunnel junction dielectric thickness of 12 nm for V_{GS} at 0 V (□) and at 0.3 V (○). The line represents the model calculation with $C_S=C_D=0.05$ aF, $R_S=6.3\times10^8$ Ω, $R_D=8.9\times10^8$ Ω, and $C_{GS}=0.3$ aF.

symmetrical and asymmetrical transistors with relatively high current drive in the nanoampere range. The asymmetrical case is a design with SET neighboring features that create localized uneven polishing, resulting in rounding of one of the junctions and thus in conductance differences. Other I_{DS}-V_{DS} curves were obtained on a symmetrical layout and one example is presented in Fig. 2(b). We also scanned the back-gate bias and observed a transistor effect. The drain current is modulated by the back-gate voltage and showed regular oscillations, as presented in Fig. 3. We have observed a back-gate leakage through the backside oxide on the samples with sub-100 nm thickness. The leakage is a back gate to source current of about 100 pA/V_{GS} and occurred after several temperature cycling tests. Metallic SETs are known to be surprisingly well described within a certain size range by a set of basic rules called the orthodox theory.[9,10] To model the devices at room temperature, we have used Monte Carlo simulations within this framework with capacitance

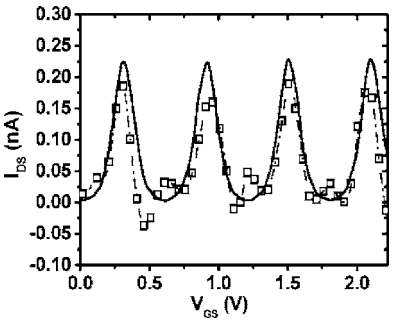

FIG. 3. SET drain current behavior as a function of the back-gate bias at low drain voltage (25 mV). The line is the asymmetrical SET model and the squares (□) are the data. A dotted line is added as a guide to the eye. A gate to source leakage to of 100 pA/V_{GS} was removed from the data to represent it on the same scale as the model.

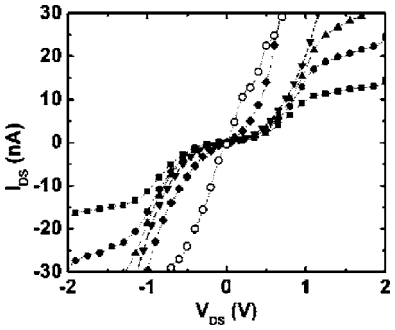

FIG. 4. SET curves as a function of temperature for the design with the charging energy of 457 meV. Temperatures are 296 K (■), 316 K (●), 336 K (▲), 386 K (▼), and 433 K (♦). The back gate is grounded except for the open circles where V_{GS} is 0.3 V at 433 K.

and resistance values close to what is expected from the geometry of the devices. The dimensions were extracted from measurements using a scanning electron microscope (SEM) and the oxide thickness was verified by ellipsometry. In the case of the asymmetrical transistor of Fig. 2(a), the junction dimensions were 10 nm wide by 2 nm thick with an 8 nm layer of TiO_x grown at low temperature. The dielectric constant of 3.5 of the titanium oxide was extracted from junction current curves as a function of electric field and temperature. This value is typical of an amorphous TiO_x thin film.[11,12] With a parallel plate model we evaluated the gate capacitance at 2.3×10^{-19} F and the source and drain capacitances at 7.7×10^{-20} F. Considering the relative measurement error of the SEM at this small size scale, these values are in good agreement with the model values which are 2.3×10^{-19} F for the gate capacitance and 6.0×10^{-20} F for the source and drain capacitances. These results confirmed that this self-aligned junction fabrication process is capable of subattofarad resolution. We have explored many scenarios and combinations of possible unexpected multiple junctions and conductance but none of them could explain our data other than Coulomb blockade arising from standard SET formation. With this model, we have estimated our charging energy at 457 meV.

The I_{DS}-V_{DS} curve was then characterized as a function of temperature and is presented in Fig. 4. Measurements on the design with the highest charging energy were made up to the limit of the experimental setup at 433 K and the nonlinearity attributed earlier to Coulomb blockade was still being observed. This is because the charging energy E_C of 457 meV is still more than 12 times the value of thermal fluctuations at 433 K. Taking this same factor of 12 as a criterion for an initial approximation, one finds that even if some fabrication steps deviate from nominal values and reduce E_C by 25% to 343 meV, Coulomb blockade could still be observable up to around 330 K. This temperature reaches the upper specification limit of normal operation of many Si-FETs processes. It is then clear in this case that the SET operating temperature alone is not the limiting factor in hybrid design fabrication. This conclusion is important for circuit designers because it sets a value above room temperature under which Coulomb blockade can be guaranteed.

The first three designs fabricated with this approach were all functional devices. A larger number of SETs based on this approach will need to be fabricated in order to evaluate the complete yield and repeatability of the process. Nevertheless, as an initial step, we have demonstrated the proof of concept of this method. Getting high temperature data gave us a valuable insight on how SETs evolve above room temperature and what kind of process tolerances will be required to establish hybrid circuit fabrication. We also believe that this device platform might have some use to study and validate concepts of single charge tunneling theory at very high temperature.

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[1] K. Likharev, Proc. IEEE **87**, 606 (1999).
[2] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa, J. Phys.: Condens. Matter **14**, R995 (2002).
[3] K. Miyaji, M. Saitoh, and T. Hiramoto, Appl. Phys. Lett. **88**, 143505 (2006).
[4] Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K. Murase, IEEE Trans. Electron Devices **47**, 147 (2000).
[5] A. Toriumi, K. Uchida, R. Ohba, and J. Koga, Physica B **272**, 522 (1999).
[6] K. S. Park, S.-J. Kim, I.-B. Baek, W.-H. Lee, J.-S. Kang, Y.-B. Jo, S. D. Lee, C.-K. Lee, J.-B. Choi, J.-H. Kim, K.-H. Park, W.-J. Cho, M.-G. Jang, and S.-J. Lee, IEEE Trans. Nanotechnol. **4**, 242 (2005).
[7] P. Xiaodan and A. Broers, J. Appl. Phys. **71**, 6189 (1992).
[8] J. R. Barnes, A. C. F. Hoole, M. P. Murrell, M. E. Welland, A. N. Broers, J. P. Bourgoin, H. Biebuyck, M. B. Johnson, and B. Michel, Appl. Phys. Lett. **67**, 1538 (1995).
[9] D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, edited by B. Altshuler, P. Lee, and R. Webb (Elsevier, Amsterdam, 1991), pp. 173–271.
[10] G. L. Ingold and Y. V. Nazarov, in *Single Charge Tunneling*, edited by H. Grabet and M. H. Devoret (Plenum, New York, 1992), pp. 21–108.
[11] K. Matsumoto, M. Ishii, J.-I. Shirakashi, K. Segawa, Y. Oka, B. J. Vartanian, and J. S. Harris, Tech. Dig. - Int. Electron Devices Meet. **1995**, 363.
[12] F.-C. Chiu, S.-K. Fan, K.-C. Tai, J. Y. Lee, and Y.-C. Chou, Appl. Phys. Lett. **87**, 243506 (2005).