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Conception, fabrication et caractérisation de diodes Schottky planaires terahertz

Design, Fabrication and Characterization of Terahertz Planar Schottky Diode

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RÉSUMÉ

Dans cette thèse, les diodes Schottky pour des applications en ondes millimétriques et aux fréquences térahertz sont étudiées. Une méthodologie de conception et d'optimisation est proposée pour améliorer la performance de telles diodes. La conception et les simulations sont effectuées à l'aide d'un programme basé sur un modèle analytique. Les différentes méthodes de calcul de la fréquence de coupure de la diode sont définies, étudiées et classifiées selon les applications potentielles. En utilisant un modèle de diode générique et général, une nouvelle approche pour calculer la fréquence de coupure est suggérée pour les applications de mélangeur / multiplicateur. Cette approche permet d'évaluer la tension seuil avec une précision beaucoup plus grande et proche de la réalité. En outre, la conception d'une diode Schottky en tenant compte dès le départ l'application visée (détecteur direct, mélangeur ou multiplicateur) est étudiée. Cette thèse montre que l'ingénierie de la structure épitaxiale a un impact important lorsque l'on utilise une conception de diode basée sur l'application finale comme proposée. Un procédé de microfabrication a été entièrement développé et caractérisé. Une méthode de planarisation unique est introduite pour permettre de connecter la diode par des ponts à air en minimisant les effets parasites. Afin d'éviter une coûteuse lithographie par faisceau électronique, une anode en forme de T est produite en utilisant une technique de photolithographie. Ce procédé est fiable et répétitif, est de faible coût et offre une grande souplesse en matière de conception en plus de répondre au besoin d'une production de masse, pour laquelle la lithographie par faisceau d'électrons n'est guère possible. Le procédé final nécessite simplement deux étapes de métallisation, nombre minimal possible que nous avons atteint. En raison des exigences de recuit du contact ohmique, il est impossible d'avoir moins de deux étapes de métallisation. Le processus de planarisation proposé repose sur l'utilisation de différents taux de gravure plasma de deux résines couramment utilisées. Pour les travaux réalisés dans cette thèse, une épitaxie GaAs HBT disponible au sein du laboratoire a été utilisée. Les résultats de caractérisation de diodes réalisés dérivés des mesures DC et RF sont rapportés et comparés avec les résultats de la simulation. Les résultats de mesure montrent une réduction significative de la capacité parasite de la diode à moins de 20% de sa capacité totale. Par conséquent, le procédé de conception et de fabrication de ce travail peut fournir des diodes qui

peuvent fonctionner au-delà du térahertz avec des dimensions pour l’anode plus grandes que les diodes trouvées dans la littérature et qui peuvent donc être fabriquées uniquement par des techniques de photolithographie optique.

Abstract

In this thesis, Schottky diodes for millimeter waves and terahertz application are scrutinized. A design and optimization methodology is proposed to improve the diode performance. Design and simulations are performed by using an analytical model based code. Diode cut-off frequency calculation methods are studied and classified for different applications. Considering general diode equivalent circuit model, a new approach for calculating the cut-off frequency is suggested for mixer/multiplier applications. This approach provides cut-off much closer to its practical value. Also, the diode design based on its application, direct detector and mixer/multiplier, is studied. It is shown that the epitaxial structure engineering has impact on diode application based design. For diode realization a microfabrication process is developed. Unique planarization method is introduced which provides necessary substruction for the airbridges. In order to avoid expensive e-beam lithography, a T-shaped anode is produced by employing photolithography technique. This process is repeatable, reliable, low cost, gives high flexibility in design terms, and suitable for mass production. The final process merely requires two metallization steps which is minimum possible number due to annealing requirement of ohmic contact. The proposed planarization process is based on using different plasma etching rates of two common resists. In the diode fabrication an available GaAs HBT epitaxial wafer is used. The realized diode characterization results derived from DC and RF measurements are reported and compared with the simulation results. The measurement results showed significant reduction in parasitic capacitance of the diode to under twenty percent of its total capacitance. Therefore, the design and fabrication method of this work can provide diodes to operate over one terahertz with larger anode area (that can be produced by photolithography techniques).

To my beloved mother, brother, and my love Ali,

And to the memory of my father

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1 Introduction

1.1 Terahertz gap

Terahertz (THz) is an electromagnetic spectrum that lies between microwave and infrared frequencies. This frequency band does not have unique definition. However, many references are considering it as the spectrum between100 GHz (0.1 THz) and 30 THz. A variety of novel applications have been introduced within this spectrum, inspired by optical and microwave technologies, and advances in micro- and nano-fabrication techniques, [1].

Due to existence of molecular resonances and other physical phenomena in THz band, many applications can leverage such properties. At the same time, it is the least explored part of the spectrum (hence a so-called “THz gap” [2]), due to the lack of efficient active and passive components. More precisely, there is currently no low-cost, compact and efficient sources and detectors [3], [4]. Nevertheless, thanks to the enormous research efforts, performed during the past decades, the size of the gap has been diminished. The first practical solution for using THz band was generating and detecting of pulsed THz waves by femtosecond-pulse lasers in the early 1990s [5]. Later in the 2000s by development of THz semiconductor devices a new chapter in this technology has been opened and fueled many interesting applications.

1.2 Terahertz applications

The THz range became a hot topic during the past decades due to several interesting potential applications, such as a high data rate short-range communication, spectroscopy, biology (disease detection, e.g. cancer), astronomy, imaging, security, terrain mapping, and environmental studies [6].

Spectroscopy is one of the main applications of THz waves because of the spectral signature molecules, especially the organics and biologicals, in this region. THz radiation can transmit through opaque materials while it excites their molecular resonance and it is sensitive to bonding of atoms. Materials can be categorized into three categories according to their behaviors when they are exposed to THz radiation. Metals are highly reflective, polar materials (water) are highly

absorptive, and nonpolar and nonmetallic material such as plastic, wood, paper, and fabrics which are opaque to the optical frequencies, are transparent to the THz frequencies [2]. This make this region of spectrum ideal for imaging applications. Figure 1-1 shows an integrated circuit (IC) image with visible light and THz imaging. The metal circuit and the semiconductor wafer inside the IC package are visible to THz waves [4]. Moreover, the THz gap is a free frequency band for high data rate communications. The demand for bandwidth in wireless communications has doubled every 18 months for the past 25 years [7]. Thus, moving to higher frequencies to have wider bandwidth is inevitable. A fully integrated THz system can facilitate the path toward the next generation of telecommunication systems.

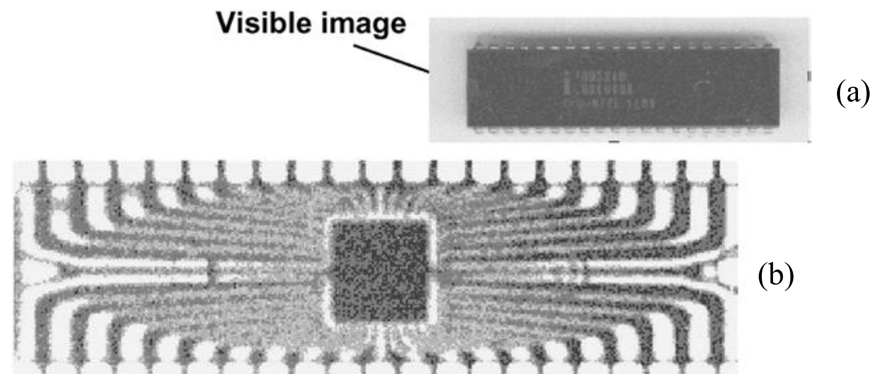


Figure 1-1 Image of an IC using (a) visible light and (b) with THz imaging. The IC black epoxy package [4].

1.3 Terahertz devices

THz circuits consists of different active (e.g. diodes and transistors) and passive (e.g. waveguides, antennas, and filters) elements. Many researches have been dedicated to provide a compact, efficient and low-cost materials and solutions to overcome the lack of THz components. For instance, considering waveguides, various structures made of either metallic or dielectric materials have been proposed in the literature [8]–[10]. Metallic waveguides suffer from metallic losses of metal parts while dielectric waveguides suffer from radiation and dielectric losses. Although planar structures are more lossy, they are more attractive since they are able to be integrated with other active components.

THz detection and generation is the most important and challenging part of THz systems. Detectors and sources could come from microwave-electronic devices, optical approaches or a combination of both [11]. However, for the THz region, RF detectors demonstrated superior performance compared to their optical counterparts [12]. THz detectors can be divided into incoherent (direct) and coherent (mixing) categories [13]. A simple schematic of both direct and mixing detection approaches is shown in Figure 1-2. Bolometers and pyroelectric crystals fall into the direct category, however, they are slow and perform only in low temperatures. Coherent detectors include nonlinear optical crystals, photoconductive antennas [14], hot electron bolometers (HEBs), superconducting tunnel junctions (STJs), superconductor-isolator-superconductor (SIS) tunnel junctions, tunneling quantum dot inter-sublevel photo-detectors (T-QDIPs), and Schottky diodes. STJs, SISs, HEBs, and T-QDIPs are cryogenic detectors while the others can function on room temperature.

A bolometer is a thermal detector that includes a temperature-dependent resistance and two metallic contacts. The resistive element is made of a very low thermal capacity and high temperature coefficient material that can provide a large resistance variation according to the input signal [3]. High mobility semiconductors with temperature sensitivity or superconductor can be used for THz bolometers at cryogenic temperatures.

The high electron mobility transistors (HEMTs) lately become very interesting in THz region especially for detection and generation. These structures naturally promoting emission and detection of THz waves, due to its two-dimensional (2D) Plasmon in hetero-structure semiconductor that provide a channel with high mobility and low resistivity [15]–[22].

Between all technologies used for THz detection and generation, the suitable technology should be chosen base on project requirements, application, budget, and available fabrication facilities. Some of the noted technologies are cryogenic and require a low temperature system; others are limited by the size of the device or designed just for pulse operation. Schottky diodes are compatible with pulsed and continuous signals and can operate at room temperature. The GaAs Schottky diode provides high sensitivity, large instantaneous bandwidth, and large spectral resolution [23]. Hence, Schottky diode technology was selected for this thesis.

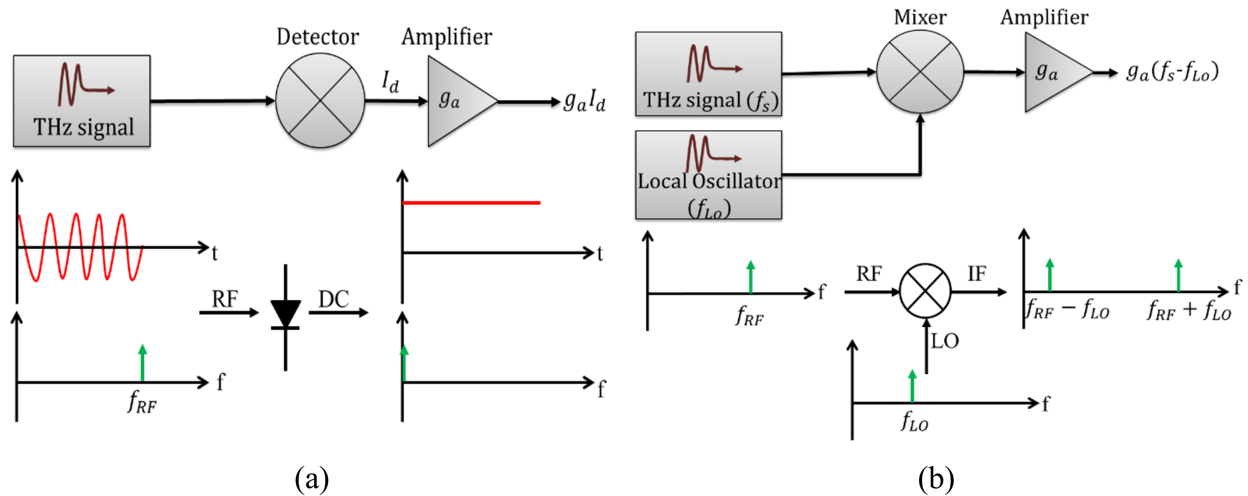


Figure 1-2 Schematic of different detector types. (a) Direct detection. (b) Mixing detection.

1.4 Schottky diode for THz applications

The Schottky diodes have been employed in different application in THz systems (e.g. sources, detectors, mixers, and phase-shifters) [24]–[27]. Different properties of diodes are leveraged according to the application that they are used for. In detection systems, diodes are used as a rectifier (direct detection) where the nonlinear resistive element of diode and its current value are the key elements. However, in the heterodyne detectors and sources where the diode is used as a mixer and multiplier, the key element is the diode nonlinear capacitance. Therefore, the diode application should be considered in design and performance study. Moreover, at design stage, considering application will result in better optimization of the diode. So far, several research dedicated to study the diodes in terms of equivalent circuit, design, structure, fabrication, frequency performance, efficiency, temperature noise, and parasitic effects [28]–[35]. Nevertheless, the application based study of the diode and its effect on the design and optimization is missed. In this work, an application based studies of diode and comparison of its performance in different applications is reported. The design and optimization of the diode by considering its application are proposed. Also, comprehensive studies of the diode frequency behavior for each application categories are presented. The diode frequency behavior is characterized by the cut-off frequency, which is defined by the power portion of the used nonlinear element of the diode. Since, in each category the used nonlinear element is different, the cut-off frequency and its formulation

should be defined based on the application. In the presented cut-off frequencies formulation, the effect of all circuit elements of the diode is considered.

In this thesis, a THz Schottky diode is developed to be used in integrated circuits operating at room temperature and able to work with pulse or continuous signals. The developed diode in this work has a lower parasitic capacitance that improves the cut-off frequency. Also, the lack of effective fabrication process for the diode mass production encouraged us to develop a low-cost, reliable, repeatable and flexible fabrication process. GaAs is selected as the semiconductor host because it has high sensitivity, large bandwidth, and spectral resolution. GaAs is one of the best choices among the semiconductors for the THz frequency, due to the high saturated electron velocity and electron mobility. It has lower parasitic resistivity and lower noise. Moreover, GaAs devices are less sensitive to own heating due to their wide energy band-gap. On the other hand pure GaAs has high resistivity and high dielectric constant which provides very good isolation when it is used as a substrate at high frequencies.

1.5 Thesis outline

This thesis includes six chapters. In Chapter 2, the Schottky diode definition, structure, history, applications in THz frequencies, and the state of the art are discussed. The design process, simulation, and analytical studies of the diode are presented in chapter 3. Also in chapter 3, different approaches for studying the diode performance are discussed and a new, more accurate approach is suggested. The epitaxy structure engineering for the diode which depends on the diode application and the unique fabrication process that is developed for realization of the diodes is described in chapter 4. Moreover, the mask design, details of the fabrication process and challenges faced during the process development are described in chapter 4. In chapter 5, the characterization and measurement results, setups, procedures, and parameter extraction methods used for the characterization of diode are explained. The conclusion of this work and some suggestions for further research are provided in chapter 6.

2 Literature Review: Toward THz Schottky Diode

2.1 Introduction

In order to achieve practical THz systems at room temperature with reasonable size and cost to meet various application requirements, a versatile, flexible and compact integrated transceiver system is required [36]. The Schottky diode is one of the most useful and popular device for millimetre-wave and THz detection. The planar structure of the diode is very compact, integrable, mechanically stable, and low noise [37]. Therefore, the Schottky diode can be an essential and critical element of THz systems. The diode is based on the metal-semiconductor rectifying system. For the first time, in 1938, Walter Schottky presented a theory that, expresses the capability of raising potential across the semiconductor's barrier, is so-called the Schottky barrier. Meantime, Mott presented another theoretical model for potential across the metal-semiconductor junction which is called the Mott operation [38]. Appendix A presents an overview of Schottky and metal-semiconductor contacts.

2.2 Schottky diode

A Schottky diode is a metal-semiconductor contact in which the work function of the metal is higher than that of the semiconductor ($\phi_m > \phi_s$). In order for the device to be able to pass the current, it needs another connection as second port. Therefore, another metal-semiconductor contact but in Ohmic mode (Appendix A) is required. The device structure is shown in Figure 2-1.

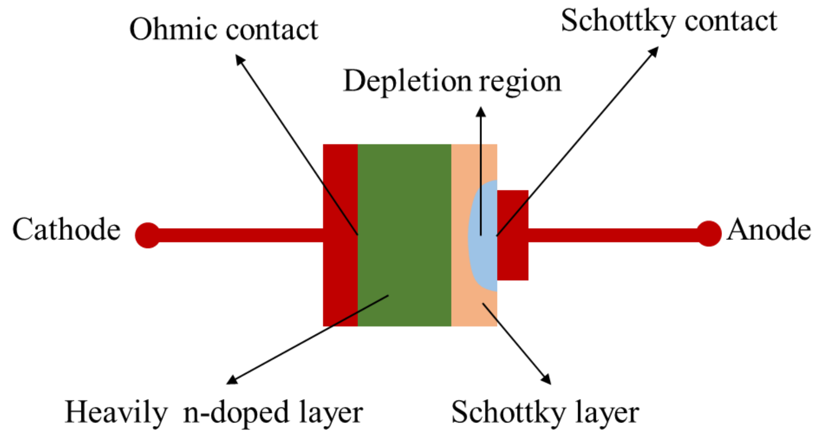


Figure 2-1 The Schottky diode structure.

A general explanation of the metal-semiconductor contacts is given in Appendix A. The heart of the diode is a Schottky mode metal-semiconductor contact. The interface of the semiconductor with metal is depleted due to the difference of the work functions. The depletion region width W_D depends on the junction build-in potential φ_{bi}, the Schottky layer doping level N_D, its permittivity ε_s, and the junction voltage bias V_j;

$$W_D(V_j) = \sqrt{\frac{2\,\varepsilon_s}{q\,N_D}(\varphi_{bi} - V_j)} \tag{2-1}$$

The junction capacitance C_j of this contact is a function of the depletion region width W_D:

$$C_j(V_j) = \frac{A\,\varepsilon_s}{W_D(V_j)} \tag{2-2}$$

where A is the junction area. Therefore, the junction capacitance is a function of voltage bias.

Since the main current transport mechanism of the Schottky diode is thermionic emission, when the positive voltage bias is applied (forward bias regime) the diode current is obtained by:

$$I = I_s(\exp\left(\frac{q\,V_j}{k_B T}\right) - 1) \quad (2\text{-}3)$$

where k_B is Boltzmann's constant, T is the temperature, and I_s is saturation current. That is:

$$I_s = A\,R^* T^2\ \exp\left(-\frac{q\,\varphi_B}{k_B T}\right) \quad (2\text{-}4)$$

where R^* is Richardson's constant. Since the diode also includes a series resistance R_s due to the resistivity of contacts and the current path though the semiconductor (here GaAs), the applied voltage bias V_b and the junction voltage V_j relation is expressed as:

$$V_j = V_b - I\,R_s \quad (2\text{-}5)$$

In this work we developed an analytical model of Schottky diode based on expanded physical behavior analysis as briefly explained above. The diode behavior is simulated and studied by using this developed simulation environment to optimize and characterize the diode barrier, equivalent circuit, and parasitic elements.

In order to develop the Schottky diode for THz applications some improvement (mainly in design process) are required. Modifications such as; using a high mobility semiconductor host, reducing the capacitance of the diode by reducing its anode size, minimizing the parasitic elements, and reducing the system noise.

2.3 Development of the diode structure and technologies

THz Schottky diodes are presented in different configuration such as whisker contact, planar (with surface channels), quasi-vertical (anode and cathode are vertically mounted and has surface channel interconnection), and two dimensional electron gas Schottky layer structure.

2.3.1 Whisker diode

Young and Irvin (1965) proposed the first technique that is used for realization of sub-millimeter (sub-mm) waves and THz Schottky diodes, called a "whisker diode." The technique was based on gently squeezing off a metallic whisker on GaAs epitaxy die which had a large Ohmic contact on the back side of the chip [39]. At the end of 1980 decade, T. Crowe and colleagues at the University of Virginia started working on sub-mm and THz systems based on GaAs Schottky diodes [40]. They have used Young and Irvin's fabrication technology of vertical structure diodes [39]. A cross-sectional view of this diode is shown in Figure 2-2. In order to couple to this diode, they used whisker contact to minimize the diode's additional coupling series resistance and shunt capacitance. The diode with the whisker contact is shown in Figure 2-3. After Young and Irvin, many research teams at the University of Virginia, Bell Labs, MIT, Chalmers, and Texas Instruments tried to improve and optimize design and fabrication technology of epitaxial GaAs Schottky diodes. They studied the effect of electron tunneling across the barrier of the diode current-voltage (I-V) curve [41]. Also, they investigated the diode series resistance behavior as a function of skin effect and plasma resonance [42]. Another researcher studied the source of the noises, such as hot-electron noise, in the diode [43].

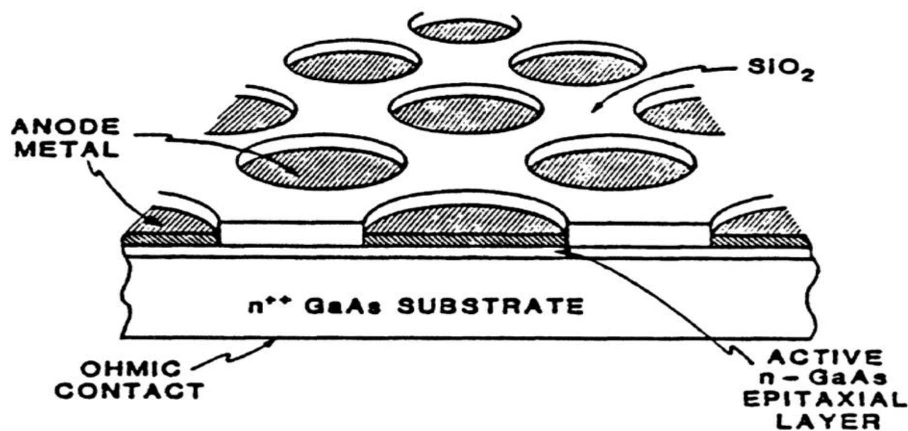


Figure 2-2 Young and Irvin's vertical structure Schottky diode cross-sectional view [40].

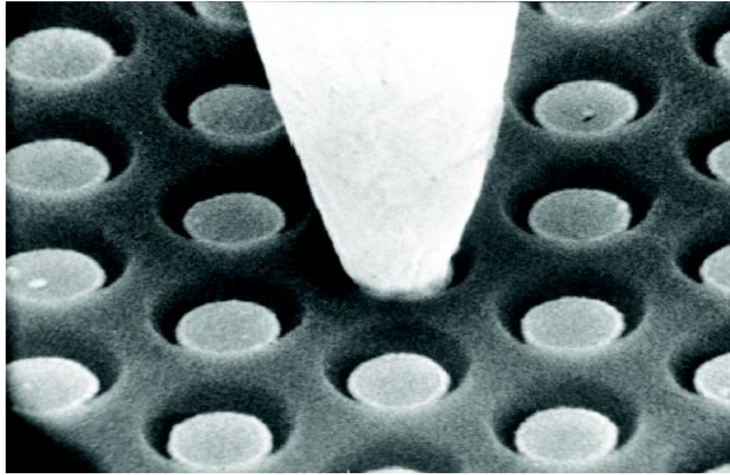


Figure 2-3 SEM image of vertical structure Schottky diode with Whisker contact [44].

2.3.2 Planar structures

In parallel with THz whisker diode development, improvement in micro-fabrication methods and technology enabled reaching new frontiers by:

- reducing the size of the Anode

- controlling doping concentration and thickness of each layer of the epitaxy structure

- air-bridge techniques to reduce the parasitic elements

which improved the diode performance and increased its cut-off frequency. Then, W. Bishop *et al.* (1990) presented the first planar Schottky diode which has attracted much attention [37]. This planar diode was realized by making both contacts on one side of the chip, and employing bridges to connect the anode and cathode to the circuit. Figure 2-4 shows the schematic side view of the proposed diode in [37].The planar structure can work at THz frequencies by using air bridges, which have lower parasitic capacitance. The planar diode is preferred over the whisker design due to its compactness, ease of integration, and mechanical stability. However, due to the whisker diode's vertical structure, the anode placed directly over the backside Ohmic contact has smaller parasitic capacitance and series resistance in comparison to planar structures. The advancement from whisker to a planar device gives freedom to develop integrated circuits based on Schottky

diodes suitable for many applications [27], [45]–[47]. The planar diodes have been realized with different materials and technologies such as CMOS [48], GaAs, and GaN [49]. Epitaxial GaAs Schottky barrier diodes are frequently used in THz heterodyne detectors, mixers, and solid state sources. After the introduction of the planar diodes in [13], many researches focused on improving the diode performances in terms of cut-off frequency, efficiency, responsivity, sensitivity, and device noises. Also, RF losses and thermal heating are discussed in the literature [11], [35]. In [11] the electro-thermal model of the Schottky diode is presented. This model can give the device hot spot temperatures which will be helpful for circuit reliability studies.

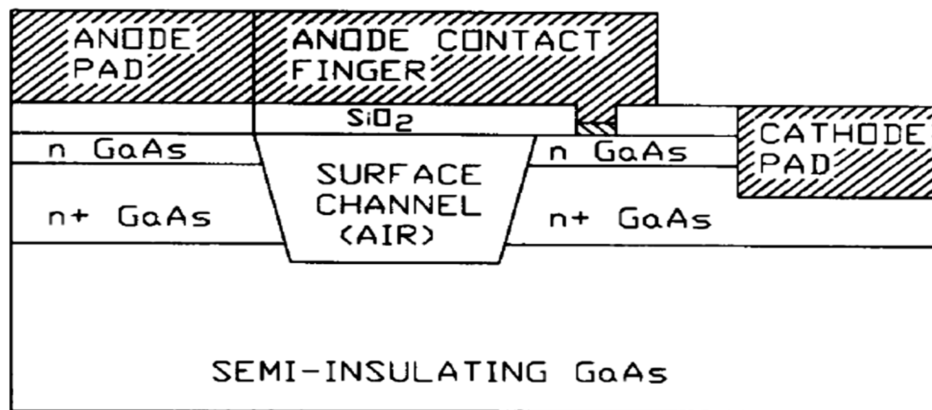


Figure 2-4 Schematic of cross section view of surface channel diode [37]

2.3.3 Quasi-vertical structures

The quasi-vertical is another reported structure, which is combination of the two above structures [50]–[53]. In this structure, the anode and cathode are placed vertically while the structure is planar. The quasi-vertical diode is achieved by making a large ohmic contact (cathode) from the back side below the anode contact while both anode and cathode have access from top side, as shown in Figure 2-5. This structure is easier to integrate than the whisker structure due to surface channel anode access, and also has vertical structure advantages. However, the vertical structure diode has some limitation due to its backside process requirement which add some complexity to the fabrication process.

A quasi-vertical Schottky diode [50] has recently been reported that can be integrated into planar millimeter and submillimeter-wave circuits. The diode structure is based on backside processing and bonding of the diode epitaxy to a host high-resistivity silicon substrate that supports both the vertical diode and its associated circuitry (Figure 2-5).

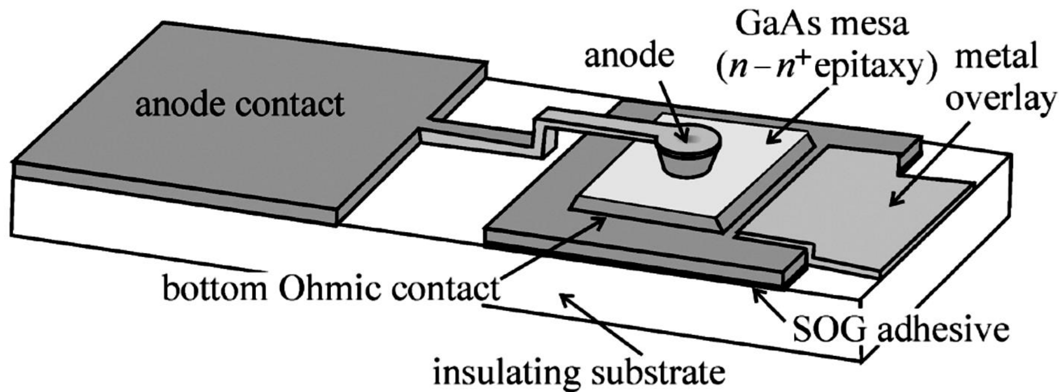


Figure 2-5 Schematic of quasi-vertical diode [50].

2.3.4 2D electron gas Schottky diode

In 1992, W. Peatman at Virginia University proposed a new two-dimensional electron gas (2DEG) based millimeter/sub-millimeter diode for multiplication applications [54]. The Schottky contact was placed along the edge of a 2DEG based on AlGaAs/InGaAs/GaAs heterostructure (geometry of the structure is shown in Figure 2-6). This geometry has the combination of low series resistance and high breakdown voltage. The high breakdown caused by the 2D electric field spreading in the depletion region and the low series resistance is due to the excellent transport properties of the 2DEG. Meanwhile, the electron transit-time of this structure is lower than the conventional Schottky diode due to high electron velocity of the 2DEG. Also, a 2DEG Schottky diode by AlGaN/GaN heterostructure for THz detection is experimentally demonstrated in [49].

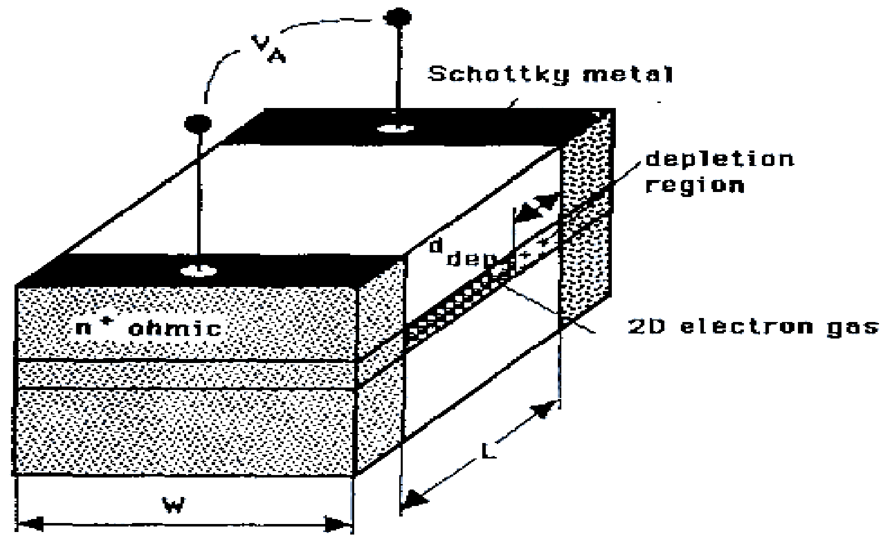


Figure 2-6- Geometry of the 2DEG structured Schottky diode [54].

2.3.5 CMOS technology diode

CMOS technology was also used for realization of the Schottky diode for high frequency applications. The first mmWave Schottky diode frequency doubler fabricated in CMOS was presented in [48]. An array of the diodes shunt connected were implemented in CMOS technology without any process modifications. Due to the shunt array, the series resistance was reduced, which increased the cut-off frequency. In the fabrication of diodes, $CoSi_2$ is used in the interface of metal-semiconductor contact which enhanced the barrier height. The $CoSi_2$-Si diodes on the n- and p-well substrates are fabricated without a guard ring in 130-nm foundry CMOS process. By using these techniques, they reached the highest cut-off frequencies for Schottky diodes fabricated with silicon. This work shows the CMOS technology potential for mmWave and far-infrared detection systems. The idea was used in [55] for an 8x8 parallel Schottky diode in CMOS technology. The proposed diode in [48] was also used in sub-millimeter CMOS integrated circuits and presented in [56] and [57]. A broadband detector for 0.6 to 1 THz using 65 nm CMOS technology and integrated silicon lens for imaging is presented in [58].

According to this summary of the diode structures and technology, the diode has been realized in not integrable whisker contact or integrated planar structure although it sacrifices partly the diode performance due to the higher parasitic elements. However, by developing the micro/nano-fabrication techniques the parasitic problem has been significantly diminished. A mixed structure is called quasi-vertical is developed that has both structures benefits. Also, some other technologies such as 2D electron gas and CMOS are used in the diode design and realization.

2.4 THz Schottky diode applications

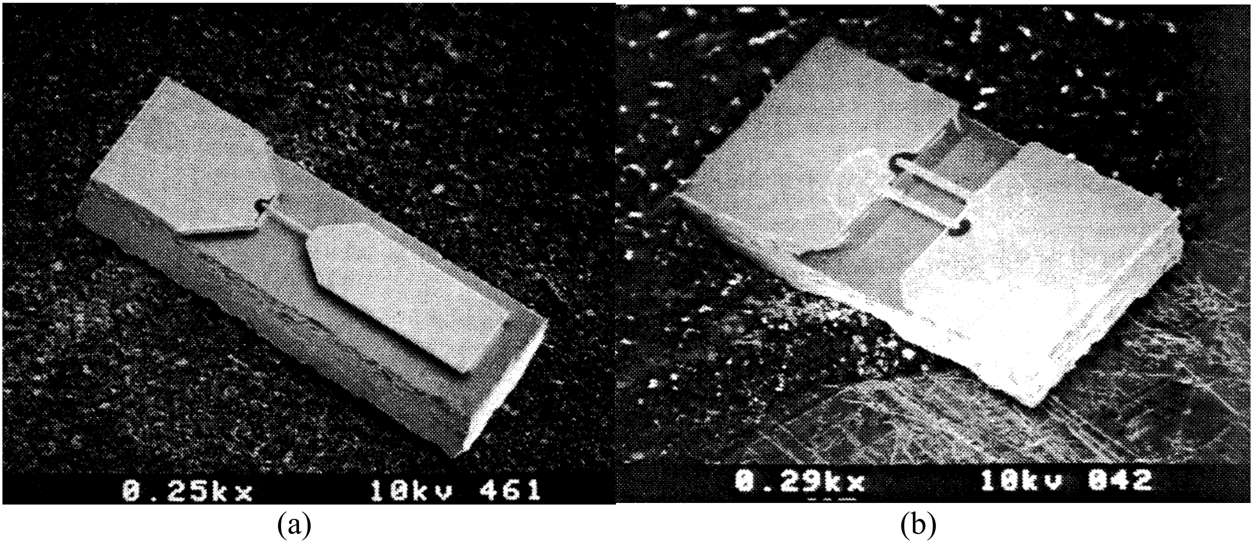
In previous sections, different THz Schottky diode technologies, which have been published in literature, are reviewed. In this thesis, in order to achieve better integration capability, planar structures are considered. Planar configuration are more attractive since they are well-developed for different applications. Also, in most performed researches and investigations, studies were not considering diode's application. Therefore, this thesis is focused on bringing a comprehensive study and generalized design methodology for different diode applications. In the following subsections, multiple applications are discussed and comprehensive literature review is performed.

2.4.1 Mixer diode-heterodyne receiver

In [31], the planar diode, which was presented by the University of Virginia research team [37], is used around 800 GHz and it is shown in Figure 2-7 (a). Also, back-to-back diodes were presented as a mixer in a heterodyne receiver (see Figure 2-7 (b)). They studied the thermal noise and sources of the losses in the diode circuit. In this kind of receiver, diodes are the source of the noise, but most losses occur between the antenna and mixer. In another work [32], they studied physics of a diode with degenerately-doped GaAs and the effect of this heavily doped barrier for THz application of the device.

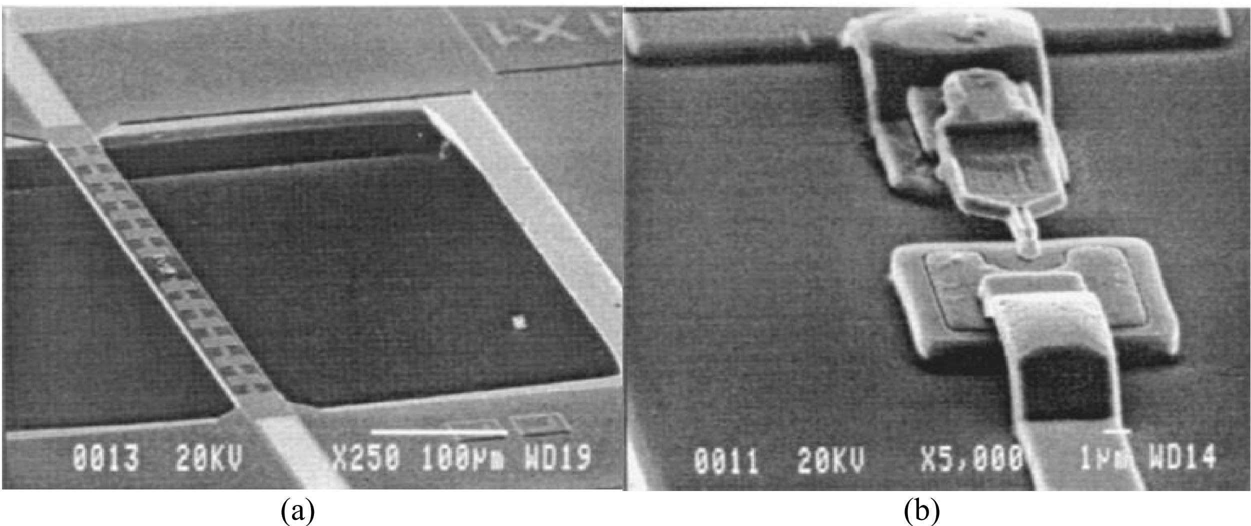
Meanwhile, the JPL (Jet Propulsion Laboratory) group proposed a monolithic mixer based on the Schottky diode, which achieved 2.5 THz frequency at room-temperature [59]. The diode and circuit membrane were based on a GaAs substrate. The mixer is employed in a heterodyne THz detection system. The received signal is mixed with a signal generated by far-infrared laser oscillator and provides an RF signal at few GHz. In the diode fabrication, they employed a T-shape anode technique presented by Alien and Reddy from the University of California, Santa Barbara

[60], [61]. A thin GaAs membrane was used to prevent the bulk substrate skin-depth effect, which increased the diode resistance at high frequency as discussed in [40]. Figure 2-8 is a SEM image of the 2.5 THz monolithic mixer with the GaAs membrane. This membrane was created by making a wide and deep trench all around and under the circuit strip.



(a) (b)

Figure 2-7 The Planar Schottky diode which presented by the Crowe team in 1991 [31].



(a) (b)

Figure 2-8 SEM image of (a) the 2.5 THz Monolithic Schottky diode mixer with the thin GaAs membrane, (b) the diode zoom in image [59].

2.4.2 Multiplier diode- THz source

Thereafter, a cryogenic all solid-state monolithic multiplier chain with 1.5 THz output signal is presented [46]. The multiplier chain provided the 1.5 THz signal by four steps doubling of a 95 GHz input signal with a membrane diodes arrays chain. The block diagram of the complete multiplier source containing a cascade of four frequency doublers is shown in Figure 2-9. The applied diodes in the chain are separately designed and fabricated for their frequency range. The diodes' fabrication was described in two categories, one for the frequencies below 1 THz and second for the frequencies above 1 THz. For instance, photolithography is employed in the first group to make the anode contact. However, since a much smaller anode contact area (~0.3 μm^2) is required, in the second diodes group (over 1 THz), an electron-beam lithography process was used in the anode contact process. A summary of the THz sources based on GaAs Schottky diode multiplier is presented in [62].

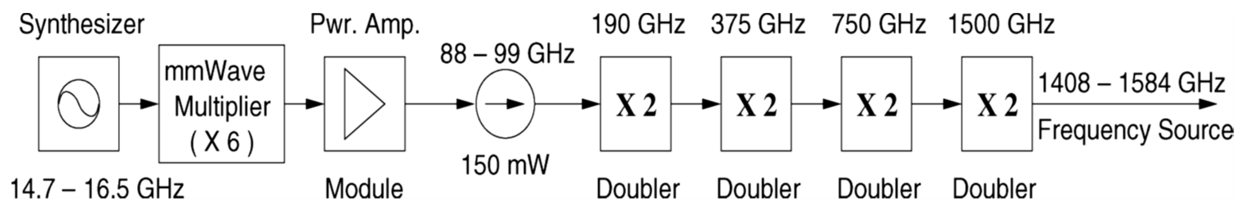


Figure 2-9 Schematic block diagram of the all-solid-state 1500-GHz multiplier source by using four-step multiplier chain [46].

A substrate-less Schottky diode-based multiplier at 200, 400 and 800GHz was presented by the JPL group [63]. The design reduced RF losses and improved system efficiency. Figure 2-10 shows how the 400GHz substrate-less doubler with a GaAs frame holder implemented which is excited by input rectangular waveguide. Then, a Schottky diode tripler at 1.9 THz was presented by developing the previous technology in [64].

Figure 2-11 is the 3D view of the 1.9 THz GaAs Schottky diode-based tripler. It shows the configuration of diodes in the circuit and how the ciruit excites the input and output rectangular waveguides.

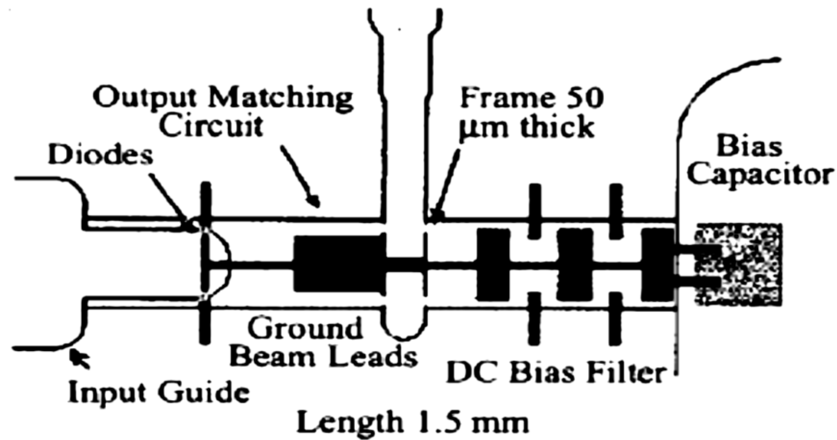


Figure 2-10 400 GHz Substrate-less Schottky diode doubler [63].

A continuous wave coherent source at room temperature for 2.5 THz is presented in [65]. This source with unprecedented 270 GHz bandwidth, achieved by using three cascaded Schottky diode-based frequency triplers, can be used in continuous wave, modulated or pulsed mode.

2.4.3 All-solid-state heterodyne receiver

A 1.2 THz receiver based on the Schottky diode mixer was presented in [66]. In this design, the mixer local oscillator (LO) signal was also provided by a Schottky diode-based multiplier chain [66]. It was the first all-solid-state heterodyne receiver in the 1.2 THz range which worked at room temperature. There was another diode-based mixing system with diode chain LO at 900 GHz presented in [67] that has a cryogenic system to cool the mixer to 120 K.

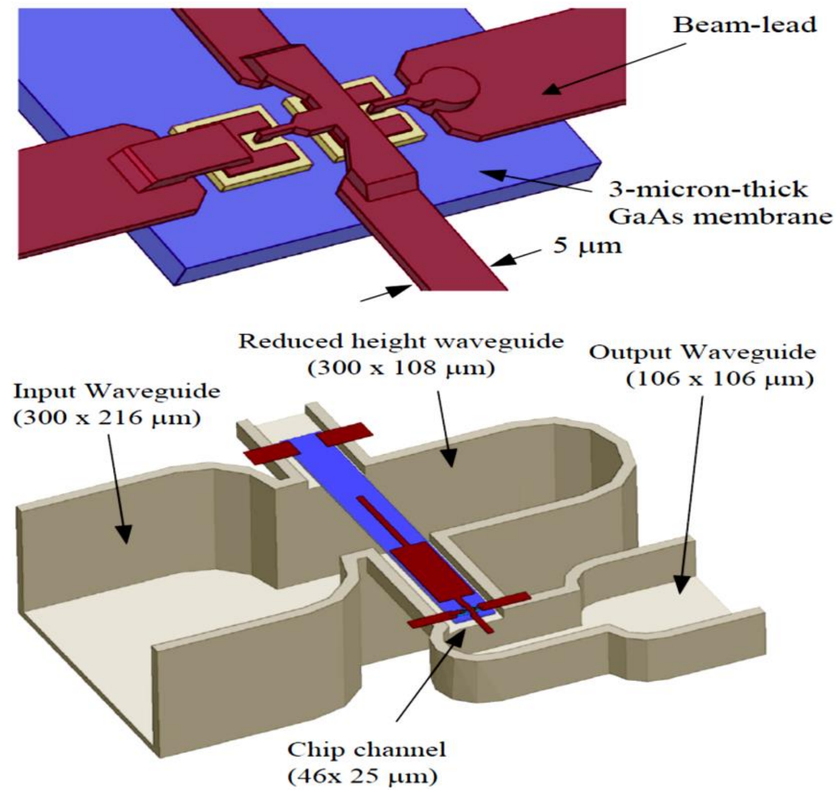


Figure 2-11 The 1.9 THz tripler [68].

2.4.4 Rectifier diode- direct detection

In the high frequency bands, direct detection is very attractive since there is no need for local oscillator. To do so, Schottky diodes have been used for direct detection in THz band.

A broadband THz detector based on a zero-bias Schottky diode is introduced in [69]. The diode and on-chip lithographic antenna are bonded to a hemispherical silicon lens. Both the top and side views of this broadband THz detector are shown in Figure 2-12. The diode is mounted across the feed point of the sinuous antennas by using a flip-chip technique. In [25], a THz rectification system is presented which has the detector diode and the planar antenna fabricated together to improve performance by decreasing the diode size. Also, a tunable lens-coupled annular-slot antenna and a Schottky diode rectifier are reported in [70]. The resonance frequency of the slot antenna is tuned from 140 to 220 GHz by diode capacitance which is a bias dependent variable.

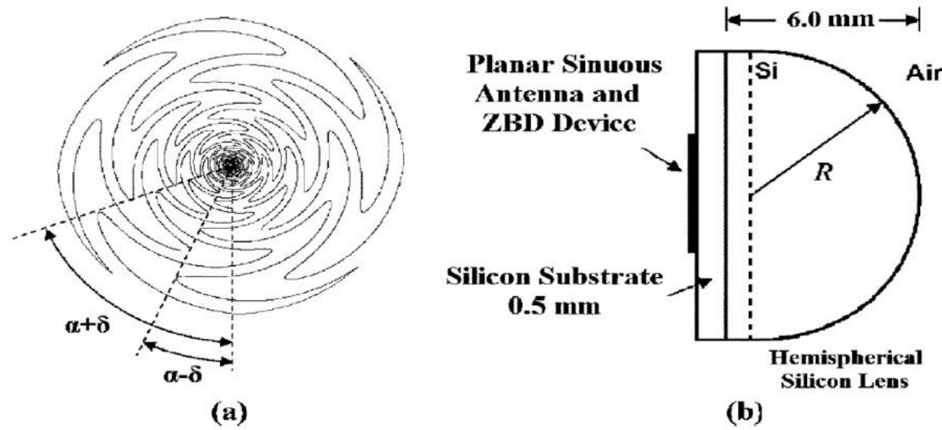


Figure 2-12 Broadband THz detector based on direct detection, (a) the planar sinuous antenna with a flip-chip diode in the center, (b) the diode detector and antenna mounted on a hemispherical silicon substrate lens [69].

In this chapter the diode structural progress, technologies and application developments in the literature are summarized. In most reported works the focus have been on the method of using the diode in a specific application and circuit. The diode itself, design, and optimization is studied in a limited number of reports such as [28], [29], [42], [71]. And the diode characterization is studied in [25], [33], [72], [73]. So, there is a lack of comprehensive study on the diode based on its application and comparison of its performance in each application. Also, studies of application impact on the diode design are missing in the literature. Therefore in this thesis, the diode optimization and frequency behavior based on the application are categorized and compared. On the other hand, the fabrication processes presented in the literature [25], [30], [46], [74], [75] are not cost-effective, flexible, reliable, and repeatable enough to use for mass production and commercial application of the diode. In this thesis, a fabrication process for the diode mass production is presented which is low-cost, more flexible, and easy to repeat is presented.

3 Schottky Diode Application-based Study

Submillimeter Wave GaAs Schottky Diode Application-Based Study and Optimization for 0.1- 1.5 THz

Here a design and optimization method for Schottky diodes is proposed. By employing the optimization method, parasitic capacitance of the diode is significantly reduced (under 20% of the total capacitance) to be able to operate up to 1.5 THz which is confirmed through DC and RF measurements presented in chapter 5. The diode responsivity and noise equivalent power (NEP) is also investigated. Moreover, limiting factors of the diode cut-off frequency in mixer/multiplier and detector mode applications are studied. It is shown that, in mixer/multiplier mode, the usable voltage bias range (with acceptable cut-off frequency) is limited by the exponential reduction of R_j. Therefore, a new approach for more practical cut-off frequency calculation is introduced which is valid for wide ranges of R_j values. Also, a detailed formula is presented for calculation of the diode cut-off frequency for the detector application mode.

3.1 Introduction

There is great interest in the submillimeter-wave spectrum due to its numerous applications in astronomy, spectroscopy, security, surveillance, disease detection, DNA identification and telecommunication [76], [77]. Lack of compact and efficient submillimeter-wave active and passive components slow down technological progress required for realization of the aforementioned applications. Neither design, simulation nor fabrication of these components are fully developed, with fabrication being the biggest challenge.

Diodes are critical elements in submillimeter-wave circuits. During recent decades, GaAs Schottky barrier diodes have been the preferred choice and have had the most significant progress. They are presently used in several submillimeter and terahertz (THz) circuits such as mixers [40], [45], [46], [59], multipliers in solid state sources [46], phase shifters [27], and detectors [25]. For instance, in

[46], an all solid-state monolithic multiplier chain of membrane diodes is presented where the multiplier chain employs four doubling steps to reach 1.5 THz from 95 GHz input signal. This Schottky diode-based multiplier was developed to serve as a submillimeter-wave local oscillator for a heterodyne receiver.

Cut-off frequency is the main parameter in defining the behavior of a diode. It is estimated by $f_c = 1/2\pi C_j R_s$ where R_s and C_j are series resistance and junction capacitance respectively [38], [48]. However, influence of other components of the diode equivalent circuit model and their bias dependency needs to be considered to achieve more accurate results. It is also of significant importance to provide an application-based study for the diode cut-off frequency since different sources of nonlinearity is targeted.

In order to expand the diode cut-off frequency to submillimeter-wave region, reducing the junction capacitance by shrinking the anode size has been the main approach [31], [47], [63]. However, aside from the junction capacitance, the parasitic elements such as parasitic capacitance, have high impact on the diode frequency performance and limits the cut-off frequency. For instance, in [73] the reported parasitic capacitance is 4-5 times larger than the junction capacitance. Therefore, the diode performance is mainly limited by its parasitic elements rather than the junction capacitance.

In the present work, we review and compare four approaches to estimating the cut-off frequency of Schottky diodes. In particular, we extend these approaches by considering the bias dependence of all components, and discuss new limitations that arise.

3.2 Design and Simulation

The design process starts by specifying the frequency range of operation. It is first necessary to define the electron mobility and plasma frequency. These parameters are used to select the appropriate semiconductor and its doping density. Then, based on the wafer specifications, i.e., layers architecture and their properties including thickness, dopant and electron mobility, the performance of the diode can be simulated. A set of design parameters are assumed as the initial values and further optimizations are performed to achieve the desired characteristics. The input variables are semiconductor active layers (Schottky and n-well doped layers) doping, mobility, resistivity and their thicknesses, contact

areas, shapes and their distance, both contact barrier heights, specific contact resistivity (Ohmic), operating frequency, and temperature.

The aforementioned calculations are accomplished by developing a code based on the analytical model of diode. The flowchart of the described design and optimization process is shown in Figure 3-1. Fabrication limitations, such as achievable UV-lithography alignment and precision and having access to high mobility GaAs epitaxy wafers should be taken into account. Initial value of some parameters may be extracted from literature at the beginning to estimate and optimize requirements of epitaxy structure. After determining the epitaxy structure, the parameters (such as contacts barrier heights, specific contact resistivity, layers resistivity and mobility) are replaced by measurement results from quick tests such as TLM, C-V and Van-der-Pauw.

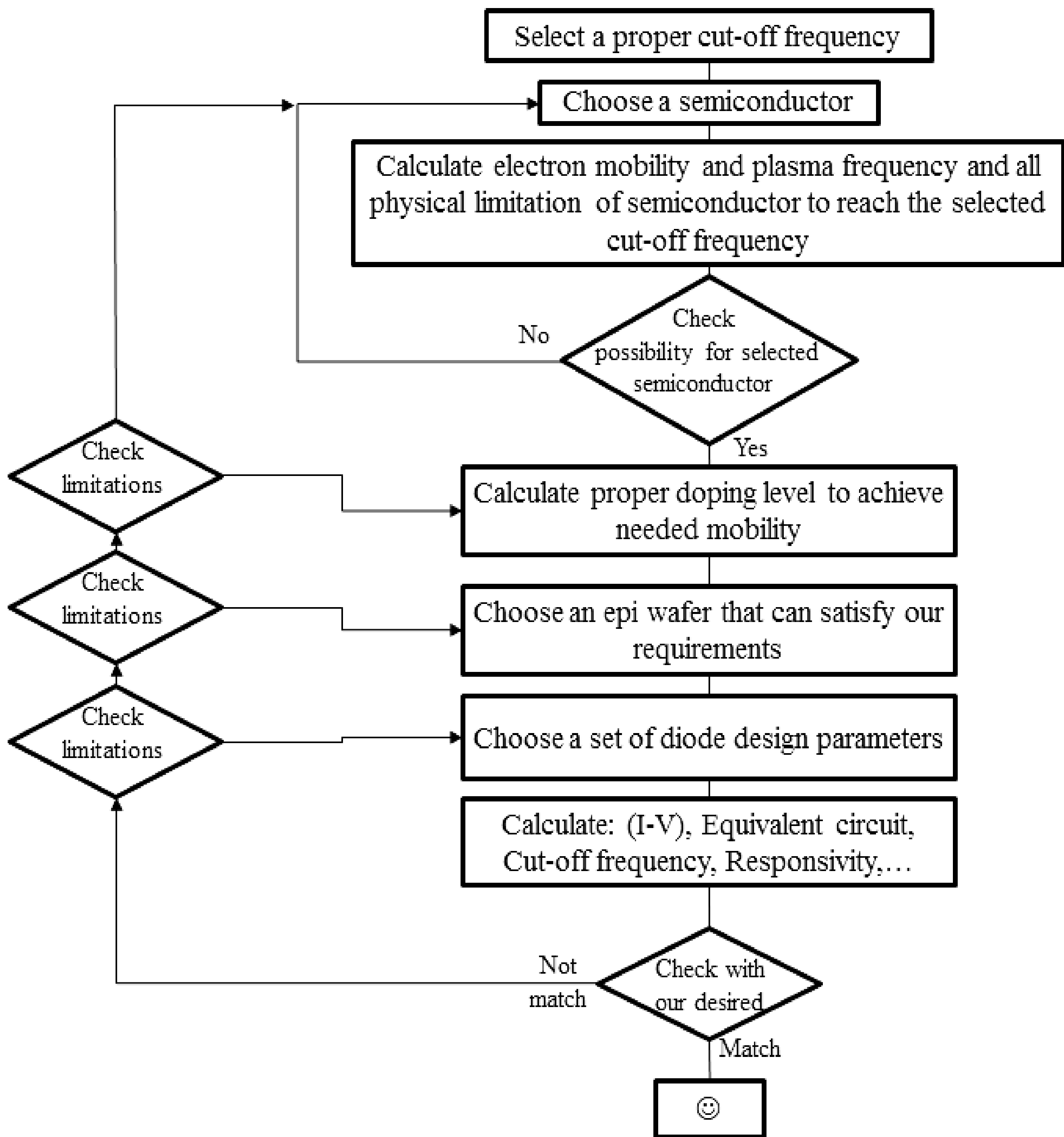


Figure 3-1. Design and optimization process for Schottky diodes.

3.3 Optimization

The cut-off frequency of diodes and related operating frequency ranges are generally linked to the series resistance and junction capacitance through the $R_s \cdot C_j$ factor. Therefore, most of the literature focuses on decreasing the anode dimensions to reduce the junction capacitance, and thereby improve the cut-off frequency.

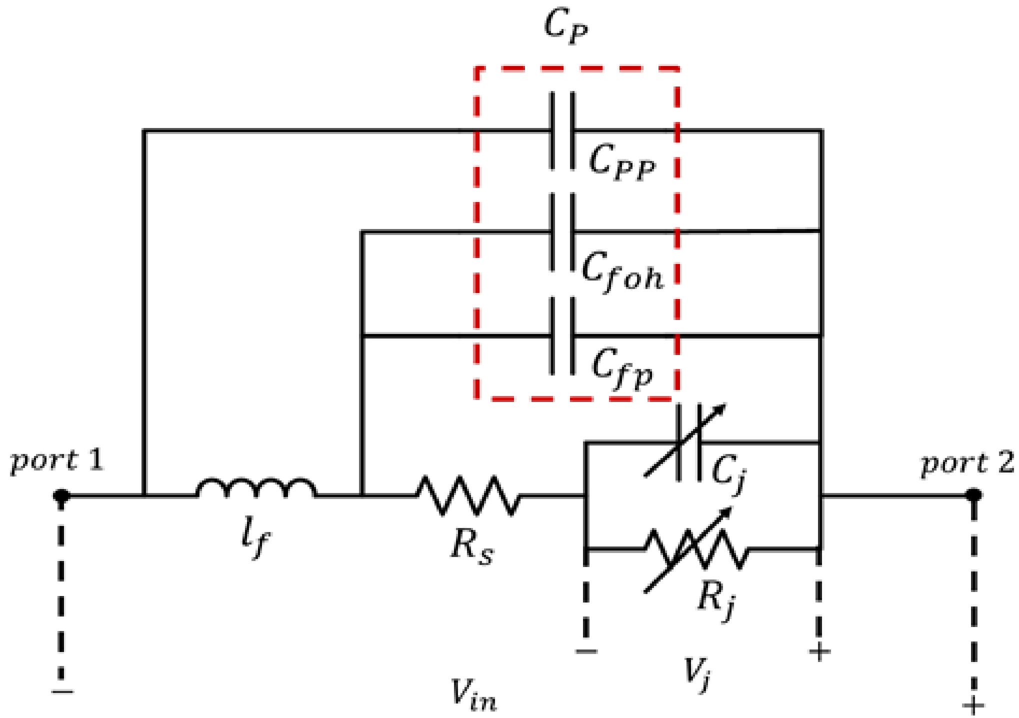
Figure 3-2 (a) shows the Schottky diode equivalent circuit. The diode parasitic components are identified for various parts of the device, as explained in Figure 3-2 (b). The total series resistance is $R_s = R_{sl}(V) + R_{sub} + R_{oh} + R_{p1} + R_{p2}$ in which only R_{sl} has dependency to voltage bias. R_{sl} represents the part of the Schottky layer that is not depleted and therefore grows sub-linearly with the voltage bias across the junction. The junction capacitance C_j and the resistance R_j are the heart of the Schottky diode, which their voltage-dependency generates its nonlinear characteristic.

The total capacitance is defined as $C_T = C_j(V) + C_p = C_j(V) + C_{fp} + C_{foh} + C_{pp}$, where C_p is the sum of all parasitic capacitances. In this work, the impact of C_p on the cut-off frequency is taken into account by considering the total capacitance C_T instead of C_j. Although C_p and C_j, as shown in Figure 3-2, are not exactly in parallel, C_T gives a good estimation of the diode total capacitance and practical cut-off frequency. By reducing the junction capacitance, C_T is dominated by parasitic term that becomes the main limitation of the device. In many cases the parasitic capacitance is shown to be several times larger than the junction C_j itself. For example, in [78], diodes with anode areas of ~1 μm^2 have a total capacitance (C_T) of ~10 fF where the C_j portion is only 1.5-2 fF. Also, in [73] diodes with a claimed cut-off frequency of ~20 THz have C_{j0}=1.3-1.8 fF (C_j at zero bias) and C_p= 5.5-8.5 fF. Therefore, practical cut-off frequencies for those diodes are in the range of 3.9-3.4 THz.

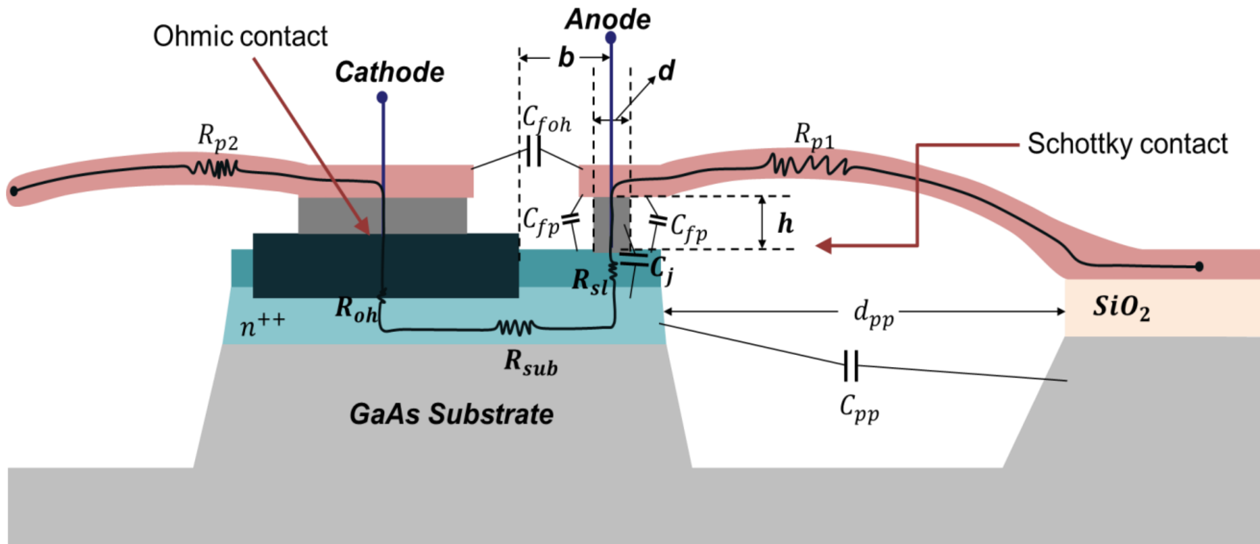
In this work, all parasitic capacitances are taken into account to accurately estimate the practically achievable cut-off frequency. A fabrication process is presented that decreases all parasitic capacitances. Therefore, for a given anode area, the total capacitance of the diode is smaller which leads to higher cut-off frequency. This is accomplished by:

- Increasing the gap between the mesa surface and the finger (h in Figure 3-2 (b)) which reduces the parasitic capacitance between finger and mesa (C_{fp}).
- Increasing the distance between the anode finger and the Ohmic contact and its air-bridge. This reduces the parasitic capacitance between the finger and the Ohmic contact (C_{foh}).
- Increasing the distance between the mesa and input/output transmission lines (here 15-20 µm). Also, embeding a trench (as deep as 5-8 µm) around the mesa to deliver a lower pad-to-pad parasitic capacitance C_{pp}.

The Schottky layer also is of prime importance in optimizing the diode performance. In order to minimize R_{sl}, the thickness and doping of the Schottky layer should be chosen so that it is fully depleted at a bias voltage (V_{Mott}) just below the desired operating bias. Below V_{Mott} the diode operates in the Mott condition [71], [79] and has a quasi-constant capacitance value, providing low non-linear component. At the operating bias, almost all the Schottky layer is depleted, thus minimizing R_{sl}, and the capacitance C_j varies with bias and can provide the required non-linear behavior. These conditions are achieved for Schottky layer thicknesses between 70-130 nm, doping levels between 10^{16} to 10^{18}, and by managing the diode operating bias to put the diode in the optimal situation. Using a thin epilayer around 100 nm and less improves the drift velocity and effective scattering frequency of the Schottky layer [40]. By further increasing the voltage bias above V_{Mott}, both C_j and R_s start to increase and this reduces the cut-off frequency.



(a)



(b)

Figure 3-2. (a) Diode equivalent circuit model. C_{pp} is the pad-to-pad parasitic capacitance, C_{fp} is the capacitance between finger and mesa, and C_{foh} is the capacitance between finger and the Ohmic contact; (b) Schematic of diode side view and equivalent circuit components. Parasitics R_{p1}, R_{p2}, R_{oh}, R_{sub} and R_{sl} are anode finger, Ohmic air-bridge, Ohmic contact, n-well doped channel and the un-depleted Schottky layer resistance, respectively.

3.4 Cut-off Frequency

In this section, five approaches to calculate the cut-off frequency are discussed. The first three apply to mixers and multipliers that usually make use of the diode capacitance which is the dominant non-linear term at low forward or reverse bias. The fourth and fifth approaches are mainly used in direct detection and rectification through the diode's non-linear resistance which is more dominant in higher forward bias regime. The third approach is developed and improved for more accuracy by considering a detailed model and dependency of its components to the voltage bias for mixer/multipliers applications. Also, the fifth approach is developed that gives better understanding of the diode performance.

Approach 1:

In reverse or at low forward biases at radio frequencies, where the junction resistance R_j is much larger than junction reactance ($X_j = 1/j\omega C_j$), the equivalent circuit of Figure 3-2 (a) can be simplified to a series RC circuit (R_s , C_j). Eq. (3-1) is the most common formula to calculate the cut-off frequency of a diode.

$$f_C = \frac{1}{2\pi R_s C_j} \tag{3-1}$$

where $R_s = R_{s0}$ and $C_j = C_{j0}$ are the series resistance and the junction capacitance of diode at zero bias, respectively.

Approach 2:

The bias voltage dependency of the diode's parameters was not considered in approach 1. Therefore, in the second approach, Eq. (3-1) is applied while considering the bias dependence of the series resistance (R_s) and the junction capacitance (C_j). In the first and second approaches, the frequency at which, the power wasted in R_s is equal to half of the input power, is defined as the cut-off frequency.

Approach 3:

In the forward regime, the junction resistance R_j decreases and becomes comparable to the junction reactance X_j and cannot be ignored. Here, all bias voltage dependences, the junction resistance (R_j) and the effect of parasitic capacitances are considered in the calculation of the cut-off frequency.

In this approach the cut-off frequency definition is the same as in the second approach, where the parasitic series resistance absorbs half of the input power or:

$$\frac{P_j}{P_{in}} \sim \frac{|V_j|^2}{|V_{in}|^2} = \frac{{R_j}^2 + \left(\omega C_T R_j^2\right)^2}{\left(R_s\left(1 + \left(\omega C_T R_j^2\right)^2\right) + R_j\right)^2 + \left(\omega C_T R_j^2\right)^2} = \frac{1}{2} \xrightarrow{yields} f_{Crj} \tag{3-2}$$

where the junction resistance at forward bias (R_j) is given by:

$$R_j = \frac{1}{\left({}^{\partial I}/_{\partial V_j}\right)} \equiv \frac{1}{G} \tag{3-3}$$

In this last equation V_j is the voltage over the junction and is related to the forward bias voltage (V_F) as:

$$V_j = V_F - IR_s \tag{3-4}$$

Approach 4:

For direct detection and rectification applications, the non-linear junction resistance is the only element of the diode equivalent circuit that plays role. Here, the absorbed power in junction resistance R_j is the key parameter to define the cut-off frequency. It is defined as the frequency for which the absorbed power in R_j is reduced to half of its maximum value [80]. Eq. (3-5) gives the ratio of absorbed power in the junction resistance P_{Rj} to the total absorbed RF power P_{RF}:

$$\frac{P_{Rj}}{P_{RF}} = \frac{R_j}{R_s\left(1 + \omega^2 C_T^2 R_j^2\right) + R_j} \tag{3-5}$$

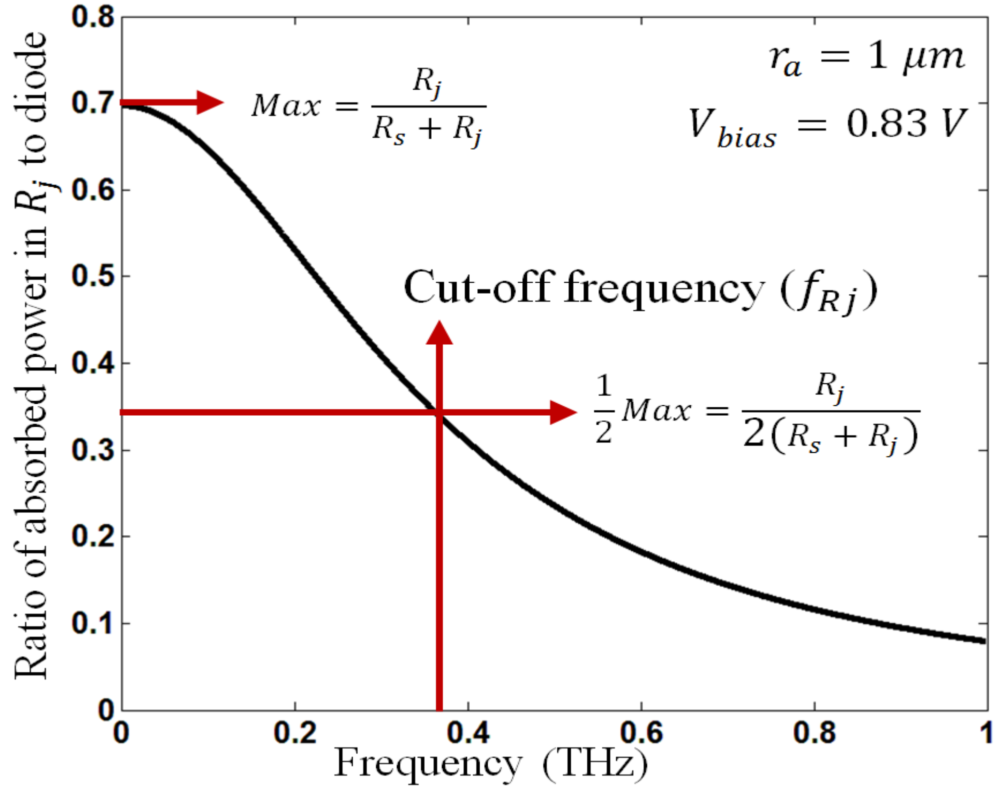


Figure 3-3. Ratio of the absorbed power in the junction resistance R_j to the total absorbed RF power. The maximum ratio value at each bias point occurs at $\omega = 0$ and is equal to $R_j/(R_s + R_j)$. The cut-off frequency is defined as the frequency for which this ratio reduces to half of the maximum value.

In the fourth approach, the effect of parasitic capacitances through the total capacitance (C_T) approximation, is considered like the third approach. Figure 3-3 shows the power ratio of Eq. (3-5) as a function of frequency for a fixed voltage bias (+0.83 V) for our diode with 1 μm anode radius (r_a=1 μm). The cut-off frequency is extracted by that procedure for each bias value:

$$f_{Rj} = \frac{\left(1 + \frac{R_s}{R_j}\right)^{1/2}}{2\pi C_T (R_s R_j)^{1/2}} \tag{3-6}$$

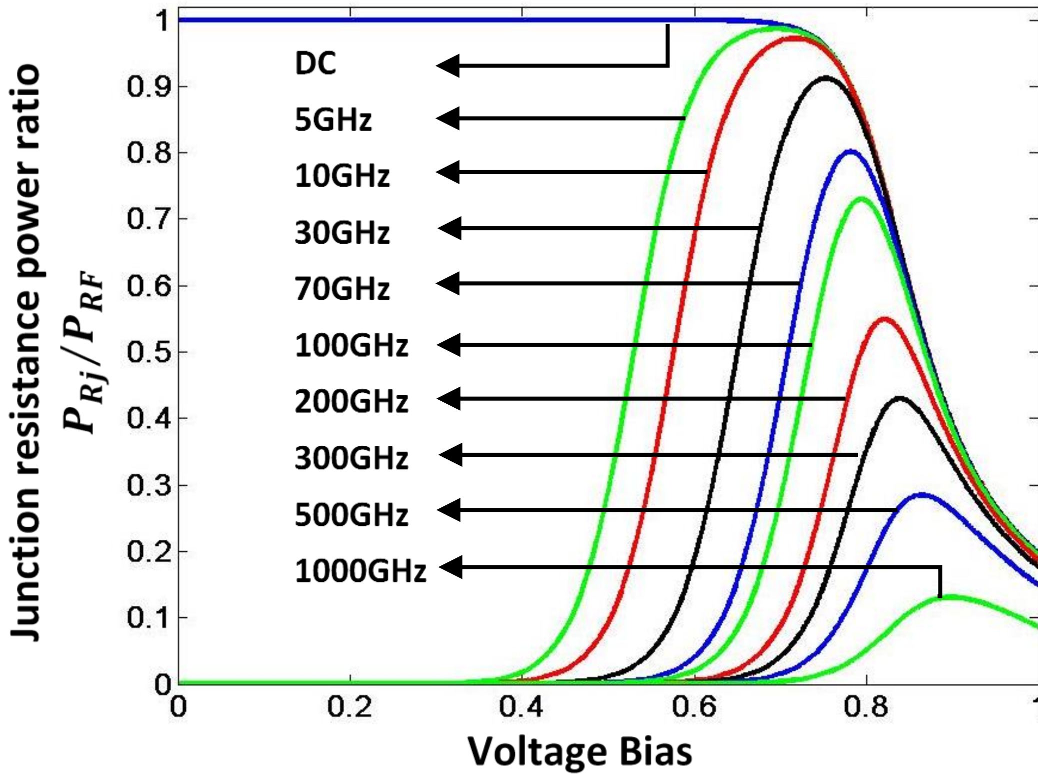


Figure 3-4. Junction resistance power ratio P_{Rj}/P_{RF} as a function of voltage bias and frequency.

The maximum value for the absorbed power ratio in the junction resistance R_j, which happens at DC, is shown in Figure 3-4 (DC labeled). This max-ratio starts to decrease at higher biases where R_j is reduced enough to be comparable with the series resistance R_s. Also, the junction resistance power ratio P_{Rj}/P_{RF} is shown in Figure 3-4 as a function of the bias voltage changes for frequencies going from DC to 1 THz. For each frequency, the peak power ratio occurs at a bias voltage for which R_j and C_T reactance (X_{C_T}) are in balance ($X_{C_T} = \sqrt{\mathrm{R_j}(\mathrm{R_j}||\mathrm{R_s})}$). As the frequency

increases, the decrease of the maximum power absorbed in R_j is indicative of the reduction of the detection/rectification efficiency. Using half of the total power definition for the cut-off frequency, that has been used in the previous approaches, would result in limiting the diode below ~100 GHz despite the fact that the diode can still function above that frequency, but with a reduced efficiency as will be shown in section section 3.5.

The four approaches are illustrated in Figure 3-5 at forward biases for the 1 μm anode radius diode. The cut-off frequency reduction of the third approach (f_{Crj}) with respect to the second approach (f_C) comes from the parasitic capacitances (C_p) impact. The behavior difference in higher voltage range is due to the rapidly decreasing R_j with bias. This R_j reduction dramatically reduces the "mixer/multiplier" mode cut-off frequency and limits this mode voltage bias operational range.

One can observe that, the mixer/multiplier mode (f_C and f_{Crj}) and the direct-detection/rectification mode (f_{Rj}) have very different voltage bias dependencies, as shown in Figure 3-5. This is because the two applications make use of the non-linearity of different components in the diode equivalent circuit model.

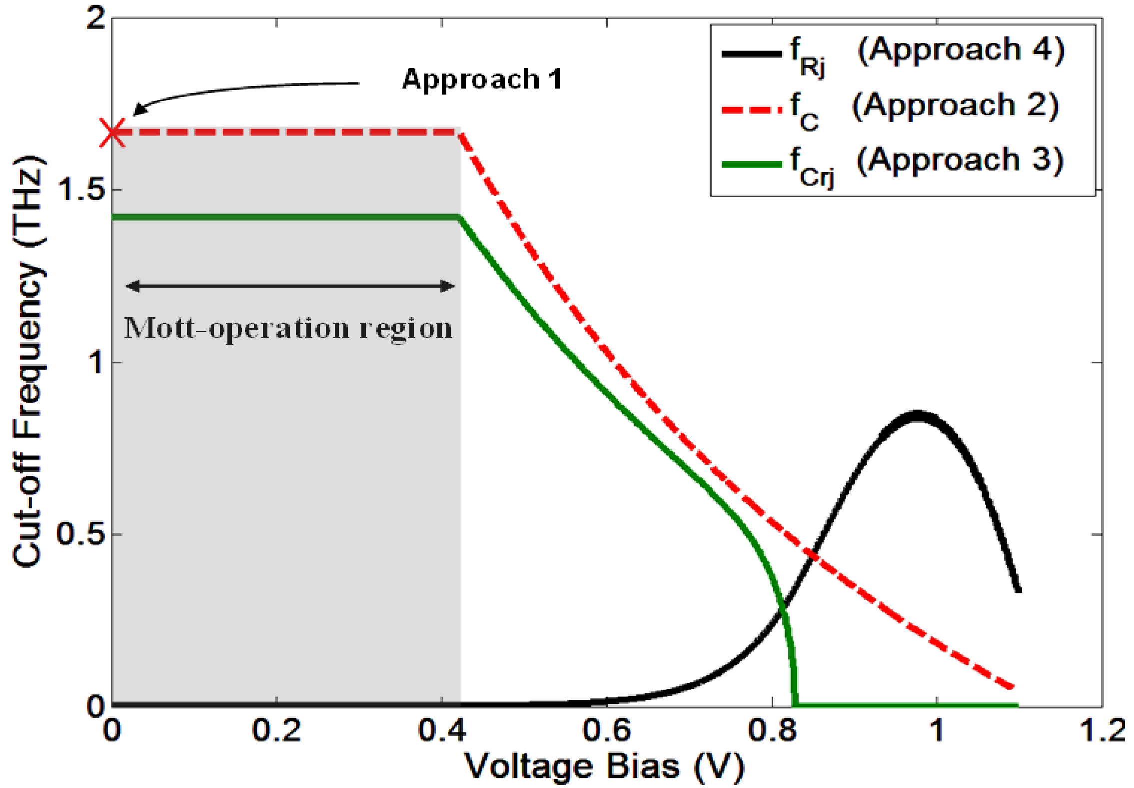


Figure 3-5. Comparison between different methods for cut-off frequency calculation. The f_C is the second approach and f_{Crj} is the third approach (mixer and multiplier applications). The f_{Rj} is the fourth approach, for direct detection applications.

The fabricated diodes, due to the employed hetero-structure and Schottky layer doping level and its thickness, are in Mott-operation mode (for voltage biases up to 0.4 V). While the whole Schottky layer thickness is depleted, both series resistance and junction capacitance are at the minimum values and steady which result in a constant cut-off frequency for this bias range (see Figure 3-5). Also, the vertical shift between f_C and f_{Crj} is due to considering the parasitic capacitance in calculation of f_{Crj}. This shift is much smaller than reported diodes in references [33], [73], [78], because of the small parasitic capacitance of the proposed diodes.

Approach 5:

In direct detection applications, the non-linearity of the junction resistance (R_j) is used to generate a DC current response. In the literature, the cut-off frequency is defined when the absorbed power

in R_j reaches half of its maximum value, as is described in approach 4. However, this maximum absorbed power in R_j (which occurs at DC) is drastically reduces by increasing the voltage bias. In other words, the diode maximum achievable efficiency decreases as its bias increases. Also, f_{Rj} is rising, as is shown in Figure 3-6, but it doesn't represent the same efficiency for the diode along the bias axis. Therefore, a new approach for calculating the diode cut-off frequency is required. In this paper, a new approach is presented which is based on the constant efficiency of the diode according to the absorbed power in R_j. The results for the fabricated diode is illustrated in Figure 3-6 when the absorbed power in R_j reaches to 10, 20, and 40 percent of input power. Therefore, according to the sensitivity of the next block in the receiver chain the minimum efficiency of absorbed power in R_j will determine cut-off frequency of the diode. On the other hand, by increasing the diode DC bias the noise level increases which leads to lower sensitivity. Accordingly, although the cut-off frequency increases as the bias increase, the minimum required efficiency grows which means higher efficiency curve may be required as is shown in Figure 3-6.

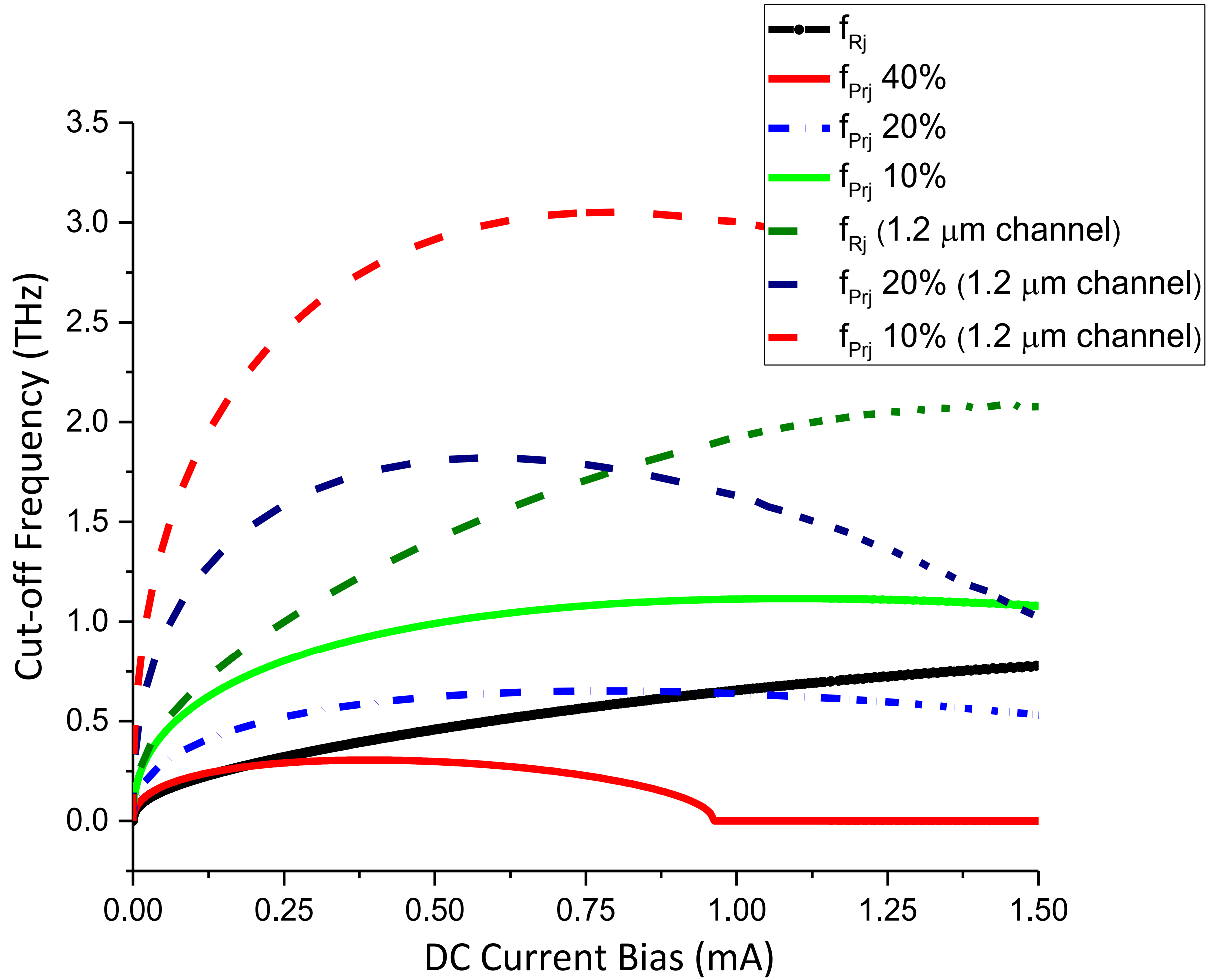


Figure 3-6. Cut-off frequency of diode for direct detection/ rectification applications (it is assumed that the circular diode contact has 1 μm radius). f_{Rj} is calculated by Eq. (2) and f_{Prj} is the new approach with 10, 20, and 40 percent minimum efficiency of absorbed power in R_j. The results are presented for two channel thicknesses of less than 350 nm and 1.2 μm. In the cut-off calculation the impact of parasitic capacitance of diode is taken into account by using $C_T=C_j+C_p$.

3.5 Responsivity and NEP

In direct detection/rectification applications, the real cut-off frequency is dependent on the sensitivity of the next block in the receiver chain. The rectified current for an input voltage signal $V = V_0 + v_0 \cos(\omega t)$ is calculated by taking the Taylor series expansion [81] for small signals resulting in,

$$I = I(V) + \frac{v_0^2 G'}{4} + v_0 G \cos(\omega t) + \frac{v_0^2 G'}{4} \cos(2\omega t) \tag{3-7}$$

where G is defined in Eq. 3 and $G' = \partial G/\partial v$. The DC rectified current due to the input RF signal is $v_0^2 G'/4$. This current for a 1 μm anode radius diode is shown in Figure 3-7 for an input voltage of 5 mV.

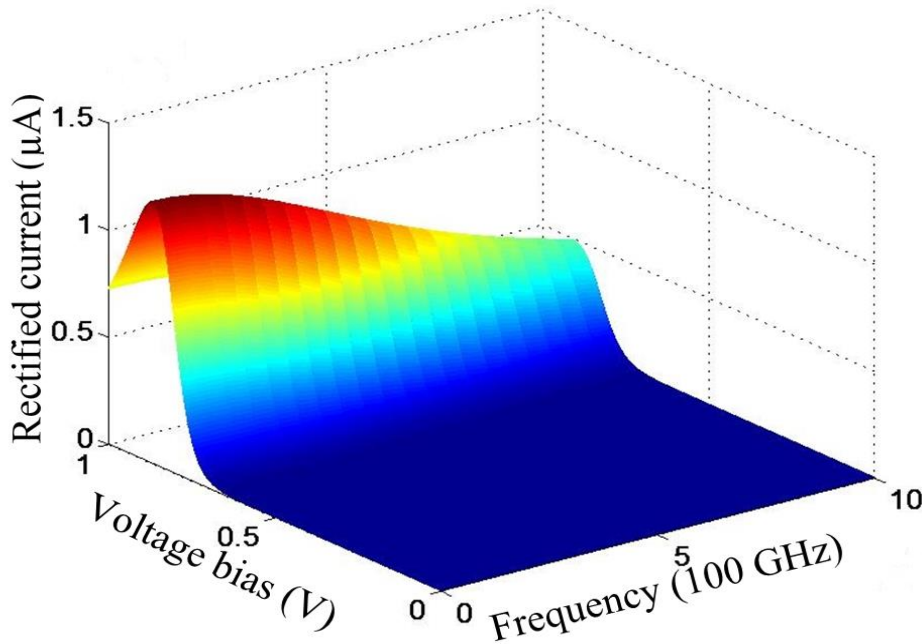


Figure 3-7. The simulation result of rectified current for 1 μm anode radius of this work design when the input signal amplitude is 5 mV.

The important characteristic of the diode for direct detection is current sensitivity β_i defined as the DC rectified current over the RF power to the junction. Using Eq. (3-7) we get:

$$\beta_i = \frac{\Delta I_{dc}}{P_{Rj}} = \frac{G'}{2G} \qquad A/W \tag{3-8}$$

Also, the voltage sensitivity (β_v) which is the DC voltage change across the junction due to received RF signal:

$$\beta_v = \frac{\Delta V_{dc}}{P_{Rj}} = \beta_i \,.\, R_j \quad V/W \tag{3-9}$$

At low frequencies and low voltage biases, R_j and C_j are normally much larger than R_s. At high frequencies, however, R_s and the junction impedance become comparable. Therefore, effects of R_s and C_j on voltage sensitivity due to junction resistance R_j absorbed power ratio is,

$$\beta_{v1} = \frac{\Delta V_{dc}}{P_{RF}} = \frac{\Delta V_{dc}}{P_j} \cdot \frac{P_{Rj}}{P_{RF}} = \beta_i R_j \cdot \frac{R_j}{R_s\left(1 + \omega^2 C_j^2 R_j^2\right) + R_j} = \beta_{i1} \,.\, R_j \tag{3-10}$$

where the power ratio P_{Rj}/P_{RF} is taken from Eq.(3-5). The load resistance (R_l) also reduces the voltage sensitivity by,

$$\beta_{v2} = \beta_{v1} \cdot \frac{R_l}{R_l + R_j} \tag{3-11}$$

If the diode is connected to a system with impedance Z_0, the β_v will be affected by the reflection coefficient (ρ) as,

$$\beta_{v3} = \beta_{v2}(1 - \rho^2) \tag{3-12}$$

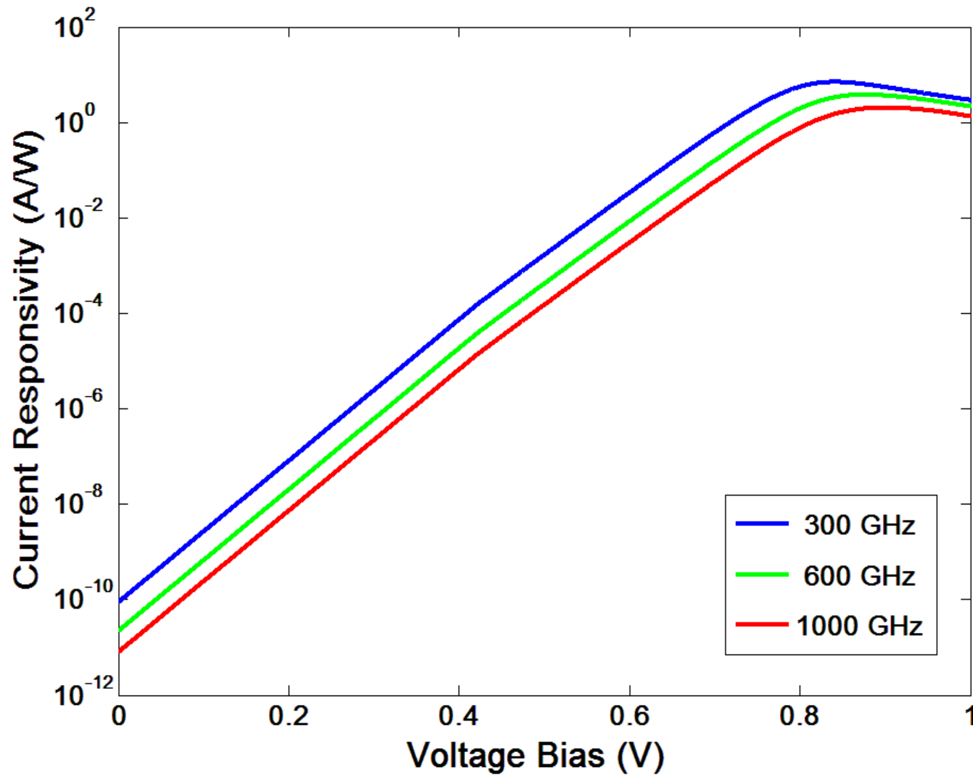


Figure 3-8. The estimated current responsivity β_{i1} as a function bias voltage for 300, 600 and 1000 GHz.

Figure 3-8 and Figure 3-9 illustrate the expected current (β_{i1}) and voltage (β_{v1}) responsivity of our 1 µm radius diode at 300, 600 and 1000 GHz as a function of voltage bias.

Another evaluation scale for diode detectors is Noise Equivalent Power (NEP). The $(NEP)_0$, the frequency independent part of NEP and the diode NEP, are estimated by using the theory presented in [80] and the fitted diode model using measurement results. Figure 3-10 and Figure 3-11 show the results of estimated $(NEP)_0$ and NEP for the fabricated diode with 1 µm anode radius. In Figure 3-11, the diode NEP for 0.2, 0.5, 0.7 and 0.82 V bias voltages is presented as a function of frequency. The diode NEP for 0.82 V bias voltage at 300, 500 and 600 GHz is 1.5, 2.8 and 3.7 $pW/\sqrt{Hz}$, respectively.

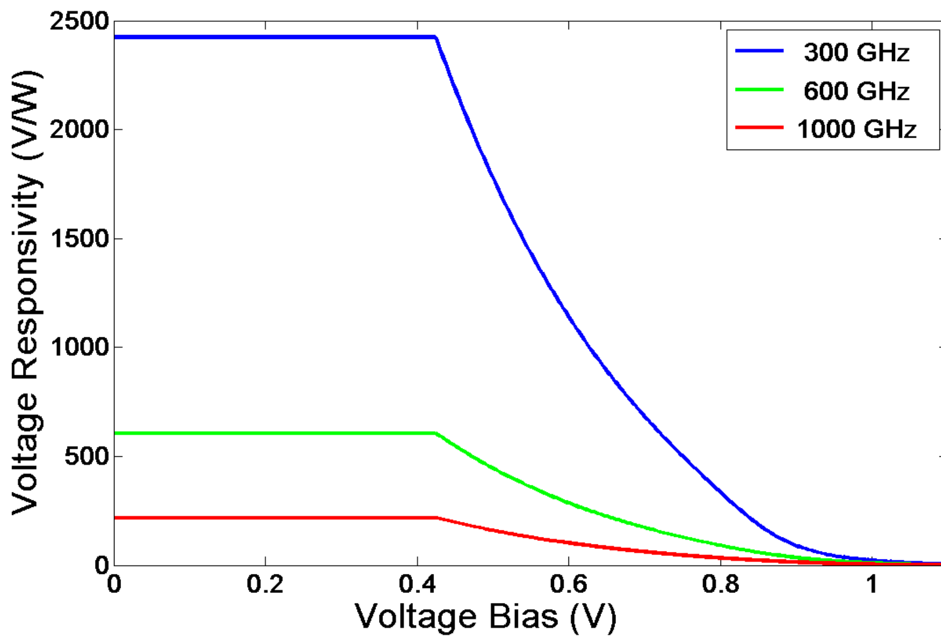


Figure 3-9. The estimated voltage responsivity β_{v1}, as a function bias voltage for 300, 600 and 1000 GHz.

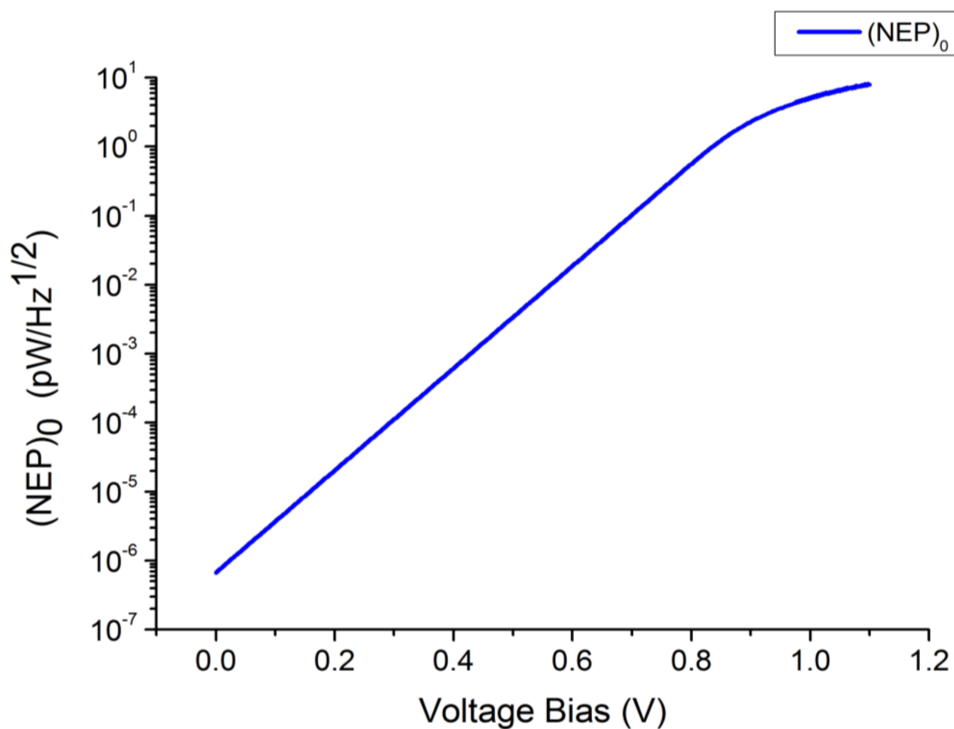


Figure 3-10. The frequency independent part of Noise Equivalent Power $(NEP)_0$ as a function of voltage bias for the designed diode with 1 μm anode radius.

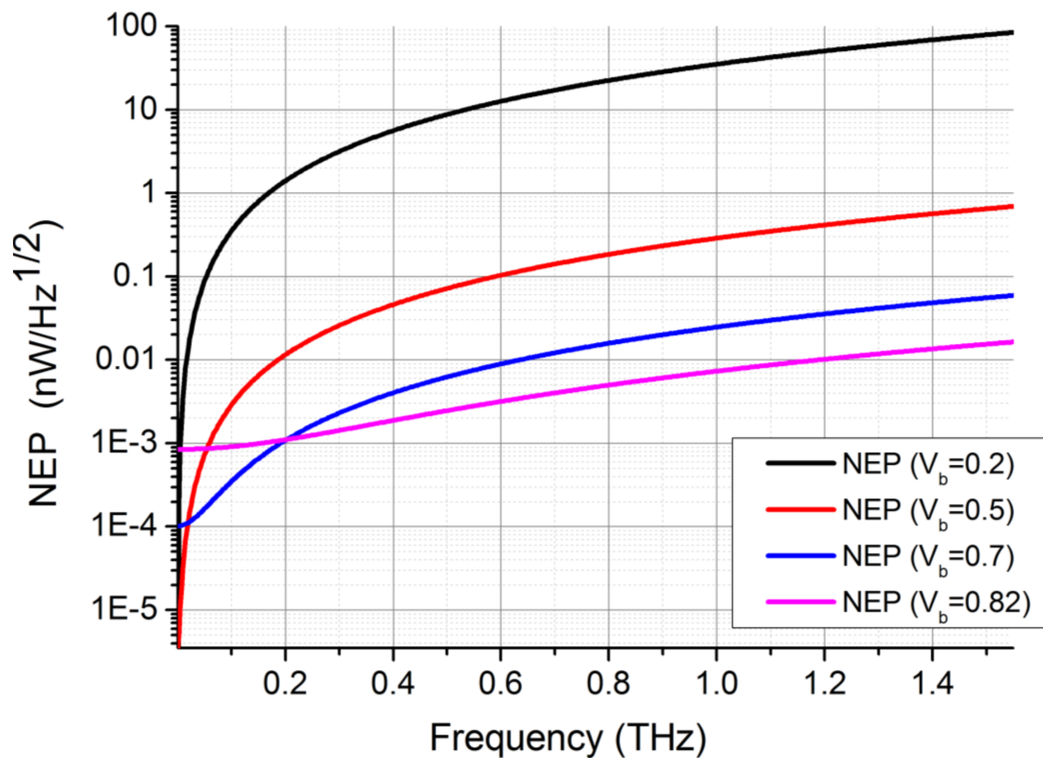


Figure 3-11. Noise Equivalent Power (NEP) as a function of frequency for the designed diode with 1 µm anode radius at 0.82 V voltage bias.

In this chapter the limiting factors of the cut-off frequency both in detector/rectifier and mixer/multiplier modes have been studied. For the mixer/multiplier applications, the conventional method for calculation of the cut-off frequency is advanced and improved. It is shown that the proposed method is able to provide a more accurate and more practical results. It is also demonstrated that, since the diode performance is mainly limited to its parasitic components, the sole reduction of the anode diameter cannot deliver higher cut-off frequencies. Therefore, an optimization method to minimize the parasitic elements of diode, chiefly the C_p is devised. In order to decrease the parasitic capacitance, the air-bridge and connection pads structures are modified. Using this design method, it is shown that the need for very small contacts can be mitigated, and for frequencies below 1.5 THz, the expensive electron-beam lithography step can be avoided, as it is discussed in chapter 4.

4 The Epitaxial structure engineering and Fabrication

A Low-Cost Fabrication Method for Sub-Millimeter Wave GaAs Schottky Diode

We present a modified process for the fabrication of terahertz (THz) and sub-millimeter wave diodes. Based solely on photolithography, this process gives more flexibility in design parameters and allows a significant reduction in the device parasitic capacitances. A key feature of the process is that the Schottky contact, the air-bridges, and the transmission lines, are fabricated in a single lift-off step. The process relies on a planarization method that is suitable for trenches 1 to 10 μm deep and is tolerant to end-point variations. The process is compatible with a large range of anode sizes depending on the frequency target. This process is also compatible, without any changes, with electron-beam lithography to produce very small anode areas. We also present an analysis of the effect of the Schottky layer thickness on cut-off frequency. The measurement and characterization results show an excellent agreement with the simulations.

4.1 Introduction

One of the obstacles to the development of sub-millimeter wave devices is lack of low-cost, reliable and efficient fabrication techniques. Schottky diodes are key elements in electronic circuits which their fabrication becomes more and more challenging in high frequencies due to the small size of the device and high sensitivity to parasitic elements.

As is discussed applications of Schottky diodes can be classified in two main categories: direct detection/rectification [72], [82], in which the non-linearity of the junction resistance is used; and mixer and multipliers [45], [46], [59], [66], [77] that exploit the non-linearity of the junction capacitance. The relation between the diode's cut-off frequency and its application is discussed in chapter 3. One of these specifications is the Schottky layer thickness, for which the impact on the diode performance, for different applications, is studied in this chapter.

In the fabrication of the diode a low cost, reliable, flexible, and repeatable process is required if THz technology is to be commercialized and used for mass production. The so far reported fabrication methods in order to realize a sub-millimeter Schottky diode are summarized here, for comparison. Although the overall processes have similarity since all resulted alike structure, their approaches are different.

In [84] a fabrication process presented by using a planarization method based on pouring a polymeric resist to fill the trenches and make a flat surface by cap the wet resist with a polished superstrate glass and let the resist dry and remove the glass. Then, etch back the polymeric resist. This process is extremely sensitive to the etch-back stop point. Also, since the glass layer shapes the planarization resist, its thickness cannot be accurate. Therefore, etch back time would be a challenge.

A research group which have had effectual progress in fabrication of sub-mm/THz wave diodes is Jet Propulsion Laboratory (JPL). They reported two fabrication processes for their diodes. This paper proposed a process for diodes under 800 GHz which used reshaping resist to build air-bridge without trench underneath. The second process was for diodes above 800 GHz which includes planarization. Acetone spray etch-back technique was employed in the planarization (as we discussed it in our manuscript). These processes are used at JPL for THz diodes for several projects such as their room temperature receiver [66].

The other method that was employed for the diode realization is to build the bridge then wet etch the isolation trench in the presence of the finger contact bridge such as in [83] and [85].

Comparing above listed processes with this work fabrication process presented in this chapter shows the novelty of our approaches in many aspects.

In [47], two processes for fabrication of sub-millimeter wave Schottky diodes have presented. First, for frequencies below 1 THz, a patterned resist reflow technique was used to provide air-bridge support. Second, for frequencies above 1 THz, an acetone spray etching back technique of PMMA was employed for planarization and to make the air-bridges supports. These processes require several metallization steps for diodes and their required interconnections. Another process based on an e-beam lithography has presented in [83]. In this process, a trench is wetly etched under the fabricated bridge to reduce the parasitic capacitance.

These fabrication processes are currently used to produce THz diodes primarily for research purposes and few other expensive products. Thus, low-cost, reliable, flexible microfabrication methods are needed if THz technology is to be commercialized and used for mass production.

Here we proposed two fabrication strategies for the same design of THz GaAs diodes: 1- Multi-Step Metallization (Multi-SM); 2- Double-Step Metallization (Double-SM). Although, both methods produce diodes with almost the same geometry, the Double-SM method is less complicated and has several advantages.

These processes include a new planarization method that gives more flexibility in fabrication and some of the design parameters. It can also be used in the fabrication of other THz integrated circuits in order to reduce parasitic capacitances. In the final process, the T-shaped anode is fabricated using photolithography. Smaller contact size (in order to increase the diode cut-off frequency) is achievable with this process, with only one added step E-beam lithography for anode openings, without any changes in other steps of the process (with the same planarization).

In the final process, the UV-lithography based T-shaped contact using multiple steps of UV and deep-UV is used with three layers resist. The diode and its integrated waveguides are fabricated by using only two metallization steps. First step is Ohmic contact which has to be annealed, and therefore its metallization should be done separately. The second metallization step is used to create the anode, air-bridges (interconnecting bridges) and waveguides (or other passive circuit elements). Therefore, two metallization steps are the minimum number possible in fabrication of Schottky diodes. The methods presented here are reliable, low-cost, and offer more flexibility for the device and the circuit designers.

4.2 Epitaxial structure engineering

One of the pivotal parameters in the diode design is the thickness of Schottky layer, especially when its doping is in lower range. The diode performance as function of the Schottky layer thickness for different applications are studied here. The Schottky layer is considered to be n-doped GaAs with doping level of $4\times 10^{16} cm^{-3}$ and thickness variation from 5 to 300 nm. The n-

well doped channel with $5\times 10^{18} cm^{-3}$ doping level and thicknesses (D) of less than 350 nm and 1.2 µm is presumed. In the fabricated diode a 110 nm Schottky layer is selected and the channel layer is <350nm. Although, thicker channel is more desired, it is selected based on the availability of the wafer.

For the design of our diodes, we have developed a model based on the detailed geometry and material properties of the diodes. In studying the diode performance over the frequency spectrum, the relevant application should be taken into account as is discussed in chapter 3. Since diodes have two nonlinear elements in parallel (R_j and C_j as is shown in Figure 3-2), the application will specify which one is dominant. The diode-equivalent model is shown in Figure 3-2.

The effect of some diode design parameters, such as anode contact size and Schottky layer dopant, have already been studied *e.g.* in [40]. Here we focus on effect of the Schottky layer thickness on the diode's frequency behavior as a function of voltage bias.

In the case of direct detection applications, Figure 4-1 shows the cut-off frequency (f_{Rj}) (Chapter 3-approach 4) and the new approach cut-off (f_{Prj}– Chapter 3-approach 5 with minimum efficiency of 20%, as function of the Schottky layer thickness and voltage bias. In the low voltage biases, R_j is so large that it is almost an open circuit. Also, as bias increases (for the fabricated diode in this work, 1 Volt and higher) the diode is in high level injection and Ohmic effect region of current-voltage (I-V) curve. Therefore, these two regions are not suitable for direct detection/rectification applications. In this application and with the abovementioned Schottky layer dopant, thicknesses between 30 to 150 nm is suggested. According to Figure 4-1, outside the suggested range, the diode cut-off frequency is much lower than its optimum point.

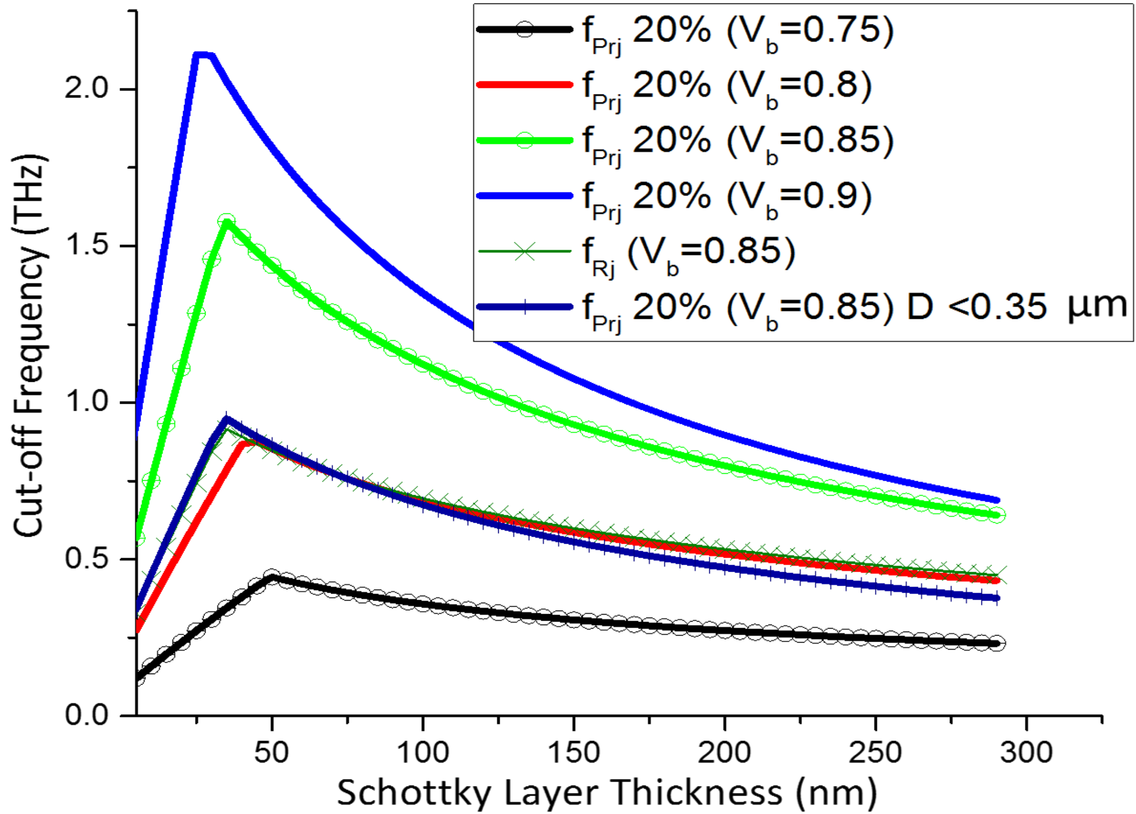


Figure 4-1. Cut-off frequency of a diode for direct detection applications as a function of the Schottky layer thickness for different voltage biases. The diode has a 1 µm radius circular anode contact and a $4\times 10^{16}\ cm^{-3}$ doped Schottky layer and channel thickness D=1.2 µm. The results are compered at V_b=0.85 V with f_{Rj} (Eq. 2) and the new approach for channel thickness (D) <350 nm (as it is in the fabricated diode in this work).

Figure 4-2 shows the cut-off frequency of a multiplier diode (f_C) for different bias points as a function of Schottky layer thickness. The Mott mode border shows the point that the diode goes to Mott-operation, where the C_j is constant and therefore there is no multiplication due to nonlinearity of C_j. Thus, the proper voltage bias area for a multiplier diode is after Mott mode border and before the diode is turned ON. When it is ON, the resistance R_j is small enough to take a considerable portion of the signal power. In mixer and multiplier application, diodes with $4\times 10^{16} cm^{-3}$ Schottky layer doping and more than 80 nm thickness is suggested. According to Figure 4-2 the proper bias range becomes very narrow or disappears for 80 nm or thinner Schottky layers.

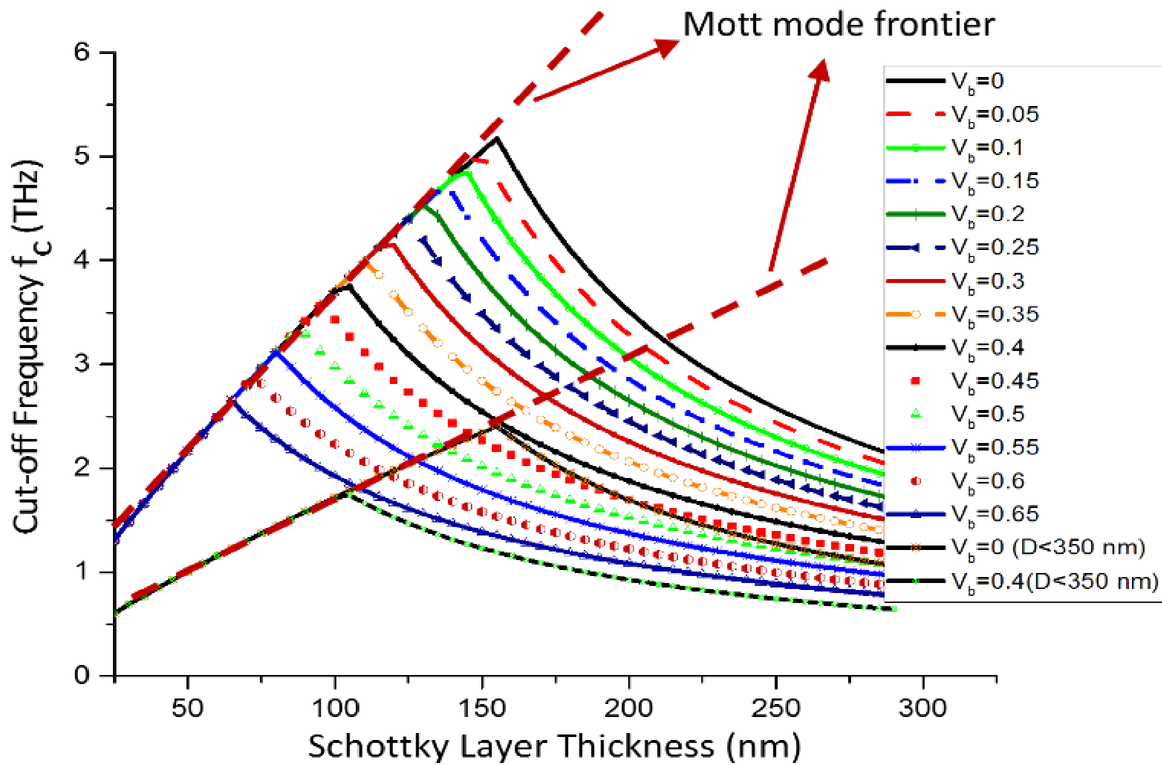


Figure 4-2. The multiplier application cut-off frequency of the diode, with 1 µm radius circular anode contact and $4\times 10^{16} cm^{-3}$ doped Schottky layer, as a function of Schottky layer thickness for different bias points. The results are compared for two channel thickness (D) <350 nm (as it is in the fabricated diode in this work) and 1.2 µm. In the cut-off calculation the impact of parasitic capacitance of diode is taken into account by using C_T=C_j+C_p.

From the strict cut-off frequency point of view, it is possible to design a diode that can be used for both applications. For instance, with a 110 nm thick Schottky layer and $4\times 10^{16}\ cm^{-3}$ dopants, diode can operate at biases between 0.43 V and 0.65 V as a multiplier, and at biases between 0.7 and 0.9 V as direct detector.

Engineering of the Schottky layer, which includes its doping level and thickness, have significant impact on diode frequency performance. An optimized combination for the voltage bias, the Schottky layer thickness, and its doping level can be achieved for certain application through studies demonstrated in Figure 4-1 and Figure 4-2. By adjusting the voltage bias, we are able to optimize the diode for a certain application, or have a multi-purpose diode. The fabricated diode in this work is a multi-purpose diode.

4.3 Fabrication

Two microfabrication processes are developed which are based on photolithography and avoid expensive e-beam lithography. The two processes provide a T-shaped Schottky contact and air-bridge through planarization over deep etched trenches. Both points are critical to lower the parasitic capacitance of the diode. The Multi-SM method is more accessible because it does not require deep-UV technology. However the Multi-SM method is more complicated due to its multiple metallization steps in comparison to the Double-SM method.

4.3.1 Overview

In the realization of the diode, an available HBT GaAs wafer with a low n-doped ($4\times 10^{16}/cm^3$) as Schottky layer and highly doped (n^+) contact layer ($5\times 10^{18}/cm^3$- less than 350 nm thickness) has been used, due to budget constraints. The highly doped layer we are working with is very thin in comparison to the one in other work, which are normally ~1.5 μm thick to decrease the series resistance of diode. In this work the impact of the optimization method on the diode capacitance is considered, and the thin channel does not have influence on it.

Some of the techniques developed for these processes, such as planarization, T-shape contact and air-bridge over the trench, can be used for fabricating other sub-millimeters devices as well. Since there is an increasing need for commercialization of sub-millimeters and THz technologies, it is necessary to find a reliable, low-cost and flexible microfabrication method that can be used for mass production. The presented methods in this work provide more flexibility in design of the device and circuits, low-cost, and highly reliable. It is based on the facts that in the final presented method (double-SM):

- Number of metal deposition which mainly include thick Gold (Au) deposition is reduced to two which one of them (ohmic contact) does not include thick metal layers. Moreover, the thermal evaporation is a costly process.
- This process avoid time and cost consuming e-beam lithography for the anode and air-bridge by reducing the parasitic capacitance of the diode structure and improve the diode performance. Even in the case that very small contact is required, only the anode opening which is a fraction of micro-meter square will require e-beam process.

- All resists and chemicals used in this process are the common, available and low cost products. Especially in the case of planarization method, which is normally a complicated, time and cost consuming process, our reported process is flexible, simple, and repeatable, with high error tolerance, time and cost efficient. For example in compare to planarization method presented in [84], which is the last presented process by VDI group. That is based on pouring a polymeric resist to fill the trenches and make its surface flat by cap the wet resist with a polished superstrate glass and let the resist dry and remove the glass. Then, etch back the polymeric resist.

Moreover, presented process in this work can provide higher reliability and yield according to:

- Simplified process
- Flexibility and easier repeatability
- High error toleration of the planarization process
- The fact that the air-bridge is built in the last step so there is no damage risk due to next step, unlike so far reported processes.
- Failure probability of other steps, which are in common with the other reported processes, such as mesa etching, ohmic contact and lift-off process can be assumed the same. Note, number of lift-off process is only two in Double-SM process which is the minimum number.

The primary method, although it is more complicated and included additional limitations in comparison to the final method, is nevertheless easier to achieve because it does not require Deep-UV technology. These two fabrication strategies are called Multi-Step Metallization (Multi-SM) for the primary process and Double-Step Metallization (Double-SM) for the final process. In both processes a unique method is introduced for planarization and air-bridges which are placed over the trenches. The air-bridge process includes a T-shaped contact fabricated using only photo-lithography. However, in the case of the smaller size Schottky contact, which is considered for increasing the diode functional frequency, E-beam lithography can be used. The air-bridge process that includes the E-beam step is completely compatible with the proposed planarization method. It merely substitutes one UV-lithography step with E-beam for the Schottky contact openings.

4.4 Mask design

Before the fabrication starts, the process needs to be designed in order to draw the masks. In the designed masks, six diodes with different anode contact areas are designed from 3 to 28 μm^2. These diodes include four design with circular shape anode (radiuses: 1, 1.25, 1.5, 2 µm) and two design with elliptical shape anode (axis: 2;3, and 4;6 µm). The designed mask set also contains a back-to-back diodes mixer configuration with the above mentioned diodes. The single diodes are employed in three kinds of connection formations. One configuration is for DC measurement, with two connection pads for anode and cathode as is shown in Figure 4-3 (a). The other two configurations are designed for RF measurement by using coplanar waveguide (CPW). In the second configuration, the diodes are in series with CPW at the middle of line with two probe measurement setup. In the third configuration, the diode is in parallel and ground ended with one probe measurement setup. The RF characterization configurations are shown in Figure 4-3 (b-c). The CPW lines are designed for 0-40 GHz band which is the frequency band of our available VNA that is used for the diodes characterization. Also, an on-board TRL calibration kit (Figure 4-3 (d)) is used for calibration of the VNA. For the projected fabrication process, eight mask layers were required. The two presented processes have some common steps and each process has its own advantages.

The masks were designed for a 1.2 × 1.2 cm sample size. For each layer, an opening frame was designed around the mask layer. The opening frame is wide to ensure we can easily see the sample through it without requiring a microscope. The frame is used to find the small sample under the five inch dark-field glass mask. It is more useful when the opening patterns of the layer are very small. This frame saves time in alignment process and makes it easier. The size of the inner frame is the same as the sample. Therefore, aligning the sample edges with this frame is the first step of alignment that accelerates this process significantly.

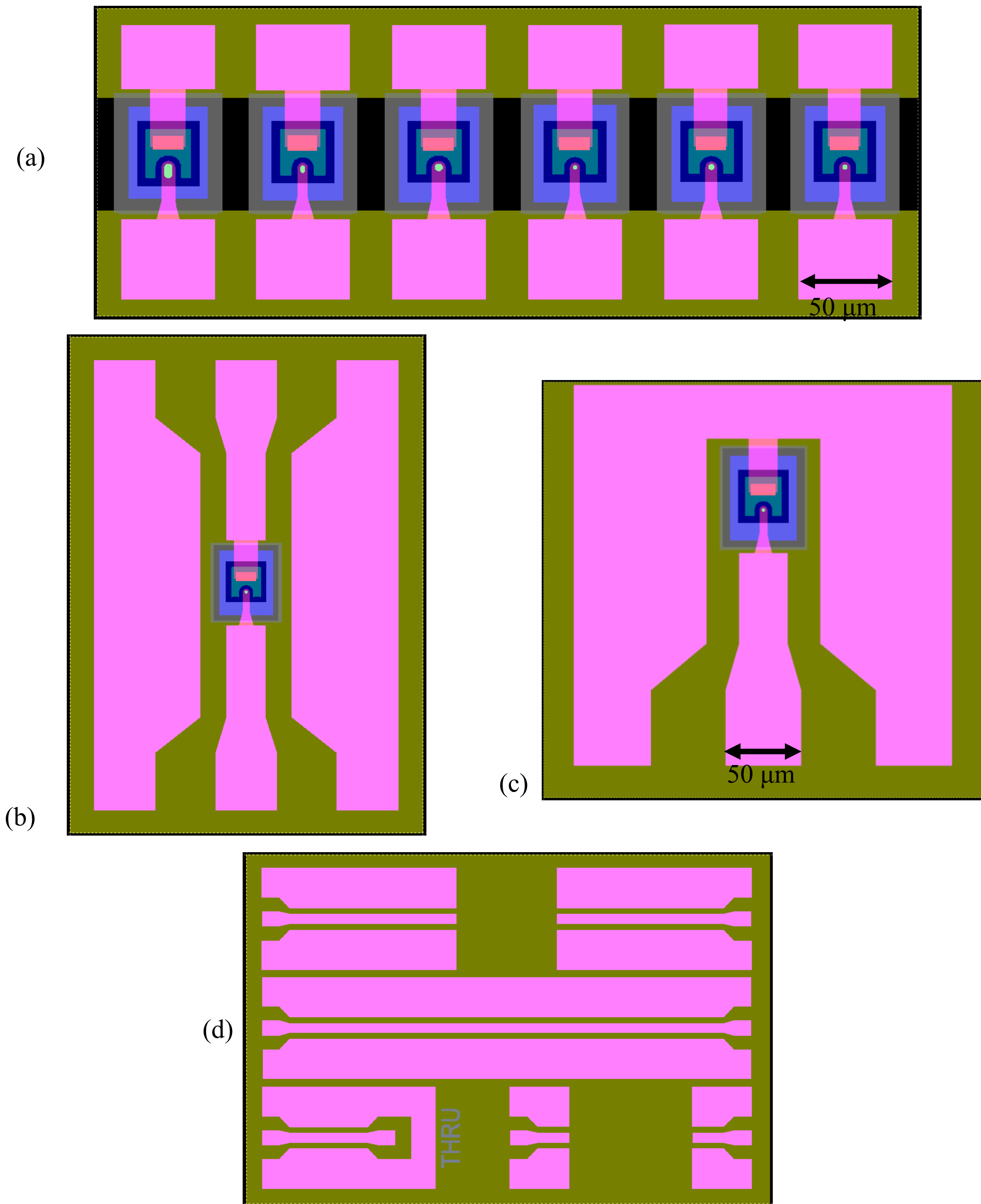


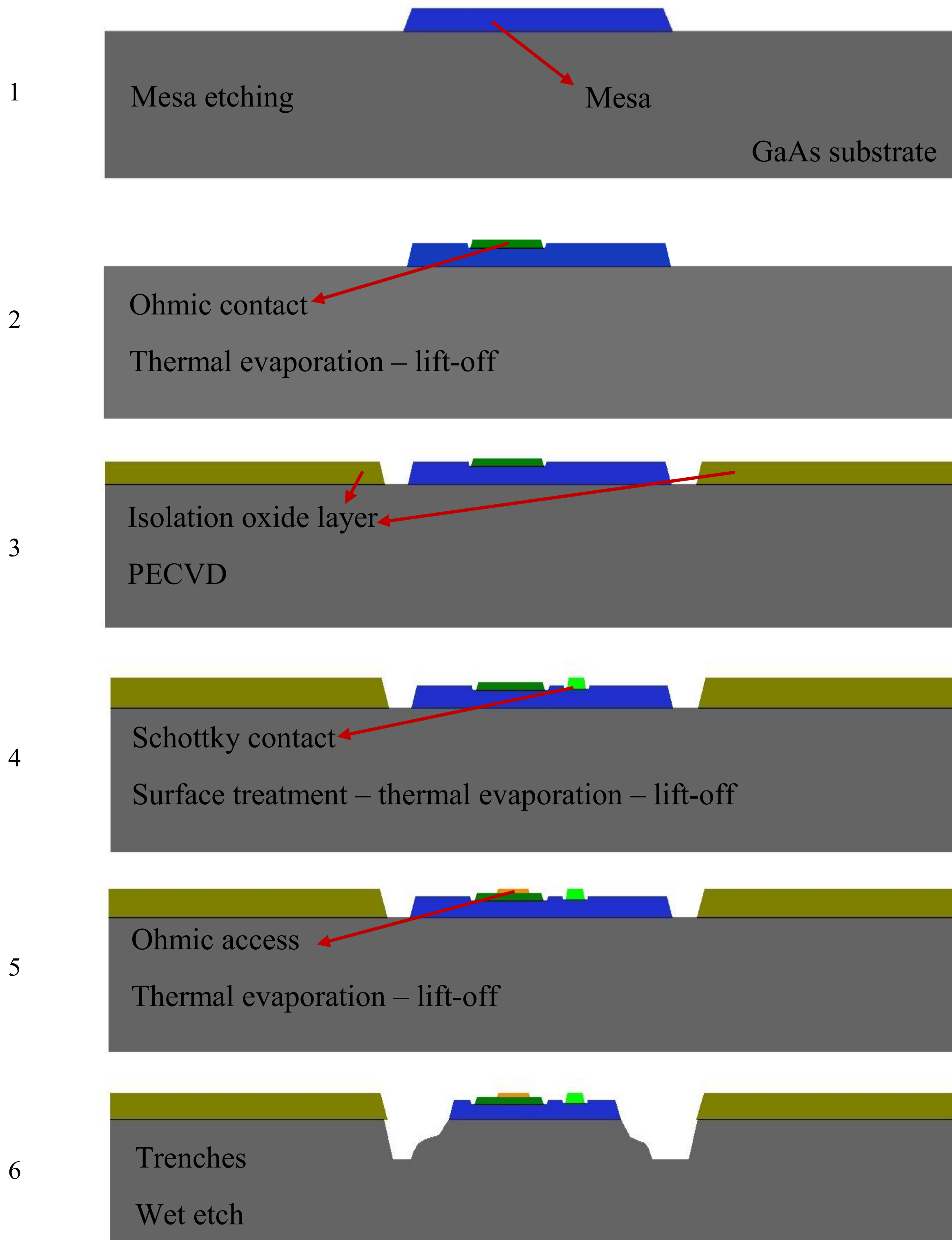
Figure 4-3 The designed structures and diodes on the mask, (a) the single diodes configuration for CD measurement, (b) the series configuration of the single diode for two probe RF measurement, (c) the shunt configuration of the single diode for one probe RF measurement, (d) the RTL on-board calibration kit.

Before staring the diode fabrication process, we needed to dice the wafer to 1.2 × 1.2 cm samples. Also, the selected wafer is double-side polished, making it impossible to recognize without electrical measurement the top side of wafer after dicing it. It is very important since just one side of the wafer has the epitaxy structure on. Consequently, before dicing the wafer, we labeled and numbered each sample by a brief wet-etch on the backside of the wafer. This also makes the samples easy to distinguish from each other. For that, we first coat a thick resist on the top side of the wafer for protection. Then, we laminate a dry-film resist on the both sides of the wafer. The dry film is considered because we do not want to risk the top side to be scratched by coating resist upside-down on the backside of the wafer. Also, the dry film is much thicker than normal liquid resists so it can protect the top side (the epitaxy structure) during the photolithography and etching process on the backside of the wafer.

4.5 Multi-SM process (primary)

The diode fabrication starts with wet etching the mesa with $H_2O_2{:}H_3PO_4{:}H_2o$ (10:10:400) ml solution, to reach the un-doped substrate (Figure 4-4 (1)). Since, the solution contains hydrogen peroxide (H_2O_2), the etch rate is not constant over time after making the solution. Therefore, for more accurate and repeatable results, we considered the time between making the solvent and starting the etching process. The Ohmic contact ($Ge{:}Au{:}Ni{:}Au$) is thermally evaporated and patterned by a lift-off process (Figure 4-4 (2)). When the Ohmic contacts are patterned, and before the metal deposition, a brief wet etching of GaAs is required to remove the lower doped Schottky layer over the Ohmic contact area. After the metal is deposited, in order to change the contact mode from rectifier to Ohmic, it is annealed at 435˚C by using rapid thermal annealing (RTA). An isolation layer of silicon oxide (SiO_2) by plasma-enhanced chemical vapor deposition (PECVD) is deposited. This dielectric layer isolates the metallic contact pads and transmission lines from the substrate GaAs and prevents the leakage through the bulk substrate (Figure 4-4 (3)). The Schottky contact, with a pre-surface treatment, is thermally evaporated and patterned by the lift-off process (Figure 4-4 (4)). The treatment is made to avoid Fermi level pinning. For the cathode bridge, an access pad mounted over the ohmic contact is created by ($Ti{:}Au$) thermal evaporation and a lift-off process (Figure 4-4 (5)). The ohmic access height is leveled with Schottky contact height. All around the mesa a wide trench is etched with $H_2O_2{:}H_3PO_4{:}H_2o$ solution with 4-8 µm for isolating

the diode (Figure 4-4 (6)). The diodes are connected to the circuit by two air-bridges. In order to build the bridges over the trenches first they need to be planarized to support the bridges during the process. The planarization process is explained in chapter 4 in detail. The presented process is done by using multi layers of PMMA resist and thick SHIPLY as cover layer which has partly planarization feature (Figure 4-4 (7)). The SHIPLY is patterned to cover just the mesa and trenches areas. Then, the stacked-up resist is etched back by plasma oxygen until the surface of Schottky contact, ohmic access and connection lines appear (Figure 4-4 (8)). The air-bridges are built over the planarized trenches by a ($Ti{:}Au$) thermal evaporation and lift-off process (Figure 4-4 (9)). Finally, the connection lines are thermally evaporated and patterned by a lift-off process (Figure 4-4 (10)). The process is schematically demonstrated in Figure 4-4. Also, the SEM image is shown in Figure 4-3 of the fabricated diode by using this process.


1
Mesa etching
Mesa
GaAs substrate
2
Ohmic contact
Thermal evaporation – lift-off
3
Isolation oxide layer
PECVD
4
Schottky contact
Surface treatment – thermal evaporation – lift-off
5
Ohmic access
Thermal evaporation – lift-off
6
Trenches
Wet etch

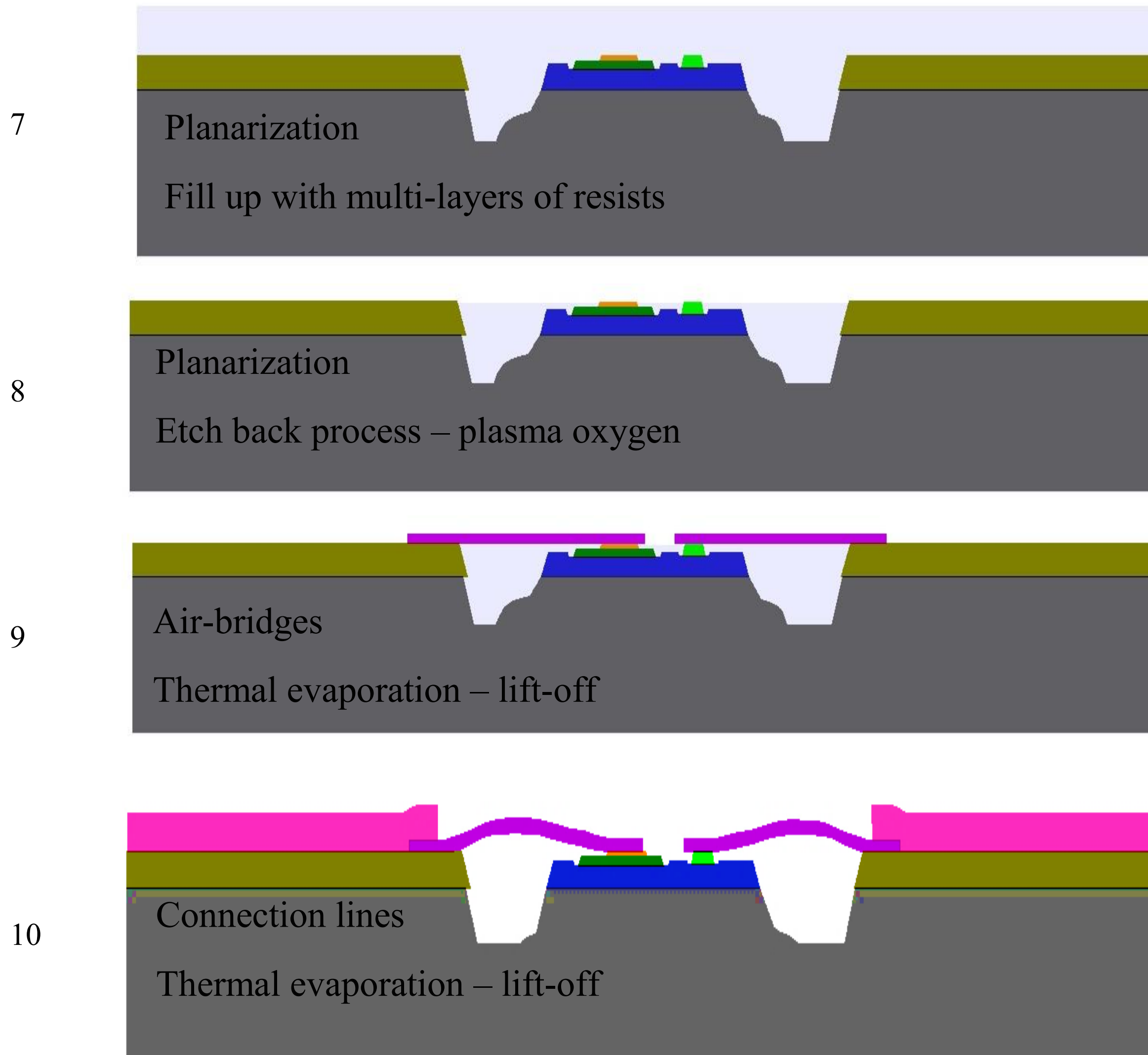
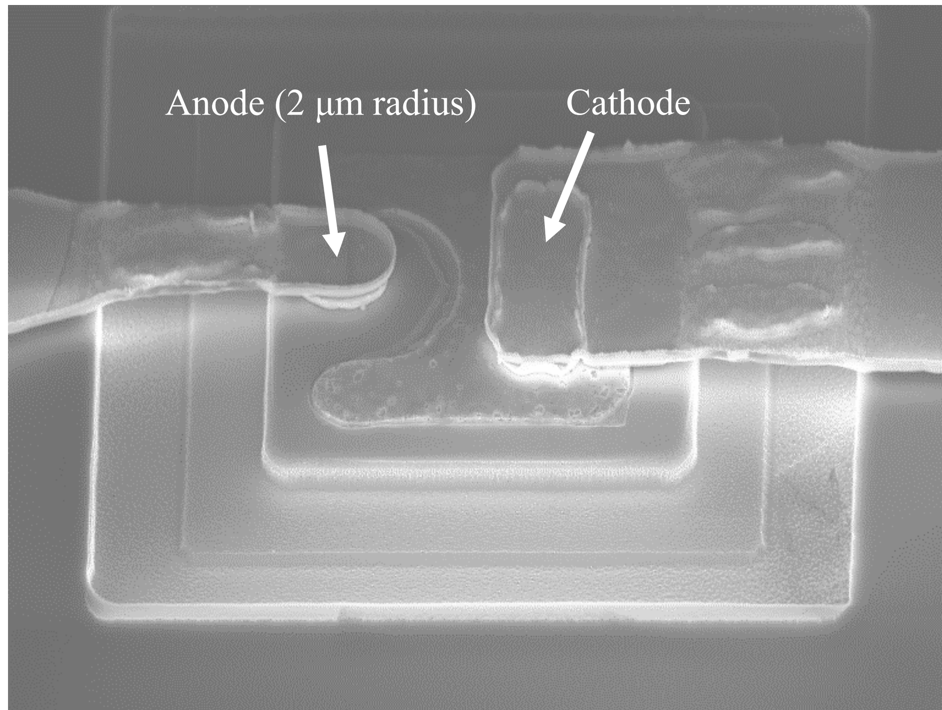
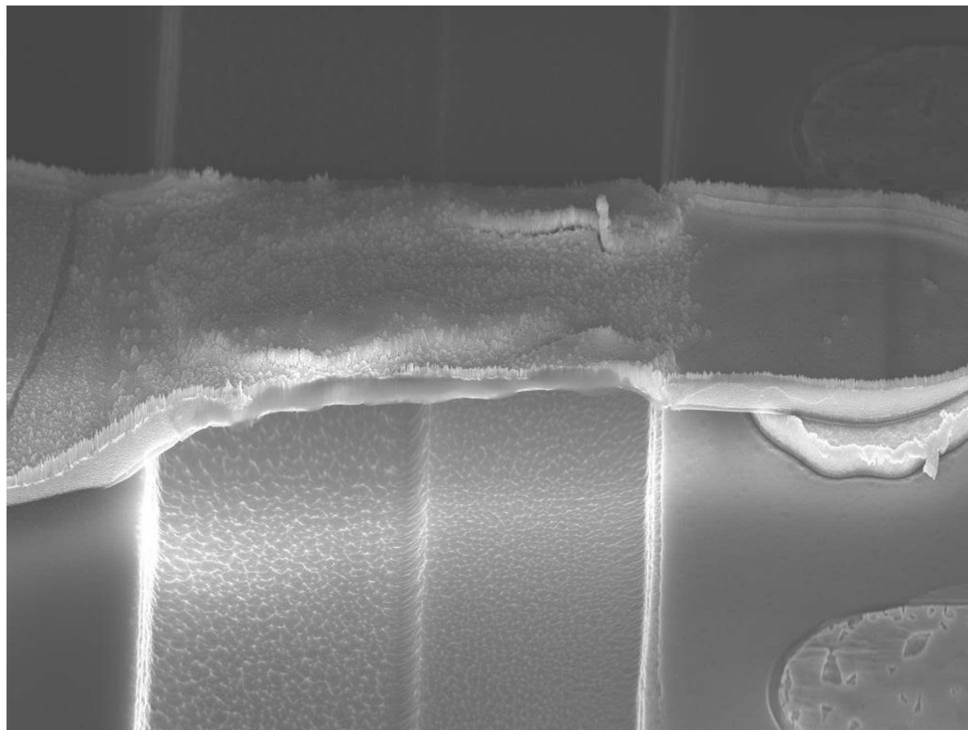


Figure 4-4 Schematic explanation of the diode primary fabrication process.



(a)



(b)

Figure 4-5 SEM image of the fabricated diode by the Multi-SM process, (a) The diode view, (b) Anode finger zoom in.

4.6 Double-SM process (final)

The presented Multi-SM process was modified to a more reliable, repeatable, flexible, cost effective, and easier process. The number of thick Gold (Au) metallization steps is reduced from four in the Multi-SM to only one in the Double-SM. The total number of metallization steps in the modified method is two, one for the Ohmic contact that needs to be annealed, and a second one for the all other metallic parts (including the anode contact, air-bridges, Ohmic access pad, and transmission lines). Reducing the number of steps also reduces the complexity of the process and amount of required lithography and alignment. The stand-off height of the bridges from the mesa level (h), which is an important parameter in this work, in the Multi-SM depends on the etch-back stop point of the planarization process, which makes it very critical with the identical height being hard to replicate every time. In the Double-SM, the stand-off height is completely independent of the planarization process. It is as easy as coating a resist with the desired thickness.

The first difference is the trench etching which needed to be done prior to the Schottky metal deposit. The trench is planarized with a polymer and with a single lift-off step the anode Schottky metal, the air bridges and the transmission lines are formed. In the following sub-sections the key elements of this process is described and discussed.

4.6.1 Planarization method

The idea is to fill the trenches with one resist (so-called filling resist), but not necessarily resulting in a planarizing feature. Then, a second resist with a partially planarized capability (which exist in most resists) is applied on top (so-called cover resist). The filling resist should not be affected by the cover resist developer and the filling resist should have higher temperature tolerance. Also, the filling resist should have a higher etch rate than the cover resist for the etch-back.

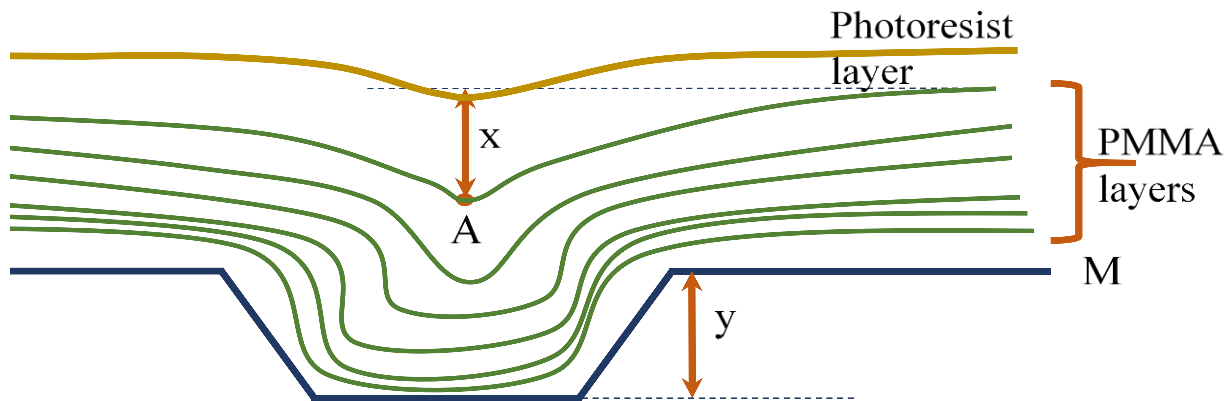


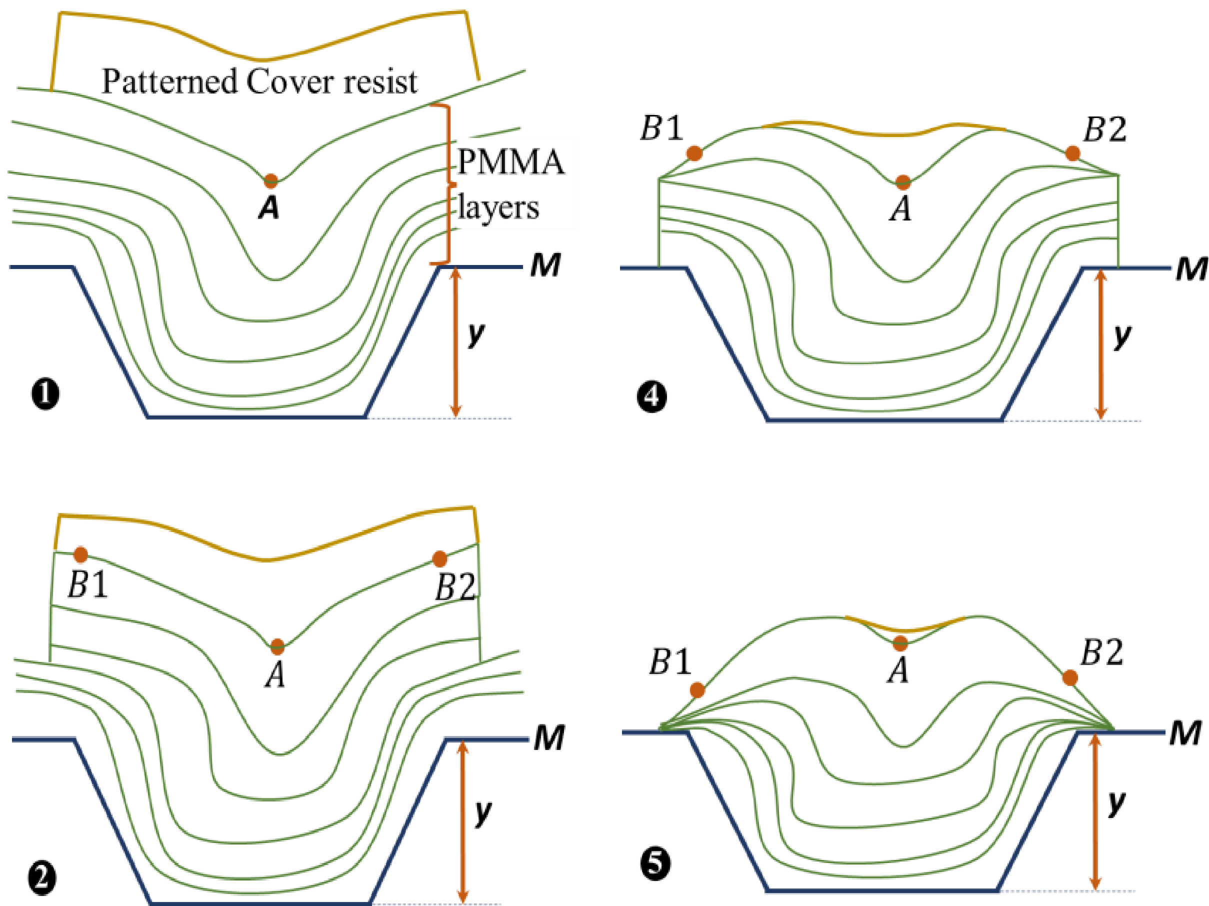
Figure 4-6. Trench filled by coating several layer of PMMA and covered by thick photoresist. The green lines illustrate the multiple layers of PMMA gradually filling and partially planarizing the trench.

Initially, the trench is filled with multiple layers of PMMA. It is found that it is beneficial to use lower PMMA-to-solvent density layers initially and gradually move to higher density PMMA afterwards. The number of layers depends on the depth of the trenches and the PMMA densities. This step is completed when the level of PMMA at the center of the trench (A) is higher than the mesa (M) as shown in Figure 4-6. The gradually filling and partially planarization of the trench is also illustrated in Figure 4-6.

A thick resist is then spun over the PMMA and patterned to remain only over the trench, as shown in Figure 4-7 (1). This "cover resist" should be thick enough, depending on the trench depth, to be able to obtain a sufficiently flat top surface, as is shown in Figure 4-7. In this work, a positive resist SHIPLEY-series 18 and a negative one AZ-nLOF 2020 are successfully tested.

The planarization process continues by etching back the resist in an oxygen plasma. Figure 4-7 illustrates the process considering that the cover resist etch rate is lower than the filling PMMA resist (e.g. SHIPLEY etch rate is 3-4 times slower). During the etching process points, B1 and B2 are reaching the PMMA faster than point A (Figure 4-7(3)). Since the etch rate of PMMA is much faster than cover resist, the level of points B1 and B2 are reduced faster than point A. So the combination of the cover resist thickness distribution, and its etching rate difference with the underneath resist forms the arch as is displayed in Figure 4-7 (6). The etch-back is completed when all surfaces of the sample, except the trench area, are cleaned of resist and the trench is only filled

with PMMA. Unlike the Multi-SM, this process is much less sensitive on the etching stop point since another resist will be spun over to form and support the air bridges and T-shaped anode as is described in Figure 4-9. The final profile of PMMA over the trench can be controlled by changing the cover-resist thickness and soft or hard baking it. The planarization method has tested positively for 1 to 8 μm deep trenches, which demonstrates the high degree of flexibility of the method.



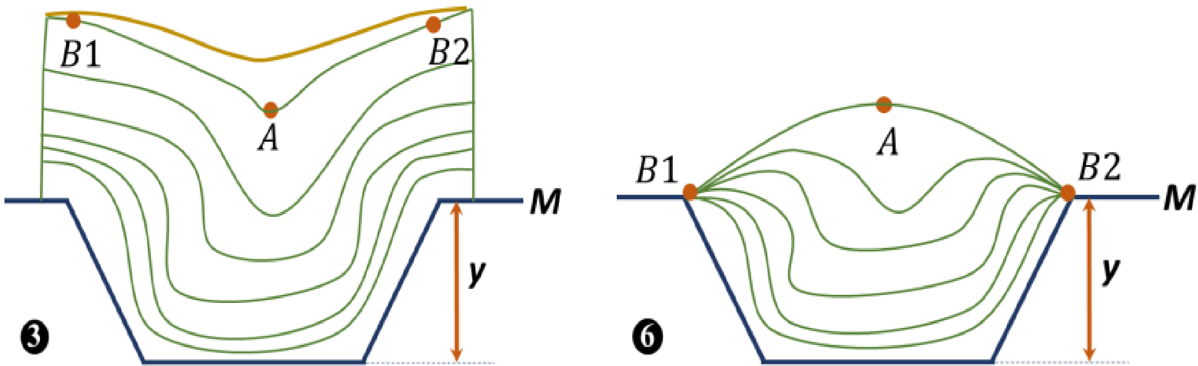
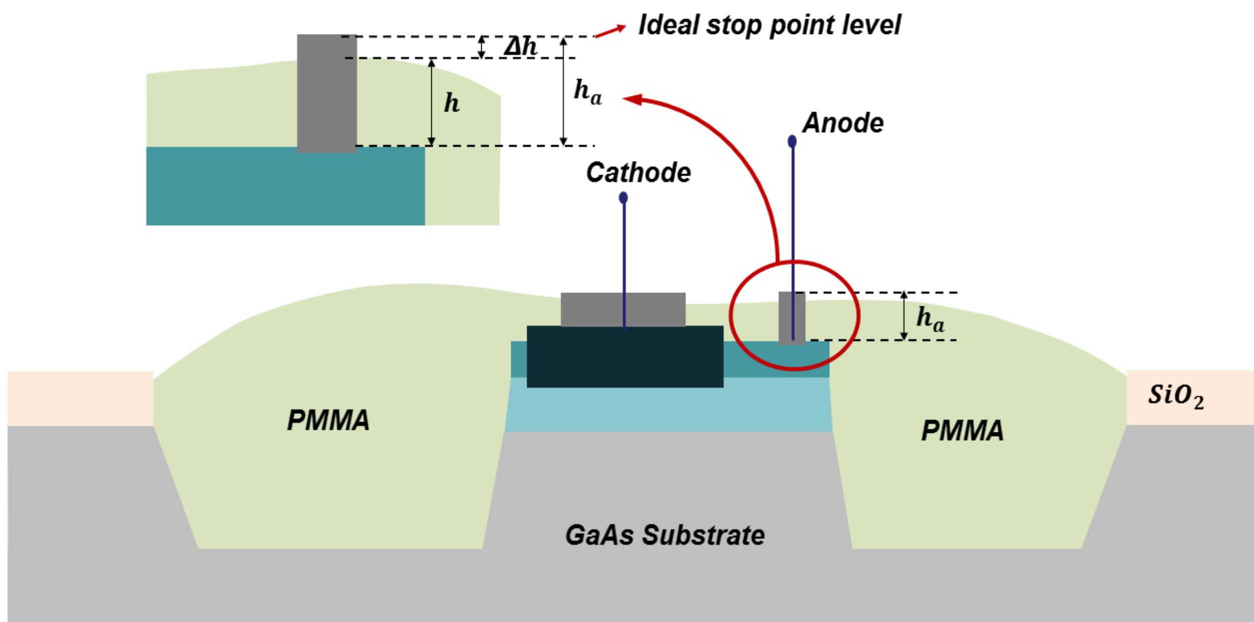


Figure 4-7. Planarization process: trench filled by coating several layer of PMMA and cover resist is patterned to remain just over the trenches. The resist surface transforms during the etching back process.

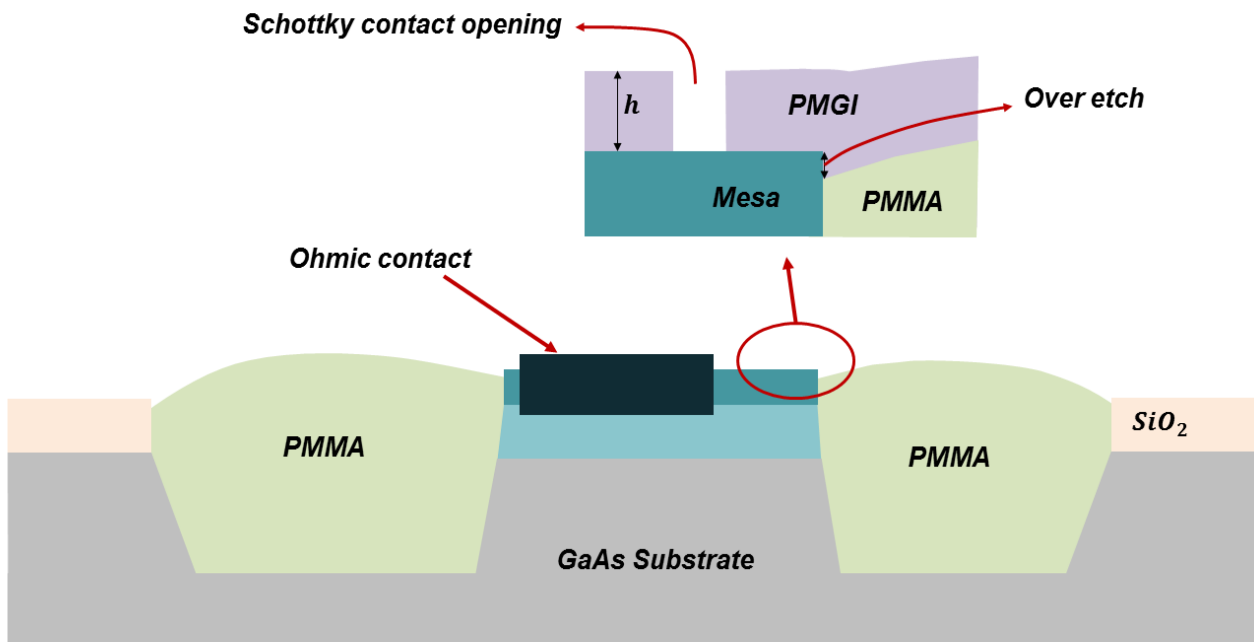
The difference between etch-back stop points (end points) in the two presented processes is illustrated in Figure 4-8. Ideal stop point in Multi-SM is achieved when the anode, ohmic-access, and SiO_2 surfaces are cleaned as is shown in Figure 4-8 (a). This process can tolerate over-etching error for the stop point. However, it cannot bear leftovers on the surface. Over etching height (Δh) defines the real anode contact stand-off height is,

$$h = h_a - \Delta h \tag{4-1}$$

where h_a is the contact stand-off height in the design, as is explained in Figure 4-8 (a). This can affect the diode parasitic capacitance and subsequently the diode performance.



(a)



(b)

Figure 4-8 The planarization etch-back stop point: (a) The Multi-SM process etch stop point effect on the diode structure, (b) The Double-SM process etch stop point effect is vanished by using a second resist (PMGI) on the planarized PMMA to support the air bridges.

The Double-SM etch-back stop point is reached when the mesa and oxide surfaces appear, as is shown in Figure 4-8 (b). This process can tolerate leftovers of planarization resist (PMMA) and its over etch from the stop point in the etch-back process. This is due to the fact that the planarization resist (PMMA) is only used to fill the trenches. Thereafter, another resist (PMGI) is coated over it to support the bridge and provide the stand-off (Figure 4-8 (b)). Therefore, the etch stop error toleration is as high as several hundred nanometers. Even if PMMA slightly remain over contacts or oxide surface, the leftover PMMA can be cleaned during the air-bridge process. On the other side, the over etch step will be smoothed out by coating PMGI over it.

4.6.2 T-shape contact and Air-bridge

After planarizing the trench, the T-shaped anode and air bridges are fabricated together in one step. Three layers stack of resists is used as described in Figure 4-9 to obtain the stand-off of the T-shape anode and the deep undercut required for the lift-off of a thick metal layer. First, the poly-methyl-glutar-imide (PMGI) is spun as the bottom layer. Its thickness determines the gap between air bridge and mesa surface (h in Figure 4-10). Since the PMGI exposure time is quite long, the height h can be controlled by partially flood exposing (without mask) of the PMGI layer. This enables spinning thicker resist over the planarized PMMA which decreases the process sensitivity to the etch-back stop point. Using the above method, the thickness of PMGI is reduced to 1 μm (from initial value of 1.5-2 μm). Afterward, it is patterned by using deep-UV for the anode, the Ohmic contact and transmission lines. Alternatively, electron-beam lithography could be used to pattern very small anodes (smaller than 1μm anode dimension) in PMGI, and deep-UV lithography used for the Ohmic contact and transmission lines. The undercut (middle) layer and top SHIPLEY resist are spun over the PMGI and patterned to form the air bridges and transmission lines. The important point about the choice of undercut layers is that its developer should not affect the bottom PMGI layer.

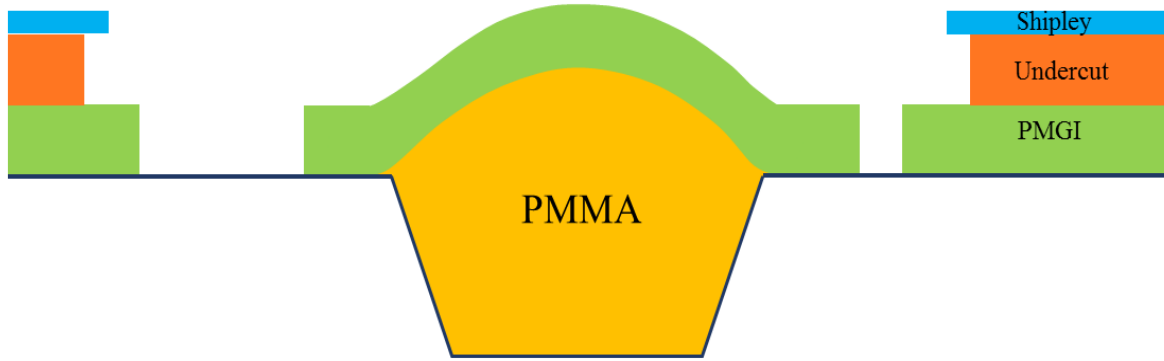


Figure 4-9. Three layers resist process to make a T-shaped contact bridge.

Before metalizing the anode and bridges, surface cleaning and passivation is required to avoid Fermi level pinning. To do so, a Ti/Au is deposited to reach a total thickness of larger than the PMGI layer. Then, the lift-off reveals the Schottky contact (anode), air bridges, transmission lines and other part of circuit simultaneously.

The SEM image of the final device is shown in Figure 4-10. The trenches depth in this case is 6 µm, the anode air bridge is 30 µm long, and mesa area is 24µm × 27µm. The T-shaped anode gap (h in Figure 4-10) is 1 µm. The double-SM process has less metallization steps and fewer lithography and alignment steps. The multi-SM process has 8 lithography and 5 metallization steps while the double-SM has 5 lithography and 2 metallization steps.

The use of PMGI allows fabrication of tall neck T-shaped anodes as illustrated in Figure 4-10. The height of neck is taller than the previously reported results. In most other works this gap is less than 300 nm and sometimes partially or completely filled with a dielectric. Our approach reduces significantly the parasitic capacitance. Also, series resistance and inductance decrease due to the air-bridge cross section area. The proposed fabrication method therefore allows fabrication of larger anode areas with the same cut-off frequency. Moreover, by using electron-beam lithography to reduce the anode size, these devices could efficiently reach higher cut-off frequencies since the PMGI resist that is used for opening the contacts is also sensitive to E-beam. To do so, in the mask design the anode opening should be on a separate mask which is design for E-beam lithography.

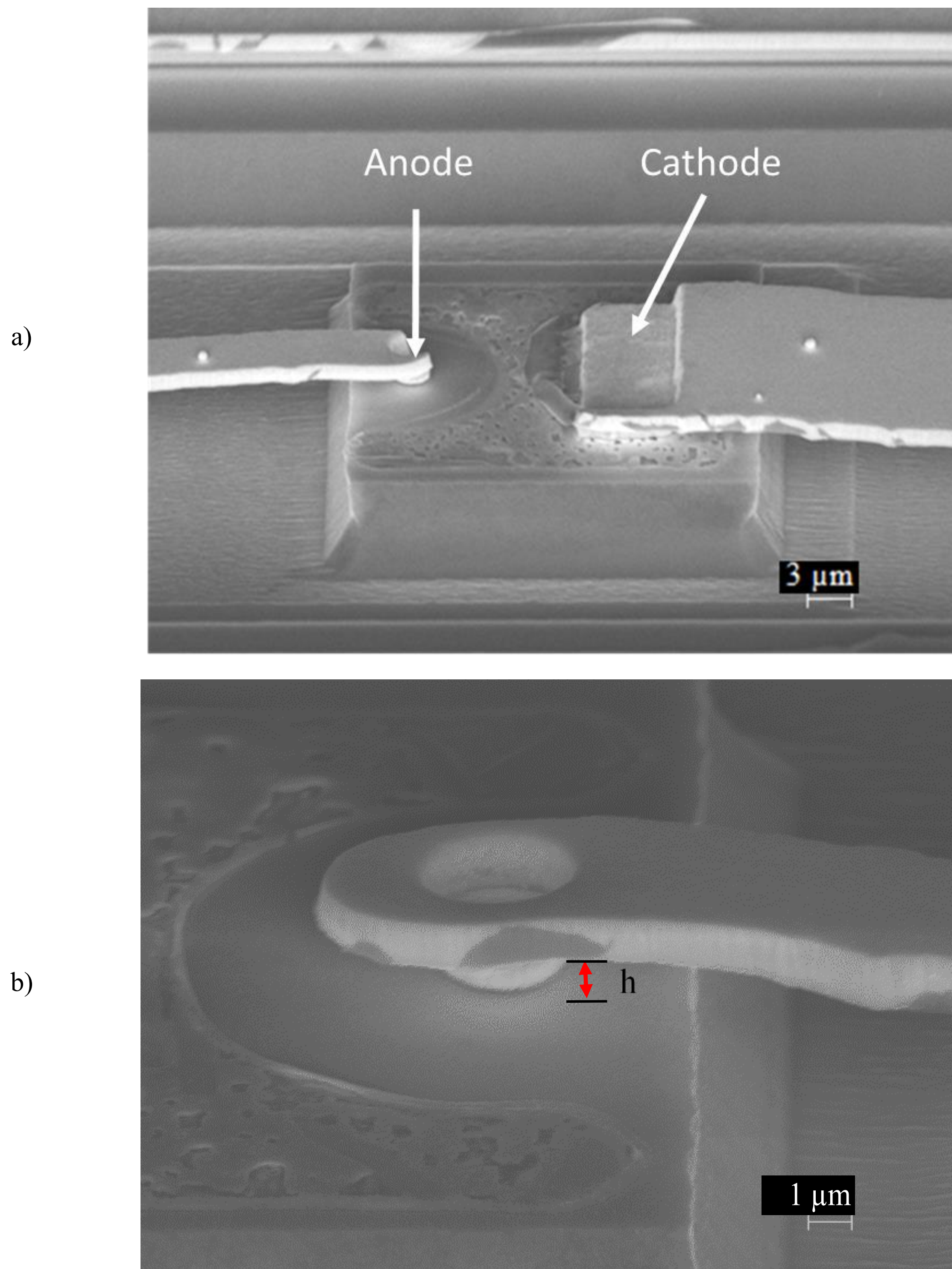
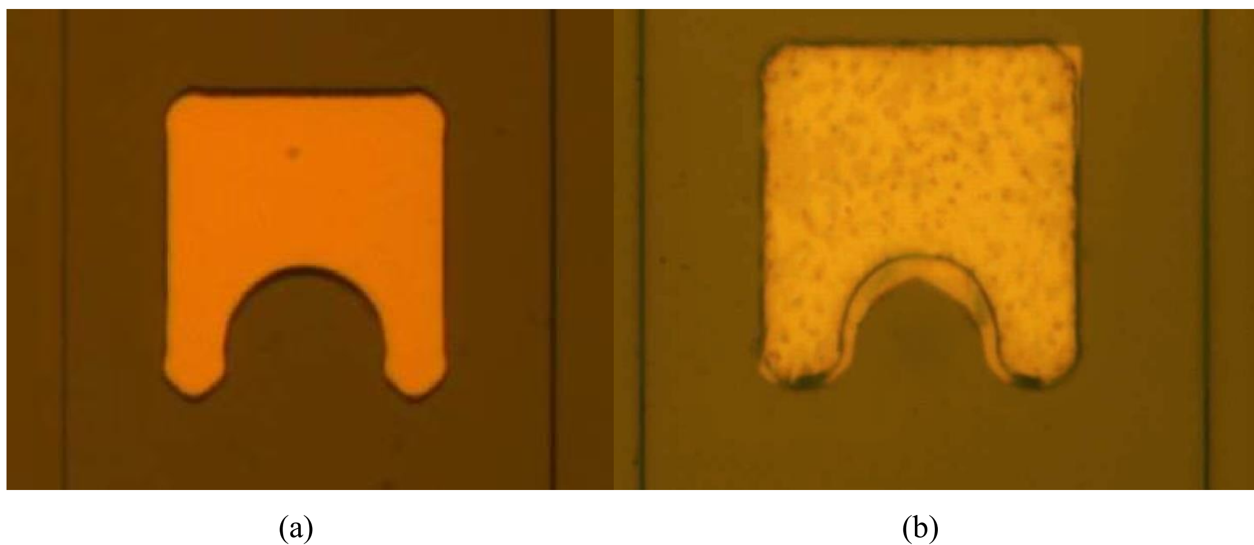


Figure 4-10 SEM images of diodes fabricated with the double-SM method. a) Global view of the mesa, Schottky and Ohmic contacts. b) Anode region with the stand-off height indicated.

4.7 Challenges

4.7.1 Ohmic contact annealing

One of our challenges was in the ohmic contact process, because the process of annealing the Ohmic metal, the contact shape (especially in the corners and curves edges) deformed due to the spread of the melted metal. This issue is shown in Figure 4-11 where (a) and (b) are the metallized Ohmic contact before and after annealing, respectively. In order to solve this problem, the order of evaporated metals were modified from $Ni/Ge/Au/Ni/Au$ to $Ge/Au/Ni/Au$.



(a) (b)

Figure 4-11 The ohmic contact annealing issue, The contact metals $Ni/Ge/Au/Ni/Au$ are thermally evaporated, (a) before annealing (b) after annealing.

This deformation issue was due to the fact that nickel impose a delay on germanium diffusion into GaAs, and this delay makes the top gold layer melt and deform. Therefore, we removed the bottom layer nickel from the metal evaporation order that facilitate the diffusion of germanium into the GaAs wafer. Removing the bottom nickel also caused more and deeper metal diffusion that provide less contact resistance. Also, the top gold layer thickness was reduced to avoid the deformation. The annealed contact after process modification is shown in Figure 4-12.

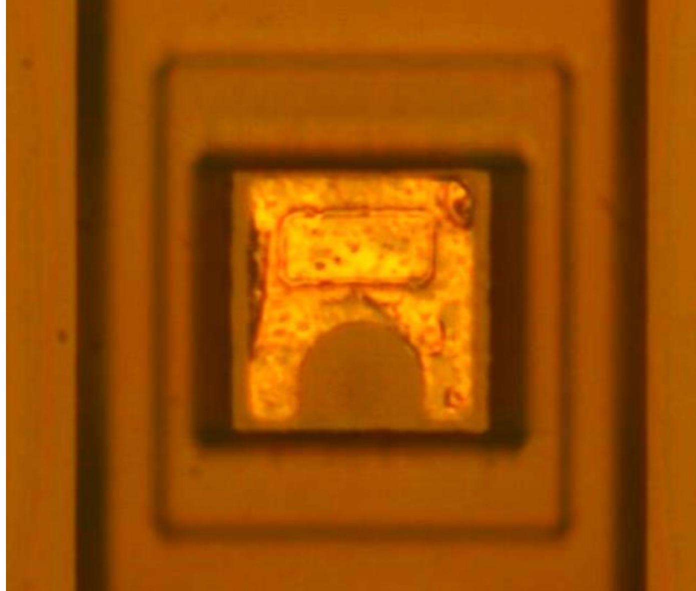


Figure 4-12 The modified ohmic contact after annealing. The contact metals $Ge/Au/Ni/Au$ are thermally evaporated.

4.7.2 Trenches etching

In the masks design, the distance between the opening border of the trench and ohmic contact is designed around 5 μm. This margin enabled us to use wet etching instead of dry etching which had been considered at initial process design. Wet etching is easier, faster and more cost effective than dry etching of GaAs, because the isotropic nature of GaAs wet etching makes an undercut as is shown in Figure 4-13. The 5 μm margin will be partly added to the trench size, depend on the trench etching depth. Moreover, in the GaAs dry etch, the resist is bombarded and partially etched. Therefore, thicker resist is needed that also depends on the trench depth, imposing very tight limitations on the trench depth which are not tolerable. Also, the remaining resist becomes very firm, which makes the dry etching less favorable. The high energy plasma ions collision with the resist surface makes the resist harder to remove.

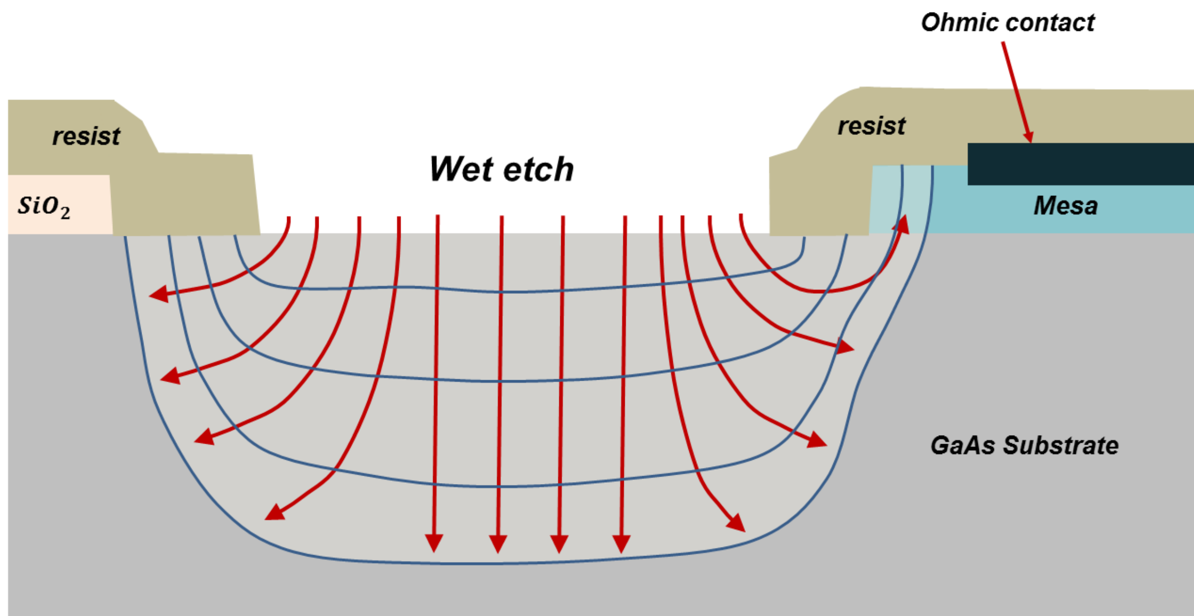


Figure 4-13 The wet etching process of the trenches.

4.7.3 Planarization challenges

Resist selection

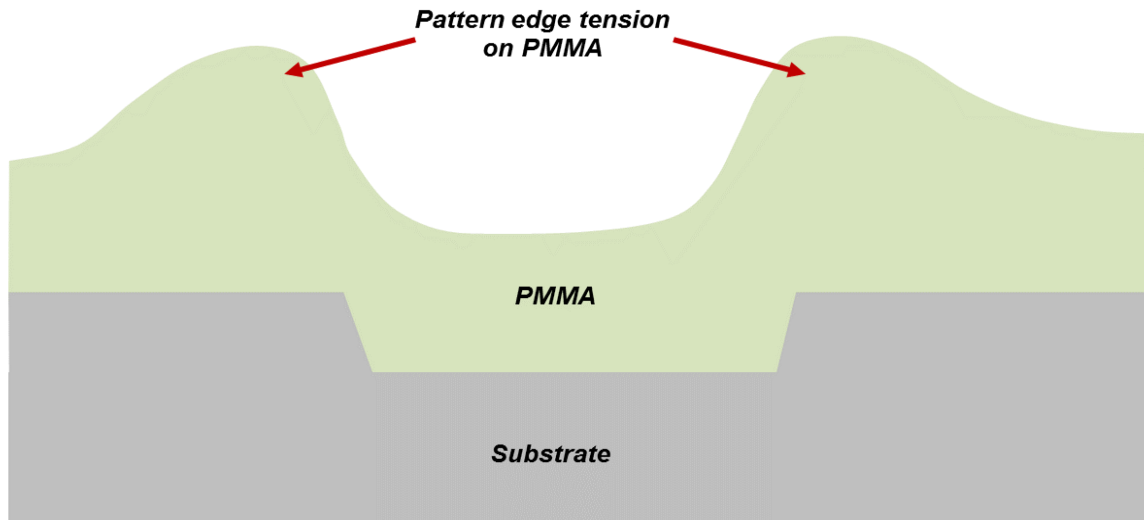
In order to develop the planarization process, several resist methods have been tested. First, an available planarization resist PC3-1500 was considered to fill the trench and make the surface planar, then etch it back and do the lithography at the presence of PC3 to build the bridge over it. Then a second resist which should be compatible with PC3 resist underneath was required. The problem with the PC3 was that it is washed away during the second resist coating. Several resist have tested, including LOR, PMGI, Shipley, Az9242, Az4903, PMMA, Durimide, KMPR, and NR4-8000. Thus, the PC3 was dropped and we tried to find another resist to fill up the trenches. For that, several resists were tested, including: Durimide and thick-PMMA which did not have planarization feature; KMPR which is hard to remove at the end and also cannot be put in plasma etcher; NR4-8000 and AZ(9245, 4903) which are also washed away by second layer coating; and the AZ series which also do not have the planarization feature.

Why PMMA?

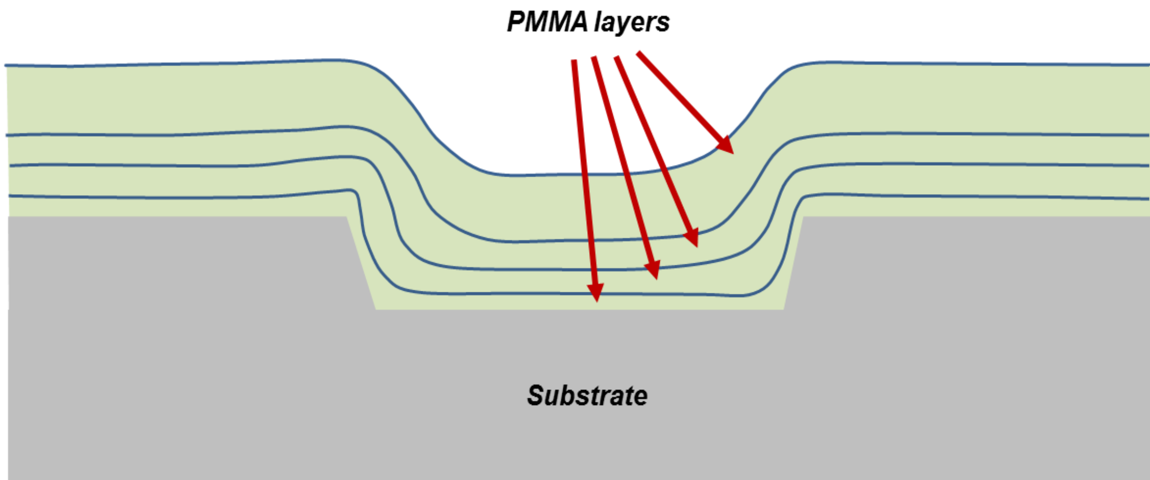
The Polymeric PMMA got our attention because:

- It is available in a large variety of thicknesses
- The possibility of having multilayers of this resist without the hard-baking requirement of previous layers
- The possibility of coating other resists over it, without any changes on the underneath PMMA.
- It is not affected by the MF-319 developer that we normally use for developing other resists in this process.
- It has higher temperature tolerance in comparison to the normal resists which may be use in the presence of PMMA underneath.

In the primary test we used a thick layer PMMA. The issue was that the viscose PMMA showed tensions by facing the sharp edges of deep patterns. As is shown in Figure 4-14 (a), the high viscose PMMA, caused bumps of resist around the sharp edges. Testing the more diluted PMMA showed that by reducing the viscosity of the resist, patterns edge tension is reduced. Therefore, we started with diluted PMMA which provided a thin layer, and continued coating several layers by increasing the viscosity of PMMA gradually as is shown in Figure 4-14 (b). This method solved the tension at the edge of deep trenches, and we were able to fill the trenches with PMMA layers. Although it wasn't completely planar, it reduced around 50% of the trench depth. The trenches are filled with PMMA when the downhill of the PMMA surface level is higher than the top of mesa level.



(a)



(b)

Figure 4-14 Spreading of PMMA over a trench (a) One thick layer that get extreme tension at the trench edges, (b) The multi layers start from thin to thicker layers.

Cover resist challenges

Now the trenches are filled but still we need to make it planar. Therefore, a second resist that has more a planarizing feature is required. Since the PMMA is not affected by developer MF319, we can do lithography on the top resist while there is PMMA underneath. So, a thick SHIPLEY (S1818) is coated over and patterned to cover only the mesa and the trenches area. As is shown in Figure 4-15, because the PMMA thickness on the flat area of the sample is thicker than on the

motif area (diode area), the SHIPLEY patterning is necessary. Figure 4-15 shows the surface profile of a cross section of a diode mesa in between two trenches measured by a Dektak profilometer. Therefore, if the cover SHIPLEY is not patterned, there is some left over PMMA on the flat surface at the desired etch stop point. This issue is shown in Figure 4-16. It shows a test sample after etch-back, namely that the cover SHIPLEY had not patterned before the etch-back process.

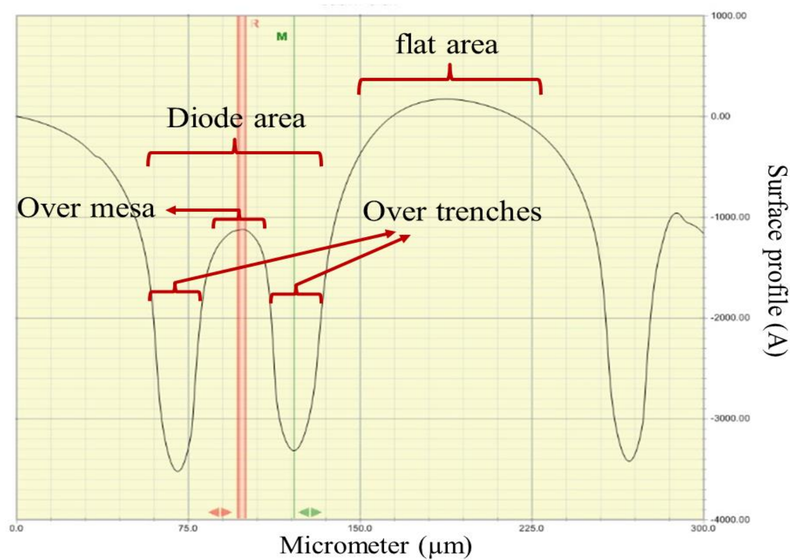


Figure 4-15 A cross section surface profile of the diode, when the trenches are filled by PMMA.

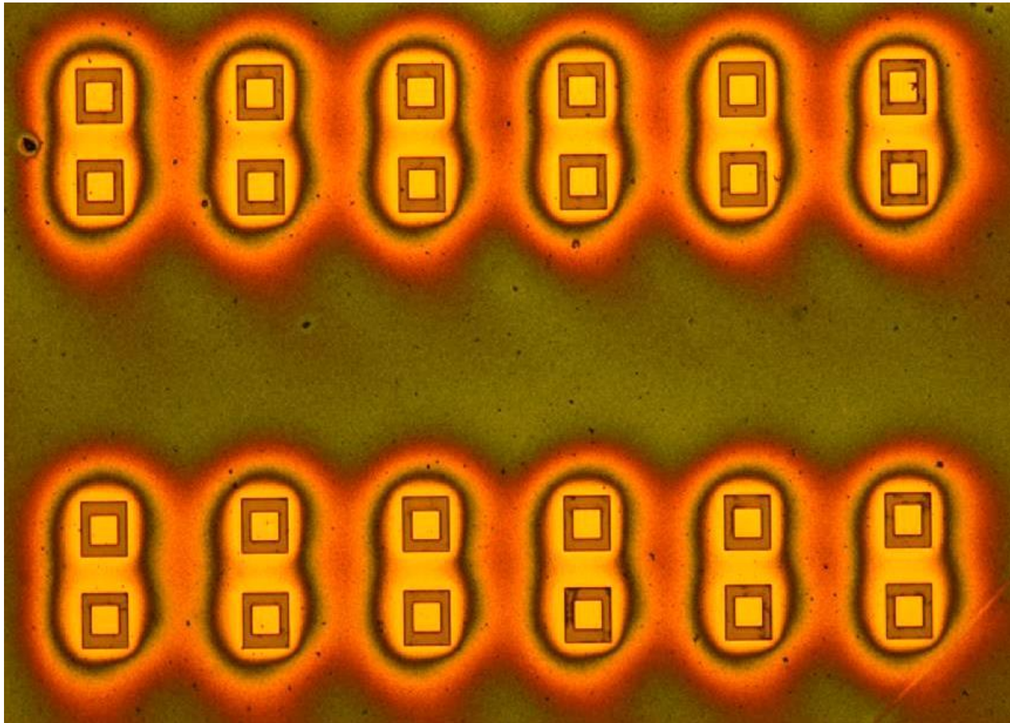


Figure 4-16 Optical microscope image of the test sample that planarized without patterning the cover SHIPLEY. The PMMA around the motifs (trenches) is cleaned by Plasma Oxygen etching, but there is left over PMMA on the flat areas.

Etch-back process

The resist dry etch is a combination of two different actions. The first one is due to the chemical etching by the oxygen, which happens in all direction, and the second is due to the collision of the high energy plasma ions and resist surface which is directional in the plasma direction. The effect of these two actions, is more important when the ICP etching system is considered. While developing the etch-back process with ICP etcher, we saw that when the plasma energy is high, the edges of the patterned resist are hardened by plasma-like walls remaining around the diode. Even by over etching the trenches, the resist walls still remain partly as shown in Figure 4-17. This issue is solved and the desired result achieved when the chemical etching in the chamber is dominant. The chemical etching dominancy, can be achieved by increasing the oxygen percentage and pressure in the chamber and at the same time by applying low plasma power and decreasing its horizontal directionality by tuning its parameters.

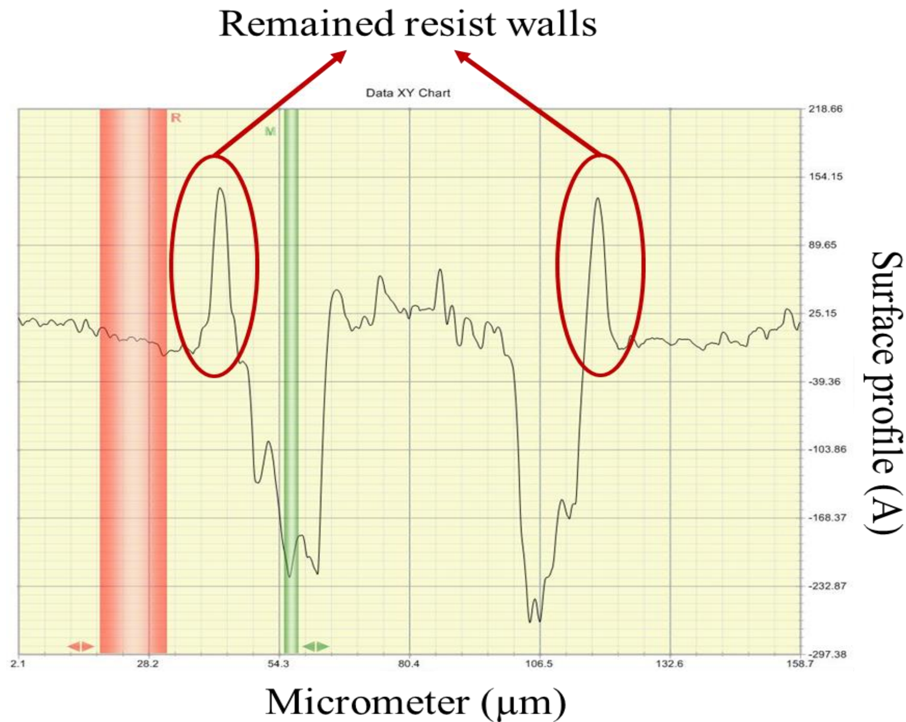
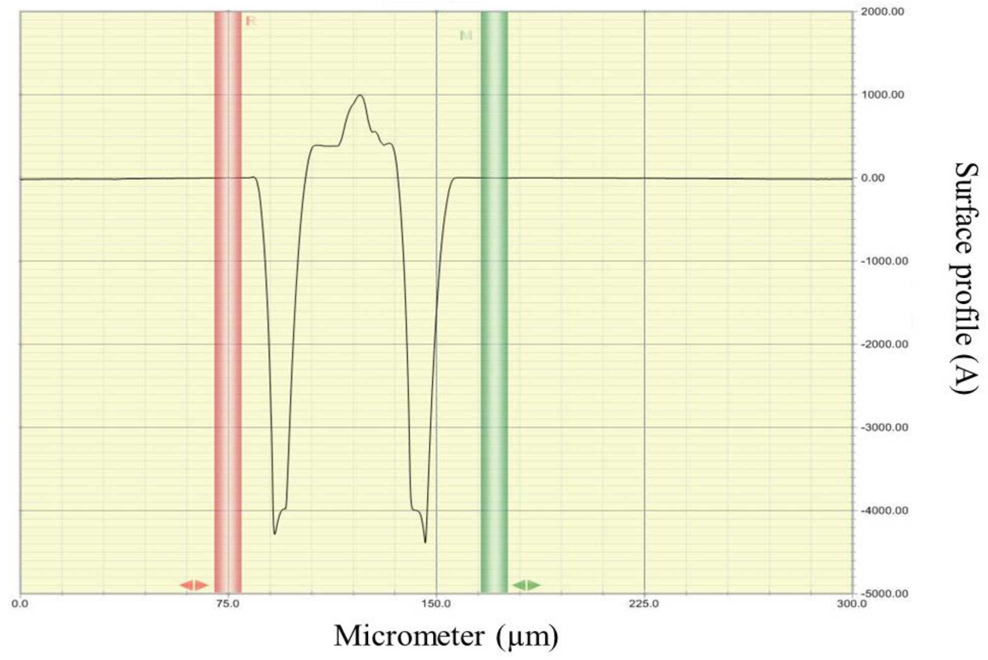


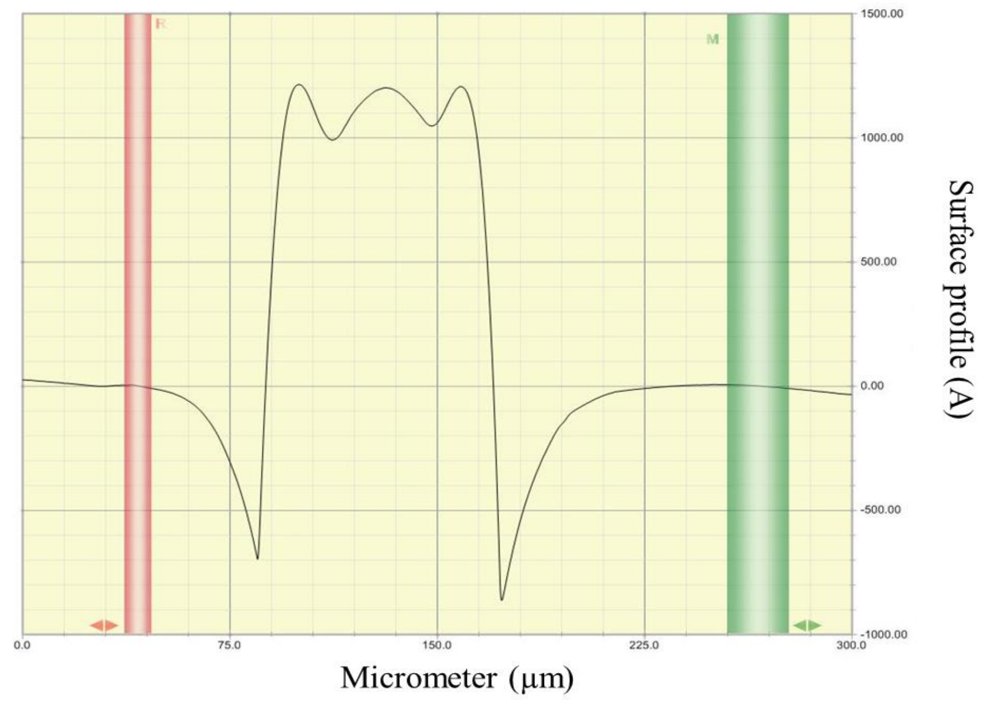
Figure 4-17. The stubborn resist walls at the edges of the resist pattern.

The PMMA etching tests shows that its etching rate by plasma-oxygen is significantly higher than the other resists like SHIPLEY that we have tested. By using this feature of PMMA, the planarization is completed as is explained in Figure 4-18 and chapter 4 in detail. Figure 4-18 shows the surface profile of the diode cross section before filling the trenches (a) when it is ready for etching-back (b), during the etch-back, (c) and after completing the etch-back (d). The profiles are measured by using a Dektak profilometer.

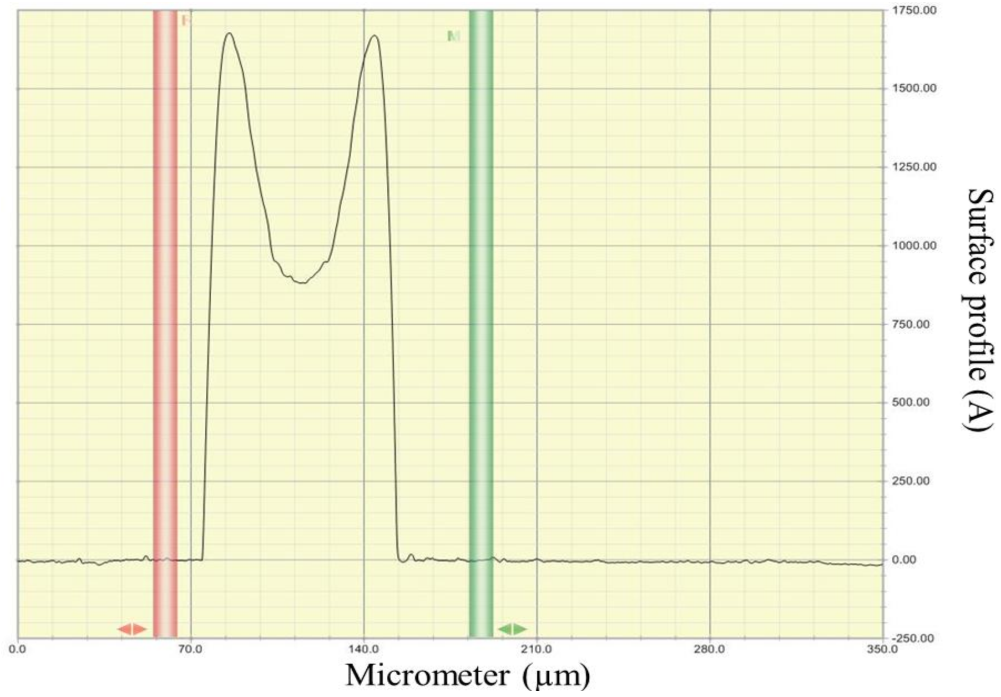
(a)



(b)



(c)



(d)

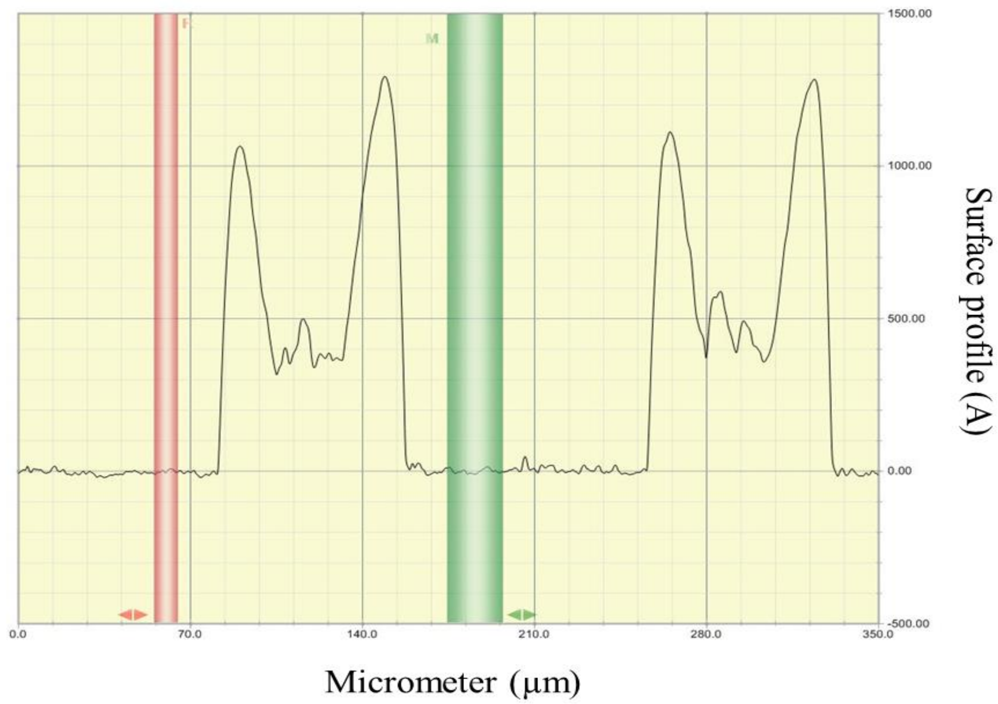


Figure 4-18. The diode cross section surface profile, measured by Dektak profilometer. (a) the empty trenches, (b) filled by PMMA, covered by SHPLEY 1818 and patterned (ready for etch-back), (c)in the half way of the etch-back process, and (d) after completed etch-back.

4.7.4 Air-bridges with T-shape contact

The UV based T-shape contact method

In Double-SM, the incorporated UV-lithography based T-shape contact and airbridge processes allow us to build all metallic parts in one lift-off process, except the Ohmic contact. For the T-shape contact a stack of three different resists is required. The bottom resist patterns the contacts, the second resist (middle one) provides an undercut gap for the lift-off process, and the top resist shapes the bridges. The selected resist for bottom layer, PMGI, is Deep-UV sensitive. Since in our lab we have a flood exposure Deep-UV system, a thin SHIPLEY employed as a hard mask to pattern the PMGI layer. The hard mask is removed during developing PMGI. Then the middle and top resists, PMMA and SHIPLEY respectively, are coated and patterned. The connection pads and transmission lines are on both contact and bridges masks to be fabricated in the same metallization step.

Developing the method and Challenges

First we tested the PMGI as the bottom layer, LOR as the middle layer, and SHIPLEY as the top layer. However, the problem was that LOR solvent affects the PMGI. Although the PMGI etching rate is much lower, it changes the opening size and thickness of PMGI. Since the bottom layer (PMGI) contains the anode opening, we cannot tolerate this change on the anode size and its finger stand-off. The SEM image of the sample that we used for this resists combination is shown in Figure 4-19. The anode contact size got larger and the stand-off was reduced significantly. Therefore, we changed the middle resist to PMMA, which has a different developer that does not affect the underneath PMGI. The SEM image of the fabricated diode by using the final process is shown in Figure 4-10, showing that the issue is perfectly solved.

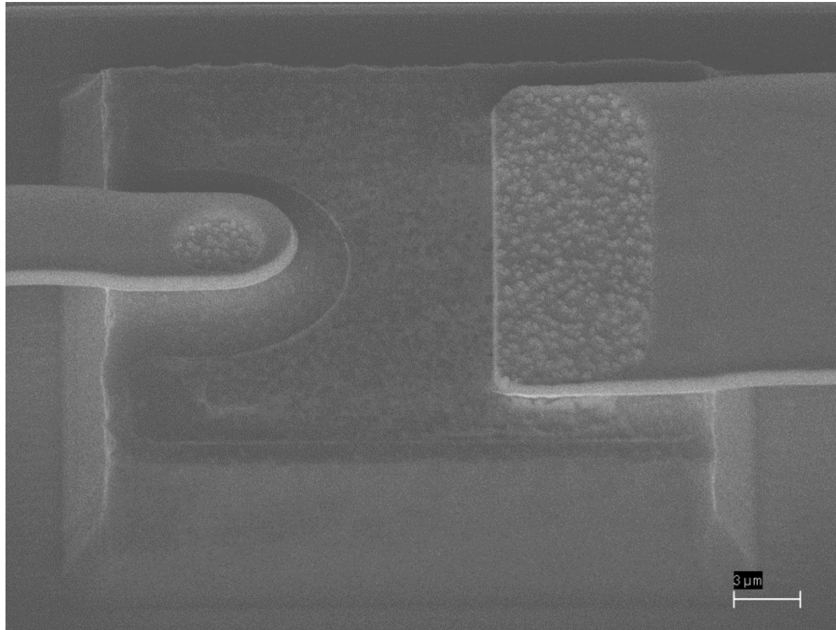


Figure 4-19. The SEM image of the sample that in the T-shape contact and air-bridge process, the LOR resist is used as the middle resist layer to provide the undercut.

4.8 Flip-chip diode

In order to use the developed diodes in different circuits, the easiest and best way is the flip-chip method. This means fabricating the diodes so that the cut will be to the individual diode. Then we can flip-chip the diodes on any circuit. In most circuits that we may consider for these diodes, the diode is the most critical part in the fabrication. By this method we don't need to provide a set of high precision expensive masks for each set up and circuit. Also by this method, we can fabricate circuits which are normally much larger in comparison to the diode size, on any desired substrate without wasting a large area of the expensive epitaxial structure GaAs wafer.

For that, we redesigned the mask set to include:

- Proper size contact pads
- Enough space for the dicing process
- The backside etching process for thinning the substrate
- The diodes can be all UV process and be able to substitute the anode opening with an E-beam process in order that a smaller anode area is needed

- Support for the additional steps for cutting the diodes

4.9 Conclusion

In this chapter, first the effect of Schottky layer thickness on the cut-off frequency of a diode, for direct detection and mixing applications, is studied and discussed. A submillimeter/THz diode is designed and simulated. Then, a novel microfabrication process is proposed and implemented. This process, in comparison with other reported researches, is less complicated and therefore is more cost effective and reliable. Most importantly, it provides more flexibility in the design and significantly decreases the parasitics of the diode. The tall neck T-shaped anode is fabricated by photolithography. Apart from the Ohmic contact that needs to be annealed, all other conductors, including the Schottky contact, are made by one lift-off step. A key part of the fabrication process is the planarization of the trench. We believe that the developed method is more reliable due to its high tolerance to process etch back end point. The measured DC and RF characteristics of the diode and extracted parameters are presented in chapter 5.

5 Characterization and measurement

With the goal of minimizing the parasitic capacitance, we have presented a new microfabrication process that allows more flexibility in choosing the design parameters. Here we present measurement results that confirm the new fabrication method's benefits, and conclude by estimating the cut-off frequency of our diodes and various performances indicators.

The most important parameters in the diode characterization, used to model and describe the diode behavior, are as follows;

- Saturation Current (I_s)
- Ideality factor (η)
- Barrier height (φ_B)
- Series resistance (R_s)
- Junction resistance (R_j)
- Junction capacitance (C_j) / Total capacitance (C_T)

These parameters define the diode and are required to calculate the diode cut-off frequency, responsivity, and noise equivalent power (NEP). They can also be used to describe diode frequency behavior depending on the application. In order to achieve to these parameters, we did some DC and RF measurements.

The design and fabrication process of the diode using an HBT GaAs wafer and with anode radius of 1 to 2 µm was presented in previous chapters. The measurement results, setups, characterization methods, and parameters extraction methods are described in this chapter. In the fabricated diodes, the trenches width (d_{pp}) is 17-20 µm, the anode and cathode distance (b) is 5 µm, and the anode finger stand-off (h) is 0.9-1 µm, which are the parameters shown in Figure 3-2.

5.1 DC setup, current-voltage (I-V) measurement

The most important and common characteristic of a diode is the DC current-voltage curve (I-V). Several parameters of the diode can be extracted from this curve. For this measurement, our setup includes a Keithley 4200 semiconductor characterization system, a four probe station, and the diode with two connection pads as is shown in Figure 5-1. The four probe configuration is considered as a consequence of subtracting the cable and connector resistance. The measurement results are presented in chapter 3.

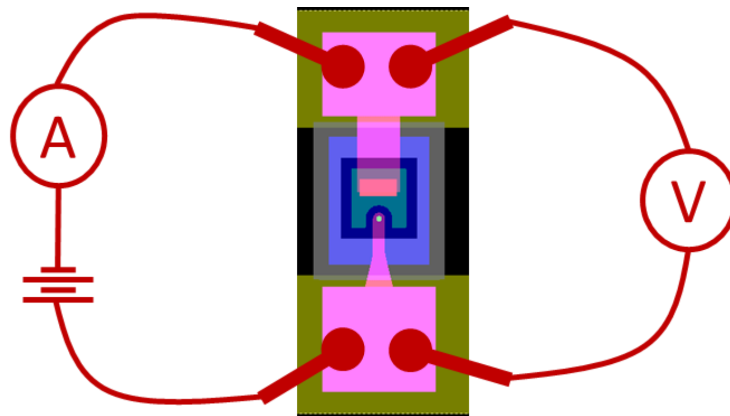


Figure 5-1. Four probe I-V measurement setup.

5.1.1 Saturation current

The saturation current I_S of the diode can be extracted directly from the measured I-V curve. It is defined as the intersection of the diode current line extrapolation in logarithmic scale, when it is in the diffusion current range. The I_S extraction of the fabricated diode is shown in Figure 5-2.

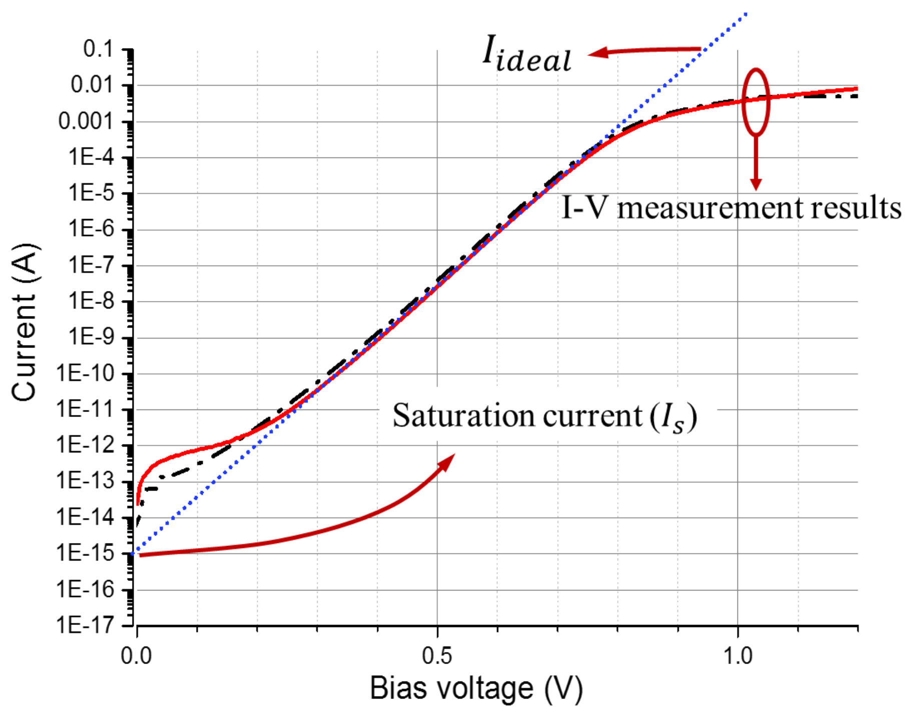


Figure 5-2. The extraction of the saturation current from the measured I-V curve.

5.1.2 Ideality factor

The diode current, when $V \gg V_T$ and it is far from the linear part of current ($V \gg IR_s$), is due to the diffusion process:

$$I = I_s(exp(qV/\eta kT) - 1) \tag{5-1}$$

where I_s is the saturation current, η is the ideality factor, and V is the voltage bias of the diode. So the ideality factor is determined by:

$$\eta = \frac{V}{V_T \ln \frac{I}{I_s}} \tag{5-2}$$

By using the measured current and Eq. (5-2) we can extract the ideality factor of the fabricated diode. The result for the fabricated diode is shown in Figure 5-3.

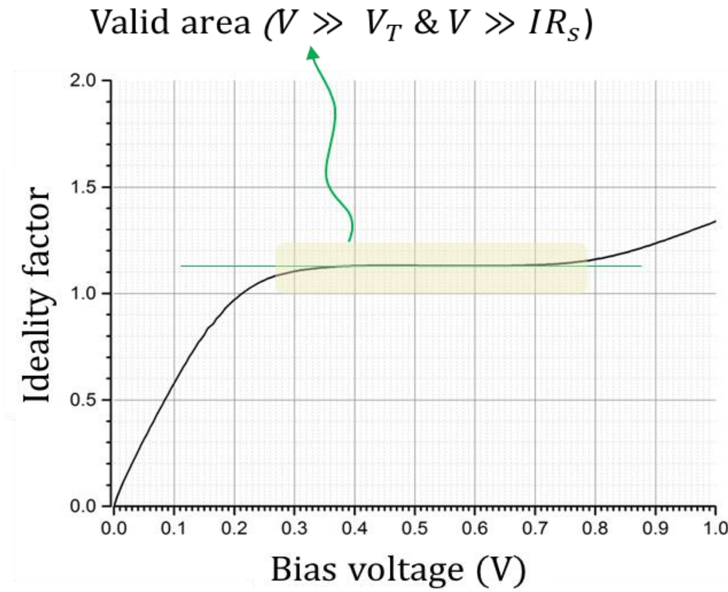


Figure 5-3. The extracted ideality factor from the measured current of the fabricated diode by using Eq. (5-2).

5.1.3 Barrier height

The Barrier height can be obtained by having the diode I-V curve and saturation current since:

$$I_s = AR^*T^2 exp(-q\varphi_{BN}/kT) \tag{5-3}$$

where A is the anode contact area, R^* is the Richardson constant, and φ_{BN} is the Barrier height. Therefore, the barrier height is obtained by:

$$\varphi_B = -V_T \ln \frac{I_s}{AR^*T^2} \tag{5-4}$$

The initial amount of the Richardson constant R^* can be extracted from literature. The extracted saturation current I_s, and ideality factor η from measurement are applied in the developed analytical model in this work to obtain the diode Richardson constant R^* and subsequently the Barrier height φ_B, by fitting the I-V curve of the model with the measured I-V curve.

5.1.4 Junction resistance

The diode junction resistance R_j is defined as:

$$R_j = \frac{1}{\left({}^{\partial I}/_{\partial V_j} \right)} \tag{5-5}$$

In Figure 5-4 the extracted junction resistance is shown for one of the fabricated diodes by using Eq. (5-5) and the measured I-V curve. As it is apparent in Figure 5-4, the R_j reduction is limited at high current regime due to effect of series resistance increase.

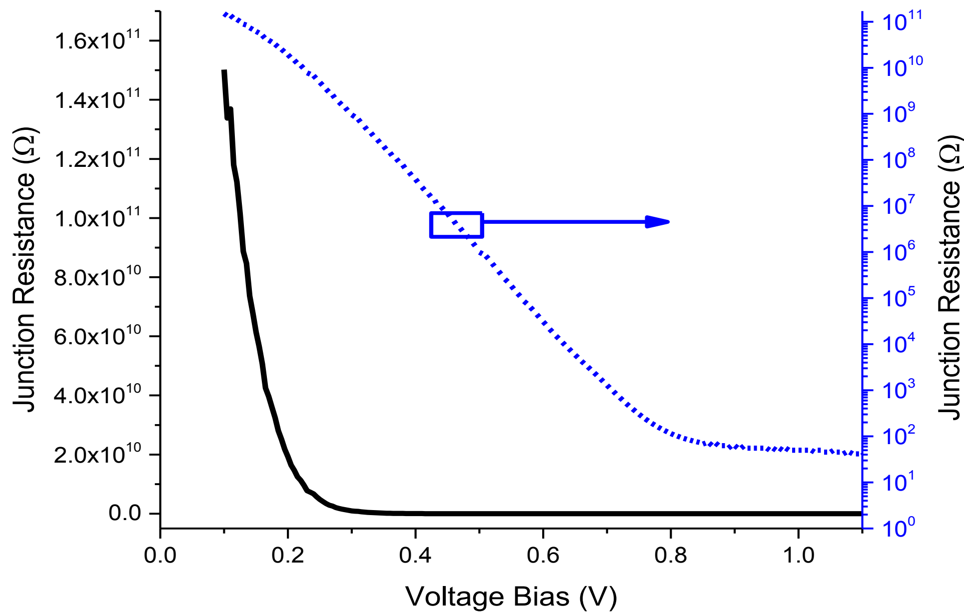


Figure 5-4 The junction resistance R_j of the fabricated diode extracted from measured I-V curve.

5.1.5 Series resistance

In order to extract the series resistance R_s two methods are employed.

I-V curve slope

In this method, the series resistance R_s is directly extracted from the measured I-V curve. At the high forward bias current, where R_j gets significantly low and most part of the voltage bias is higher than the series resistance, the I-V curve slope can give us the approximate series resistance of the diode. Figure 5-5 explains the extraction of series resistance by using the measured I-V curve slope for a diode with 2 μm radius anode.

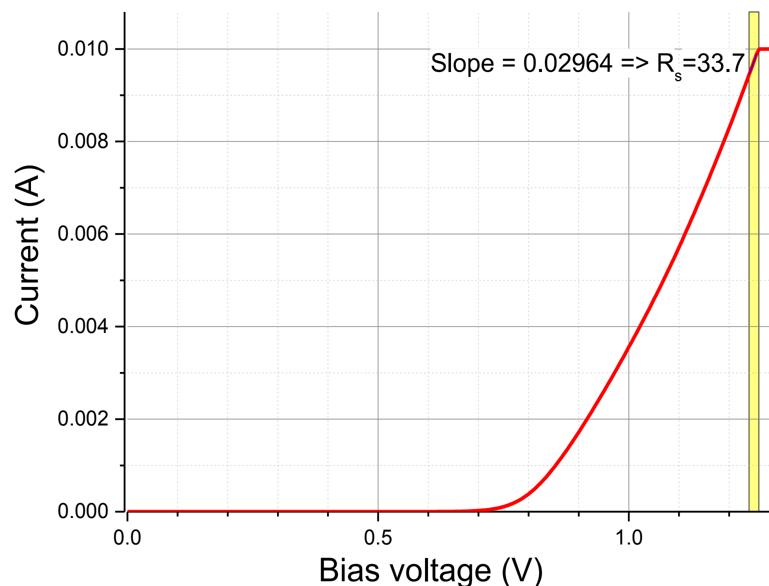


Figure 5-5 Measured I-V curve of a 2 μm radius anode diode and the series resistance extraction from the slope of the curve at its high current regime which is almost resistive.

Current deviation

In this method, the series resistance R_s of the diode is obtained by considering its effect on the current slope by increasing the bias voltage at forward bias regime. By increasing the bias and subsequently the current of the diode the voltage drop on the series resistance increase. It makes a deviation on the current curve from the ideal diode and its current is obtained from Eq. (5-1). This current deviation from the ideal diode current is shown in Figure 5-2. This deviation obtains by finding the voltage difference (ΔV) for each current value (I_m=I_i). The dropped voltage (ΔV) is due to the series resistance as shown in Figure 5-6.

$$\text{For } (I_m = I_i){:}\ log\, I_i = aV_i + b = log\, I_m \ \rightarrow\ V_i = \frac{log\, I_m - b}{a}$$
$$\Delta V = V_m - V_i = V_m - \frac{\log I_m - b}{a} \qquad (5\text{-}6)$$

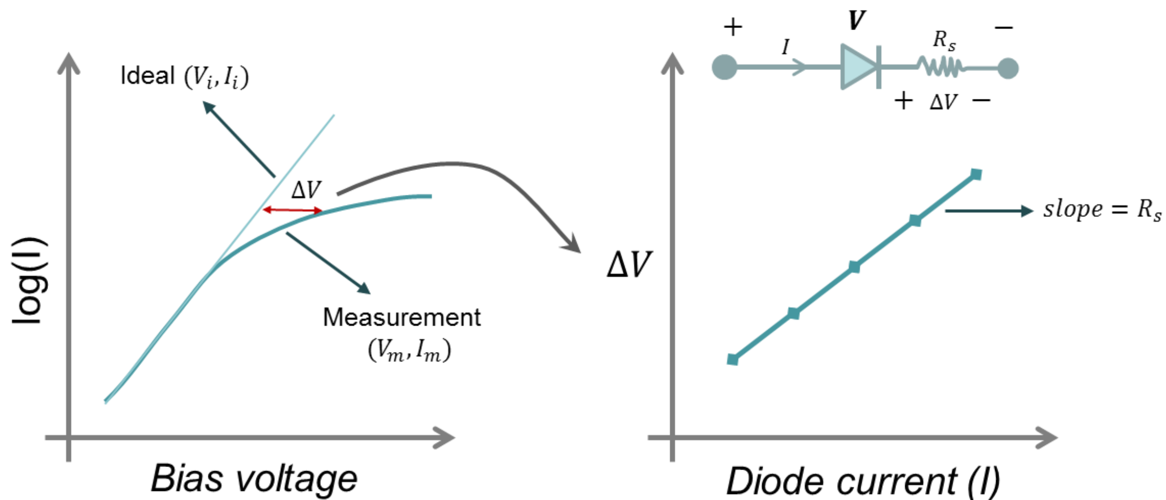


Figure 5-6 The current deviation method for extraction of the diode series resistance R_s.

Figure 5-6 explains the extraction method of series resistance by using the high forward bias current-deviation from the ideal current line of the diode. The result for a 2 µm radius anode diode is presented in Figure 5-7. The series resistance of the diode with 2 µm radius anode is 30 Ω by

using the measured I-V and deviation-current method. This method is more accurate than the previous method, which is the I-V curve slope.

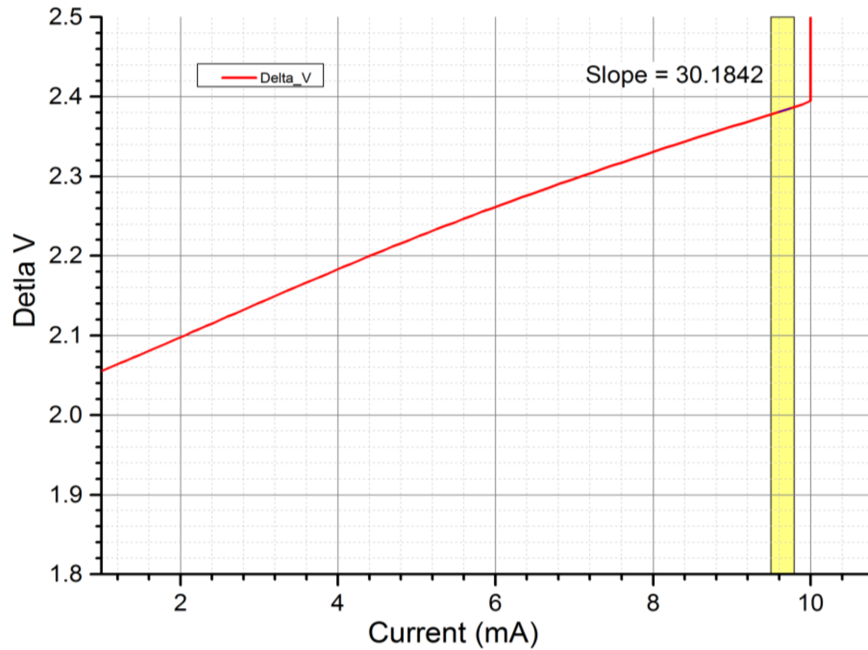


Figure 5-7 The diagram of voltage delta ΔV as function of measured current for the fabricated diode with 2 μm radius anode.

5.1.6 DC Measurement results

The fabricated diodes have d_{pp} of 17-20 μm, b of 5 μm and h of 0.9 μm (parameters are shown in Figure 3-2 (b)). The most important and common characteristic of a diode is its DC current-voltage (I-V) curve. Several parameters of the diode can be extracted from this measurement. In Figure 5-8 the simulated and measured I-V curves of a 2 μm anode radius diode are compared. Some of the parameters derived from current-voltage measurement are shown in Table 1. It is worth to note that, the barrier height for Ti and GaAs Schottky contacts are reported around 0.82-0.83 eV [86], [87] and for the realized GaAs diodes, with different metal configuration contacts, between 0.5-1 eV [25], [30], [72], [88]. Table 2 compares other parameters of the presented diode with some other reported diodes.

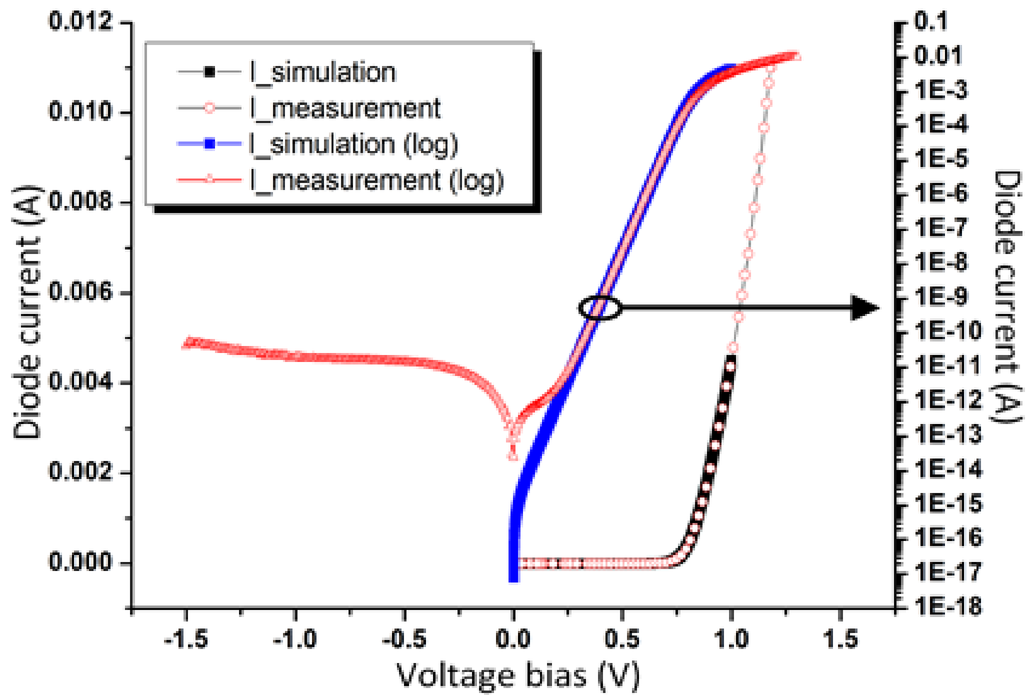


Figure 5-8. Measured and simulated I-V curve of 2 μm radius circular anode diodes.

The lumped element values of the diode equivalent circuit (Figure 3-2 (a)), as a function of the voltage bias for the 1 μm anode radius diodes are presented in Figure 5-9. Due to the Mott-operation mode of diode, below 0.4 V bias, the series resistance R_s is constant. The junction resistance R_j simulation and measurement results are compared in Figure 5-9.

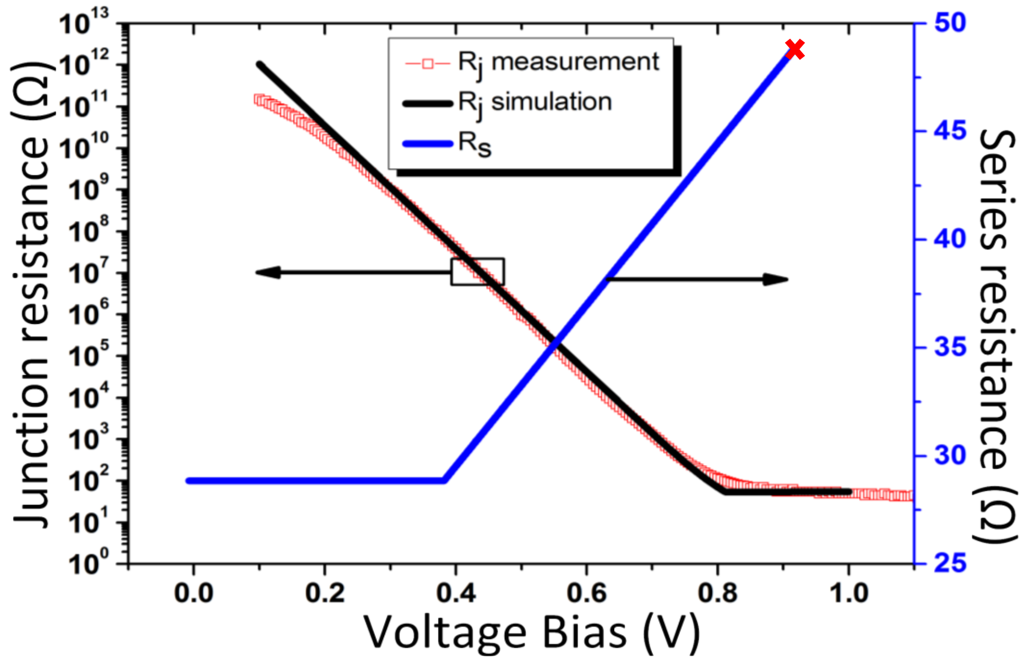


Figure 5-9. Equivalent circuit model components for 1µm anode radius diode. The junction and series resistance, R_j and R_s, simulated and measured results. The measured R_s at 0.9 V bias is ~48 Ω as it is marked by red cross sign.

Saturation current (I_s)	9×10^{-16} A
Barrier height (φ_B)	0.817 eV
Ideality factor (η)	1.13
Series resistance (R_s)-close to 10 mA	30 Ω

Table 2-1. Fabricated diode parameters (with 2 µm anode radius) extracted from I-V measurement.

5.2 TLM method

The TLM method is a well-known method for characterizing the Ohmic-contact. It is based on measurement of the resistance between two Ohmic-contact pads, which is repeated for pads with different distance. The structure that is used in this work is shown in Figure 5-10.

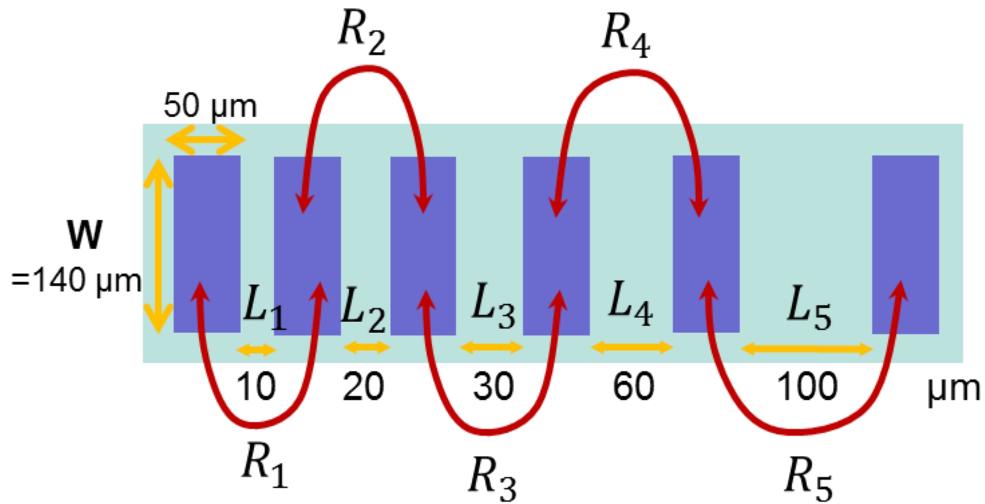


Figure 5-10 The TLM structure that is used in this work.

The 4-probe method is employed for this measurement to exclude the probes and cables resistance. The measured resistances are plotted in Figure 5-11. The Ohmic contact resistance R_c, the n-well doped layer sheet resistance R_{sheet}, and the transfer length L_T can be obtained from this plot. The specific contact resistance ρ_c is obtained from the contact resistance R_c:

$$R_c = \frac{\rho_c}{A_c} \tag{5-7}$$

where A_c is the contact area. The planar structure that is used in this work the current distribution is not homogenous on the contact area as it is in vertical structure. This difference of the current distribution between planar structure and vertical structure is shown in Figure 5-12.

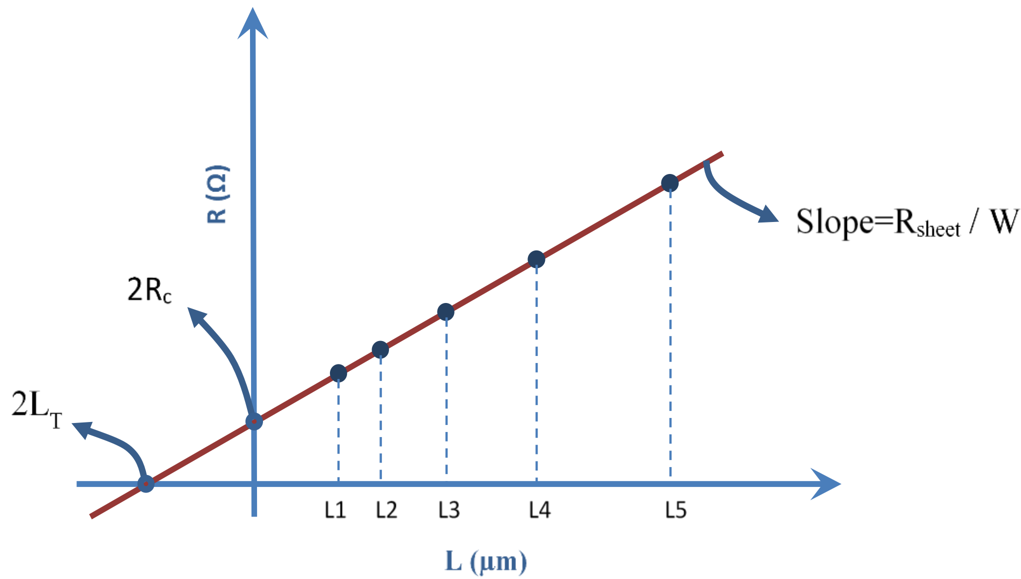


Figure 5-11 Schematic of the TLM measurement results plotting and explanation of parameters extraction from the plot.

The non-uniform current flow into the contact, as is shown in Figure 5-12 (b), causes an effective contact length from the edge of the contact that is called transfer length L_T. So, the contact effective area and subsequently the Ohmic contact resistivity ρ_c is:

$$A_{eff} = L_T \times W \implies \rho_c = R_c \times A_{eff} \tag{5-8}$$

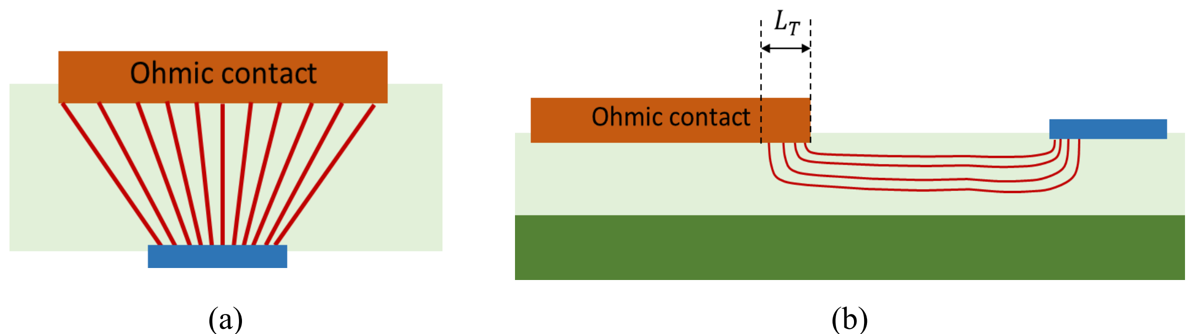


Figure 5-12 The side view of current flow between an ohmic contact and (a) a backside contact, (b) another contact in planar structure.

The TLM method results show that the Ohmic contact optimization, which is presented in chapter 4, can reduce the Ohmic contact resistivity ρ_c from $3.5 \times 10^{-6}\ \Omega.\mathrm{cm}^2$ to $1 \times 10^{-6}\ \Omega.\mathrm{cm}^2$. The channel sheet resistance R_{sheet} is obtained 16.3 Ω/m^2. These parameters are used in the analytical model simulation.

5.3 RF measurements

The device characterization is completed with its frequency behavior characterization.

5.3.1 S-parameters measurement

The S-parameters measurement of the diode is very important in characterizing the device. The S-parameter measurement shows the device frequency behavior, and we can also extract the diode capacitance from the results. The S-parameters and impedance of the device are required in order to use it in a circuit.

The measurement setup includes a Vector Network Analyzer (Anritsu-VNA37369C) 0-40 GHz, a probe station with two GSG probes, and onboard CPW transmission line that leads the signal from probes to the diode. The measurement setup is illustrated in Figure 5-13. The onboard CPW with the diode is shown in Figure 4-3(b) for two probe measurement and Figure 4-3(c) for the one probe measurement.

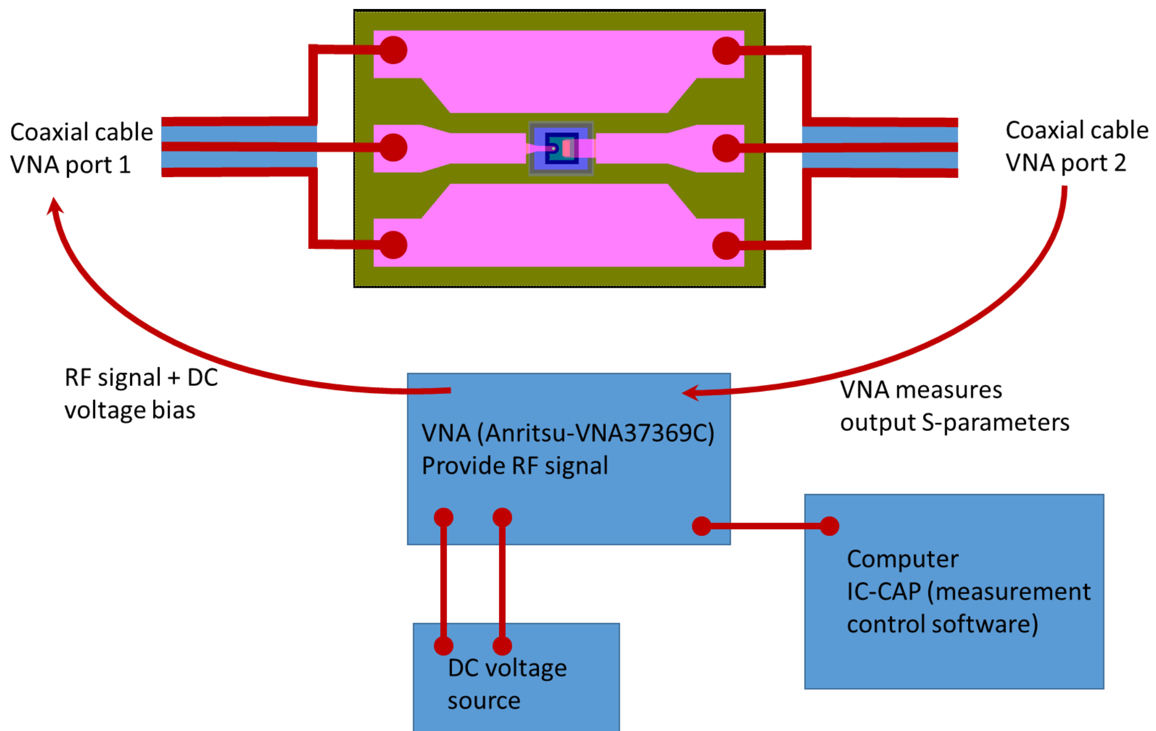


Figure 5-13 RF measurement setup.

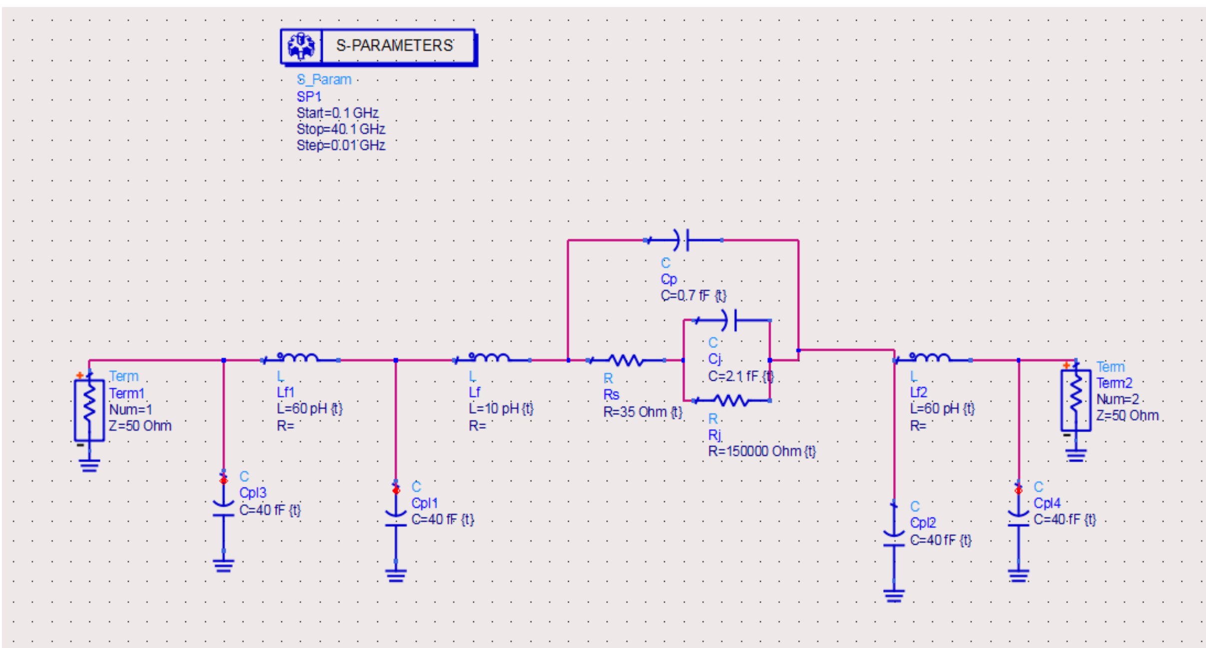


Figure 5-14 The equivalent circuit of the diode + CPW lines that is simulated by ADS to fit the S-parameters with the measurement result and extract the diode capacitance.

5.3.2 RF Measurement results

The fabricated diode has been measured using a CPW transmission line where the diode is placed in series in the middle of the line. The measurement results are then compared to the Advanced Design System (ADS) simulations of the equivalent circuit model as shown in Figure 5-15. The components values of the equivalent circuit model, shown in Figure 3-2 (a) are tuned to fit the measurement results.

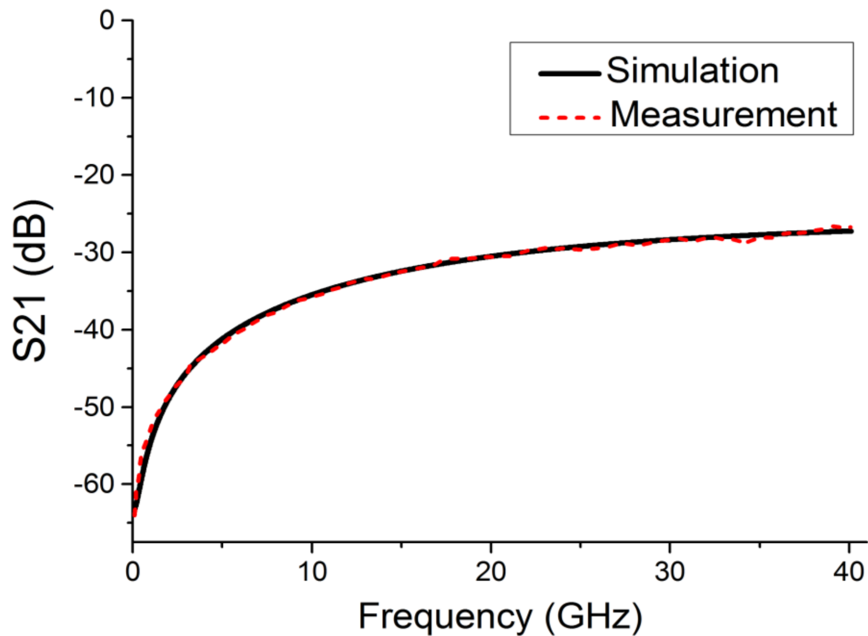


Figure 5-15. The measured S21 parameter for a 1 µm anode radius diode and the fitted ADS model. The diode is in series between the two VNA ports.

The zero bias total capacitance for diodes with different anode areas are extracted from the measured S-parameters. The result is summarized in Figure 5-16 which shows the total capacitance of diode at zero bias as function of the anode radius (r_a). One can observe that, the measured total capacitance of the diode, at zero bias and for 1 µm anode radius is 3.3 fF.

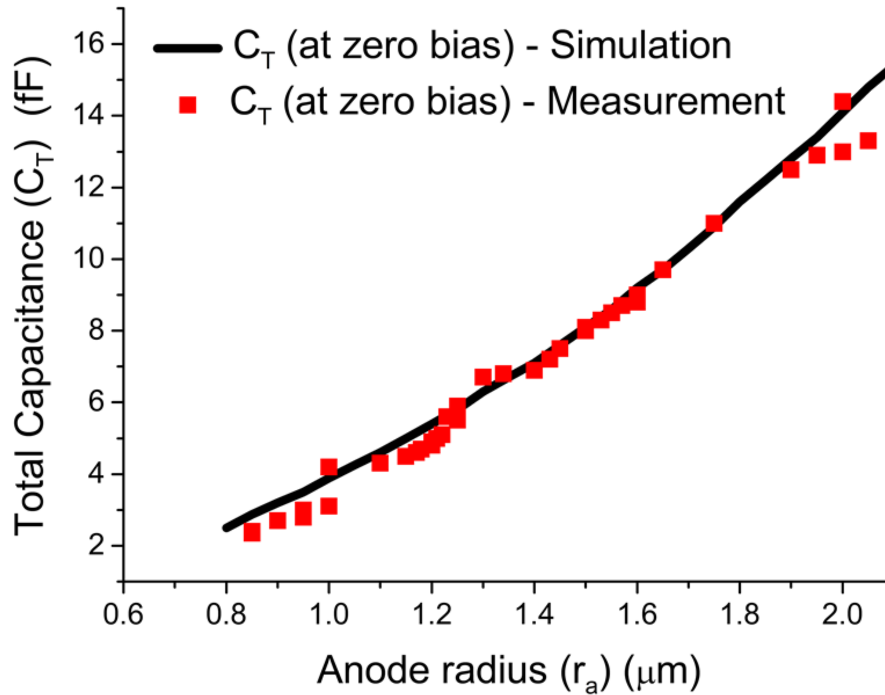


Figure 5-16. The measured and simulated total capacitance C_T at zero bias for the diodes with anode radius between 0.8 to 2 μm.

The measured S21 parameters of the 1.25 μm anode diode for different forward bias voltages are plotted in Figure 5-17. It can be observed that the S21 parameter is a function of the voltage bias. This is due to the dependency of the junction capacitance and resistance to this voltage. At very low frequencies, because the impedance of C_T is comparable to R_j, the S21 parameter is strongly dependent on the changes of R_j. At the higher frequency, the R_j power ratio is reduced (Figure 3-4) and therefore the S21 becomes mostly dependent on C_T, especially at the diode off-state when the R_j is very large. Figure 5-18 shows the extracted total capacitances from S-parameter measurements when the diode is biased from 0 to 1 V. The results are compared with simulations for diodes with 1, 1.25, 1.5 and 2 μm anode radiuses.

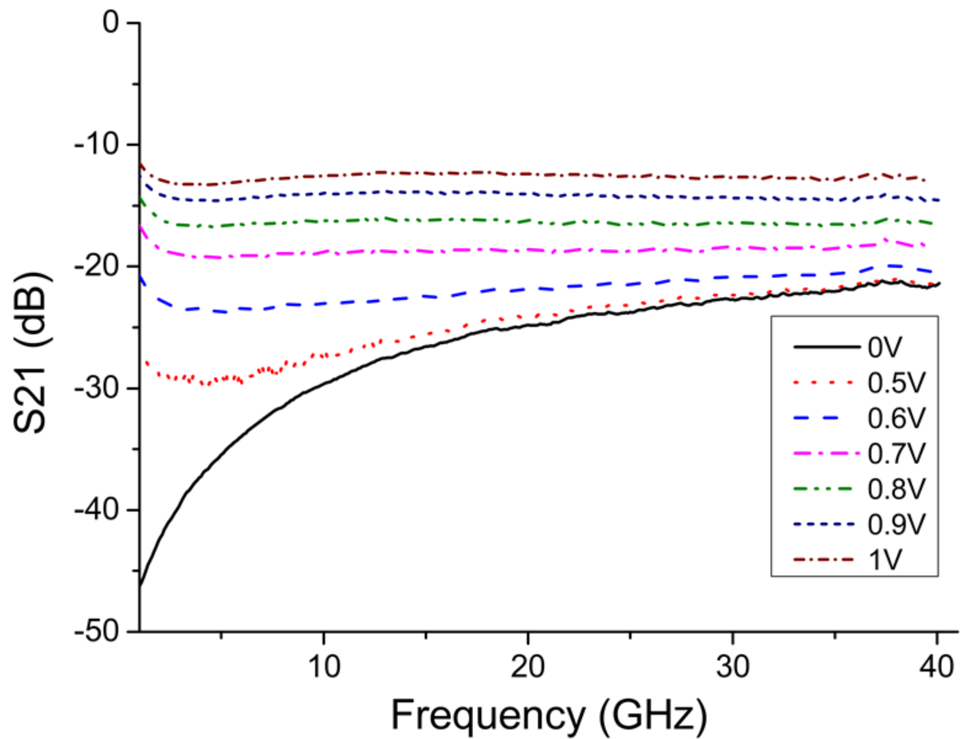
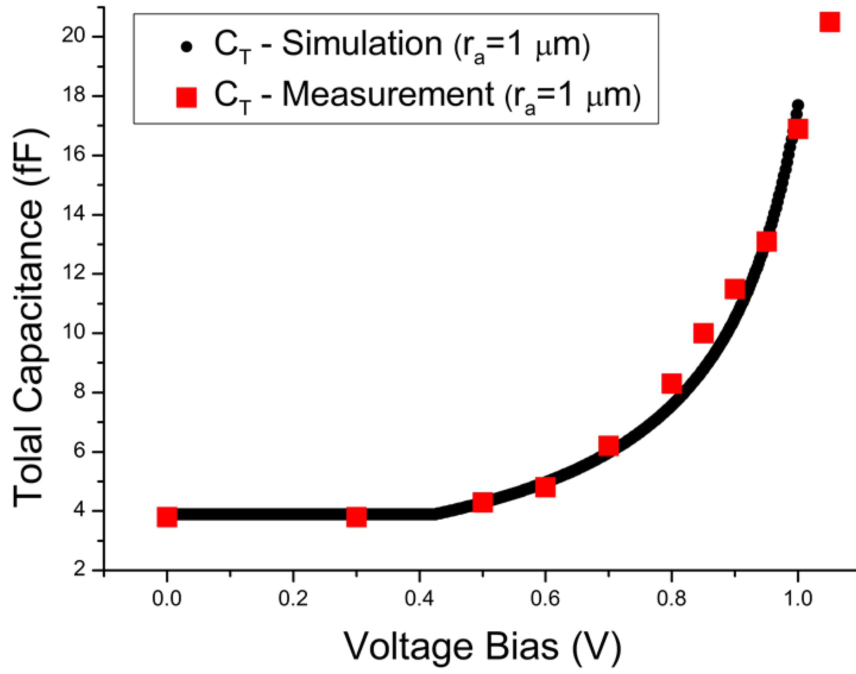


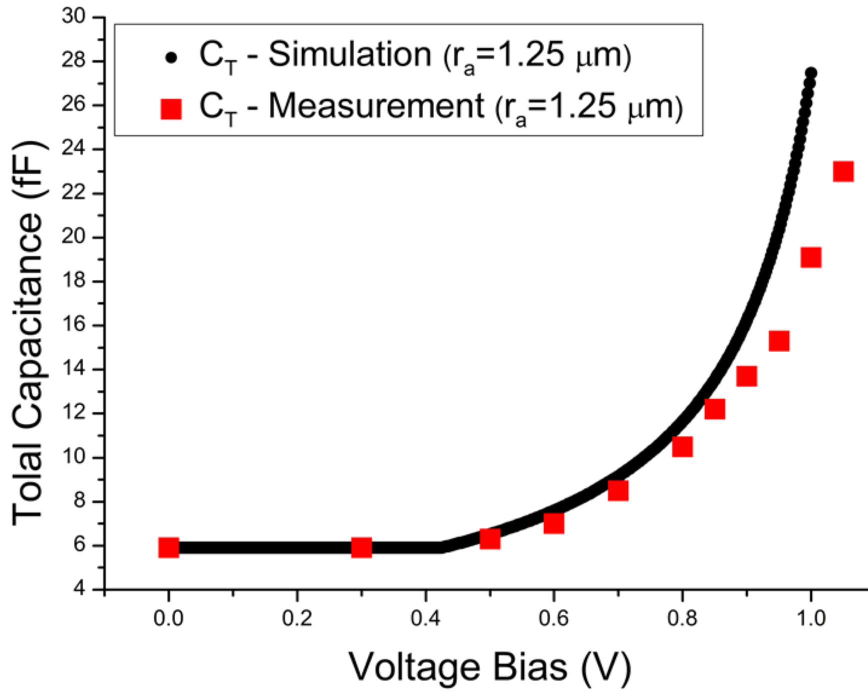
Figure 5-17. The measured S21 parameter of the 1.25 μm radius diode at various voltage biases. The diode is in series between the two VNA ports.

Figure 5-9 to Figure 5-18 are demonstrating the extracted diode parameters and equivalent circuit components using both measurements and simulations. The presented results are also confirming the success of the design and fabrication method which significantly reduced the diode's parasitic capacitance. This will considerably enhance the diode's practical cut-off frequency. The parasitic capacitance C_p for this diode is only 0.6 to 1.1 fF depending on the anode dimension, which is significantly smaller than the other reported diodes.

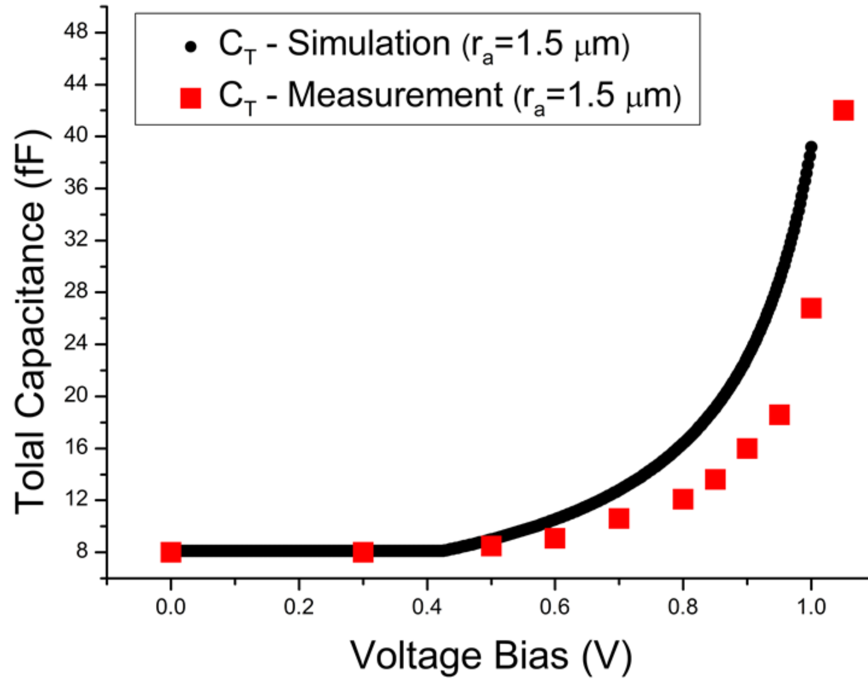
(a)



(b)



(c)



(d)

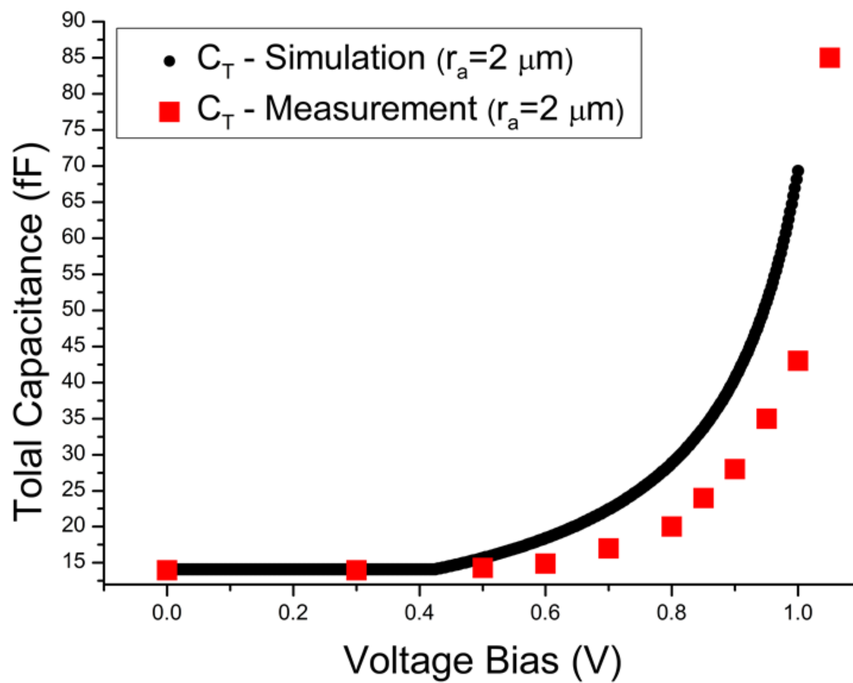


Figure 5-18. Total capacitance C_T that was extracted from measured S-parameters of the biased diodes from 0 V to 1 V and with (a) 1 μm, (b) 1.25 μm, (c) 1.5 μm and (d) 2 μm anode radius, is compared with the simulation results.

Table 2 is comparing the parameters of the proposed and recently reported diodes. This table shows significant progress in reducing the parasitic capacitance (C_p). However, the proposed diode has not been designed and optimized for minimum series resistance due to the epitaxy structure that is used in this project. The structure was selected due to its availability and it is not designed for application as is explained in chapter 4.

Therefore, using the reported design method, it is shown that the need for very small contacts can be mitigated, and for frequencies below 1.5 THz, the expensive electron-beam lithography step can be avoided. Moreover, very small contacts make more fragile devices and reduces their mechanical stability. Using the available GaAs hetero-structure, diodes with various anode diameters with optimized geometry are fabricated. The measured total capacitance C_T for a 1 µm anode radius diode is shown to be 3.9 fF that includes only 0.6 fF of parasitic capacitance. This diode can be used for up to 1.4 THz in mixer mode.

It is worth to mention that in submillimeter and THz diode researches, it is common to characterize the diode at lower frequencies such as [55], [57], [71]. The 1.4 THz cut-off is obtained from the measured parameters of the diode. In most reported diodes, junction capacitance without taking into account the parasitic capacitance has been considered in cut-off frequency calculation. However, as it is mentioned before, here the total capacitance of diode, including the parasitic capacitance, is considered in calculation of cut-off frequency. Also in this calculation the extended method presented in this work which is more accurate have used. It is a conventional method to introduce a diode individually based on this cut-off frequency as it is used in [48], [50], [89].

Ref.-year	Anode area μm^2	I_s (A)	η	R_s (Ω)	C_{j0} (fF)	C_p (fF)	f_{Cj0} $^{(*)}$ (THz)	f_{CT0} $^{(**)}$ (THz)	f $^{(***)}$ (THz)	NEP $(pW/\sqrt{Hz})$
[50]-2015	4.5	4×10^{-13}	1.28	4.5	7	4	5	3.2	-	-
[33]-2013	10	-	-	8	10	5	2	1.3	-	-
[82]-2013	0.95	0.98×10^{-15}	1.18	13.67	1.42	-	8	-	0.26-0.4	60
[89]-2012	-	1.75×10^{-14}	1.21	4	5.8	9.5	6.8	2.6	0.22	-
[83]-2011	2	1.6×10^{-12}	1.47	16	5	-	2	-	0.22	-
[90]-2011	0.4 × 1.4	-	-	35	1.5	-	3	-	0.3	-
[91]-2009	-	11×10^{-6}	1.13	19	-	-	-	-	0.2	20
This work	3.1	9×10^{-16}	1.13	26	3.3	0.6	1.85	1.5	0.6	3.7

(∗) First approach of cut-off frequency calculation, at zero bias and without considering parasitic capacitance.
(∗∗) Cut-off frequency at zero bias with considering parasitic capacitance.
(∗∗∗) The frequency that the diode is used and/or the NEP is reported in this frequency.

Table 2. Parameters of THz diodes presented in the recent literature compared to the diode proposed in this work. [33], [50], [82], [83], [89]–[91]

5.4 Mixer anti-parallel diodes

Another configuration we designed has back-to-back diodes as is shown in Figure 5-19. This configuration is a good choice for multiplication application. The back-to-back structure needs to be at zero bias since it is a symmetric configuration as is shown in Figure 5-19, and applying a DC bias take one of the diodes out-range. The fabricated diode, in this work, is in the Mott-operation below +0.4 V bias, due to the Schottky layer specifications, doping level and thickness. The junction capacitance C_j is constant when the diode is in the Mott-operation, as is discussed in chapter 3. Therefore, part of the signal power consumed to raise the diode to 0.4 V has no multiplication output. Thus, the signal power part that is applied to the diode after 0.4 V merely provides other harmonics. The measurement result for the back-to-back diodes with 2 μm radius anodes and Figure 5-19 setup is shown in Figure 5-20. The input signal is 6 GHz with +14dBm power. The output as is shown in Figure 5-20 includes harmonics of the input signal.

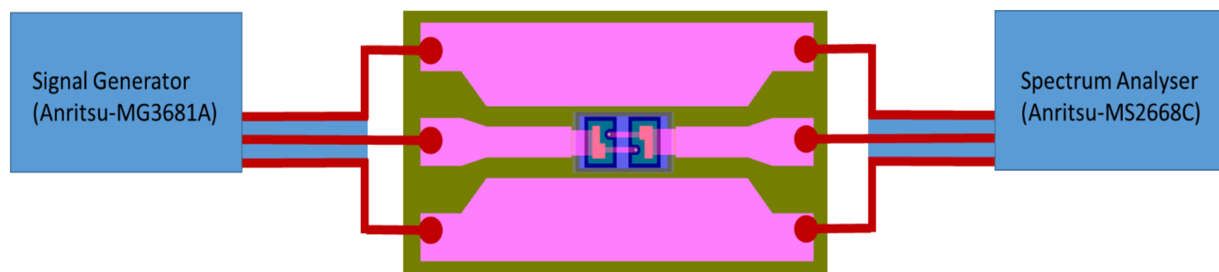


Figure 5-19 The back-to-back diodes structure with the connection onboard transmission line and measurement setup.

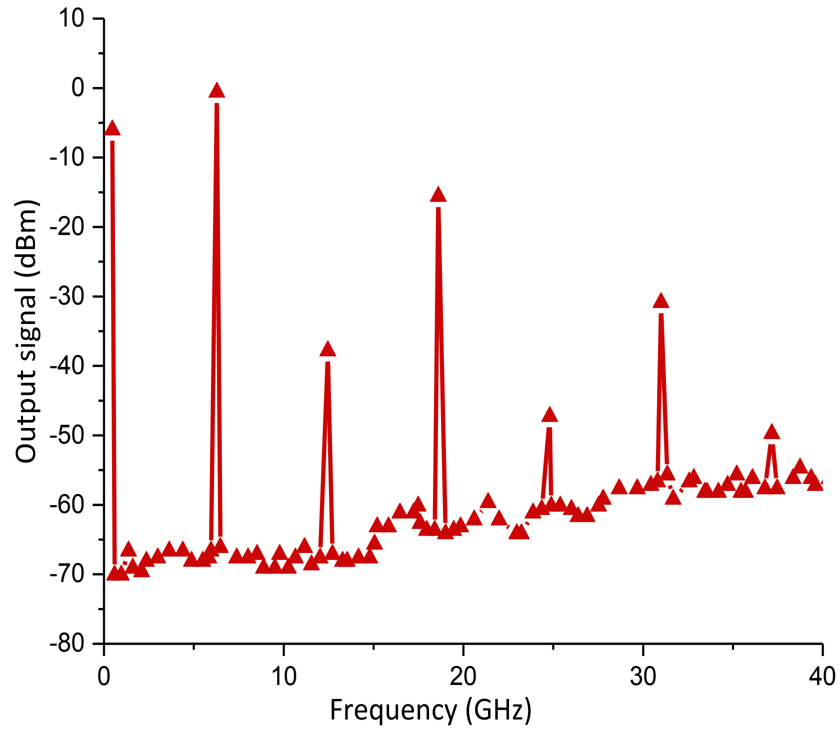


Figure 5-20 The back-to-back diodes multiplication measurement result for 6 GHz input signal with +14 dBm power.

6 Conclusion and future works

6.1 Conclusion

In this work, we redesigned the GaAs planar Schottky diode for mm Waves and THz applications. The objective was to maximize the performance of the diode by reducing the parasitic elements of the diode. To do so, an optimization methodology is proposed. The optimization is applied by using a code which is developed, based on the analytical formulation, for design and simulation of the diode. The simulation results are presented and discussed. Accordingly, for realization of the optimized diode, a reliable, repeatable and cost effective fabrication process is developed. The process includes fabrication of T-shaped contact and air-bridges over the deep trenches. The T-shaped anode process provides larger stand-off in comparison to other works and its values are controllable, according to the design. The air-bridge is built as the same time as the T-shaped anode when the trenches are planarized. In the design process, application of the diode is also taken into account. By using this strategy the diode can be designed either specifically for direct detection, mixing/multiplication, or even as a multipurpose diode that can be used for different applications by adjusting its voltage bias. The diode behavior is also classified by considering the application. The result is presented for diodes operating between 0.1-1.5 THz by using the available HBT GaAs wafer used for fabrication of the diodes. The main contributions of this work are the following:

- A design method is reported that is based on analytical model by taking into account the device application. For the first time, the Schottky diode engineering is studied by considering its application.
- Comparison is made between the existing approaches for calculating the diode cut-off frequency and a new approach proposed in this work. The new approach is based on considering all diode-equivalent circuit elements and also the application of the diode. The result for the fabricated diode in this work are shown.
- A unique, reliable, low-cost and flexible fabrication process for the diode that can be a good candidate for high volume production is developed and presented here.
- The fabrication process includes air bridges over the deep trenches, T-shaped contact, and a new adaptive planarization method. The T-shaped contact process is developed based on

all photolithography for anode contacts larger than 2 μm^2. Also, for anodes smaller than 2 μm^2, the process merely substitutes one photolithography step with an electron-beam lithography and without any other change.

- The total capacitance of the diode is significantly reduced in comparison to reported diodes with the same anode area size. The measurement results prove the design successful for reducing the parasitic elements of the diode and improving diode performance.

6.2 Future work

We have some suggestion for next steps in pursuing this work as follows:

- Developing a backside process (back side of the sample) in order to thin the diode substrate. The thick bulk GaAs substrate at mm-Waves and higher frequencies increases the parasitic elements of diode.
- Using the epitaxial structure that supports optimized design performance. The epitaxial structure that is used in this work was the available HBT GaAs which is not designed and optimized for this diode structure, as is explained in chapter 3 and 4. Although we had very good results, the diode performance can be improved significantly, especially for series resistance, by using an epitaxy structure that is designed for this application. Also, repeatability of the fabrication process and its precision will greatly increase. Since the current HBT structure requires a wet etch process to reduce the n-doped layer thickness that have used as Schottky layer, some uncertainty is added to the process results since the wet etch process is not accurate enough for the Schottky layer thickness that has large impact on the diode performance. The Schottky layer doping can be optimized as is explained in chapter 4. On the other hand, the n-well doped (ohmic-contact) layer in our HBT structure was very thin, and its doping level is better higher. By optimizing the n-well doped layer we can reduce the parasitic series resistance significantly.
- In order to increase the device cut-off frequency, fabrication of diodes by using the developed E-beam substituted step for anode opening as is mentioned in chapter 4, is suggested.
- In order to make characterization of the diode more precise, measurement at higher frequency (over 100 GHz) is required. For this high frequency measurement, monolithic

waveguides fabrication and the network analyzer (VNA) or extension heads for that frequency range is required.

- The next important step is using the developed diode in a circuit. That can be achieved by two different methods:
  - First, a monolithic circuit that the circuit is fabricated on in the same substrate (GaAs) as the diode is. That would necessitate a new mask set to support the required space for the designed circuit around the diode for fabricating the circuit.
  - The second method is using the flip-chip diode as explained in chapter 4. In this method we can use the diced individual diode or the back-to-back mixers in the any arbitrary circuit on any substrate.
- In order to commercialize the diode, developing a packaging process is required.

7 Conclusion (en français)

Dans ce travail, nous avons revu en profondeur la conception de la diode Schottky planaire sur un substrat GaAs pour des applications en ondes millimétriques et térahertz. L'objectif était de maximiser les performances de la diode en réduisant les ses éléments parasites. Pour ce faire, une méthodologie d'optimisation est proposée. L'optimisation est appliquée en utilisant un programme qui a été développé, sur la base de la formulation analytique, pour la conception et la simulation de la diode. Les résultats de la simulation sont présentés et une discussion a été présentée. Pour réaliser la diode dont la conception a été optimisée, un procédé de fabrication fiable, reproductible et à coûts faibles est développé. Le procédé comprend la fabrication de d'une anode en forme de T et de ponts à air jetés sur des tranchées profondes. Le procédé pour développer une anode en forme de T offre une plus grande résistance à la rupture par rapport à d'autres travaux et ses valeurs sont contrôlables, selon la conception. Le pont à air est construit en même temps que l'anode une fois les tranchées planarisées. Le processus de conception proposé tient compte de l'application de la diode dès le début de la conception. En utilisant cette stratégie, la diode peut être conçue spécifiquement pour l'application souhaitée, c'est à dire soit une détection directe soit une fonction de mélange, soit une fonction multiplicatrice, ou même soit dans un objectif de multifonction, les fonctions étant alors sélectionnées par la polarisation de la diode pour la rendre la plus efficace possible. Le comportement de la diode et plus particulièrement sa fréquence de coupure, peut également être classé en considérant l'application. Tous les résultats présentés dans cette thèse le sont pour des diodes fonctionnant entre 0,1 et 1,5 THz en utilisant une épitaxie GaAs HBT disponible au laboratoire utilisée pour la fabrication des diodes.

Les principales contributions de ce travail sont les suivantes:

• une méthode de conception basée sur un modèle analytique et tenant compte de l'application souhaitée. À notre connaissance, c'est la première fois que l'ingénierie des diodes Schottky est étudiée en considérant en premier l'application à laquelle eslle est dédiée.

• une comparaison entre les approches existantes pour le calcul de la fréquence de coupure des diodes est présentée et une nouvelle approche pour ce calcul est proposée. Cette nouvelle approche

se base d’une part sur tous les éléments du circuit équivalent de la diode ainsi que sur l'application visée.

• un nouveau procédé de fabrication unique, fiable, peu coûteux et flexible pour les diodes permettant d’envisager une production à grand volume élevé.

• une extension possible de ce procédé pour des diodes à fréquences encore plus élevée. Effectivement le processus de fabrication comprend des ponts à airs sur des tranchées profondes, un contact en forme de T et une nouvelle méthode de planarisation adaptative. Le contact en forme de T est développé à l’aide de photolithographies optiques permettant une taille minimale 2 μm^2. Ainsi, si l’on veut monter en fréquence, seule l’étape de fabrication de l’anode (inférieure à 2 μm^2) doit être substituée par une lithographie par faisceau d’électrons.

• une réduction significative de la capacité totale de la diode en comparaison avec les diodes rapportées dans la littérature pour une dimension d'anode équivalente. Les résultats de mesure prouvent que la conception et le procédé de fabrication proposé permettent de réduire les éléments parasites et donc l’améliorer de la performance des diodes.

Appendix A

Metal-semiconductor contacts

The metal-semiconductor (M-S) contacts providing access from semiconductors to the rest of the circuit. They are dividing into two categories a) rectifying contact and b) non-rectifying (Ohmic) contact. The energy bands for the metal and the semiconductor (n-type) before having contact are shown in Figure A-0-1 (a). The difference of metal and semiconductor work functions affects the thermal equilibrium energy band and cause the potential barrier at the contact interface [92]. Figure A-0-1 (b) is shown the metal-semiconductor junction in the thermal equilibrium situation.

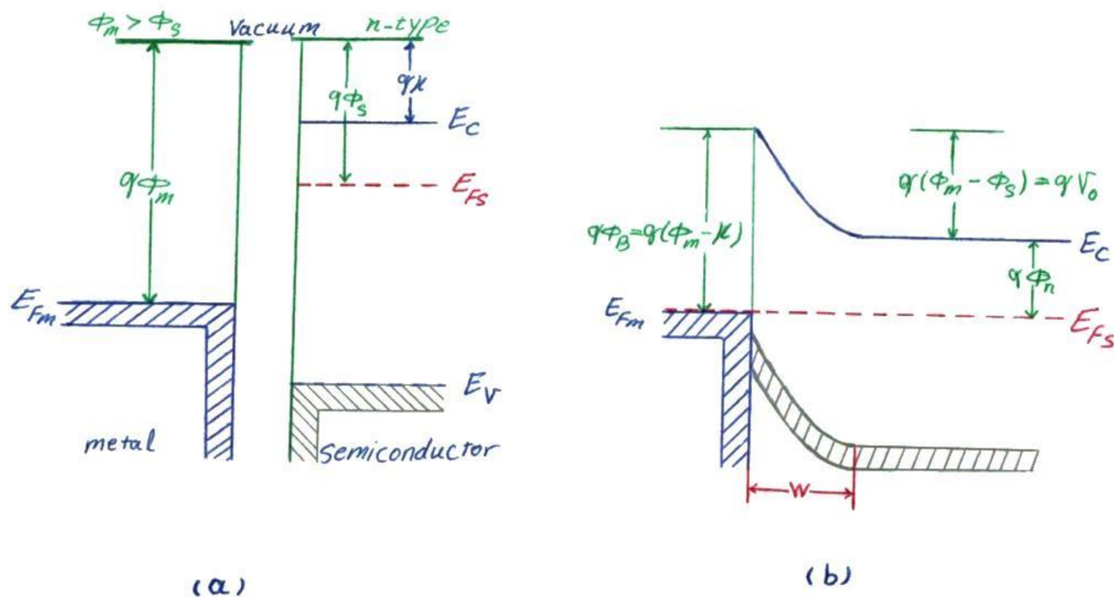


Figure A-0-1 Metal and n-type semiconductor energy band diagrams, (a) before instance of contact, and (b) after contact is built, at thermal equilibrium.

In Figure A-0-1:

E_{FM} : Metal Fermi level

E_{FS} : Semiconductor Fermi level

E_C : Semiconductor conduction band edge

Φ_M : Work-function of metal in vacuum

Φ_S : Work-function of semiconductor in vacuum

χ : Electron affinity

v_0 : Equilibrium contact potential

q : Electron charge

The electron affinity energy (χ) of a semiconductor is difference of energy between the vacuum energy to the conduction band edge. It is the material fundamental property and not a function of the semiconductor doping. However, the semiconductor work function Φ_s depends on the doping level, since the fermi level E_{FS} is a function of doping type and concentration.

In the connection interface of the metal and semiconductor, there is a barrier for an electron in the metal, with energy equal to E_{FM}, to flow toward the semiconductor. Height of this barrier is equal to the difference between Φ_M and χ.

$$\Phi_B = \Phi_M - \chi \tag{A-1}$$

The contact potential (v_0) control the amount of passing net electron from the semiconductor to the metal. This potential equals to difference of the metal and semiconductor work-functions.

$$v_0 = \Phi_M - \Phi_S \tag{A-2}$$

The metal-semiconductor contacts are classified into 4 types as explained in Figure A-0-2:

1. Rectifying contact of n-type semiconductor with metal ($\Phi_m > \Phi_s$)

   The Schottky diodes are mainly are in this category.

2. Rectifying contact of p-type semiconductor with metal ($\Phi_m < \Phi_s$)

3. Ohmic contact of n-type semiconductor with metal ($\Phi_m < \Phi_s$)

   It is used for interconnecting the n-type semiconductors

4. Ohmic contact of p-type semiconductor with metal ($\Phi_m > \Phi_s$)

   It is used for interconnecting the p-type semiconductors

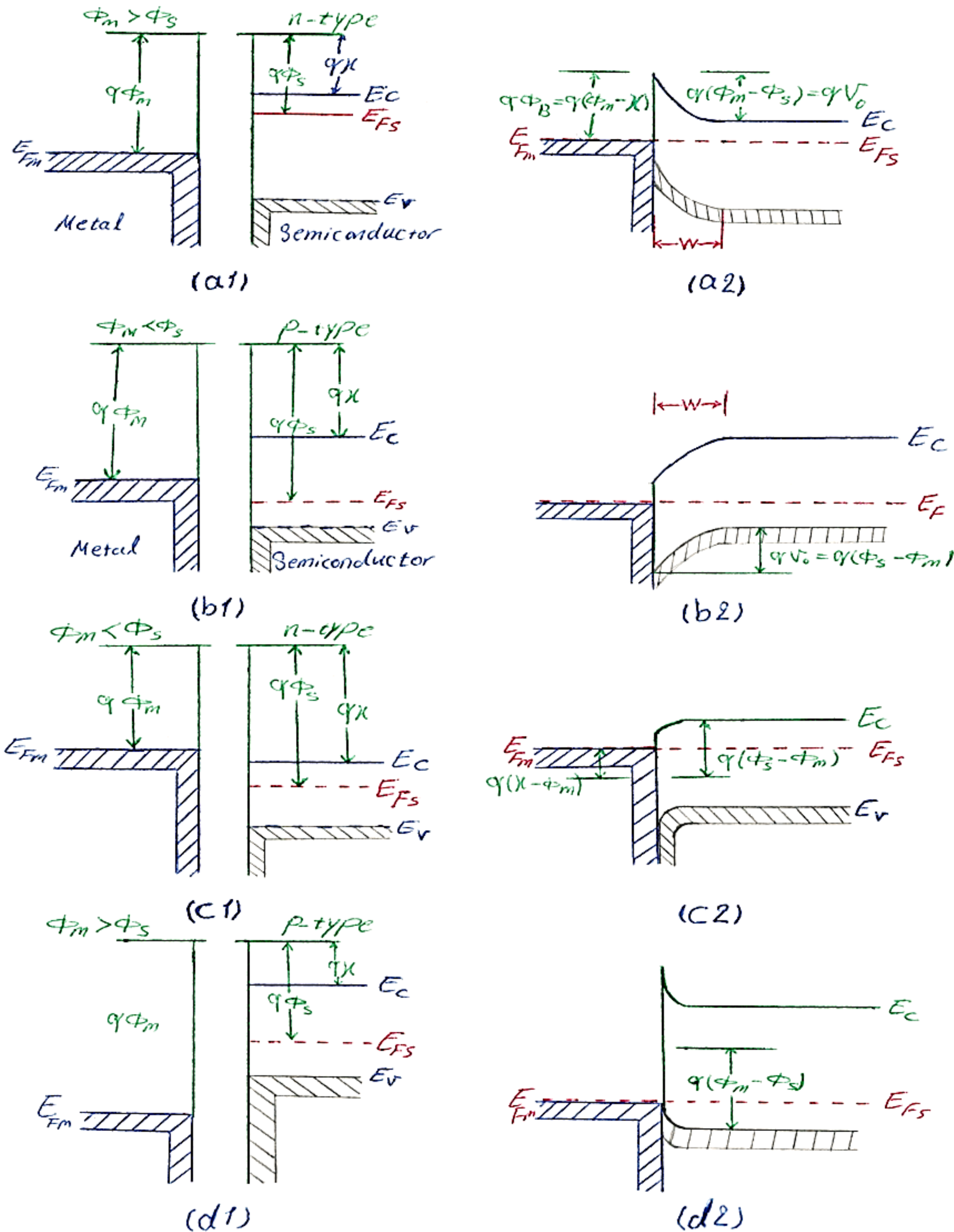


Figure A-0-2 Metal-Semiconductor contact types energy band diagrams. Rectifying contacts: (a)$\Phi_m > \Phi_s$ for an n-type semiconductor (a1) before joining (a2) the junction equilibrium energy diagram, (b)$\Phi_m < \Phi_s$ for an p-type semiconductor (b1) before joining (b2) the junction equilibrium energy diagram. Ohmic contact: (c) $\Phi_m < \Phi_s$ for an n-type semiconductor (c1) before joining (c2) the junction equilibrium energy diagram, (d) $\Phi_m > \Phi_s$ for an p-type semiconductor (d1) before joining (d2) the junction equilibrium energy diagram [93].

In the diode structure two metal-semiconductor contacts are exist, one is rectifying contact and the other one is an ohmic contact as interconnection of the diode into the circuit.

Schottky contact – rectifying contact

The metal-semiconductor contact with nonlinear current is called Schottky or rectifying contact, due to its current flow directional properties. It means this contact has much higher current flow in one direction than the other one. In this contact depletion layer is formed just in semiconductor side, the thickness of this depletion layer (W) is shown in Figure A-0-1. The current nonlinearity of this contact is similar to p-n junction:

$$I = I_0\left(e^{qV/kT} - 1\right) \tag{A-3}$$

where I_0 is reverse saturation current.

Figure A-0-1 (b) is shown the ideal Schottky contact with n-type semiconductor. Figure A-0-3 is shown the real contact energy band diagram when the applied voltage across the junction is either zero (V=0), forward bias (V>0), or backward bias (V<0). The barrier height difference from its ideal value, Φ_B is $\Delta\Phi$ as is shown in Figure A-0-3, which is given by:

$$\Delta\Phi = \sqrt{\frac{q\xi_m}{4\pi\varepsilon_s}} \tag{A-4}$$

where ξ_m is the maximum value of electric field at the junction interface.

$$\xi_m = \sqrt{\frac{2qN_D|\psi_s|}{\varepsilon_s}} \tag{A-5}$$

$$|\psi_s| = \Phi_B - \Phi_n + V_R \tag{A-6}$$

where N_D is the semiconductor doping concentration, V_R is the contact reverse bias voltage, and Φ_n is energy difference between contact fermi level and the semiconductor conductive bang energy level as is shown in Figure A-0-1.

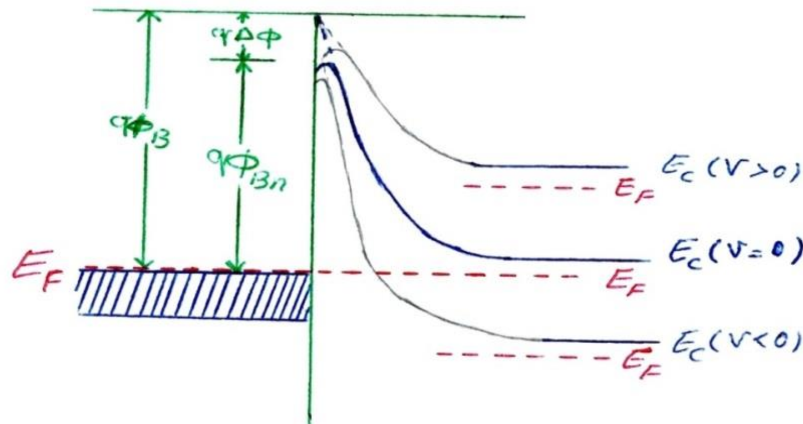


Figure A-0-3 Energy diagram of the practical Schottky diode in forward, zero and reverse biases. qΔΦ is the Schottky effect reduction of barrier height due to the thermal equilibrium.

The thickness of depletion region, W and the energy band diagram of the contact as a function of voltage bias is shown in Figure A-0-4.

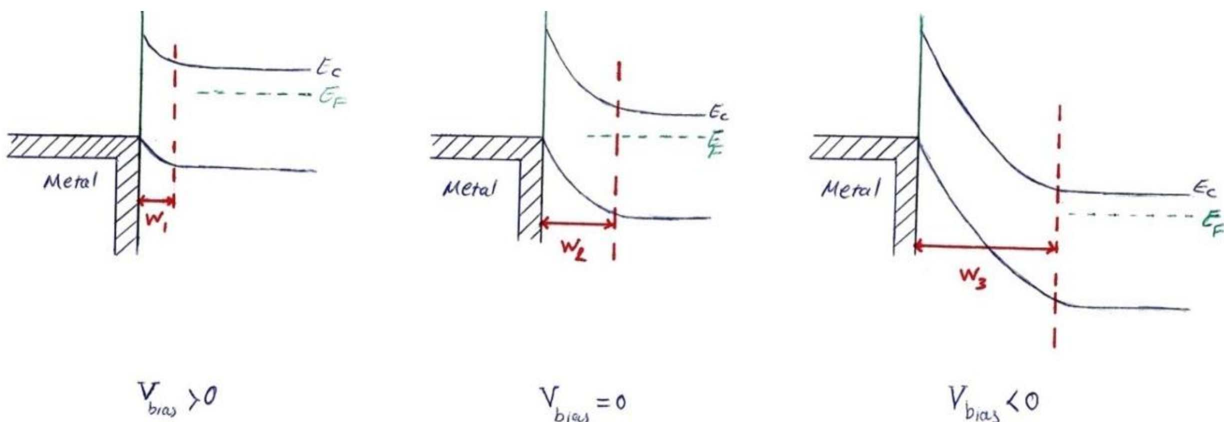


Figure A-0-4 The Schottky contact energy diagram in forward, zero and reverse biases.

Ohmic contact – non-rectifying contact

The Ohmic contact is normally built by thermal annealing the M-S contact with heavily doped semiconductor. The contact annealing cause metal diffusion into the semiconductor at the contact area. The Ohmic contact have linear I-V characteristic and it does not have depletion layer in contact interference. In this type of metal-semiconductor contact the majority carriers are flowing from metal into the semiconductor.

Appendix B

List of publications

- Sarvenaz Jenabi, A. Malekabadi, D. Deslandes, F. Boone, and S. A. Charlebois, "Submillimeter Wave GaAs Schottky Diode Application Based Study and Optimization for 0.1- 1.5 THz," *Solid. State. Electron.*, vol. 134, pp. 65–73, 2017.

  https://doi.org/10.1016/j.sse.2017.05.008

- Sarvenaz Jenabi, D. Deslandes, F. Boone, and S. A. Charlebois, "A low-cost fabrication method for sub-millimeter wave GaAs Schottky diode," Semicond. Sci. Technol., vol. 32, no. 10, Oct. 2017.

  https://doi.org/10.1088/1361-6641/aa860c

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