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The development of metallic single electron transistor (SET) depends on the downscaling and the electrical properties of its tunnel junctions. These tunnel junctions should insure high tunnel current levels, low thermionic current, and low capacitance. The authors use atomic layer deposition to fabricate Al_2O_3 and HfO_2 thin layers. Tunnel barrier engineering allows the achievement of low capacitance Al_2O_3 and HfO_2 tunnel junctions using optimized annealing and plasma exposure conditions. Different stacks were designed and fabricated to increase the transparency of the tunnel junction while minimizing thermionic current. This tunnel junction is meant to be integrated in SET to enhance its electrical properties (e.g., operating temperature, I_{ON}/I_{OFF} ratio). © *2014 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4853075]

I. INTRODUCTION

Dielectric stacks have become a suitable solution to continue the gate dielectric down-scaling, without deteriorating the field effect transistor characteristics.[1–3] Several dielectric stacks have been proposed as great candidates for nonvolatile memory applications (flash memory, etc.).[2,4] Metal–insulator–metal capacitors with HfO_2 and Al_2O_3 dielectric stacks have been subject to different studies in RF and analog circuits applications.[5–7] The development of single electron memory could benefit from the on-going development in tunnel barrier engineering. Indeed, considering crested barriers would help ameliorate the writing process necessary for bit-addressable applications.[4]

In the case of a single electron transistor (SET), the tunnel junction dielectric requirements are different compared to nonvolatile memory or CMOS gate dielectric (high transparency and low capacitance are required). One of the conditions to observe Coulomb oscillations in SET at room temperature is having $e^2/C_{tot} > 5k_BT$ (with $5k_BT \approx 0.13$ eV at room temperature), where e is the elementary charge, C_{tot} is total capacitance of the SET island, k_B is Boltzmann constant, and T is the temperature.[4,8] Consequently, the SET requires extreme miniaturization and a low dielectric constant junction in order to minimize C_{tot}. Furthermore, SET suffers from low tunnel current levels (ON current) and high thermionic current (OFF current).

In this work, we tackle SET requirements using atomic layer deposition (ALD). First, we investigate the effect of *in situ* O_2 plasma exposure and *ex situ* annealing in N_2 atmosphere on Al_2O_3 and HfO_2 thin films deposited by plasma enhanced ALD (PEALD) in order to achieve low tunnel junctions capacitances. Second, we study engineered tunnel junctions composed of Al_2O_3 and HfO_2 layers to increase tunnel transparency while keeping low thermionic current. These tunnel junctions will be integrated in SET to enhance its electrical properties (e.g., operating temperature, I_{ON}/I_{OFF} ratio). Conformability and thin film uniformity of deposited films are additional motivation behind the use of PEALD.[9]

II. EXPERIMENTAL SET UP

A. Test structures

All structures were fabricated on a p-type Si substrate with 500 nm of grown thermal SiO_2 and 100 nm of Pt evaporated on top (bottom electrode). Then, Al_2O_3 and HfO_2 were deposited by PEALD using trimethyl aluminum (TMA) ($AlMe_3$) and $Hf(NMe_2)_4$ precursors, respectively. Both precursors were heated at 75 °C while the depositions were conducted at 250 °C. Prior to deposition, H_2O and O_2 residuals

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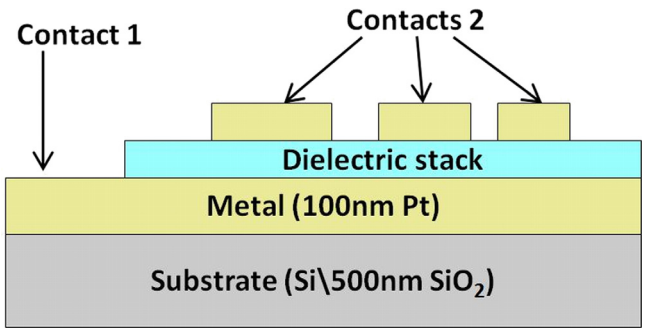

FIG. 1. (Color online) Schematic of the samples used for dielectric characterization. On a Si-500 nm SiO_2 substrate, a back electrode of 100 nm Pt on which the dielectric stack was deposited. A 50 nm sputtered Pt top electrodes of different sizes were formed by a liftoff process for the top electrode.

are pumped away for 1200 s. The deposition cycle starts with a precursor pulse [TMA or $Hf(NMe_2)_4$] and precursor purge time. While Ar flow is kept at 200 sccm, the O_2 flow is increased from 0 to 20 sccm and the plasma exposition at 300 W is carried during 20, 30, or 40 s. After the plasma exposure, the O_2 flow is restored to 0 sccm; this is followed by a waiting time to purge the reaction product. In addition to the deposition of single thin Al_2O_3 or HfO_2 layers, different stacks of HfO_2 and Al_2O_3 were considered. After dielectric deposition, a lift-off process was used to define a 50 nm Pt top electrode deposited by sputtering with surfaces ranging between 40×40 μm^2 and 100×100 μm^2. On the sample periphery, the dielectric stacks were etched in an hydrofluoric acid (HF) solution to reach the bottom electrode (see Fig. 1). Table I summarizes HfO_2 and Al_2O_3 deposition parameters.

B. Characterization and modeling methodology

The objective of this work is to investigate the tunnel junction electrical properties; consequently, we have endorsed a characterization protocol in order to extract dielectric parameters. First, thicknesses of the deposited layers were measured using an *in situ HORIBA Jobin-Yvon* ellipsometer at five points on each sample for various thicknesses (50 nm–15 nm–10 nm–5 nm) and for both materials. A second *ex situ Jobin-Yvon UVISEL* ellipsometer was used to confirm the measurements. Deposition rates for both dielectrics have been evaluated at 0.09 nm/cycle. Knowing the thickness, low frequency (1 kHz) capacitance–voltage characteristics were used to measure the capacitance and evaluate effective dielectric constants for each structure. Additionally, Fowler–Nordheim (FN) current plots [$\ln(J/E^2)$ vs $1/E$] were used to extract effective mass and barrier height in the FN regime (high electrical field). Using the extracted parameters, measured current versus voltage data were compared to transfer matrix formalism and Wentzel–Kramers–Brillouin simulations in the FN regime.[10] Both tunnel current and capacitance were measured using a Keithley 4200 characterization system.

III. RESULTS FOR SINGLE LAYER OF Al_2O_3 OR HfO_2

In order to examine surface morphology, Al_2O_3 and HfO_2 thin films were deposited on Si layer after HF solution treatment, and the topography was investigated using AFM. The root mean square roughness morphologies for HfO_2 and Al_2O_3 were measured to be less than 0.5 nm, which is at the limit of the instrumentation resolution. This assesses the high uniformity of thin films deposited by PEALD compared to any other deposition technique. All the thin films deposited on Pt layer were also observed using AFM. Measured surface roughness was again less than 0.5 nm, and the samples were free from defects (e.g., pinholes).

One of the objectives of this work is to lower the overall capacitance while keeping high tunnel current. Actually, the effect of N_2 annealing and the O_2 plasma exposure were both recognized to lower the capacitance. For both techniques, the thickness of the layers was measured using ellipsometry before and after treatment in order to monitor the potential impact of this parameter.

C-V, *J-V*, and FN-plots for Al_2O_3 and HfO_2 (for *in situ* 20 s and 40 s O_2 plasma exposition) are shown in Figs. 2 and 3, respectively. For each dielectric, we compare the effect of O_2 plasma exposition time on the capacitance and current levels. It appears clearly from Figs. 2(b) and 3(b) (for both Al_2O_3 and HfO_2) that exposing the dielectric to 40 s of O_2 plasma at each PEALD cycle (instead of 20 s) has considerably reduced the capacitance as required by the targeted application. In Fig. 4, Al_2O_3 and HfO_2 measured capacitance has been reduced at 40 s of O_2 plasma exposure to reach 6.7 mF/m^2 for Al_2O_3 and 8.4 mF/m^2 for HfO_2 (which correspond to an effective dielectric constant of 4.2 for Al_2O_3 and 5.5 for HfO_2 considering no modification in thickness).

The decrease of the measured capacitance can be attributed to a decrease in the overall dielectric constant of the structure, the increase of the dielectric thickness, or a combination of both mechanisms. Ellipsometry measurements and the slight decrease in tunnel current are both evidence that no significant change happened to the thickness. During plasma exposure, a thin and low dielectric constant Pt-dielectric interface layer can be formed. However, this interface is not thick enough to explain the change in capacitance.[11] It is thus conceivable that this change is structural and compositional modification in the dielectrics (O/Al and O/Hf ratios or Carbon contamination). It has been reported that plasma O_2 pulse length is not directly related to the growth rate of the Al_2O_3 thin films and that O/Al ratio was

TABLE I. Al_2O_3 and HfO_2 PEALD parameters.

Material	Precursor	Power	Exposition time	Gas flows	Temperature	Rate
Al_2O_3	TMA	300 W	20 s, 40 s	O_2 20 sccm, Ar 200 sccm	250 °C	0.9 Å/cycle
HfO_2	$Hf(NMe_2)_4$	300 W	20 s, 40 s	O_2 20 sccm, Ar 200 sccm	250 °C	0.9 Å/cycle

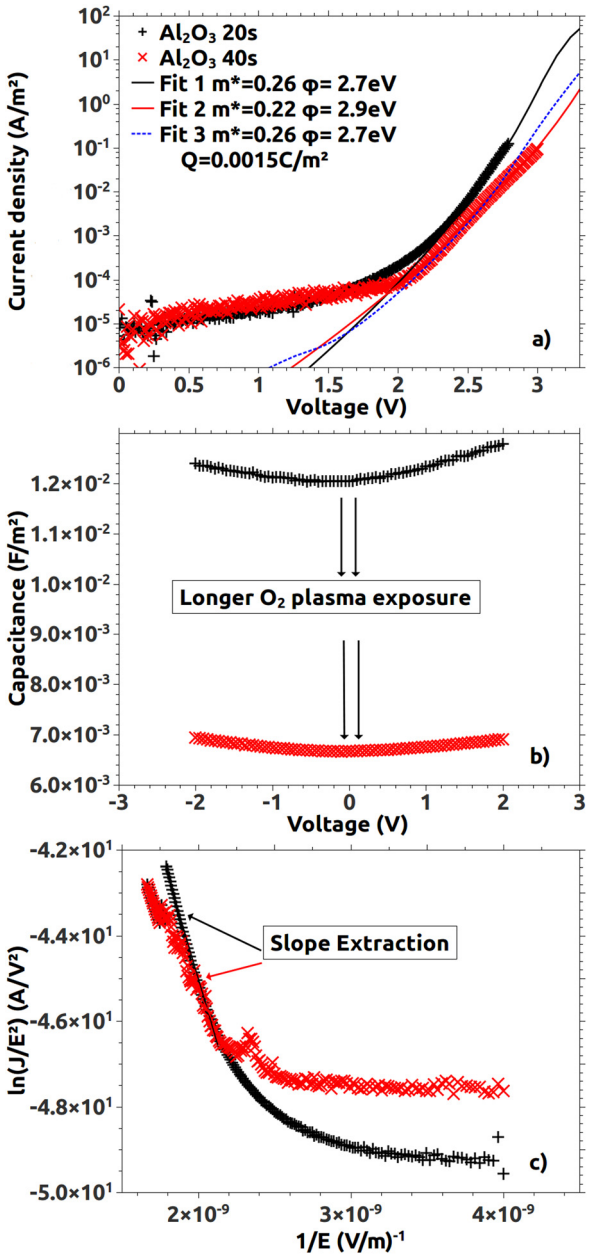

FIG. 2. (Color online) Effect of 20 s and 40 s exposure of Al_2O_3 to O_2 plasma on electrical properties; (a) J-V, (b) C-V, and (c) FN-plot (measurement at 300 K).

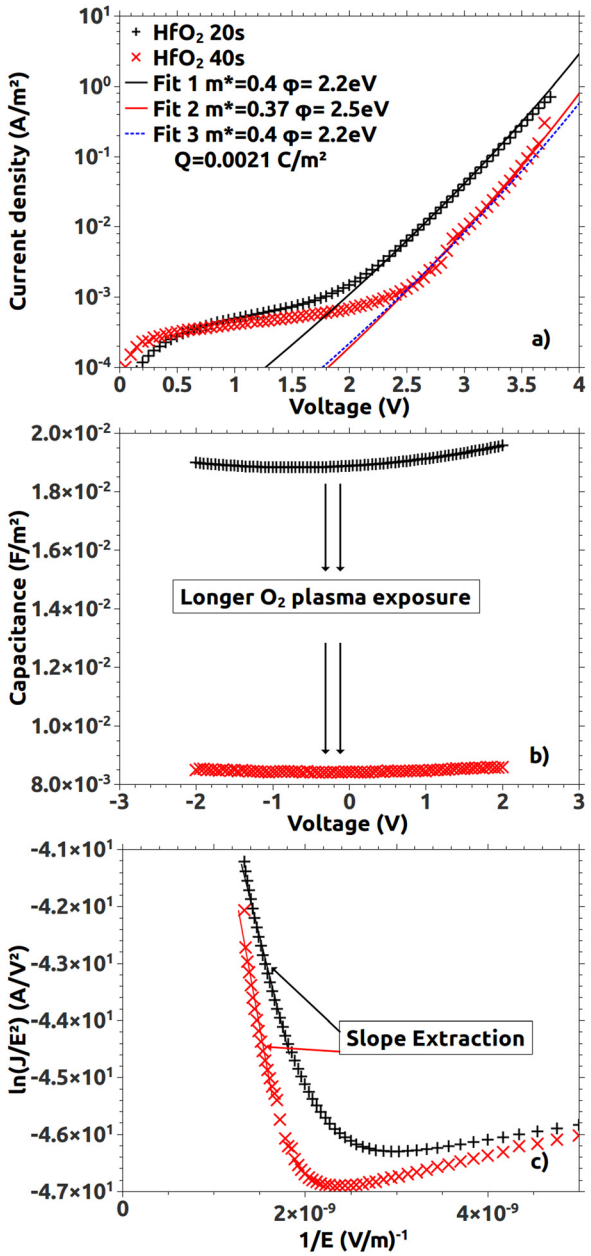

FIG. 3. (Color online) Effect of 20 s and 40 s exposure of HfO_2 to O_2 plasma on electrical properties; (a) J-V, (b) C-V, and (c) FN-plot (measurement at 300 K).

reduced with increasing pulse length.[12] This means that in addition to the removal of -CH_3 group by oxygen radicals, which happens during the first 20 s of exposure, the extended exposure may have formed a denser and amorphous Al-O-Al network, which is in agreement with the O/Al ratio.[13]

Currents for Al_2O_3 and HfO_2 films were plotted versus applied voltage in Figs. 2(a) and 3(a). From FN plots in Figs. 2(c) and 3(c), slopes were calculated at high electric field for the four studied dielectrics. Those slopes were used to extract barrier height Φ and effective mass m*, which were then verified against J-V characteristics at high electric field [in Figs. 2(a) and 3(a)]. The extracted parameters are described in Table II. It can be noticed that tunnel current was reduced (about 1 decade), which is marked by a shift to the right in positive voltage in Figs. 2(a) and 3(a). As additional negative charges within the dielectric would increase the potential barrier, this shift can be attributed to the increase in negative fixed charges.[14] It is known that Al_2O_3 and HfO_2 films can have important negative fixed charges density.[15,16] Negative fixed charges can be partially explained by the impact of vacuum ultraviolet radiation from the plasma. In fact, negative charge density is proportional to the plasma exposure time.[17,18] In Figs. 2(a) and 3(a), the third fit shows that the addition of negative charge density (0.0015 C/m^2 for Al_2O_3 and 0.0021 C/m^2 for HfO_2) to the studied films can explain the decrease in tunnel current. However, decrease in permittivity suggests change in the structure and composition of the material, which can

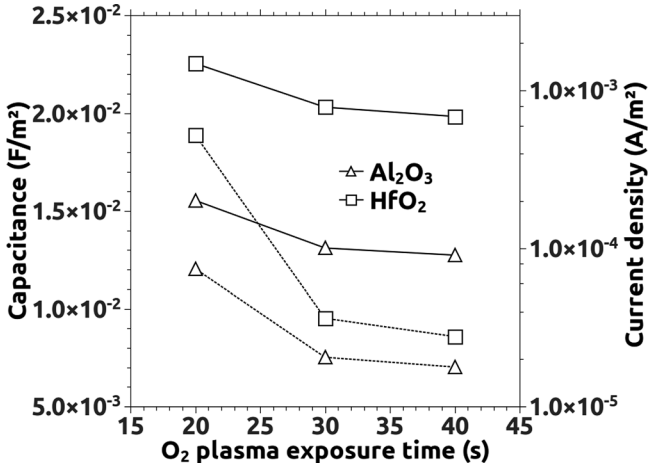

FIG. 4. Effect of PEALD *in situ* 300 W O_2 plasma exposition time on the Al_2O_3 and HfO_2 capacitance (continous lines) and current density at 2 V (dashed lines).

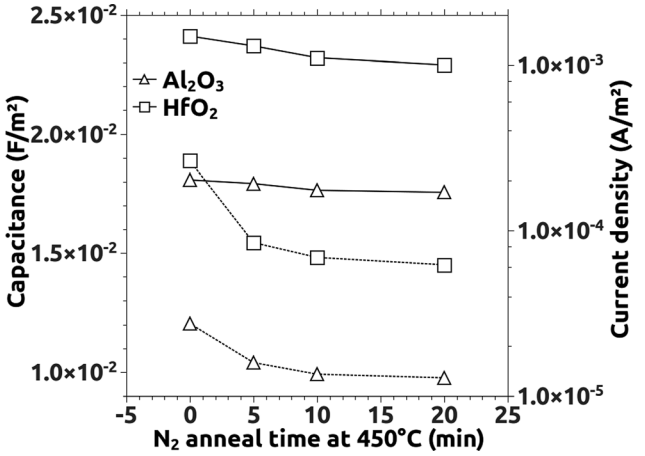

FIG. 5. Effect of annealing time at 450 °C in N_2 atmosphere on Al_2O_3 and HfO_2 capacitance (continuous lines) and current density at 2 V (dashed lines).

then impact the current levels. After all, at least from an electrical behavior point of view, the changes in the structure, composition, and negative fixed charge density can be represented as a modification of barrier height Φ and effective mass m*.

The effect of N_2 annealing on the capacitance and tunnel current was also investigated and results are displayed in Fig. 5. Al_2O_3 and HfO_2 were annealed in N_2 at 450 °C for 5, 10, and 20 min. The measured capacitance decreased after 5 min annealing at 450 °C to settle around 10 min annealing time (from 11.5 mF/m^2 to 9.2 mF/m^2 for Al_2O_3 and from 18.5 mF/m^2 to 14.2 mF/m^2 for HfO_2). In Fig. 5, for both Al_2O_3 and HfO_2, we notice a slight change in the current levels measured at 2 V for all samples for different annealing times (less than 30 μA/m^2 for Al_2O_3 and 45 μA/m^2 for HfO_2). Since capacitance is inversely proportional to thickness and tunnel current is inversely proportional to the exponential of the thickness, the slightest change in thickness would have affected considerably tunnel current. This argument reinforces the accuracy of the ellipsometry measurements evidencing no significant change in the dielectric thickness. Therefore, we attribute the decrease in capacitance and in tunnel current to the structural change in the dielectrics. In fact, N_2 annealing can also cause structural change to the dielectrics since it can influence the oxygen content and the oxygen vacancies in the studied dielectric film.[19]

IV. CRESTED BARRIER ENGINEERING

A TiO_x tunnel junction was first used for our metallic SET, where the low barrier height of this dielectric (~0.35 eV) insured a high tunnel current, but thermionic current was comparable to the tunnel current at room temperature.[20] In order to ensure high tunnel transparency and low thermionic current at moderate electrical fields, different crested barrier designs were investigated.[4,21] These designs aim to achieve an engineered variable oxide thickness (VARIOT) dielectric to optimize tunnel current.[21] By alternating the same ALD recipes of Al_2O_3 and HfO_2, we have achieved the crested structures composed of sandwiched layers of Al_2O_3 and HfO_2 as described in Fig. 6. Al_2O_3 and HfO_2 were deposited using a 20 s of O_2 plasma exposure. Additionally, structures U and A were deposited using a 40 s of O_2 plasma exposure to study the effect of longer plasma exposure on those crested barriers. *C-V* and *J-V* measurements were conducted in order to compare crested barriers against a 4.5 nm Al_2O_3 single layer. We thus aim to achieve higher transparency for the same or lower effective oxide thickness.

In Fig. 7(b), *C-V* measurements confirm that all the structures, deposited using a 20 s of O_2 plasma exposure have the same capacitance (~14.3 mF/m^2). Structures deposited using a 40 s of O_2 plasma exposure features a lower capacitance. However, measured capacitances for different structures are dissimilar (10.3 mF/m^2 for structure U and 9.0 mF/m^2 for

TABLE II. Extracted parameters at 300 K. C is the capacitance, Φ is the barrier height, m* is the effective mass, e^2/C_{tot} is the charging energy of an SET island having two tunnel junctions with 20 nm^2 capacitance area, $J_{Thermionic}$ and J_{tunnel} are thermionic and tunnel current, respectively, at 2 V bias.

Material	Plasma time (s)	Thickness (nm)	C (mF/m^2)	Φ (eV)	m*	$J_{Thermionic}$ (A/m^2)	J_{tunnel} (A/m^2)	e^2/C_{tot} (eV)
Al_2O_3	20 s	5	12.04	2.7	0.26	$<10^{-10}$	0.0002	0.31
	40 s	5	6.67	2.9	0.22	$<10^{-10}$	0.0001	0.53
HfO_2	20 s	5	18.87	2.2	0.4	$<10^{-10}$	0.0015	0.19
	40 s	5	8.43	2.5	0.37	$<10^{-10}$	0.0007	0.41
Crested U 20 s	20 s	6	14.4	—	—	$<10^{-10}$	0.5769	0.26
Crested U 40 s	40 s	6	10.3	—	—	$<10^{-10}$	0.0521	0.36

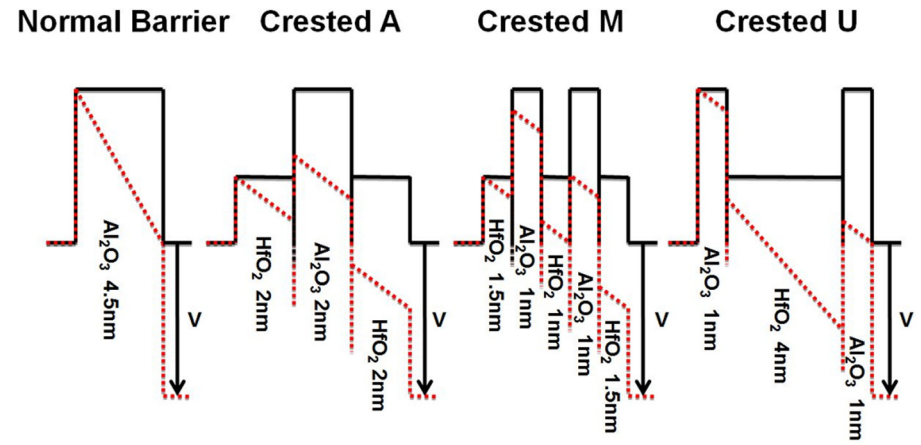

FIG. 6. (Color online) Crested barriers designs and associated layers thicknesses.

structure A) and are higher than expected ($\sim$8 mF/m^2). The longer plasma exposure could have favored the formation of different Al_2O_3–HfO_2 interfaces.

Using the different dielectric stacks composed of Al_2O_3 and HfO_2 (both of which have different barrier heights and dielectric constants), we have achieved a transparency of the tunnel junction that surpasses the transparency of a single layer. For 20 s of O_2 exposed films, we observe a higher current for all the crested structures compared to 4.5 nm of Al_2O_3 [Fig. 7(a)]. In fact, the structures A and M show similar behavior and higher current at lower electric field, while the structure U gives higher current at 1 V bias and above. These differences are mainly related to the design of those structures. In a specific structure, the voltage drop through each layer is related to its dielectric constant, its thickness, and the voltage drop through the other layers. In the case of the crested U, for instance, the voltage drop across the third layer corresponds to the voltage drop of the first layer plus the voltage drop of the second one. As a matter of fact, the current is higher since the third layer is completely transparent to tunnel current, while the current through the second layer is already in the Fowler–Nordheim regime (triangular barrier). In this specific case, the effective overall tunneling thickness is considerably reduced and tunnel current transparency is increased at low applied potentials.[8] Based on the same principle, tunnel junctions similar to structure U have been fabricated and measured.[22] The fabricated tunnel junctions were composed of 2 nm Al_2O_3—1 nm HfO_2—3 nm Al_2O_3 stack. Compared to structure U, this stack is in the same range of tunnel current density ($\sim$1 A/m^2 at 2 V).[22] As expected, structures deposited with a 40 s of O_2 plasma exposure shows lower tunnel current. Increase in negative fixed charge density can be the reason explaining that effect. However, the structure U exposed at 40 s of O_2 plasma still show high tunnel current at 40 s for a considerably lower capacitance.

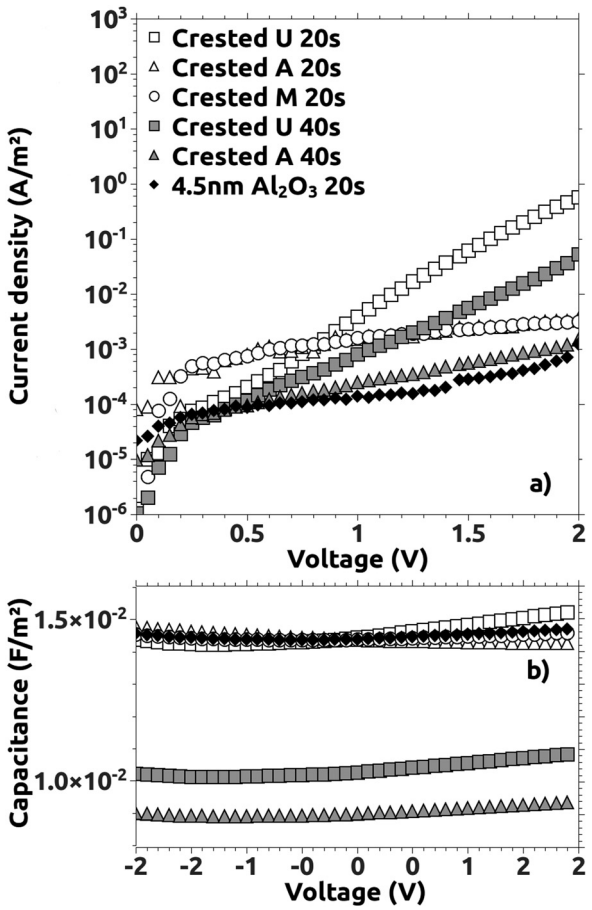

FIG. 7. Crested barriers: (a) C-V and (b) J-V electrical measurements.

Important parameters were summarized in Table II for the sake of comparison. For each capacitance, charging energy was calculated for a 20 nm^2 capacitance area, achieved for previously reported SETs.[5,7] All the structures have satisfactory charging energies ($e^2/C_{tot} > 0.13$ eV) for SET operation at room temperature. It is also noticeable that with the barrier heights of the studied materials ($\Phi > 2.2$ eV), thermionic current is not measurable while we could keep reasonable tunnel current values. It can be noticed in Table II that for structure U (for both 20 s and 40 s exposure), the current level is highly augmented compared to single layer structures, while the charging energy is kept to a reasonable level ($\sim 5k_BT$ @ 300 K) and thermionic current is beyond the measurement limits.

V. CONCLUSIONS

PEALD deposited dielectric layers offer clear advantages to microelectronic device development including the uniformity of the deposited layers. In this study, we have succeeded in enhancing the electrical properties of the deposited layers in order to attain the requirements of SET tunnel junction. This tunnel junction requires a low capacitance, high tunnel current levels, and low thermionic current. Low capacitances were achieved for both Al_2O_3 and HfO_2 using annealing and plasma exposure time. Moreover, the high potential barriers of the studied materials insured a low thermionic current level. We were also able to clearly enhance tunnel current levels using different stack designs composed of Al_2O_3 and HfO_2. The tunnel barrier engineering by means of adjusting deposition conditions are very promising for metallic SET application as it will allow increasing the operating temperature and enhancing electrical performance, especially the I_{ON}/I_{OFF} ratio. Therefore, this study is continuing in three ways (1) advanced analysis of electrical dielectric stack properties, e.g., charge density; (2) evaluating SiO_2 featuring low dielectric constant and high barrier dielectric to substitute Al_2O_3; (3) integration of the ALD crested barriers in the metallic SET process.

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