A MODIFIED BOOST CONVERTER WITH REDUCED INPUT CURRENT RIPPLE

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ABSTRACT

A Modified Boost Converter with Reduced Input Current Ripple

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Battery-powered trends in consumer electronics, transportation, and renewable energy sectors increase demands on DC/DC converter technology. Higher switching frequency and efficiency reduces solution size and cost, while increasing power capabilities. Still, switching noise remains the primary drawback associated with any DC/DC converter. Reducing a converter's input ripple helps prevent switching noise from spreading to other systems on a shared DC power bus. This thesis covers the analysis, simulation, and implementation of a recently-proposed boost converter topology, alongside an equivalent standard boost converter, operating in steady-state, continuous conduction mode. A Matlab-based simulation predicts each converter's input ripple performance using a state-space model. The converters' hardware implementation minimizes component and layout differences to create an equivalent comparison. The simulation and hardware measurements demonstrate a 40% input current ripple reduction using the modified topology. Replacing standard boost converters with the modified topology minimizes the switching noise conducted through a system's DC power network.

Keywords: dc/dc, boost, converter, input, current, ripple

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1. INTRODUCTION

Globally, electricity continues growing faster than any form of end-use energy consumption [1]. Many primary energy sources, including fossil fuels, nuclear, hydro, solar, and wind, fuel the electric power generation serving numerous end-uses. Between generation and end-use, power electronics control the electrical energy flow to countless systems. Electrical systems increasingly rely on power electronics as growing electricity demand strains global energy supplies.

Power electronics achieve high-efficiency energy transfer using switches. While on, an ideal switch conducts current without a voltage drop across the device. Conversely, the ideal switch does not conduct current while off, regardless of voltage imposed across the device. The product of voltage across the device and current through the device always remains zero, preventing the ideal switch from dissipating power. Transistors, diodes, and other semiconductor devices provide the electronic switching capability to realize power converters. General Electric introduced the first power semiconductor device, a thyristor, in 1958 [2]. Later technologies including power bipolar and field-effect transistors increased energy capacity and switching frequency. A power converter's switches alternately direct energy from the source into reactive storage elements, typically inductors and capacitors, and from storage elements to the load. This switch-mode behavior resembles a metro station, where trains periodically transfer passenger groups to their destination [3].

Power converters adapt energy flow between alternating current (AC) and direct current (DC) forms at varying voltage levels. These circuits commonly perform a combination of rectification (AC/DC conversion), inversion (DC/AC conversion), and

step-up or step-down DC/DC conversion. Traditional electronic power supplies step-down AC line voltage through a large 60-Hz transformer, rectify the low-voltage AC, and distribute power to different subsystems using linear voltage regulators. DC/DC converters eliminate the need for bulky transformers and inefficient linear regulators by increasing (step-up) or decreasing (step-down) DC voltages. High-efficiency and high-frequency operation minimize heat dissipation and magnetic component size, reducing overall power supply size. These characteristics enable the miniaturization of modern electronic devices.

Today, DC power source trends increase systems' DC/DC converter performance demands. Portable electronics need high efficiency to reduce size and extend battery life. Battery electric vehicles operate at high DC voltages to manage increasing power requirements. Microinverters for solar photovoltaic (PV) modules often include intermediate DC/DC conversion to reach appropriate AC output voltage levels. These trends point toward increased DC/DC converter deployment and a need to continue improving converter performance.

2. BACKGROUND

2.1 Switching Noise

The primary drawback associated with DC/DC converters, switching noise, presents a significant challenge for system engineers. Switch-mode operation adds AC ripple to a converter's DC input and output signals. Poorly designed DC/DC converters allow this switching noise to spread to nearby circuits, causing electromagnetic interference (EMI). EMI refers to undesired conducted or radiated electromagnetic signals that degrade or impair the performance of electrical systems. Minimizing switching noise and preventing its transmission helps improve system reliability.

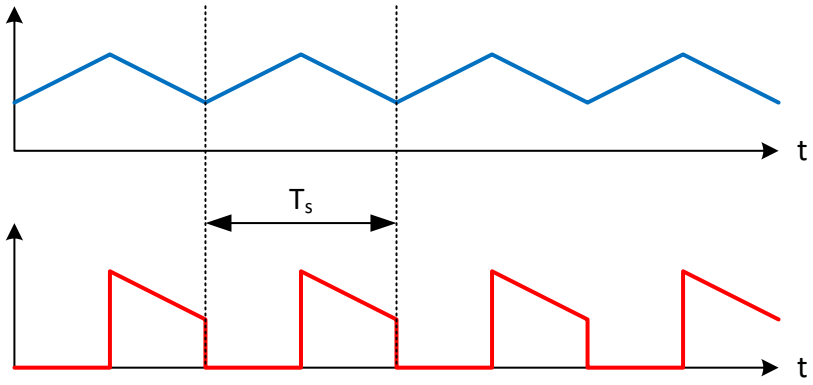

Figure 2-1. Typical Triangular and Trapezoidal Switching Waveforms

Switching noise spreads through both electromagnetic conduction and radiation. DC/DC converters typically produce triangular and trapezoidal waveforms such as those shown in Figure 2-1. These waveforms carry significant energy at the switching frequency (2-1) and its harmonics which typically sit between 100 kHz and several MHz. The sharp transitions particularly associated with trapezoidal waveforms contain energy at much higher frequencies in the GHz range. Conduction dominates EMI transmission at

lower frequencies, before parasitic effects dominate electrical circuits, and radiation increases at higher frequencies, when wavelength approaches physical conductor length.

$$f = \frac{1}{T} \qquad (2-1)$$

EMI regulations reflect the characteristics of switching noise among other sources. Typical tests limit conducted emissions between 150 kHz to 30 MHz and radiated emissions from 30 MHz to 2 GHz. Government regulators impose EMI limits to ensure electrical interoperability, particularly among wireless electronics and power supplies connected to the AC grid. Mitigating switching noise helps achieve EMI compliance in many applications. At a system level, specific grounding and shielding techniques reduce conducted and radiated EMI introduced by switching noise sources [4]. Switching noise also propagates within systems from power converters to nearby signal conductors [5]. Printed circuit board (PCB) layout and grounding techniques help minimize EMI radiation along high-frequency current paths [6] [7]. These approaches primarily focus on containing radiated switching noise emission. Preventing switching noise conduction relies on reducing or containing ripple at the power converter's input and output terminals.

2.2 Input Ripple

The discontinuous currents caused by switch-mode operation add an AC ripple component to any DC/DC converter's input current. When input current ripple conducts through a voltage source, switching noise spreads to other circuits connected to the same source. This conducted EMI significantly impacts systems that draw power from rectified AC-line voltage or a battery. Current ripple also adversely impacts maximum power

point tracking (MPPT) and the transfer efficiency of solar photovoltaic modules [8] [9]. Reducing the current ripple seen by a converter's input source beneficially impacts many systems.

Designers may choose a DC/DC converter topology based on the relative amount of current ripple introduced. Inductor-fed topologies (boost, Cuk, and SEPIC) produce significantly less input current ripple than switch-fed topologies (buck and buck-boost). At a minimum, most designs employ an input capacitor for input ripple reduction. This simple solution provides adequate filtering performance for some applications. High-performance converters must incorporate additional input ripple reduction methods, including more complex filters, multiphase interleaving, and specialized topologies.

2.3 Input Filters

Adding a filter between the input source and power converter provides bi-directional noise isolation. Figure 2-2 displays the general input filter configuration, using a low-pass response to attenuate high-frequency AC ripple. The filter attenuates both voltage ripple introduced by the source and current ripple introduced by the converter. This behavior prevents noise from spreading between systems connected to the same voltage source, such as a battery or rectified line voltage feeding multiple DC/DC converters. Input filters help system designers contain EMI without changing the DC/DC converter topology.

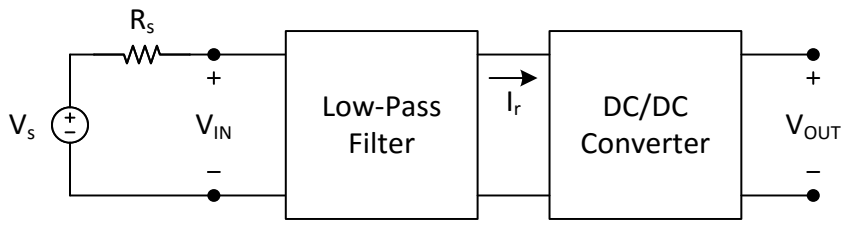

Figure 2-2. DC/DC Converter with Input Filter Network

Though adding the filter improves ripple suppression, the interaction between filter and converter may destabilize the system. Yu and Biess first described these conditions in 1971 [10]. Later analysis performed by R. D. Middlebrook, provided graphical criteria that predict instability when the filter's output impedance exceeds the converter's input impedance at any frequency [11] [12]. Middlebrook developed a canonical DC/DC converter model capable of predicting a converter's input impedance based on design parameters [11] [12]. Figure 2-3 presents the canonical converter input impedance determined by the converter's inductance, output capacitance, and load resistance. Jang and Erickson later adapted the Middlebrook criteria to predict instability in current-mode controlled converters [13]. These tools provide the means to design an input filter in conjunction with a converter or as a modification to an existing converter.

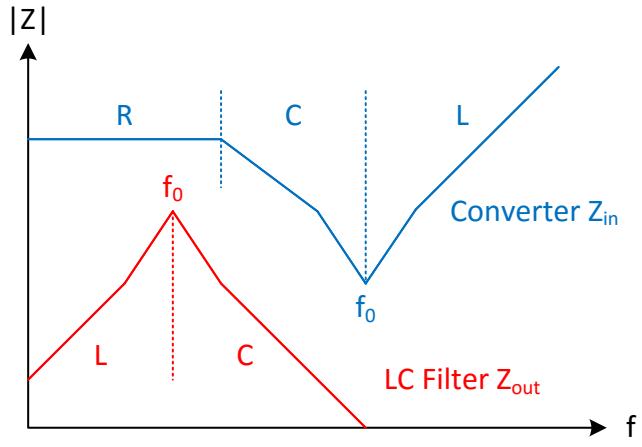

Figure 2-3. Middlebrook Criteria with Generic Impedance Curves

Higher-order input filters present instability risk due to resonant behavior. A generic LC filter exhibits output impedance characteristics of the form shown in Figure 2-3. Resonant frequency location and damping factor determine whether the filter violates the Middlebrook criteria. Lowering the filter's resonant frequency eases damping requirements but increases the filter component sizes. Figure 2-4 presents two damped LC filter circuits; Erickson demonstrates optimal damping for both filters [14]. Yu and Salato offer a damping technique that uses the LC filter's parasitic series resistances to minimize the number of filter components [15]. Most input filter design approaches either seek to minimize the filter's impact on converter performance or the filter's cost (number of components, size, etc.) [16] [17] [18] [19].

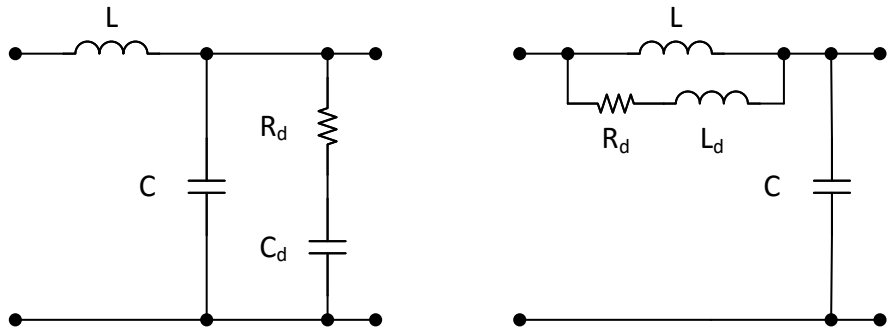

Figure 2-4. Shunt (Left) and Parallel (Right) Damped LC Filters

Input filter designers minimize conducted EMI in new or existing systems. Input filters help compensate for noisy converter topologies. The filter must be designed to prevent impacting the DC/DC converter's stability by employing one of many available damping techniques. An optimally designed input filter reduces switching noise conduction, without impacting transient response, at minimal additional cost and physical size.

2.4 Interleaved Multiphase

High-power applications often require multiphase power converters, which operate several implementations of the same converter topology in parallel. In these designs, each phase only provides a fraction of the total load, reducing the converter's total power dissipation [20]. Low-voltage, high-power computer processor applications influence many designs based around the multiphase buck topology [21] [22] [23].

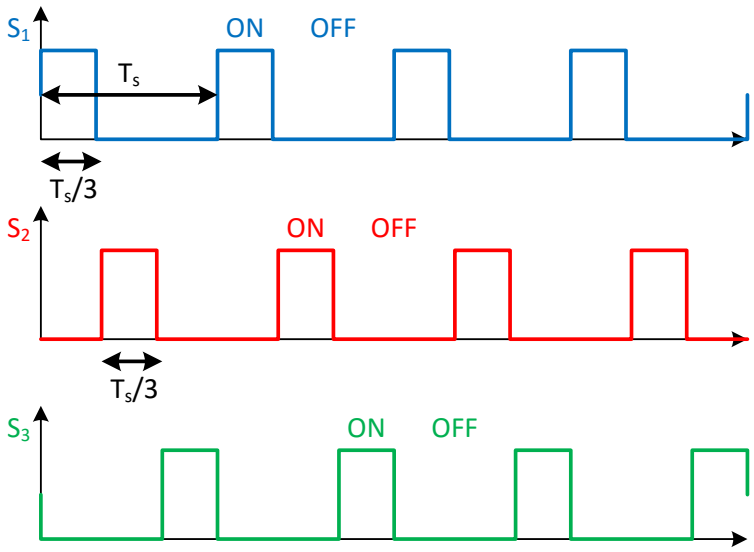

Figure 2-5. Three-Phase Interleaved Switching

Interleaving the multiphase converter's switching signals reduces the ripple introduced and scales the ripple frequency proportional to the number of phases. Interleaved switching signals turn on each phase alternately rather than in unison. Figure 2-5 demonstrates three-phase interleaved switching. The switching controller implements interleaving by introducing a proportional delay between each converter phase. The delayed current waveforms sum at the input and output terminals, and the resulting ripple appears at a multiple of the switching frequency. Table 2-1 summarizes the relationship between the number of converter phases, switching delay, and overall ripple frequency.

Table 2-1. Interleaved Multiphase Converter Properties

Number of Phases	Switching Delay	Ripple Frequency
2	$\frac{1}{2}T$	$2f$
3	$\frac{1}{3}T$	$3f$
4	$\frac{1}{4}T$	$4f$

Interleaving creates ripple reduction because of the delay between each phase. The duty cycle, shared across all phases, determines the ripple cancellation. Figure 2-6 demonstrates current ripple cancellation at the output terminal of a two-phase buck converter. The inductor current ripple flowing through the output capacitor cancels, when the converter operates at a 50% duty cycle. Similarly, a three-phase converter would achieve complete ripple cancellation at 33% and 67% duty cycles, and a four-phase converter would achieve complete cancellation at 25%, 50%, and 75%.

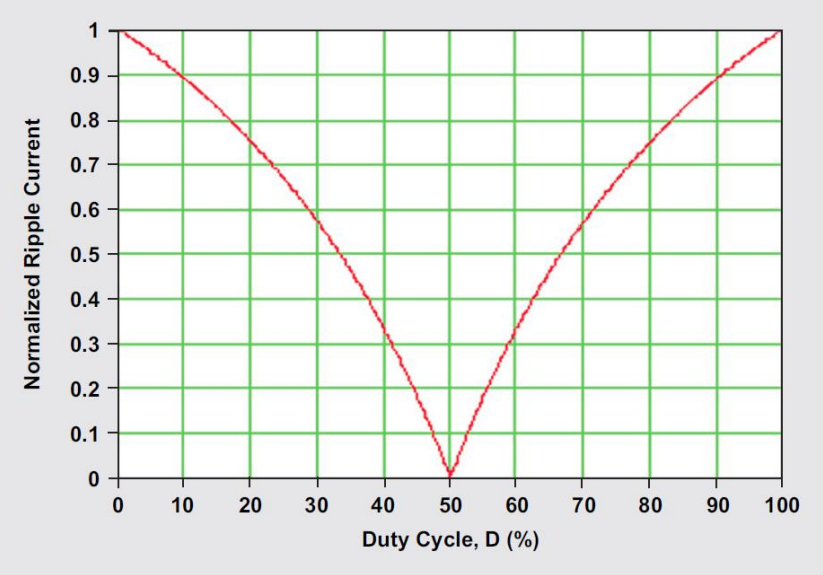

Figure 2-6. Two-Phase Buck Converter Current Ripple Cancellation [20]

The combined ripple cancellation and frequency scaling eases filtering requirements. A multiphase converter requires a much smaller filter than a single-phase converter to achieve equivalent ripple performance. Ripple cancellation also reduces the inductance per phase required to match single-phase performance. These characteristics decrease the solution size for high-power applications. However, the relationship between duty cycle and ripple cancellation restricts design choices. A two-phase converter only achieves significant ripple reduction at duty cycle around 50%. Increasing the number of phases provides more options, but significantly increases design complexity.

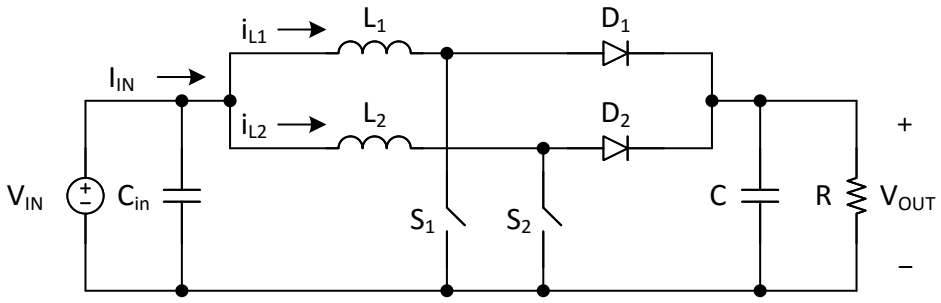

Figure 2-7. Two-Phase Boost Converter

Parallel converters in a multiphase solution reduce the conduction losses associated with a large input current, and interleaved switching provides some ripple cancellation. A multiphase boost converter, shown in Figure 2-7, also exhibits inductor ripple cancellation properties at the input terminal [24]. High-power solar PV inverters benefit from using multiphase boost converters because of current sharing and ripple cancellation [25] [26]. These converters undoubtedly improve efficiency, but restrict duty cycle selection when operated for maximum ripple reduction.

2.5 Boost Converter

Figure 2-8 depicts the boost topology, a standard DC/DC step-up converter, which contains a single switch and operates alternately between two states: switch-on and switch-off.

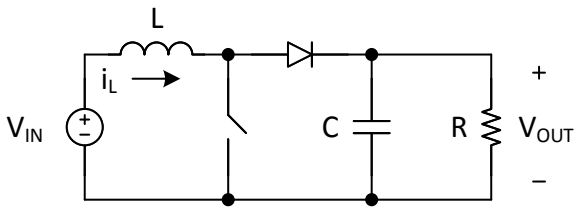

Figure 2-8. Standard Boost Converter Topology

Duty cycle, referred to as a percentage or a ratio less than unity, relates the switching period to the time spent in the switch-on (2-2) and switch-off (2-3) states.

$$t_{ON} = D \cdot T \qquad (2-2)$$

$$t_{OFF} = (1 - D) \cdot T \qquad (2-3)$$

Circuit operation depends on the relationship between inductor current and voltage (2-4).

$$V_L = L \cdot \frac{di_L}{dt} \qquad (2-4)$$

Turning the switch on and off changes the voltage applied across the inductor, alternately increasing and decreasing inductor current. This action, stores energy from the input source in the inductor's magnetic field, and then releases energy to the load. Because the converter always applies voltage across the inductor, the converter's input current never settles to a flat DC level. Inductor current ripple manifests as input current ripple in a boost converter.

2.5.1 Switch-ON State

In the switch-on state, the inductor stores energy from the input, while the capacitor releases energy to drive the load. Turning the switch on, reverse biases the diode, separating the circuit's two halves as in Figure 2-9.

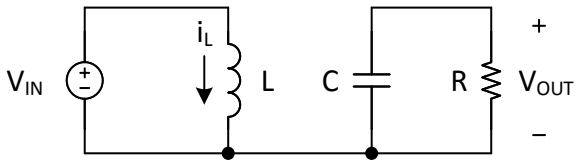

Figure 2-9. Boost Converter Switch-ON State

The inductor current ramps up with slope (2-5) defined by equation (2-4). Constant input voltage guarantees a fixed linear slope (2-6), equivalent to the change in current relative to the time spent in the switch-on state (2-2). This equivalence leads to a description of the peak-to-peak current ripple (2-7).

$$\frac{di_L}{dt} = \frac{V_{IN}}{L} \qquad (2-5)$$

$$\frac{\Delta i_{L(ON)}}{\Delta t_{ON}} = \frac{V_{IN}}{L} \qquad (2-6)$$

$$\Delta i_{L(ON)} = \frac{V_{IN} \cdot DT}{L} \qquad (2-7)$$

2.5.2 Switch-OFF State

In the switch-off state, energy from input source and energy stored in the inductor flow to the capacitor and load. With the switch off, the diode becomes forward biased and connects the inductor to the output node as in Figure 2-10.

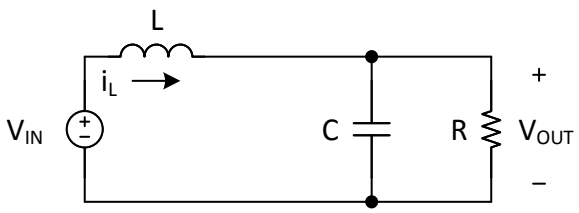

Figure 2-10. Boost Converter Switch-OFF State

The difference between input and output voltage determines inductor current slope (2-8) while the switch remains 'OFF'. Assuming constant DC input and output voltage, the switch-off state also exhibits linear inductor current slope (2-9). Equation (2-10) presents the peak-to-peak inductor current ripple during the switch-off state.

$$\frac{di_L}{dt} = \frac{V_{IN} - V_{OUT}}{L} \qquad (2-8)$$

$$\frac{\Delta i_{L(OFF)}}{\Delta t_{OFF}} = \frac{V_{IN} - V_{OUT}}{L} \qquad (2-9)$$

$$\Delta i_{L(OFF)} = \frac{(V_{IN} - V_{OUT}) \cdot (1 - D)T}{L} \qquad (2-10)$$

2.5.3 DC Transfer Function

Under steady-state operating conditions, inductor current reaches a fixed DC value. Figure 2-11 depicts these conditions, where net inductor current change reaches zero.

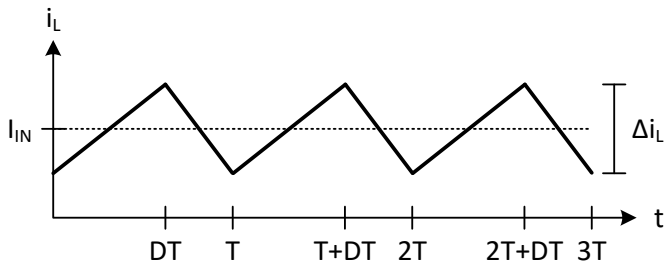

Figure 2-11. Boost Converter Steady-State Inductor Current

Equation (2-11) describes the steady-state operating condition mathematically.

$$\Delta i_{L(ON)} = \Delta i_{L(OFF)} \qquad (2-11)$$

Substituting the inductor current ripple expressions in the switch-on (2-7) and switch-off (2-10) state leads to the boost converter's DC voltage transfer function (2-13).

$$\frac{V_{IN} \cdot DT}{L} = \frac{(V_{IN} - V_{OUT}) \cdot (1-D)T}{L} \qquad (2-12)$$

$$V_{OUT} = \frac{V_{IN}}{(1-D)} \qquad (2-13)$$

The ideal power relationship (2-14), in a lossless converter, extends the DC voltage transfer function to the DC current transfer function (2-15).

$$P_{OUT} = V_{OUT} I_{OUT} = P_{IN} = V_{IN} I_{IN} \qquad (2-14)$$

$$I_{IN} = \frac{I_{OUT}}{(1-D)} \qquad (2-15)$$

2.5.4 Continuous Conduction Mode Operation

A DC/DC converter's inductor current describes the operating mode. Continuous conduction mode (CCM) implies inductor current flow throughout the switching cycle. Discontinuous conduction mode (DCM) occurs when the inductor current drops to zero during the switch-off state. In this scenario, the diode prevents negative current flow and

the inductor current remains at zero until the next switch-on cycle. DCM naturally occurs, when a converter operates under light loads well below specified maximums. The general converter design process assumes CCM operation at maximum rated load.

A special CCM case called boundary conduction mode (BCM), illustrated by Figure 2-12, delineates the barrier between CCM and DCM. BCM represents the minimum conditions for CCM operation.

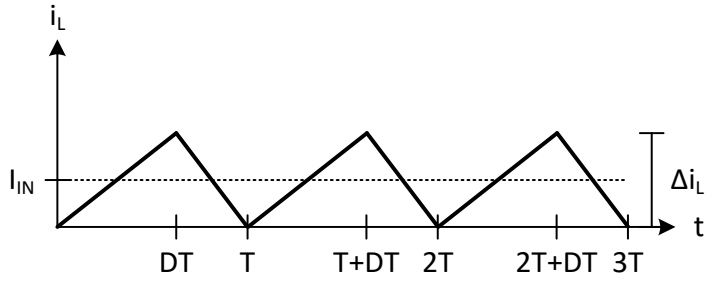

Figure 2-12. Boost Converter BCM Inductor Current

Maintaining CCM operation constrains inductor current ripple given the desired average inductor current level. The BCM constraint (2-16) describes a minimum inductance, known as the critical inductance (2-17) required to maintain continuous conduction.

$$\frac{\Delta i_L}{2} \leq I_L \qquad (2-16)$$

$$L_c \geq \frac{V_{IN} \cdot DT}{2I_{IN}} \qquad (2-17)$$

2.5.5 Component Ratings

Voltage and current waveforms help determine each component's basic ratings. Manufacturers specify voltage ratings as peak values and current ratings as average or

RMS values. Figure 2-13 defines component current and voltage polarities in the boost converter.

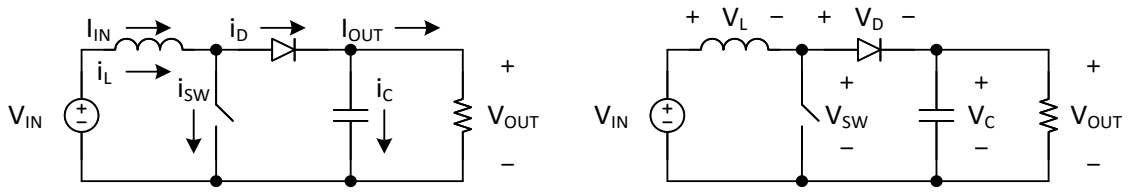

Figure 2-13. Boost Converter Current and Voltage Polarities

Inductor current splits between the switch and diode. These components conduct alternately; the switch carries the inductor current during the ‘ON’ state and the diode carries the inductor current during the ‘OFF’ state. Diode current splits between the output capacitor and the load. The load conducts the DC output current and the output capacitor conducts the AC component of the diode current. Figure 2-14 depicts the current waveforms for each component.

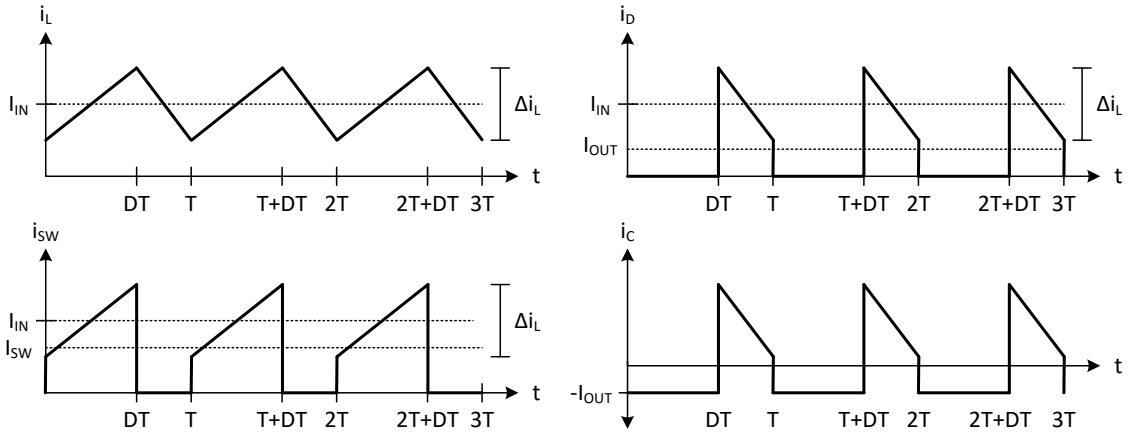

Figure 2-14. Boost Converter Current Waveforms

During the switch-on state, the inductor see the input voltage and the reverse-biased diode sees the output voltage. During the switch-off state, the inductor sees a

negative voltage, equal to the difference between input and output voltages, while the switch sees the output voltage across its terminals. Capacitor voltage always equals the output voltage, including the additional ripple caused by integrating the capacitor current. Figure 2-15 illustrates each component's voltage waveform.

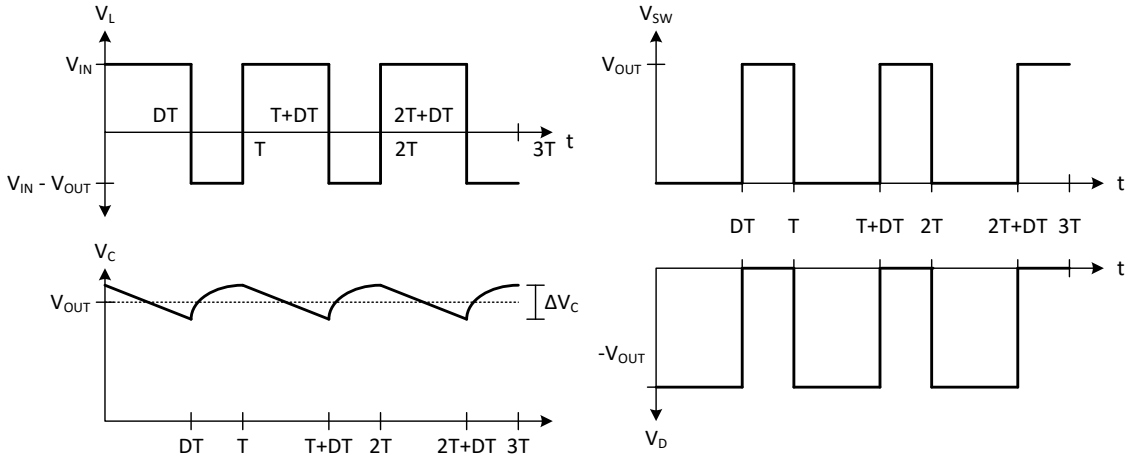

Figure 2-15. Boost Converter Voltage Waveforms

Table 2-2 summarizes the boost converter's relevant component ratings determined based on voltage and current waveforms.

Table 2-2. Boost Converter Component Ratings [27]

Component	Rating	Value
Switch	Drain Current	$I_d > I_{IN} \cdot D$
	Drain-Source Voltage	$V_{ds} > V_{OUT}$
Diode	Forward Current	$I_F > I_{OUT}$
	Max. Repetitive Reverse Voltage	$V_{rrm} > V_{OUT}$
Capacitor	DC Voltage	$V_{C(\max)} > V_{OUT} + \frac{\Delta V_{OUT}}{2}$
Inductor	Saturation Current	$I_{sat} > I_{IN} + \frac{\Delta i_L}{2}$
	RMS Current	$I_{rms} > \sqrt{{I_{IN}}^2 + \frac{{\Delta i_L}^2}{12}}$

2.5.6 Capacitor Sizing

Capacitors handle the AC current ripple at a DC/DC converter's input and output terminals. During steady-state operation, the net charge stored and released by a capacitor must approach zero over the switching cycle. Charging and discharging the capacitor introduces voltage ripple across the capacitor (2-18), the primary design parameter associated with input and output capacitors.

$$\Delta V = \frac{Q}{C} \qquad (2-18)$$

Integrating the positive or negative portion of the ripple current over a half switching cycle specifies the maximum charge stored or released by the capacitor. Figure 2-16 applies this technique to a boost converter's output capacitor.

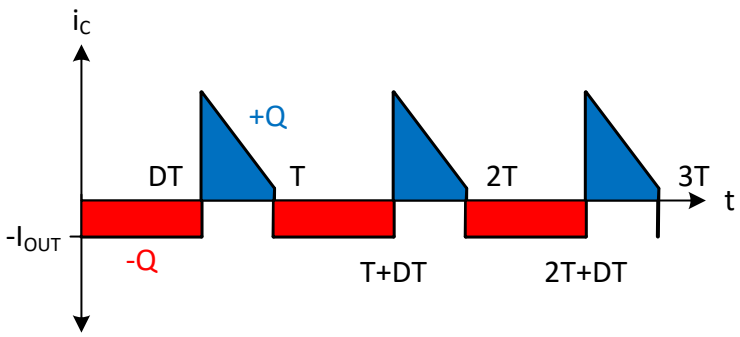

Figure 2-16. Boost Converter Output Capacitor Charge Storage

The DC output current and switching cycle parameters determine the output capacitor charge (2-19). Combining equations (2-18), (2-19), and (2-20) expresses the required output capacitance to achieve a specified voltage ripple ratio (2-21).

$$Q_{C_{out}} = I_{OUT} \cdot D \cdot T \qquad (2-19)$$

$$I_{OUT} = \frac{V_{OUT}}{R} \qquad (2-20)$$

$$C_{out} = \frac{D \cdot T}{R \cdot \frac{\Delta V_{out}}{V_{OUT}}} \qquad (2-21)$$

Though often omitted from schematics during theoretical analysis, practical DC/DC converter implementations require an input capacitor. This provides a low-impedance source for high-frequency current ripple drawn by the converter. Inductor current ripple determines the charge stored on a boost converter's input capacitor, as Figure 2-17 depicts.

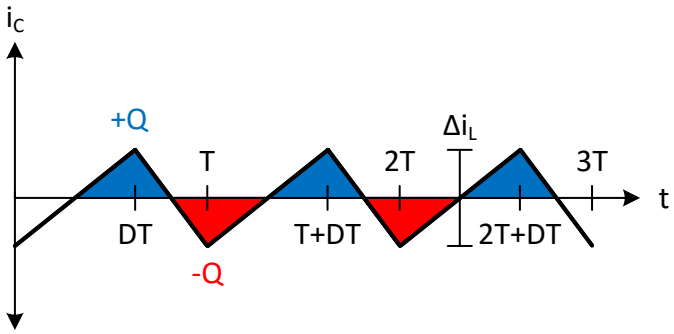

Figure 2-17. Boost Converter Input Capacitor Charge Storage

Like the output, input voltage ripple requirements determine input capacitance. Applying inductor current ripple (2-7) and input capacitor charge (2-22) expressions to the capacitor's charge-voltage relationship (2-18) specifies input capacitance in terms of converter parameters and input voltage ripple specifications (2-23).

$$Q_{C_{in}} = \frac{\Delta i_L \cdot T}{8} \qquad (2-22)$$

$$C_{in} = \frac{D \cdot T^2}{8L \cdot \frac{\Delta V_{IN}}{V_{IN}}} \qquad (2-23)$$

2.6 Novel and Modified Topologies

Many step-up converter applications require performance beyond the standard boost converter's capabilities. Such needs produce novel step-up topologies designed to optimize different performance criteria; including efficiency, ripple performance, step-up conversion ratio, size, and cost [28] [29] [30] [31].

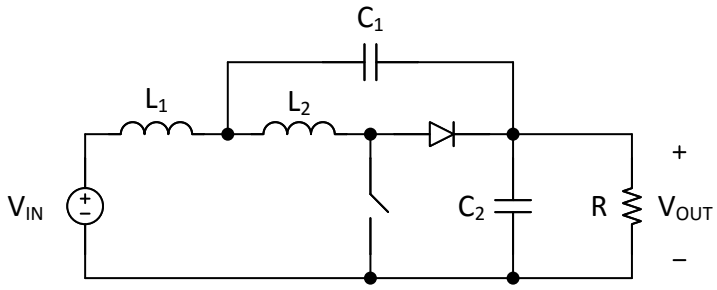

Figure 2-18. Modified Boost Converter

New and modified topologies trade additional complexity for performance enhancement. Figure 2-18 shows a relatively simple modification proposed by Karanam as part of a step-up inverter application [32]. Karanam implemented the modified boost converter, focusing on performance of the inverter rather than the boost converter itself. Using analysis, simulation, and hardware implementation techniques, this work intends to prove the following thesis statement. During steady-state, CCM operation, Karanam's modified boost converter provides a 40% input current ripple reduction compared against an equivalent standard boost converter.

3. DESIGN REQUIREMENTS

Comparing two related converter topologies requires common performance criteria and design constraints. Equivalent operating conditions and performance measurements ensure proper evaluation of topological converter modifications. This performance comparison primarily concerns the converter's input current ripple, measured through the input inductor. Physical size and cost constitute secondary comparative concerns as some applications value performance over size and cost. A valid performance comparison requires uniform design constraints on input voltage, output voltage, output power, switching frequency, inductance, input capacitance, and output capacitance. Selecting these parameters per standard boost converter characteristics establishes the comparative baseline.

3.1 Current Ripple Performance

Input current ripple relates to the converter's inductor current ripple, especially in boost topologies which place the inductor at the input terminal. Current ripple measurements typically concern the peak-to-peak value. But specifications typically remain relative to the established DC current level, as a percentage much like voltage ripple. The boost topology's input current ripple percentage (3-1) relates directly to peak-to-peak inductor current ripple (2-7) and DC input current (2-14).

$$\%\Delta i_{IN} = \frac{\Delta i_L}{I_{IN}} \qquad (3-1)$$

$$\%\Delta i_{IN} = \frac{{V_{IN}}^2 \cdot D}{L \cdot f \cdot P_{OUT}} \qquad (3-2)$$

Specific applications dictate the tolerable inductor current ripple percentage. Generally, most design guidelines suggest ripple below 40%. Choosing a relatively large ripple percentage differentiates a topological modification that reduces ripple. Targeting 40% current ripple in a standard boost design provides adequate opportunity to improve performance without exceeding practical limits.

3.2 Functional Parameters

A DC/DC converter's functional parameters determine the component values that complete the converter's design requirements. Table 3-1 summarizes the chosen functional parameters for both boost converters. Three factors influence power and voltage level selection: DC input current, DC voltage gain, and laboratory power supply capabilities. DC/DC converters with large DC input current require larger inductors to achieve low current ripple. A topological modification designed to reduce input current ripple provides greater benefit among converter with large DC input current. Because DC voltage gain correlates with DC input current, high-gain converters also benefit from input ripple current reduction. The available DC power supplies also informed power and voltage parameters. The voltage ripple values reflect compensation for non-ideal capacitors, which produce more ripple due to equivalent series resistance (ESR).

Table 3-1. Functional Converter Parameters

Parameter	Value
Output Power	30 W
Output Voltage	20 V
Input Voltage	6 V
Output Voltage Ripple	0.5%
Input Voltage Ripple	0.5%
Inductor Current Ripple	40%

3.3 Standard Boost Design

The functional parameters listed in Table 3-1 determine converter component values and operating conditions. Two key operating conditions, duty cycle (3-3) and load resistance (3-4), directly relate to functional power and voltage levels.

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \qquad (3-3)$$

$$R = \frac{{V_{OUT}}^2}{P_{OUT}} \qquad (3-4)$$

The chose power and voltage levels specify a 70% duty cycle and 13.333Ω load resistance.

$$D = 1 - \frac{6\ V}{20\ V} = 0.7$$

$$R = \frac{(20\ V)^2}{30\ W} = 13.333\ \Omega$$

A third operating condition, switching frequency, provides a degree of freedom to adjust component values. Increased switching frequency reduces the inductor (3-5), output capacitor (2-21) and input capacitor (2-23) component values. Because the performance comparison regards inductor current ripple, switching frequency's impact on inductor value outweighs the impact on capacitor values.

$$L = \frac{{V_{IN}}^2 \cdot D}{\%\Delta i_{IN} \cdot f \cdot P_{OUT}} \qquad (3-5)$$

Switching frequency also constrains switching controller selection. Some controllers offer adjustable switching frequency, while others operate at a fixed frequency. Generally, most controllers operate between 100 kHz and 2 MHz. Selecting a

200 kHz switching frequency keeps all three component values within reasonable ranges and preserves a wide selection of switching controllers.

$$L = \frac{(6\ V)^2 \cdot 0.7}{0.4 \cdot (200\ kHz) \cdot (30\ W)} = 10.5\ \mu H$$

$$C_{out} = \frac{D \cdot T_s}{R \cdot \frac{\Delta V_{out}}{V_{OUT}}} = \frac{0.7 \cdot (5\ \mu s)}{(13.333\ \Omega) \cdot (0.005)} = 52.5\ \mu F$$

$$C_{in} = \frac{D \cdot {T_s}^2}{8L \cdot \frac{\Delta V_{IN}}{V_{IN}}} = \frac{0.7 \cdot (5\ \mu s)^2}{8 \cdot (10\ \mu H) \cdot (0.005)} = 43.75\ \mu F$$

Table 3-2 presents the complete design requirements, derived from the functional parameters and stated design goals, using standard boost converter relationships. These constraints establish the baseline performance of the standard boost converter and limit the modified design to validate the performance comparison.

Table 3-2. Converter Design Parameters

Parameter	Value
Output Power	30 W
Output Voltage	20 V
Output Current	1.5 A
Input Voltage	6 V
Input Current	5 A
Load Resistance	13.333 Ω
Switching Frequency	200 kHz
Switch Duty Cycle	70%
Inductance	10 µH
Output Capacitance	50 µF
Input Capacitance	44 µF

4. ANALYSIS AND SIMULATION

Basic converter analysis techniques describe converter performance by exploiting inductor current slope assumptions. These assumptions eliminate the need to solve the underlying differential equations that describe inductor current and capacitor voltage. Section 2.5 presents a typical boost converter analysis assuming a linear inductor current slope during both switching states. Linear inductor current slope implies pure DC voltage across the inductor and a converter switching frequency higher than the converter's LC resonant frequency. These assumptions remain valid for properly-designed boost converters, and the simple analysis accurately predicts inductor current ripple.

The modified boost converter topology challenges the assumptions that facilitate simplified analysis. Assuming the converter's switching frequency exceeds the circuit's resonant frequencies, linear current slope analysis predicts large L_2 current ripple, proportional to V_{IN}, and zero L_1 current ripple, based on the DC voltages Figure 4-1 depicts across each inductor.

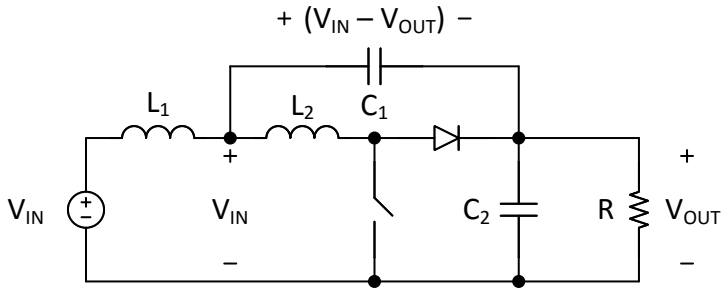

Figure 4-1. Modified Boost Converter DC Voltages

This simple analysis ignores the small voltage ripple on both capacitors, which induces a small current ripple in both inductors. The linear current slope analysis remains accurate when large current ripple introduced by DC voltage across the inductor masks

the small addition. In the modified boost converter, simple analysis accurately predicts L_2 current ripple, but not L_1 current ripple, which depends entirely on small AC voltage ripple applied across the inductor. Therefore, input current ripple prediction requires more complex analysis of the modified boost converter.

State space analysis describes a DC/DC converter using a set of time differential equations. Averaging the state space representations during switch-on and switch-off operation provides the converter's DC transfer function, verifying boost-type behavior. Transformation to the *m*-domain, normalizes the time-domain state equation over the converter's switching period. Solving the *m*-domain state equation describes steady-state converter behavior. Unlike sinusoidal waveforms, analytical switching waveform expressions provide little intuition towards performance measurements such as peak-to-peak, RMS, and average values [33]. Computer-aided, numerical solutions provide relevant boost converter performance measurements, particularly peak-to-peak and percent input current ripple, facilitating converter design choices. Analyzing the known standard topology alongside the modified topology validates the steady-state model.

4.1 State Space Analysis

The state space analysis method describes a system's dynamic elements, state variables, as a set of first-order differential equations known as the state equation. DC/DC converters require a state equation, for each switching state. Control loop and DC transfer function analysis rely on the averaged state equation over all the converter's switching states. Combining the individual state equations sequentially describes the converter's dynamic behavior across the complete switching cycle.

Energy storage elements, capacitors and inductors, determine a DC/DC converter's dynamic behavior. Simple differential relationships make inductor currents and capacitor voltages the best state variable choices. Circuit analysis completes the associated first order differential equations. Kirchhoff's voltage law (KVL) replaces inductor voltage with capacitor voltage state variables and Kirchhoff's current law (KCL) replaces capacitor current with inductor current state variables. The complete state equation describes each state variable's derivative using the system's state variables and inputs.

4.1.1 Standard Boost Converter

The standard boost converter's state model requires two state variables, inductor current, i_L, and output voltage, v_o, shown in Figure 4-2.

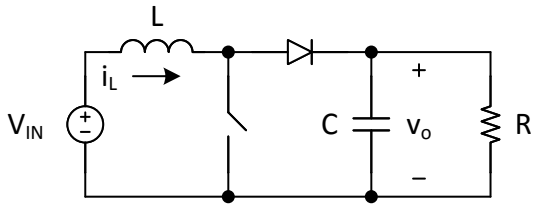

Figure 4-2. Standard Boost Converter State Variables

Figure 4-3 displays the standard boost state variables during the switch-on state.

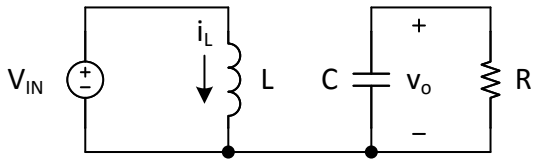

Figure 4-3. Standard Boost Converter Switch-On State Variables

KVL determines the inductor current differential equation (4-1) and KCL provides the output voltage differential equation (4-2).

$$\frac{di_L}{dt} = \frac{1}{L} V_{IN} \qquad (4-1)$$

$$\frac{dv_o}{dt} = -\frac{1}{CR} v_o \qquad (4-2)$$

The switch-on state equation (4-3) summarizes the state variable differential equations in matrix form.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{IN} \qquad (4-3)$$

Figure 4-4 depicts the standard boost state variables in the switch-off state.

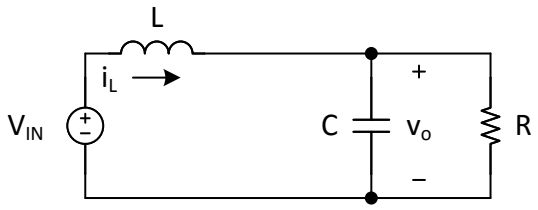

Figure 4-4. Standard Boost Converter Switch-Off State Variables

KVL around the circuit and KCL at the output node determine the inductor current (4-4) and output voltage (4-5) differential equations.

$$\frac{di_L}{dt} = \frac{1}{L} V_{IN} - \frac{1}{L} v_o \qquad (4-4)$$

$$\frac{dv_o}{dt} = \frac{1}{C} i_L - \frac{1}{CR} v_o \qquad (4-5)$$

The switch-off state equation (4-6) summarizes both state-variable differential equations in matrix form.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{IN} \qquad (4-6)$$

Summing the switch-on and switch-off state equations, weighted by duty cycle and inverse duty cycle, provides the average state equation across the switching period (4-7).

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = D \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + (1-D) \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{IN} \qquad (4-7)$$

The DC transfer functions describe the circuit's behavior as the state variables reach pure DC values. Under these conditions both differentials approach zero.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

Solving the resulting inductor current equation (4-8) yields the DC voltage transfer function (4-9).

$$0 = (1-D)\left(-\frac{1}{L}\right) V_{OUT} + \frac{1}{L} V_{IN} \qquad (4-8)$$

$$V_{OUT} = \frac{V_{IN}}{(1-D)} \qquad (4-9)$$

Solving the output voltage equation (4-10) yields the DC current transfer function (4-12).

$$0 = D\left(-\frac{1}{CR}\right) V_{OUT} + (1-D)\left(\frac{1}{C}\right) I_{IN} + (1-D)\left(-\frac{1}{CR}\right) V_{OUT} \qquad (4-10)$$

$$I_{OUT} = \frac{V_{OUT}}{R} \qquad (4-11)$$

$$I_{IN} = \frac{I_{OUT}}{(1-D)} \qquad (4-12)$$

State space averaging produces the same DC transfer functions presented in Section 2.5.3 using steady-state current ripple constraints.

4.1.2 Modified Boost Converter

The modified boost converter's state space model requires two additional state variables. Figure 4-5 shows the two inductor currents, i_{L1} and i_{L2}, and two capacitor voltages, v_{C1} and v_o, describing the modified boost converter's dynamics.

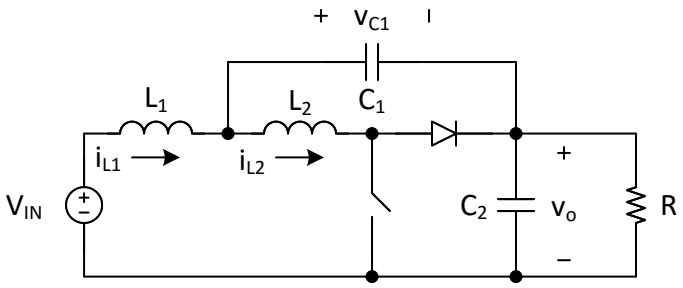

Figure 4-5. Modified Boost Converter State Variables

Figure 4-6 depicts the modified boost state variables during the switch-on state.

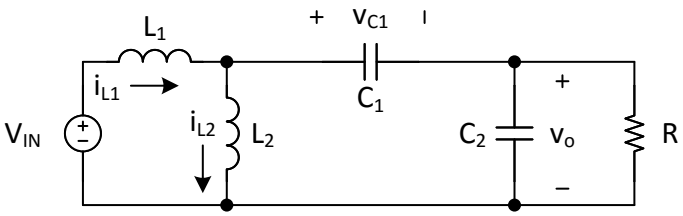

Figure 4-6. Modified Boost Converter Switch-On State Variables

KVL around the outer loop provides the L_1 current differential equation (4-13) and KVL around the inner loop provides the L_2 current differential equation (4-14).

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1}v_{C1} - \frac{1}{L_1}v_o + \frac{1}{L_1}V_{IN} \qquad (4-13)$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2}v_{C1} + \frac{1}{L_2}v_o \qquad (4-14)$$

KCL at the circuit's two nodes provide the capacitor voltage differential equations for v_{C1} (4-15) and v_o (4-16).

$$\frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} - \frac{1}{C_1} i_{L2} \qquad (4-15)$$

$$\frac{dv_o}{dt} = \frac{1}{C_2} i_{L1} - \frac{1}{C_2} i_{L2} - \frac{1}{C_2 R} v_o \qquad (4-16)$$

The modified boost converter's switch-on state equation (4-17) contains the state-variable differential equations in matrix form.

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} \qquad (4-17)$$

Figure 4-7 shows the modified boost converter state variables in the switch-off state.

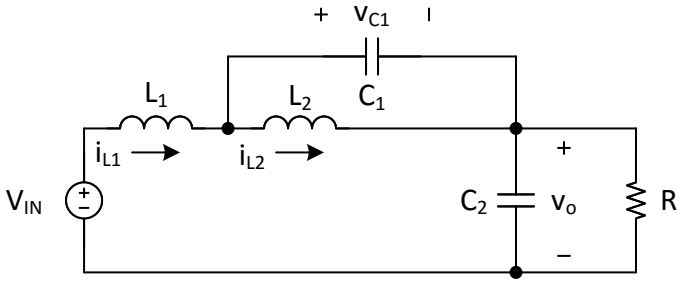

Figure 4-7. Modified Boost Converter Switch-Off State Variables

KVL around the circuit's outer loop determines the L_1 current differential equation (4-18). KVL in the C_1 loop determines the L_2 current differential equation (4-19).

$$\frac{di_{L1}}{dt} = -\frac{1}{L_1} v_{C1} - \frac{1}{L_1} v_o + \frac{1}{L_1} V_{IN} \qquad (4-18)$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2} v_{C1} \qquad (4-19)$$

KCL at the circuit's nodes determines the C_1 voltage differential equation (4-20) and C_2 voltage differential equation (4-21).

$$\frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} - \frac{1}{C_1} i_{L2} \qquad (4-20)$$

$$\frac{dv_o}{dt} = \frac{1}{C_2} i_{L1} - \frac{1}{C_2 R} v_o \qquad (4-21)$$

The modified boost converter's switch-off state equation (4-22) contains the four state-variable differential equations in matrix form.

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{C_2 R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} \qquad (4-22)$$

Summing the modified boost converter's state equations, weighted by their switching period fraction, produces the average state equation (4-23).

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = D \cdot A_{switch-on} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_o \end{bmatrix} + (1-D) \cdot A_{switch-off} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} \quad (4-23)$$

$$A_{switch-on} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & -\frac{1}{C_2} & 0 & -\frac{1}{C_2 R} \end{bmatrix}$$

$$A_{switch-off} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & -\frac{1}{C_2 R} \end{bmatrix}$$

The differentials approach zero as the state variables reach their DC value.

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Solving the averaged L_1 current equation (4-24) and the averaged L_2 current equation (4-25) determine the relationships between the circuit's average voltages (4-25 and 4-27).

$$-\frac{D}{L_1}(V_{C1} + V_{OUT}) - \frac{(1-D)}{L_1}(V_{C1} + V_{OUT}) + \frac{1}{L_1}V_{IN} = 0 \qquad (4-24)$$

$$V_{IN} = V_{C1} + V_{OUT} \qquad (4-25)$$

$$\frac{D}{L_2}(V_{C1} + V_{OUT}) + \frac{(1-D)}{L_2}V_{C1} = 0 \qquad (4-26)$$

$$V_{C1} = -DV_{OUT} \qquad (4-27)$$

Consolidating both relationships produces the modified boost converter's DC transfer function (4-28).

$$V_{OUT} = \frac{V_{IN}}{(1-D)} \qquad (4-28)$$

Solving the average C1 voltage equation (4-29) demonstrates the equality between the average inductor currents (4-30).

$$\frac{D}{C_1}(I_{IN} - I_{L2}) + \frac{(1-D)}{C_1}(I_{IN} - I_{L2}) = 0 \qquad (4-29)$$

$$I_{IN} = I_{L2} \qquad (4-30)$$

Considering the equality of the average inductor currents while solving the average C_2 voltage equation (4-31) yields the DC current transfer function (4-32).

$$\frac{D}{C_2}\left(I_{IN} - I_{L2} - \frac{V_{OUT}}{R}\right) + \frac{(1-D)}{C_2}\left(I_{IN} - \frac{V_{OUT}}{R}\right) = 0 \qquad (4-31)$$

$$I_{IN} = \frac{I_{OUT}}{(1-D)} \qquad (4-32)$$

The modified boost converter's DC transfer functions match the standard boost topology, demonstrating functional equality. On average, both converters share the same relationships between switch duty cycle and input and output quantities.

4.2 Steady-State m-Domain State Equations

During steady-state operation, a DC/DC converter returns to the same state at the beginning of each switching cycle. The switch-on and switch-off state equations each govern a portion of the cycle. Modeling the switching transition creates a unified, periodic state equation. An *m*-domain state equation describes the converter's behavior over a generalized switching cycle.

Independent variable transformation (4-33) partitions the time domain into a set of discrete switching cycles in the *m*-domain [33].

$$t = (n + m)T \qquad (4-33)$$

$$n = 0, 1, 2, 3, \ldots$$

$$0 \leq m < 1$$

Applying the transformation reduces a periodic, time-domain differential equation (4-34) into an *m*-domain differential equation (4-35) describing the n^{th} time-domain cycle.

$$\frac{dx(t)}{dt} = x(t) \qquad (4-34)$$

$$\frac{dx_n(m)}{dm} = x_n(m) \cdot T \qquad (4-35)$$

The transformation also simplifies the converter's switching transition model. Transitions in the time domain occur relative to the switching period and duty cycle. However, *m*-domain switching transitions depend only on duty cycle, allowing a simple piecewise function to model the transition. Figure 4-8 illustrates this difference.

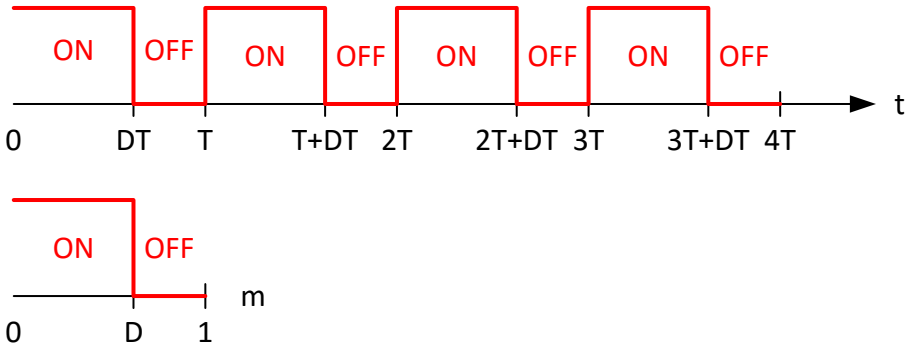

Figure 4-8. Time-domain and *m*-domain Switching Transitions

4.2.1 Standard Boost Converter

The standard boost converter's switch-off state equation (4-6) contains two terms not present in the switch-on state equation (4-3). Applying the standard boost switching function (4-36) to the switch-off equation models the transition in the *m*-domain.

$$f_b(m) = \begin{cases} 0, for\ 0 \le m < D \\ 1, for\ D \le m < 1 \end{cases} \qquad (4-36)$$

The standard boost *m*-domain state equation (4-37) describes the converter's behavior during a generalized, steady-state switching cycle.

$$\begin{bmatrix} \frac{di_{L,n}}{dm} \\ \frac{dv_{o,n}}{dm} \end{bmatrix} = \begin{bmatrix} 0 & -f_b(m)\frac{T}{L} \\ f_b(m)\frac{T}{C} & -\frac{T}{CR} \end{bmatrix} \begin{bmatrix} i_{L,n} \\ v_{o,n} \end{bmatrix} + \begin{bmatrix} \frac{T}{L} \\ 0 \end{bmatrix} V_{IN} \qquad (4-37)$$

4.2.2 Modified Boost Converter

The modified boost switch-on state equation (4-17) contains two terms not present in the switch-off state equation (4-18). Applying the modified boost switching function (4-38) to the switch-on equation models the transition in the *m*-domain.

$$f_{mb}(m) = \begin{cases} 1, for\ 0 \le m < D \\ 0, for\ D \le m < 1 \end{cases} \qquad (3-38)$$

The modified boost *m*-domain state equation (4-39) describes the converter's behavior during a generalized, steady-state switching cycle.

$$\begin{bmatrix} \frac{di_{L1,n}}{dm} \\ \frac{di_{L2,n}}{dm} \\ \frac{dv_{C1,n}}{dm} \\ \frac{dv_{o,n}}{dm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{T}{L_1} & -\frac{T}{L_1} \\ 0 & 0 & \frac{T}{L_2} & f_{mb}(m)\frac{T}{L_2} \\ \frac{T}{C_1} & -\frac{T}{C_1} & 0 & 0 \\ \frac{T}{C_2} & -f_{mb}(m)\frac{T}{C_2} & 0 & -\frac{T}{C_2 R} \end{bmatrix} \begin{bmatrix} i_{L1,n} \\ i_{L2,n} \\ v_{C1,n} \\ v_{o,n} \end{bmatrix} + \begin{bmatrix} \frac{T}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{IN} \qquad (4-39)$$

4.3 Numerical m-Domain State Equation Solutions

Matlab's *ode45* function provides numerical state equation solutions. Solving the system of first-order differential equations requires initial conditions (ICs). State variable average values, obtained through circuit analysis, provide initial condition estimates. Under steady-state conditions, each state variable's final value during the switch-off state equals its initial value during the switch-on state. Iteration gradually reduces the solutions' steady-state error; the difference between final switch-off value and initial switch-on value.

4.3.1 Initial Condition Estimates

A converter's state variable averages depend on the average voltages and currents associated with its reactive components. During steady-state operation, the average voltage across an inductor and the average current through a capacitor both approach zero. Under these conditions, the average inductor currents and capacitor voltages relate to the converter's known input and output parameters.

Table 4-1 summarizes the average voltage and current associated with the standard boost converter's inductor and capacitor.

Table 4-1. Standard Boost Converter Component Averages

Component	Voltage	Current
L	0 V	I_{IN}
C	V_{OUT}	0 A

Table 4-2 summarizes the average voltage and current associated with the modified boost converter's reactive components.

Table 4-2. Modified Boost Converter Component Averages

Component	Voltage	Current
L_1	0 V	I_{IN}
L_2	0 V	I_{IN}
C_1	V_{IN} - V_{OUT}	0 A
C_2	V_{OUT}	0 A

Table 4-3 lists the estimated initial condition for each state variable in the standard and modified boost converters, based on functional requirements and the associated DC transfer functions.

Table 4-3. State Equation Initial Condition Estimates

Standard Boost Converter		Modified Boost Converter	
State Variable	Estimate	State Variable	Estimate
i_L	5 A	i_{L1}	5 A
		i_{L2}	5 A
v_o	20 V	v_{C1}	-14 V
		v_o	20 V

These functional converter design parameters provide reasonable initial condition estimates that allow the iterative state equation solution to converge.

4.3.2 Iterative State Equation Solution

Custom Matlab functions implement the iterative state equation solution process for both the standard and modified boost converters. Each function requires converter design information, including component values, switching period, input voltage, output voltage, and output power. Component values and switching period populate the state equation matrices, while input-output parameters provide the initial condition estimates for each state variable. The scripts decouple the state equation into switch-on and switch-off equations, facilitating Matlab's *ode45* function, and return the concatenated solution over the *m*-domain after iteration converges.

Figure 4-9 depicts the iteration process, controlled by the steady-state error. Once the final state variable values of the switch-off solution match the initial values of the switch-on solution, within 0.0001%, the function stops iterating.

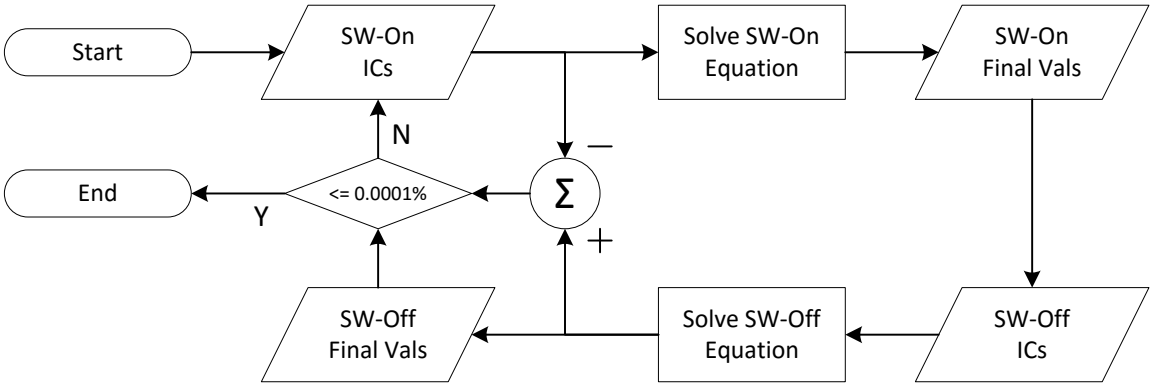

Figure 4-9. Iterative Numerical State Equation Solution

APPENDICES

MA contains the Matlab files *boost_cycle.m* and *boost_mod_cycle.m*, which implement the iterative state equation solution functions for the standard and modified boost converters.

4.4 Modified Boost Design Process

The baseline design restricts modified boost converter design choices. These parameters, detailed in Chapter 3, set switching frequency and output capacitance (C_2) directly and constrain the modified topology's total inductance. Dividing the specified total inductance between L_1 and L_2, and sizing the additional capacitor C_1 remain the only topology design choices.

Design constraints limit the converter's total inductance at 10µH, the sum of L_1 and L_2. This design process considers three allocations of 10µH between L_1 and L_2: a 50/50 split, a 25/75 split, and a 75/25 split. Converter resonant frequencies and physical

size limit the C_1 value range. The converter's resonant behavior determines the minimum C_1 value keeping the highest resonant frequency below the 200-kHz switching frequency. Setting the maximum C_1 value at 50 µF, the specified converter output capacitance, limits the modified boost converter's additional physical size. Matlab informs final component value selection, based on input current ripple performance predicted by the numerical state space equation solutions.

4.4.1 Resonant Frequencies

The modified boost converter topology complicates resonant frequency analysis. The standard topology contains one resonance during the switch-off state. Inspection suggests multiple resonances in the modified boost converter during the switch-of state. Figure 4-10 illustrates an AC simulation of the modified boost converter's switch-on and switch-off circuits used to observe the converter's resonant frequencies.

Each circuit's input impedance characteristics indicate resonant behavior. Figure 4-11 portrays the switch-on circuit's two resonant frequencies and the switch-off circuit's three resonant frequencies with C_1 equal to 1 µF. The impedance curves align at higher frequencies, suggesting the circuits share two similar resonances. However, these resonant frequencies do not match exactly; they separate as C_1 value increases.

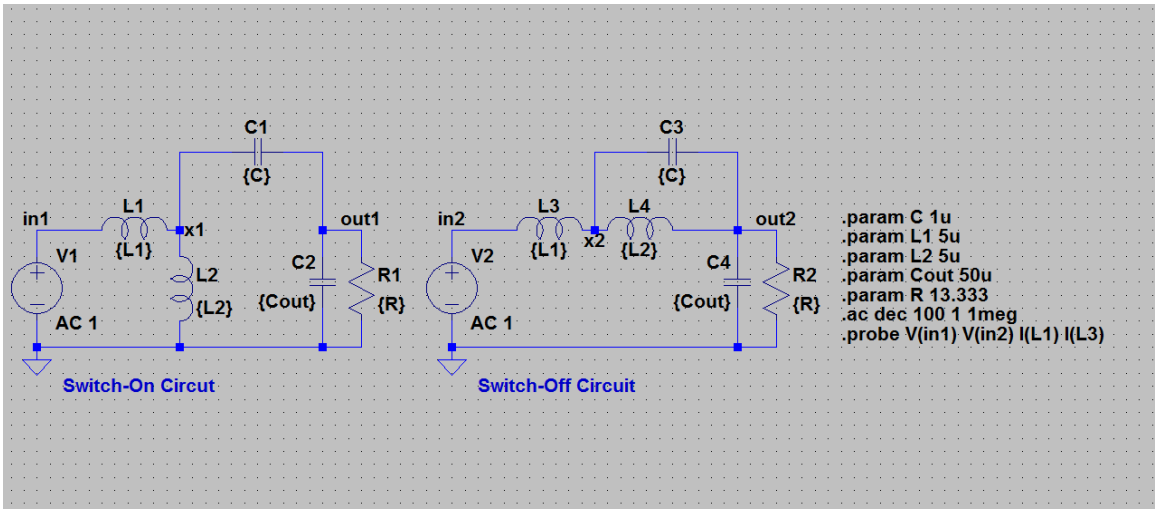

Figure 4-10. LTSpice Modified Boost Converter Resonance Simulation

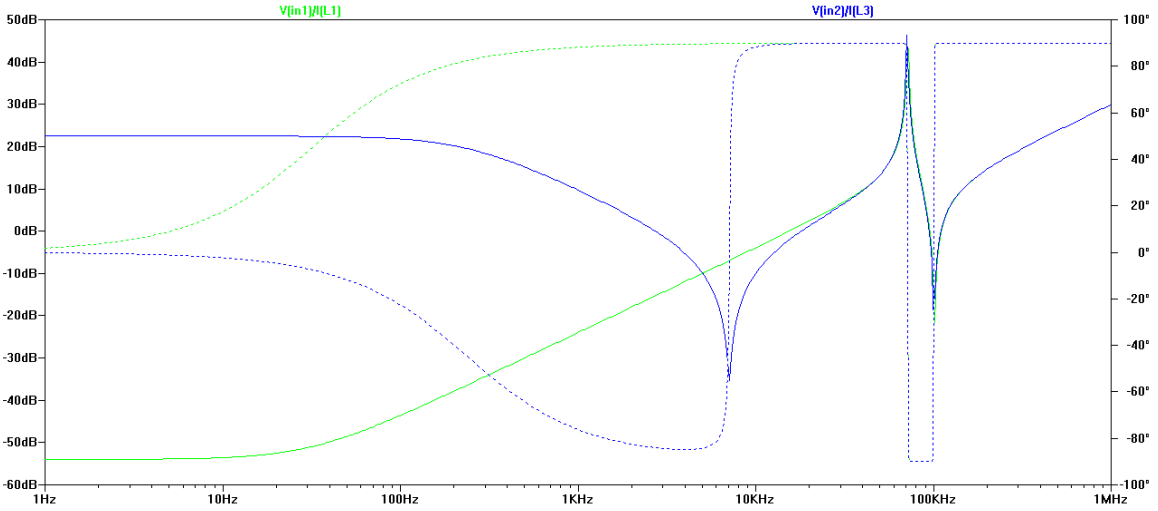

Figure 4-11. LTSpice Modified Boost Converter Simulated Input Impedance

Figure 4-12 plots the converter's highest resonant frequency, obtained from the Figure 4-10 simulation, over a range of C_1 values. These data suggest C_1 values greater than 1uF prevent the converter's maximum resonant frequency from exceeding the 200-kHz switching frequency. The data also indicate that the inductance split between L_1 and L_2 impacts resonant frequency less as C_1 value approaches output capacitance value.

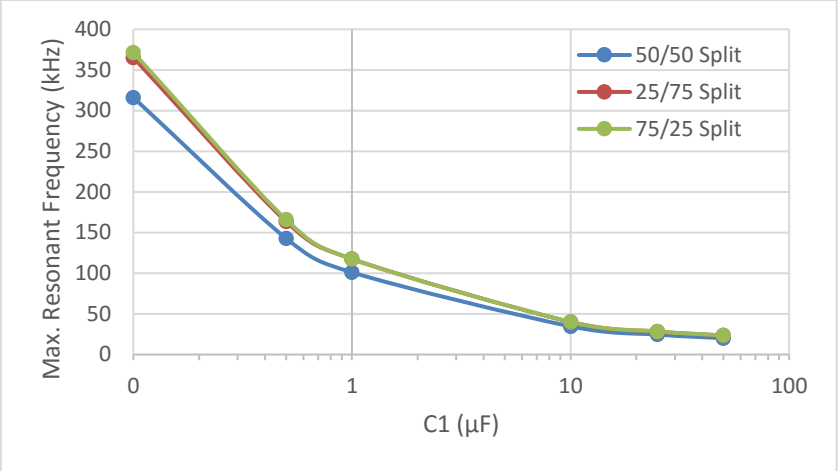

Figure 4-12. Max. Modified Boost Resonant Frequency versus C_1 Value

4.4.2 Component Sizing

The L_1 current state variable predicts the converter's input current ripple performance. Matlab provides the numerical state equation solution, calculating ripple performance using the maximum, minimum, and average L_1 current values. Appendix A contains the script *boost_mod_design_comp.m*, executing these calculations for all three L_1/L_2 inductance splits over the selected C_1 value range. Figure 4-13 charts the converter's performance based on component sizing.

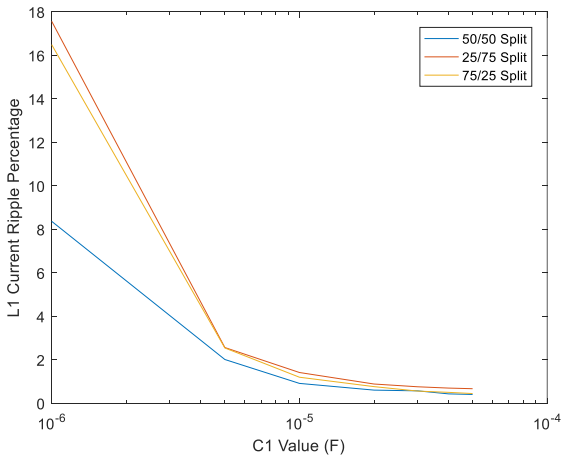

Figure 4-13. Modified Boost Converter Component Sizing Chart

These performance predictions agree with a simplistic explanation of the input current ripple. A larger C_1 value reduces the voltage ripple across L_1, and smaller v_{L1} changes induce smaller i_{L1} changes. The L_1/L_2 inductance split's impact on current ripple performance and maximum resonant frequency decrease as C_1 value approaches output capacitance value. Selecting a 50/50 inductance split simplifies component selection. Table 4-4 lists the modified boost converter design parameters chosen based on predicted input current ripple performance.

Table 4-4. Modified Boost Converter Component Values

Component	Selected Nominal Value
L_1	5 µH
L_2	5 µH
C_1	30 µF
C_2	50 µF

4.5 Design Simulation

The numerical state equation solution method provides limited design simulation by directly solving for each state variable over a single, steady-state switching cycle. These waveforms provide all necessary information, either directly or indirectly, to physically implement the converter. Given specific converter design parameters, a Matlab-simulation script performs iterative state equation solution, plots the state variable waveforms, and calculates relevant state variable measurements indicating converter performance. Comparing each converter's Matlab-simulation against theoretical DC performance and a complementary LTSpice simulation, evaluates the *m*-domain state equation model's efficacy. Table 4-5 summarizes the simulated converter designs, including functional parameters and component values. Section 4.5.3 compares both simulation technique's relevant converter performance measurements.

Table 4-5. Converter Design Parameter Summary

Standard Boost Design		**Modified Boost Design**	
V_{IN}	6 V	V_{IN}	6 V
V_{OUT}	20 V	V_{OUT}	20 V
P_{OUT}	30 W	P_{OUT}	30 W
f_{SW}	200 kHz	f_{SW}	200 kHz
R	13.333 Ω	R	13.333 Ω
L	10 µH	L_1	5 µH
		L_2	5 µH
C	50 µF	C_1	30 µF
		C_2	50 µF

4.5.1 Matlab Simulation

The *boost_sim.m* script in Appendix A simulates the standard boost design's performance. Figure 4-14 portrays the Matlab-simulated inductor current and capacitor voltage in the standard boost converter design. The simulated waveforms take the expected shape Section 2.5.5 presents.

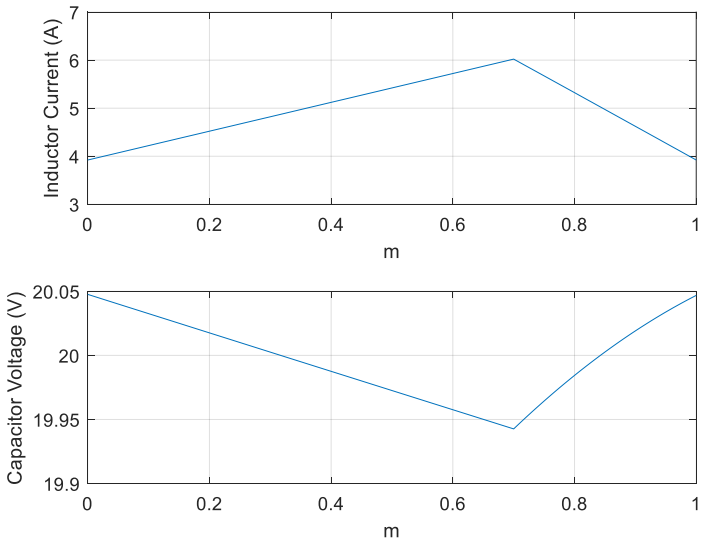

Figure 4-14. Matlab State Variable Waveforms for Standard Boost

Table 4-6 compares relevant Matlab simulation measurements and theoretical standard boost converter design values. The simulated average state variable values match theoretical values within one percent, while the peak-to-peak and percent ripple values match to five percent error. Appendix B contains complete standard boost measurements obtained through Matlab-simulation.

Table 4-6. Matlab and Theoretical Standard Boost Design Performance

	Inductor Current (A)			**Capacitor Voltage (V)**		
	Matlab	Theory	%Diff	Matlab	Theory	%Diff
Average	4.9591	5	-0.818%	19.998	20	-0.01%
Peak-Peak	2.1	2	5%	0.105	0.1	5%
%Ripple	42.346%	40%	5.865%	0.5249%	0.5%	4.98%

The *boost_mod_sim.m* script in Appendix A simulates the modified boost design's performance. Figure 4-15 presents the simulated inductor current waveforms, demonstrating agreement between the state equation model and the simplistic circuit analysis. The voltage across L1 approaches zero, and the small voltage ripple produced by current through C1 induces small current ripple through L1. The voltage across L2 approaches the standard boost converter's inductor voltage, but at half the total inductance of the standard boost design, L2 experiences twice the current ripple. These waveforms indicate the modified design's ability to contain switching noise, presenting only a small current ripple at the converter input.

Figure 4-16 depicts both capacitor voltage waveforms, demonstrating voltage ripple performance comparable to the standard boost design. The iterative state equation solution method favors minimizing L_1 current's steady-state error, the difference between initial and final values, based on the state design goal. Both capacitor voltage waveforms suffer larger steady-state error due to the chosen hierarchy.

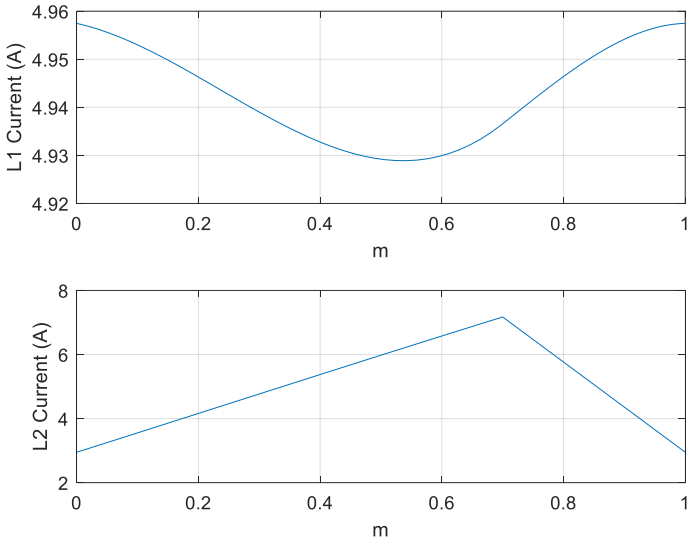

Figure 4-15. Matlab Modified Boost Inductor Current Waveforms

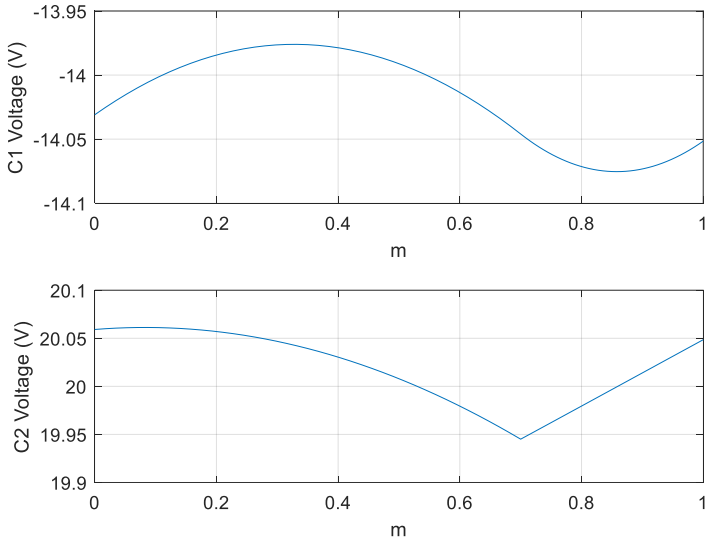

Figure 4-16. Matlab Modified Boost Capacitor Voltage Waveforms

The simulation script determines capacitor current waveforms calculated from inductor current solutions and the known DC output current, using KCL relationships during each switching state. Figure 4-17 shows simulated capacitor current waveforms which help determine capacitor current ratings. Under ideal steady-state conditions, average capacitor current approaches zero. These waveforms exhibit non-zero averages

and indicate the Matlab-simulation's functional limitations; small state variable solution error compounds through further calculation required to determine related waveforms.

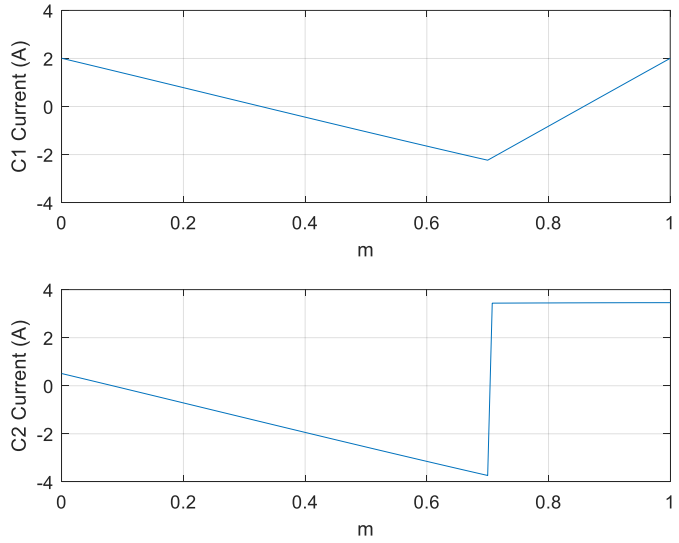

Figure 4-17. Matlab Modified Boost Capacitor Current Waveforms

Table 4-7 compares simulated average state variable values and theoretical state variable averages derived from DC circuit analysis and functional converter parameters. Despite favoring minimal inductor current steady-state error, the Matlab simulation predicts average state variable values within approximately one percent of theory. Appendix B contains complete Matlab simulation performance measurements.

Table 4-7. Matlab and Theoretical Modified Boost Design DC Performance

	L_1 Current (A)	**L_2 Current (A)**	**C_1 Voltage (V)**	**C_2 Voltage (V)**
Matlab	4.9446	5.0384	-14.032	20.012
Theory	5	5	-14	20
%Diff	-1.108%	0.768%	0.2286%	0.6%

4.5.2 LTSpice Simulation

LTSpice transient simulations provide complete benchmark comparison against the Matlab-based simulations. Both converter spice simulations use non-ideal switches and open-loop PWM control. The measure command captures the relevant converter performance data over the simulation's final 50 ms, ten switching cycles; average and peak-to-peak measurements determine Spice-simulated ripple percentage. Appendix B contains complete LTSpice performance measurements for both standard and modified boost designs.

Figure 4-18 depicts the LTSpice transient simulation of the standard boost converter design. Figure 4-19 shows the standard boost state variable waveforms over the transient simulation's final ten switching cycles. These waveforms indicate approximate ripple performance similar to the Matlab simulation.

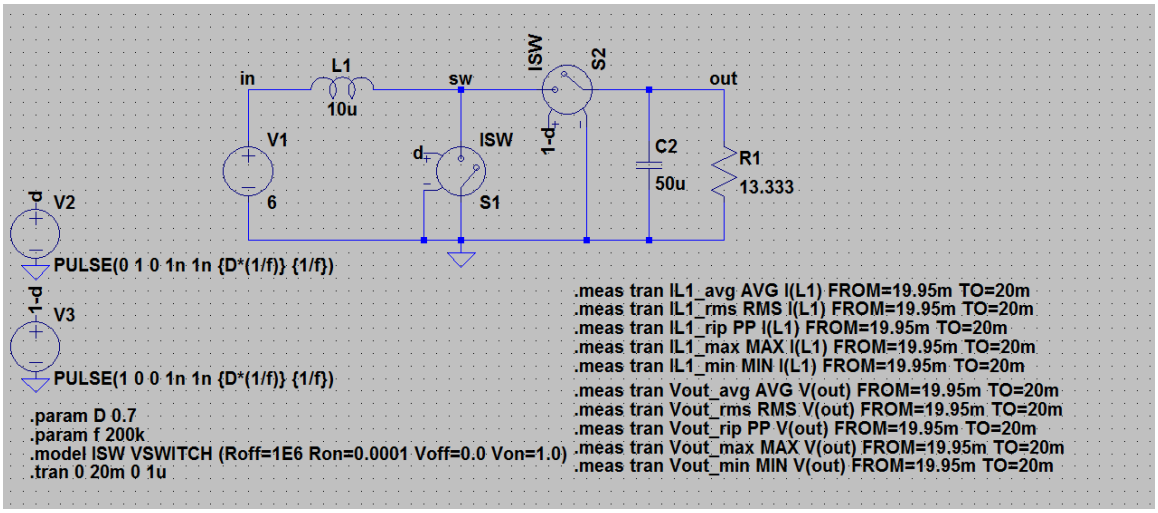

Figure 4-18. LTSpice Standard Boost Transient Simulation

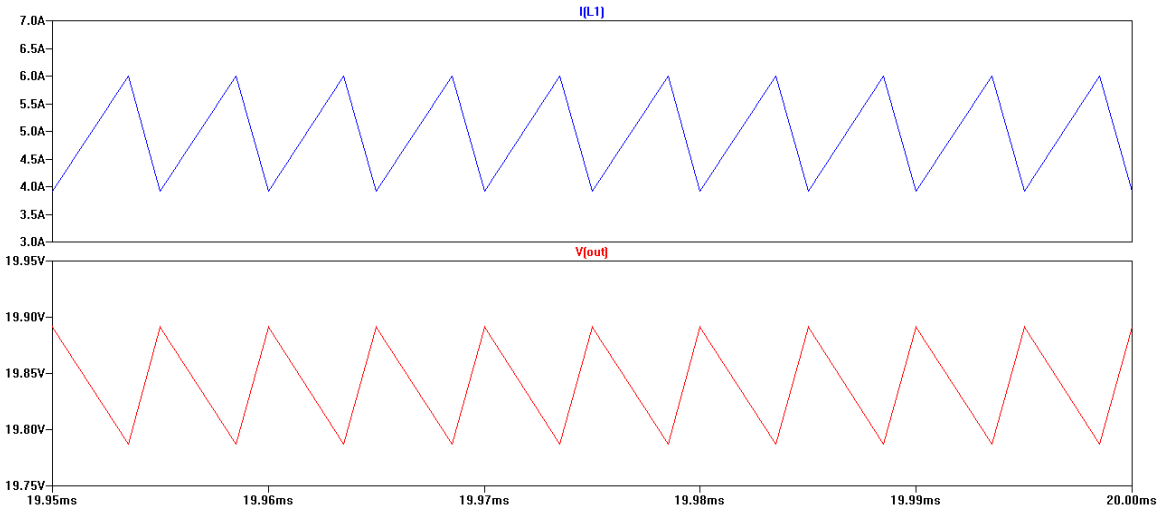

Figure 4-19. LTSpice State Variable Waveforms for Standard Boost

Figure 4-20 shows the LTSpice transient simulation for the modified boost converter design. Figure 4-21 presents the LTSpice modified boost inductor current waveforms, again demonstrating the design's small input current ripple. LTSpice also predicts L_2 current ripple twice the standard boost design's value.

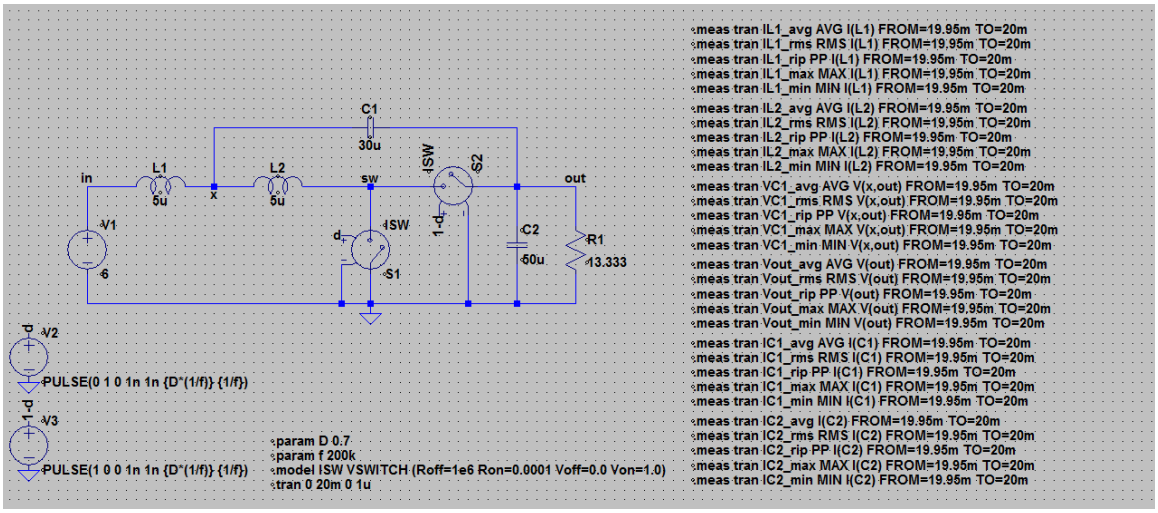

Figure 4-20. LTSpice Modified Boost Transient Simulation

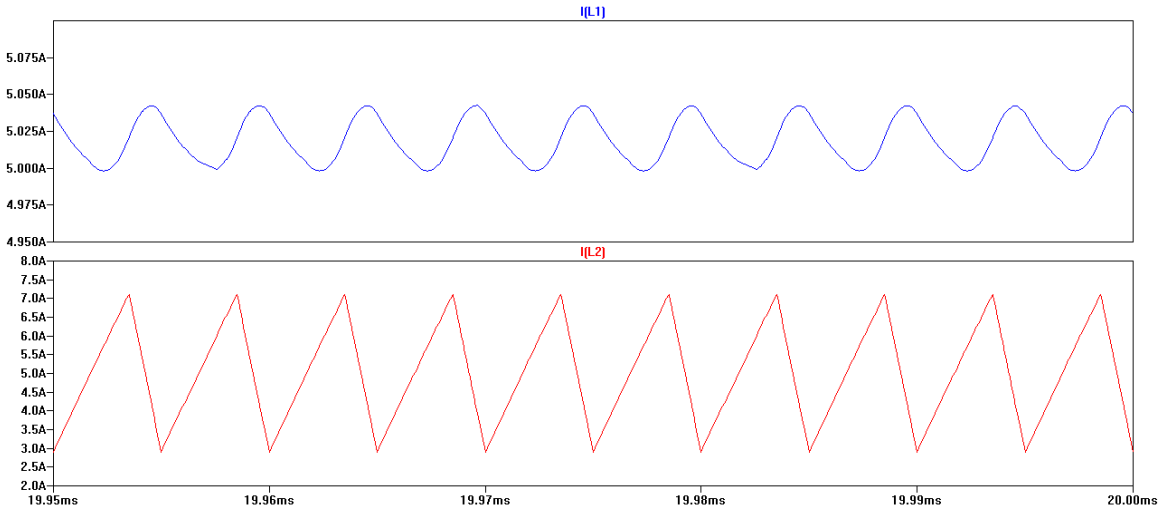

Figure 4-21. LTSpice Modified Boost Inductor Current Waveforms

Figure 4-22 depicts the modified boost capacitor waveforms, demonstrating output capacitor voltage ripple equivalent to the standard boost design. The LTSpice simulation measures C_1 voltage between nodes *x* and *out* shown in Figure 4-20.

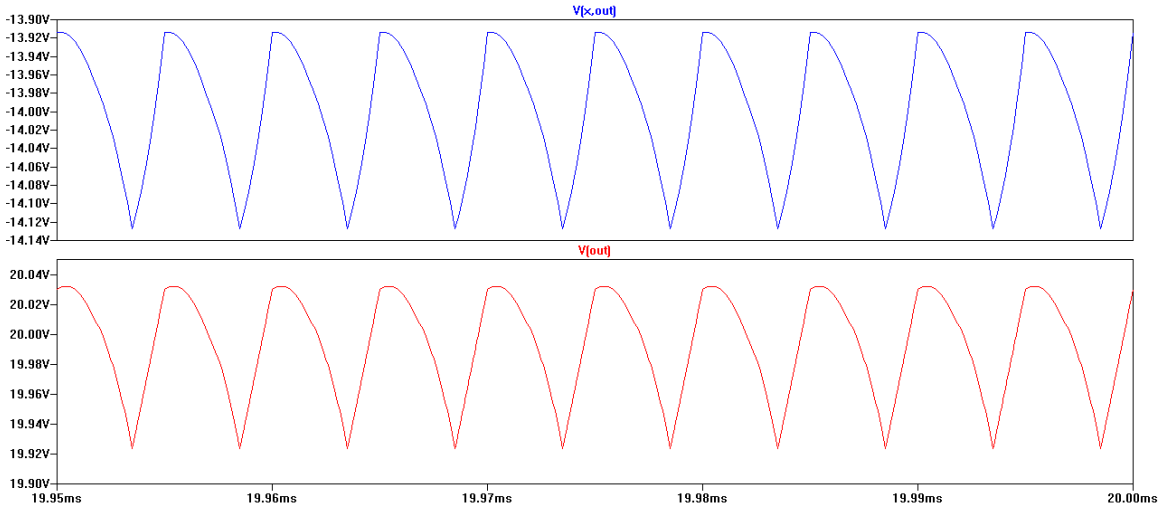

Figure 4-22. LTSpice Modified Boost Capacitor Voltage Waveforms

Figure 4-23 shows the LTSpice modified boost design's large capacitor current ripple, like the Matlab modified boost simulation.

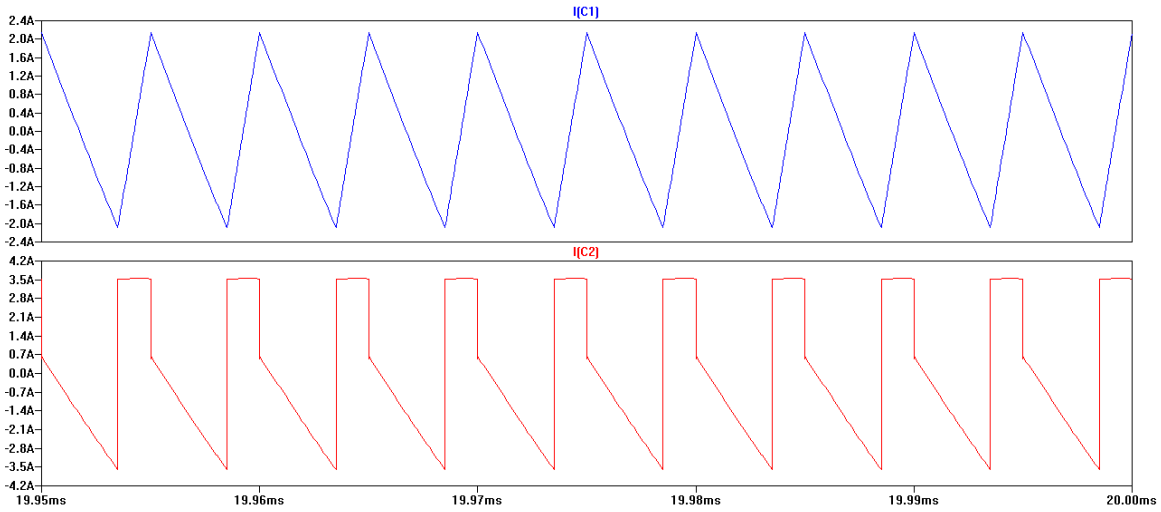

Figure 4-23. LTSpice Modified Boost Capacitor Current Waveforms

4.5.3 Simulation Comparison

Selected relevant measurements form a comparative basis between simulation methods. Average state variable measurements verify each design's DC behavior. Peak-to-peak and percent ripple state variable measurements, relative to measured averages, quantify each design's ripple performance. The modified boost design RMS capacitor current measurements pertain to component current rating requirements. LTSpice measurements serve as nominal values when calculating percent differences.

Table 4-8 compares the simulated standard boost design's DC and ripple performance measurements. Both simulations match within 1%, across all three measurements.

Table 4-8. Standard Boost Simulation Measurement Comparison

	Inductor Current (A)			**Capacitor Voltage (V)**		
	Matlab	LTSpice	%Diff	Matlab	LTSpice	%Diff
Average	4.9591	4.9627	-0.07%	19.998	19.839	0.80%
Peak-Peak	2.1	2.0827	0.83%	0.105	0.1042	0.77%
%Ripple	42.346%	41.967%	0.90%	0.525%	0.525%	-0.06%

Table 4-9 compares the modified boost design state variable and capacitor current measurements. Average L_1 current matches within three halves of a percent, and the other state variable average measurements match within half of a percent. LTSpice predicts significantly larger L_1 current ripple and C_1 voltage ripple; given the small absolute peak-to-peak values, the difference between simulations carries less importance. Simulated C_1 RMS currents match within two percent, and C_2 RMS currents match within 12% despite the Matlab simulation measuring non-zero average capacitor current, an imperfect steady-state condition.

Table 4-9. Modified Boost Simulation Measurement Comparison

	L_1 Current (A)			**L_2 Current (A)**		
	Matlab	LTSpice	%Diff	Matlab	LTSpice	%Diff
Average	4.9446	5.0188	-1.48%	5.0384	5.0183	0.40%
Peak-Peak	0.0286	0.0444	-35.59%	4.2209	4.2098	0.26%
%Ripple	0.578%	0.885%	-34.69%	83.77%	83.889%	-0.14%
	C_1 Voltage (V)			**C_2 Voltage (V)**		
	Matlab	LTSpice	%Diff	Matlab	LTSpice	%Diff
Average	-14.032	-13.999	0.24%	20.012	19.993	0.10%
Peak-Peak	0.0993	0.2134	-53.47%	0.1162	0.1084	7.20%
%Ripple	0.708%	1.524%	-53.57%	0.581%	0.542%	7.10%
	C_1 Current (A)			**C_2 Current (A)**		
	Matlab	LTSpice	%Diff	Matlab	LTSpice	%Diff
RMS	1.2429	1.2242	1.53%	2.8323	2.5308	11.91%

Both simulation's produce similarly shaped converter waveforms, except standard boost output voltage and modified boost C_1 voltage. Theoretically, the standard boost output voltage follows a roughly quadratic trajectory during the switch-off state, as Figure 2-16 shows charge accumulating at a decreasing rate due to negative current slope. This analysis assumes output voltage ripple exerts a negligible effect on load current. The LTSpice simulation produces non-ideal load current, consequently affecting the output

voltage waveform. Additionally, solution uniqueness affects the state equation simulation model. The iterative, numerical solution method simply finds a set of solutions exhibiting steady-state error, difference between initial and final values over a switching cycle, below a predefined threshold. The iterative method does not guarantee a unique solution. However, Sections 4.5.1 and 0 demonstrate general waveform similarity, for both converter designs, across simulation methods.

Though Matlab and LTSpice simulation results differ in some respects, both methods predict significant input current ripple reduction between standard boost and modified boost designs. Table 4-10 summarizes input current ripple performance across both topology's equivalent design, projecting reduction from a 40% baseline to below 1% ripple.

Table 4-10. Simulated Boost Converter Input Current Ripple Reduction

	Standard Boost		**Modified Boost**	
	Peak-Peak (A)	%Ripple	Peak-Peak (A)	%Ripple
Matlab	2.1	42.346%	0.0286	0.578%
LTSpice	2.0827	41.967%	0.0444	0.885%

5. HARDWARE

The converters' hardware implementation covers power component selection, switching controller design, and printed circuit board (PCB) assembly. Hardware testing determines each converter's performance based upon state variable measurements. Implementation priorities include minimizing non-topological differences and characterizing steady-state, CCM operation.

5.1 Power Components

Each converter's power component ratings must exceed expected voltage and current conditions based on theory or simulation. Most components experience similar voltage and current stresses in both topologies. The modified boost topology primarily impacts L_2, C_1, and output capacitor (C_2) current ratings.

5.1.1 Inductors

Both converter implementations use Wuerth Elektronik's WE-FAMI series through-hole, shielded power inductors [34]. The modified boost converter contains two 4.7 µH inductors chosen to occupy less PCB area than the standard boost converter's single 10 µH inductor. Table 5-1 summarizes important properties for each inductor selected.

Table 5-1. WE-FAMI Series Inductor Properties

Use	Inductance	I_{DC}	I_{sat}	Max DCR	Tol.	Footprint
Modified Boost	4.7 µH	6.5 A	9.6 A	12.5 mΩ	20%	60.82 mm^2
Standard Boost	10 µH	8.9 A	12.4 A	9.5 mΩ	20%	172 mm^2

Both inductors meet the design's current requirements. The DC current rating exceeds the 5 A average current though each inductor in the standard boost and modified

boost. The modified boost's L_2 maximum current of approximately 7 A, remains below the inductor saturation rating.

5.1.2 Capacitors

Both converter implementations use multilayer ceramic capacitors (MLCCs) in the power path. Using MLCCs mitigates the capacitor equivalent series resistance's (ESR) effects ranging from increased output voltage ripple to parasitic control-loop zeros. This choice keeps power-path capacitors closer to the ideal components assumed during analysis and simulation. Configuring multiple MLCCs in parallel accommodates large ripple current. MLCCs, current-limited only by heat dissipation, offer a smaller, cheaper solution than electrolytic capacitors. Table 5-2 describes the worst-case current through each power-path capacitor, based on Matlab simulation, and the corresponding MLCC configuration.

Table 5-2. Power-Path Capacitor Current and MLCC Configuration

Component	Worst-Case Current		Value	Configuration
Input Capacitor	Standard Boost	0.614 A_{RMS}	44 µF	22 µF x 2
Modified Boost C_1	Modified Boost	2.8323 A_{RMS}	28.2 µF	4.7 µF x 6
Output Capacitor	Modified Boost	1.2429 A_{RMS}	47 µF	4.7 µF x 10

Table 5-3 lists properties of both MLCCs implementing power-path capacitors.

Table 5-3. Power-Path MLCC Properties

Component	Capacitance	V_{DC} Rating	Dielectric	Tol.	SMD Package
Input Capacitor	22 µF	10 V	X7R	20%	1210
Modified Boost C_1	4.7 µF	25 V	X7R	10%	1206
Output Capacitor					

5.1.3 Switch and Diode

The switching components experience similar stresses in both converter designs. Both topologies expose no more than the output voltage across both switching devices. Additionally, both devices carry the same average currents in each converter. Each converter implementation uses a IRF60B217 n-channel MOSFET switch and a MBR10100G Schottky diode [35] [36]. Table 5-4 summarizes each component's ratings and expected operating conditions. Voltage rating margins accommodate parasitic ringing at a converter's switching node. Current rating margins ensure power dissipation within component packaging capabilities.

Table 5-4. Switching Component Rating Margins

IRF60B217 MOSFET		**MBR10100G Diode**	
Peak Drain-Source Voltage (V_{DS})		Peak Repetitive Reverse Voltage (V_{rrm})	
Rating	60 V	Rating	100 V
Expected	20 V	Expected	20 V
Margin	40 V	Margin	80 V
Continuous Drain Current (I_D)		Average Forward Current (I_F)	
Rating	60 A	Rating	10 A
Expected	3.5	Expected	1.5 A
Margin	56.5 A	Margin	8.5 A

5.2 Switching Controller

Both converters use an identical control circuit built around the LM3478 low-side, current-mode switching controller [37]. Large inductor current in both designs disqualify most internal switch devices and relatively low switching frequency further limits controller selection. The LM3478 balances control features and external component requirements; providing variable switching frequency but fixed soft-start, under-voltage

lockout, over-voltage protection, and short-circuit protection. Table 5-5 describes each LM3478 pin's function.

Table 5-5. LM3487 Pin Descriptions [37]

Pin Name	Pin No.	Description
I_{SEN}	1	Current sense input. Connect to low-side sense resistor.
COMP	2	Control loop compensation. Connect RC-network.
FB	3	Output feedback. Set to 1.26 V with output voltage divider.
AGND	4	Analog ground.
PGND	5	Power ground.
DR	6	Gate drive. Connect to external MOSFET gate terminal.
FA/SD	7	Frequency adjust and shutdown. Grounded resistor sets switching frequency. Pull high for 30 µs to shut down.
V_{IN}	8	Power input. Connect 2.97 V to 40 V supply.

External components configure the essential control functions in the LM3478, including switching frequency, current limit, output voltage, and loop compensation.

5.2.1 Switching Frequency

A resistor connected between the FA/SD pin and ground sets the internal oscillator frequency. The LM3478 datasheet provides the frequency adjust resistor equation (5-1) [37].

$$R_{FA} = 4.503 \cdot 10^{11} \cdot f^{-1.26} \qquad (5-1)$$

$$R_{FA} = 4.503 \cdot 10^{11} \cdot (200\ kHz)^{-1.26} \approx 94.2\ k\Omega$$

The standard values 93.1 kΩ and 1.13 kΩ connected serially implement resistance corresponding to a 200 kHz switching frequency.

5.2.2 Sense Resistor

The controller's current feedback loop determines inductor current indirectly. A low-side current sense resistor provides a voltage proportional to the inductor current

while the switch conducts. This voltage applied to the I_{SEN} pin determines when the controller turns the switch off.

A sense resistor sets the inductor current limit enforced by the controller's current feedback loop. Figure 5-1 depicts the LM3478 low-side sense resistor configuration. The I_{SEN} pin receives a voltage proportional to the inductor current while the switch conductions. PWM logic resets the DR pin when I_{SEN} voltage exceeds an internally-generated control signal, turning off the converter's switch [37].

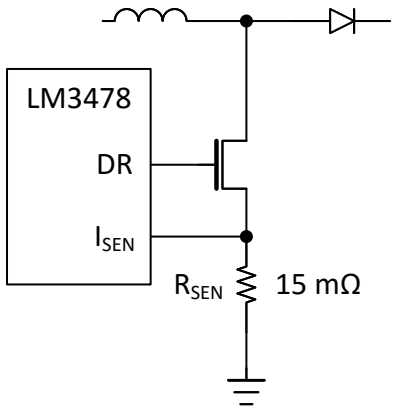

Figure 5-1. LM3478 Current Sense Resistor

Sizing the sense resistor determines the peak current value required to trip the controller's internal limit. The datasheet suggests a 20% margin above peak switch current (5-2) [37]. The standard boost design requires a 7.2A current limit; simulation results suggest this also covers the modified boost design.

$$I_{SW(limit)} = 1.2 \cdot \left(I_{IN} + \frac{\Delta i_L}{2}\right) \qquad (5-2)$$

$$I_{SW(limit)} = 1.2 \cdot \left(5\ A + \frac{2\ A}{2}\right) = 7.2\ A$$

The controller's internal current feedback parameters also affect the sense resistor value. Table 5-6 lists several internal LM3478 current feedback parameters. These values

describe the voltage required to trigger the current limit. The LM3478 provides an internal slope compensation ramp, preventing sub-harmonic oscillation during operation at duty cycles above 50% [37].

Table 5-6. LM3478 Current Sense Feedback Parameters [37]

Parameter	Value (mV)			Description
	Min.	Typ.	Max.	
V_{SENSE}	135	156	180	Current sense threshold voltage.
V_{SL}	52	92	132	Internal compensation ramp voltage.
V_{SL}ratio	0.3	0.49	0.7	V_{SL}/V_{SENSE} ratio.
V_{SC}	250	343	415	Short-circuit current limit voltage.

The desired current limit and LM3478 current feedback parameters determine the required sense resistor value (5-3) [37]. Both converters use a 15 mΩ sense resistor.

$$R_{SEN} = \frac{V_{SENSE} - (D \cdot V_{SENSE} \cdot V_{SLratio})}{I_{SW(limit)}} \qquad (5-3)$$

$$R_{SEN} = \frac{0.156\,V - (0.7 \cdot 0.156\,V \cdot 0.49)}{7.2\,A} = 14.235\,m\Omega$$

An upper limit prevents the sense resistance from affecting the current feedback loop stability (5-4), without adding additional, external slope compensation [37].

$$R_{SEN} < \frac{2V_{SL} \cdot f \cdot L}{V_{OUT} - 2V_{IN}} \qquad (5-4)$$

$$R_{SEN} < \frac{2 \cdot (0.092\,V \cdot 200\,kHz \cdot 10\,\mu H)}{20\,V - 12\,V} < 46\,m\Omega$$

The selected 15 mΩ sense resistor falls well below the stability threshold.

5.2.3 Output Voltage Divider

Programming the converter's output requires a voltage divider sized to provide 1.26 V at the feedback (FB) pin, matching an internal reference [37]. The feedback signal and reference voltage drive an error amplifier. The error signal offsets the current limit

threshold voltage, approaching zero as the controller achieves output regulation. Figure 5-2 depicts the feedback network designed to program a 20 V output.

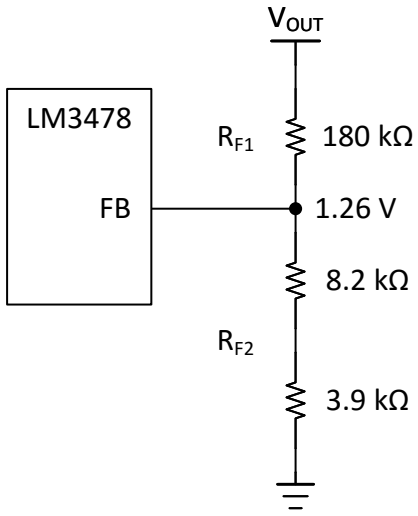

Figure 5-2. Output Voltage Feedback Divider

The datasheet provides an equation for R_{F2} (5-2), which rearranged specifies the ratio of R_{F1} to R_{F2} (5-3).

$$R_{F2} = \frac{(1.26\ V) \cdot R_{F1}}{(V_{OUT} - 1.26\ V)} \qquad (5-5)$$

$$\frac{R_{F1}}{R_{F2}} = \frac{V_{OUT}}{1.26\ V} - 1 \qquad (5-6)$$

The Figure 5-2 network achieves the ratio required to program a 20 V output using standard, 1% tolerance resistor values.

$$\frac{R_{F1}}{R_{F2}} = \frac{20\ V}{1.26\ V} - 1 = 14.873 \approx \frac{180\ k\Omega}{(8.2\ k\Omega + 3.9\ k\Omega)} = 14.876$$

5.2.4 Loop Compensation

Current-mode control eases the LM3478 compensation requirements. A type-I integrator sufficiently compensates most LM3478 boost applications [38]. Figure 5-3

shows the loop compensator design, adding both a pole and a zero to the control-to-output transfer function.

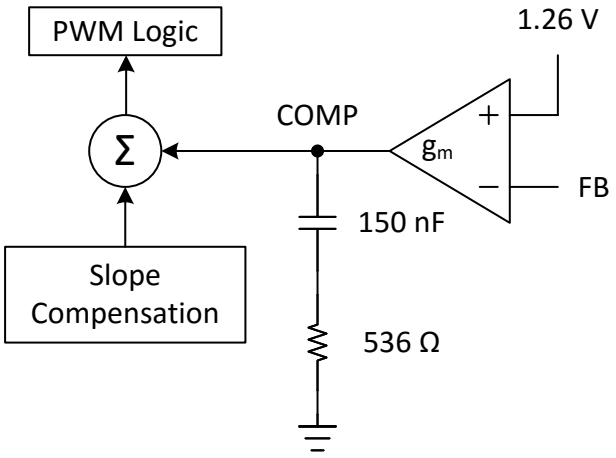

Figure 5-3. LM3478 Type-I Loop Compensator

The selected compensator design provides adequate performance during steady-state converter testing. Further optimization falls outside the steady-state hardware operation scope. Appendix C fully documents compensator design calculations per Texas Instruments guidelines [38].

5.3 Implementation and Testing

Eagle CAD provides the schematic capture and PCB layout tools to complete hardware implementation. Matching the converters' operating conditions to the highest achievable degree minimizes the impact of non-topological factors on performance measurements. This task raises significant challenges, but the results demonstrate the modified boost topology's ability to reduce input current ripple.

5.3.1 Schematics

The converter schematics reflect designed similarities, using identical components and connections. The topological power-path modification creates the only significant difference between the two schematics. Figure 5-4 and Figure 5-5 show simplified schematics of the standard and modified boost converters. For simplicity, C_{IN} and C_{OUT} refer to the multiple MLCCs comprising the input and output capacitors. Likewise, C_1 refers to the multiple MLCCs comprising the modified boost's auxiliary capacitor. Each inductor carries the reference designator associated with the theoretical circuit; L in the standard boost and L_1 and L_2 in the modified boost. The simplified schematics also condense the frequency adjust and output feedback networks made up of multiple resistors.

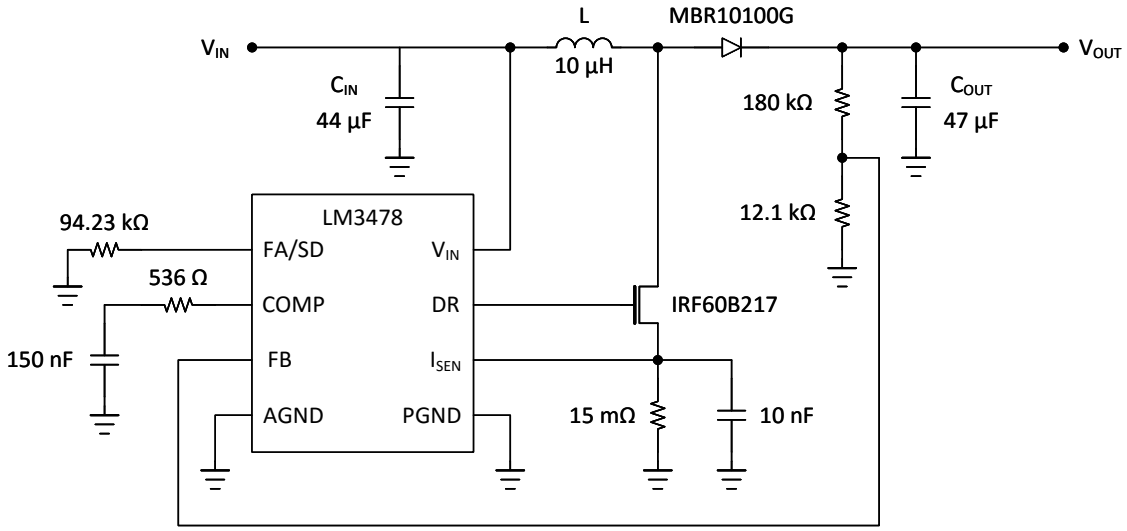

Figure 5-4. Simplified Standard Boost Design Schematic

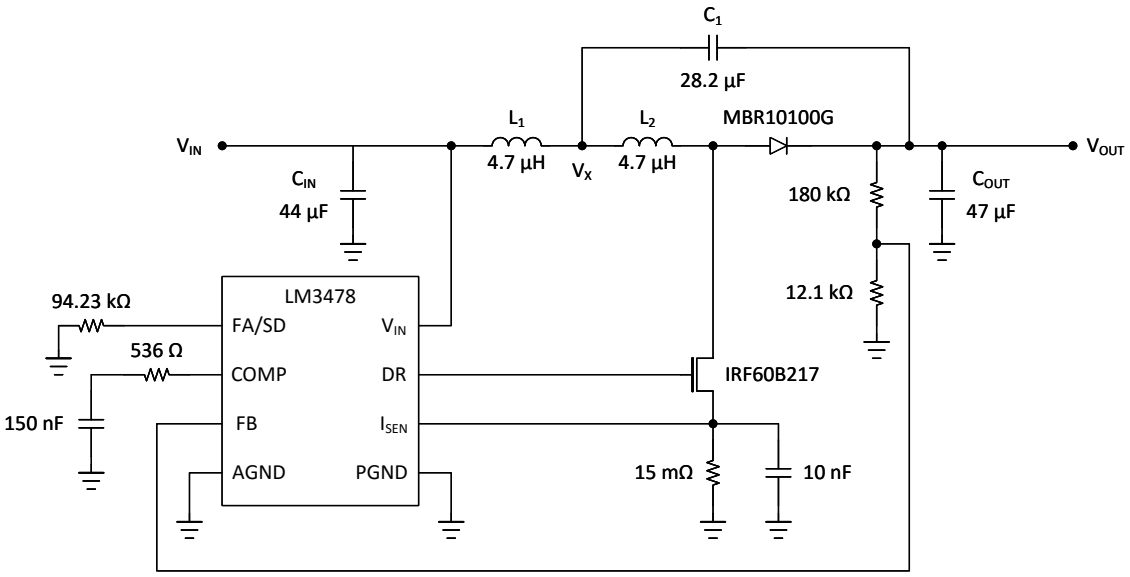

Figure 5-5. Simplified Modified Boost Design Schematic

Appendix D presents the complete schematics produced using Eagle CAD and the electrical bill of materials, detailing component ratings and tolerances.

5.3.2 PCB Layout

Each converter occupies half of the two-layer board. The control circuits receive identical layout and both power paths generally follow a ‘U’ shape. Copper polygons connect power components, minimizing conduction losses along the power path. Both converters share a ground plane that resembles a ‘3’ enclosing the power paths on top and bottom layers. Figure 5-6 highlights these PCB attributes. Appendix D contains large images of both PCB layers.

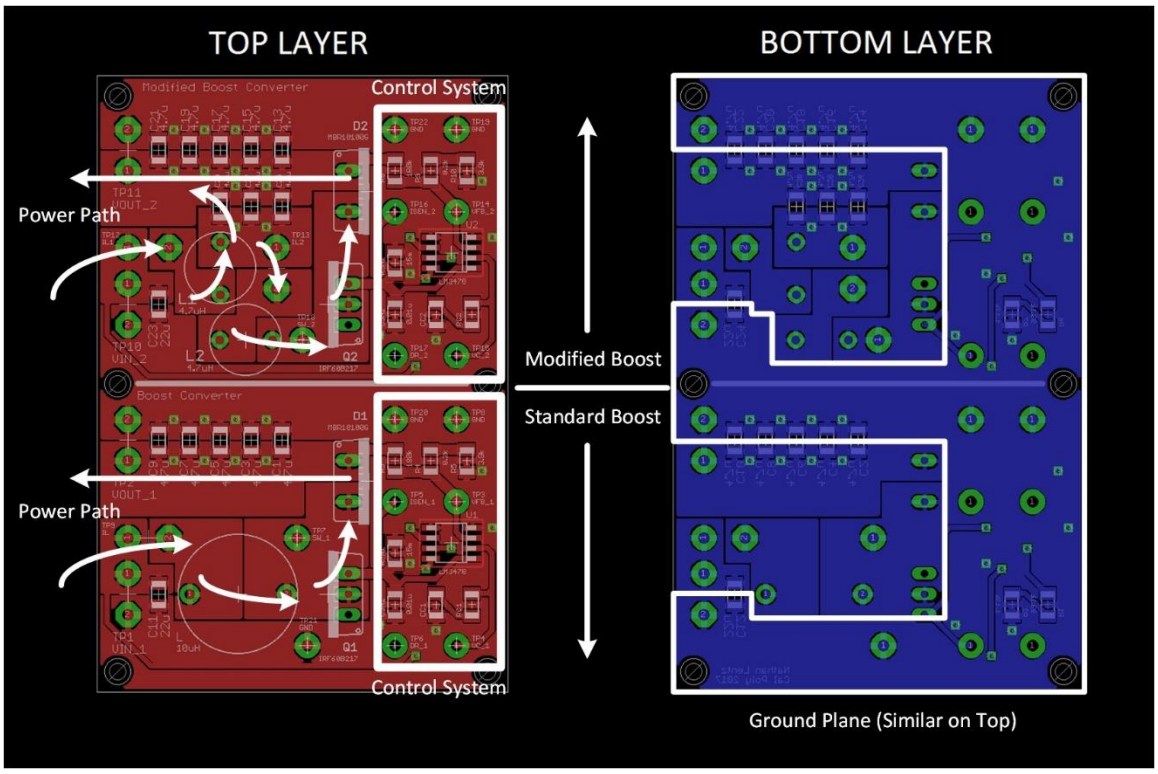

Figure 5-6. Top and Bottom PCB Layers Annotated

Figure 5-7 shows both converters assembled on the PCB, before adding current-probe wire loops.

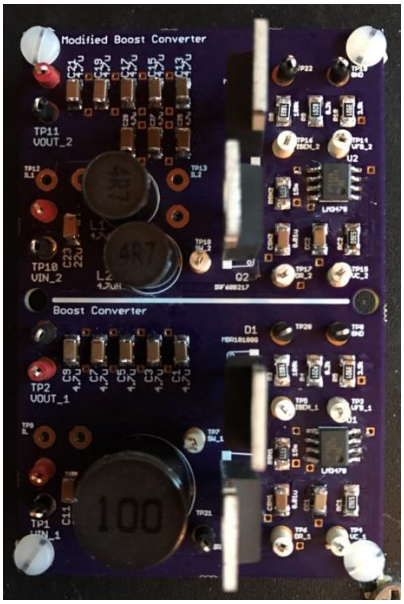

Figure 5-7. Assembled PCB (Top View)

5.3.3 Test Configuration

The hardware test configuration contains a Goodwill Instruments GPR-6060D DC power supply, two Rigol DM3058E multimeters, a Teledyne LeCroy HD4096 oscilloscope, and a BK Precision 8510 electronic load. The power supply and electronic load indicate DC input and output current. The multimeters measure DC voltage directly at each converter's input and output terminals. The oscilloscope, triggered by the converter's gate drive signal, primarily provides state variable measurements.

Figure 5-8 depicts each instrument's connection to the standard boost converter.

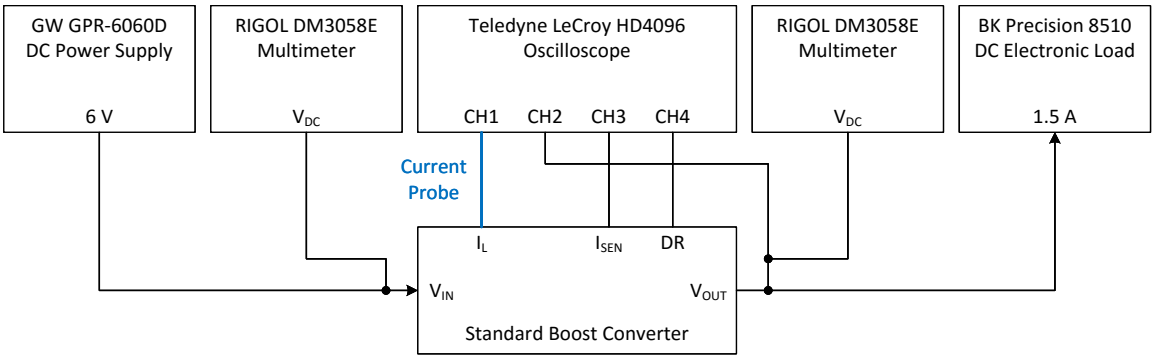

Figure 5-8. Standard Boost Converter Hardware Test Connections

Figure 5-9 illustrates the modified boost converter's connections to each test instrument. Oscilloscope connections vary depending on the state variable measurement. The scope's current probe alternates between the PCB's L_1 and L_2 current measurement loops. The CH3 scope probe contacts the current sense voltage test point during L_2 current measurements. The scope measures C_1 voltage as the difference between the V_x voltage on CH3 and the output voltage on CH2.

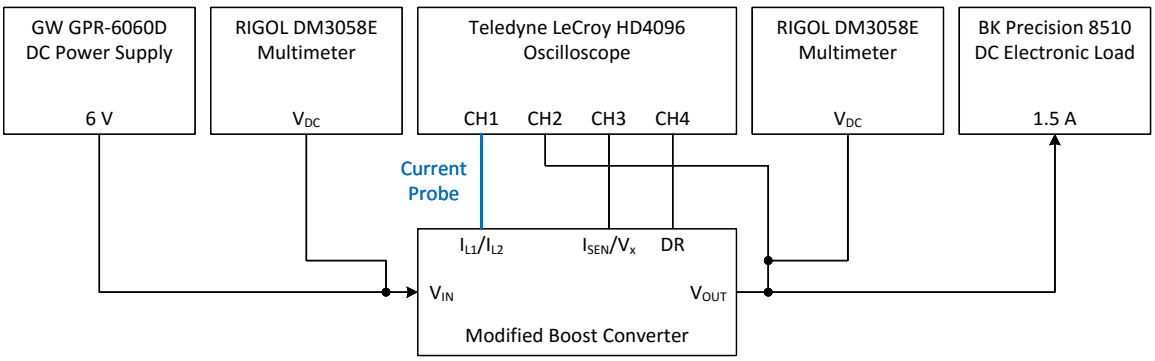

Figure 5-9. Modified Boost Converter Hardware Test Connections

During initial testing, the controller's current limit prevented both converters from achieving nominal output voltage at full load conditions. Large inductor current ripple carried through the sense resistor triggered the current sense voltage threshold, limiting PWM duty cycle and lowering output voltage. The modified design's larger L_2 current ripple limits the duty cycle more than the standard design's inductor current ripple, causing a difference in output voltage. Lowering the sense resistor value raises the controller's current limit, alleviating the output voltage difference at full load. Table 5-7 compares the output voltage difference after dropping the sense resistance from 15 mΩ to 12 mΩ.

Table 5-7. Converter Output Voltage Difference at Full Load

Sense Resistor	15 mΩ	12 mΩ
Standard Boost V_{OUT}	16.23 V	18.39 V
Modified Boost V_{OUT}	15.3 V	17.86 V
Difference	0.93 V	0.53 V

Table 5-8 compares each converter's DC characteristics measured at full load after reducing the current sense resistance. Considering tolerances and parasitic effects, the difference between full-load DC characteristics proves acceptable. The primary comparison metric, input current ripple percentage, remains unaffected by a small DC input current difference.

Table 5-8. Converter Full Load DC Characteristics Comparison

	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency
Standard Boost	5.27	6.08	32.04	18.39	1.5	27.58	86.08%
Modified Boost	5.3	5.81	30.79	17.86	1.5	26.79	87.01%
Difference	-0.03	0.27	1.25	0.53	0	0.79	-0.93%

Figure 5-10 describes each test point used testing the converter assemblies. The V_X node's wire lead connects at the beginning of the L_2 current-probe loop. Both final assemblies contain 12 mΩ sense resistors.

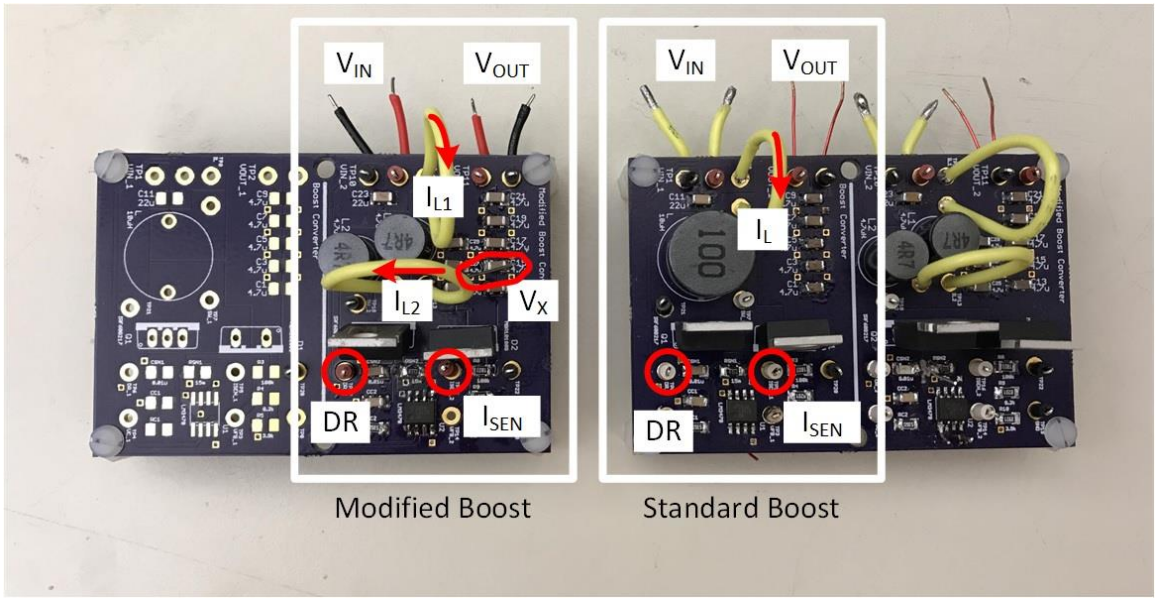

Figure 5-10. Final Converter Assembly Test Points

Figure 5-11 depicts the complete test configuration on the laboratory bench. The DC power supply and electronic load connect to the converter's mounted input and output terminals, minimizing current path resistance. Multimeters and the output voltage scope probe connect to the additional wire leads.

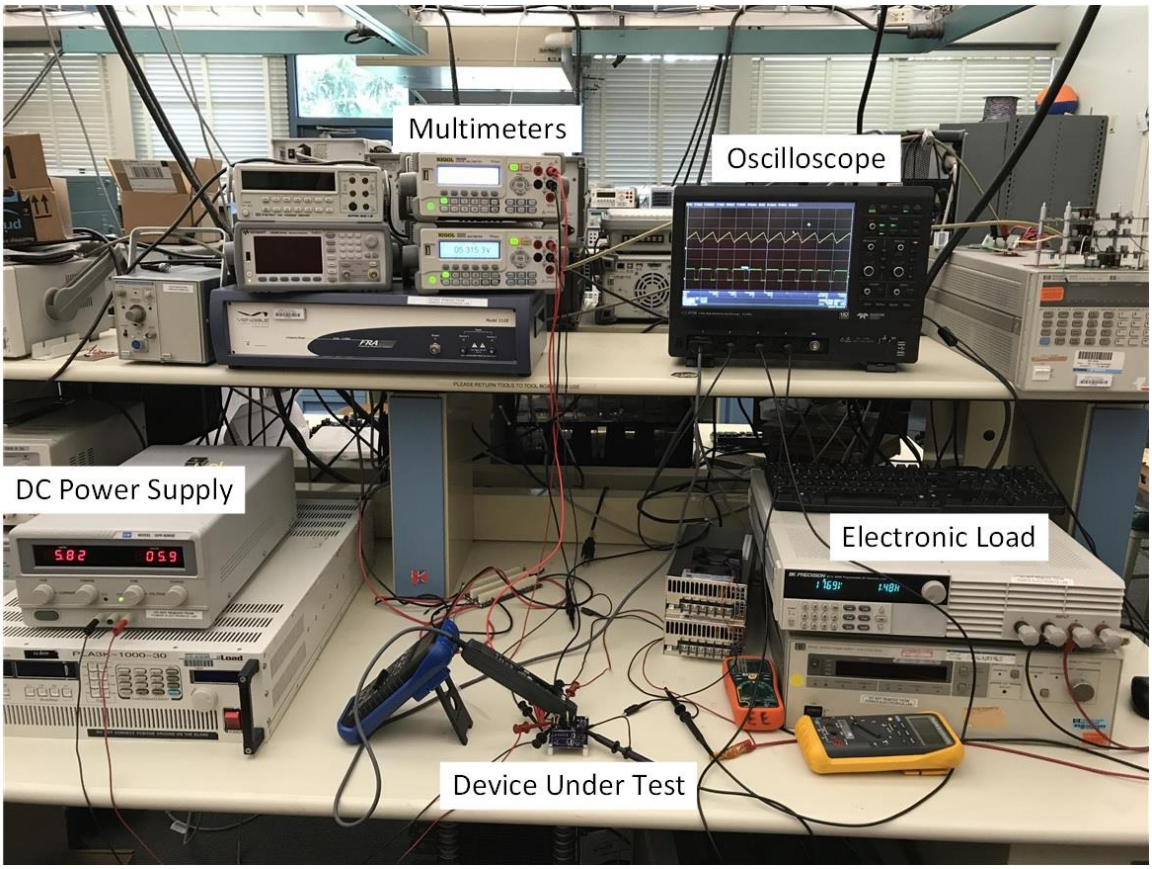

Figure 5-11. Laboratory Test Configuration

5.3.4 State Variable Measurements

Both converter state variable measurements rely on a combination of built-in scope measurement functions and manual cursor measurements, applied under appropriate signal coupling conditions.Table 5-9 summarizes the method used for each measurement. Parasitic ringing eliminates the scope's ability to autonomously measure maximum, minimum, and peak to peak voltage values; cursor measurements better represent topological performance.

Table 5-9. State Variable Oscilloscope Measurement Methods

Measurement	Current		Voltage	
	Coupling	Cursors	Coupling	Cursors
Average	DC	N	DC	N
RMS	DC	N	DC	N
AC RMS	AC	N	AC	N
Maximum	DC	N	AC	Y
Minimum	DC	N	AC	Y
Peak-Peak	DC	N	AC	Y

Figure 5-12 depicts the standard boost hardware's inductor current waveform. The current exhibits the expected triangular shape, but the 75.5% duty cycle and 185.8 kHz switching frequency differ from nominal values.

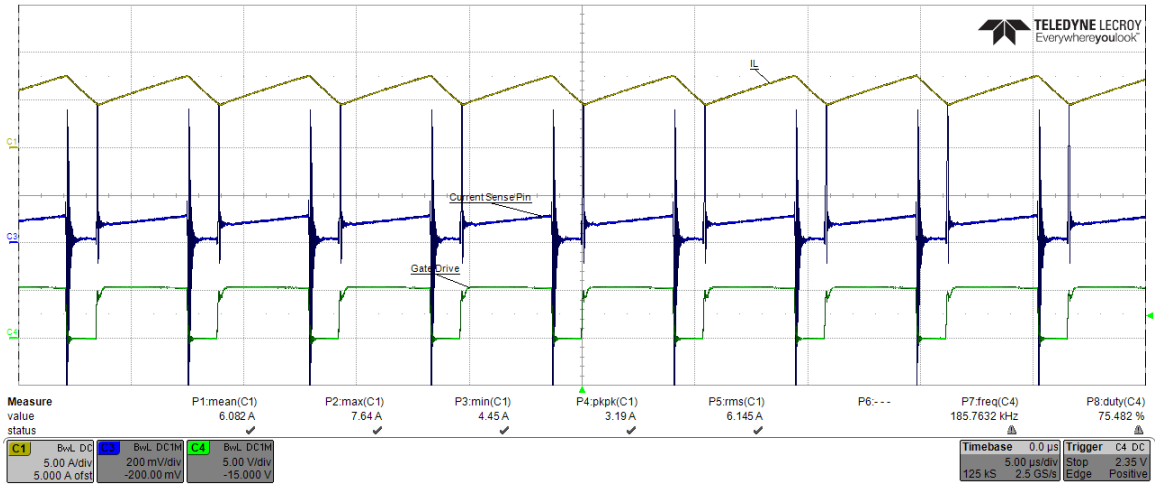

Figure 5-12. Standard Boost Hardware Inductor Current

Figure 5-13 illustrates the standard boost output voltage measurement. Ignoring the implementation's parasitic ringing, the waveform follows the expected characteristic trends; negative linear slope with the switch on, and concave down quadratic with the switch off.

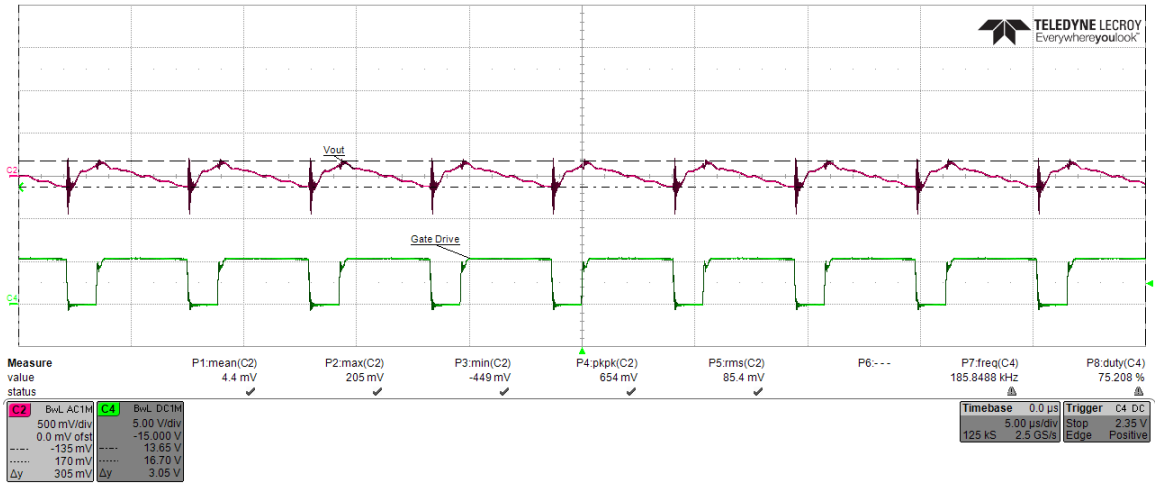

Figure 5-13. Standard Boost Hardware Output Voltage (AC Coupling)

Table 5-10 lists the standard boost design's hardware state variable measurements. The converter's power loss increases the average inductor current and switching duty cycle. Inductance tolerance, increased duty cycle, and decreased switching frequency account for the 52.45% current ripple. Increased inductor current ripple flows through the output capacitor, raising the output voltage ripple.

Table 5-10. Standard Boost Converter Hardware Test Results

	I_L (A)	V_{out} (V)
Average	6.082	18.231
RMS	6.145	18.232
AC RMS	0.897	0.0854
Max.	7.64	18.401
Min.	4.45	18.096
Peak-Peak	3.19	0.305
%Ripple	52.45%	1.67%

Figure 5-14 shows the modified boost L_1 current measurement. The waveform looks almost triangular, but curves before the switch turns off. Like the standard boost, the 74.333% duty cycle and 192.66 kHz switching frequency differ from nominal values.

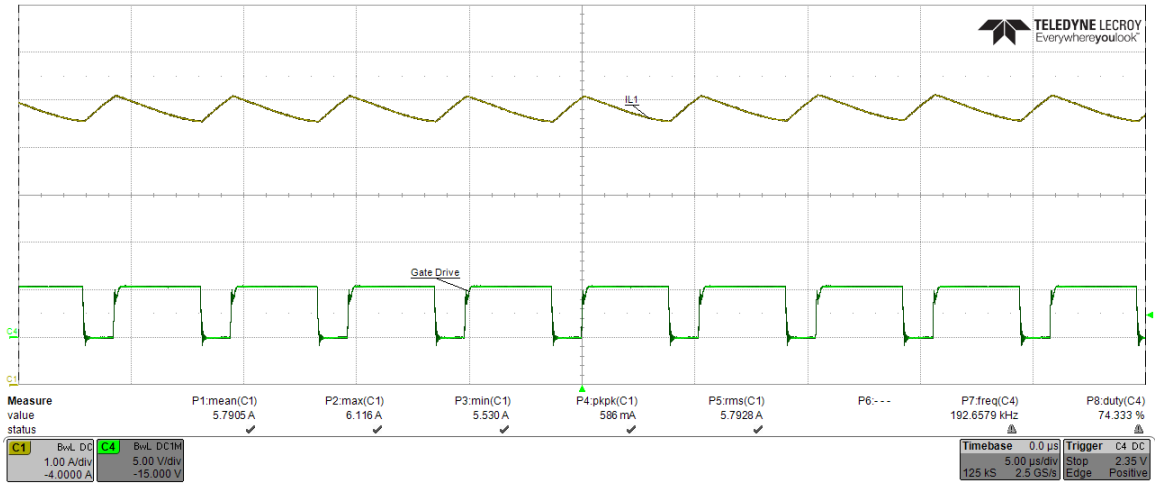

Figure 5-14. Modified Boost Hardware L_1 Current

Figure 5-15 portrays the modified boost L_2 current waveform, precisely matching a triangular shape.

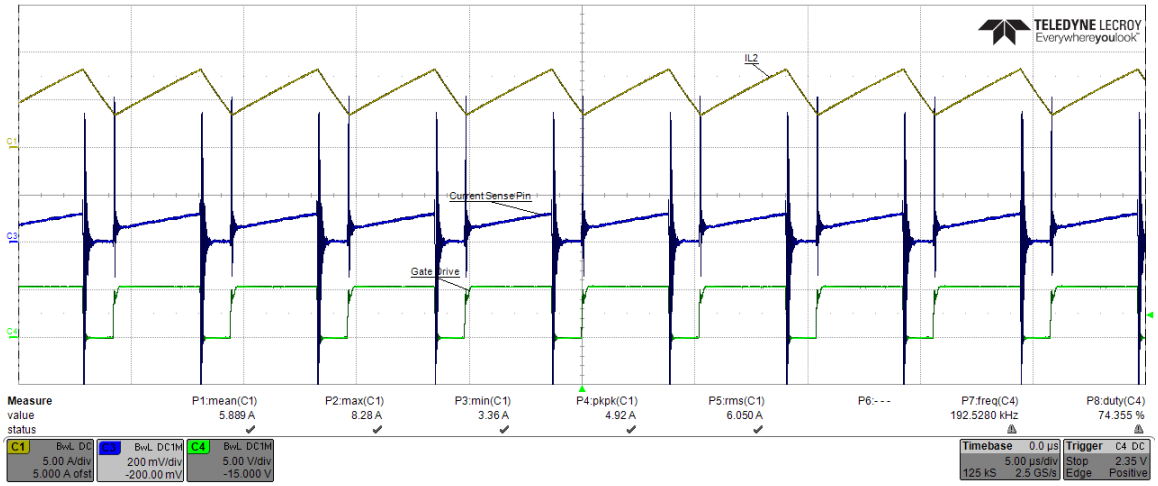

Figure 5-15. Modified Boost Hardware L_2 Current

Figure 5-16 illustrates C_1 voltage measurement for the modified boost converter. This measurement determines voltage between the V_X and V_{out} nodes using the scope's math function. Parasitic ringing affects both nodes, and the resulting voltage differential. Small oscillations obscure the underlying waveform shape, which only vaguely resembles simulation results.

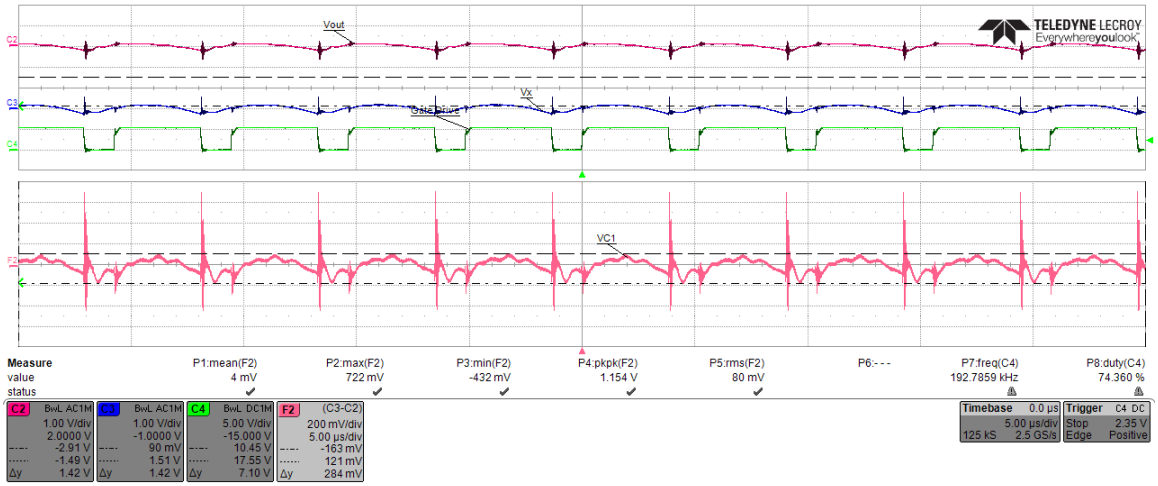

Figure 5-16. Modified Boost Hardware C_1 Voltage (AC Coupling)

Figure 5-17 contains the modified boost converter's output voltage measurement. Ignoring parasitic oscillation and small oscillations, the general waveform shape resembles a quadratic curve with the switch on, and a linear slope with the switch off.

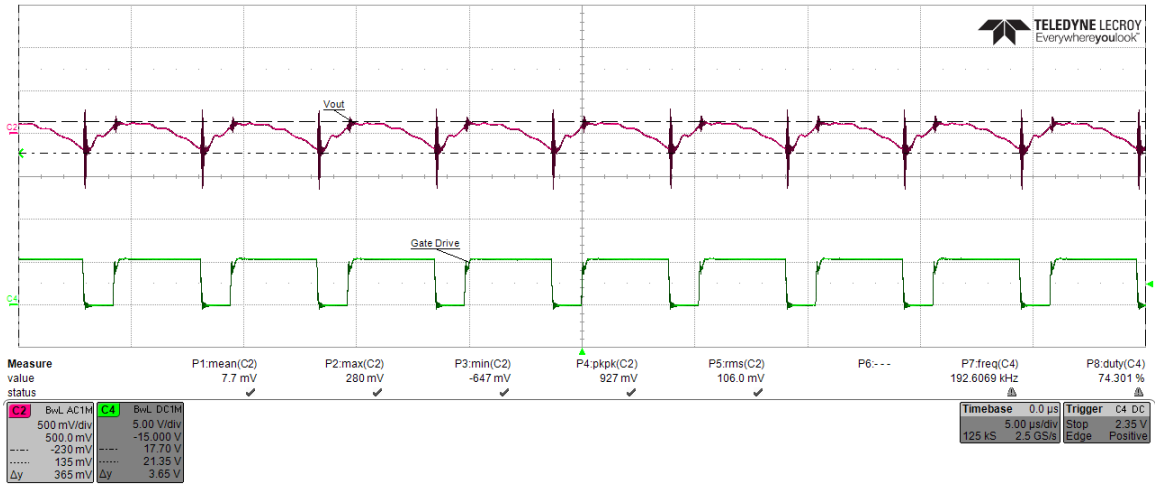

Figure 5-17. Modified Boost Hardware Output Voltage (AC Coupling)

Table 5-11 lists the modified boost converter state variable measurements. Like the standard converter, power dissipation increased the average inductor currents and duty cycle. Inductor tolerances, increased duty cycle, and decreased switching frequency impact peak-to-peak L_2 current ripple; larger average L_2 current keeps the percent ripple

close to the nominal 80% value. Despite non-ideal output voltage regulation, the C1 voltage remains consistent with the converter's DC characteristics; the difference between average input voltage (5.3 V) and output voltage. Larger L2 ripple current also increases C_1 and output voltage ripple.

Table 5-11. Modified Boost Converter Hardware Test Results

	I_{L1} (A)	I_{L2} (A)	V_{C1} (V)	V_{out} (V)
Average	5.7905	5.889	-12.512	17.825
RMS	5.7928	6.05	12.512	17.825
AC RMS	0.1636	1.41	0.08	0.106
Max.	6.116	8.349	-12.391	17.96
Min.	5.53	3.469	-12.675	17.595
Peak-Peak	0.586	4.88	0.284	0.365
%Ripple	10.12%	82.87%	2.27%	2.05%

5.3.5 Irregular Conduction Limitations

Theoretically, raising the controller's current limit further, by lowering sense resistance, allows both converters to regulate output voltage closer to the nominal value at full load. In practice, operating too far below the controller's current limit caused irregular conduction patterns. Figure 5-18 shows the standard boost converter's irregular periodic conduction under 800 mA loading.

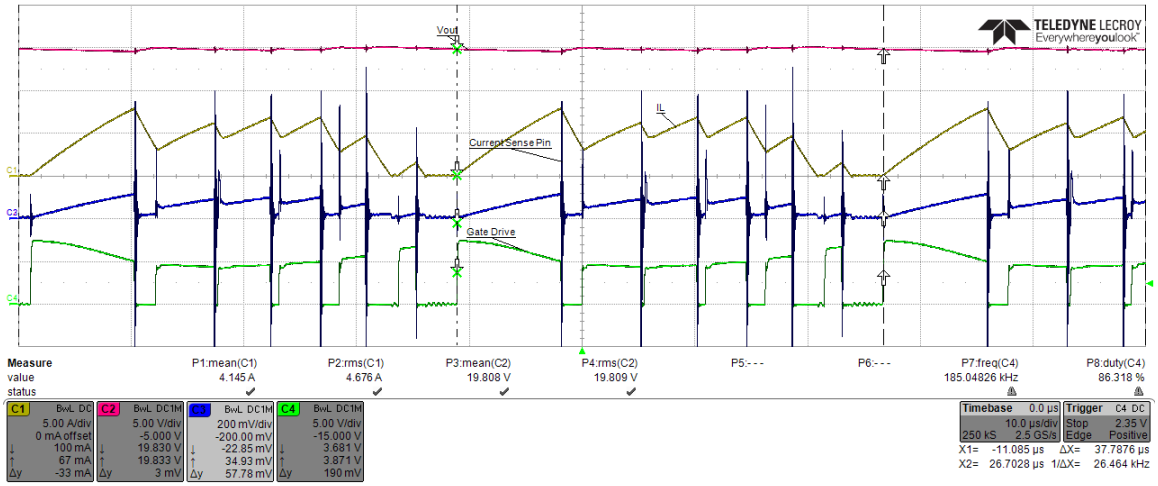

Figure 5-18. Standard Boost Subharmonic Oscillation at 800 mA Load

Figure 5-19 shows the modified boost converter's irregular conduction pattern under 1.1 A loading.

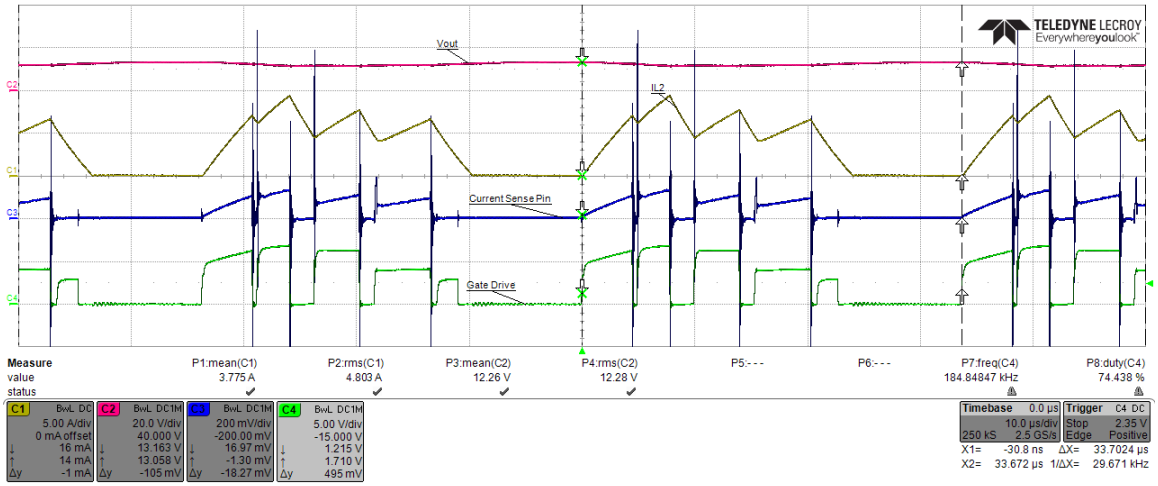

Figure 5-19. Modified Boost Subharmonic Oscillation at 1.1 A Load

The inductor currents resemble the subharmonic oscillations that occur in current-controlled converters at duty cycle above 50% [37]. The LM3478 provides internal slope compensations to prevent subharmonic oscillation. The datasheet establishes a sense resistance limit (5-4), beyond which additional slope compensation becomes necessary. The converter parameters establish a 46 mΩ sense resistance limit, well above the

original (15 mΩ) and final (12 mΩ) implemented values. Despite similar appearances, subharmonic oscillation does not completely explain the irregular conduction patterns.

Both converters exhibit similarly irregular inductor current, suggesting the control system, identical in each converter, causes the behavior. This issue prevents further improving output voltage regulation at full load. Neither converter could achieve steady-state, CCM operation under 1.5 A loading with a sense resistor less than 12 mΩ.

5.4 Performance Comparison

Several hardware factors forcing non-ideal operation affected the two converters differently. Average output voltage at full load, dependent on the controller's current limit, differs by 0.53 V (Table 5-7). Larger peak current through the switch caused lower output voltage in the modified boost converter. The controller's internal current limit tolerance also impacts the output voltage difference for better or worse. Switching frequency averages 185.7 kHz in the standard boost and 192.6 kHz in the modified boost. The difference, 6.9 kHz (3.72%), falls outside the frequency adjust resistor network's 2%, implicating internal oscillator tolerances. Parasitic resistances along the power path, due to layout or component tolerances, cause conduction losses. Switching losses change with frequency, parasitic MOSFET capacitance, and diode reverse recovery. Converter efficiency, the accumulation of these loss factors, differs by 0.93% (Table 5-8); most importantly affecting the average inductor currents.

Despite these differences, the modified boost converter hardware demonstrates a significant input current ripple reduction on a percent basis. Table 5-12 summarizes the input current performance of each converter.

Table 5-12. Hardware Input Current Ripple Comparison

	Standard Boost	Modified Boost	Difference
Average	6.082 A	5.7905 A	0.2915 A
Peak-Peak	3.19 A	0.586 A	2.604 A
%Ripple	52.45%	10.12%	42.33%

The converters' average inductor current exceeds the nominal 5 A value. Peak-to-peak current ripple also tops simulated values (Table 4-10). Relative to the simulations, both hardware measures increase almost proportionally in each converter; the corresponding hardware current ripple percentages both calculate approximately 10% above simulated values. Thus, the modified boost converter provides consistent input current ripple reduction, 41.08% to 42.33%, across simulation and hardware. Figure 5-20 illustrates this trend.

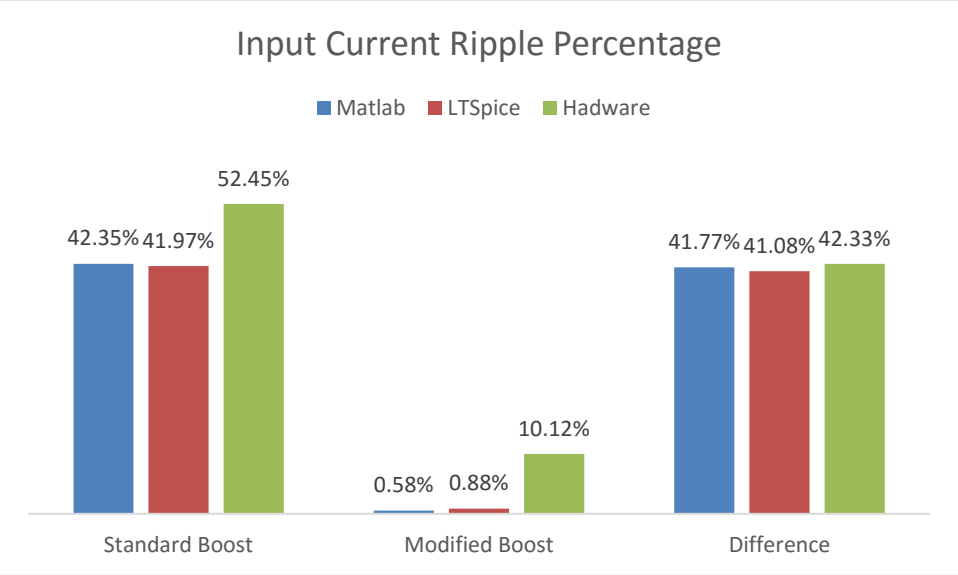

Figure 5-20. Input Current Ripple Performance in Simulation and Hardware

6. CONCLUSION

This thesis demonstrates the significant input current ripple reduction, approximately 40%, provided by Karanam's modified boost converter. The topological modification prevents complete analysis using simplistic DC/DC converter techniques. A state-space analysis describes the converter's steady-state, CCM operation and numerical state-equation solutions provide theoretical current ripple measurements. This approach produces results consistent with a standard LTSpice simulation.

Hardware realities created differing output voltage conditions under full load. Current through each converter exceeds theoretical expectations due to power dissipation. Minimizing the difference between the converters' DC output voltage required adjusting the switching controller's current limit. Lowering the current sense resistance raises the current limit, improving output regulation. An unexplained control system property prevents CCM operation under 1.5 A loading, with a sense resistor lower than 12 mΩ. This prevents ideal output voltage regulation in both converters. During final testing, the converters average output voltages differed by 0.53 V, the maximally equivalent operating condition achieved.

The hardware performance measurements reflect the impact of component tolerances and parasitic effects. Percent input current ripple increased in both converters, compared against simulated predictions. Regardless, the percent current ripple reduction, between the standard and modified boost topologies, remains consistent across hardware; 41.77%, 41.08%, and 42.33% in Matlab, LTSpice, and hardware. The consistency demonstrates the topological modification's benefit, in theory and practice.

Reducing a boost converter's input current ripple generally benefits many applications. The modified boost converter either reduces input ripple, given a fixed input capacitance, or reduces the input capacitance required to ensure a specified input ripple. The modified topology does not require additional inductance or a significant board area increase. These characteristics all benefit noise-sensitive, space- and cost-constrained systems such as solar PV microinverters or battery-powered portable electronics.

Widespread application of Karanam's modified boost converter faces significant challenges. This thesis concerned only the converter's steady-state, CCM operation. Future work must also examine steady-state, DCM operation using a new or similar analysis technique. An optimized, iterative state-equation solution method would benefit any future CCM or DCM analysis. While functional, the method this work proposes provides minimal computational efficiency. These future analyses may provide optimized design procedures necessary to repeatedly implement the modified boost topology. The converter's transient characteristics also merit further investigation. Modelling the voltage- and current-mode control transfer functions would inform controller selection and optimal loop compensation. This future work will decide the circumstances where Karanam's modified boost converter provides the most benefit.

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APPENDICES

A. MATLAB Scripts

boost_cycle.m

```
%-------------------------------------------------------------------------
--
% Solve the boost converter state equation over one switching cycle
% Parameters:
%   Vin  --  Input Voltage (V)
%   Vout --  Output Voltage (V)
%   Iin  --  Input Current (A)
%   T    --  Switching Period (Hz)
%   D    --  Duty Cycle
%   R    --  Load Resistance (Ohms)
%   L    --  Inductance (H)
%   C    --  Output Capacitance (F)
% Returns:
%   m    --  m-Axis Vector
%   sol  --  State Solution Vector
%-------------------------------------------------------------------------
--
function [m, sol] = boost_cycle(Vin,Vout,Iin,T,D,R,L,C)
%-- Define Constants ---------------------------------------------------
--
% Switching Intervals
sw_on_interval = [0 D];
sw_off_interval = [D 1];
% State Variable Steady-State Error Tolerances
sum_ss_error_tol = 0.000002;    % Sum of all state variable errors
il_ss_error_tol = 0.000001;     % Inductor current errors
%-- Initial Solution ---------------------------------------------------
--
% Estimate initial state values
init_state = [Iin Vout];
% Switch-On state equation and solution
sw_on_eqn = @(m,x1) [(T/L)*Vin;
                     (-T/(C*R))*x1(2)];
[m1,x1_sol] = ode45(sw_on_eqn,sw_on_interval,init_state);
% Establish intermediate state values
interm_state = [x1_sol(end,1) x1_sol(end,2)];
% Switch-Off state equation and solution
sw_off_eqn = @(m,x2) [(-T/L)*x2(2)+((T/L)*Vin);
                      ((T/C)*x2(1))+((-T/(C*R))*x2(2))];
[m2,x2_sol] = ode45(sw_off_eqn,sw_off_interval,interm_state);
% Establish final state values
fin_state = [x2_sol(end,1) x2_sol(end,2)];
% Calculate state error
error = abs((fin_state-init_state)./init_state);
%-- Iterative Solutions ------------------------------------------------
--
while (sum(error) >= sum_ss_error_tol) && (error(1) >= il_ss_error_tol)
    % Update initial state values
    init_state = fin_state;
    % Switch-On state equation and solution
    sw_on_eqn = @(m,x1) [(T/L)*Vin;
```

```
                        (-T/(C*R))*x1(2)];
    [m1,x1_sol] = ode45(sw_on_eqn,sw_on_interval,init_state);
    % Update intermediate state values
    interm_state = [x1_sol(end,1) x1_sol(end,2)];
    % Switch-Off state equation and solution
    sw_off_eqn = @(m,x2) [(-T/L)*x2(2)+((T/L)*Vin);
                          ((T/C)*x2(1))+((-T/(C*R))*x2(2))];
    [m2,x2_sol] = ode45(sw_off_eqn,sw_off_interval,interm_state);
    % Update final state values
    fin_state = [x2_sol(end,1) x2_sol(end,2)];
    % Calculate updated state error
    error = abs((fin_state-init_state)./init_state);
end

%-- Concatenate Return Vectors ---------------------------------------
--

% m-axis
m = [m1; m2(2:end)];
% State solution
sol = [x1_sol(:,1) x1_sol(:,2); x2_sol(2:end,1) x2_sol(2:end,2)];

end
```

boost_mod_cycle.m

```
%-------------------------------------------------------------------------
--
% Solve the modified boost converter state equation over a switching
cycle
% Parameters:
%   Vin  --  Input Voltage (V)
%   Vout --  Output Voltage (V)
%   Iin  --  Input Current (A)
%   T    --  Switching Period (Hz)
%   D    --  Duty Cycle
%   R    --  Load Resistance (Ohms)
%   L1   --  Inductance (H)
%   L2   --  Inductance (H)
%   C1   --  Capacitance (F)
%   C2   --  Capacitance (F)
% Returns:
%   m    --  m-Axis Vector
%   sol  --  State Solution Vector
%   ic   --  Capacitor Current Vector
%-------------------------------------------------------------------------
--

function [m, sol, ic] = boost_mod_cycle(Vin,Vout,Iin,T,D,R,L1,L2,C1,C2)

%-- Define Constants -----------------------------------------------------
--

% Average Output Current
Iout = (Vin*Iin)/Vout;
% Switching Intervals
sw_on_interval = [0 D];
sw_off_interval = [D 1];
% State Variable Steady-State Error Tolerances
sum_ss_error_tol = 0.000004;
il1_ss_error_tol = 0.000001;

%-- Initial Solution -----------------------------------------------------
--

% Estimate initial state values
```

```
init_state = [Iin Iin -D*Vout Vout];
% Switch-On state equation and solution
sw_on_eqn = @(m,x1) [(-T/L1)*x1(3)+(-T/L1)*x1(4)+(T/L1)*Vin;
              (T/L2)*x1(3)+(T/L2)*x1(4);
              (T/C1)*x1(1)+(-T/C1)*x1(2);
              (T/C2)*x1(1)+(-T/C2)*x1(2)+(-T/(C2*R))*x1(4)];
[m1,x1_sol] = ode45(sw_on_eqn,sw_on_interval,init_state);
ic1 = [x1_sol(:,1)-x1_sol(:,2) (x1_sol(:,1)-x1_sol(:,2))-Iout];
% Establish intermediate state values
interm_state = [x1_sol(end,1) x1_sol(end,2) x1_sol(end,3) x1_sol(end,4)];
% Switch-Off state equation and solution
sw_off_eqn = @(m,x2) [(-T/L1)*x2(3)+(-T/L1)*x2(4)+(T/L1)*Vin;
              (T/L2)*x2(3);
              (T/C1)*x2(1)+(-T/C1)*x2(2);
              (T/C2)*x2(1)+(-T/(C2*R))*x2(4)];
[m2,x2_sol] = ode45(sw_off_eqn,sw_off_interval,interm_state);
ic2 = [x2_sol(:,1)-x2_sol(:,2) x2_sol(:,1)-Iout];
% Establish final state values
fin_state = [x2_sol(end,1) x2_sol(end,2) x2_sol(end,3) x2_sol(end,4)];
% Calculate state error
error = abs((fin_state-init_state)./init_state);

%-- Iterative Solutions ------------------------------------------------
--

while (sum(error) >= sum_ss_error_tol) && (error(1) >= il1_ss_error_tol)
    % Update initial state values
    init_state = fin_state;
    % Switch-On state equation and solution
    sw_on_eqn = @(m,x1) [(-T/L1)*x1(3)+(-T/L1)*x1(4)+(T/L1)*Vin;
                  (T/L2)*x1(3)+(T/L2)*x1(4);
                  (T/C1)*x1(1)+(-T/C1)*x1(2);
                  (T/C2)*x1(1)+(-T/C2)*x1(2)+(-T/(C2*R))*x1(4)];
    [m1,x1_sol] = ode45(sw_on_eqn,[0 D],init_state);
    ic1 = [x1_sol(:,1)-x1_sol(:,2) (x1_sol(:,1)-x1_sol(:,2))-Iout];
    % Establish intermediate state values
    interm_state = [x1_sol(end,1) x1_sol(end,2) x1_sol(end,3)
x1_sol(end,4)];
    % Switch-Off state equation and solution
    sw_off_eqn = @(m,x2) [(-T/L1)*x2(3)+(-T/L1)*x2(4)+(T/L1)*Vin;
                  (T/L2)*x2(3);
                  (T/C1)*x2(1)+(-T/C1)*x2(2);
                  (T/C2)*x2(1)+(-T/(C2*R))*x2(4)];
    [m2,x2_sol] = ode45(sw_off_eqn,sw_off_interval,interm_state);
    ic2 = [x2_sol(:,1)-x2_sol(:,2) x2_sol(:,1)-Iout];
    % Update final state values
    fin_state = [x2_sol(end,1) x2_sol(end,2) x2_sol(end,3)
x2_sol(end,4)];
    % Calculate updated state error
    error = abs((fin_state-init_state)./init_state);
end

%-- Concatenate Return Vectors -----------------------------------------
--

% m-axis
m = [m1; m2(2:end)];
% State solution
sol = [x1_sol(:,1)     x1_sol(:,2)     x1_sol(:,3)     x1_sol(:,4);
       x2_sol(2:end,1) x2_sol(2:end,2) x2_sol(2:end,3) x2_sol(2:end,4)];
% Capacitor current
ic = [ic1(:,1)     ic1(:,2);
      ic2(2:end,1) ic2(2:end,2)];

end
```

boost_mod_design_comp.m

```
%-------------------------------------------------------------------------
% Determine the input current ripple performance across multiple C1 values
% and several L1/L2 inductance splits
%-------------------------------------------------------------------------

%-- Operational Converter Parameters -------------------------------------

Vin = 6;
Vout = 20;
Pout = 30;
f = 200E3;

%-- Calculate Remaining Operational Parameters ---------------------------

Iin = Pout/Vin;
D = -(Vin-Vout)/Vout;
T = 1/f;
R = (Vout^2)/Pout;

%-- Component Value Constraints ------------------------------------------

C1 = [1E-6 5E-6 10E-6 20E-6 30E-6 40E-6 50E-6];
N = length(C1);
C2 = 50E-6;
L = 10E-6;

%-- 50/50 Inductance Split -----------------------------------------------

L1 = 0.5*L;
L2 = 0.5*L;

%-- Solve Converter State Equation ---------------------------------------

state_avg1 = zeros(N,4);
state_max1 = zeros(N,4);
state_min1 = zeros(N,4);
% Loop over C1 values
for n = 1:N
    [m, sol] = boost_mod_cycle(Vin,Vout,Iin,T,D,R,L1,L2,C1(n),C2);
    % Calculate average, max, and min for each state variable solution
    for k = 1:4
        state_avg1(n,k) = mean(sol(:,k));
        state_max1(n,k) = max(sol(:,k));
        state_min1(n,k) = min(sol(:,k));
    end
end

%-- 25/75 Inductance Split -----------------------------------------------

L1 = 0.25*L;
L2 = 0.75*L;

%-- Solve Converter State Equation ---------------------------------------

state_avg2 = zeros(N,4);
state_max2 = zeros(N,4);
state_min2 = zeros(N,4);
% Loop over C1 values
for n = 1:N
    [m, sol] = boost_mod_cycle(Vin,Vout,Iin,T,D,R,L1,L2,C1(n),C2);
    % Calculate average, max, and min for each state variable solution
    for k = 1:4
        state_avg2(n,k) = mean(sol(:,k));
        state_max2(n,k) = max(sol(:,k));
        state_min2(n,k) = min(sol(:,k));
    end
end

%-- 75/25 Inductance Split -----------------------------------------------
```

```
L1 = 7.5E-6;
L2 = 2.5E-6;

%-- Solve Converter State Equation ---------------------------------------

state_avg3 = zeros(N,4);
state_max3 = zeros(N,4);
state_min3 = zeros(N,4);
% Loop over C1 values
for n = 1:N
    [m, sol] = boost_mod_cycle(Vin,Vout,Iin,T,D,R,L1,L2,C1(n),C2);
    % Calculate average, max, and min for each state variable solution
    for k = 1:4
        state_avg3(n,k) = mean(sol(:,k));
        state_max3(n,k) = max(sol(:,k));
        state_min3(n,k) = min(sol(:,k));
    end
end

%-- Calculate current ripple for all inductance splits -------------------

state_ripple1 = state_max1 - state_min1;
state_ripple_percent1 = state_ripple1./abs(state_avg1)*100;

state_ripple2 = state_max2 - state_min2;
state_ripple_percent2 = state_ripple2./abs(state_avg2)*100;

state_ripple3 = state_max3 - state_min3;
state_ripple_percent3 = state_ripple3./abs(state_avg3)*100;

%-- Plot current ripple against C1 values --------------------------------

figure
semilogx(C1,state_ripple_percent1(:,1),C1,state_ripple_percent2(:,1),C1,state_ripp
le_percent3(:,1))
xlabel('C1 Value (F)'); ylabel('L1 Current Ripple Percentage');
legend('50/50 Split','25/75 Split','75/25 Split');
```

boost_sim.m

```
%-------------------------------------------------------------------------
% Determine a standard boost design's state variable waveforms using the
% boost_cycle function. Measure relevant waveform characteristics and plot
% both state variable waveforms.
%-------------------------------------------------------------------------

%-- Operational Converter Parameters -------------------------------------

Vin = 6;
Vout = 20;
Pout = 30;
f = 200E3;

%-- Calculate Remaining Operational Parameters ---------------------------

Iin = Pout/Vin;
D = -(Vin-Vout)/Vout;
T = 1/f;
R = (Vout^2)/Pout;

%-- Design Component Values ----------------------------------------------

L = 10E-6;
C = 50E-6;

%-- Solve State Equation and Separate Waveforms --------------------------

[m, sol] = boost_cycle(Vin,Vout,Iin,T,D,R,L,C);
i = sol(:,1);
v = sol(:,2);

%-- Measure Waveform Characteristics -------------------------------------

state_avg = [mean(i) mean(v)];
```

```
state_max = [max(i) max(v)];
state_min = [min(i) min(v)];
state_ripple = state_max - state_min;
state_ripple_percent = state_ripple./state_avg*100;
state_rms = [root_mean_sq(i) root_mean_sq(v)];
state_rms_ac = [root_mean_sq(i-mean(i)) root_mean_sq(v-mean(v))];

%-- Tabulate Waveform Measurements ----------------------------------------

InductorCurrent  = [state_avg(1);
                    state_rms(1);
                    state_rms_ac(1);
                    state_max(1);
                    state_min(1);
                    state_ripple(1);
                    state_ripple_percent(1)];
CapacitorVoltage = [state_avg(2);
                    state_rms(2);
                    state_rms_ac(2);
                    state_max(2);
                    state_min(2);
                    state_ripple(2);
                    state_ripple_percent(2)];
Measures = {'Average','RMS','AC RMS','Max','Min','Ripple','Percent Ripple'};
tab = table(InductorCurrent,CapacitorVoltage,'RowNames',Measures)

%-- Plot Waveforms ---------------------------------------------------------

figure
subplot(2,1,1)
plot(m,i);
xlabel('m'); ylabel('Inductor Current (A)');
grid on
subplot(2,1,2)
plot(m,v);
xlabel('m'); ylabel('Capacitor Voltage (V)');
grid on
```

boost_mod_sim.m

```
%-------------------------------------------------------------------------
% Determine modified boost state variable and capacitor current waveforms
% using the boost_mod_cycle function. Measure relevant waveform
% characteristics and plot each set of inductor currents, capacitor
% voltages, and capacitor currents.
%-------------------------------------------------------------------------

%-- Operational Converter Parameters ---------------------------------------

Vin = 6;
Vout = 20;
Pout = 30;
f = 200E3;

%-- Calculate Remaining Operational Parameters -----------------------------

Iin = Pout/Vin;
D = -(Vin-Vout)/Vout;
T = 1/f;
R = (Vout^2)/Pout;

%-- Design Component Values ------------------------------------------------

L = 5E-6;
C1 = 30E-6;
C2 = 50E-6;

%-- Solve State Equation and Separate Waveforms ----------------------------

[m, sol, ic] = boost_mod_cycle(Vin,Vout,Iin,T,D,R,L,L,C1,C2);
il1 = sol(:,1);
il2 = sol(:,2);
vc1 = sol(:,3);
vc2 = sol(:,4);
ic1 = ic(:,1);
ic2 = ic(:,2);
```

```
%-- Measure Waveform Characteristics -------------------------------------

state_avg = [mean(il1) mean(il2) mean(vc1) mean(vc2) mean(ic1) mean(ic2)];
state_rms = [root_mean_sq(il1) root_mean_sq(il2) root_mean_sq(vc1)
root_mean_sq(vc2) root_mean_sq(ic1) root_mean_sq(ic2)];
state_rms_ac = [root_mean_sq(il1-mean(il1)) root_mean_sq(il2-mean(il2))
root_mean_sq(vc1-mean(vc1)) root_mean_sq(vc2-mean(vc2)) root_mean_sq(ic1-
mean(ic1)) root_mean_sq(ic2-mean(ic2))];
state_max = [max(il1) max(il2) max(vc1) max(vc2) max(ic1) max(ic2)];
state_min = [min(il1) min(il2) min(vc1) min(vc2) min(ic1) min(ic2)];
state_ripple = state_max - state_min;
state_ripple_percent = state_ripple./abs(state_avg)*100;

%-- Tabulate Waveform Measurements ---------------------------------------

L1Current = [state_avg(1);
             state_rms(1);
             state_rms_ac(1);
             state_max(1);
             state_min(1);
             state_ripple(1);
             state_ripple_percent(1)];
L2Current = [state_avg(2);
             state_rms(2);
             state_rms_ac(2);
             state_max(2);
             state_min(2);
             state_ripple(2);
             state_ripple_percent(2)];
C1Voltage = [state_avg(3);
             state_rms(3);
             state_rms_ac(3);
             state_max(3);
             state_min(3);
             state_ripple(3);
             state_ripple_percent(3)];
C2Voltage = [state_avg(4);
             state_rms(4);
             state_rms_ac(4);
             state_max(4);
             state_min(4);
             state_ripple(4);
             state_ripple_percent(4)];
C1Current = [state_avg(5);
             state_rms(5);
             state_rms_ac(5);
             state_max(5);
             state_min(5);
             state_ripple(5);
             0];
C2Current = [state_avg(6);
             state_rms(6);
             state_rms_ac(6);
             state_max(6);
             state_min(6);
             state_ripple(6);
             0];
Measures = {'Average','RMS','AC RMS','Max','Min','Ripple','Percent Ripple'};
tab =
table(L1Current,L2Current,C1Voltage,C2Voltage,C1Current,C2Current,'RowNames',Measu
res)

%-- Plot Waveform Pairs --------------------------------------------------

figure
subplot(2,1,1)
plot(m,il1); xlabel('m'); ylabel('L1 Current (A)');
grid on
subplot(2,1,2)
plot(m,il2); xlabel('m'); ylabel('L2 Current (A)');
grid on

figure
subplot(2,1,1)
```

```
plot(m,vc1); xlabel('m'); ylabel('C1 Voltage (V)');
grid on
subplot(2,1,2)
plot(m,vc2); xlabel('m'); ylabel('C2 Voltage (V)');
grid on

figure
subplot(2,1,1)
plot(m,ic1); xlabel('m'); ylabel('C1 Current (A)');
grid on
subplot(2,1,2)
plot(m,ic2); xlabel('m'); ylabel('C2 Current (A)');
grid on
```

B. Design Simulation Data

Matlab

Table B-1 lists the complete Matlab standard boost design simulation measurement set.

Table B-1. Matlab-simulated Standard Boost Design Measurements

	Inductor Current (A)	Capacitor Voltage (V)
Average	4.9591	19.998
RMS	4.997	19.998
AC RMS	0.6139	0.0307
Max.	6.0215	20.048
Min.	3.9215	19.943
Peak-Peak	2.1	0.105
%Ripple	42.346%	0.5249%

Table B-2 lists the complete Matlab modified boost design simulation measurement set.

Table B-2. Matlab-Simulated Modified Boost Design Measurements

	L_1 Current	L_2 Current	C_1 Voltage	C_2 Voltage	C_1 Current	C_2 Current
Average	4.9446 A	5.0384 A	-14.032 V	20.012 V	-0.0938 A	0.8794 A
RMS	4.9446 A	5.1876 A	14.032 V	20.012 V	1.2429 A	2.8323 A
AC RMS	0.0096 A	1.2353 A	0.0375 V	0.0359 V	1.2429 A	2.6923 A
Max.	4.9575 A	7.1709 A	-13.976 V	20.061 V	2.0075 A	3.4575 A
Min.	4.9289 A	2.95 A	-14.075 V	19.945 V	-2.2343 A	-3.7343 A
Peak-Peak	0.0286 A	4.2209 A	0.0993 V	0.1162 V	4.2418 A	7.1918 A
%Ripple	0.5778%	83.77%	0.7078%	0.5807%	N/A	N/A

LTSpice

Table B-3 lists the complete LTSpice standard boost design simulation measurement set.

Table B-3. LTSpice Standard Boost Design Measurements

	Inductor Current (A)	Capacitor Voltage (V)
Average	4.9627	19.839
RMS	4.999	19.839
Max.	6.004	19.892
Min.	3.921	19.787
Peak-Peak	2.0827	0.1042
%Ripple	41.967%	0.5252%

Table B-4 lists the complete LTSpice modified boost design simulation measurement set.

Table B-4. LTSpice Modified Boost Design Measurements

	L_1 Current	L_2 Current	C_1 Voltage	C_2 Voltage	C_1 Current	C_2 Current
Average	5.0188 A	5.0183 A	-13.999 V	19.993 V	523 µA	50 µA
RMS	5.0188 A	5.1638 A	13.999 V	19.993 V	1.2242 A	2.5308 A
Max.	5.0425 A	7.1121 A	-13.913 V	20.032 V	2.1349 A	3.5427 A
Min.	4.9982 A	2.9023 A	-14.127 V	19.234 V	-2.0914 A	-3.5861 A
Peak-Peak	0.0444 A	4.2098 A	0.2134 V	0.1084 V	4.2263 A	7.1288 A
%Ripple	0.8847%	83.889%	1.5244%	0.5422%	N/A	N/A

C. Control Loop Compensation

Recommended loop compensation places the crossover frequency (C-1) approximately a decade below the boost converter's right-half-plane (RHP) zero [38].

$$f_c \approx \frac{f_{z-RHP}}{10} \qquad (C-1)$$

A RHP zero (C-2) results from the separation of the inductor and load during the boost converter's switch-on state [38]. The standard boost design's control transfer function contains a RHP zero at approximately 19.1 kHz. The compensator places the crossover frequency around 2 kHz.

$$f_{z-RHP} = \frac{R\left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi \cdot L} \qquad (C-2)$$

$$f_{z-RHP} = \frac{(13.333\ \Omega)\left(\frac{6\ V}{20\ V}\right)^2}{2\pi \cdot (10\ \mu H)} \approx 19.1\ kHz$$

$$f_c \approx \frac{19.1\ kHz}{10} \approx 2\ kHz$$

The type-I compensator design adds a pole and a zero to the control-to-output transfer function. The compensation capacitor and the error amplifier's output resistance, given as 50 kΩ, place the compensator pole (C-3) approximately two decades below the crossover frequency [38]. The compensation capacitor and resistor place the compensator zero (C-4) near the crossover frequency [38].

$$f_{p-comp} = \frac{1}{2\pi \cdot C_{comp} R_{out}} \approx \frac{f_c}{100} \qquad (C-3)$$

$$f_{z-comp} = \frac{1}{2\pi \cdot C_{comp} R_{comp}} \approx f_c \qquad (C-4)$$

The standard component values 150 nF and 536 Ω provide appropriate compensator pole and zero locations.

$$f_{p-comp} = \frac{1}{2\pi \cdot (150\ nF)(50\ k\Omega)} = 21.22\ Hz$$

$$f_{z-comp} = \frac{1}{2\pi \cdot (150\ nF)(536\ \Omega)} = 1.979\ kHz$$

D. Hardware Documentation

Eagle CAD Schematics

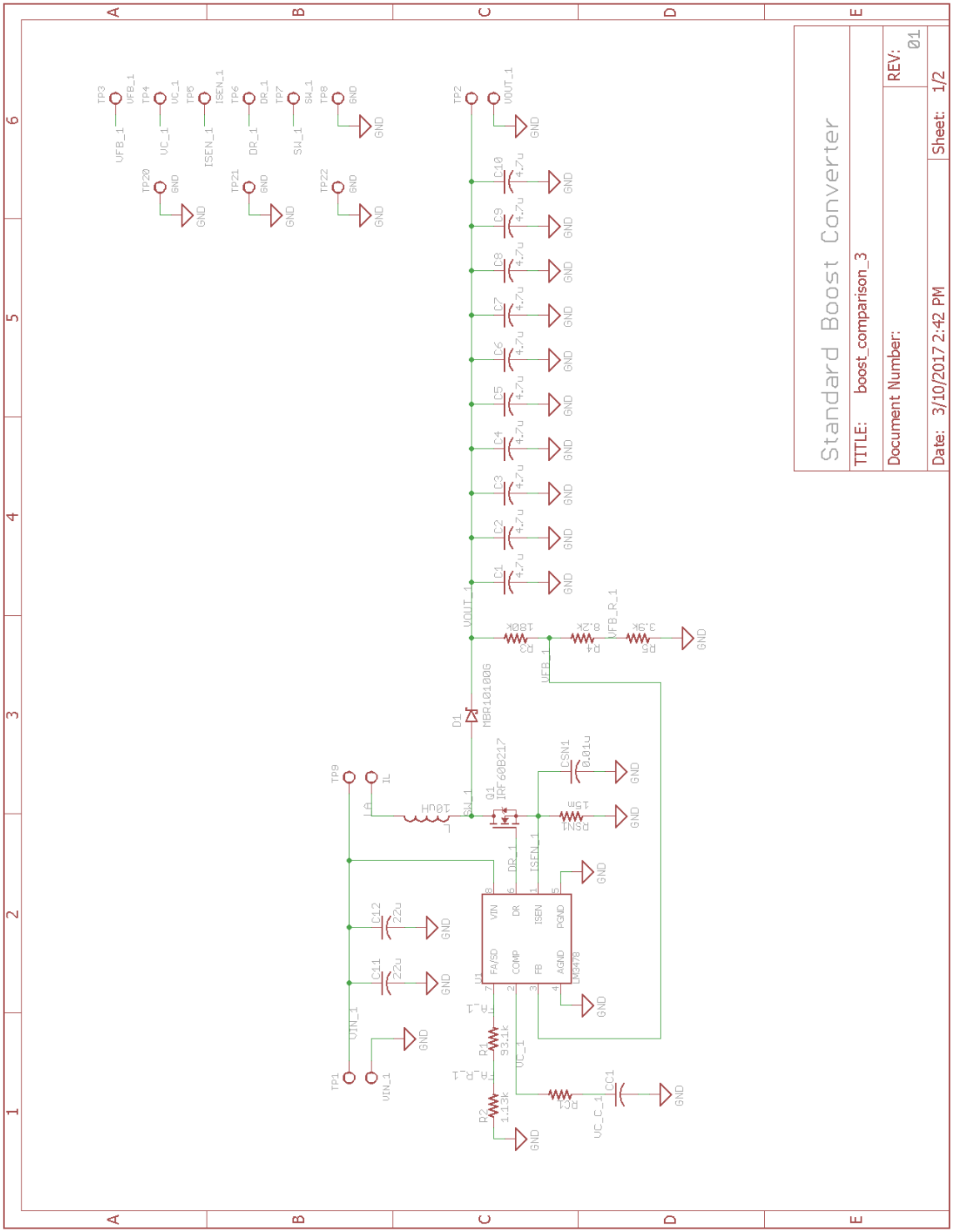

Figure D-1. Standard Boost Converter Eagle CAD Schematic

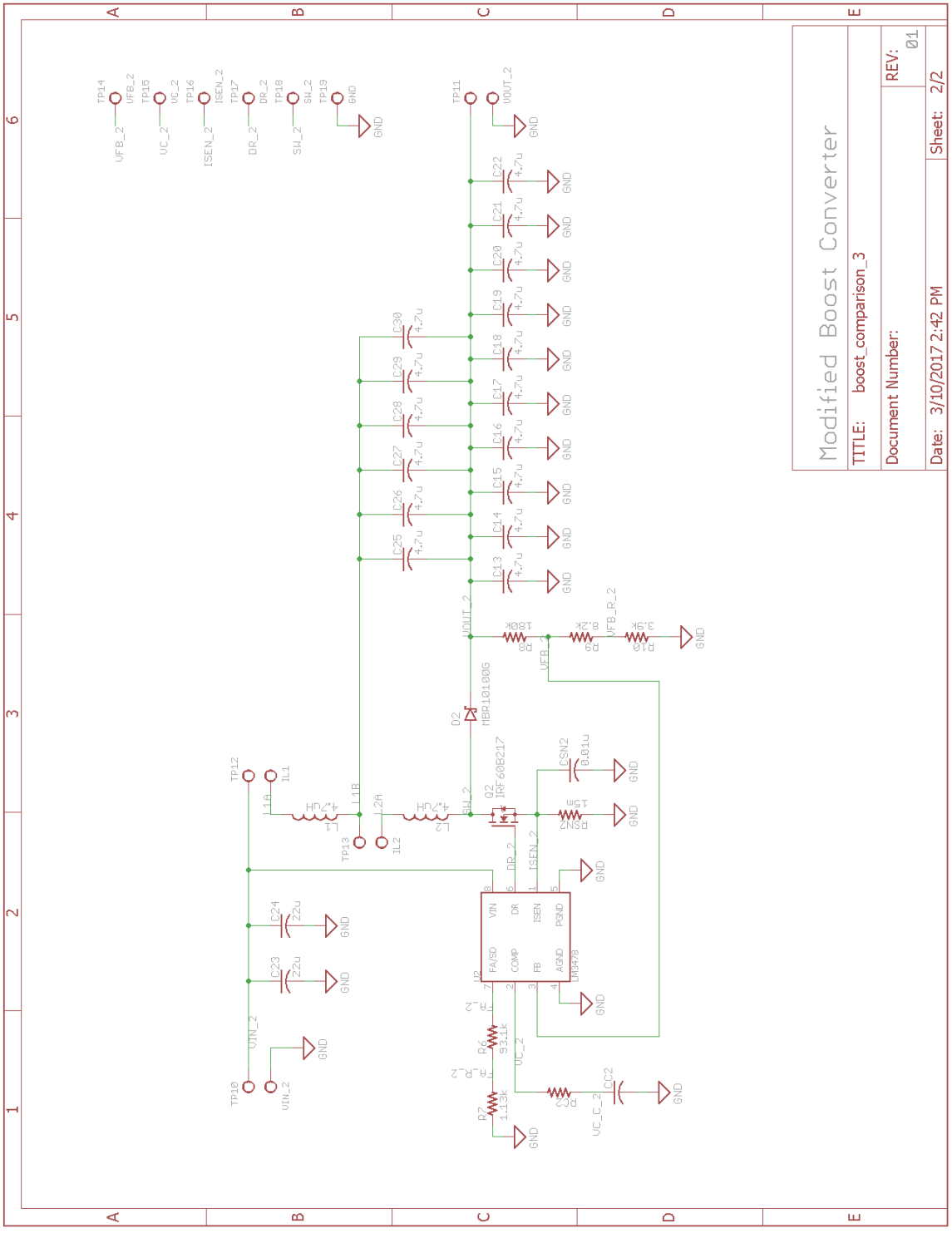

Figure D-2. Modified Boost Converter Eagle CAD Schematic

Eagle CAD PCB Layout

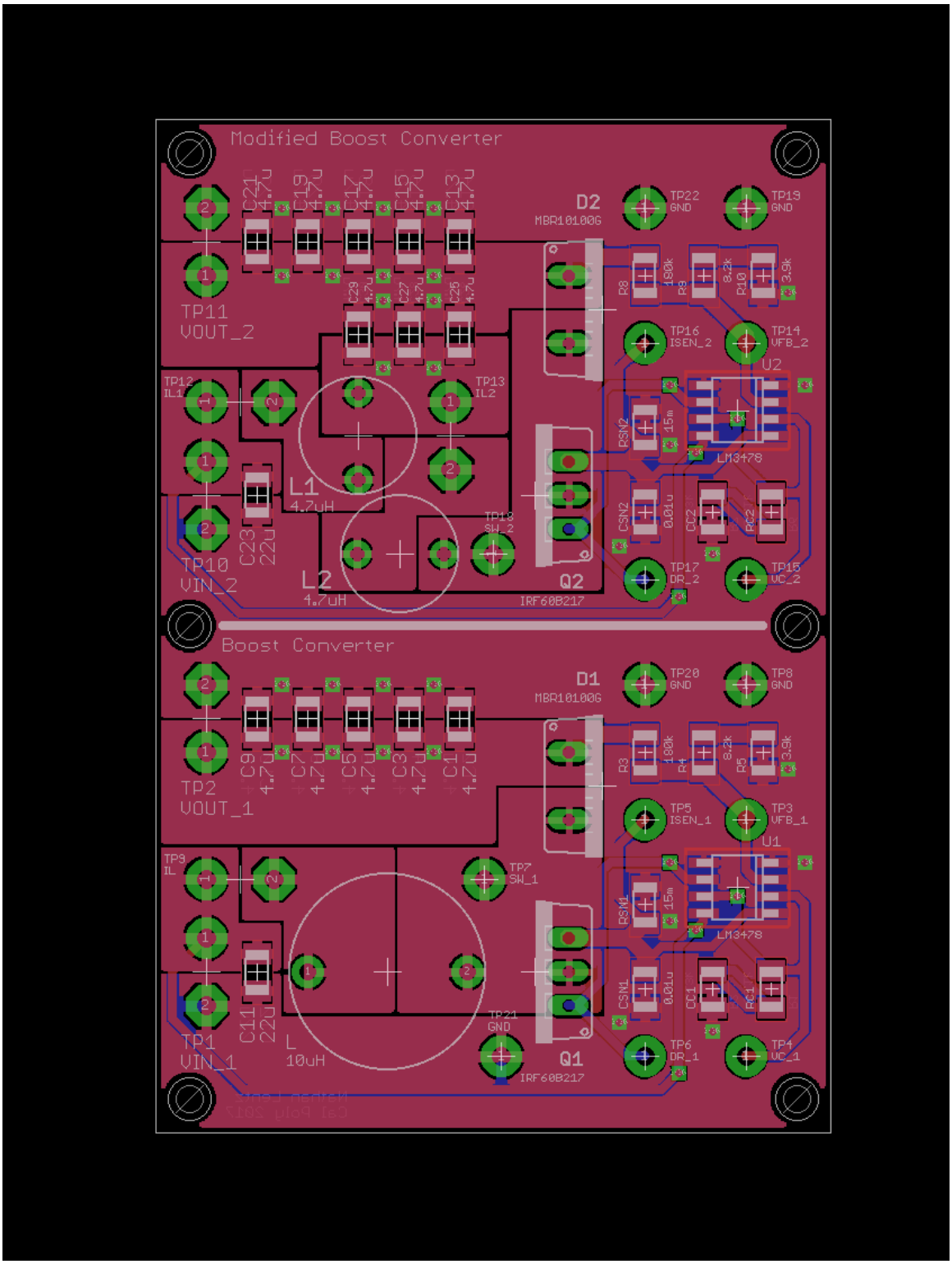

Figure D-3. Eagle CAD PCB Layout

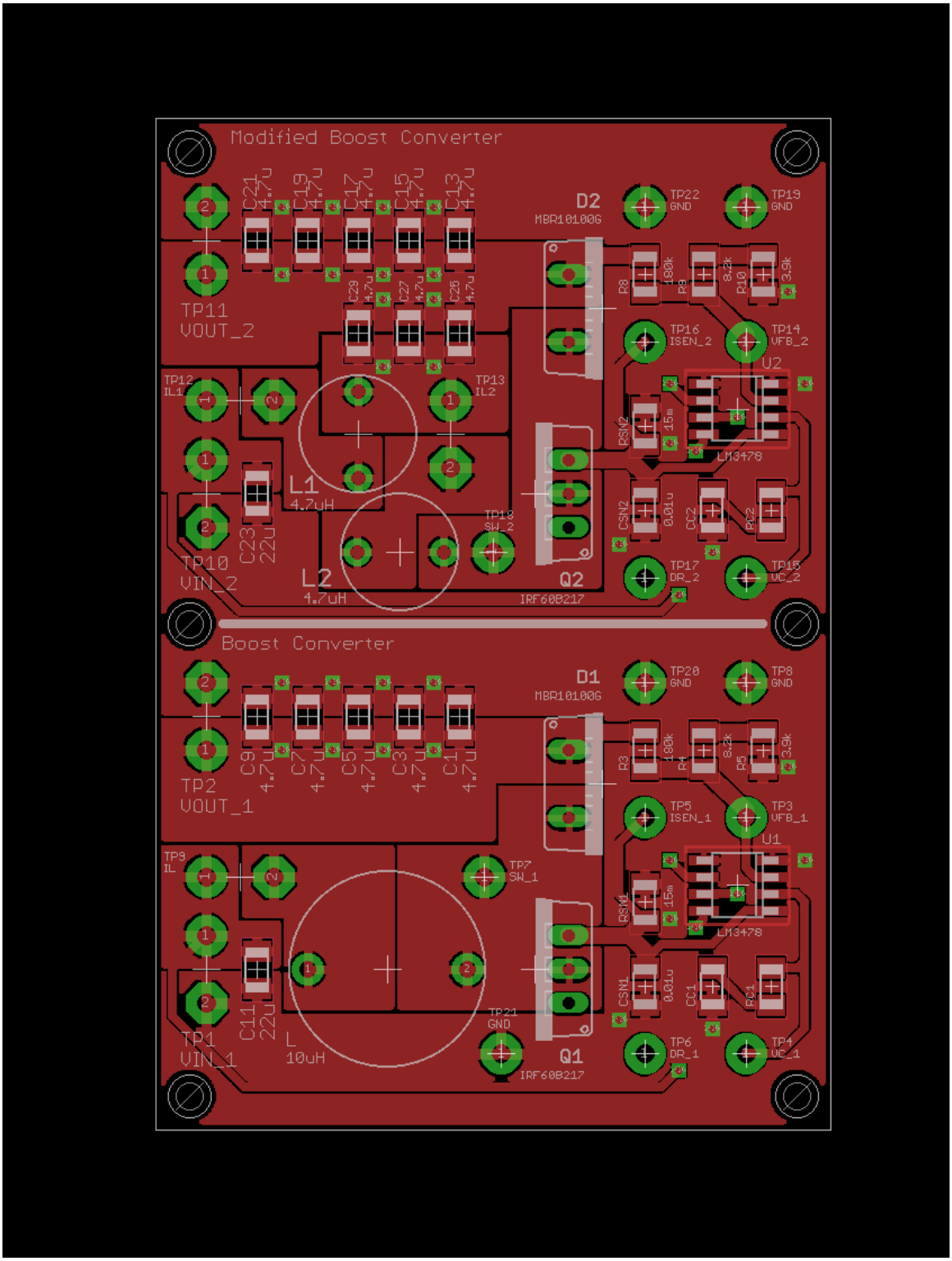

Figure D-4. Top PCB Layer

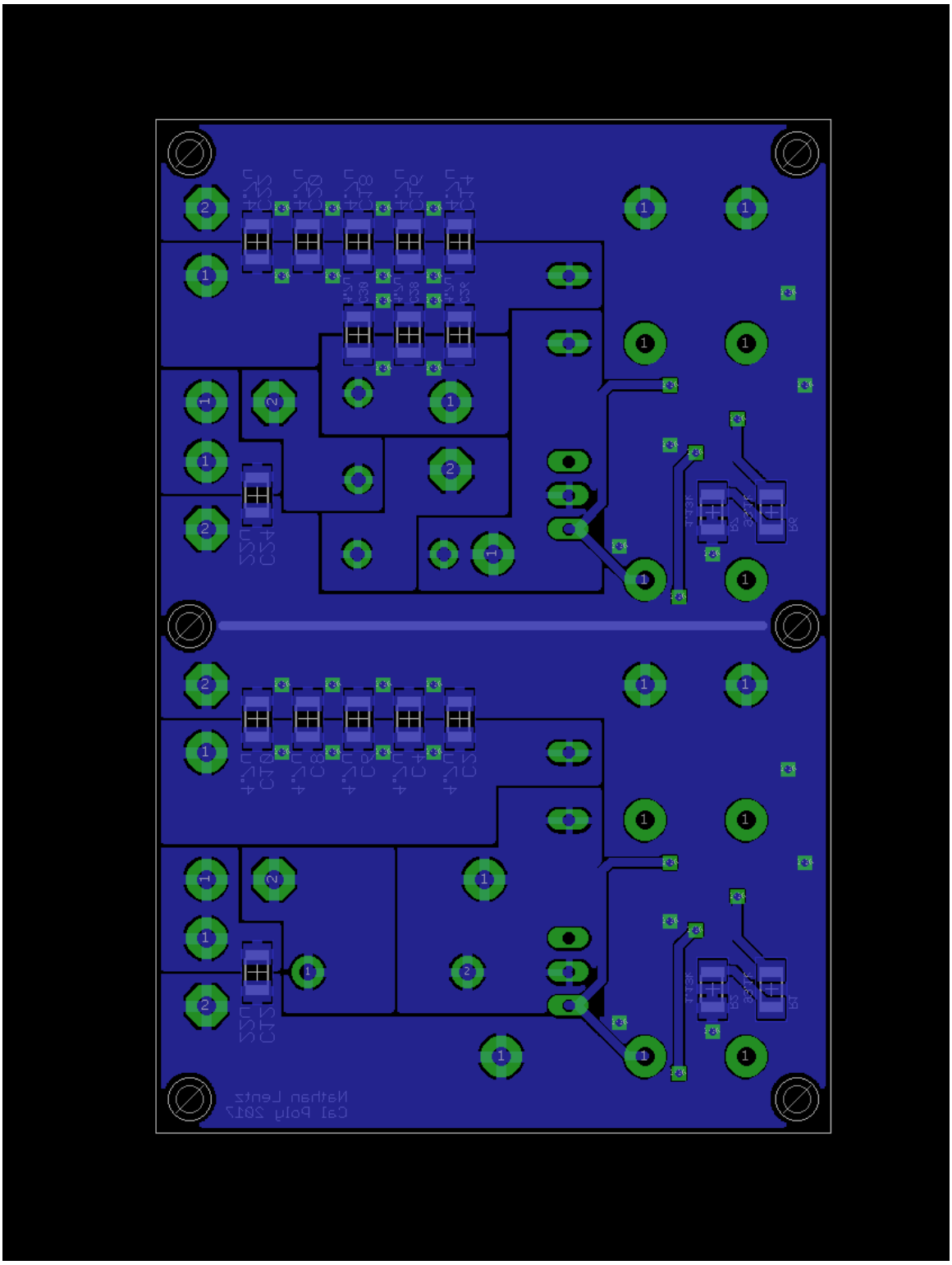

Figure D-5. Bottom PCB Layer

Bill of Materials

Table D-5. Electrical Bill of Materials

Eagle Ref. Des.	Description	Qty.	Mfg.	Part No.
RSN1-2	15mΩ SMD 1206 1% 250mW	2	Vishay	WSL1206R0150FEA
R1, R6	93.1kΩ SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF9312V
R2, R7	1.13kΩ SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF1131V
R3, R8	180kΩ SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF1803V
R4, R9	8.2kΩ SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF8201V
R5, R10	3.9kΩ SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF3901V
RC1-2	536Ω SMD 1206 1% 250mW	2	Panasonic	ERJ-8ENF5360V
CC1-2	0.15uF SMD 1206 100VDC 10% X7R	2	Murata	GRM31MR72A154KA1L
C11-12, C23-24	22uF SMD 1206 10VDC 20% X7R	4	Murata	GRM31CR71A226ME5L
CSN1-2	0.01uF SMD 1206 25VDC 5% X7R	2	Kemet	C1206C103J3RAUTO
C1-10, C13-24, C25-30	4.7uF SMD 1206 25VDC 10% X7R	26	Murata	GRM31CR71E475KA88
L	10uH 8.9A 12.4Asat 8mOhm 20%	1	Wuerth	744750530100
L1-2	4.7uH 6.5A 9.6Asat 4.1mOhm 20%	2	Wuerth	744750230047
Q1-2	NMOS TO220 60V 60A 7.3mOhm	2	Infineon	IRF60B217
D1-2	Schottky TO220-2 10A 100V	2	ON Semi	MBR10100G
U1-2	Low Side N-Channel Controller	2	TI	LM3478MM/NOPB
TP1-2, TP10-11	Red Test Point	4	Keystone	5000
TP1-2, TP8, TP10-11, TP19-22	Black Test Point	9	Keystone	5001
TP3-7, TP14-18	White Test Point	10	Keystone	5002