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Spatio-Temporal Pattern Recognition in Neural Circuits with Memory-Transistor-Driven Memristive Synapses

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Abstract—Spiking neural circuits have been designed in which the memristive synapses exhibit spike timing-dependent plasticity (STDP). STDP is a learning mechanism where synaptic weight (the strength of the connection between two neurons) depends on the timing of pre-and post-synaptic action potentials. A known capability of networks with STDP is detection of simultaneously recurring patterns within the population of afferent neurons. This work uses SPICE (simulation program with integrated circuit emphasis) to demonstrate the spatio-temporal pattern recognition (STPR) effect in networks with 25 afferent neurons. The neuron circuits are the leaky integrate-and-fire (I&F) type and implemented using extensively validated ambipolar nanocrystalline silicon (nc-Si) thin-film transistors (TFT) models. Ideal memristor synapses are driven by a nanoparticle memory thin-film transistor (np-TFT) with a short retention time attached to each neuron circuit output. This device serves to temporally modulate the conductance path from post-synaptic neurons, providing rate-based and timing-dependent learning. With this configuration, the use of a crossbar structures would also be possible, providing dense synaptic connections and potentially reduced energy consumption.

Keywords—neuromorphic circuits; memristor; spike timing-dependent plasticity (STDP); spatio-temporal pattern recognition

I. INTRODUCTION

Synaptic learning in biological systems depends not only on the firing rates of the pre- and post-synaptic neurons, but also on the precise timing difference between action potentials [1]–[3]. This spike timing-dependent plasticity (STDP) is known to be responsible for certain abilities observed across many animal species, including rapid response to threat stimuli and sound source localization [4]–[8]. Networks with STDP learning also have the ability to perform feature extraction and can learn to recognize and classify recurring temporal patterns and sequences [9]–[15]. Because these patterns may only occur in a subset of a given neuron’s afferents (located at different points in space), it is referred to as spatio-temporal pattern recognition (STPR) [16]–[18]. The focus of this work is using simulation of larger networks with STDP learning to demonstrate their ability to perform STPR without supervision. All neuron circuits use normal rectangular action potentials and operate on timescales similar to those observed in biology.

A diagram of the system connections used in this work is shown in Figure 1. In a typical application, analog input current signals would be applied to the input layer of neurons. These neurons would then initiate action potentials whenever the voltage at the input node to the circuit reached the specified firing threshold. That output pulse is then applied to the gate and drain of a memory transistor (np-TFT) which drives current through the axonic memristive synapses to stimulate the post-synaptic neuron. Whenever that pre-synaptic pulse is applied to the device, charge is also trapped in the nanoparticle layer, which shifts the device threshold voltage and keep the channel partially active for some amount of time. In this implementation, the charge is released from the traps such that the threshold voltage decays exponentially over a time scale of approximately 100 ms. If a post-synaptic spike occurs during this time, a depressive voltage pulse is sent in the reverse direction. The amount of reverse current that subsequently flows through the memristive synapse depends on how long it has been since occurrence of the pre-synaptic action potential [19]–[21]. Consequently, the system performs STDP.

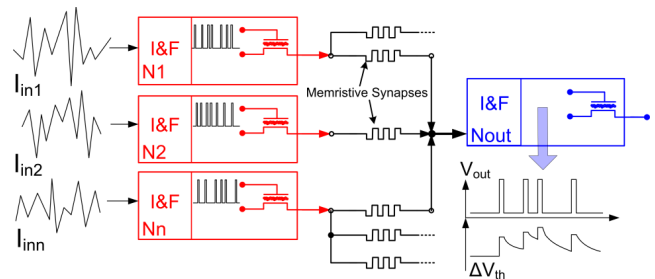


Figure 1. Illustration of the system connections in a typical network simulation. Analog input signals cause the leaky integrate-and-fire (I&F) input neurons to spike and inject current through the axonic memristors using the short-term memory transistors (np-TFTs). The short-term memory transistor both stimulates post-synaptic neurons (via memristive synapses) and provides time modulation of the reverse current conductance path. Plots at bottom right show the effect of higher frequency action potentials on the memory device and how the threshold voltage continues to shift with rapid firing.

In the network simulations, afferent neurons are set to fire at a certain rate with Poisson-distributed inter-spike intervals (ISIs). Periodically, the afferents leave the random mode for 100 ms and present their unique pattern. These recurring patterns are the same each time for individual neurons, but

different among the afferents. During the 60 second transient simulation, the networks learn to recognize when the patterns occur by appropriately adjusting the synaptic weights via STDP. This effect is observed via firing of the single output neuron. At first, the output neuron responds randomly to the input spike trains and is not selective to the recurring patterns with relatively higher firing rate. After time (or a certain number of pattern presentations), the output responds only during pattern presentations, with only occasional false positives.

The following section provides details of the individual device operation and models for the nc-Si TFTs, np-TFTs, and memristors. Section III then describes the circuit and network configuration and control parameters used in a simulation of STPR. The networks simulation results are analyzed further in Section IV. Accuracy and false positive rate are examined, as well as afferent neuron firing rate averages to illustrate the effects are not due solely to high population firing rate at the time of pattern presentation. Finally, conclusions and future work are discussed in Section V.

II. DEVICE MODELS

All of the device models used in this work have been described in detail previously. The most important behavioral aspects will be repeated in this section, beginning with the submicron ambipolar nc-Si TFTs which comprise the leaky I&F neuron circuits. The SPICE models for these devices have been thoroughly vetted using measured data [22], [23]. They are then connected into the spiking neuron circuit configuration shown in Figure 2, which is a modified version of that originally proposed by Mead [24]. Previous work used models of similar ambipolar devices to show the potential for their use in neuron circuits [25], [26]. However, the device models and subsequent neuron circuit behavior were also verified through fabrication and testing [27]. Current work involves design, simulation, fabrication, and testing of various CMOS I&F neuron designs [28]–[31]. These circuits will be more compact, robust, tunable, and require less power than those using nc-Si TFTs.

The circuit parameters used for all subsequent simulations are listed in Table 1 and correspond to the Figure 2 schematic. In some cases, the voltage values listed are fairly large, again because of the use of TFTs with operating points very different from silicon CMOS devices. Slightly larger voltages are also required to appropriately charge up the memory transistors, as described in the next section. In particular, the typical 5 V output pulses are assumed to be modified as follows: at the same time a given neuron circuit produces an action potential, the gate voltage V_{pg} applied to the np-TFT is 7.5 V and the drain voltage V_{inj} is 2.25 V. When the neuron circuit is not firing, these voltages are zero. Additional voltages V_{lk} and V_{rst} separately control the path for removal of charge from the membrane capacitor C1. Leakage when the neuron is not firing is determined by V_{lk} , whereas V_{rst} essentially controls the action potential width, which is 1 ms. During an action potential, capacitor C1 is also isolated from the input synapses by a transistor to avoid pulse width fluctuations due to differing amounts of excitation. The depression voltage V_{dep} is

simultaneously applied to the reverse conduction path through the memristors.

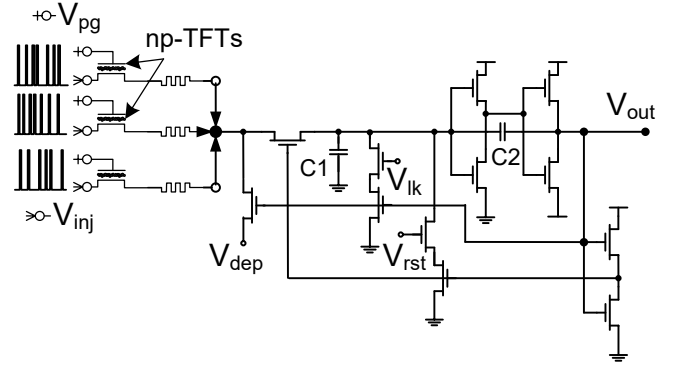


Figure 2. Schematic of the leaky I&F neuron circuit using submicron ambipolar nc-Si TFTs. A third inverter must be added to compensate for poor gain and transfer curve characteristics. Extra transistors and voltage modifications are not expected to be necessary in CMOS implementations.

Table 1. Circuit parameters used for all simulations (as labeled in Figure 2).

Parameter	Value	Description
V_{dep}	8 V	Controls amount of synaptic depression
V_{lk}	1.3 V	Sets current leakage during non-firing
V_{rst}	2.4 V	Sets reset current and thus pulse width
C1	20 pF	Membrane capacitance that integrates the input currents
C2	12 pF	Positive feedback capacitance
V_{out}	-0.25 or 5 V	Neuron circuit output
V_{inj}	0 or 2.25 V	Drain voltage on np-TFT during spike
V_{pg}	0 or 7.5 V	Gate voltage on np-TFT during spike

A. Memory Transistors

In one sense, the purpose of a drive transistor at the neuron output is to inject current through the axonic synapses without requiring that current to be provided by the output inverter. A device with larger channel width can be used to deliver more total current. The np-TFTs used here perform that duty, but also act as an intermediary between the spiking neurons and axonic synapses that controls current flow. In other words, addition of the memory function serves to modulate the conductance of the current path through the synapse in a manner that depends on the firing of the neuron. Current is injected toward the synapses when the neuron fires, and electrons are also drawn into the nanoparticles in the insulator, shifting the device threshold voltage. Over time, the charge leaks back into the channel and the threshold voltage returns to the resting value. If a post-synaptic action potential occurs while a significant amount of charge is still trapped, reverse current flows through the memristor (when V_{dep} is applied by the post-synaptic neuron) because the channel of the np-TFT remains partially on.

Short-term memory effects can be realized in a typical TFT device through the incorporation of a metal nanoparticle layer inside the gate dielectric. The overall fabrication process is very similar to that of the ambipolar nc-Si TFTs, the only difference being that deposition of the gate dielectric is halted part way through. At this step, the dielectric surface is chemically sensitized to enable gold nanoparticle attachment. Resulting nanoparticle coverage is highly uniform with this approach, and the process can be optimized to obtain nanoparticle density that

results in the desired amount of charge trapping. From this step, the remainder of the dielectric layer can be deposited. Different thicknesses of dielectric above and below the nanoparticle layer can be used to modify the programming voltage and retention time. Use of different metals other than gold and smaller nanoparticle size distributions may alter the properties as well. Organic and amorphous silicon TFTs with similar characteristics have also been demonstrated [32]–[34].

Behaviorally, the device operates identically to nc-Si TFTs without a nanoparticle layer when gate voltage is low (<1 V). Programming the device can be accomplished by applying gate voltage of larger magnitudes. At higher electric fields, the gate currents are sufficient to result in the trapping of charge and an associated threshold voltage shift. The shifts were measured in a fabricated device using a programming voltage pulse applied to the gate for 1 ms with subsequent examination of the transient drain current decay. The SPICE model parameters were then tuned to fit the measured data. The amount of trapped charge is calculated assuming Fowler-Nordheim (F-N) tunneling of electrons through the gate insulator with a trapping coefficient of 10%. While the np-TFT SPICE model is also capable of capturing Poole-Frenkel conduction or any combination of the two mechanisms, the F-N model provided the best fit to both transient and DC gate current measurements. The resulting np-TFT model is only valid for total oxide thickness that is the same as the measured TFT, and it cannot directly be scaled for situations with different programming pulse magnitudes. Again, thinner oxides with optimized geometry and trapping layer location are capable of achieving much lower voltage operation.

B. Memristive Devices

At the core, memristors are the most important elements in this neuromorphic system since they are used as the synapses. Their switching behavior essentially dictates both the design and voltage outputs of the neuron circuits, as well as the retention requirements of the memory transistor. Digital memory applications are concerned with fast operation and having only a few stable device states whose conductance is different enough to be easily distinguished by readout circuitry. On the other hand, synapses for most typical neuromorphic systems should have a larger number of conductance states that are closely spaced and change very little with successive stimulation. An infinite number of states is not required since biological synaptic weights are actually also quantized (they are based on the integer number of neurotransmitter-containing vesicles in the synaptic cleft) [35]. For this approach, the most important trait is that devices should be bipolar and capable of changing resistance incrementally in both positive and negative directions.

An ideal memristor based on the variable resistor model presented by Strukov et al. is used in this work [36], [37]. The devices are presumed to have active layer thickness of D , and the boundary of the ‘doped’ region of higher conductance has instantaneous position w . Thus, the ratio w/D is referred to as the state variable, and can change only between zero (when the device is in the high resistance state R_{off}) and one (device in the low resistance state R_{on}). In all the simulations, $R_{\text{off}}=50$ M Ω and

$R_{\text{on}}=1$ M Ω , while the device active layer thickness is $D=10$ nm and the dopant mobility is set to 200×10^{-15} m²/V-s.

The behavior of this memristor model can be illustrated by SPICE simulation using rectangular applied voltage pulses as shown in Figure 3a. Each pulse has duration 1 ms (similar to an action potential), but different magnitudes. The resulting memristor state variable w/D (proportional to instantaneous conductance) is plotted in Figure 3b, and the steps are bigger for the pulses of larger magnitude. Although ideal memristors are difficult to realize in practice, there are many different material systems and device structures that are close approximations. One of the main advantages of this network design is that circuit parameters are tunable to deal with asymmetric weight changes in non-linear devices [38]. Specifically, tuning can be accomplished by changing the injection voltage V_{inj} on the drain of the np-TFT (see Table 1) as well as the value of the feedback voltage pulse V_{dep} .

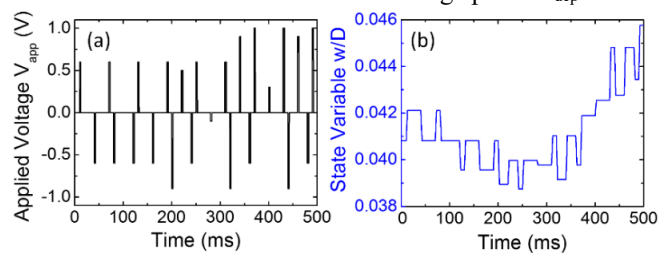


Figure 3. (a) Applied voltage pulses with varying height but constant 1 ms width being applied to the ideal memristor SPICE model. (b) Change in memristor state variable versus time for the voltage pulses shown.

III. TRANSIENT NETWORK SIMULATION

To demonstrate STPR, a network containing 25 afferent neuron circuits feeding one output neuron via np-TFT driven memristive synapses was connected in SPICE as in Figure 1. For the purpose of reducing compute times, signals representing the responses of the afferent neurons to temporal signals embedded in Gaussian white noise are applied directly to np-TFTs, instead of including the full afferent neuron circuits. This is accomplished with piecewise-linear (PWL) functions which closely approximate the spike trains generated by neuron circuits. The PWL functions have action potentials that occur randomly (generated by a Poisson process), except during the presentation of patterns. Each neuron’s pattern is also generated by a Poisson process with the same ISI distribution such that the average firing rate of a neuron does not change due to a pattern. Figure 4 is a scatter plot of output neuron and all 25 afferent firing times. Temporal pattern occurrences are highlighted. At first, N_{out} fires randomly, even in response to the patterns randomly embedded in the noise which start three seconds into the simulation (Figure 4a). After repeated exposure, firing of N_{out} starts to coincide with the pattern presentations (Figure 4b). In this time frame of roughly 3.5 seconds starting at 37 seconds into the simulation, the network successfully detects all 13 presented patterns with only two false positives, indicated by red arrows near the time axis.

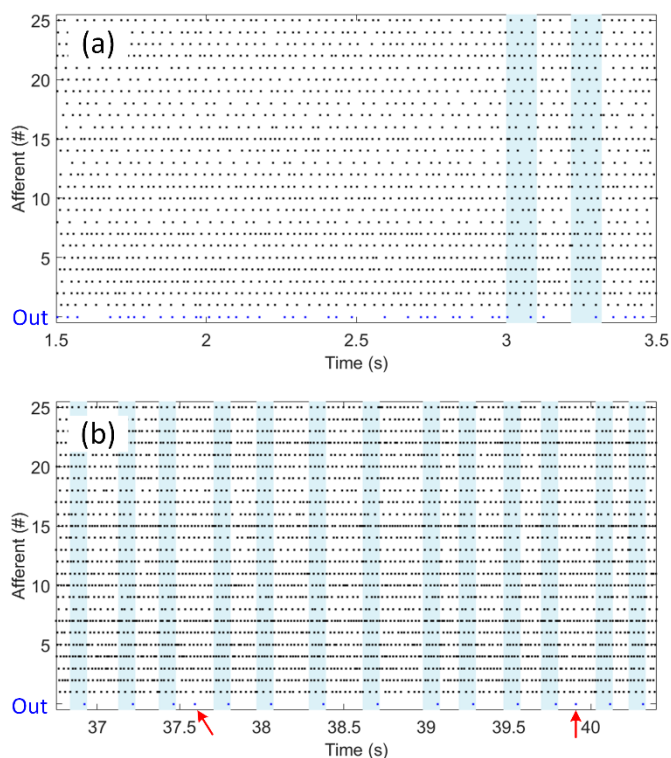


Figure 4. Simulation A demonstrates learned recognition of spatio-temporal patterns in a 25-neuron network. (a) Initially, the output neuron fires randomly and is not correlated with pattern presentation. (b) After ~30 to 40 seconds of unsupervised learning, synaptic weights adjust such that the output neuron fires only at the time of pattern presentations, with a few false detections (indicated by arrows). Pattern occurrences are highlighted by the shaded regions, and all afferents in this simulation present patterns.

Temporal evolution of the synaptic weights in the system can also be tracked by the simulation as shown in Figure 5. Initial weights are set randomly in a Gaussian distribution with mean resistance of 25 M Ω ($w/D=0.5$) and standard deviation of 5 M Ω . As the simulation progresses, synapses which are less important in signaling pattern presentations are depressed. This decrease in weight appears to be an approximately exponential decay with time. By the end of the 60 second simulation, essentially only three afferent neurons play a significant role in triggering firing of the output neuron. Additionally, starting at 50 seconds, the average interval between pattern presentations changes from every 300 ms to every 700 ms. When this occurs, the false positive rate increases slightly, and there is also an inflection point in the rate of synaptic weight change. It is unknown at this time whether a longer simulation would result in different final distributions, or how significant a role pattern presentation frequency plays. In part, future work will investigate the dependence of successful pattern recognition on the frequency of pattern presentation. It will also involve increasing the number of afferent neurons, changing the fraction of afferents involved in pattern presentation, and adding timing jitter to the start of patterns as well as to spikes within the patterns.

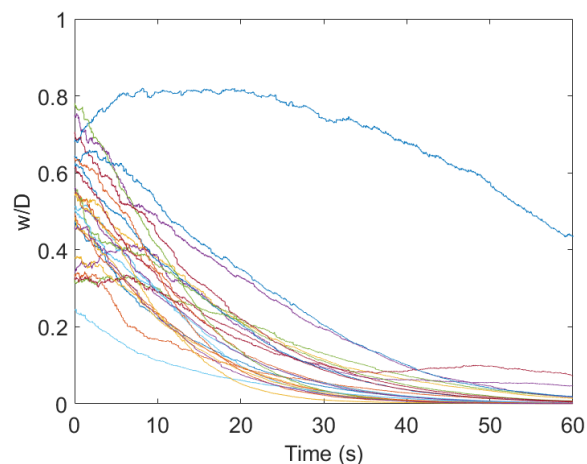


Figure 5. Evolution of all 25 synaptic weights (represented in different colors) versus time in simulation A. This plot helps determine which afferents are most important in triggering the output neuron to recognize the pattern and fire. It also shows the random initialization of the weights centered around an average of $w/D=0.5$, and an inflection point in the rate of synaptic weight change around 50 seconds when the average interval between pattern presentations changes.

To confirm that the network does perform STDP during learning, timing differences between spike pairs and the subsequent weight changes is examined. This is done using the nearest-neighbor spikes between the output and any of the afferent neurons. An example from the simulation is shown in Figure 6 for the synapse connecting neuron 1 and the output. Although the data is very scattered, it clearly demonstrates a strong similarity to pair-based STDP measurements near the origin. Scatter is primarily due to the fact that the calculation considers non-nearest-neighbor spike interactions. In other words, the np-TFT threshold voltage shifts depend on firing rate, and the weight change is not purely pair-based.

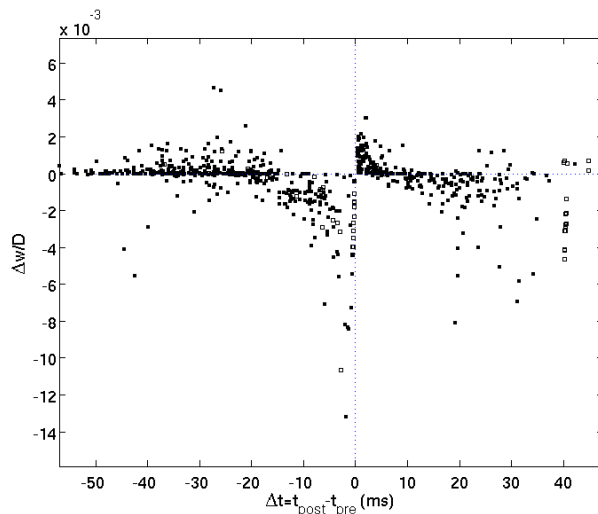


Figure 6. A pair-based STDP curve calculated for the entirety of the simulation. Each point represents the weight change of the synapse connection neuron one and the output due to a single pre-post or post-pre pair. Scatter at larger Δt is likely due to high frequency interactions that have not been removed from the raw data. Open symbols are specifically for action potential pairs that are part of patterns in the afferent neuron 1.

IV. DISCUSSION

Other data collected during the simulation helps explain the operation of these networks. One of the most important metrics may be analysis of the population firing rate of the afferent neurons over the course of the simulation. This helps ensure pattern detection is not due to instantaneous high firing rate (coincidence detection) that could be caused by an error in the simulation code. Figure 7 shows the population firing rate using 10 ms time bins for the course of the simulation, and for a representative sample between four and five seconds (inset). The population average firing rate is approximately 40 Hz, which also matches the average set for each individual afferent.

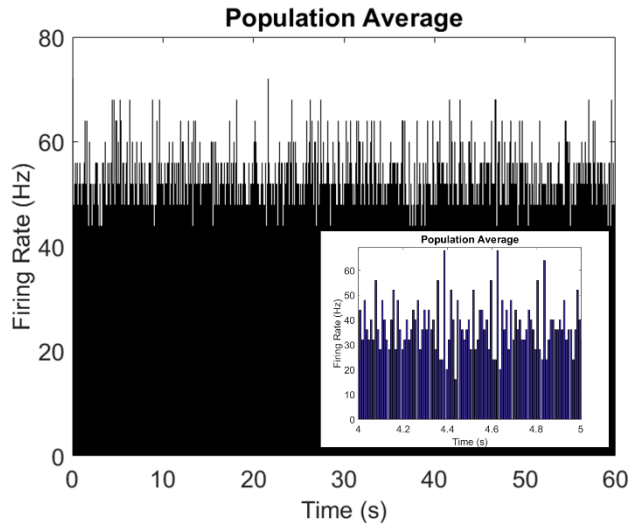


Figure 7. The average firing rate of the population in the simulation can be shown to demonstrate the recognition is not based on coincidence detection or sudden high population firing rates. This is shown here using 10 ms time bins for the entire 60 second simulation time as well as a representative sample between 4 to 5 seconds (inset).

Average firing rates for each afferent neuron and the output have also been calculated to confirm they correspond with the values set in the PWL input files. Specifically, the average firing rate of each afferent was set randomly based on a Gaussian distribution with mean of 40 Hz and standard deviation of 10 Hz. Figure 8 shows the average rates during the first five and last five seconds of the simulation, calculated as the number of firing events in the interval divided by five seconds. Of note is the fact that the firing rates of the afferents are very similar during both time frames, as would be expected based on the firing rate settings. The values for these neurons would look essentially the same if examined over the whole time course of the simulation. In comparison, the output neuron firing rate (labeled as ‘0’ and shown in red) changes dramatically over the course of the simulation. Again, for the final ten seconds, patterns are being presented at a frequency of approximately 1.5 per second. With one spike per pattern, this same firing rate would be expected for the output. However, the slightly higher (~40%) false positive rate causes an apparent average frequency of just over 2 Hz in Figure 8b.

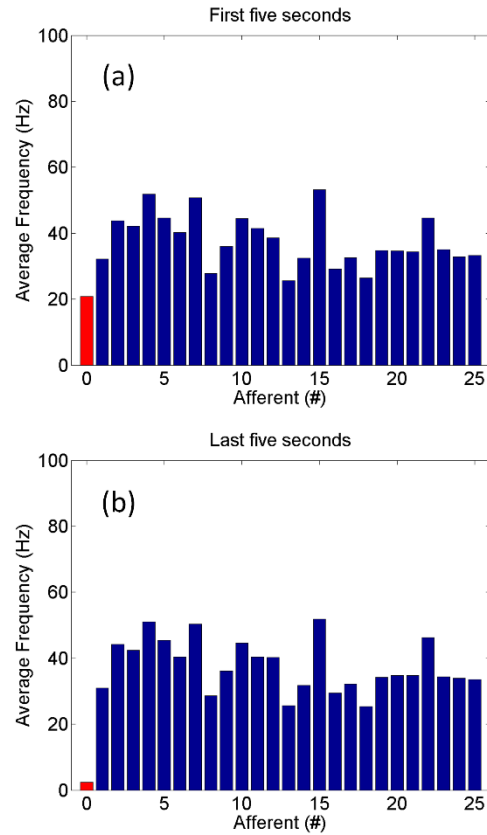


Figure 8. To ensure the system is stable and neuron frequencies are as expected, the average firing rates of the output and each afferent neuron can be plotted at different times. Average firing rates of afferent neurons and the output during the first five seconds of simulation are shown in (a), and the last five seconds in (b).

Finally, multiple simulations must be performed with the same network control parameters to demonstrate the pattern detection capability is not anomalous. Another representative simulation (denoted as ‘B’) was performed to verify that the network parameters in Table 1 would result in successful identification of other random pattern sets. Thus, new PWL input files and initial synaptic weight distributions were generated using the same mean and standard deviation values quoted previously. Figure 9 again shows scatter plots of each firing event occurring during the 60 second transient simulation B. The random firing that occurs at the beginning of the simulation is shown in Figure 9a, and it can be observed that the patterns for each afferent are different in simulation B compared to the example in section III. Figure 9b shows that the network indeed learns to detect the patterns in simulation B, but they are identified by a pair of output spikes (doublet) rather than a single action potential. The pattern detection success rate is again 100% with only a few false positives.

Understanding why patterns are identified by single versus double spikes in different situations will require extensive statistical examination using results from many simulations. Evolution of synaptic weights versus time as well as the final synaptic weight distributions after learning may again provide

key insights. In particular, it is not clear from the results whether synaptic learning is additive (weight change does not depend on actual synaptic weight), or multiplicative (in which learning is a function of the weight) [9], [39], [40]. The latter seems more plausible based on the operation principle of these circuits, in that the conductance of the reverse current path through the memristor certainly depends on the instantaneous weight. However, Figure 10 shows synaptic weight changes for simulation B. Again, a majority of synaptic weights decrease approximately exponentially in time. Several other synapses appear to have key involvement in pattern detection, but in this case one particular synapse is much more important, as its weight saturates to the maximum value of $w/D=1$. This results in a final synaptic weight distribution that is bimodal, and indicative of an additive rule [41]. Other analysis factors such as population firing rate and average firing rates appeared roughly the same in both simulations.

Consequences of numerous other factors on pattern detection success rates must also be examined in the future. One of these is the effect of afferent average firing rates, where one or more neurons with fast spiking frequencies could have a detrimental effect in terms of overstimulating the output. In addition, properties of the memristive synapses such as the R_{off}/R_{on} resistance ratio could have enormous consequences for pattern detection accuracy. On the other hand, limitations in the dynamic range of the memristors could also be mitigated in

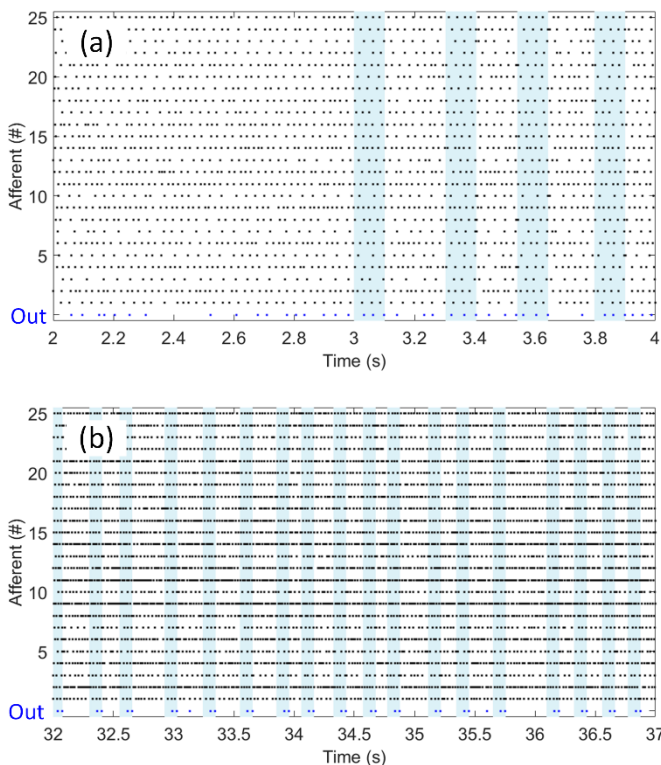


Figure 9. Results of simulation B using the same circuit and network parameters as simulation A, but with different random spikes and patterns as well as different initial synaptic weight distribution. (a) Initially, the output neuron fires randomly and is not correlated with pattern presentation, as expected. However, (b) shows that successful pattern detection in this system is indicated by doublets in contrast to single spikes. The success rate is still 100% with very few false positives.

networks with a very large number of afferents. The total number of afferents as well as the fraction of those actually presenting patterns is also important. In both cases shown in this work, all 25 afferents present patterns with no spike jitter. Additional noise and and/or smaller percentage of afferents presenting patterns are likely to significantly reduce pattern

detection accuracy. Finally, longer simulations should be run to provide estimates of stability with very diverse sets of pattern presentation frequencies and intervals. In an ideal case, the network would learn to detect patterns even if they occur at very irregular and sparse intervals.

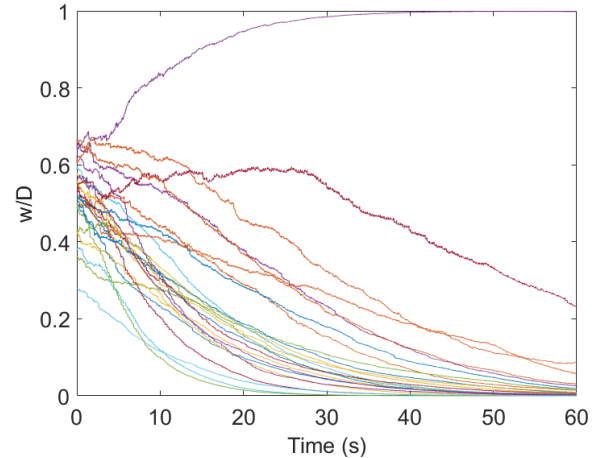


Figure 10. Evolution of all 25 synaptic weights for simulation B. In this case, one neuron (afferent 11) plays an extremely important role in the indication of a pattern and its weight saturates to a value of one.

V. CONCLUSIONS

Since the recent re-emergence of memristive devices, there has been great interest in their use as synapses in neuromorphic electronic systems. This is due to the behavioral similarities shared with biological synapses, as well as the possibility that memristors can achieve synaptic density and energy efficiency of the same order of magnitude as the human brain. This work demonstrates a unique approach to achieving realistic STDP learning rules for systems with memristive synapses. Then, using these rules, it is shown that the system is fundamentally capable of performing STPR even with a relatively small number of afferents. Future work will continue to make the network more efficient and optimize the control parameters to achieve higher pattern detection success rates with fewer false positives. This will require statistical analysis of many simulations using control variables that contribute in many different ways to this relatively complex network behavior.

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