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Effects of Ta incorporation in Y_2O_3 gate dielectric of InGaZnO thin-film transistor

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The effects of Ta incorporation in Y_2O_3 gate dielectric on the electrical characteristics of InGaZnO thin-film transistor are investigated. With an appropriate Ta content in the Y_2O_3 gate dielectric, the saturation mobility of the thin-film transistor can be significantly increased, about three times that of the control sample with Y_2O_3 gate dielectric. Accordingly, the sample with a Ta/Ta+Y ratio of 68.6% presents a high saturation mobility of 33.5 $cm^2\ V^{-1}\ s^{-1}$, low threshold voltage of 2.0 V, large on/off current ratio of 2.8×10^7, and suppressed hysteresis. This can be attributed to the fact that the Ta incorporation can suppress the hygroscopicity of Y_2O_3 and thus reduces the Y_2O_3/InGaZnO interface roughness and also the traps at/near the interface, as supported by atomic force microscopy and low-frequency noise measurement, respectively. However, excessive Ta incorporation in the Y_2O_3 gate dielectric leads to degradation in device performance because Ta-related defects are generated. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4965849]

The amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) own high carrier mobility (>10 $cm^2\ V^{-1}\ s^{-1}$), excellent uniformity of device performance, and low-temperature processing and thus have been intensively investigated for applications in the next-generation active-matrix flat-panel displays, which require fast refresh, high resolution and large panel size.[1,2] In addition, the fabrication process of a-IGZO TFTs is compatible with the present technology employed for the mass production of a-Si TFTs. Currently, the best IGZO devices can do well in active-matrix liquid-crystal displays (AMLCD) and nearly meet the needs of organic light-emitting diode (OLED) displays. However, the high power consumption of a-IGZO TFTs due to high operating voltage and large gate leakage limits their applications, especially in portable devices. Therefore, many researchers have tried to adopt various high-k materials, e.g., Y_2O_3, HfLaO, and $BaSrTiO_3$,[3–5] as the gate dielectric of a-IGZO TFTs in the past few years. Among them, the a-IGZO/Y_2O_3 TFT could present low leakage current, high breakdown voltage and good high-temperature reliability due to both wide band gap (5–6 eV) and excellent thermal stability of Y_2O_3 dielectric.[6,7] However, the Y_2O_3 film is hygroscopic and its k value is relatively low (11–18), which reduces the practical application value of a-IGZO/Y_2O_3 TFT. On the other hand, Ta_2O_5 gate dielectric with a high k value (~29) has been widely adopted in a-IGZO TFTs to reduce the operating voltage.[8–10] More importantly, the Ta_2O_5 film is much less hygroscopic than the Y_2O_3 film. It was reported that Ta incorporation in La_2O_3 gate dielectric could improve the electrical characteristics of IGZO TFT because Ta incorporation could enhance the moisture resistance of the La_2O_3 film and thus decrease the trap density at/near the dielectric/IGZO interface.[11] Therefore, the aim of this work is to investigate the effects of Ta incorporation in Y_2O_3 gate dielectric of IGZO TFT. In detail, Ta incorporation with different doses is tried out to identify the optimal Ta content for the best device performance.

First, the standard RCA method was employed to clean the p-type silicon wafers (⟨100⟩, 0.01–0.02 Ω cm), which acted as both substrate and gate electrode. Then, a gate dielectric film was deposited by sputtering in an Ar/O_2 mixed ambient, with Ta metal target and Y_2O_3 ceramic target under various powers to realize different Ta contents. After that, all the samples were annealed at 400 °C for 10 min in an N_2 ambient with a flow rate of 500 mL/min. Subsequently, a 60-nm IGZO film acting as the channel layer was deposited by sputtering with a ceramic target (Ga_2O_3:In_2O_3:ZnO = 1:1:1) in an Ar/O_2 (24 sccm/1 sccm) mixed ambient. Next, a conventional photolithography and lift-off process were carried out to form the source/drain electrodes with a channel of 100 μm in width (W) and 30 μm in length (L), and the electrodes consisted of 20-nm Ti and 80-nm Au deposited by electron-beam evaporation. At last, all the samples were annealed at 350 °C for 20 min in forming gas (N_2:H_2 = 95:5) to reduce the contact resistance of the source/drain electrodes.

The electrical characteristics of the a-IGZO TFTs were measured by an HP 4145B semiconductor parameter analyzer. In addition, the Al/dielectric/Si metal-insulator-semiconductor (MIS) capacitors were also prepared in order to monitor the gate-oxide capacitance per unit area (C_{ox}) by using an HP 4284A precision LCR meter. The thicknesses of dielectric and a-IGZO films were measured by a Wvase 32 ellipsometer. In addition, Nanopics 2100 atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS) were employed to measure the surface roughness and elemental composition of the gate dielectrics, respectively.

The chemical composition of the gate dielectric films was measured by XPS, and the Y 3d and Ta 4d signal is shown in Fig. 1. Accordingly, the atomic ratio of Ta/(Y+Ta) is 0%, 47.7%, 68.6%, and 72.7% for the samples A, B, C,

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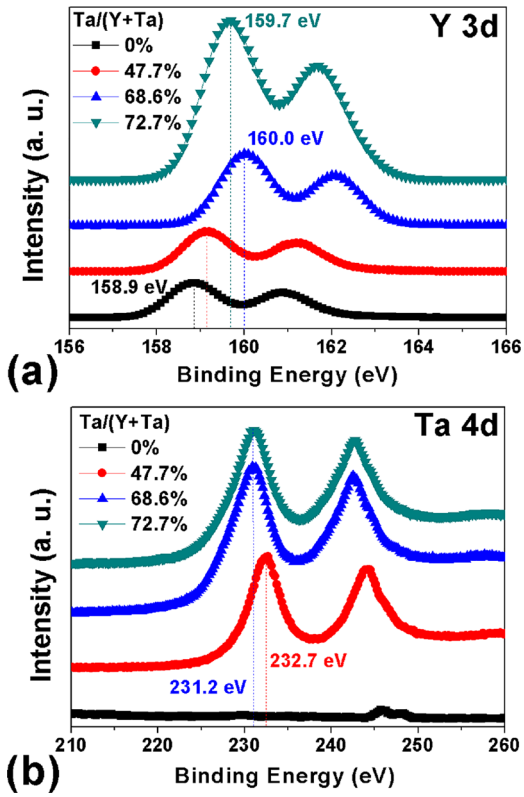

FIG. 1. XPS spectra of Y 3d and Ta 4d for the gate dielectric films with different Ta/(Y+Ta) atomic ratios: 0% (sample A), 47.7% (sample B), 68.6% (sample C), and 72.7% (sample D).

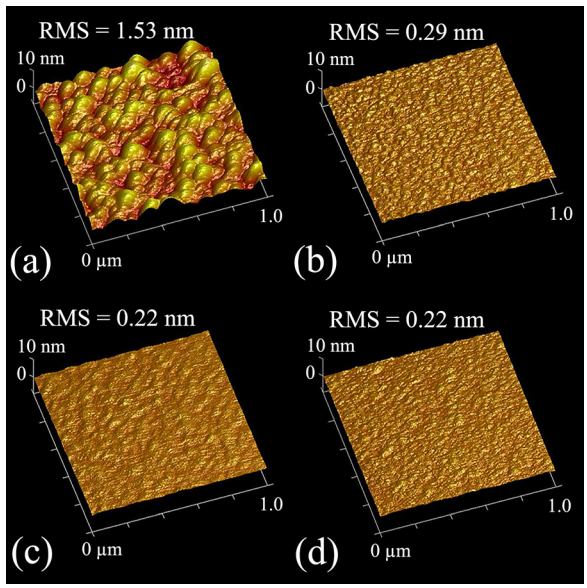

FIG. 2. AFM image of the gate dielectric films: (a) sample A, (b) sample B, (c) sample C, and (d) sample D.

and D, respectively. In Fig. 1(a), the Y $3d_{5/2}$ peak is located at 158.9 eV for sample A, higher than the ideal value (156.8 eV) of the Y-O bond in the NIST Database, suggesting the formation of Y-OH bond,[12] which results from the hygroscopicity of Y_2O_3. With Ta incorporation, the Y $3d_{5/2}$ peak shifts to higher binding energy because Ta incorporation changes the hybridization of valence levels in TaYO and further influences the Y-O bonding strength. However, the Y $3d_{5/2}$ peak of sample D (159.7 eV) shifts to lower binding energy in comparison to sample C (160.0 eV) because excessive Ta incorporation induces Ta-related acceptor-like traps as negatively charged centers in sample D. In Fig. 1(b), the Ta $4d_{5/2}$ peak shifts from 232.7 eV (sample B) to 231.2 eV (samples C and D) for increasing Ta content in the gate dielectric film. It can be ascribed to the fact that Ta incorporation can suppress oxygen vacancy, which is positively charged with an electric field affecting its neighbors, thus leading to an increase in binding energy.[13] In addition, the position of Ta $4d_{5/2}$ peak for the TaYO films with heavy Ta incorporation (in samples C and D) is very close to the ideal value of 230.6 eV for Ta_2O_5 from the NIST Database.

The AFM images in Fig. 2 exhibit the surface roughness of the gate dielectrics with different Ta contents, and the root-mean-square (RMS) values are listed in Table I. It is clear that the surface roughness is effectively reduced by Ta incorporation, with RMS decreasing from 1.53 nm (sample A) to 0.22 nm (samples C and D). The relatively large surface roughness of sample A is resulted from the non-uniform volume expansion of the Y_2O_3 film after moisture absorption,[14] but Ta incorporation helps enhance the resistance of the gate dielectric film against moisture absorption in the other samples. Fig. 3 shows (a) the schematic diagram of the IGZO TFT with TaYO gate dielectric and (b) the cross-sectional structure of Si/TaYO/IGZO layers for sample C by transmission electron microscopy (TEM). According to the TEM image, the TaYO/IGZO interface is very smooth for sample C with a Ta/(Y+Ta) atomic ratio of 68.6%, which is consistent with the AFM result. In addition, a thin silicate layer (thickness = 5.2 nm) between the gate dielectric and Si substrate can be observed, which should be due to the mixing between the gate dielectric and Si substrate during the post-deposition annealing at 400 °C.

As shown in Fig. 4, the forward and reverse transfer characteristics of the samples are measured as gate voltage (V_{GS}) first sweeps from −3 V to 8 V and then back to −3 V with a sweeping speed of 0.65 V/s. The drain voltage (V_{DS}) is fixed at 5 V. Accordingly, threshold voltage (V_{th}) and saturation mobility (μ_{sat}) are extracted from a linear fitting to the

TABLE I. Electrical parameters of a-IGZO TFTs in this work.

Sample No.	A	B	C	D
Ta/(Y+Ta)	0%	47.7%	68.6%	72.7%
$\mu_{sat\_forward}$ ($cm^2V^{-1}s^{-1}$)	11.5	18.4	33.5	24.0
$\mu_{sat\_reverse}$ ($cm^2V^{-1}s^{-1}$)	6.3	16.6	23.1	21.8
V_{th} (V)	3.1	2.5	2.0	1.8
ΔV_{th} (V)	1.8	1.6	1.1	2.0
I_{on}/I_{off} (10^7)	5.6	4.6	2.8	2.8
I_{on} (μA)	56.0	186	320	369
I_{off} (10^{-12}A)	1.0	4.0	11	13
SS (V/dec)	0.190	0.204	0.190	0.184
C_{ox} (μF/cm^2)	0.14	0.21	0.22	0.29
N_t ($10^{12}cm^{-2}$)	1.9	3.2	3.0	3.8
α_H	123.8	75.4	8.1	52.5
T_{ox} (nm)	55.9	39.7	39.9	37.5
k	8.7	9.2	9.6	12.1
RMS (nm)	1.53	0.29	0.22	0.22

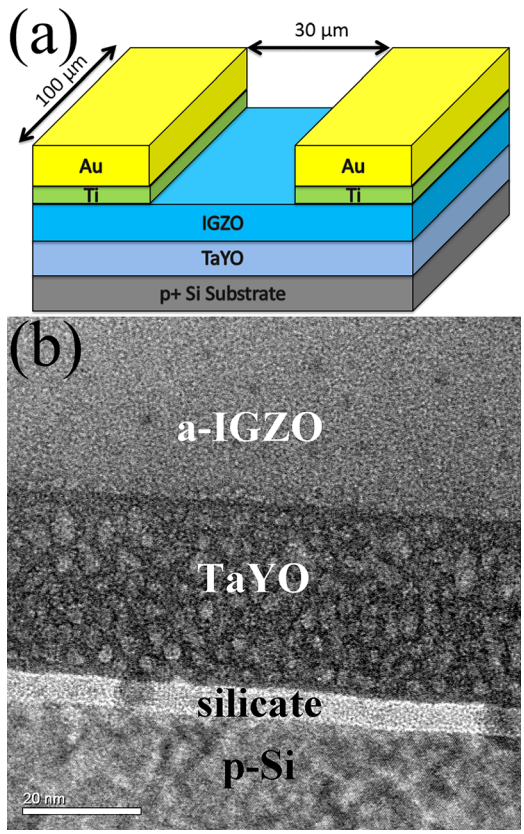

FIG. 3. (a) Schematic diagram of IGZO TFT with TaYO gate dielectric. (b) Cross-sectional TEM image of Si/TaYO/IGZO layers in sample C.

plot of $I_D^{1/2}$ versus V_{GS}, based on the I–V equation of field-effect transistor operating in the saturation region

$$I_D = (\mu_{sat} C_{ox} W/2L)(V_{GS} - V_{th})^2. \quad (1)$$

The on current (I_{on}) is defined at $V_{DS} = 5$ V and $V_{GS} = 8$ V, while the off current (I_{off}) is the minimum current in the transfer curve. The extracted electrical parameters are listed in Table I. For sample A, the electrical performance is relatively poor with a low μ_{sat} (11.5 $cm^2V^{-1}s^{-1}$), which should be attributed to a large Y_2O_3/IGZO interface roughness and a high trap density at/near Y_2O_3/IGZO interface. The moisture absorption of the Y_2O_3 film not only induces non-uniform volume expansion but also increases oxygen vacancies,[15] which can act as acceptor-like traps as revealed by a large positive ΔV_{th} of 1.8 V, also consistent with other results.[16,17] With Ta incorporation, μ_{sat} is significantly increased to 18.4 $cm^2V^{-1}s^{-1}$ and 33.5 $cm^2V^{-1}s^{-1}$ for samples B and C with a Ta/(Y+Ta) atomic ratio of 47.7% and 68.6%, respectively. On the one hand, the smoother dielectric/IGZO interface after Ta incorporation contributes to less scattering on channel carriers, resulting in higher μ_{sat} and I_{on} values because the conduction channel is formed mainly in a very thin layer close to the interface.[18] On the other hand, Ta incorporation reduces the hygroscopicity of the gate dielectric film and thus the generation of oxygen vacancies[11] at/near the dielectric/IGZO interface, resulting in weaker Coulomb scattering on the channel carriers. Furthermore, a decrease of ΔV_{th} from 1.8 V (sample A) to 1.1 V (sample C) is also achieved by higher Ta content in gate dielectric film. Compared to sample A, fewer acceptor-like traps are filled during the forward sweeping in samples B and C with Ta incorporation, and so smaller V_{GS} increase is needed during the reverse sweeping to accumulate the same number of electrons in the conduction channel. In addition, amorphous Y_2O_3 film is easy to crystallize with a crystallization temperature of ~400 °C,[19] but Ta incorporation can suppress its crystallization and thus trap generation,[20] which enhances the positive effects of Ta incorporation.

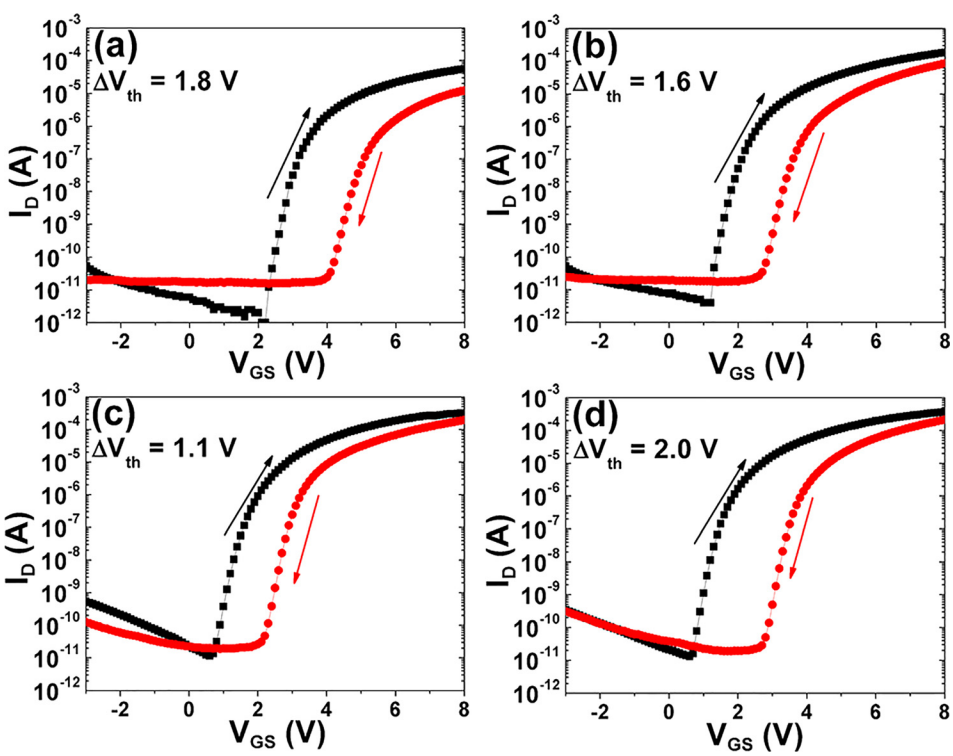

FIG. 4. Forward and reverse transfer characteristics of a-IGZO TFTs: (a) sample A, (b) sample B, (c) sample C, and (d) sample D.

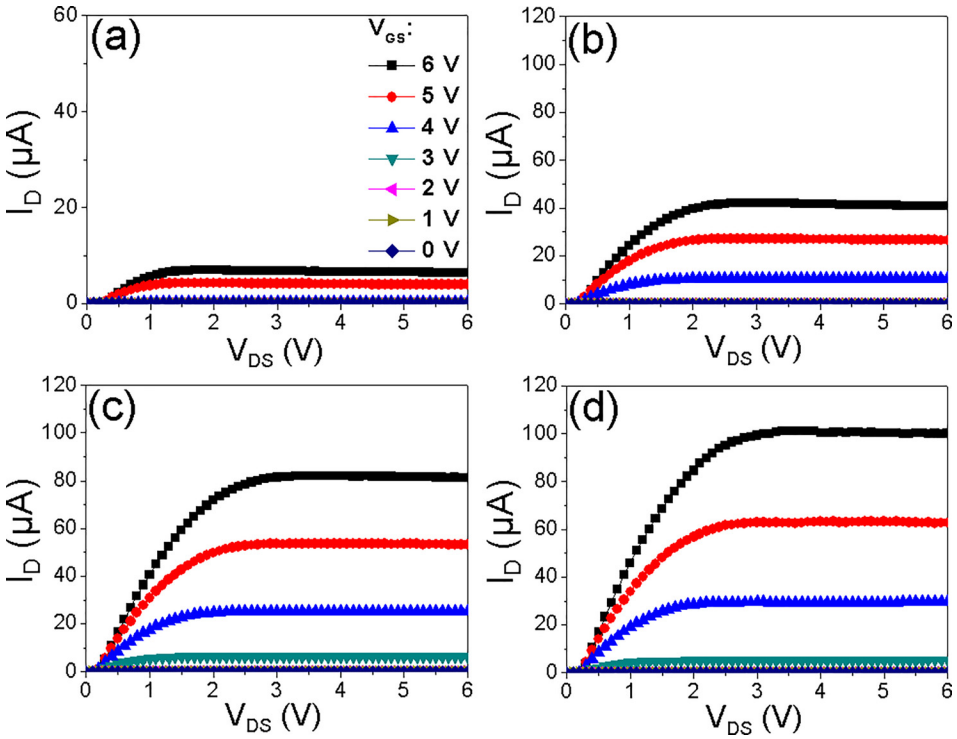

FIG. 5. Output characteristics of a-IGZO TFTs: (a) sample A, (b) sample B, (c) sample C, and (d) sample D.

The trap density (N_t) at/near the dielectric/IGZO interface can be calculated by the equation for the subthreshold swing (SS) of the transistor

$$SS = \frac{KT\ln 10}{q}\left[1 + \frac{q}{C_{ox}}N_t\right], \tag{2}$$

where k is Boltzmann's constant, T the temperature in Kelvin, and q the electron charge.[11] As shown in Table I, although the SS of the devices look similar, their N_t values are quite different. Sample A has the lowest N_t (Y_2O_3 is well-known to be an excellent passivating agent) but shows the lowest carrier mobility due to its largest dielectric roughness. On the other hand, sample C displays the highest mobility because it has the smallest dielectric roughness and also lowest N_t among the Ta-doped samples.

However, the performance of the a-IGZO TFT degrades when the Ta/(Y+Ta) atomic ratio reaches 72.7% (sample D), leading to μ_{sat} of 24.0 $cm^2V^{-1}s^{-1}$ and ΔV_{th} of 2.0 V, both inferior to those of sample C. This should be due to the fact that excessive Ta incorporation could generate more Ta-related traps, e.g., Ta interstitials, at/near the dielectric/channel interface.[21] In addition, Ta is also an excellent n-type dopant in oxide film[22] and can increase the carrier concentration at the dielectric/channel interface, which could partly explain the higher I_{on} value of sample D (369 μA) than that of sample C (320 μA) even with a lower μ_{sat}. Also, the higher k value of sample D than sample C results in larger C_{ox} and thus higher I_{on}. Owing to the higher trap density of Ta_2O_5, I_{off} significantly rises from 1×10^{-12} A (sample A) to 13×10^{-12} A (sample D). In addition, the k value of the dielectric film monotonically increases with Ta content from 8.7 (sample A) to 12.1 (sample D) due to the higher k value of Ta_2O_5 than that of Y_2O_3 and so induces the reduction of V_{th} from 3.1 V (sample A) to 1.8 V (sample D).

The output characteristics of the samples are exhibited in Fig. 5. For all the samples, a linear relation between I_D and V_{DS} is observed in the range of low V_{DS} and current saturation is displayed in the range of high V_{DS}, which are the typical characteristics of field-effect transistor in an n-type enhancement mode.

The low-frequency noise (LFN) measurement is conducted with a fixed gate overdrive voltage ($V_{GS} - V_{th}$) of 5.0 V and V_{DS} of 1.0 V to ensure that the samples work in the linear region, and the results are shown in Fig. 6. At low drain voltage (linear region), the carrier density is uniform along the channel and so the LFN can reflect the average defect density over the entire channel region. The larger gate-oxide thickness (T_{ox}) of sample A contributes to its larger V_{th}, but it does not affect the comparison of LFN because the gate overdrive voltage ($V_{GS} - V_{th}$) is fixed at the same value for all the samples. The carrier-mobility fluctuation model predicts that S_{ID}/I_D^2 should vary as $1/I_D$, which cannot completely explain the LFN results in the insert of Fig. 6, implying that the LFN also originates from carrier-number fluctuation caused by the trapping and detrapping of charge carriers at/near the dielectric/channel interface.[23,24] Based on the LFN results in Fig. 6, the Hooge's constant (α_H), which reflects the level of LFN, is extracted according to the following equation:[25]

$$\frac{S_{ID}(f)}{I_D^2} = \frac{\alpha_H q}{fWLC_{ox}|V_{GS} - V_{th}|}, \tag{3}$$

where f is the frequency and q is the electron charge. In Table I, the lowest noise is achieved by sample C with the smallest α_H of 8.1, supporting the above conclusion that its trap density at/near the dielectric/IGZO interface is the lowest among the Ta-doped samples. This result further proves that Ta incorporation with an appropriate dose can effectively suppress the

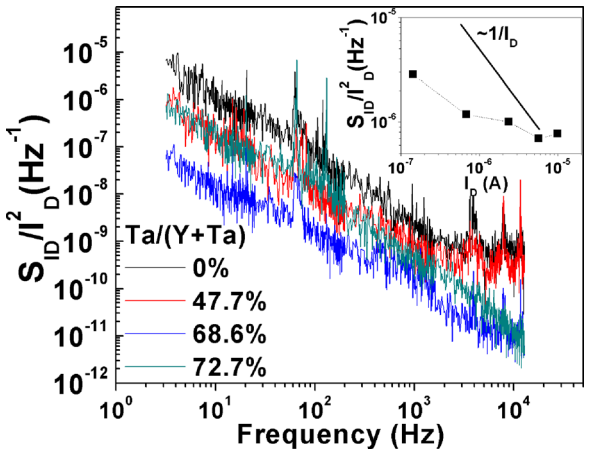

FIG. 6. LFN characteristics of a-IGZO TFTs with different Ta/(Y+Ta) atomic ratios in gate dielectric film.

trap generation at/near the dielectric/IGZO interface caused by the hygroscopicity of Y_2O_3. However, excessive Ta incorporation can generate more Ta-related defects and thus induce a higher noise level, as revealed by sample D with a larger α_H of 52.5. Though with the lowest N_t, sample A has the largest α_H because its largest dielectric roughness induces the strongest carrier scattering among the samples.

In this work, the electrical characteristics of a-IGZO TFT with Y_2O_3 gate dielectric have been improved by incorporating Ta in the gate dielectric. It is found that by enhancing the moisture resistance of the Y_2O_3 gate dielectric, the Ta incorporation with an appropriate dose reduces not only the dielectric/channel interface roughness but also the traps at/near the interface. As a result, the device performance can be significantly improved. For example, the sample with a Ta/(Y+Ta) atomic ratio of 68.6% has achieved high μ_{sat} of 33.5 $cm^2 V^{-1} s^{-1}$, low V_{th} of 2.0 V, large I_{on}/I_{off} of 2.8×10^7, and relatively small ΔV_{th} of 1.1 V. However, excessive Ta can generate defect states at/near the dielectric/channel interface and in the dielectric bulk, thus degrading the electrical performance of the device. In addition, AFM and LFN results also well support the physical mechanisms responsible for the effects of Ta incorporation on the electrical characteristics. In summary, the TaYO gate dielectric is a promising candidate for realizing high-performance a-IGZO TFT in advanced flat-panel displays.

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