

Design of Highly Efficient Broadband Class-E Power Amplifier Using Synthesized Low-Pass Matching Networks

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Abstract—A new methodology for designing and implementing high-efficiency broadband Class-E power amplifiers (PAs) using high-order low-pass filter-prototype is proposed in this paper. A GaN transistor is used in this work, which is carefully modeled and characterized to prescribe the optimal output impedance for the broadband Class-E operation. A sixth-order low-pass filter-matching network is designed and implemented for the output matching, which provides optimized fundamental and harmonic impedances within an octave bandwidth (L -band). Simulation and experimental results show that an optimal Class-E PA is realized from 1.2 to 2 GHz (50%) with a measured efficiency of 80%–89%, which is the highest reported today for such a bandwidth. An overall PA bandwidth of 0.9–2.2 GHz (84%) is measured with 10–20-W output power, 10–13-dB gain, and 63%–89% efficiency throughout the band. Furthermore, the Class-E PA is characterized through measurements using constant-envelope global system for mobile communications signals, indicating a favorable adjacent channel power ratio from –40 to –50 dBc within the entire bandwidth.

Index Terms—Broadband, Class-E, GaN, high efficiency, high power, low-pass matching network, power amplifier (PA), synthesis.

I. INTRODUCTION

HIGH-POWER and high-efficiency power amplifiers (PAs) are very important for modern wireless communication systems, especially those in base-stations, to achieve low-cost and highly reliable transmitters. High-efficiency PAs are commonly realized using switch-mode topologies, such as Class-D, Class-E, and Class-F⁻¹, or harmonic-tuned circuitries, like Class-F and Class-J [1]. Those high-efficiency PAs usually require a high saturation level of the device and accurate harmonic engineering, leading to bandwidth restrictions in their frequency response [2]–[4].

Nevertheless, future communication systems, e.g., WiMax and LTE, would require wider bandwidths, not only for the coverage of multiple frequency bands, but also due to the increasing effective bandwidth of the signal, i.e., up to 100 MHz. The military wireless systems require even wider bandwidths, typically

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TABLE I
STATE-OF-THE-ART HIGH-EFFICIENCY BROADBAND PAs

Reference	PA Mode	BW (GHz, %)	Gain (dB)	P_{out} (W)	Eff.(%)
2009 [8]	Class-J	1.4–2.6, 60%	11–12	9–11	57–72
2009 [9]	Class-E	2.0–2.5, 22%	10–13	7–12	74–77
2009 [10]	Class-E	0.6–1, 50%	12–18	45–49	66–87
2010 [11]	N/A	1.8–3.1, 53%	9–10	20–50	56–65
2010 [12]	N/A	1.9–4.3, 78%	9–11	10–15	57–72
This work	Class-E	0.9–2.2, 84%	10–13	10–20	63–89

above an octave. The distributed amplifier (DA) is a common solution for wideband amplification [5]. However, this approach requires multiple devices, which results in a low overall efficiency. Another possible solution based on the optimization of the fundamental harmonic impedance has been presented in [6] and [7], achieving multioctave bandwidths. However, significant higher order harmonics remain in such designs, leading to relatively low efficiencies ($\approx 50\%$ in [6] and 20% in [7]) and harmonic distortion.

Thus, realizing high-power and high-efficiency PAs within a broad bandwidth is a critical research area. To date, several design techniques have been proposed and demonstrated with an optimization of bandwidth and efficiency [8]–[12]. Several critical features of these PAs are summarized in Table I. It is important to note that the matching network topologies used in those designs are equivalent to low-pass prototypes with an order $n \leq 4$. Higher order low-pass prototypes have not yet been widely applied in the broadband PA design, although they can potentially yield improved matching quality and wider bandwidth.

Herein, we present a practical method for designing a broadband high-efficiency Class-E PA that employs high-order low-pass circuit topologies at the input ($n \geq 8$) and output ($n \geq 6$). Compared to Class-D designs, the presented Class-E PA exhibits simpler circuitry and reduced sensitivity to parasitics. Compared to Class-F and Class-F⁻¹ designs, it is more forgiving to harmonic terminations requirements and allows for a broadband performance. The presented design is based on a commercially available 25-W Cree GaN HEMT. A three-stage Chebyshev low-pass network ($n = 6$) is synthesized for the output matching, and it is implemented using transmission lines, as those in [13]–[15], which yield a better PA performance than that using lumped elements [15]. Optimal fundamental, second-harmonic, and third-harmonic impedance terminations are provided for the transistor output over a broad bandwidth. The output parasitics of this packaged GaN transistor are carefully characterized and de-embedded in confirming a wideband

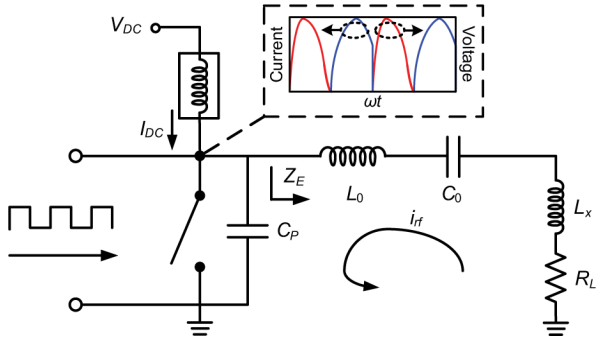


Fig. 1. Ideal Class-E PA topology.

Class-E behavior. This design achieves a state-of-the-art performance compared to the recently published results (Table I). In particular, it exhibits the highest broadband reported efficiency. Furthermore, modulated testing using a global system for mobile communications (GSM) signal shows a very good potential of this Class-E PA for amplifying constant-envelope signals.

II. BROADBAND CLASS-E PA

A. Review of the Classic Class-E PA Theory

The conventional ideal Class-E PA topology is depicted in Fig. 1. For this PA circuitry [16], the transistor is considered as a switch and a capacitor (C_P) is connected in parallel with it. If the transistor switch is turned on, the current flows entirely through the switch (field-effect transistor (FET)'s drain and source, or bipolar junction transistor (BJT)'s collector and base) and the voltage is zero. This current can be expressed as

$$i_{sw}(t) = I_{DC}(1 + a \sin(\omega t + \phi)). \quad (1)$$

When the switch is turned off, the current flows entirely into the capacitor, which is charged simultaneously. During this off-state interval, the voltage on this parallel capacitor is given by

$$\begin{aligned} v_{sw}(t) &= \frac{1}{C_P} \int_0^t i_{sw}(t') dt' \\ &= \frac{I_{DC}}{\omega C_P} (1 + a(\cos(\omega t + \phi) - \cos \phi)). \end{aligned} \quad (2)$$

There are two boundary conditions for the ideal Class-E operation [13], [16], [17], referred as zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions. Assume the switch is turned off at $t = 0$ and turned on at $t = T/2$, those two conditions are given by

$$\begin{aligned} v_{sw} \left(t = \frac{T}{2} \right) &= 0 \\ \frac{\partial v_{sw}}{\partial t} \left(t = \frac{T}{2} \right) &= 0 \end{aligned} \quad (3)$$

where T denotes the time period of one Class-E duty cycle. The ZVS condition prevents simultaneous nonzero voltage and current across the switch device, and ZVDS enforces the current to

start flowing after the voltage has reached zero (soft switching). The value of a and ϕ can be determined uniquely by applying these two constraints, leading to

$$a = \sqrt{1 + \frac{\pi^2}{4}} \quad (4)$$

$$\phi = -\arctan \frac{2}{\pi}. \quad (5)$$

Consequently, as shown in the rectangular box in Fig. 1, there is no overlap between the transient drain (or collector) current and voltage, which leads to a zero dc power dissipation and 100% drain efficiency.

Using Fourier-series expansions [13], [17], the optimal fundamental load, yielding perfect Class-E operation, can be determined by

$$Z_{E,f_0} = \frac{0.28}{\omega C_P} e^{49^\circ}. \quad (6)$$

This impedance presents inductive, which is illustrated in Fig. 1.

In the ideal Class-E mode, the total current through the combined switch-capacitor tank is a pure sinusoidal wave, and the harmonics are entirely due to the voltage. In turn, the ideal impedances at higher order harmonic frequencies are infinite

$$Z_{E,nf_0} = \infty, \quad n \geq 2. \quad (7)$$

B. Broadband Class-E PA Scheme

The classic Class-E topology shown in Fig. 1 is indeed for the narrowband design, as the series LC resonator has a limited frequency response. Equation (6) also indicates that the optimum load impedance is frequency varying. To implement the broadband Class-E PA, two problems are to be addressed. First, a matching network is needed to transform Z_0 to Z_E for the switch-capacitor tank over a significant bandwidth, e.g., $>50\%$. Second, a broadband filter, whose passband covers the desired bandwidth, is needed to provide infinite impedance at harmonic frequencies, replacing the LC resonator. In this research, the matching network and filter is co-designed in order to reduce the circuit complexity.

Furthermore, the perfect switching behavior is not achievable at the gigahertz frequency level because of the nonideal effects of the transistor and nonsquare wave driven signal at the input. Practically, the transistor gate/base is biased at the pinch-off point. The input signal now needs to be sufficiently large to turn the transistor on during the entire positive half duty-cycle and subsequently turn it off during the negative half duty-cycle [1]. The proposed realistic broadband Class-E PA topology is shown in Fig. 2.

It is important to note, however, that the bandwidth of this matching network design method is limited to one octave [8] because the second harmonic of the low-end fundamental will occur in the passband if the bandwidth is above one octave. Thus, the original target frequency band is from 1 to 2 GHz (L -band). To achieve a multioctave bandwidth, one can design multiple matching networks for different bands and use switches to select the proper one.

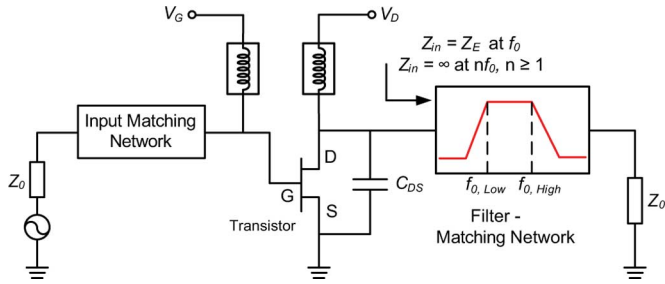


Fig. 2. Broadband Class-E PA topology.

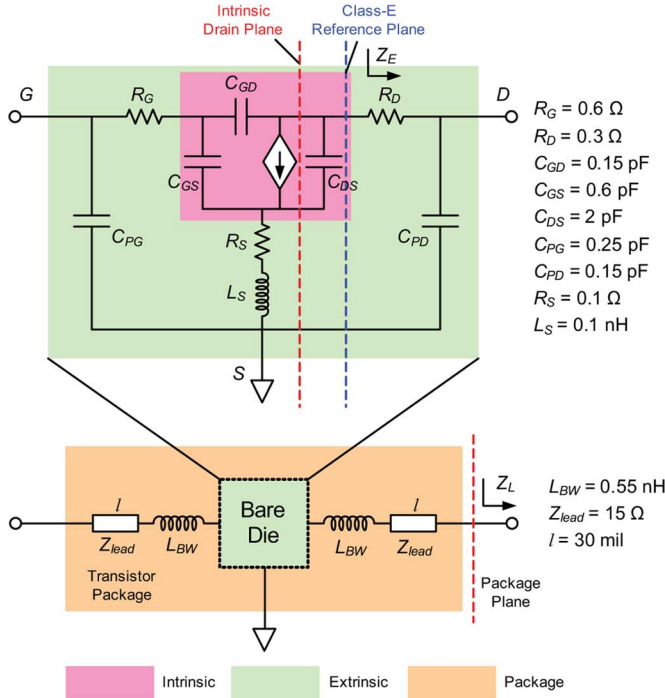


Fig. 3. Typical GaN transistor model showing the parasitics [18], [19].

C. Design of Broadband Class-E PA Using a Packaged GaN HEMT

Recent developments in solid-state techniques have enabled wide bandgap devices, such as GaN and SiC HEMTs, which significantly improve transistor performance from conventional CMOS techniques. To date, GaN HEMTs have been applied in numerous high-efficiency broadband PA designs [8]–[12]. In this research, a GaN transistor is selected as the active component to implement the broadband Class-E PA. In general, GaN transistors exhibit high breakdown voltage, low and voltage-independent output capacitance (C_{DS}), and low turn-on resistance (R_{ON}) [18]. These characteristics are very important for realizing high-efficiency switch-mode PAs. However, current commercially available GaN HEMTs that are appropriate for discrete designs are typically packaged. Their packages often introduce nonnegligible parasitics. Fig. 3 shows a typical equivalent circuit of a 25-W Cree GaN HEMT (CGH40025) [18], [19], which is sealed in the Cree 440166 package. Fig. 3 also lists the approximate values of those parasitics. The intrinsic parasitic values, i.e., C_{DS} , C_{GD} , and C_{GS} , are approximated based on [18] and the manufacturer’s datasheet. The extrinsic parasitic

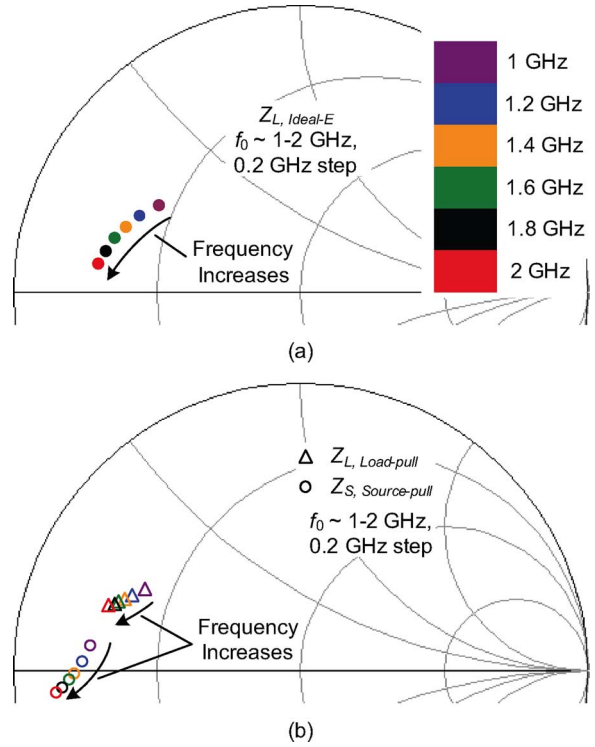


Fig. 4. Characterization of Cree GaN CGH40025 at package plane (Z_L) throughout L-band. (a) De-embedded optimal output impedance from ideal Class-E model. (b) Optimum output and input impedances extracted from load-pull and source-pull simulations.

values, i.e., C_{PD} , C_{PG} , L_S , R_S , R_D , and R_G , are estimated using the method presented in [19]. The package model is provided by the manufacturer. Using this packaged transistor to design a Class-E PA, these parasitic effects need to be carefully considered in order to perform a sufficiently accurate matching. Especially, the output capacitance of the transistor (C_{DS}) can be taken advantage to replace the shunt capacitor C_P in the ideal topology, which is the main advantage of the Class-E topology over the other switch-mode PA, Class-D.

Fig. 4(a) shows the ideal Class-E impedance of this transistor at the device package plane (Z_L) de-embedded from the Class-E reference plane (Z_E). Z_L and Z_E are illustrated in Fig. 3. However, the intrinsic parasitics are usually nonlinear (voltage dependent), which might lead to an accuracy degradation of this theoretical model in the high power case. Fortunately, a very good nonlinear model of this transistor is available from the manufacturer, which is also optimized for switch-mode PA designs [18]. Therefore, the load-pull simulation is conducted on the GaN transistor using Agilent’s Advanced Design System (ADS)¹ in order to find a more accurate load impedance. It is worthy noting that the optimal impedance obtained here is referred to the package plane, as the package effect has been incorporated in the transistor model. In the load-pull simulation, a sufficiently large input RF power, i.e., >1 W, is applied to drive the transistor as a switch. Fig. 4(b) shows the simulated efficiency-optimized load impedance of this transistor at 1–2 GHz. Fig. 4(a) and (b) indicates the similar load impedance

¹Agilent Technol. Inc., Santa Clara, CA, 2009. [Online]. Available: <http://www.agilent.com>

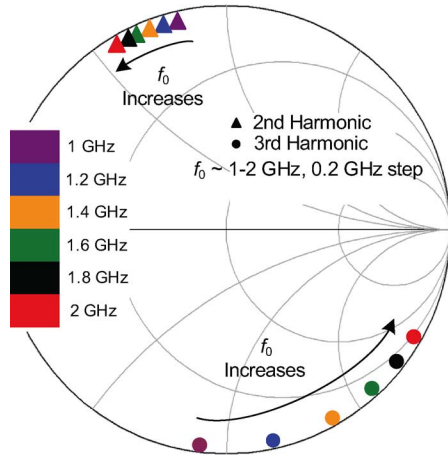


Fig. 5. Optimal impedance of the second and third harmonics extracted from load-pull simulation.

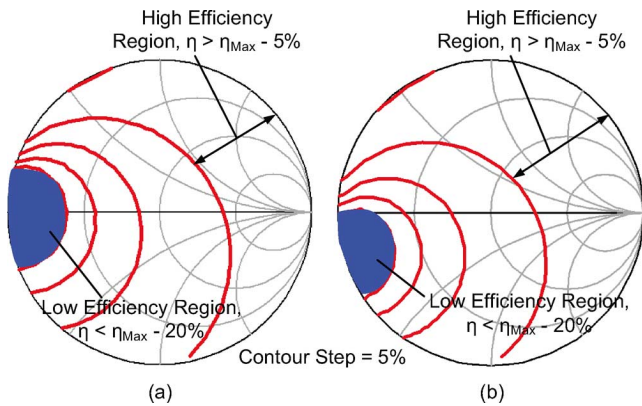


Fig. 6. Simulated load-pull contours of the second harmonic impedance: (a) at $2f_0 = 2$ GHz and (b) at $2f_0 = 4$ GHz.

region for the Class-E operation within this frequency range, while the load-pull impedance spreads less than the ideal one. The broadband Class-E behavior will be further demonstrated using waveform engineering in the schematic simulation of the entire PA (Section IV). The source-pull simulation is also conducted to obtain the optimum input impedance of the transistor, which is shown in Fig. 4(b).

Harmonic impedance matching is another very important aspect in the high-efficiency PA design. Theoretically, infinite harmonic impedances need to be provided at the Class-E reference plane, which is, however, not achievable using any realistic filter circuit. Moreover, the parasitics need to be considered. Thus, the load-pull simulation is carried out again to prescribe the optimal harmonic impedances at the package plane. Fig. 5 depicts the optimal impedances of second and third harmonics when f_0 varies from 1 to 2 GHz.

As expressed in [13], the second harmonic impedance plays the most important role in impacting the efficiency of a Class-E PA. Fig. 6 shows the simulated load-pull contours of the second harmonic at 1 and 2 GHz, indicating the tolerable region of the second harmonic impedance in which high efficiency can be achieved. Fig. 7 illustrates the contours of the third harmonic at 1 and 2 GHz, which underlines that the efficiency is less sensitive

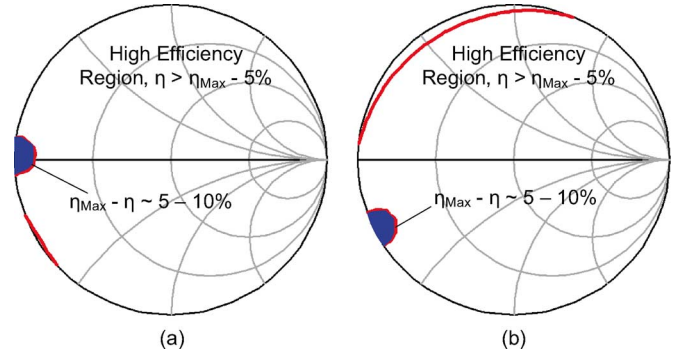


Fig. 7. Simulated load-pull contours of the third harmonic impedance: (a) at $3f_0 = 3$ GHz and (b) at $3f_0 = 6$ GHz.

to the third-harmonic impedance with a maximum efficiency drop of only 10% in the small blue regions (in online version).

To sum up, there are two requirements of the matching network for broadband Class-E PA:

- provide the appropriate fundamental-frequency impedance across the continuum spectrum of frequencies across the desired bandwidth;
- provide the appropriate harmonic impedance which stays in the high-efficiency region.

In the broadband PA design, compromises are always unavoidable in matching the necessary impedances across the desired bandwidth [20]. Also, as the second harmonic impedance of the frequency near 1 GHz would be close to the fundamental matching impedance of 2 GHz, an optimal design within 1–2 GHz is hard to achieve in practice. Therefore, the presented design strives for achieving optimal results in the 1.2–2-GHz region.

III. DESIGN AND IMPLEMENTATION OF INPUT AND OUTPUT MATCHING NETWORKS USING LOW-PASS TOPOLOGY

A. Matching Network Topology Selection for Broadband Class-E PA

There are actually numerous circuit topologies to realize broadband matching such as a $1 : n$ impedance transformer. Fig. 8 shows the most common broadband matching methods, including multiple transmission line sections synthesized using the small reflection method [21], magnetic coupling network [21], and multistage ladder networks. However, the first two networks [see Fig. 8(a) and (b)] give the same impedance for the high-order harmonics as the fundamental one. Thus, they are not applicable for highly efficient PAs. From the ladder-based networks [see Fig. 8(c) and (b)], only the low-pass and bandpass behaviors are useful. However, a conventional low-pass filter or a conventional bandpass filter do not lead to the optimal behavior because of the restrictions imposed in their out-of-band behaviors, as is explained in Fig. 9, which do not yield the minimum possible in-band ripple. If these restrictions are lifted [e.g., steep out-of-band attenuation below the lowest frequency, shown in Fig. 9(b)], a lower ripple can be achieved within the desired bandwidth [23] for a given number of ladder steps. Consequently, the low-pass matching network

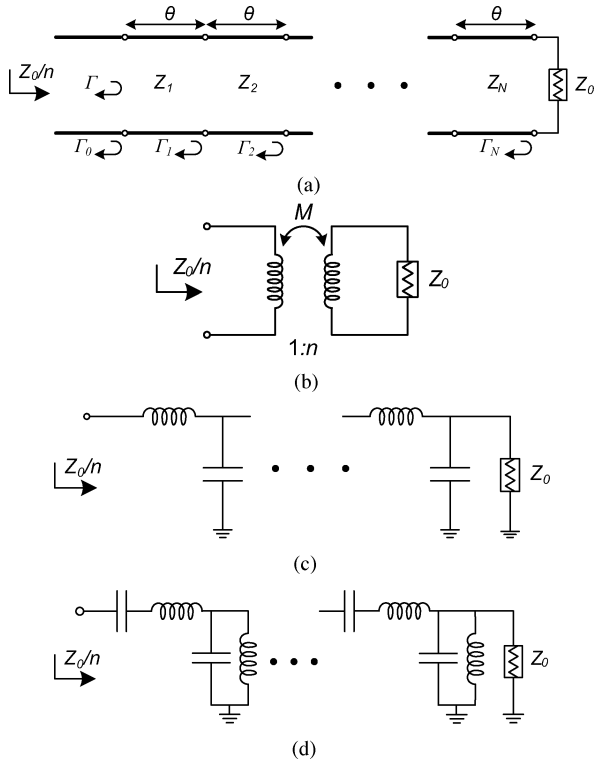


Fig. 8. Common broadband matching networks. (a) Small reflection theory [21]. (b) Magnetic coupling structure. (c) Multistage low-pass ladder network. (d) Multistage bandpass ladder network.

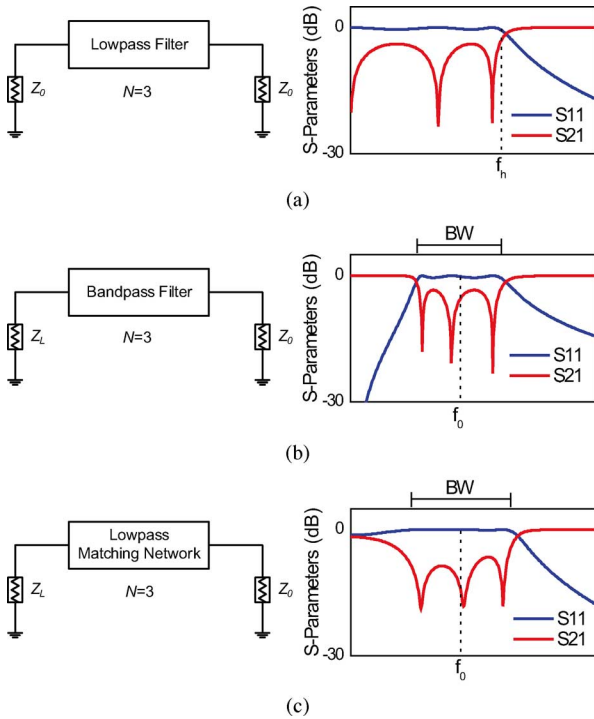


Fig. 9. Comparison of ADS simulated frequency responses between: (a) conventional low-pass filter, (b) bandpass filter, and (c) low-pass matching network [23].

approach instead of conventional filters is selected to realize this broadband Class-E PA.

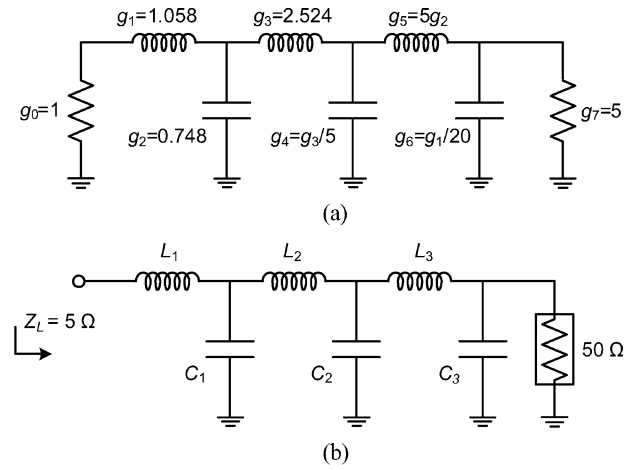


Fig. 10. Three-stage low-pass matching network: (a) prototype, (b) scaled to the 50-Ω system, and 1.6-GHz center frequency.

The low-pass matching network synthesis using a Chebyshev prototype has been theoretically presented in [23]. However, this presentation only covers the real-to-real impedance transformer. In this design, the GaN transistor requires an inductive output impedance, as depicted in Fig. 4. Therefore, this theoretical method is not sufficient. In this section, a more practical method for synthesizing a real-to-complex low-pass matching network is introduced.

B. Synthesis of the Multistage Low-Pass Matching Network

It is well known in filter theory that higher order designs lead, in general, to wider bandwidth and steeper stopband attenuation [22]. This is also true to low-pass matching network design. In the *L*-band Class-E PA design, the optimal load impedance actually varies with frequency, as illustrated in Fig. 4. The real part of this frequency-varying impedance is around 10 ($Z_{L,1.6G} = 10 + 8j$), leading to a transformation ratio of 5:1. To achieve this ratio throughout an octave bandwidth with an in-band ripple of <0.1 dB, at least three stages are needed for the low-pass network, as expressed theoretically in [23]. One- or two-stage low-pass matching networks yield an in-band ripple of 0.9–1.4 and 0.2–0.3, respectively. As the target impedance Z_L is a complex number, there are two main steps in the design process that are described in the following.

Step 1) The first step is to design a 5:1 real-to-real Chebyshev low-pass matching network within the desired bandwidth. A prototype three-stage 5:1 low-pass transformer with a bandwidth of 80% is extracted from [23], as shown in Fig. 10(a). These g -elements denote a low-pass transformer in a normalized system with 1-Ω impedance and 1-rad/s angular frequency [23]. This prototype is scaled to the 50-Ω system at a center frequency of $f_0 = 1.6$ GHz by

$$L_n = g_{2n-1} \frac{\omega'_0}{\omega_0} \frac{50}{g_0} \quad (8)$$

$$C_n = g_{2n} \frac{\omega'_0}{\omega_0} \frac{g_0}{50} \quad (9)$$

TABLE II
PARAMETERS OF THE THREE-STAGE LOW-PASS MATCHING NETWORKS FOR REAL-TO-REAL AND REAL-TO-COMPLEX TRANSFORMATIONS

Elements	Real-to-Real	Real-to-Complex
C_1	7.7 pF	8.4 pF
L_1	1.1 nH	1.7 nH
C_2	5.2 pF	5.9 pF
L_2	2.5 nH	2.2 nH
C_3	2.3 pF	2.2 pF
L_3	3.7 nH	3.5 nH

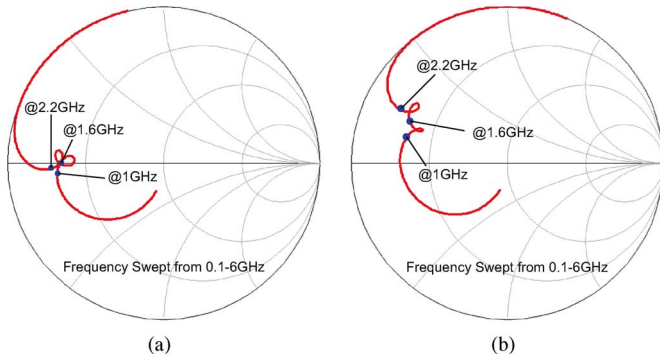


Fig. 11. Simulated input impedance of the three-stage low-pass matching network: (a) a 1:5 real-to-real Chebyshev transformer, (b) with a larger L_1 optimized for PA output matching.

where ω'_0 and g_0 represent the normalized angular frequency and impedance. Fig. 10(b) shows the scaled low-pass matching network with the values of elements listed in Table II. The simulated results are shown in Fig. 11(a), indicating the frequency response with a double-knot shape around the target impedance.

Step 2) The second step is the post-optimization of the real-to-real transformer in the first step, which already yields a starting point, in order to form a real-to-complex transformer. The simplest option is to simply increase L_1 to 1.8 nH, as shown in Fig. 11(b). However, this does not yield an optimal result. A computer-aided design (CAD) optimization is needed, in which the input port impedance is set to be $10 - j8$ (conjugate of the optimal impedance at the center frequency). Each element of this network is gradually adjusted until a Chebyshev response is observed (flat in-band S_{21} and equal-ripple in-band S_{11}). The achieved S -parameters are shown in Fig. 12(a). The input impedance of this optimized matching network is shown in Fig. 12(b). The element values are shown in Table II in comparison with the real-to-real case.

C. Distributed-Element Implementation of the Low-Pass Output Matching Network

The most straightforward way to implement the designed three-stage matching network is to build it with lumped inductors and capacitors, as shown in the circuit schematic (Fig. 12). However, given the difficulty in getting high-quality inductors

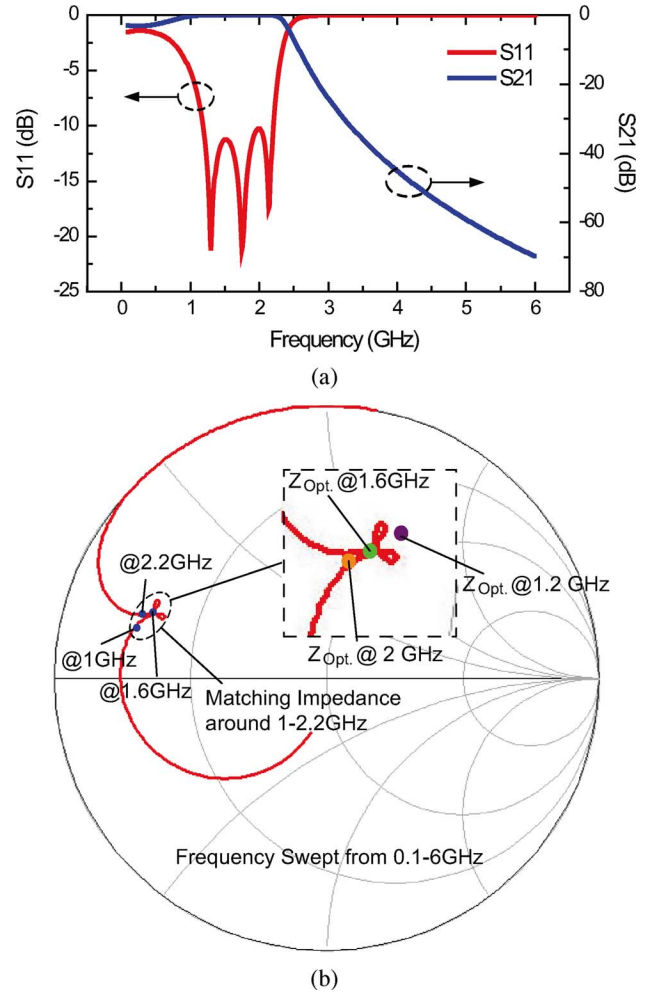


Fig. 12. Synthesized three-stage low-pass network for output matching: (a) simulated S -parameters when using port 1 and port 2 impedances of $10 - j8 \Omega$ and 50Ω and (b) simulated input impedance.

and capacitors at the desired frequency range, the low-pass matching network is implemented with all-distributed elements in this paper.

The inductors are replaced by high-impedance (high- Z) transmission-line sections and the capacitors are replaced by low-impedance (low- Z) open-circuit stubs. The implementation of the matching network designed in Section III-B is shown in Fig. 13. Due to fabrication tolerances in our setting, the allowed smallest linewidth is 20 mil, which leads to a $96\text{-}\Omega$ microstrip line on the 20-mil-thick Rogers Duroid 5880LZ printed circuit board (PCB) ($\epsilon_r = 1.96$).² Using short-line-approximation theory expressed in [21], the length of the short high- Z transmission lines are calculated by

$$\omega L \simeq Z_l \beta l \Rightarrow l \simeq \frac{v_p L}{Z_l} \quad (10)$$

where Z_l is the characteristic impedance of the line, and β and v_p are the propagation constant and phase velocity of the transmission line, respectively. For the open-circuit stubs, which are

²Rogers Corporation, Rogers, CT. [Online]. Available: <http://www.rogerscorp.com/>

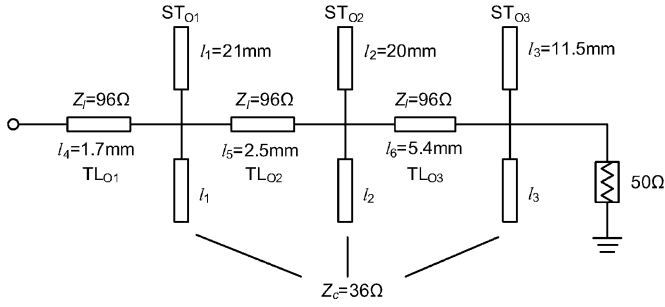


Fig. 13. Implemented low-pass output matching network using distributed elements.

identically placed on both sides of each node, the length of each stub is calculated by

$$\frac{1}{\omega C} = 2 \frac{Z_c}{\tan \beta l} \Rightarrow l = \frac{\arctan(2\omega Z_c C)}{\beta} \quad (11)$$

where Z_c is the stub characteristic impedance, which is 36Ω in this design.

Equations (10) and (11) provide a starting point to run a CAD-based post-optimization. The parameters of this matching network is optimized using ADS together with the transistor in order to achieve an optimal Class-E PA performance. The finalized design of this output matching network is shown in Fig. 13. Fig. 14 shows the simulated input impedances of this implemented matching network from schematic and full-wave simulations throughout the band of 1–2.2 GHz, including fundamental, second, and third harmonics. A good agreement between schematic and full-wave simulations is observed. The fundamental impedance region (red solid line in online version) indicates a good matching quality from 1.2 to 2 GHz, compared to the load-pull results plotted in Fig. 4. It is also seen from Fig. 14 that the second-harmonic impedance is very close to the optimum region shown in Fig. 5 when $f_0 \geq 1.2$ GHz. The third harmonic impedance moves along the boundary of Smith Chart, which falls in the high-efficiency region for most of the frequencies, except around $f_0 = 1.8$ GHz. However, the efficiency drop due to the third harmonic around $f_0 = 1.8$ GHz is $< 10\%$. Considering the fundamental and harmonic matching conditions, as illustrated in Section II, an optimized Class-E operation can be achieved from 1.2 to 2 GHz.

D. Broadband Input Matching Network Design

The desired input impedance of the GaN transistor is shown in Fig. 4(b). This impedance has a real part varying from 4.5 to 2Ω and an imaginary part varying from 3.9 to -3.1Ω . As the imaginary part has a variable polarity and a small amplitude, this broadband matching problem is considered as a 20:1 real-to-real impedance transformation (from 50 to 2.5Ω) within 1–2.2 GHz. Compared to the case of output matching, this transformation ratio is much greater so a four stage low-pass network is designed to implement the input matching.

The Chebyshev low-pass prototype of a 20:1 impedance transformer with 80% fractional bandwidth [23], shown in Fig. 15(a), is applied and scaled to the desired frequency band and 50- Ω system impedance. The implementation of this circuit

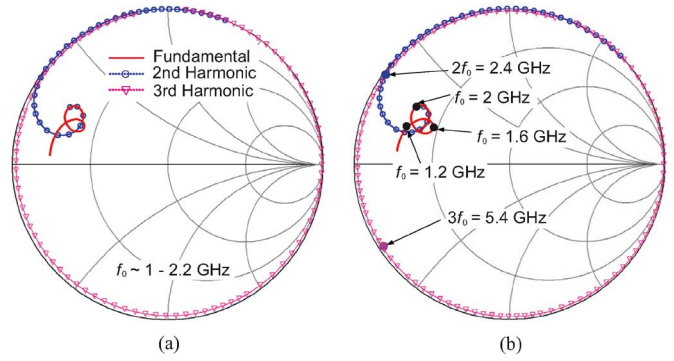


Fig. 14. Fundamental and harmonic impedances of the implemented output matching network between fundamental bandwidth of 1–2.2 GHz extracted from: (a) schematic simulation and (b) full-wave simulation.

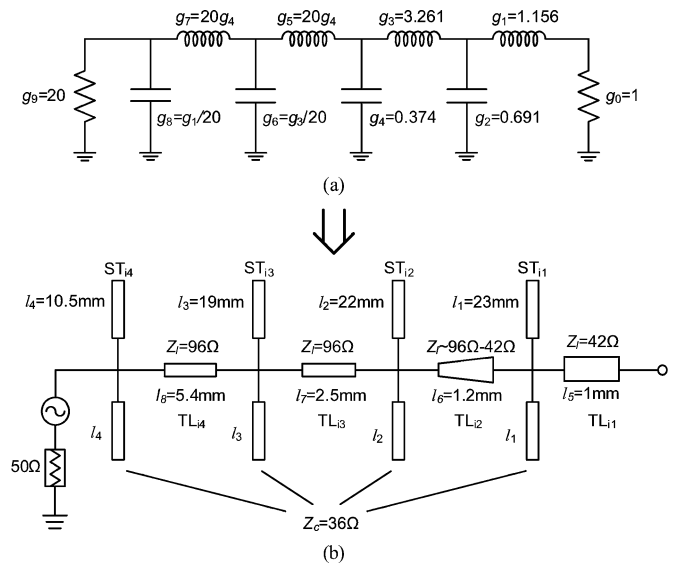


Fig. 15. Design and implementation of the input matching network. (a) Eighth-order low-pass prototype. (b) Implemented circuit using transmission lines.

follows a similar path to the one shown before for the output matching network using distributed elements (Section III-C). The final circuit schematic and its parameters are shown in Fig. 15(b). It is important to note that the implemented schematic initially yields a 0.65-mm 96- Ω transmission line (TL_{i2}) for implementing g_3 , implying that the stubs surrounding this line are too close to each other, leading to a nonnegligible coupling effect. As expressed in (10), the length of this line can be increased by decreasing the impedance. However, a normal higher impedance transmission line leads to an unbalanced ST_{i2} because of the different widths of TL_{i2} and TL_{i3} . Thus, a 1.2-mm tapered line is used here to replace the 96- Ω transmission line. Simulation using the open-ended coupled-line model is conducted to investigate the coupling effects between the stubs. Three pairs of the closest stubs of input and output matching networks are characterized, and the results are shown in Fig. 16, indicating a weak coupling of < -30 dB within the desired bandwidth. Fig. 17 plots the matching impedance of this input matching network extracted from schematic and full-wave simulations, showing a good agreement between them. The simulation results further demonstrate that the weak coupling

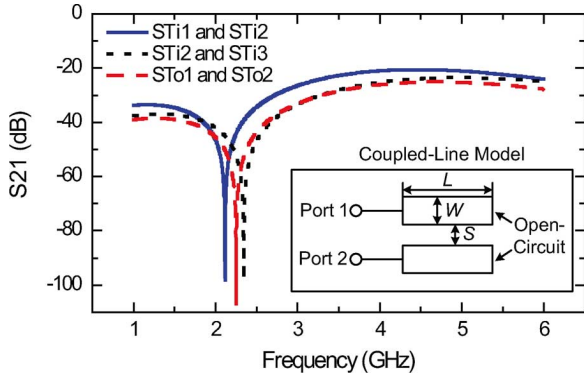


Fig. 16. Investigation of the coupling effect between the closest stubs using the coupled-line model.

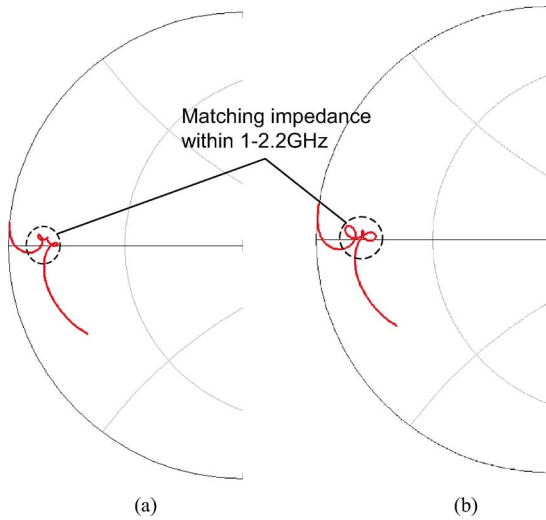


Fig. 17. Simulated impedance of the implemented input matching network. (a) Schematic simulation. (b) Full-wave simulation.

effects have no significant impact on the low-pass matching network. A good coverage of the optimal input impedance is also observed compared to that shown in Fig. 4(b).

IV. PA DESIGN AND IMPLEMENTATION

The Class-E PA is realized by connecting the GaN transistor to the input and output matching networks designed in the above sections. The circuit schematic diagram of the designed Class-E PA is shown in Fig. 18. In the PA implementation, the transmission line (TL_{O1}) of the output matching network is modified to fit the package lead of the transistor, while keeping the same frequency response as the original version. The gate bias network is realized using a 22-nH inductor (L_{G1}) followed by a 0.5- μ H conical inductor (L_{G2}) together with shunt capacitors presenting a “short circuit” for both RF and lower frequency (megahertz level). This network is simulated using realistic models from manufacturers, yielding a large impedance of $|Z_L| > 2000$ at the gigahertz level, which can be considered as an ideal open. The drain bias circuit is realized using a 25-nH inductor with a large current handling capability of 3.5 A and shunt capacitors. This network presents a simulated impedance of $0.5 + 185j$ at 1 GHz and $8 + 400j$ at 2 GHz, which presents

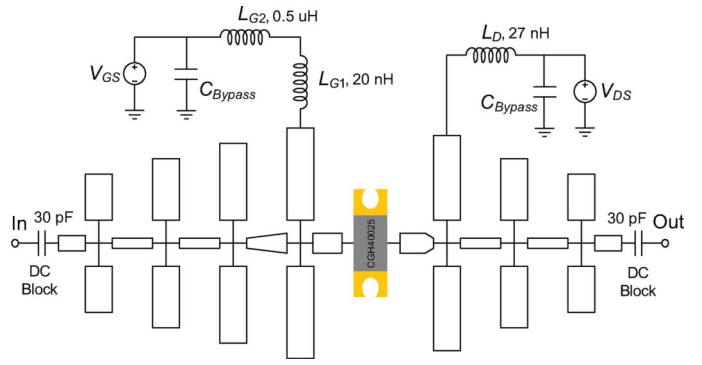


Fig. 18. Circuit schematic of the broadband Class-E PA.

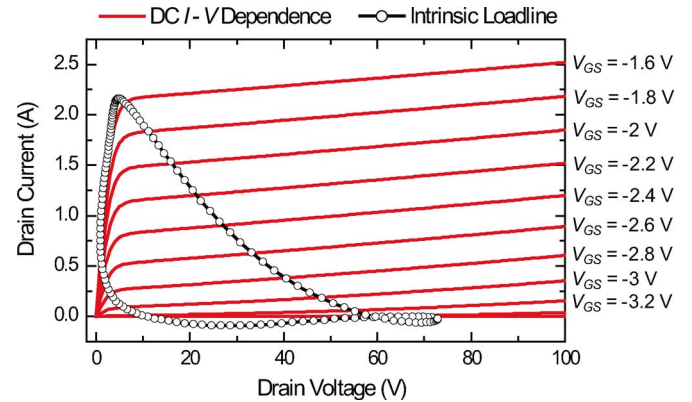


Fig. 19. Simulated $I-V$ characteristics of the GaN transistor and dynamic loadline at its intrinsic drain plane when the PA is operating at 1.2 GHz.

a near open circuit. Two 30-pF capacitors are connected at the input and output ports as dc blocks.

The entire PA is simulated in ADS using the harmonic-balance simulator including the effects of realistic bias circuits and dc blocks. Fig. 19 shows the simulated dynamic loadline of the Class-E PA at 1.2 GHz and 15-W output power, indicating a favorable switching behavior. The density of the circle markers implies the amount of time that the transistor is operating in different regions. Fig. 20 shows the simulated voltage and current waveforms at the intrinsic drain plane, when the broadband Class-E PA is operating at 1.2, 1.6, and 2 GHz with 15-W output power. Compared to the ideal waveforms (Fig. 1), the simulated results show a similar shape and the difference is mainly due to the nonideal switching effect, which causes a $< 100\%$ drain efficiency.

The PA is fabricated on the Rogers 5880LZ substrate (same as the ones used to implement the matching networks). Fig. 21 shows the fabricated PA mounted on a copper substrate with connecting screws. The bottom copper plate acts as not only the ground plane, but also as a heat sink. The dimensions of the entire PA testing board are also given in Fig. 21.

V. EXPERIMENTAL RESULTS

A. Continuous-Wave (CW) Measurements

The PA is tested using the single-tone CW signal from 0.9 to 2.2 GHz with 0.1-GHz step. The transistor gate is biased at the

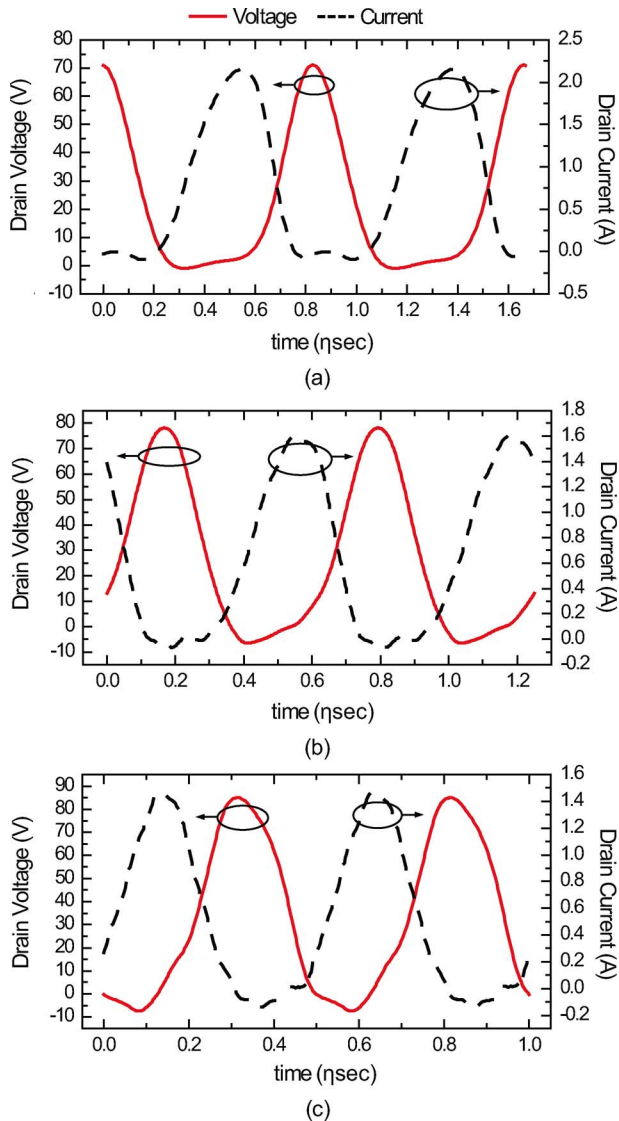


Fig. 20. De-embedded intrinsic drain waveforms of voltage and current from ADS simulation: (a) at 1.2 GHz, (a) at 1.6 GHz, and (c) at 2 GHz.

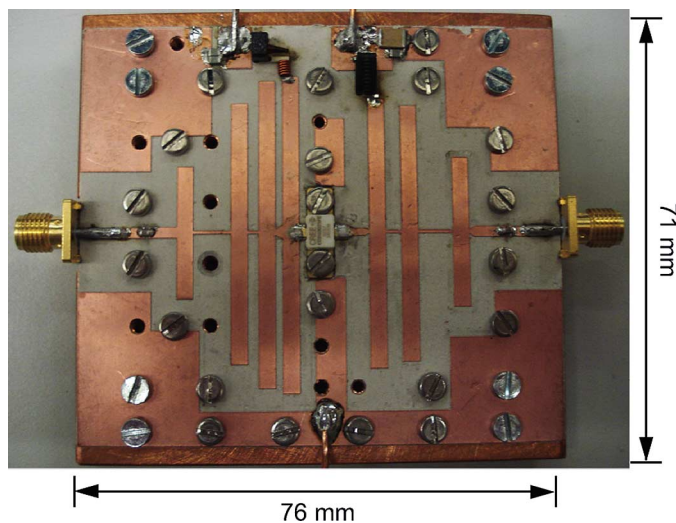


Fig. 21. Fabricated circuit of broadband Class-E PA.

threshold of -3.3 V in the measurement. The CW signal is generated by an Agilent E4433B signal generator and boosted by

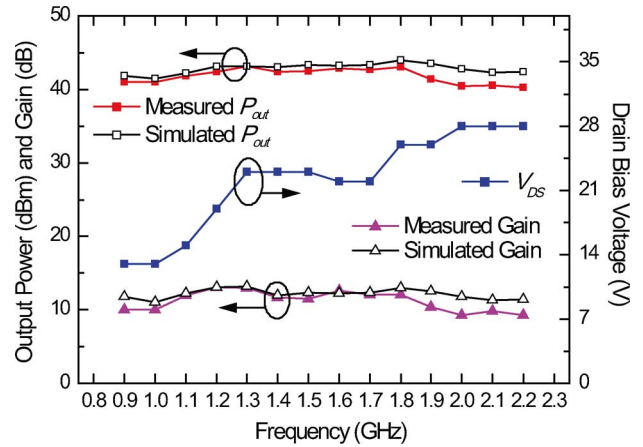


Fig. 22. Measured and simulated output power and gain across the entire bandwidth.

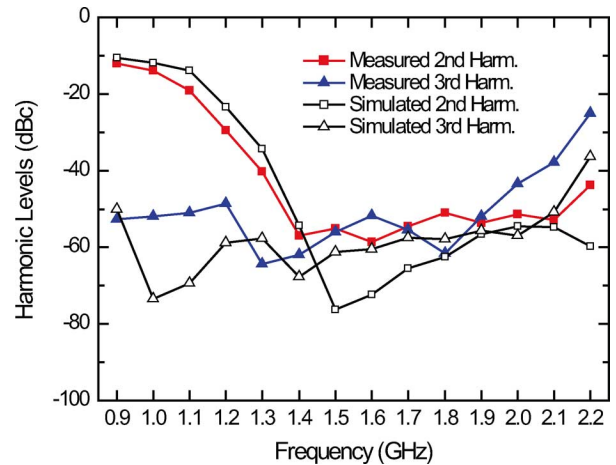


Fig. 23. Measured and simulated harmonics over the entire bandwidth.

a commercial wideband pre-amplifier (Mini-Circuits,³ ZHL-16 W-43+) to provide a sufficiently large driving power of around 31 dBm for the broadband testing. The PA output power is measured using an Agilent E4448 spectrum analyzer. Fig. 22 shows the measured and simulated fundamental output powers from 0.9 to 2.2 GHz, which are within the range of 10–20 W. The drain bias voltage (blue line in online version of Fig. 22) applied in CW testing is optimized for PAE. The same gate and drain bias voltages are applied in the simulation and measurements. The power gain of this broadband Class-E PA is also plotted in Fig. 22, which ranges from 10 to 13 dB within the entire bandwidth. The second and third harmonics are also measured using the spectrum analyzer, which are shown in Fig. 23. When operating below 1.2 GHz, the second harmonic remains significant because it falls in (or close to) the fundamental bandwidth. From 1.3 to 2 GHz, the harmonic levels fall from -40 to -60 dBc as the favorable harmonic impedances are provided by the output matching network.

Fig. 24 shows the PA efficiencies within the entire band obtained from measurements and simulation. The measured

³Mini-Circuits Corporation, Brooklyn, NY. [Online]. Available: <http://www.minicircuits.com/>

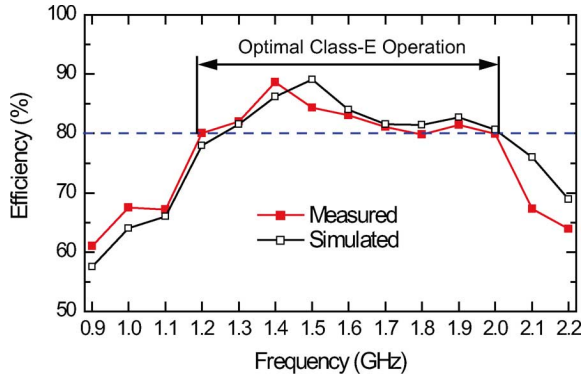


Fig. 24. Measured and simulated drain efficiency within 0.9–2.2 GHz.

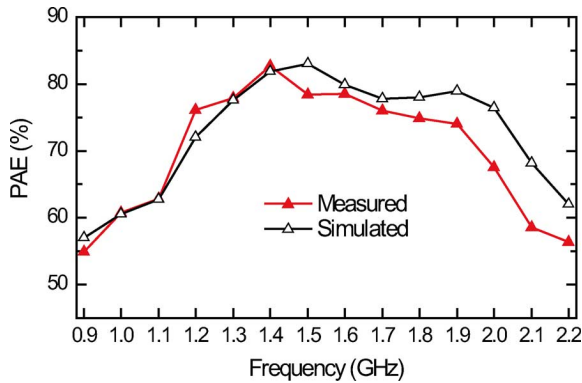


Fig. 25. Measured and simulated PAE over the entire bandwidth.

PA efficiency is above 80% between 1.2–2 GHz, which is the bandwidth for the optimal Class-E operation, as discussed in Section III-C and proven in the above Section IV. The maximum measured value is 89% at 1.3 GHz. The measured efficiency is over 60% throughout the overall bandwidth from 0.9 to 2.2 GHz. This is the highest average efficiency ($\cong 80\%$) achieved at *L*-band for such a wide bandwidth and for this power level today. In order to explain the gradual drop of efficiency from approximately 80%–89% to 60%–70% at <1.2 and >2 GHz, we need to consider the matching network performance. Specifically, the output matching network provides a suboptimal match at the fundamental frequency below 1.2 GHz. Furthermore, as already mentioned, the second harmonic level is quite high below 1.2 GHz (-15 and -20 dBc for 1- and 1.1-GHz CW signals, respectively). The same is true above 2 GHz, except that the third harmonic becomes more significant, which is possibly due to the self-resonance of the implemented components. The measured and simulated broadband PAEs are shown in Fig. 25.

The PA is also characterized under different driving levels to evaluate its dynamic performance. Fig. 26 shows the measured gain, output power, drain efficiency, and PAE at 1.6 GHz, while the input power is swept from 15 to 31 dBm. The gain compresses at $P_{in} = 24$ dBm and power-added efficiency (PAE) reaches its maximum value at the input power of 30 dBm. The PAE drops from 79% to 23% when the output power decrease from 43.5 to 30 dBm. An improved PA performance at back-off power levels can be obtained by techniques such as: 1) envelope elimination and restoration (EER) transmitters [24], [25]

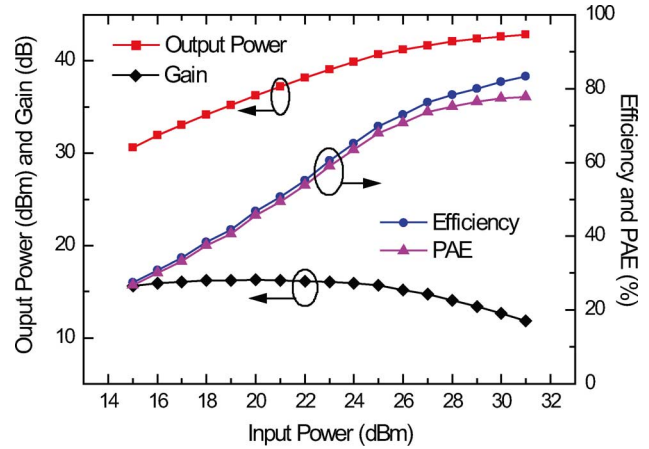


Fig. 26. Measured output power, gain, efficiency, and PAE versus input power at 1.6 GHz.

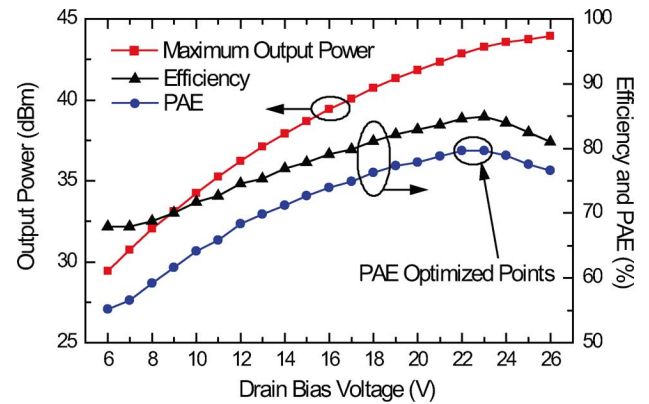


Fig. 27. Measured efficiency and output power versus drain bias voltage at 1.6 GHz.

and 2) burst-mode transmitters [26], [27], which typically apply switch-mode PAs for their efficient performance at the saturated power level. To prove this, we tested this PA under different drain bias voltages. Fig. 27 shows the maximum measured output power and efficiency versus drain bias at 1.6 GHz. It is seen that a high efficiency ($>70\%$) can be maintained within a large voltage supplying range, indicating that this PA is especially suitable for the EER/burst-mode transmitters. A maximum power of 44.5 dBm is found at the bias voltage of 26 V. A dynamic power range of 16.5 dB is achieved with the supply voltage varying from 6 to 26 V. It is also seen from Fig. 27 that the maximum PAE (79%) is yielded not at the maximum bias voltage, but at lower points of 22–23 V. This phenomenon is also observed in [12] and [15].

B. GSM Modulated-Signal Measurements

To evaluate the PA performance in an actual GSM communication system, this Class-E PA is tested using a minimum-shift keying (MSK)-modulated GSM signal with a modulation symbol rate of 500 ks/s, which has a constant envelop. This GSM signal is generated by an Agilent E4438C signal generator and is amplified to a sufficiently large driving level by the commercial PA already mentioned in Section V-A. The bias condition used in this modulated measurement is same as that ap-

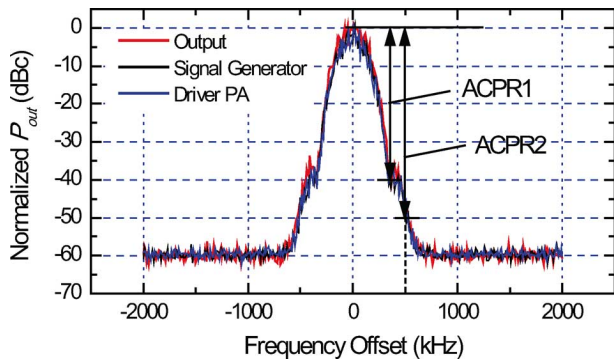


Fig. 28. Measured output spectrum from the PA, measuring with an MSK-modulated 500-kHz GSM signal centered at 1.7-GHz.

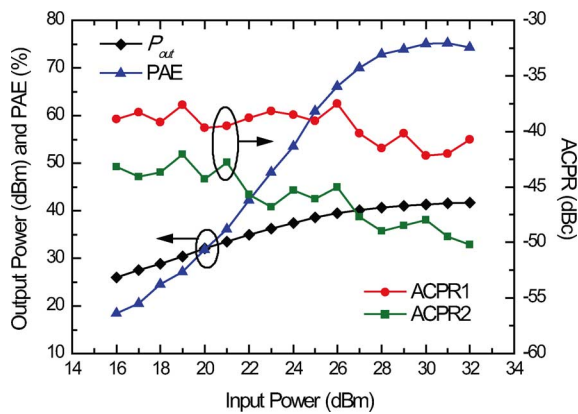


Fig. 29. Measured PA performance with a power-swept GSM signal at 1.7 GHz.

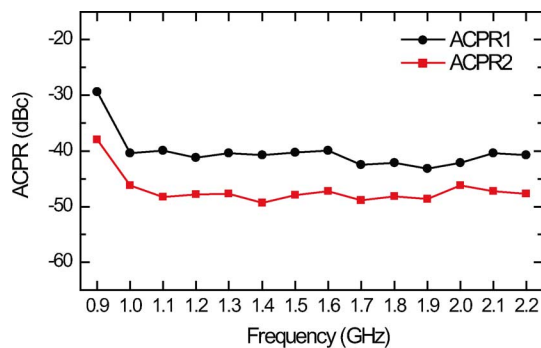


Fig. 30. Measured broadband PA linearity characterized under stimulus of a frequency-swept GSM signal.

plied in the CW testing. Fig. 28 shows the captured output spectrum at 1.7 GHz with an input stimulus of 31 dBm. Compared to the input spectrums from signal generator and driver PA, the Class-E PA is almost “distortion free” for the GSM signal. The adjacent channel power ratio (ACPR) is measured at 300- and 500-kHz frequency offsets, as illustrated in Fig. 28. Fig. 29 shows the average output power and PAE, as well as ACPR1 and ACPR2 when the input power level is swept from 31 to 16 dBm. Fig. 30 shows the ACPR1 and ACPR2 across the entire bandwidth, which are around -40 and -50 dBc, respectively.

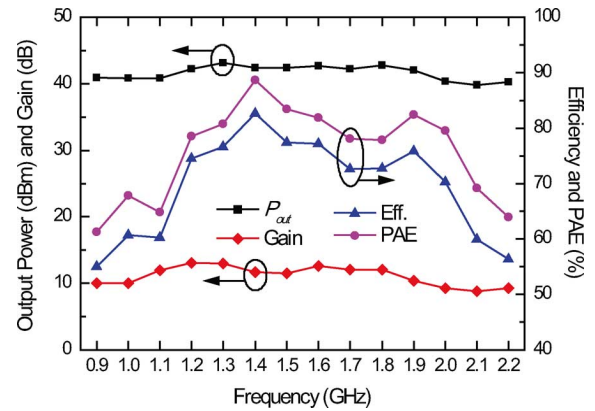


Fig. 31. Measured broadband PA performance characterized under stimulus of a frequency-swept GSM signal.

Fig. 31 plots the measured PA performance over the entire bandwidth under stimulus of the GSM signal, including average gain, output power, efficiency, and PAE, which are very close to the corresponding CW performance, as shown in Section V-B.

VI. CONCLUSION

In this paper, a practical methodology based on low-pass filter synthesis has been presented to realize a broadband Class-E PA using low-pass matching networks. A three-stage low-pass network has been synthesized and implemented for the output matching of a Cree GaN transistor, which provides broadband impedance matching for both fundamental and harmonics. The broadband Class-E operation has been demonstrated using simulated waveform engineering. An efficient PA performance has been measured across a bandwidth of 0.9–2.2 GHz (84% fractional bandwidth, centered at 1.6 GHz). It is the first time that a very high PA efficiency of $>80\%$ has been achieved over a significant bandwidth from 1.2 to 2 GHz (50%). Moreover, the measurements using modulated GSM signals reveal a good potential for application in the constant-envelope-signal communication systems.

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REFERENCES

- [1] S. C. Cripps, *RF Power Amplifier for Wireless Communications*, 2nd ed. Boston, MA: Artech House, 2006.
- [2] A. Adahl and H. Zirath, “A 1 GHz class E LDMOS power amplifier,” in *33rd Eur. Microw. Conf.*, Oct. 2003, vol. 1, pp. 285–288.

- [3] A. Dupuy, K. M. K. H. Leong, and T. Itoh, "Class-F power amplifier using a multi-frequency composite right/left-handed transmission line harmonic tuner," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2005, pp. 2023–2036.
- [4] P. Saad, H. M. Nemati, M. Thorsell, K. Andersson, and C. Fager, "An inverse class-F GaN HEMT power amplifier with 78% PAE at 3.5 GHz," in *39rd Eur. Microw. Conf.*, Oct. 2009, vol. 1, pp. 496–499.
- [5] K. Entesari, A. R. Tavakoli, and A. Helmy, "CMOS distributed amplifiers with extended flat bandwidth and improved input matching using gate line with coupled inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 2868–2871, Dec. 2009.
- [6] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "High efficiency ultra-wide-band power amplifier in GaN technology," *Electron. Lett.*, vol. 44, no. 2, pp. 130–131, Feb. 2008.
- [7] A. Sayed, A. A. Tanany, and G. Boeck, "5 W, 0.35–8 GHz linear power amplifier using GaN HEMT," in *39rd Eur. Microw. Conf.*, Oct. 2009, vol. 1, pp. 488–491.
- [8] P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A methodology for realizing high efficiency Class-J in a linear and broadband PA," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3196–3204, Dec. 2009.
- [9] M. P. van der Heijden, M. Acar, and J. S. Vromans, "A compact 12-watt high-efficiency 2.1–2.7 GHz class-E GaN HEMT power amplifier for base stations," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 657–660.
- [10] A. A. Tanany, A. Sayed, and G. Boeck, "Broadband GaN switch mode class E power amplifier for UHF applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 761–764.
- [11] D. Wu, F. Mkadem, and S. Boumaiza, "Design of a broadband and highly efficient 45 W GaN power amplifier via simplified real frequency technique," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2010, pp. 1090–1093.
- [12] P. Saad, C. Fager, H. Cao, H. Zirath, and K. Andersson, "Design of a highly efficient 2–4-GHz octave bandwidth GaN-HEMT power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 7, pp. 1677–1685, Jul. 2010.
- [13] T. B. Mader, E. W. Bryerton, M. Markovic, M. Forman, and Z. Popovic, "Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 10, pp. 1391–1398, Oct. 1998.
- [14] A. J. Wilkinson and J. K. A. Everard, "Transmission-line load-network topology for Class-E power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1202–1210, Jun. 2001.
- [15] Y. Lee and Y. Jeong, "A high-efficiency class-E GaN HEMT power amplifier for WCDMA applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 622–624, Aug. 2007.
- [16] N. O. Sokal and A. D. Sokal, "Class E—A new class of high-efficiency tunes single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 3, pp. 168–176, Jun. 1975.
- [17] E. Cipriani, P. Colantonio, F. Giannini, and R. Giofre, "Optimization of Class E power amplifier design above theoretical maximum frequency," in *Proc. Eur. Microw. Integr. Circuits Conf.*, Oct. 2008, pp. 514–517.
- [18] R. Pengelly, B. Millon, D. Farrell, B. Pribble, and S. Wood, "Application of non-linear models in a range of challenging GaN HEMT power amplifier designs," presented at the IEEE MTT-S Int. Microw. Symp. Workshop, Jun. 2008.
- [19] G. Wilkinson, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.
- [20] R. M. Fano, "Theoretical limitations on broadband matching of arbitrary impedances," *J. Franklin Inst.*, vol. 249, pp. 57–83, 139–154, Jan. 1950.
- [21] D. M. Pozar, *Microwave Engineering*, 3rd ed. Boston, MA: Wiley, 2005.
- [22] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, 1st ed. Boston, MA: McGraw-Hill, 1964.
- [23] G. L. Matthaei, "Tables of Chebyshev impedance-transformation networks of low-pass filter form," *Proc. IEEE*, vol. 52, no. 8, pp. 939–963, 1964.
- [24] K. Y. Kim, J. H. Kim, S. M. Parck, and C. S. Park, "Parasitic capacitance optimization of GaAs HBT Class E power amplifier for high efficiency CDMA EER transmitter," in *Proc. IEEE RFIC Symp.*, Jun. 2007, pp. 733–736.
- [25] K. Y. Kim, W. Y. Kim, and C. S. Park, "Dual-mode high-dynamic range class E HBT power amplifier for WCDMA EER transmitters," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 10, pp. 572–574, Oct. 2010.
- [26] P. Reynaert, "Polar modulation," *IEEE Microw. Mag.*, vol. 12, no. 1, pp. 46–51, Feb. 2011.
- [27] D. R. Parveg, P. Singerl, A. Wiesbauer, H. M. Nemati, and C. Fager, "A broadband, efficient, overdriven Class-J RF power amplifier for burst mode operation," in *Proc. 40th Eur. Microw. Conf.*, Sep. 2010, pp. 1666–1669.



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