



A low noise and power consumption, high-gain LNA in 130 nm SiGe BiCMOS using transmission lines

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Abstract

A two-stage low-noise amplifier (LNA), designed using GlobalFoundries' 130 nm SiGe BiCMOS process technology for 56 – 64 GHz applications is presented in this paper. The LNA consists of two cascode stages, with inductive degeneration using short stub transmission lines with a quarter wavelength. The input matching and output matching adopt T-section matching to ensure optimal noise and input matching, while realizing high gain over the desired frequency using the interstage and output matching. The designed LNA uses 7.6 mW of dc power from a 1.5 V supply, while achieving 22.99 dB gain and a noise figure of 4.43 dB at 60 GHz. It is unconditionally stable and has a 3 dB bandwidth of 3.9 dB across the V-band.

1. Introduction

The millimeter wave (mm-wave) band has become a point of interest for industry and academia over the last decade. The opportunity to design numerous circuits that serve in different applications has made this particular frequency range indispensable. Short-range wireless communication (60 GHz), quick download, imaging and automotive radar (76 GHz), which enhance blind spot detection and collision avoidance, are among the few developments in this area. The unlicensed 60 GHz band that offers 7 GHz bandwidth has been used in the design of a low-noise amplifier (LNA) and power amplifier lately, employing process technologies such as complementary oxide metal semiconductor (CMOS), bipolar CMOS and III-V semiconductor elements.

At the mm-wave band, more LNA circuits are built using the multi-stage approach, as a single-stage design is inefficient in meeting the expected design trade-offs. The cascode topology fits well in realizing expected design

goals [1]. This topology exhibits better stability and high reverse isolation because of the common-base transistor, improved bandwidth and high gain across the mm-wave frequency. As highlighted by [2], the output admittance of the cascode topology is quite low in comparison to the common-emitter topology because it has a low capacitive component.

The stub-matching technique, better associated with microstrip lines, offers more 3 dB bandwidth and a flat gain across the frequency of interest. Its manifestations are as series transmission line, open circuited stub or short-circuited stub. When incorporated in the design of an LNA a microstrip transmission line benefits from the lower capacitive component per unit length and offers a high impedance transmission line for reduced size matching networks [3], hence its application in the design of the LNA and its suitability for broadband design.

2. Description of Circuit

Fig. 1 shows the schematics of the LNA with the components used in the design. C_1 , C_2 , TL_1 , TL_2 and TL_3 are utilized to ensure the input matching network (IMN) of Q_1 to the source impedance of 50 Ω . TL_1 , TL_2 and TL_3 are part of the T-section input matching, with TL_4 playing an additional role in the DC biasing circuit. TL_4 and TL_9 are a degenerative component, made with a short-stub transmission line, which ensures that the optimum noise impedance is equal to the input impedance. IMN also ensures a good input reflection coefficient. C_2 and C_5 are used as the pad capacitance in the design. Capacitor C_1 and C_4 are used in the circuit preventing DC flow to the 50 Ω resistor and the collector of Q_2 . C_3 and C_6 are the decoupling capacitor terminated to the ground and connected to the bias circuit of the LNA along with TL_3 and TL_8 , ensuring that the DC power supply is isolated from the RF signal of the LNA. C_3 and C_6 are made small

in value, with sufficiently high self-resonant frequency while acting as a short-frequency to RF signal. The interstage matching consists of TL₇, TL₆, C₅ and C₄, aimed at boosting the forward gain, S₂₁ and aiding the output matching network to have an excellent reflection coefficient and a circuit that is unconditionally stable. The output matching network consist of L₂, TL₁₁, C₆ and C₇. L₂ is significant for controlling the peak resonating frequency and the peak gain value of the LNA, as it is either narrow down the S₂₁ or ensures that it peaks at a lower frequency. TL₁₀ controls the peak gain of the LNA increasing or decreasing at the same frequency. V_{CC}, the collector current, is set at 1.5 V while V_{BB1} and V_{BB2} are set at 1.2 V and 0.85 V respectively for the biasing circuit.

The transistor, Q₁, used in the input matching stage consists of a CBEB layout, with an emitter finger, two base fingers and two collector fingers. The section of the transistor was based on balancing the trade-off between obtaining optimum noise performance or high-gain performance at the input matching network. In designing the input matching, the complex conjugate of optimum noise impedance, (Z_{OPT})^{*}, is equated to the input impedance, Z_{IN} of the LNA, where the normalized value of Z_{OPT} is 1.537 + j1.0862. Similarly, the source impedance Z_S is equated to the source impedance, Z_S of 50 Ω.

An inductive degenerative emitter is designed by using a shunted stub of quarter-wave length while the T-section matching network along with the pad capacitance and the input capacitance is used to realize optimal input and noise matching. The shunted stub is about 80 degrees at 60 GHz. A quarter-wave length transmission line [4] is known for a high Q-factor and a means of reducing the noise figure in the LNA. The pad capacitance is of great advantage in the on-chip or off-chip design, since any matching characteristics of the IMN would not be altered even when the pad capacitance is disconnected [5]. The DC-blocking capacitor, C₁ connected at the input of the IMN restrains DC from the 50 source resistance.

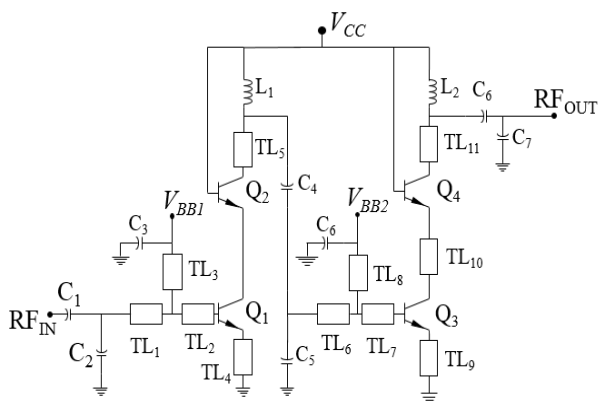


Figure 1. Circuit schematic of the developed V-band LNA at 60 GHz.

The matching of the interstage was established by equating

the complex conjugate of the input impedance (Z_{IN})^{*} to the output impedance, Z_{OUT}. The IMN consists of a series DC-block capacitor, a parallel capacitance pad and T-section matching. The T-section consists of three transmission lines of quarter-wave length; the third is used as a component in the bias network. The bias network consists of a decoupling capacitor connected in parallel with a transmission line. The selection of C₁ is such that it self-resonates at the operating frequency of 60 GHz. The bias circuit is supplied with a V_{BB2} of 0.85 V source, which is adequate for biasing Q₃ at the base.

The output matching of the LNA is designed to yield maximum gain. Although the degenerative emitter is terminated with a short-circuited shunt stub, it is necessary to minimize the noise at the second stage, since the variation of V_{BE} in biasing the LNA differs slightly. An inductor is connected between the collector of Q₃ and emitter of Q₄ to ensure a broad bandwidth for the LNA. The collector voltage, V_{CC}, is connected to Q₂ and Q₄ via the collector terminal with a voltage of 1.5 V to bias the base of Q₂ and Q₄.

3. Result and Discussion

The LNA was designed and simulated using 130 nm SiGe HBT BiCMOS GlobalFoundries' technology process. Fig. 2 shows the simulated S-parameter plot of input return loss, S₁₁ and output return loss, S₂₂. S₁₁ and S₂₂ are better than 4 db between 56.2 dB to 63 dB, while S₂₂ is better than 4 dB between 59 dB and 62 dB. Improving the values of S₁₁ and S₂₂ would result in a situation where the gain increases, but with a smaller 3 dB bandwidth.

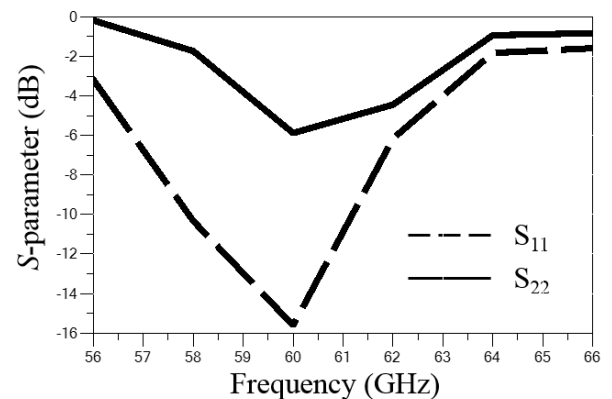


Figure 2. Simulated S-parameter: S₁₁ and S₂₂ plot across the desired frequency band, resonating at 60 GHz.

With the above simulated values of S₁₁ and S₂₂, a simulated peak gain of 22.99 dB was attained at 60 GHz, with a 3 dB bandwidth between 57.5 and 61.4 dB as depicted in Fig. 3.

Table 1: 130 nm SiGe BiCMOS LNA PERFORMANCE COMPARISON WITH STATE-OF-THE-ART LNAs

	[5] LMWC	[6] PIERS	[7] AICSP	[8] CDS	[9] EuMC	[This work]
Technology	0.18 μm BiCMOS	90 nm CMOS	90 nm CMOS	SG 25H1 (IHP)	90 nm CMOS	130 nm BiCMOS
Topology	Cascode (3 stages)	CS (2 stages)	CS + Cascode + CS	Cascode (2 stages)	Cascode (2 stages) + CE	Cascode (2 stages)
Gain (dB)	29.5	18.1	11.4	20	22	22.99
Power (mW)	11.7	32.6	14.1	7.3	13.5	7.6
Bandwidth (3 dB)	24	4.4	12.5	4 ¹	4 ¹	3.9
NF	6	6.3	3.88	6.0	3.7	4.43

¹ Estimated Values

Fig. 3 shows a plot of the stability factor, K , S_{21} and the noise factor of the LNA. The LNA is unconditionally stable across the frequency of interest, i.e. 56 – 64 GHz as the value of K is above 5. 4.43 dB and 22.99 dB values of noise figure and gain were achieved for the LNA. The noise across the frequency of interest ranges from 5.26 to 7.00 dB, with the lowest attained at 60 GHz. Table 1 shows a comparison of the recently reported V-band LNA's having a relatively wide bandwidth.

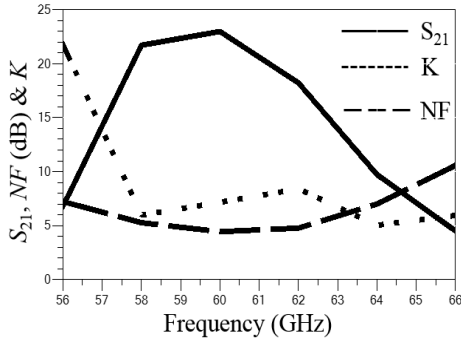


Figure 3. Plot of simulated S_{21} , stability factor, K and NF of the LNA for V-band.

The figure of merit (FOM), which contains the central RF front-end LNA parameters such as gain, S_{21} , and NF is the expected noise figure, BW is the 3 dB bandwidth, and P_D , the dissipated power, is displayed in [1]:

$$FOM = \frac{Gain \times BW [GHz]}{(NF - 1) \times P_D [mW]} \quad [1]$$

Based on [1], the FOM of the designed LNA is 3.44 GHz/mW. The improvement of FOM can be achieved by increasing the bandwidth, especially the 3dB bandwidth

4. Conclusion

A low NF, high-gain LNA across the V-band was presented using the 130 nm SiGe BiCMOS process technology. About 75 percent of the component utilized was a quarter-wave length transmission line, aimed at reducing parasitic capacitance at 60 GHz. The LNA was designed using a two-stage cascode topology with degenerative emitter to reduce the NF of the LNA. The LNA was biased at an optimal point to reduce the NF of the circuit significantly.

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6. References

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