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Reliability prediction with MTOL

Joseph B. Bernstein, Alain Bensoussan, Emmanuel Bender *

A B S T R A C T

Here, we develop a comprehensive reliability prediction of FPGA devices from data motivated by physics of failure. The Multiple Temperature Operational Life (MTOL) testing method was used to calculate the failure in time (FIT) of 3 different mechanisms on both 45 nm and 28 nm technologies. We confirmed that there is significant hot carrier injection (HCI) at sub-zero temperatures in 45 nm technology. Surprisingly, we found that 28 nm exhibits no HCI degradation even with up to 1.6 V on the core. As a result, we show that there is no effect of frequency on the reliability. This means that at 28 nm and possibly smaller technologies, the devices can be de-rated or up-rated based only on the NBTI model and therefore reliability is dependent only on operating Voltage and Temperature with a single activation energy. Notably, the activation energies and voltage acceleration factors for both technologies are remarkably similar. This demonstration shows that, unlike other conventional qualification procedures, the MTOL testing procedure gives a broad description of the reliability from sub-zero to high temperatures. This procedure provides FIT prediction which can be applied to newer technologies, specifically 20 nm and 16 nm and beyond.

Keywords:
Microelectronics reliability
Ring oscillators
Accelerated testing

1. Introduction

The key innovation of the Multiple-Temperature Operational Life (MTOL) testing method is its success in separating different failure mechanisms in devices in such a way that actual reliability predictions can be made for any user defined operating conditions. This is opposed to the common approach for assessing device reliability today, using High Temperature Operating Life (HTOL) testing [1], which is based on the assumption that just one dominant failure mechanism is acting on the device [2]. However, it is known that multiple failure mechanisms act on the device simultaneously [3]. The new approach, MTOL, deals with this issue [4] (in that paper, we called it M-HTOL). This method predicts the reliability of electronic components by combining the Failure in Time (FIT) of multiple failure mechanisms [5]. Degradation curves are generated for the components exposed to accelerated testing at several different temperatures and core stress voltage. Our data clearly reveals that different failure mechanisms act on the components in different regimes of operation causing different mechanisms to dominate depending on the stress and the particular technology. A linear matrix solution, as presented in [5], allows the failure rate of each separate mechanism to be combined linearly to calculate the actual reliability as measured in FIT of the system based on the physics of degradation at specific operating conditions.

In this article, we present experimental results of the MTOL method tested on both 45 and 28 nm FPGA devices from Xilinx that were processed at TSMC (according to the Xilinx data sheets). The FPGAs were tested over a range of voltages, temperature and frequencies. We measured ring frequencies of multiple asynchronous ring oscillators simultaneously during stress in a single FPGA. Hundreds of oscillators and the corresponding frequency counters were burned into a single FPGA to allow monitoring of statistical information in real time. Since the frequency itself monitors the device degradation, there is no recovery effect whatsoever, giving a true measure for the effects of all the failure mechanisms in real time.

Our results produced an acceleration factor (AF) for each failure mechanism as a function of core voltage, temperature and frequency. The failure rates of all of the mechanisms were then combined using a matrix to normalize the AF of the mechanisms to find the overall Failure in Time or FIT of the device. In other words we found an accurate estimate of the device lifetime and thus the reliability that can be conveniently transposed to other technologies and ASICs and not necessarily only FPGAs.

2. MTOL testing system

The FPGA configuration designed for the MTOL testing consists three main parts: (1) Accelerated Element (FPGA Chip); (2) Measurement system (Binary Counter); (3) Control & communication interface to a PC (see Fig. 1). The test systems consisted of two development boards containing either a Xilinx XC6SLX9 Spartan 6 FPGA (45 nm) built on a Mojo® board or a Zynq-7000 FPGA (28 nm) built on a Zybo® board.

* Corresponding author.
E-mail address: ebr248@gmail.com (E. Bender).

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The Spartan 6 uses TSMC's 45 nm low power process for 1.2 V core voltage and the Zynq-7000 FPGA is from high-K metal gate (HKMG) high performance low power (HPL) process that is optimized for 1.0 V core voltage. The devices contain over 9000 logic cells (LUTs), and the programs were designed to cover the full scope of the device's components. The devices included inputs for reference signals, testing points, and a micro-USB interfaces. In order to allow various voltage levels, an external DC power supplies delivered voltage to the FPGA cores after overriding the internal voltage controls in the board. We monitored the device temperature both internally and externally using an IR camera and internal temperature measurements.

2.1. The accelerated element

The accelerated element ran with several different frequencies, allowing independent measurements of the degradation effects over time as a function of frequency. In order to create a measurable accelerated system, Ring Oscillators (ROs) consisting of inverter chains were constructed (shown in Fig. 2). The frequency of each RO is given by: $1/2\ N\ T_p$, where N is the number of inverters and T_p is the time propagation delay per inverter. Each inverter chain was implemented as a complete logical cell using predefined Xilinx primitives and thus each ring oscillator was made up of the basic components of the FPGA. When degradation occurred in the FPGA, a decrease in performance and frequency of the RO could be observed. For optimal testing and chip coverage, different sized ROs were selected, ranging from 3 inverters, giving the maximum frequency possible in accordance with the intrinsic delays of the FPGA employed (400–700 MHz), and up to 4001-inverter oscillators, giving a much lower frequency (around 200 KHz). The system implemented on the chip starts operating immediately when the FPGA core voltage is connected. This allows seeing the frequency dependence of the failure mechanisms without any recovery effect.

2.2. The control system

The control system includes a programmable multiplexer (MUX), which switches between the various RO sampled outputs. Each cycle transfers a different RO for measurement and a communication controller that connects to a PC. The control system communicates with the computer via a USB connection with a simple serial protocol. The data received from the board is saved on a file in the computer in .csv format to be editable using a standard data processing program such as Excel.

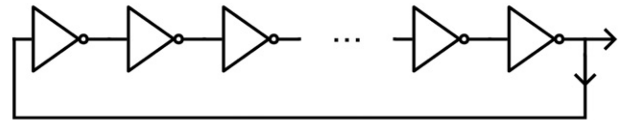

Fig. 2. Ring Oscillator is made of 2N + 1 Inverters connected in a chain.

2.3. The counter

Frequency measurements were carried out from a crystal on the board. For high-resolution measurements, a 32-bit counter was chosen. Assuming the highest available frequencies to be around 700 MHz, a Reference Clock signal of 9 Hz was fed into the FPGA. The reference signal was generated outside of the FPGA (and the accelerated environment) allowing as accurate measurements as possible. The reference signal is also returned to the exterior in order to verify that the measurement remains accurate throughout the experiments.

2.4. Testing methods

The test conditions, i.e. voltage, temperature levels defined in a test plan for imposing an acceleration of individual mechanisms to dominate others at each applied condition. For example, testing in sub-zero temperatures and high voltages, will exaggerate HCI for high frequency [6,7] but very low degradation due to BTI [8].

For each test, the FPGA board was placed in a temperature-controlled oven, similar to those used in HTOL-testing, with an appropriate voltage connected at the FPGA core from an external supply. The board was connected to a computer via USB cables. The tests were performed for 100–200 h, while the device was operating at accelerated voltage conditions - the frequencies of 140 Ring-Oscillators of different sizes were sampled every 5 min [9]. The measured data was stored in a database from which one could draw statistical information about the degradation in the device performance.

The particular testing conditions were chosen to isolate each failure mechanism allowing examination of the specific effect of that mechanism on the system and thus define its unique physical characteristics. A close inspection of the results in comparison to one another yielded

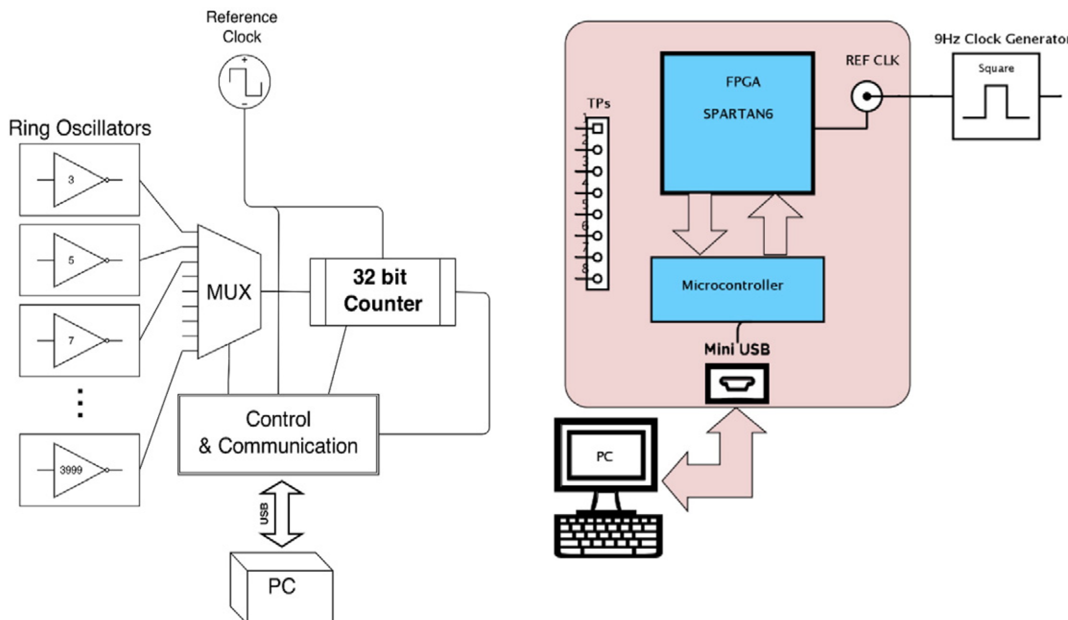

Fig. 1. Testing setup consisting of Ring oscillators, counter and communication.

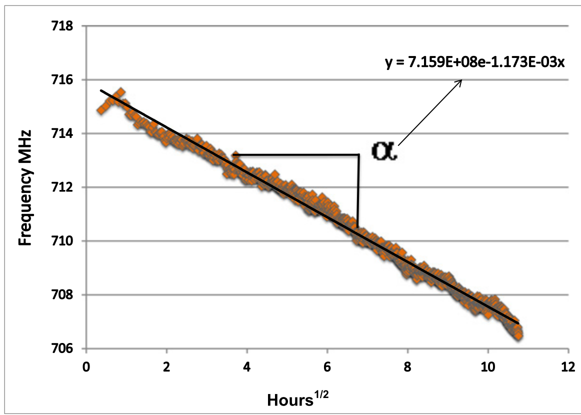

Fig. 3. Typical graph showing frequency versus square root of time showing degradation slope, α.

more precise parameters for the Acceleration Factors (AF) equations and allowed adjusting them to fit all the devices under test [10].

Finally, after completing the tests, some of the experiments with different frequency, voltage and temperature conditions were chosen to construct the MTOL Matrix. The calculated FIT was then plotted as a function of temperature and frequency for every operating voltage. Since the FIT calculation is, in essence, an average of a large number of devices (10^7 transistors), assuming the Poisson model we can postulate that the standard deviation is equal to the time to fail.

3. Separating failure mechanisms

The common intrinsic failure mechanisms affecting electronic devices are, Hot carrier Injection (HCI), Bias Temperature Instability (BTI), Electromigration (EM) and Time Dependent Dielectric Breakdown (TDDB). In our tests, no signature of TDDB was observed. This result is not surprising considering that in other accelerated test results on comparable technologies TDDB is only observed in voltages higher than 1.6 V [11]. The standard models for failure mechanisms in semiconductor devices are classified by JEDEC Solid State Technology Association and listed in publication JEP-122G [12]. The failure mechanisms can be separated due to the difference of physical nature of each individual mechanism.

4. EA and γ extrapolation

Our tests for various mechanisms included exposing the core of the FPGA to accelerating voltages above nominal. 45 nm defines the nominal voltage at 1.2 V and for 28 nm, 1.0 V. Our method of separating mechanisms allowed the evaluation of actual activation energies for the three failure mechanisms detailed above. We plotted the degradation in frequency and attributed it to one of the three failure mechanisms as will be explained further on.

The results of our experiments give both E_A and γ for the three mechanisms we studied at temperatures ranging from −50 to 150 °C. The Eyring model [13] is utilized here to describe the Failure in Time

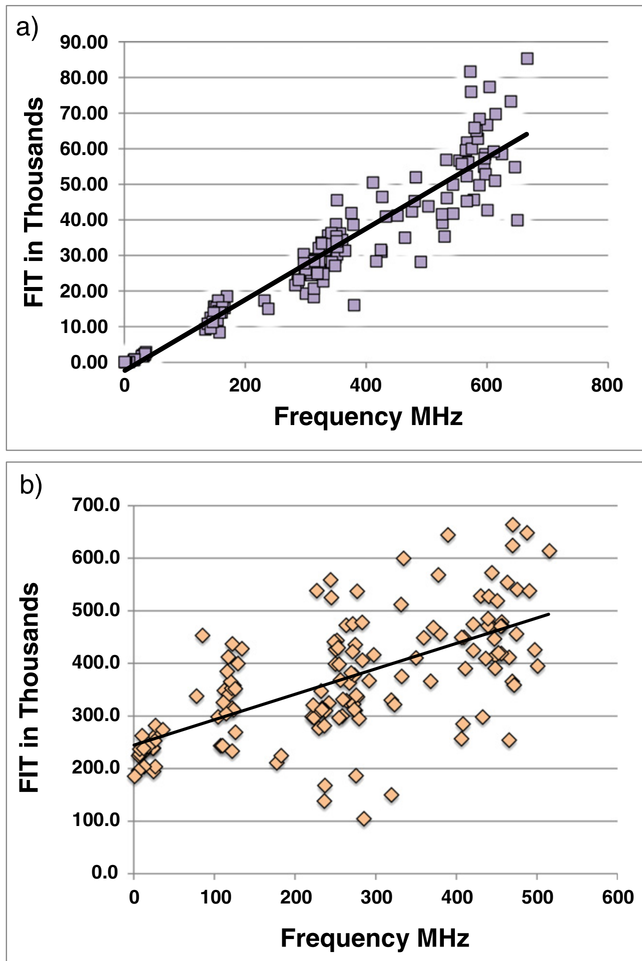

Fig. 4. Failure rate, FIT/1000, versus frequency in MHz for a) HCI, stressed at −35 °C with 2.0 V core voltage and b) BTI, stressed at 145 °C with 2.4 V at the core.

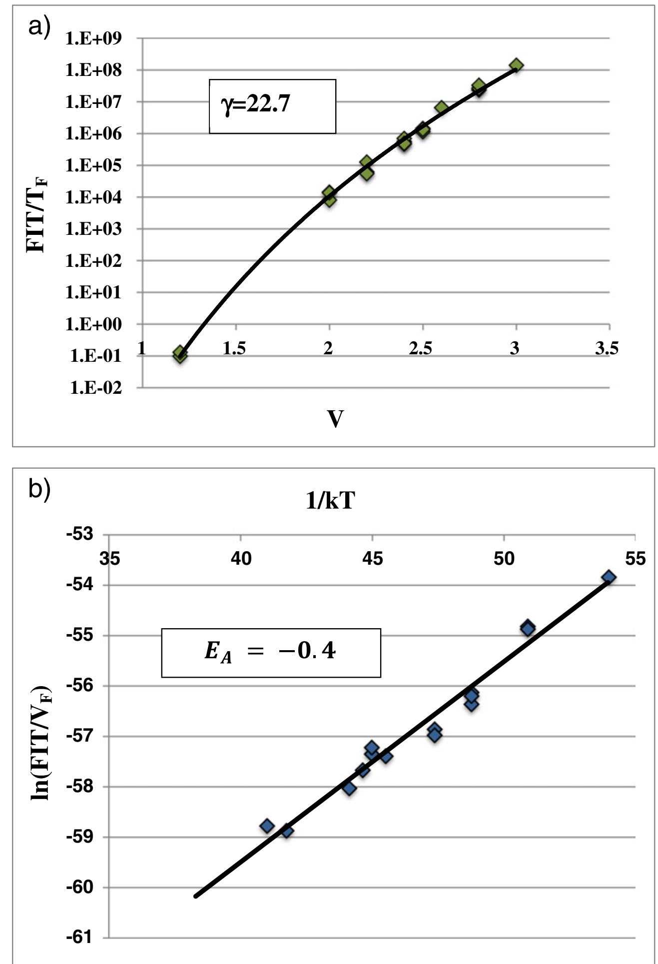

Fig. 5. a Gamma plot for HCI at 45 nm. b Activation energy plot for HCI at 45 nm.

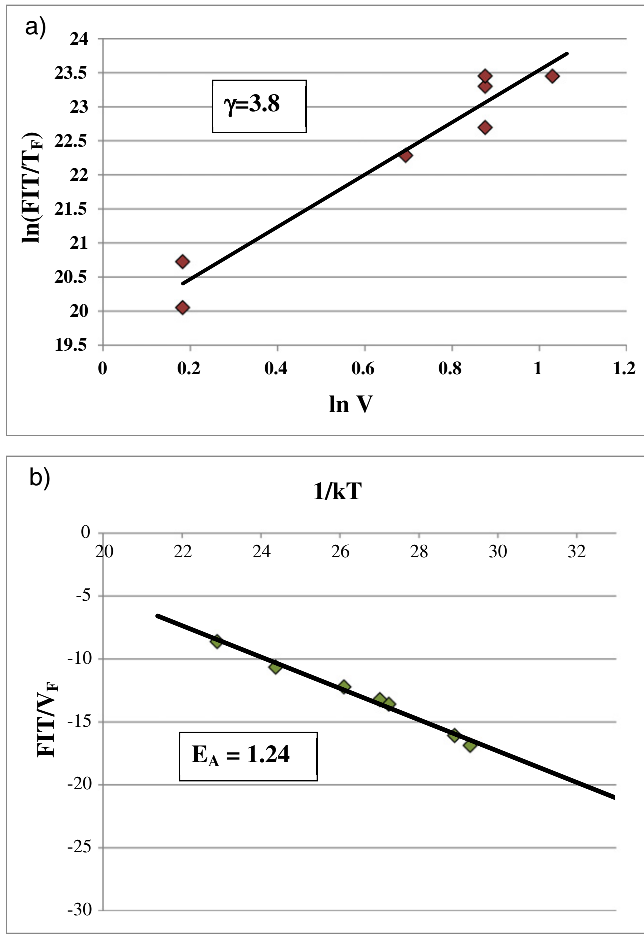

Fig. 6. a Gamma plot for EM at 45 nm. b Activation energy plot for EM at 45 nm.

(FIT) for all of the failure mechanisms. This model, using a simple constant rate (1-parameter) Poisson function, conserves strict linearity. Any additional terms would be non-linear and invalidate the Matrix. This linear, constant failure rate, approximation is born out of the observation that the statistical variability across the chip converges to the constant rate, Poisson process, allowing the linear matrix calculations to hold. The specific constant failure rate of each failure mechanisms, calculated as Failure-in-time (FIT) follows these formulae:

$$FIT_{HCI} = fV^{\gamma_{HCI}}e^{-\frac{Ea_{HCI}}{kT}} \quad (1)$$

$$FIT_{BTI} = e^{\gamma_{BTI}V}e^{-\frac{Ea_{BTI}}{kT}} \quad (2)$$

$$FIT_{EM} = fV^{\gamma_{EM}}e^{-\frac{Ea_{EM}}{kT}} \quad (3)$$

The degradation slope, α, is measured as the degradation from initial frequency as an exponential decay, approximated by taking the difference in frequency, divided by initial frequency over the time. In our experiments, we found that when the decay was dominated by BTI, the decay was proportional to the 4th root of time, while HCI and EM, being diffusion related mechanisms, have decay that is proportional to the square root of time [14], as seen in Fig. 3. This result is consistent with literature and with the JEDEC document that lists the failure mechanisms, JEP-122G [12].

For each oscillator, the ring frequency was measured and plotted against the square root of time in 45 nm devices. The slope, α, was then converted to a FIT for each test as determined by extrapolating the degradation slope to 10% degradation from its initial value. One FIT is defined as 1 failure in 10^9 part-hours [13]. Each set is plotted as an exponential decay dependent on the square root of time as shown by example in Fig. 3. This slope is then used to find the time to fail as seen in the development of FIT below (4–7).

$$\alpha_{(slope)} = \frac{\Delta f}{f_0 \times \Delta\sqrt{t}} \quad (4)$$

$$TTF = \left({}^{10\%}\big/_{\alpha}\right)^2 \quad (5)$$

$$FIT = {}^{10^9}\big/_{TTF} \quad (6)$$

$$FIT = 10^9(10 * \alpha)^2 \quad (7)$$

This makes our FIT easy to calculate, since FIT is defined as:

$$FIT = \frac{10^9}{MTTF} \quad (8)$$

where *MTTF* is the mean time to fail in hours.

The time to fail (TTF) for each point was then calculated as the square of the inverse slope times the failure criterion, which is 10% degradation [13]. Hence, the FIT for each slope is simply determined as the $(10*\alpha)^2$. The average FIT is the metric to determine the reliability since that corresponds to the MTTF in Eq. (8). This FIT value is plotted as a function of the frequency in order to determine the failure mechanisms and to fit the model parameters for each mechanism. Two typical degradation plots taken from 45 nm tests are shown in Fig. 4, the FITs, determined by the slopes, are plotted against frequency in two different experiments. The data demonstrates the clear advantage of RO generated frequencies in a single chip [15]. In the examples of Fig. 4, we see the HCI effect at a temperature of −20 °C and voltage of 2.0 V in 4a),

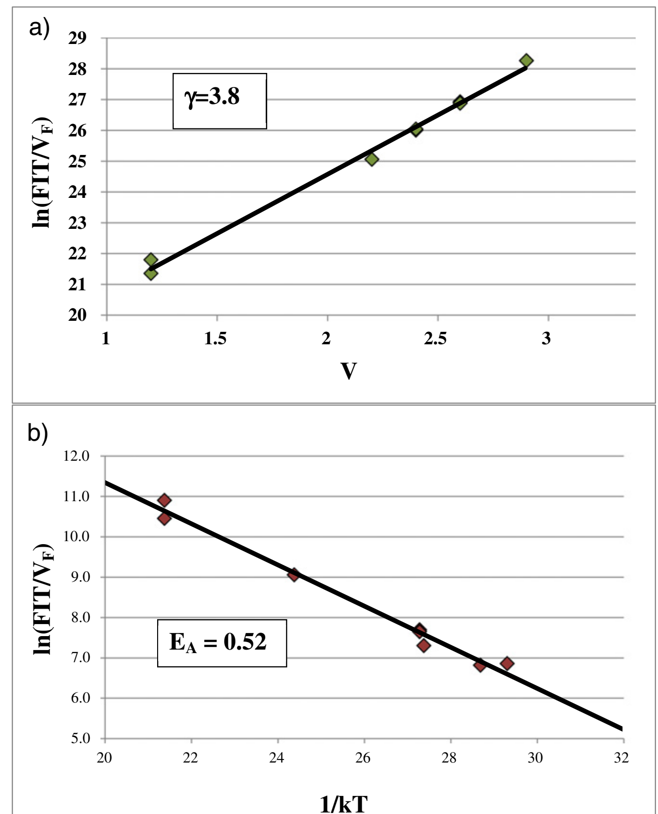

Fig. 7. a Gamma plot for BTI at 45 nm. b Activation energy plot for BTI at 45 nm.

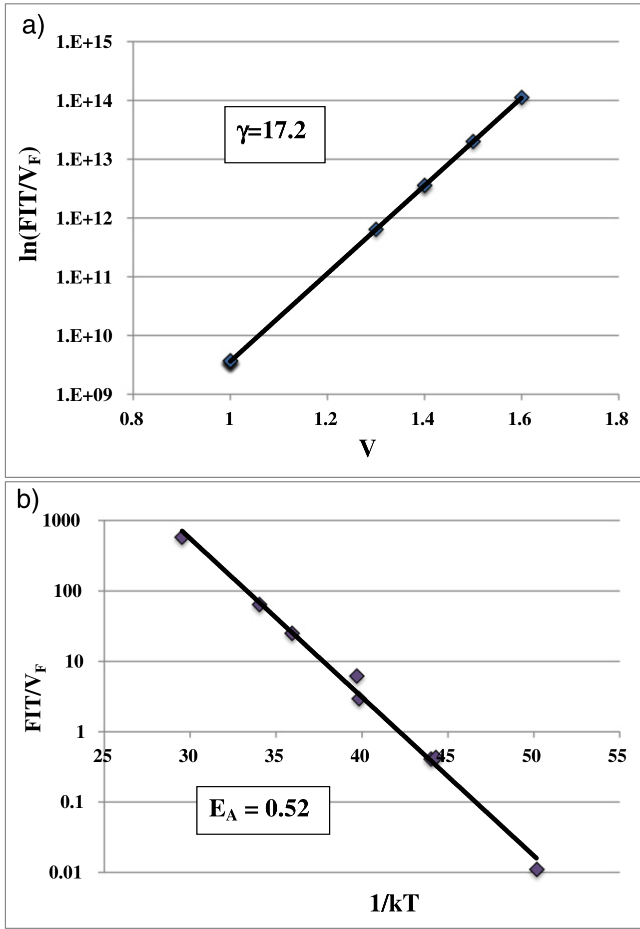

Fig. 8. a Gamma plot for BTI at 28 nm. b Activation energy plot for BTI at 28 nm.

showing FIT that is directly proportional to frequency [16], consistent with Eq. (1). Fig. 4b) shows a chip that was stressed at high voltage (2.4 V) and high temperature (150 °C) showing a strong BTI degradation at low frequency and a much shallower slope due to EM caused by an increase of effective resistance and therefore a frequency dependent effect [17]. Such curves were made for each experiment, incorporating all the oscillators across the chip spanning the range of frequencies, reflecting also the averaging effect of the longer chains. Hence, the variability is much lower than at higher frequencies, demonstrating that the averaging of many variations results in a consistent mean degradation. This strengthens credibility of modeling the failure mechanisms with equations [1–3] since the data shows a clear Poisson statistical nature. The slope of FIT versus frequency is then related at low temperatures as occurring only from HCI while at higher voltages and temperatures, it can be due to BTI [18] and EM. BTI is only responsible for low frequency degradation [19].

In order to determine the dependence of each mechanism, the activation energy as relating to the temperature factor (T_F) and voltage acceleration factors (V_F) are determined from Eqs. (1)–(3). The result of FIT versus V, T and F are plotted as follows. HCI voltage constant γ was found by plotting FIT/T_F versus V as seen in Fig. 5a. Fig. 5b shows the FIT/V_F versus 1/kT looking only at temperatures below 5 °C in order to determine the activation energy, E_A. Since both plots depend on each other, the two are performed simultaneously, where E_A is used to determine T_F, where:

$$T_F = e^{\frac{-E_a}{kT}} \tag{9}$$

$$V_F = V^{\gamma} \text{ for HCI and EM and } V_f = e^{\gamma V} \text{ for BTI} \tag{10}$$

Hence, we were able to find the correct activation energy simultaneously with its corresponding voltage factor. Our procedure was followed for all three mechanisms for the 45 nm as well as the 28 nm devices. In the 28 nm device, there was no apparent effect from HCI or EM. That is to say that no slope was found versus frequency. This is in contrast with the 45 nm devices, showing frequency related effects at both low temperatures due to HCI and a minor EM effect at high temperatures [20].

The E_A and γ for HCI are plotted in Fig. 5a and b as found in 45 nm. The plots for EM are shown in Fig 6a and b while the BTI curves are shown in Fig. 7a and b for 45 nm devices and in Fig. 8a and b for the 28 nm BTI effect. The constants are summarized in Table 1.

Table 1
Summary of E_A and γ from the curve fits.

	E_A 45 nm (eV)	γ 45 nm	E_A 28 nm (eV)	γ 28 nm
HCI	−0.4	22.7		
BTI	0.52	3.8 V^{-1}	0.52	17.2 V^{-1}
EM	1.24	3.8		

5. MTOL matrix

Now that we have fully characterized the physics of failure models relating to all three mechanisms for both 45 and 28 nm FPGA's, we were able to build the Matrix Model by choosing three points, one from each mechanism, and them solve the Eqs. (1)–(3) against the measured FIT for each condition. In the 45 nm device experiments, we chose the following data shown in Table 2. The relative factors that solve the matrix are shown in Table 3.

Table 2
T, V, F and matrix versus measured FIT.

T °C	V	F(GHz)	HCI	BTI	EM	FIT
153	1.2	1	1.71E+6	6.73E−05	4.27E−15	3672
−35	2.5	0.5	4.7E+16	1.30E−07	8.96E−26	2.37E+7
154	1.2	0	0	6.96E−05	0	2420

The procedure for finding the results of the matrix is described in previous papers [2,4,5]. This matrix has then used to construct the full reliability profile whereby FIT is calculated versus Temperature for several conditions, as shown in Fig. 9.

The same curve has been made for the 28 nm technology node.

The most notable differences between 45 and 28 nm is the lack of frequency effect at both low and high temperature, leaving only one, dominant, failure mechanism at 28 nm (Fig. 10). The consequence seems to be that there will be significantly improved reliability at low temperatures using 28 nm technology. Furthermore, there is no effect on frequency related to the reliability. Hence, there is no purpose for frequency de-rating using this technology. It is also clear that cooling the device is the major challenge and most important part of increasing the reliability of devices made using this technology [21]. Another observation is that the voltage acceleration is much greater at 28 nm, γ being over 17, as compared to 3.8 for 45 nm technology. This means that the core voltage is much more sensitive and a much greater

Table 3
Relative weighting factors that solve the matrix.

HCI	5.03873E−10
BTI	34761994.46
EM	3.11618E+17

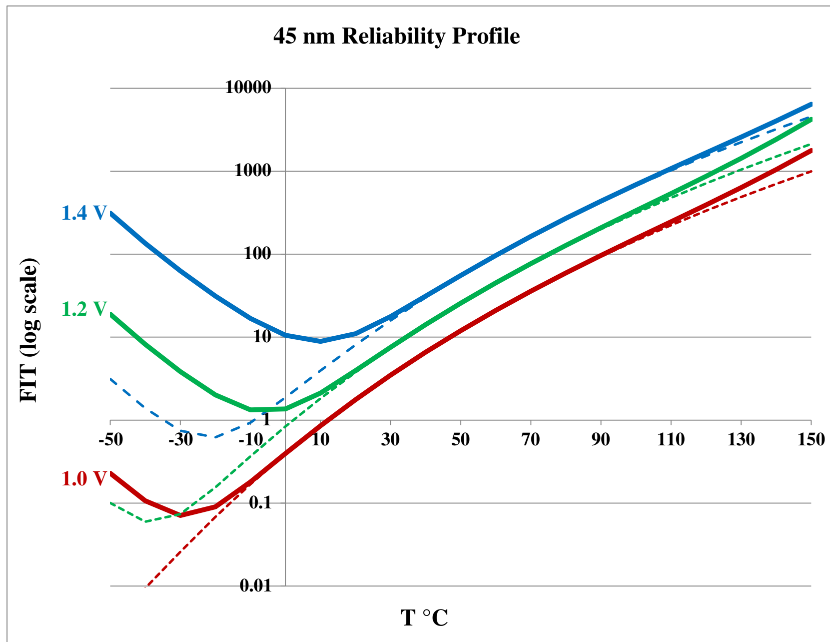

Fig. 9. Reliability curves for 45 nm technology showing FIT versus Temperature for Voltages above and below nominal (1.2 V) and frequencies from 10 MHz (dashed line) to 2 GHz (solid line).

reliability advantage would be gained by lowering the voltage. The temperature effect is exactly the same for both technologies.

One speculation as to the reason there are no hot carrier effects in the 28 nm technology is that the mean free path of electrons transported through the gate is larger than the gate length below a certain temperature. This would suggest that the electrons are transported by ballistic means below that temperature due to the properly strained channels. Hence, electrons are not able to accelerate to the point of causing damage due to HCI [22]. Data of normalized RO frequency (F/F0), versus temperature supports this claim. The 28 nm devices have a distinct transition at a particular temperature (around 60 °C), whereas the 45 nm devices have not shown any transition along the entire range of temperatures. This observation will be expanded and reported in a later study. At higher temperatures, both 45 and 28 nm devices have similar slopes. This correlates with published data attributing the transistor channel conductance to the effect of "short channel ballistic conductance" at lower temperatures [23]. In order to validate the findings detailed above, the cause of this phenomenon is being further researched in our laboratory. We have yet to see if this is true for smaller technology, but it seems that this may be an important result justifying a preference to use newer scaled technology in high-reliability applications even over older technology that may seem more mature. Radiation and thermal cycles were not studied here and can also be subjects for future investigation.

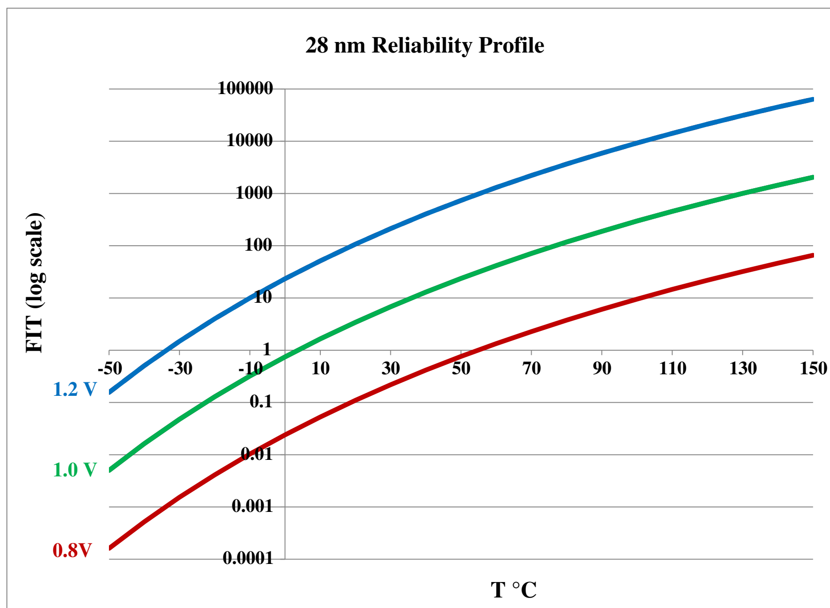

Fig. 10. Reliability curves for 28 nm technology showing FIT versus Temperature for Voltages above and below nominal (1.0 V).

6. Summary

In this research, we show an innovative and practical way to use the various physics of failure equations together with accelerated testing for reliability prediction of devices exhibiting multiple failure mechanisms. We presented an integrated accelerating and measuring platform to be implemented inside FPGA chips, making the MTOL testing more accurate, allowing these tests at the chip and perhaps at the system level, rather than only at the transistor level. The calibration of physics models with highly accelerated testing of complete commercial devices allows for actual reliability prediction. The MTOL Matrix can provide information about the proportional effect of each failure mechanism; allowing extrapolation of the expected reliability of the device under various conditions.

This practical platform can be implemented on almost any FPGA device and technology to enable making FIT calculations and reliability predictions. The results of this approach provide the basis for improvements in performance and reliability given any design or application. This method can be extended to other processes and new technologies, and can include more failure mechanisms, thus producing a more complete view of the system's reliability.

Research areas include thermal, mechanical, and electrical interactions of failure mechanisms of ultra-thin gate dielectrics, Non-volatile memory, advanced metallization and power devices. He also works extensively with the semiconductor industry on projects relating to failure analysis, defect avoidance, programmable interconnect used in Field Programmable Analog Arrays and repair in microelectronic circuits and packaging.

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Professor Joseph B. Bernstein specializes in several areas of nano-scale micro-electronic device reliability and physics of failure research, including packaging, system reliability modeling, gate oxide integrity, radiation effects, Flash NAND and NOR memory, SRAM and DRAM, MEMS and laser programmable metal interconnect. He directs the Laboratory for Failure Analysis and Reliability of Electronic Systems, teaches VLSI design courses and heads the VLSI program at Ariel University. His Laboratory is a center of research activity dedicated to serving the needs of manufacturers of highly reliable electronic systems using commercially available off the shelf parts. Professor Bernstein was a Fulbright Senior Researcher/Lecturer at Tel Aviv University in the Department of Electrical Engineering, Physical Electronics. Professor Bernstein is a senior member of IEEE.

Dr. Alain Bensoussan is Doctor Engineer and Docteur d'Etat in Applied Physics and his field of expertise is on microelectronic parts reliability at Thales Alenia Space. He is now full time seconded at Institut de Recherche (IRT) Saint Exupery, (Aeronautic, Space and Embedded Systems - AESE), Toulouse (France) as Technical Referent for micro-electronic and photonic components reliability and recognised at Thales Alenia Space as Expert on optics and opto-electronics parts. Dr. Alain Bensoussan interests lie in several areas in microelectronics reliability and physics of failure applied research on GaAs and III-V compounds MMIC (monolithic microwave integrated circuits), microwave hybrid modules, Si and GaN transistors, IC's and Deep-Sub-Micron technologies, MEMS and MOEMS, active and passive optoelectronic devices and modules. He represented Thales Alenia Space at EUROSPACE organization, nominated by this organization to support the Space Components User interests at ESA - PSWG (European Space Agency - Parts Policy and Standards Working Group) since more than 15 years.

Emmanuel Bender is a research member of the Microelectronics Reliability Laboratory in Ariel University, Israel. He finished his B.Sc. in Applied Physics in Lev Academy in Jerusalem, Israel. He is a master's student of Electrical Engineering at Ariel University.