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Flexible Oxide Thin Film Transistors: Fabrication and Photoresponse

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A young, but earnest Zen student approached his teacher, and asked the Zen master: "If I work very hard and diligently, how long will it take for me to find Zen?"

The master thought about this, then replied, "Ten years".

The student then said, "But what if I work very, very hard and really apply myself to learn fast. How long then?"

Replied the master, "Well, twenty years".

"But, if I really, really work at it, how long then?" asked the student.

"Thirty years", replied the master.

"But, I do not understand", said the disappointed student. "At each time that I say I will work harder, you say it will take me longer. Why do you say that?"

Replied the master, "When you have one eye on the goal, you only have one eye on the path".

zen tale

To my father, my first mentor

Abstract

Amorphous oxide semiconductors (AOS) are new candidates for large area and flexible electronics: thanks to their mostly ionic bonding they have a relatively high mobility ($\mu > 10\,\mathrm{cm^2V^{-1}s^{-1}}$) despite being in the amorphous phase. AOS-based thin film transistors (TFT) will thus be more performant than a-Si technologies while being cheaper than poly-Si ones. Being amorphous, they can be deposited at low temperature and on polymeric substrate, which is a key feature for employment in the creation of high-performance and large-area flexible electronics. In this thesis, several TFTs have been fabricated and characterized at CENIMAT laboratories at the University Nova of Lisbon (Portugal), where I spent 4 months as an Erasmus student, under the supervision of Prof. P. Barquinha.

These devices are composed of Molibdenum contact, a Indium-Gallium-Zinc Oxide (IGZO) semiconductive channel and a dielectric made of 7 alternate layers of SiO_2 and SiO_2+Ta_2O_5. All the devices have been deposited via sputtering on flexible substrates (PEN foils). The I-V measurements show the devices retain high mobility (tens of $10\,\mathrm{cm^2V^{-1}s^{-1}}$) even when fabricated at temperatures below 200 °C.

Their performance as phototransistors was then examined by measuring the photoresponse under UV light exposure, in particular their responsivity and the threshold voltage shift as a function of incoming wavelengths. These results also allow to make hypotheses on its operation at the microscopic scale. In particular, they indicate that i) mobility is unaffected by light, ii) both IGZO and Ta_2O_5 contribute to the photoconductivity process and iii) the photogeneration process is not adiabatic.

In addition, the thesis contains a description of the recombination process and presents a practical application of these devices in a RFID circuit. Finally, it explores the possibility of improving the bendability and performance.

Sommario

Gli ossidi amorfi semiconduttori (AOS) sono nuovi candidati per l'elettronica flessibile e su grandi aree: grazie ai loro legami prevalentemente ionici hanno una mobilità relativamente alta (μ>10 cm^{2}V^{-1}s^{-1}) anche nella fase amorfa. Transistor a film sottile (TFT) basati sugli AOS saranno quindi più performanti di tecnologie a base di a-Si e più economici di quelle a base di silicio policristallino. Essendo amorfi, possono essere depositati a basse temperature e su substrati polimerici, caratteristica chiave per l'elettronica flessibile e su grandi aree. Per questa tesi, diversi TFT sono stati fabbricati e caratterizzati nei laboratori del CENIMAT all'Università Nova di Lisbona sotto la supervisione del Prof. P. Barquinha.

Questi dispositivi sono composti di contatti in molibdeno, un canale semiconduttivo di ossido di zinco, gallio e indio (IGZO) e un dielettrico composto da 7 strati alternati di SiO_2 e SiO_2+Ta_2O_5. Tutti i dispositivi sono stati depositati mediante sputtering su sostrati flessibili (fogli di PEN). Le misure tensione-corrente mostrano che i dispositivi mantengono alte mobilità (decine di 10 cm^{2}V^{-1}s^{-1}) anche quando fabbricati a temperature inferiori a 200 °C.

Si è analizzato il funzionamento dei dispositivi come fototransistor rilevando la risposta alla luce ultravioletta e in particolare la loro responsività e spostamento della tensione di soglia in funzione della lunghezza d'onda incidente. Questi risultati consentono di formulare ipotesi sul comportamento dei dispositivi alla scala microscopica. In particolare, indicano che i) la mobilità del canale non è influenzata dall'illuminazione, ii) sia l'IGZO sia il Ta_2O_5 contribuiscono al processo di fotoconduttività e iii) il processo di fotogenerazione non è adiabatico.

La tesi contiene inoltre una descrizione del processo di ricombinazione e presenta un'applicazione pratica di tali dispositivi in un circuito per RFID. Infine, esplora la possibilità di migliorarne la flessibilità e le prestazioni.

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Introduction

With recent advancements in large area electronics and developement of active matrix LCD or OLED displays, there has been an increasing interest in devices that can act as switches or sensors that can be deposited at low costs and on a varied numbers of substrates.

Among the best candidates in this sense, Amorphous Oxide Semiconductor Thin Film Transistors can be found. The main feature of this type of materials, in particular a-IGZO, is the fact that they can retain good electrical performance ($\mu > 10\,\mathrm{cm^2V^{-1}s^{-1}}$) and a controllable charge density while also being processable on both rigid and flexible substrates at low temperatures and cost.

Even though many experiments have already demonstrated the capabilities of a-IGZO TFTs as switching devices [16], less work has been done to characterize their performance as phototransistors (to cite some of these works: [1, 24, 42]). Such devices could be employed as sensory tags, or for interactive sensors, for example sensing when something passes between the photoransistor and a light source [1]. In order for such systems to work, it would be imperative to understand for example which is the optimal working wavelength that maximizes responsivity. In addition, understanding which parts of the device interact with light and how they do it, makes it possible to understand how to improve the design.

The objective of this thesis is to study the response to light of a particular a-IGZO-based TFT design. To this end, several devices have been fabricated at CENIMAT and CEMOP laboratories at University Nova in Lisbon, where I spent 4 months as an Erasmus student, under the supervision of Prof. P.Barquinha. The response to light of a sample of these devices was then evaluated at Bologna University's Physics Department to understand

photoresponse uniformity.

Chapter 1 introduces the general characteristics and behavior of TFTs and amorphous oxide semiconductors (AOSs), focusing on the materials used in this work: amorphous Gallium Zinc Oxide (a-IGZO) and the dielectric layer.

Chapter 2 shows the fabrication process used in device production. The basis of optical lithography, the etching procedure and RF-magnetron sputtering are presented.

Chapter 3 introduces both light and electrical measurement techniques for the device, with a focus on the optical systems used (in particular the monochromator) and the electronic system used (lock-in amplifier).

In Chapter 4 measurements results are presented. First, simple electrical characterization are shown to illustrate the performance of the device in dark and the yield of the fabrication process. Afterwards, light exposure experiment are made, where in particular output variation and threshold voltage shift under illumination are monitored. Finally, the results of a practical application of the device as a sensor in a simple RFID control circuit are shown.

In Chapter 5 physical explanations for the device behavior are proposed. In particular, the focus is on which materials in the device respond to light, and the dynamics of both photogeneration and recombination process, which are stadied by fitting methods.

Chapter 6 shows an issue encountered with contact flexibility. A possible way to overcome this problem by cosputtering is proposed.

Finally, the Appendix shows a possible approach for modeling the TFT behavior in dark based on artificial neural networks (ANNs). This type of model is important for IC fabrication, as it can be exported as a representative of the component in a circuit layout simulator, such as cadence [2]. This way new integrated circuit designs can be tested and tweaked, thus making it easier to find optimal characteristics to obtain the desired results.

Considering the fabrication process can take several days depending on the design complexity, being able to optimize the layout before production is extremely important. In particular, the model shown in this section manages to simulate small signal with a much higher accuracy compared to simple artificial neural networks (ANNs), which could for instance be vital for creating an integrated version of the RFID control circuit illustrated in chapter 4 on page 43.

1

Thin film transistors

1.1 Thin film transistors

A Field effect transistor (FET) is a device comprising of two electrodes (source, drain) separated by a semiconductor, with a dielectric and another electrode (gate) on top of it [5]. The current flowing between source and drain will be modulated by varying the potential between the gate and the source. This modulation (known as field-effect) works by attracting carriers close to the dielectric/semiconductor interface as a capacitive effect, which is possible if the gate, the dielectric and the semiconductor are parallel and on top of each other, thus forming a parallel plate capacitor structure.

Thin film transistors (TFT) in particular are a class of FETs where contacts, semiconductor and dielectric are all single films deposited on top of each other on a substrate. This means that, unlike other more performant counterparts, such as MOSFETs, the substrate is not an active component of the device, and thus its production is cheaper, easier and can be done on a wide array of substrates [12]. Thanks to these features they are predominant in applications where large numbers of on/off switches deposited or large areas are needed, in particular active matrix flatplanes of flat panels display (FPD), such as liquid crystals ones (LCDs) or organic light emitting devices (OLEDs).

1.1.1 Device structure

Some of the most common device structures are shown in figure 1.1 on the next page. These are denominated by staggered and coplanar, depending if the source/drain and gate electrodes are on opposite sides or on the same side of the semiconductor channel. Among staggered and coplanar structures, two

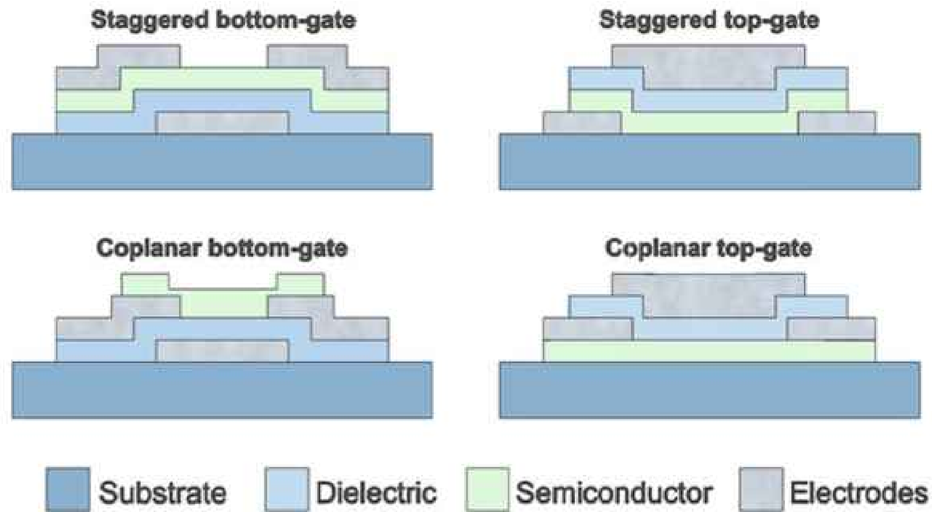


Figure 1.1: The four different TFT geometries [12]

more configuration can be distinguished: top-gate (or normal) and bottom-gate (or inverted).

Each structure presents features that make it more suitable for a particular employment. When for instance the semiconductive material used is photosensitive, as is the case for a-Si:H (amorphous hydrogenated silicon, one of the most used for this type of devices), bottom gate are preferred in the application of TFTs in LCDs, because the gate shields the channel from the backlight present [12].

1.1.2 Operation

The behaviour of a n-type TFT (that is, a TFT whose semiconductor channel allows only the movement of electrons) can be described through an energy band diagram (figure 1.2 on the facing page) of the capacitor comprised of the gate electrode, the dielectric and the semiconductor when different voltages V_{GS} are applied to the gate with respect to the source.

Assuming charge accumulation and depletion don't occur, for $V_{GS} < 0\,V$ the band bends upwards: the negative voltage on the gate electrodes repels mobile electrons from the dielectric/semiconductor interface, creating a depletion layer in this region. As can be seen in figure, in this situation (or if $V_{GS} = 0\,V$) the Fermi level is far away from the conduction band, thus a very low current I_D will flow between drain and source. In this case the device is said to be turned off. When instead $V_{GS} > 0\,V$ (figure 1.2 on the next page on the right) electrons accumulate close to the dielectric/semiconductor interface, leading to a downward band-bending in the region. Now the Fermi level start

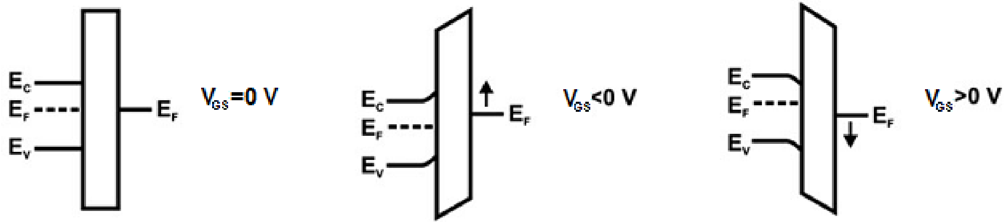


Figure 1.2: Band diagrams of an ideal gate/dielectric n-semiconductor at different gate voltages [5]

intersecating with the conduction band and a higher amount of carriers is available for conduction. In this situation a considerable current I_D will flow between source and drain once a voltage difference V_{DS} is applied to them. In this case the device is said to be turned on.

In a real case, in order to turn the device on the condition will be $V_{GS} > V_{th}$ instead. This is because a significant charge accumulation might be needed to have enough drain current (thus $V_{th} > 0\,V$) or there might already be a significant amount of free carriers (in which case $V_{th} < 0\,V$). V_{th} is known as the threshold voltage, and in general will be a function of the work function difference between the gate electrode and the semiconductor, the charge density already in the dielectric and the trap density at the interface and within the semiconductor.

For a n-type TFT, depending on whether the threshold voltage is higher or lower than 0 V, the device is said to work in accumulation or depletion mode. In the former case the device is normally turned off unless a positive gate voltage is applied, while in the latter the device is normally turned on and a negative gate voltage is needed to close the channel. While both find use in different applications, for electronics the first case is much more prevalent because it's simpler to work with [5].

When the transistor is in the on-state, different operation can be individuated, depending on the value of the drain voltage V_{DS} compared to the gate voltage V_{GS}:

- When $V_{DS} < V_{GS} - V_{th}$ the TFT is in the pre-pinch-off regime. In this case I_D follows the formula

  $$I_D = C_i \mu_{FE} \frac{W}{L} \left[\left(V_{Gs} - V_{th}\right) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

  where C_i is the dielectric capacitance per unit area, μ_{FE} is known as the field effect mobility, W is the channel width and L is the channel

length. For very low V$_{DS}$ the quadratic term $-\frac{1}{2}V_{DS}^2$ can be neglected, resulting in a linear relation between I$_D$ and V$_{DS}$. For this reason, the pre-pinch-off regime is also called linear mode. In this situation the accumulated charges are almost uniformly distributed throughout the channel.

- When V$_{DS} >$ V$_{GS} -$ V$_{th}$ the charge carriers close to the drain region feel a stronger pull towards the drain that towards the gate. For this reason no charge accumulates close to the drain. This region acts as a bottleneck for conduction and is thus called pinch-off regime. The result is that I$_D$ stops increaseing with V$_{DS}$ and is described by:

$$I_D = C_i \mu_{sat} \frac{W}{L} (V_{GS} - V_{th})^2$$

  where μ_{sat} is called saturation mobility. In this case the drain current is said to be saturated, and for this reason the pinch off regime is also called saturation mode.

The equation shown above are based on two different assumption. The first, called gradual channel approximation, is that the gradient of the lateral potential is negligible compared to the vertical one.

While this approximation is not valid near the drain in saturation mode or with very short channels, it describes fairly well most of the TFT operation. The other approximation is that the mobilities μ_{FE} and μ_{sat} are costant, while in fact in TFT they will both depend on V$_{GS}$.

In order to describe the functionality of a device, in particular I$_D$ (V$_{DS}$) and I$_D$ (V$_{GS}$) curves, the following parameters are used:

- On-Off ratio: which is the ratio of the maximum to minimum I$_D$. When the device is turned on, the higher the current that can be obtained the better the signal that comes through the device. When the device is turned off, on the other hand, a low current reduces leakage. Thus a desirable device is one for which the ratio between current in the on and off state at costant V$_{DS}$ is as high as possible. This ratio is called the on/off ratio.

- Threshold voltage (V$_{th}$): as said above, it corresponds to the lowest V$_{GS}$ that causes the accumulation in the dielectric/semiconductor interface of a charge significant enough to allow conduction. V$_{th}$ can be extrapolated by performing a linear fit of either I$_{DS}$(V$_{GS}$) at low V$_{DS}$ or of $I_{DS}^{\frac{1}{2}}(V_{GS})$ in saturation mode.

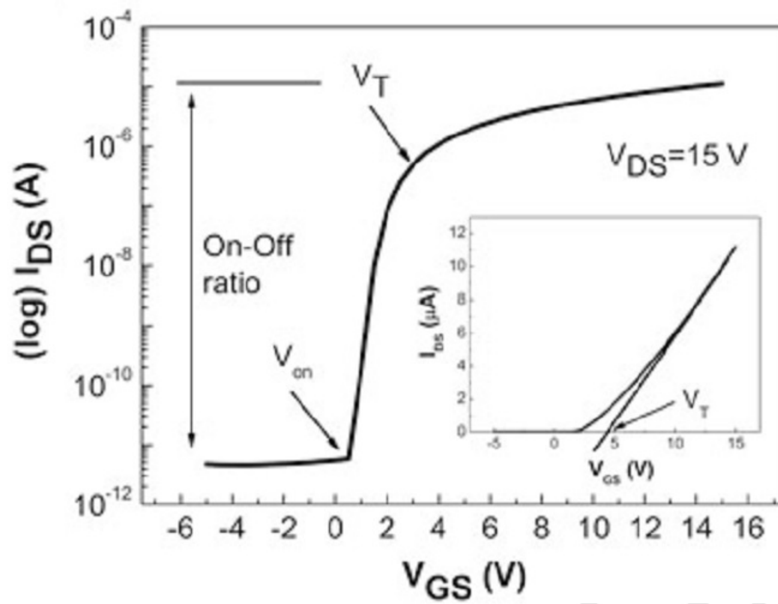


Figure 1.3: Example of an $I_D(V_{GS})$ curve and origin of some of the functionality parameters [12]

- Turn-on voltage (V_{on}): corresponds to the V_{GS} at which I_{DS} starts to increase. This value can be easily identified in a $I_{DS}(V_{GS})$ curve shown in logarithmic scale (figure 1.3).

- Subthreshold swing (S): it indicates the V_{GS} required to increase I_{DS} by one decade as seen in the subthreshold region. It is defined, in V· d^{-1} as $S = max\left(\frac{d\ln(I_{DS})}{dV_{GS}}\right)^{-1}$. A smaller S results in higher switching speed and thus is preferable.

The last important parameter is mobility, which is an indicator of the efficiency with which carriers move through a material. It not only directly affects maximum I_D, but also the maximum frequency at which it can operate (cutoff frequency f_{CO}), which is related to mobility as

$$f_{CO} = \frac{\mu V_{DS}}{2\pi L^2}$$

As aid before, there are many different ways to define mobility, depending on the operating conditions of the devices. In particular, positive charges gathered on the dielectric-semiconductor interface by a positive V_{GS} will increase coulomb scattering, thus reducing mobility. The three most relevant definitions are highlighted below.

- Effective mobility (μ_{eff}): It is considered the most correct estimation of μ, as it includes the dependancy on V_{GS}. At low V_{DS} it's determined by the conductance (g_{DS}) and requires the determination of V_{th}. In particular:

$$\mu_{eff} = \frac{g_{DS}}{C_i \frac{W}{L} (V_{GS} - V_{th})}$$

where $g_D = \frac{L \cdot I_D}{W \cdot V_G}$ is the conductance.

- Field-effect mobility (μ_{FE}): characteristic for linear mode, is defined as

$$\mu_{FE} = \frac{g_m}{C_i \frac{W}{L} V_D}$$

where the transconductance this time is defined as $g_m = \frac{\partial I_D}{\partial V_{GS}}$

- Saturation mobility (μ_{sat}): it applies in saturation mode, and is defined as

$$\mu_{sat} = \frac{\left(\frac{\partial \sqrt{I_D}}{\partial V_{GS}}\right)^2}{\frac{1}{2} C_i \frac{W}{L} V_{DS}}$$

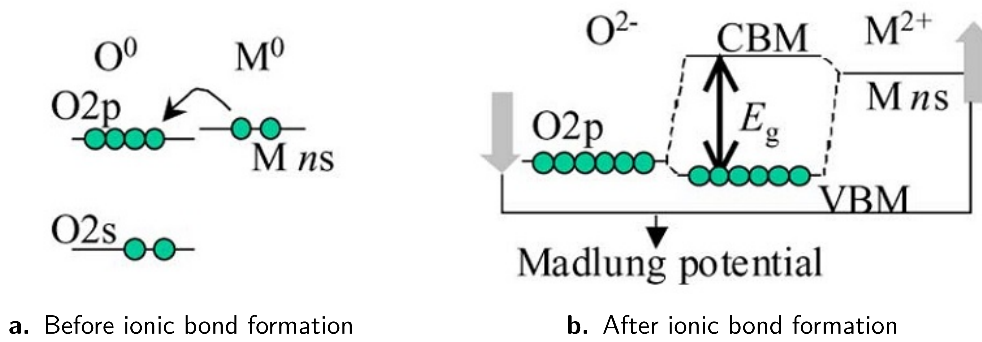
It should be noted that, being applied in a nonlinear situation, μ_{sat} is the only mobility whose measurement isn't affected by contact resistance or threshold voltage.

1.2 Amorphous oxide semiconductors

As it has been said before, the most common semiconductor employed in TFT devices is hydrogenated amorphous silicon a-Si:H, which while being easy to produce presents a really low mobility of around $1\,\mathrm{cm^2V^{-1}cm^{-1}}$.

One way to improve mobility is to employ another type of materials, known as amorphous oxide simiconductors (AOS), which can reach mobilities more than an order of magnitude greater with comparable fabrication costs.

To understand how this is achieved, the atomic composition and orbital structure of these kind of materials must be described. AOS are composed of a non-transition metal atom and an oxygen atom. When oxidation occurs charge transfer is triggered due to different affinity. In particular, one electron in the highest occupied orbital (which is of type *s*) transfers to the lowest unoccupied electron orbital, which is of type *p* (figure 1.4a on the next page). These two orbitals would normally be at a similar energy level, but ionization forms a negative electrostatic potential (known as Madelung potential) that



a. Before ionic bond formation **b.** After ionic bond formation

Figure 1.4: Origin of the AOS electronic structure [20]

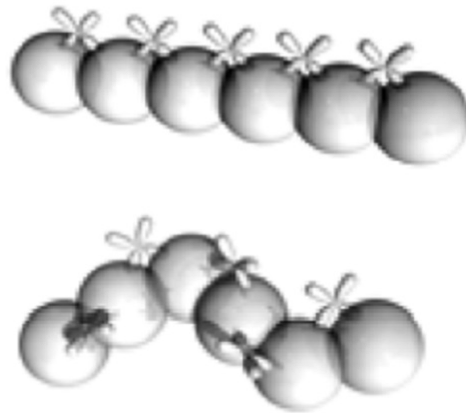


Figure 1.5: Conduction orbital overlap in cristalline AOS (above) and amorphous AOS (below)[20]

lowers the energy levels in the oxygen ions and raises those in the metal cations (figure 1.4b). Thus, the most energetic valence electrons are the ones in the oxygen filled p orbital, and the lowest conduction levels they can reach is in the s orbital of the metal [20].

This structure explains why AOS can retain high electron mobilities even in amorphous structure: the s orbitals of different metal atoms, being spherical, keep consistent overlap even when the crystal structure loses directionality (figure 1.5). One thing to note is that while the conduction electrons shift to the metal s orbital, one hole is created in the oxygen p orbital. This orbital is not spherical, thus hole mobility will be much lower compared to electron mobility: AOS are n-type semiconductors.

Other semiconductors form covalent bonds instead of ionic ones. In silicon, for example, the highest occupied levels and lowest unoccupied levels are

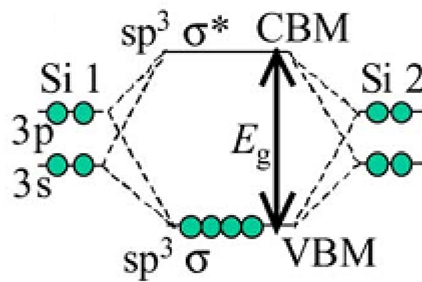


Figure 1.6: Silicon sp^3 level diagram for silicon [20]

Figure 1.7: Silicon conduction orbital overlap in crystal phase (left) and amorphous phase (right) [22]

respectively bonding and antibonding sp^3 orbitals (figure 1.6).

Electron levels such as the sp^3 ones are highly directional, which means that shifting from a crystalline to an amorphous phase causes to degradate to a much larger extent (figure 1.7) [22].

Other than the advantage of mobility, AOS present other advantages due to their amorphous nature [23]:

- They can be processed at low temperatures, because they don't require crystallization.
- They allow for a wide range of gate insulators, because they don't present lattice mismatch problems and, being n-type, the valence band offset isn't critical.
- The surface is flat and highly uniform.

- Thanks to the very low hole mobility, when a negative voltage is applied to the gate there is no risk of a hole channel (known as inversion channel) forming. This means that, unlike in the case of silicon channel, there is no need to use p-n junction contact to avoid the device having an inversion channel that allows current passage when it's turned off. Thus, simple metallic contacts can be used.

- They can be fabricated in very different ways.

1.3 Example of AOS TFT: a-IGZO tft with high-κ dielectric

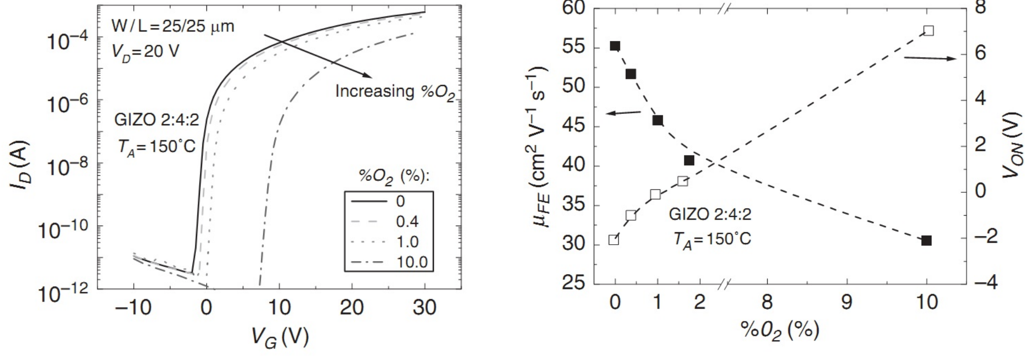
1.3.1 a-IGZO as active layer

Since the first report in 2004, many different AOS materials have been under study, including Zinc-Oxyde (ZnO), Indium-Zinc-Oxyde (IZO) and Indium-Gallium-Zinc-Oxyde (a-IGZO). Among these materials, IZO has a much higher mobility, thanks to the weak bonds between Oxygen and Zinc or Indium: oxygen vacancies are more likely to occur, thus there are more free conduction electrons in unbound metal s orbitals [20]. While this is normally a positive aspect, in the case of TFT operation it makes it hard to close the channel when the device is supposed to be off, because there will be a significant free electron density without the application of gate voltage. This results in a highly negative threshold voltage (around $-10\,\mathrm{V}$) In order to solve this problem, gallium can be added [31]: Ga-O ionic bonds are much stronger and thus gallium acts as an effective trap for oxygen, preventing vacancies from forming.

Of course, the strength of the bond also means that the s orbitals will have a smaller radius, thus an excessive number of Ga atoms will reduce electron overlap and degrade the mobility. One of the most promising Ga-In-Zn proportion used is 2:4:2 [12].

Effects of thickness and oxygen atmosphere

Other ways to bring threshold voltage close to 0 are to reduce channel thickness and increase oxygen esposition during fabrication. In plasma-based fabrication process such as sputtering, an atmosphere with a higher oxygen percentage will increase the amount of oxygen absorbed in the film and thus reduce the amount of free carriers in the device.



a. I_D vs V_{GS} curves with increasing O_2 concentration

b. μ_{FE} and V_{on} vs O_2 concentration

Figure 1.8: Mobility and turn on voltage with higher oxygen atmosphere [12]

On the other hand, oxygen bombardment increases the amount of impurities in the film, thus reducing As can be seen in figure 1.8, the $I_D(V_{GS})$ curve shifts light with higher oxygen population [12].

Oxygen absorption effectively creates a depletion layer in the device in which free carriers are removed. By reducing channel thickness, this layer makes up a higher portion of it, thus the amount of free carriers is reduced until this depletion makes up most of the device [5].

1.3.2 Dielectric layer

An optimal gate dielectric is vital to improve TFT performance. A desirable dielectric must accomplish two goals: reduce leakage corrent (which flows from the gate to the source) and have a higher capacitance. This last factor in particular increases the amount of charge in the accumulation layer, which means that a the current obtained by applying a positive voltage increases. Other than that, an ideal gate should be amorphous and atomically smooth, exhibit a large breakdown field and shouldn't create a high number of trap states in the interface with the semiconductor [40]. The capacitance of the gate/dielectric/semiconductor system can be determined by remembering capacitance C is expressed:

$$C = \frac{A}{d}\epsilon_0\kappa$$

Where A is the area, d is the thickness, ϵ_0 is the vacuum electric permittivity and κ is the relative permittivity of the material. In other words, in order to improve the capacitance of the dielectric, there are three possible ways:

increase TFT area, reduce dielectric thickness or find a material with a higher κ. Unfortunately, increasing the area or reducing its thickness reduce the resistance of the dielectric, thus increasing leakage current.

The most used gate dielectric today is SiO_2, that is thermally grown at hight temperatures on Si [13]. This kind of growing is not practical for large area electronics that must be applicable to a large amount of substrates. Also, the low channel dimension needed for the demands of miniaturization requires that in order to mantain acceptable capacitance the thickness of the SiO_2 layer must be extremely low (down to $1nm$), enought to start having leakage current problems.

In order to solve these problems, a different class of materials, called high-κ dielectrics, is being investigated. However, such materials present some drawbacks, such as a small energy gap, which can increase leakage current even if a higher thickness can be used thanks to the high κ. Also, in order to avoid charge injection at the interface, the conduction band minima of the dielectric and a-IGZO must be separated by at least 1 eV. Other than that, a desirable semiconductor must remain amorphous during the production process, because grain boundaries become preferential paths for leakage current.

Ta_2O_5 is a good candidate and avoids most of the problems listed above. The only exception is the energy gap, which is still at around 4.5 eV, compared to the 8 eV gap of SiO_2 [5]. In order to create a layer with high capacity and good resistance, the best option is to create a layer that contains a mix of the two materials (for example by cosputtering). This way the SiO_2 will block the path of charges that could move through Ta_2O_5, which will still contribute to the capacitance.

Another step forward is to alternate layers of $Ta_2O_5 + SiO_2$ (called TsiO) and layers of pure SiO_2. This is needed because without high temperature treatments the insulating characteristics of the film aren't optimal, thus a higher thickness is needed to compensate, which in turne is compensated by the higher κ of Ta_2O_5

1.3.3 *Substrate*

As said above, AOS TFTs can be deposited on a varied amount of substrates, both soft (plastic) and hard (glass). In particular, plastic substrates are promising because of the increased flexibility that would allow to employ these kind of devices in flexible electronics. Other than that, a substrate material must solve a series of prerequisites to be employable [41].

First, it must be optically clear to be employable in bottom emitting or transmissive displays.

Second, it must be as smooth as possible: thin TFT are more influenced by surface roughness, especially over short distances.

Third, its working temperatures must be compatible with the temperature used in production. Also, thermal stress mismatch between device films and substrate might cause the former to break during fabrication.

Fourth, the substrate should not release contaminants and should not react to chemicals used in fabrication process. Also, impermeability to water and gas is required to protect dimensional stability from swelling.

Different polymers satsify there requirements, such as polyethylene naphatalate, which is optically clear with more than 85% transmittance in the visible, absorb little water. Their process temperatures are relatively low though, and tend to shrink around 200 °C. In order to solve this problem, the substrate can be preshrunk by exposing it to a similar temperature before starting the fabrication process, thus making sure it won't shrink further.

2

Fabrication process

During this work, several thin film transistors have been fabricated. The high number allowed us to assert both the chance of the fabrication process giving us a working device and the consistency of their behaviour.

2.1 Device description

The device is in a staggered bottom gate configuration, which means that the deposition order will be: gate contact, dielectric layer, semiconductive channel and source/drain contacts.

- *Substrate*: The devices are deposited on PEN Q51 non-planarized sheets that are 125 μm .
- *Contacts*: 60 nm Molybdenum.
- *Semiconductor channel*: 35 nm GIZO .
- *Dielectric layer*: 7 alternating layers of SiO_2 and TsiO (co-deposition of SiO2 and Ta2O5). The deposition order is:

  SiO2|TSiO|SiO_2|TSiO|SiO_2|TSiO|SiO_2 .

The fabrication process consists in imposing the pattern via photolithography, deposit the material by sputtering deposition and eliminating the excess material by etching or lift-off. The process is repeated with every layer (gate, dielectric, semiconductor, source/drain) in a different way depending on the method used.

2.2 Substrate preparation

The PEN sheet is flexible, which means natural bending during the process could disturb the alignment of the different patterns and make lift-off more difficult. To avoid this problem, PDMS is used as adhesive to keep the PEN sheet stretched on a glass support [18].

The process flow is the following:

- First, PDMS is prepared by mixing 10 parts of silicon elastomer with 1 part of silicon curing agent and leaving the result in a vacuum for 30 minutes.
- A 10 x 10 cm glass plate is washed. The washing consists in first ultrasonic cleaning it first in acetone for 10 minutes and then in isopropyl alcohol for another 10 minutes.

After that, the glass is rinsed with water and dried with nitrogen.

- PDMS was then applied to the plate via spin coating, using a Karl-Suss RC8 spinner (figure 2.1 on the next page).
- Four 3.5 x 3.5 cm PEN sheets are cut and placed on the four corners of the glass at around 0.75 cm from each edge, and are pressed on the surface so that they adhere on the PDMS layer.
- The PDMS is then dried by putting the glass with the PEN sheets on a furnace at 85 °C for one hour.
- The glass is then washed again with the same procedure as before and cut into four 5 x 5 cm^2 , each containing one PEN square. By this way four substrates ready for fabrication are obtained.

2.3 Optical lithography

The goal of lithography is to impose a pattern from a mask to a surface. Optical lithography obtains this goal by the surface with a photosensitive material and then illuminating it with light (usually UV). If between the light and the surface a mask is put that can block the light in chosen points, the pattern of the mask will be transported on the photosensitive material on the surface, where only the illuminated zone will change their chemical behaviour.

Three components are involved in this process. First, the photoresist, second, the mask projector and third, the mask aligner.

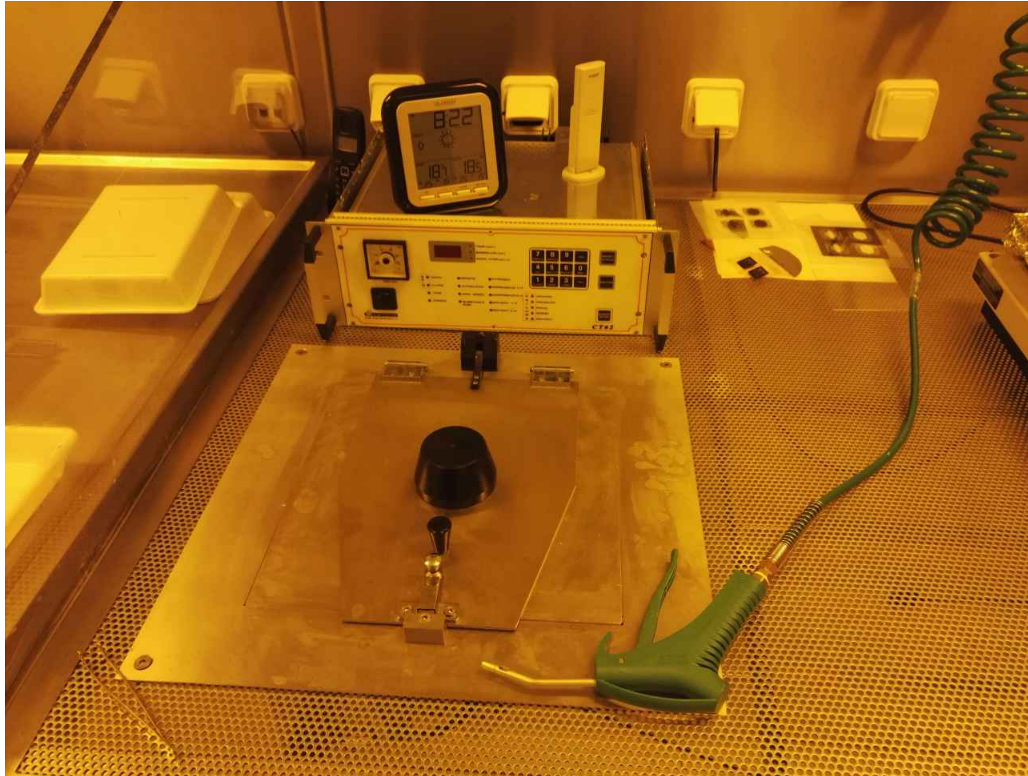


Figure 2.1: Karl-Suss RC8 spinner

2.3.1 Photoresist application

Photoresist are usually materials that either become soluble in a certain developer after exposure to light (in which case they are called positive photoresists) or stop being soluble after exposure (and they are called negative photoresist).

Photoresist materials have three main components [17]:

1. Base resin, which determines mechanical and thermal properties.

2. Photoactive compound which determines sensitivity to radiation.

3. Solvent, which control viscosity.

Usually base resins for positive resists are soluble in alkaline developers, such as phenolic novolak. Their solubility is normally inhibited by the photoactive compound, such as for example Diazonapthoquinine (DNQ). Upon exposure, the DNQ forms an acidic compound which makes the photoresist soluble. The complete reaction is shown in figure 2.2 on the following page. The first and second line show the reaction after light and hydration, the third

line show the reaction when the exposed photoresist comes in contact with the developer.

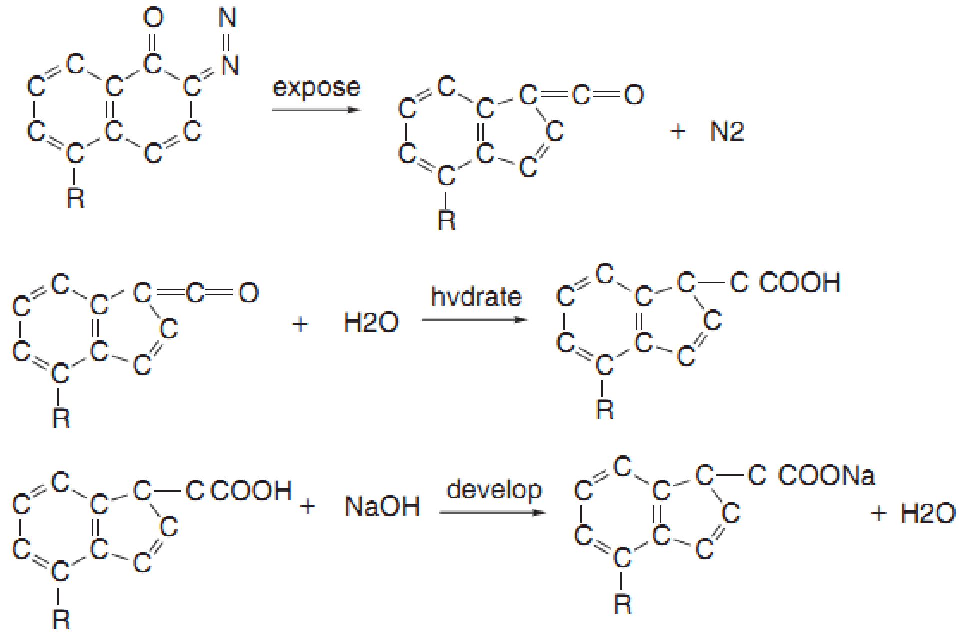


Figure 2.2: Example of photoresist reactions with UV light, hydration and developement [17]

As is shown in figure, part of this reaction requires water, which is given by the cleanroom air, which is kept at a constant humidity of around 40%. Negative resists work in the opposite way by having photoactive compounds that polymerize and thus increase their molecular weight. They are usually developed by solvents, but this can lead to swelling the polymerized photoresists, and thus have a chance to disturb the pattern.

The standard application method for the resist is spin coating. As the name tells, the surface is held by vacuum on a chuck capable of rotating at high speed. By applying a drop of photoresist on the surface and letting the chuck spin at thousands of rpm, the solvent will evaporate and the surface will have a photoresistive layer.

The evaporation of the solvent is necessary for making the photoresist solid and thus preventing mixing between exposed and unexposed zones. To obtain that, after spin coating the photoresist-covered surfaces are exposed to heat, which both evaporates the solvent and improves the adhesion between the photoresist with the surface. This process is known as soft baking [27]. In this fabrication, the photoresist AZ ECI 3012 has been used, alongside a AZ

726 MIF developer.

The deposition was done using a Headway Research Inc, model PWM32 spin coater (figure 2.3). In order to obtain a uniform layer 1.2 μm thick, the spin coating process lasted 30 s, 10 s at 3000 rpm for covering the surface and 20 s at 4000 rpm to reach the wanted thickness. Soft baking was done at 118 °C for 1m 15s.

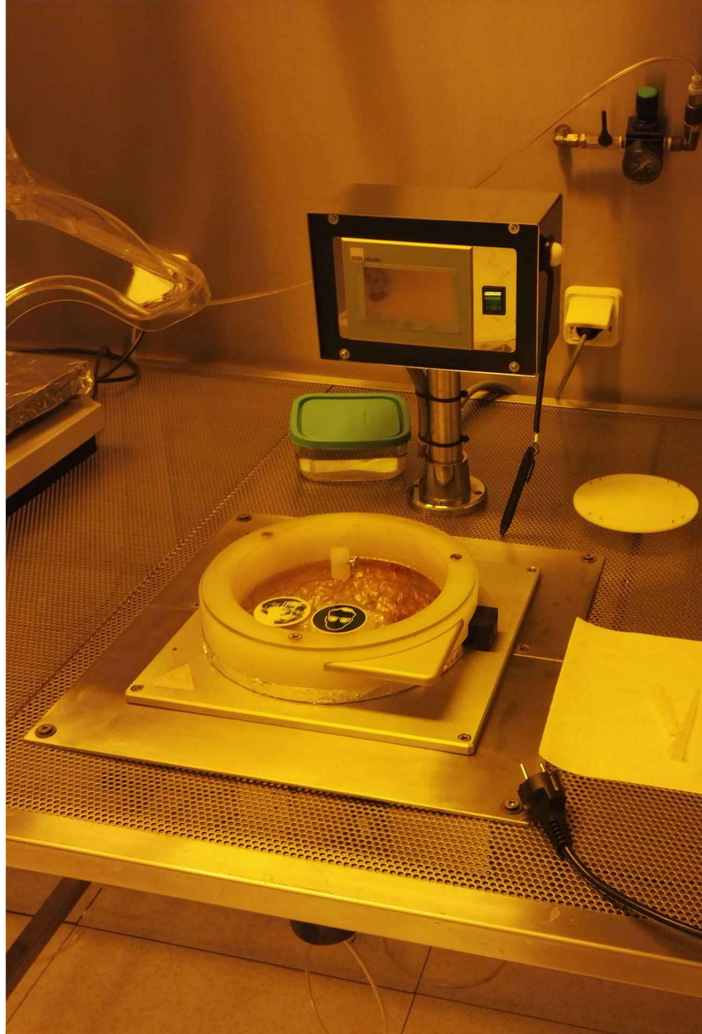


Figure 2.3: PWM32 spin coater used for photoresist coaring

2.3.2 Mask alignment and exposure

After photoresist deposition, the surface and the photomask are both loaded on a vacuum chuck and inserted into the aligner. The photomask is a square glass plate with a patterned metal film on one side. The metal film will block the light, thus preventing the photoresist from becoming soluble. Since the

design usually require the deposition of multiple layers, one different mask for each layer will be necessary. In the case of TFTs, the layers are four: one for the gate contacts, one for the dielectric, one for the semiconductor and one for the drain and source contacts.

The mask aligner usually also works as an exposure tool. The simplest way the mask's pattern can be impressed on a surface is through the contact lithography technique: the mask and the resist-covered surface are brought into contact and exposed. The advantage of this method is the fact that the resolution is only limited by the pattern dimensions on the mask, and thus can be extremely small. On the other side, contact might damage the mask, which is highly unwanted because of the difficulty of fabrication.

To avoid this problem, proximity lithography is used instead. In this case a small gap of a few μm is left between the mask and the substrate. The projected image maintains the same size of the mask. The resolution now depends on the optical system, and through Fresnel diffraction principle the minimum resolvable distance R between two patterns can be evaluated as $R \approx \sqrt{\lambda \left(g + \frac{d}{2}\right)}$ where g is the gap between the mask and the surface, λ is the wavelength of the exposing radiation (typical values are 436, 405 or 365 μm when a mercury lamp is used), and d is the thickness of the photoresistive layer [17].

To obtain working devices, the patterns from the four different mask layers must be projected exactly on top of each other, and thus an alignment procedure is necessary. The surface is held on a vacuum chuck and the alignment is performed manually using an optical microscope and an adjustable x-y stage. Marks were added to the corner of the pattern for every layer to facilitate the alignment of every layer.

The exposure has been performed with a mercury lamp, with an emission spectrum that matches the photoresistive one (which is sensible to UV and blue light). For this reason, the blue component of the light in the clean room where photolithography is performed must be filtered out.

After the surfaces have been illuminated, the exposed pattern is removed by submerging them in developing liquid for 40 seconds.

After the development, two different methods were used to translate the pattern on the photoresist on the deposited materials: etching and lift-off. The first works if the photoresist is above the deposited material, the second one if the photoresist is below the deposited material.

2.4 Etching

Etchant substances can be used to remove the layers that aren't covered by photoresist material. This requires a high amount of selectivity to ensure that the photoresist is actually more resistant to etching than the deposited material.

There are mainly two classes of etching that can be used: wet etching and plasma etching [17]. In the first case, the etchant is in a liquid solution and turns materials into soluble products. One example of such reaction is $Si(s)+2OH\text{-}(aq)+2H_2O \rightarrow Si(OH)_2(O\text{-})_2(aq)+2H_2(g)$. In the second case, the etchant is ionized and turns materials into volatile products. For example: $SiO_2(s)+CF_4(g) \rightarrow SiF_4(g)+CO_2(g)$.

Wet etching is cheaper, requiring only a way to diffuse the liquid etchant on the surface and to diffuse the by-products of the reaction away from it. The chemical reactions involved are usually reduction or oxidation ones. It also has a high level of selectivity thanks to its chemical nature and a quick etch rate of 10-100 nm/min. On the other hand, because of its simplicity there is no mechanism giving a preferred direction for the etching process, thus it tends to be isotropic like its diffusion. Because of this, the etchant attacks both horizontal and vertical surfaces, thus undercutting the material below the photoresist. While this might be a desirable feature in some situations (like for example in obtaining free standing beams), isotropic etching makes it impossible to etch patterns with line widths below 1 μm. Other than that, some of the product might hinder or catalyse the process, making it harder to control, and exothermic reactions can lead to substrate overheating.

Plasma etching, or dry etching, involves directing plasma on the deposited material. The plasma can then either physically corrode the material, react chemically with it or both. The main advantage of using plasma is that its diffusion direction can be directed with an electric field, thus making it perfectly anisotropic and avoids undercutting. Another advantage is that this precision allows to reduce the amount of etchant used compared to wet etching. The plasma is created and accelerated through RF excitation. The acceleration imparts ion energy that favours impacts and reactions only in a single direction.

Depending on the effects on the surface, two different types of etching exist. In physical dry etching, atoms from the reactive gases are ionized and used to bombard the surface and break its atomic bonds. Thanks to this, this process is highly anisotropic and there is no need to find a plasma that

can react with the surface. On the other hand, such a process is not highly selective, because ions will mechanically etch all materials.

In chemical dry etching the etchant attacks the surface by chemically reacting with it. The electrons generated in the plasma excite some of the atoms, making them highly reactive. This process is highly selective, because by choosing the etching gas we can choose which parts of the surface will be attacked, but it's also isotropic.

Reactive Ion Etching (RIE) is a method used in this works, in which plasma is generated and both ions and excited atoms are produced. Consequently, it combines chemical and physical etching and thus it brings both selectivity and anisotropy.

In this work, reactive ion etching was used for the first two layers: molybdenum gate contacts and SiO2/TsiO dielectric layer. The materials were first deposited, then the photoresist was applied, exposed and developed. Afterwards, the substrates were exposed to RIE. The etchant plasma removes the material that wasn't covered by photoresist at a much faster rate, and thus it was removed while the photoresist acted as a shield for the material it covered.

Etching has been performed using TRION PHANTOM III RIE (figure 2.4 on the facing page). Both the molybdenum and the dielectric layer have been etched using SF6 gas.

2.5 Lift-off

The lift-off process consists of removing the photoresist with acetone. If the material was deposited after the photoresist was deposited and developed, the portions of deposited materials that are above photoresists will be stripped alongside it.

In this work lift-off was used for the last two layers: IGZO channel and molybdenum source/drain contacts. The reason why lift-off is preferred to RIE is because otherwise there would be a risk of etching already deposited and patterned layers, damaging the devices.

One more thing to note is that while with RIE only the material covered with photoresist remains, with lift-off it's the opposite: only the material that was not covered remains. Which means that the photomasks for the first two layers will show patterns that will directly represent the pattern impressed on the substrate, while the ones for the last two layers will show a negative of the pattern (figure 2.5 on page 24)

Figure 2.4: TRION PHANTOM III RIE, used for the etching process

2.6 Sputtering deposition

In general, vapor deposition consists in ejecting particles from a solid target material in a vacuum and transporting them on a substrate.

Depending on whether the particles are directly deposited on the substrate or take part in a reaction that has the desired material as one of the products, the deposition method is called respectively physical or chemical vapor deposition (PVD or CVD). In particular, sputtering deposition is the most important method of physical vapor deposition (the other being thermal evaporation).

Sputtering deposition consists in using accelerated plasma to knock material from a target so that it will deposit on a substrate. Argon is usually used for this at relatively high pressures (order of mTorrs). Ar+ ions are guided on the negatively biased target and usually eject one target atom. These atoms are ejected with high energy and an equivalent temperature of tens of thousands of Kelvin and collide with argon gas at a much lower temperature (T=300 K). The cooling is called thermalization, which on one side reduces the energy of particles hitting the surface and on the other reduces the flux of

a. Etching **b.** Liftoff

Figure 2.5: Process used for the removal of excess material

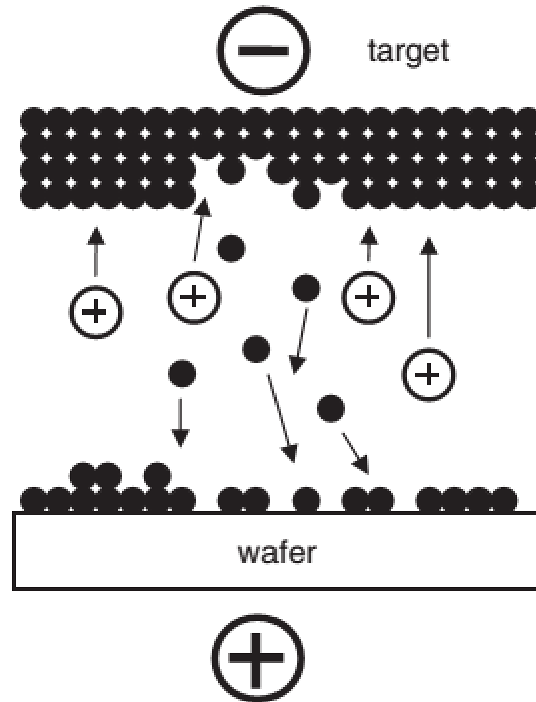


Figure 2.6: Scheme of a DC sputtering setup [18]

particles that make it to the substrate and thus the deposition rate is also lowered. Not only that, if the incoming atoms are energetic enough they can knock out weakly bonded atoms and impurities.

The simplest sputtering deposition apparatus is shown in figure 2.6 and consists of a vacuum chamber containing two electrodes: the cathode, upon which is placed the target, and the anode, that holds the substrate and is usually grounded. An inert gas — usually Argon — is inserted in the chamber and an electric field is created between the electrodes. Free electrons normally present in the gas accelerate towards the anode, ionizing atoms in their path and creating other free electrons to keep ionizing. Ar+ ions are accelerated towards the cathode knocking target atoms into the chamber (sputtering). Electrons can also recombine with ions: when this happens, a photon is emitted and this causes the gas to glow. Because of this, this state is called glow discharge plasma. During the process, argon, oxygen and other residues might get incorporated in the film. While argon incorporation, being a noble gas, might be neglected, other gases such as oxygen are more easily incorporated because they react with the film. The presence of these elements might be beneficial: for example, incorporating enough oxygen in the film causes it to oxidize almost entirely, which makes depositing oxides

much easier. This method is called reactive sputtering, and is used to obtain the semiconductive and dielectric oxides.

One issue with this method is that electronegative species such as oxygen might accept an electron and become negative ions that won't move towards the cathode but towards the anode, etch the substrate and thus interfere with the deposition process.

For what concerns sputtering setups, the simplest is DC sputtering. It involves creating a DC bias between the electrodes. While this setup requires the least amount of power and system complexity, it is limited by the fact it can't be used for depositing nonconductive materials. This is because to keep the sputtering process going, there needs to be a constant supply of electrons to prevent positive charge from accumulating on the target surface, and nonconductive materials can't provide it.

In order to operate with both conductive and insulator materials RF sputtering can be used. In this setup, the bias is alternated at a high frequency (13.56 MHz). During half a period, the voltage on the target will be negative, attracting ions for sputtering. During the other half, the voltage will be positive, attracting electron that will balance the build-up of positive charges. This way sputtering deposition of insulating material becomes possible, at the cost of a lower sputtering rate. These two setups share a common flaw: when the substrate is at a positive voltage, it is exposed to electron bombardment that can cause overheating and structural damage.

A third setup, called RF magnetron sputtering (shown in figure 2.7 on the next page), solves this problem by using magnets to confine electrons in a magnetic field above the target surface and away from the substrate. In addition, by being closer to the target they have a higher chance of ionizing gas that will result in sputtering. The only flaw is that the ions are also redirected along the magnets' field lines, and thus certain areas of the target will be preferentially eroded.

In this work, all depositions were performed via RF magnetron sputtering. For conductive materials (molybdenum) AJA ATC 1300-S (figure 2.8b on page 28) was used, while for semiconductive and insulating layers AJA ATC 1800-S was used (figure 2.8a).

2.7 Annealing

Once the fabrication is complete, heating the device for an extended period can allow its structure to overcome energetic barrier and move towards mechanical

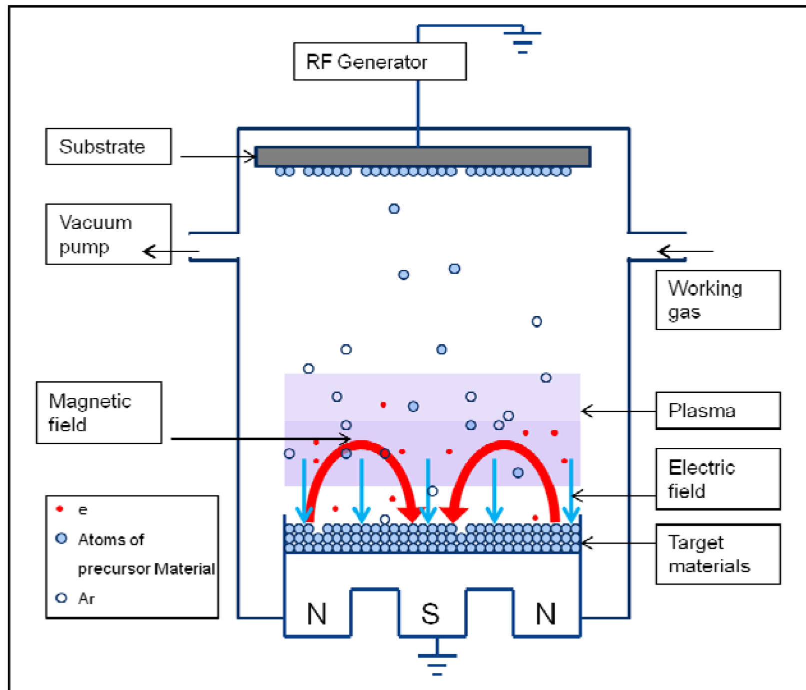


Figure 2.7: Diagram of magnetron sputtering [38]

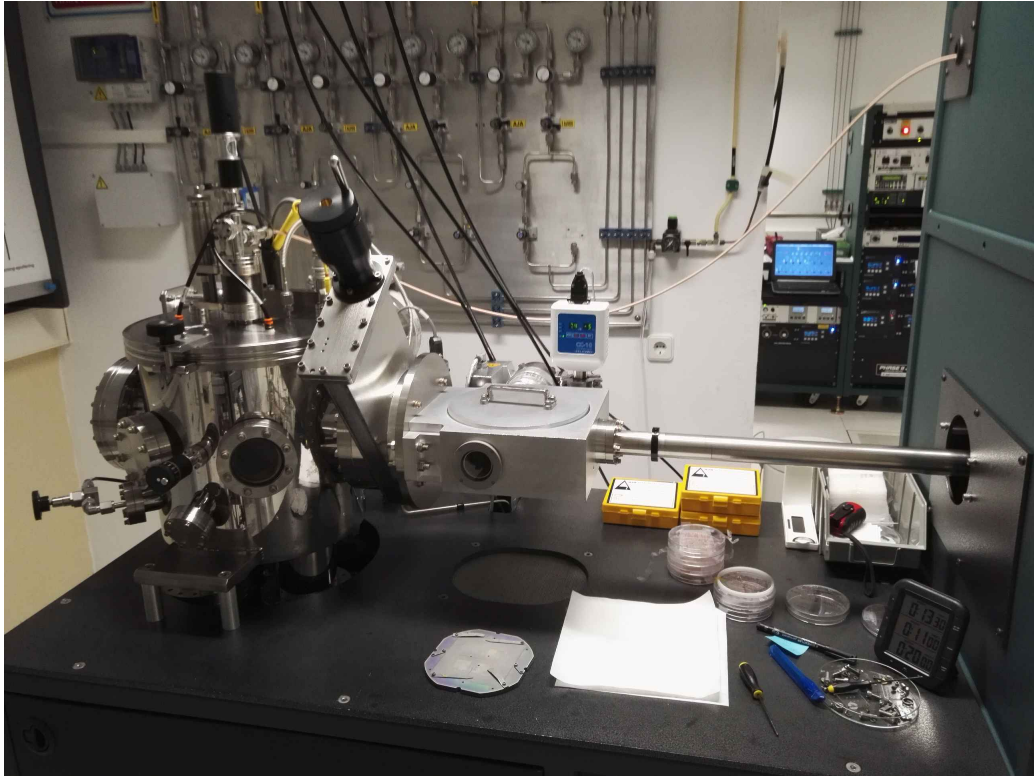
and thermal equilibrium. In oxide semiconductors, for example, thermal treatments reduce the density of impurities and defects that would otherwise act as electron traps, enhancing mobility, or allow the channel to absorb more oxygen reducing the number of vacancies, thus reducing free carrier density and bringing the turn on voltage closer to 0 [5]. Other than that, annealing allows to reduce residual mechanical stress generated during deposition that could reduce the device's bendability.

In this work, post-deposition annealing has been performed by putting the devices on a hot plate (Torrey Pines ECHOTerm) at 180 °C for one hour.

2.8 Production flow

Below are all the steps of the production of the devices.

- Substrate preparation
  - PDMS preparation
  - Ultrasound 10x10 cm glass cleaning
  - PEN sheets cutting
  - Spin coating of PDMS on glass and application of PEN sheets



a. Aja1, used for semiconductor and dielectric deposition

b. Aja3, used for contact deposition

Figure 2.8: Sputtering machines used for deposition

  - Drying on furnace
  - Dicing into 4 5x5 glasses with a PEN sheet each
- Gate electrodes
  - Molibdenum deposition
  - Photoresist spin coating
  - Soft-baking
  - Exposure at mask aligner
  - Development
  - Reactive Ion Etching
  - Removal of residual photoresist by dipping substrate in acetone
- Dielectric
  - SiO2/TsiO deposition
  - Photoresist spin coating
  - Soft-baking
  - Exposure at mask aligner
  - Development
  - Reactive Ion Etching
  - Removal of residual photoresist by dipping substrate in acetone
- Semiconductor channel
  - Photoresist spin coating
  - Soft-baking
  - Exposure at mask aligner
  - Development
  - a-IGZO deposition
  - Lift-off
- Source/Drain Electrode
  - Photoresist spin coating
  - Soft-baking

- Exposure at mask aligner
- Development
- Molibdenum deposition
- Lift-off

3

Light response measurements

In this chapter, the methods for light response measurements will be described. In particular, the focus will be first on light, in particular light generation and filtering, and then on electrical signals, in particular on how to link transistor current with the intensity of response to light using the lock-in amplifier.

3.1 Light generation

To study the photoresponse of the TFT at different wavelengths, a source that could produce light on a continuous spectrum was needed. To achieve this, a Xenon arc lamp has been used.

Xenon arc lamps are a type of gas discharge lamps. In this lamp, two electrodes are put close to each other in a glass bulb filled with xenon gas. When a strong electric field is generated at the electrodes, the gas between them is ionized. Positive ions will move towards the cathode, where they will collide with other neutral atoms and acquire an electron for them. The atom having been ionized will start moving towards the cathode, while the ion, having gained an electron, will emit a photon. The energy needed to free the electron from the neutral atom for it to recombine with the ion is given by the kinetic energy of the ion. While ions migrate towards the cathode, electrons migrate end get absorbed by the anode. This impact causes the anode to overheat, and this it requires a water cooling system. The light emitted from a Xenon lamp is white, with a spectrum similar to the one emitted by the sun. It emits almost continuously from a wavelength of 250 to 1000 nm, with peaks in the 850-900 nm region, that contain around 10% of

the photons emitted [33].

3.2 Light filtering

To get from a continuous spectrum to monochromatic light, a monochromator has been used.

Monochromators can select light wavelength via the use of a reflection grating. A reflection grating is a collection of reflecting elements separated by a distance comparable to the wavelength of light under study [34].

When monochromatic light is incident on a grating surface, it is reflected into discrete directions. Each grating groove can be seen as a very small, slit shaped source of reflected light, that combines with the one produced by all other grooves. The usefulness of gratings is in the fact that for every wavelength and for a given spacing d between grooves, there will be an angle at which the reflected light from each groove will be in phase with the light reflected from any other groove.

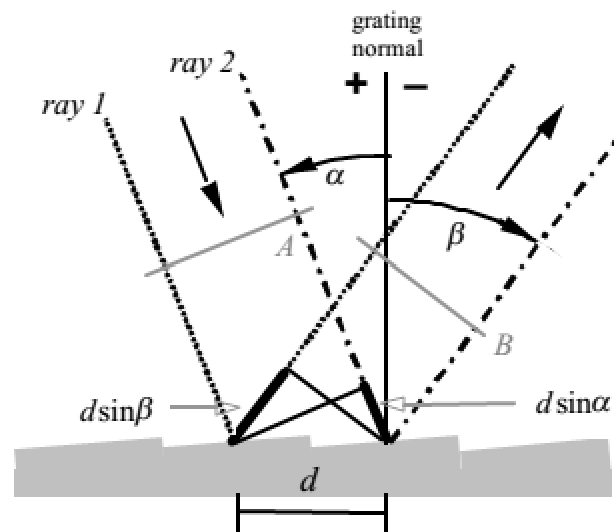


Figure 3.1: Scheme of a diffraction grating [34]

Reflection can be visualized from the geometry in figure 3.1, which shows a light wave front of wavelength λ incident at an angle α and reflected at an angle β. By convention angles are measured from the grating normal to the incident/reflected ray. The geometrical path difference between two adjacent grooves is $d \sin \alpha + d \sin \beta$. The condition for constructive interference is that the path difference must be equal to an integer multiple of the wavelength. If this condition is not satisfied, the light reflected from grooves will interfere

destructively and thus be nullified. If the incoming light is white, every wavelength will be dispersed. In a given direction the wavelengths in the reflected light that will not be nullified by destructive interference will be the ones for which the relation $m\lambda = d\,(\sin\alpha + \sin\beta)$ holds.

This fact has two consequences: first, by changing the orientation of the grating with regard to the incoming light, both α and β will be increased by the angle between the incoming light and the grating normal. This means that by changing the orientation we can obtain the effect of changing the wavelength λ that will satisfy the relation. The second consequence is that if the relation is satisfied by λ, it will also be satisfied by $\frac{\lambda}{2}, \frac{\lambda}{3}, \frac{\lambda}{4} \ldots$ (the wavelength harmonics). This might cause a problem: if for example we want to use the monochromator to select 800 nm from the white light in a particular direction, the 400, 267 and 200 nm will also be selected (see figure 3.2).

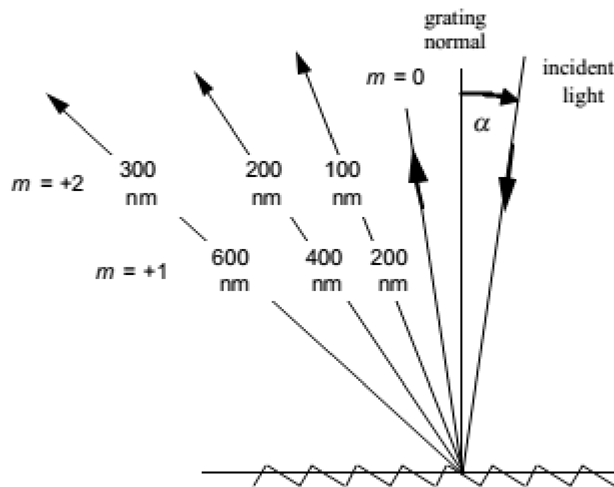


Figure 3.2: Scheme of the overlap of light from several diffraction orders [34]

In this setup, the monochromator is paired with a Xenon light, and used to investigate a-IGZO devices. Which means that on one side, knowing amorphous oxide semiconductors bandgap, we can "guess" that the most important wavelength ranges will be the ones below 400-500 nm, whose harmonics fall at the edge of the lamp emission spectrum. Other than this, a filter can be used to block ultraviolet harmonics when wavelengths between 400 and 500 nm are selected.

In order for the diffraction grating to work, incoming light must be collimated, which in terms of classical optics means light wave fronts should be all parallel to each other. Other than this, light must be directed from the light source to the grating to the TFT and its intensity must be maximized.

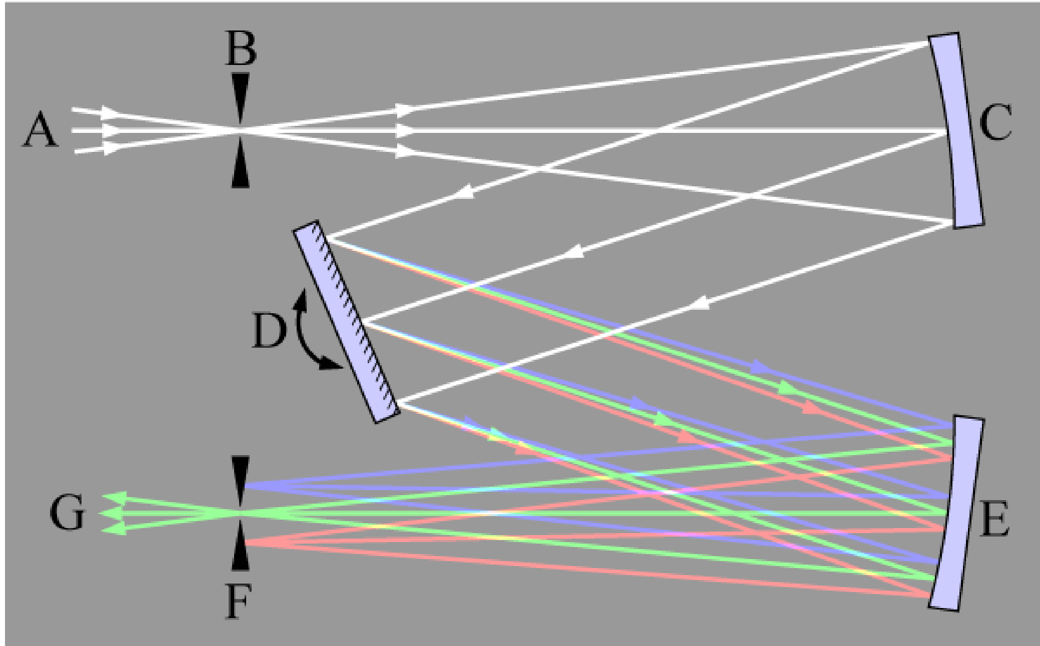


Figure 3.3: Diagram of a Czerny-Turner monochromator

To achieve all of these goals, an optical system must be implemented, that involves both the Xenon arc lamp and the monochromator. First, the light that comes out of the Xenon Arc Lamp. First, the light passes through a converging lens. The distance between the lens and the centre of the slit is equal to the lens focal distance. This way most of the light will enter the slit. To collimate the convergent light, a concave mirror is used to reflect the light onto the grating. Another concave mirror reflects the light in a particular direction into the exit slit, where the light has the same degree of collimation it had when it exited the light source. This setup is known as the Czerny-Turner monochromator, a diagram of which is shown in figure 3.3.

3.3 Electrical measurements

Electrical measurements have been performed using an electrical source meter.

Two different electrical measurements have been performed. First, threshold voltage shift and subsequent relaxation was measured under 400, 365, 300 and 250 nm light exposure. Drain current was measured while keeping Drain voltage at 0.5 V and putting the gate voltage at the values −1 V, 0 V, 1 V, 2 V, 3 V, 4 V, 5 V. After obtaining these values, threshold voltage was calculated by performing a linear fit of the square root of the drain current as a function of gate voltage. The slope of this fit will be the threshold voltage.

These measurements were performed once every 3 seconds during the process. While measurements weren't in progress all contacts were left grounded. The measurement started by leaving the device in the dark for 300 seconds, in order to evaluate the threshold voltage value before light exposure. The device was then illuminated for 60 seconds. Afterwards, measurement continued until threshold voltage went back to pre-exposure values.

Second, the output of the TFT devices was measured in dark and after 5 seconds of light exposure. The output characterization consisted in measuring the gate current while sweeping the drain voltage at different gate voltages. In particular, the sweep was from −0.5 V to 5 V with a 0.2 V step for the drain voltage and from −5 V to 5 V with a 1 V step for the gate voltage.

The third measurement involves measuring the response to light exposure for every wavelength from 500 nm to 200 nm with a step of 10 nm. There is an important issue for this particular setup: device response to light is quantified as photocurrent, which is known to increase with light exposure time. Which means that with the setup as it is, photocurrent will depend on previous exposure too. In other words, photocurrent measured when the device is exposed to 300 nm light will also depend on how much charge was generated during exposure to 310 nm, 320 nm and so on.

A way to overcome this issue is to use another electronic device known as lock-in amplifier

3.4 Lock-in Amplifier

Lock-in amplifiers are used to detect very small AC signals, down to the order of nanovolts, even while the signal is obscured by noise orders of magnitude larger. In particular they single out the component of the signal at a specific frequency through a technique known as phase sensitive detection (PSD) [36].

This technique consists in multiplying a sinusoidal signal $V_{sig}\sin\left(\omega_r t + \theta_{sig}\right)$ with another sinusoidal reference signal (lock-in reference) $V_L sin\left(\omega_L t + \theta_{ref}\right)$. The output of the phase-sensitive detection is the product of the two sine waves:

$$V_{psd} = V_{sig} V_L \sin\left(\omega_r t + \theta_{sig}\right) \sin\left(\omega_L t + \theta_{ref}\right)$$

Using trigonometry:

$$V_{psd} = \frac{1}{2} V_{sig} V_L \cos\left[(\omega_r - \omega_L) t + \theta_{sig} - \theta_{ref}\right] - \frac{1}{2} V_{sig} V_L \cos\left[(\omega_r + \omega_L) t + \theta_{sig} + \theta_{ref}\right]$$

The PSD will thus give an output that is the sum of two sinusoidal signals, one at the difference frequency $\omega_r - \omega_L$ and the other at the sum frequency $\omega_r + \omega_L$. If this output is passed through a low pass filter, the AC signal will be removed. In general, the entire output will be removed. The only case when something passes is if one of the two components goes from being a sine wave to being a constant signal. The only way this can happen is if $\omega_r = \omega_L$. In this case, the filtered PSD output will be $V_{psd} = \frac{1}{2} V_{sig} V_L \cos(\theta_{sig} - \theta_{ref})$. In other words, the output will be a DC signal proportional to the signal and the lock-in amplitude which, being provided by the user, is known.

In a real scenario, the input will be made out of a sum of actual signal and noise. The PSD will be applied to all frequencies, and the low pass filter will consequently attenuate signals far from the lock-in reference frequency. Only noise with frequency very close to the lock-in reference will be detected as very low frequency AC ($|\omega_{noise} - \omega_{ref}|$ is small) outputs while the signal whose frequency matches the reference will be be detected as a DC signal. The level of attenuation for signals that are not at the reference frequency, depends upon the low pass filter configuration, in particular in its bandwidth. The narrower the bandwidth, the more the filter will remove noise signal even when its frequency is very close to the reference. To make sure that when $\omega_r = \omega_L$ the PSD output will be a DC signal, $\theta = \theta_{sig} - \theta_{ref}$ must be indipent of time. In order to obtain that, a phase locked loop is used which locks the internal reference oscillator to this internal reference when an external reference wave is provided. Even if it's constant in time, the PSD output depends on this phase difference. In order to eliminate this dependency, a second PSD can be added. This PSD multiplies the signal with a reference shifted by 90°, which will be $V_L \sin(\omega_L t + \theta_{ref} + 90°)$. In the case $V_L = 1\acute{V}$ its own low-pass filtered PSD output will be

$$V_{psd2} = \frac{1}{2} V_{sig} V_L \sin(\theta_{sig} - \theta_{ref}) = \frac{1}{2} V_{sig} \sin\theta$$

Now there are two outputs: V_{psd}, proportional to $\cos\theta$ and V_{psd2}, proportional to $\sin\theta$. If these two signals are called X and Y we have

$$X = \frac{1}{2}V_{sig}\cos\theta \qquad and \qquad Y = \frac{1}{2}V_{sig}\sin\theta$$

These two quantities represent the signal as a vector relative to the lock-in reference oscillator. X is called the "in-phase" component, while Y is the "quadrature component". When $\theta = 0$, X measures the signal while Y is zero.

This way, if instead of X or Y we calculate the magnitude R of this vector, we have

$$R = \sqrt{X^2 + Y^2} = \sqrt{\frac{1}{2}}V_{sig}$$

Which is the root mean square amplitude of the input signal and is independent from the phase difference with the lock-in reference. If for example the lock-in amplifier displays a magnitude of 1 V, the corresponding peak-peak amplitude of the component at the reference sample will be $V_{p\text{-}p} = 2V_{sig} = 2\sqrt{2}R \sim 2.8V$

Also using X and Y, the phase can also be measured as

$$\theta = \tan^{(-1)}\frac{Y}{X}$$

As for the Fourier theorem, any signal can be described as a sum of sine waves of differing amplitudes, frequencies and phases, known as a Fourier expansion. A signal represented by the elements of this sum is said to be represented in the frequency domain, as opposed to the time domain (the way for example an oscilloscope represents the signal). In other words, the lock-in amplifier measures the amplitude of a specific line in the frequency domain of the signal. If the input signal is a sine wave, then its RMS and the PSD signal's amplitude will coincide, but in general they won't. In that case the PSD signal will only give the amplitude of one of the sine components. For example, let's suppose that the signal is a triangle wave and the reference is at the same frequency. The Fourier expansion for a triangle wave V_T with 2 V peak-peak amplitude, frequency ω and phase 0 is:

$$V_T\left(t\right) = \frac{8}{\pi^2}\sum_{k=0}^{\infty}\left(-1\right)^k\frac{sin\left[\left(2k+1\right)\omega t\right]}{\left(2k+1\right)^2} = \frac{8}{\pi^2}\sin(\omega t) - \frac{8}{9\pi^2}\sin\left(3\omega t\right) + \frac{8}{25\pi^2}\sin\left(5\omega t\right) - \ldots$$

Consequently, the measured signal will actually be $\frac{8}{\pi^2}\sin(\omega t) \sim 0,8106\sin(\omega t)\,\mathrm{V}$ and the displayed magnitude will be $\sqrt{\frac{1}{2}}0,8106\ \mathrm{V} \sim 0,5732\ \mathrm{V}$.

The diagram for the lock-in amplifier is shown in figure 3.4:

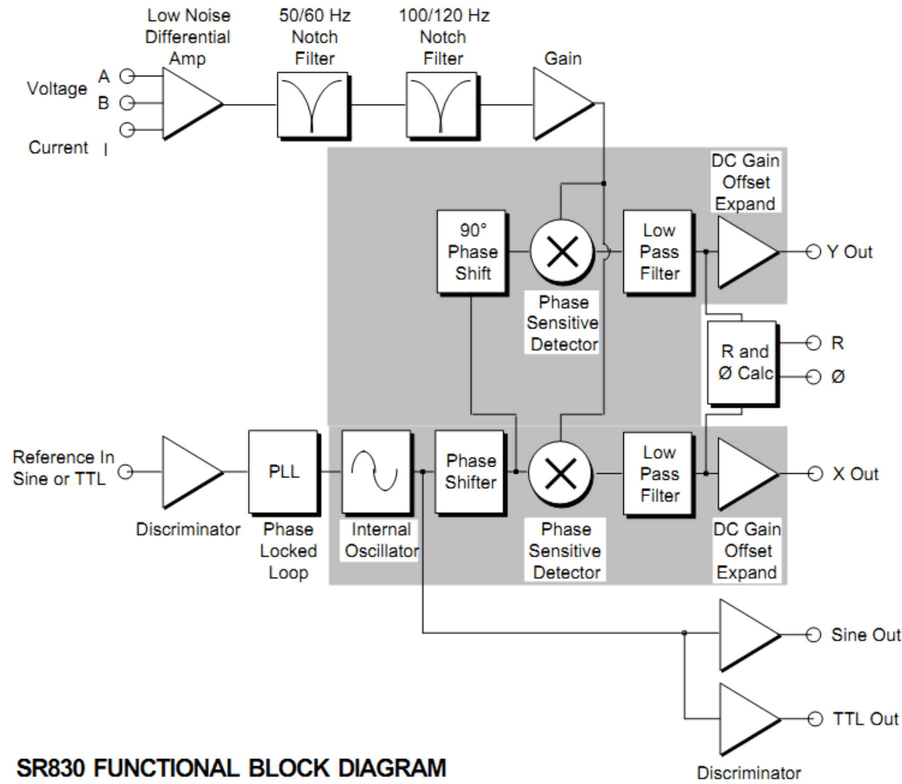


Figure 3.4: Functional Block diagram of the SR830 [36]

One more thing to note is that the lock-in amplifier presents low pass filters with different time constants (which is the RC product) to be chosen depending on the measurement. Lock-in amplifiers usually employ RC low pass filters. Their cut-off frequency, which is defined as the frequency at which the transmission function (which determines amplitude attenuation for a given frequency) is $-3\,\mathrm{dB}$, is dependent on the time constant $as f_c = \frac{1}{2\pi RC}$. In addition, multiple filters can be added in sequence. Having more filters in sequence increases the steepness of the transmission function after the cut-off frequency, as in figure 3.5 on the next page

The steepness is defined as slope of the function beyond the cut-off frequency vs the logarithm of the frequency, and is measured as dB/Octave (every octave is equivalent to doubling the frequency). Each filter has a roll-off

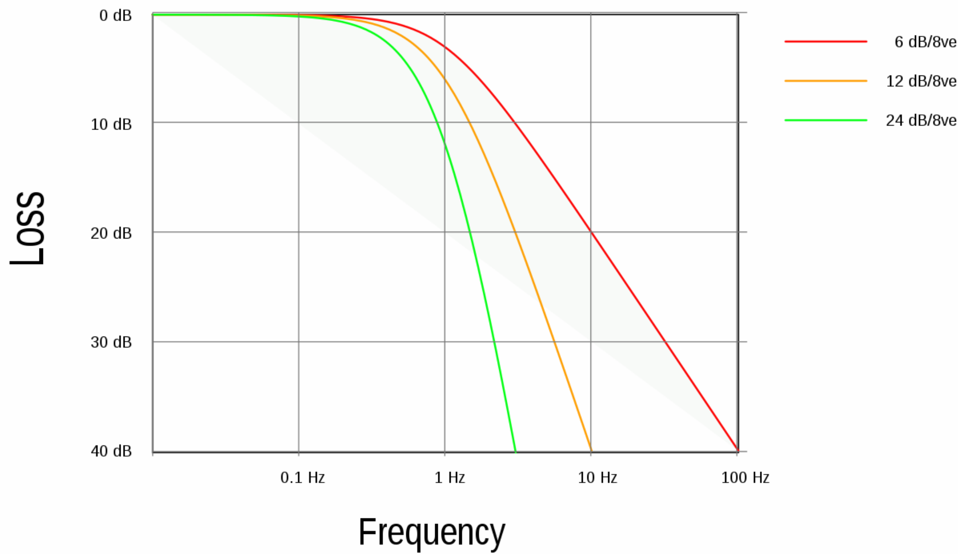


Figure 3.5: Graph showing filtering curves at different Roll-off values

of 3 dB/oct. The SR830 amplifier used in this experience can use 2, 4, 6 or 8 filters in sequence, equivalent to 6 dB/oct, 12 dB/oct, 18 dB/oct and 24 dB/oct.

It is clear that the higher the time constant and the roll-off used, the narrower and steeper the attenuation will become and the less the noise that will be present after the filtering, causing the measurement to be less noisy overall. While using longer time constants will reduce noise, it will also take more time to react to any change with the signal. As a rule of thumb, it has been assumed that the time needed to stabilize is around twenty time constants. The Roll-off also contributes to this effect, even though to a lesser extent.

In order to use the lock-in amplifier, one issues must be solved: the amplifier can only read voltage signals, and the photoresponse studied is a current signal. In order to solve this problem, a transimpedance amplifier can be used to convert and amplify the signal [19]. The output of a transimpedance amplifier (shown in figure 3.6 on the following page) is

$$V_{out} = -I_p R_f$$

And thus, the voltage signal can be easily amplified by changing the resistance

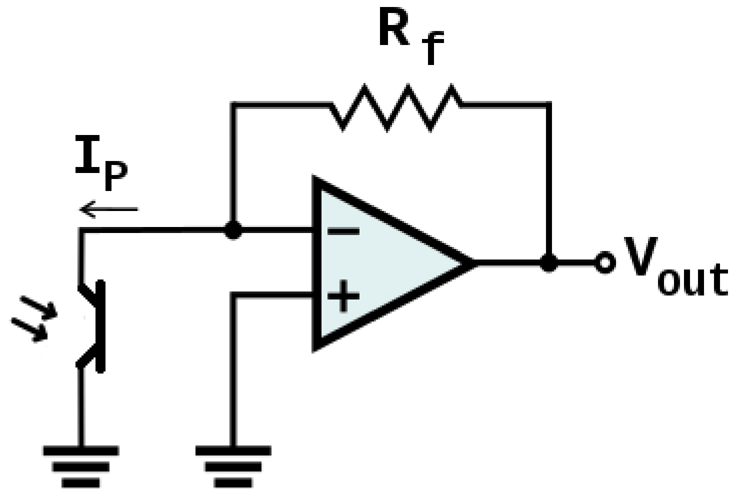


Figure 3.6: Scheme of a transimpedance amplifier

3.5 Spectrum response setup

In order to keep the photocurrent from continuously increasing under exposure, a chopper will be used to keep the light intermittent by periodically covering and uncovering the lightsource. The frequency of the intermittence can be controlled by an outside source, which will also provide a square signal with the same frequency which will be used as a reference trigger for the lock-in amplifier. Assuming the photogeneration model applies for the TFT, the current will be proportional to the charge density in the semiconductive channel, which varies as $\frac{d\sigma}{dt} = Gdt + R\sigma$ where G is the generation rate and R is the recombination rate. If the base charge density is high enough and the intermittence is frequent enough, the current will approximate a triangular wave, with a frequency equal to the one of the intermittence. Being at the same frequency as the lock-in reference it will be possible to measure the amplitude of the main sine component. From that the amplitude of the triangular wave can be evaluated and the amplitude of the photoresponse can be assessed.

3.6 Lightsource spectrum measurement

Since the light source power is not the same at all wavelengths, it will be necessary to measure it with the use of a pyroelectric sensor. These sensors are structured as a capacitance where the dielectric has the property of polarizing itself with changes in temperature. This polarization induces voltage in the

plates. In order to make sure the sensor keeps heating with light exposure, the light must be intermittent. Otherwise, the temperature increase would cause the entity of the temperature change to progressively decrease. With the use of a chopper to allow the sensor to cool down after every exposure, the voltage signal will be constant and dependant on the emission power.

4 Results

Here the results of the measurement protocols discussed before are shown. In particular, the main focus of this chapter is to demonstrate how these devices can be used as reliable UV sensors. In particular, in the first two sections, the fabricated devices and their electrical characterization are reported, alongside a rough estimate of their conductive performance. After this, the photoresponse is characterized, by first measuring the responsivity spectrum and the effect of light on output, mobility and threshold voltage. Response to consecutive light stimula is also shown. Finally, a device application in a RFID circuit is reported.

4.1 Fabrication

The n-channel thin-film transistor devices were fabricated in CEMOP and CENIMAT laboratories at FCT Nova in Lisbon (Portugal), where I spent 4 months as an Erasmus student, under the supervision of Prof. P.Barquina, following the process described in chapter 2. The devices, shown in photo and at a 1000x magnification in figure 4.1 on the next page have a staggered, bottom-gate structure. No passivation layer was applied on the samples.

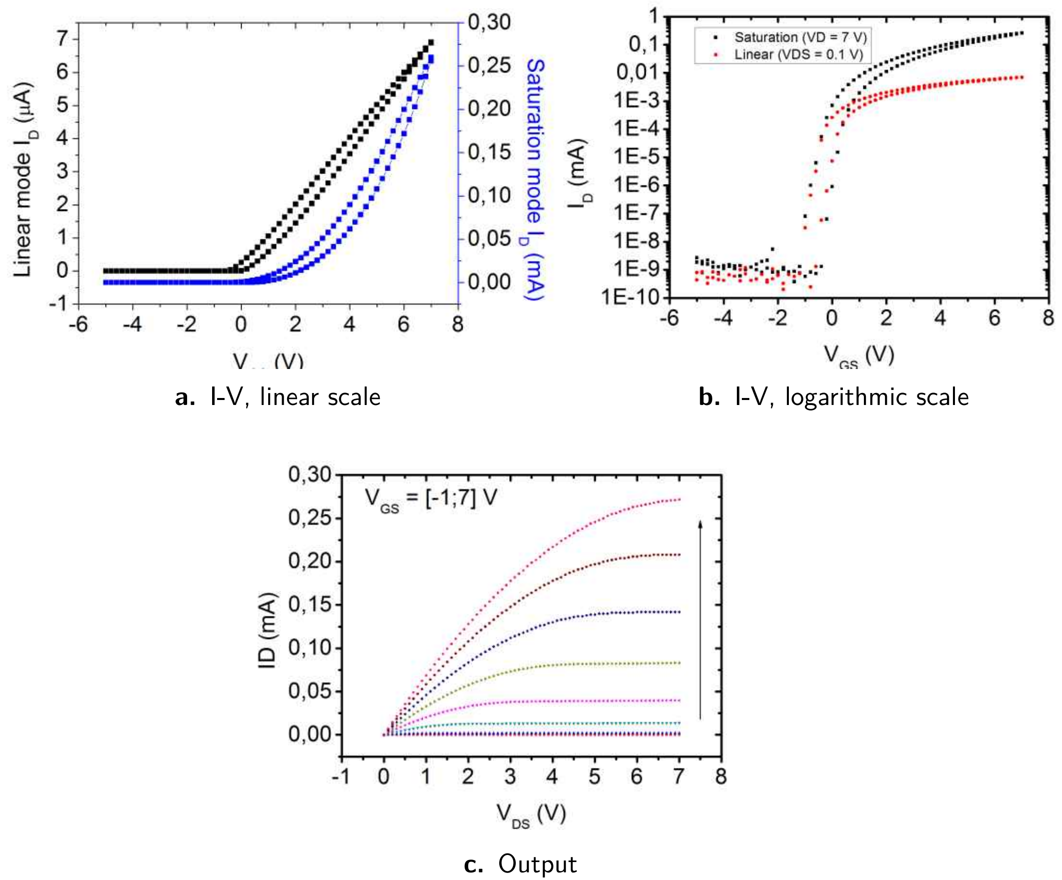
4.2 Electrical characterization

Part of the fabricated devices was characterized at the probestation to estimate the yield of the process. Out of 133 devices investigated, 93 were found to be

a. Device substrate, with 36 devices

b. Detail of a single device (1000x magnification)

Figure 4.1: Fabricated devices



a. I-V, linear scale

b. I-V, logarithmic scale

c. Output

Figure 4.2: TFT current-voltage characteristics and output

working, while the others were either never conducting or always conducting. This equals a yield of around 70%.

Out of the working devices, a sample of 25 was taken to evaluate mobility, subthreshold swing, threshold voltage and turn on voltage in both saturation and linear mode. In order to do that, linear and saturation I-V characteristics (in particular drain current as a function of gate voltage) were taken. An example of these characteristics and output current are shown in figure 4.2 on the facing page. From these characteristics parameter values distribution have been extracted, and are shown in figures 4.3, 4.4, 4.5 on the next page and 4.6 on page 47.

Rough estimates of the parameters were obtained, by using the average of the distribution as estimate and the standard deviation as error. What can be seen in particular is that the mobility values are $\mu_{lin} = (16 \pm 3)\,\mathrm{cmV^{-1}s^{-1}}$ and $\mu_{sat} = (16 \pm 3)\,\mathrm{cmV^{-1}s^{-1}}$, while subthreshold swing values are $S_{sat} = (0.2 \pm 0.18)\,\mathrm{Vdec^{-1}}$ and $S_{sat} = (0.16 \pm 0.13)\,\mathrm{Vdec^{-1}}$. Precise evaluations cannot be performed due to the low sample population, but results suggest that these samples are promising for TFT application. On the other hand, turn on voltage distribution are peaked on the ideal value of 0, but have broad distributions.

4.3 Responsivity spectrum

First, the measurement of the photoresponse as a function of incoming wavelength has been measured, following the procedure shown in the previous chapter.

First of all, the spectrum of the Xenon lamp has been measured and is shown in figure 4.7 on page 48.

In order to evaluate the device responsivity at a certain wavelength, the current amplitude must be normalized using the lamp's intensity. The responsivity is thus calculated as

$$R(\lambda) = \frac{J_{p-p}}{I(\lambda)\,LW}$$

where J_{p-p} is the current peak-peak amplitude (extracted as discussed in the previous chapter), $I(\lambda)$ is the lamp's intensity for a given wavelength and L and W are the channel length and width (20 and 320 μm respectively).

Two different measurements were performed: one where the device was kept at V_{GS} = -5 V and V_{DS} = 0.5 V and the other where it was kept at

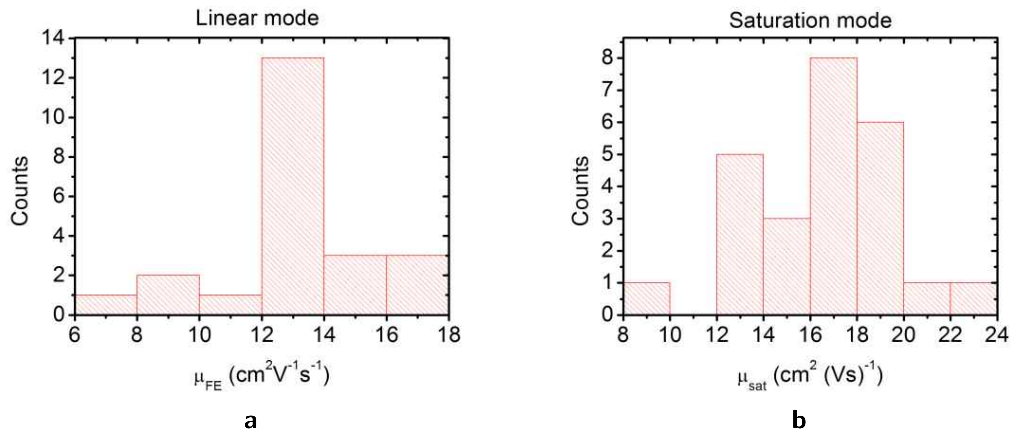


Figure 4.3: TFT mobility distribution

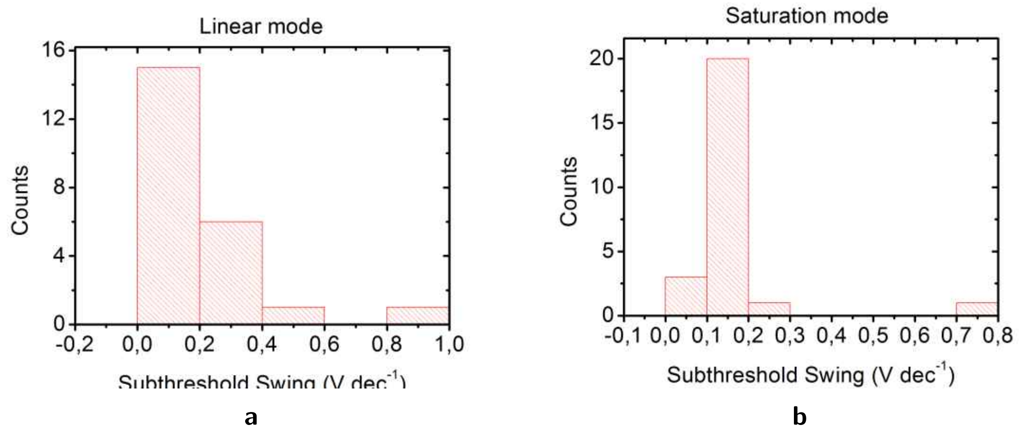


Figure 4.4: TFT subthreshold swing distribution

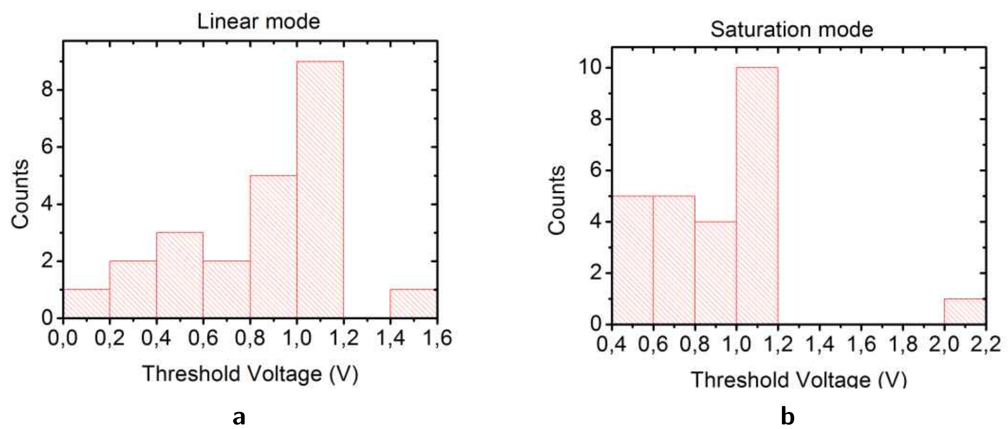


Figure 4.5: TFT threshold voltage distribution

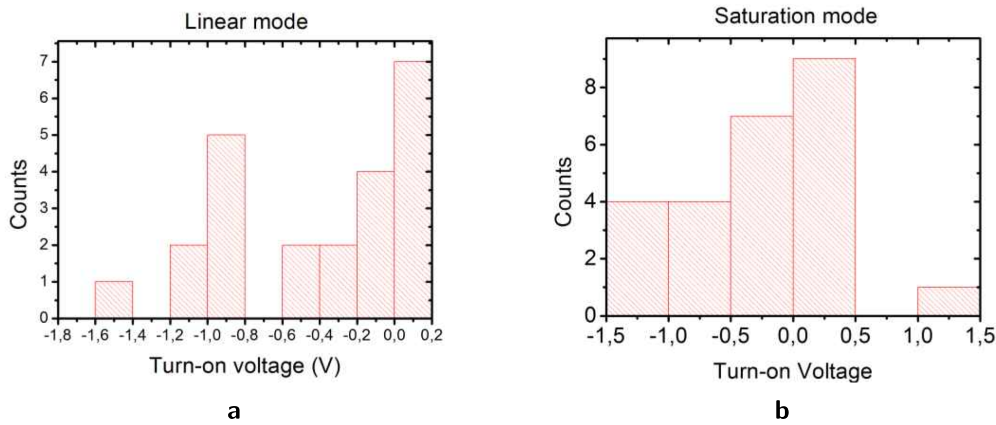


Figure 4.6: TFT turn on voltage distribution

$V_{GS} = 5$ V and $V_{DS} = 0.5$ V, corresponding respectively to the situation where the channel would be depleted of carriers without light (depletion mode) and the situation where the channel would already be open (accumulation).

Results are shown in figure 4.8 on page 49 in linear scale and in figure 4.9 on page 49 in logarithmic scale.

What can be seen is that the responsivity starts increasing between 410 and 400 nm in depletion and between 400 and 390 in accumulation mode. With decreasing wavelength, there is a progressive increase in responsivity that peaks at 310 nm. Afterwards, it starts decreasing until it reaches a local minimum at 290 nm. At 280 nm, it starts increasing again in a similar way as before (wavelength values below 230 nm weren't taken into consideration, because the light emitted by the Xenon lamp was too weak to give reliable results).

It can be concluded that, while the devices could work for violet light, they will be more indicated for UV sensors. Thus, from now on the focus will be on response to UV light. This is in agreement with results obtained in literature [1, 9, 24].

4.4 Effect of light on TFT output

Output values were measured in the way illustrated in the previous chapter: the drain voltage was swept from -0.5 to 5 V back and forth, with a 0.2 V step, while the gate voltage was swept from -5 to 5 V with a 1 V step.

Output measurements were taken with the device in the dark and after 5 s of light exposure at 365, 300 and 250 nm. The results are shown in figures 4.10

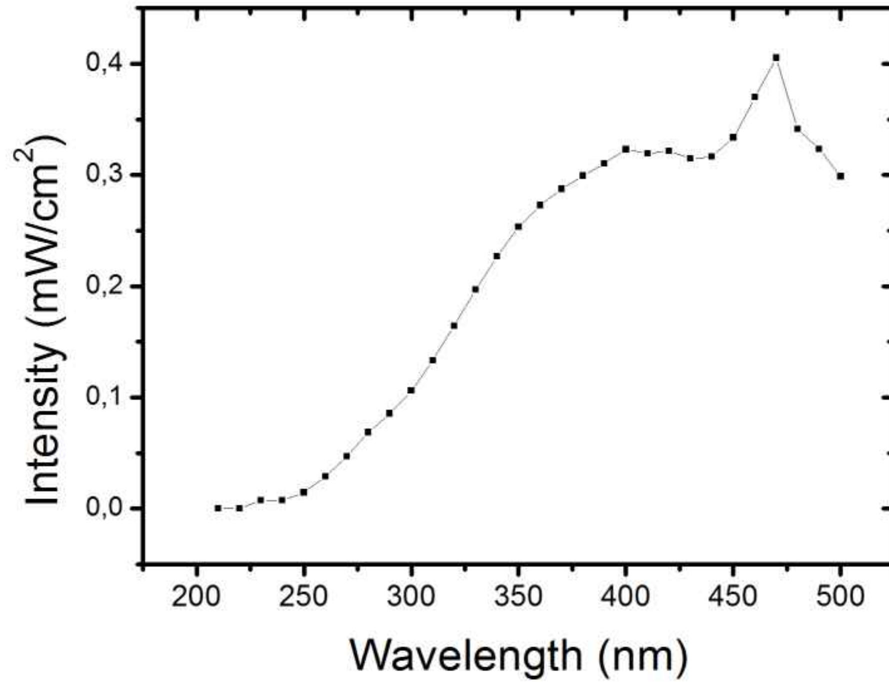


Figure 4.7: Intensity spectrum of the Xenon lamp

on page 50 at a 5 V (a-c) and at a -1 V (d-f) gate voltage.

Output current increases with light exposure, and lower wavelengths cause higher increases, which is in accordance with the responsivity curve shown above.

These measurements can also be used to show the current variation as a function of drain voltage, gate voltage and wavelength. In particular, in figures 4.11 on page 51 current variations as a function of gate voltages with 0.3 and 5 V drain voltage are shown.

What can be seen is that for drain voltages closer to 0 the responsivity grows in an irregular fashion: the current variation grows with gate voltage up until 1 V, at which point it starts dropping, except for the case where the incoming light is 250 nm. An explanation for this phenomenon will be given in section 5.2 on page 64 in the next chapter. For higher drain voltages the responsivity instead grows with V_{GS}, following a curve similar to the one the current follows.

What can be deduced from these results is that light emission increases current flowing through the transistor. Dependency between current, gate and threshold voltage is determined in saturation by

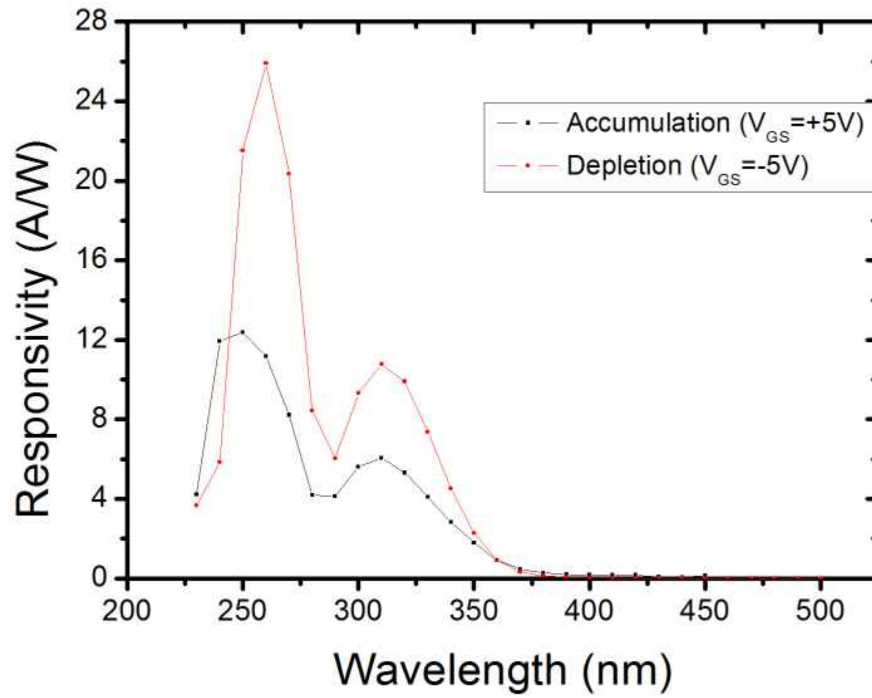


Figure 4.8: Responsivity spectrum

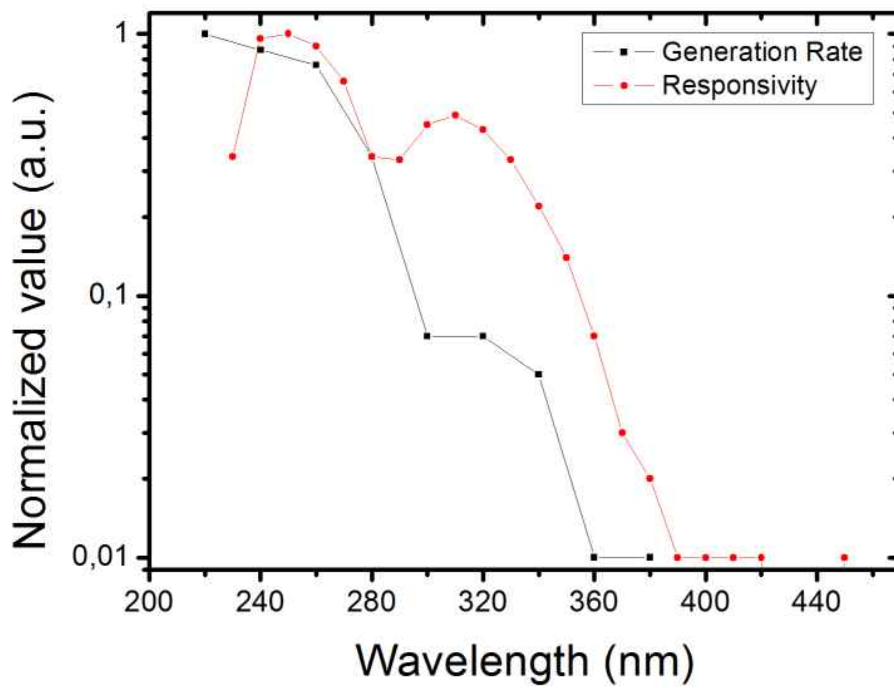
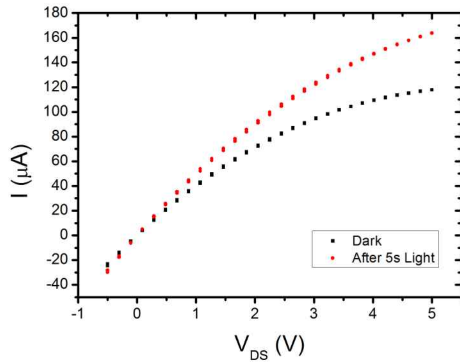
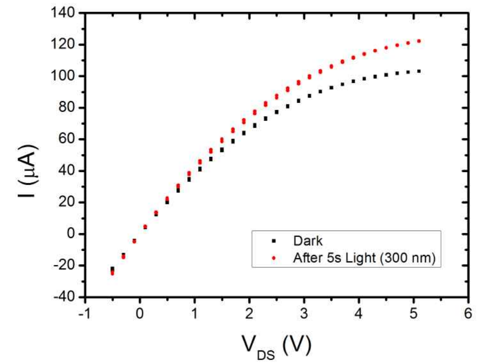


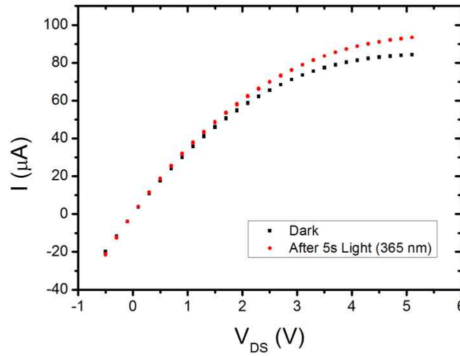
Figure 4.9: Responsivity spectrum (logarithmic scale)



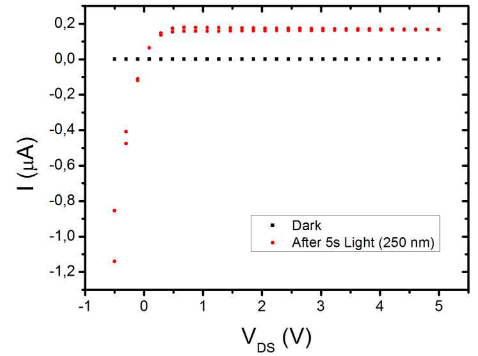
a. 250 nm



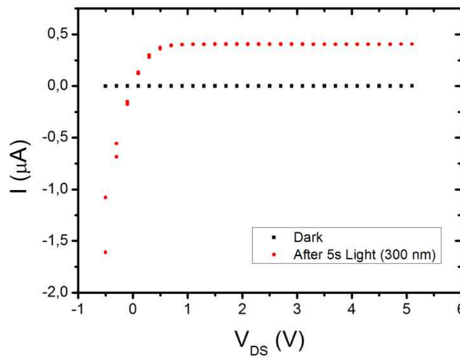
b. 300 nm



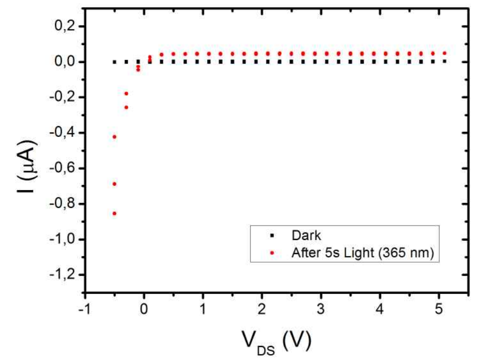
c. 365 nm



d. 250 nm

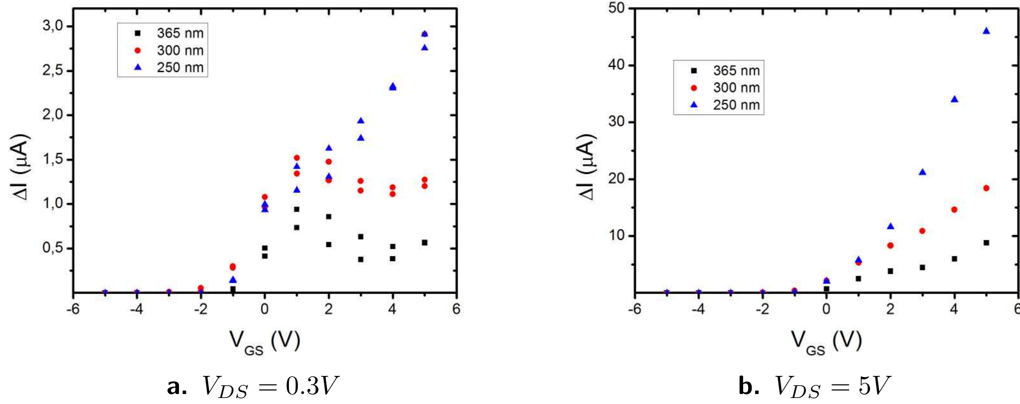


e. 300 nm



f. 365 nm

Figure 4.10: Effect of light on output when V_{GS}=5 V (a-c) and -1 V (d-e)



a. $V_{DS} = 0.3V$ **b.** $V_{DS} = 5V$

Figure 4.11: Current variation as a function of gate voltage (left) and (right)

$$I_D = C_i \mu_{sat} \frac{W}{2L} \left(V_{GS} - V_{th}\right)^2$$

where I_D is the drain current, C_i is the capacitance of the dielectric (estimated at 50 nFcm^{-2}), μ_{sat} is the saturation mobility, V_{GS} is the gate voltage (with respect to the source, which is grounded) and V_{th} is the threshold voltage.

In other words, if current is increased under illumination, at least one of two different effect must occur: either the field effect mobility has increased, or the threshold voltage has decreased.

These two possibilities can be evaluated by measuring I_D at different V_{GS} values (from -1 to 5 V, with a step of 1 V) with a constant V_{DS} value of 5 V so that the device always operates in saturation mode.

4.4.1 Effect of light on TFT mobility

Some of the curves obtained this way at different times are shown in figure 4.12 on the next page as a function of V_{GS}. During the experiment, the device was left in the dark for the first 330 seconds, then was illuminated under 250 nm light for 60 seconds and then left in the dark again for the remaining time.

According to the formula, by performing a linear film in the form of $\sqrt{I_D} = a + bV_{GS}$ the slope will be $b = \sqrt{C_i \mu_{sat} \frac{W}{2L}}$ and thus the mobility will be defined as $\mu_{sat} = \frac{b^2}{C_i} \frac{2L}{W}$

As can be seen by figure 4.12 on the following page, curves taken at different time are all parallel among each other. A mobility value has been extracted from each curve and is shown as a function of time in figure 4.13 on page 53. What can be seen is that values are all somewhat similar, between 9 and

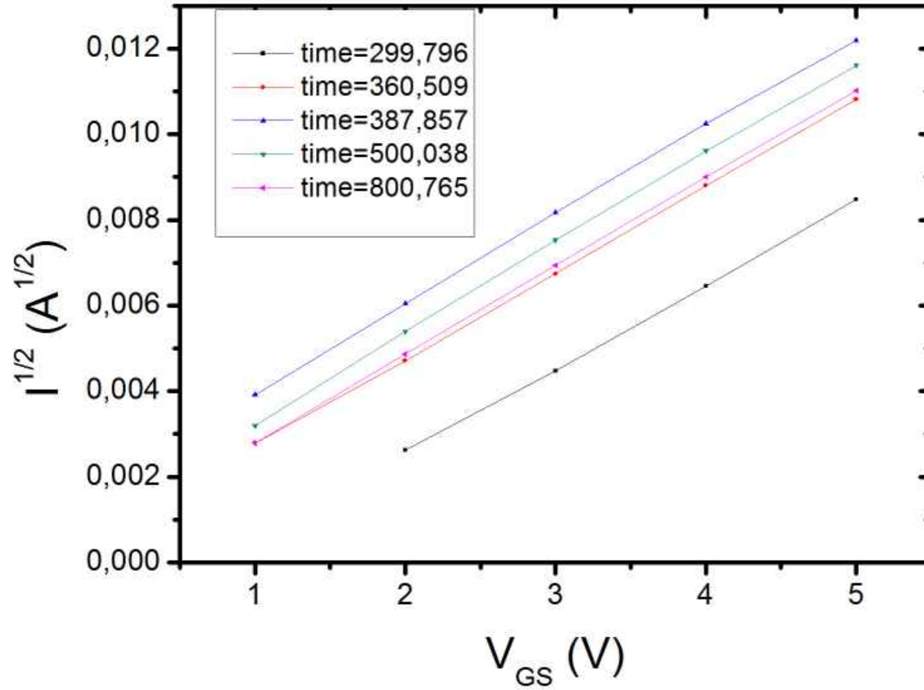


Figure 4.12: Drain currents as a function of gate voltages at different moments during the photoexcitation process

11 cm^{2}V^{-1}s^{-1}. Furthermore, the highest value in mobility appears at 500 s, which is around 140 seconds after light has been turned off. These facts lead to believe that the small variations in mobility are mostly due to random error in the measurement and possibly limited conduction stress in the device.

4.4.2 Effect of light on TFT threshold voltage

Using the same linear fit, the intercept will be

$$a = -V_{th}\sqrt{C_i \mu_{sat} \frac{W}{2L}}$$

and thus the threshold voltage can be evaluated as $V_{th} = -\frac{a}{b}$.

The threshold voltage can thus be evaluated as a function of time. Results are shown in figure 4.14 on page 54, alongside other measurements taken at 300 and 365 nm, performed on different devices.

What can be seen is that in all three cases under illumination the threshold voltage decreases, and once illumination stops it gradually returns to the original value in the range. A lower threshold voltage means that the channel

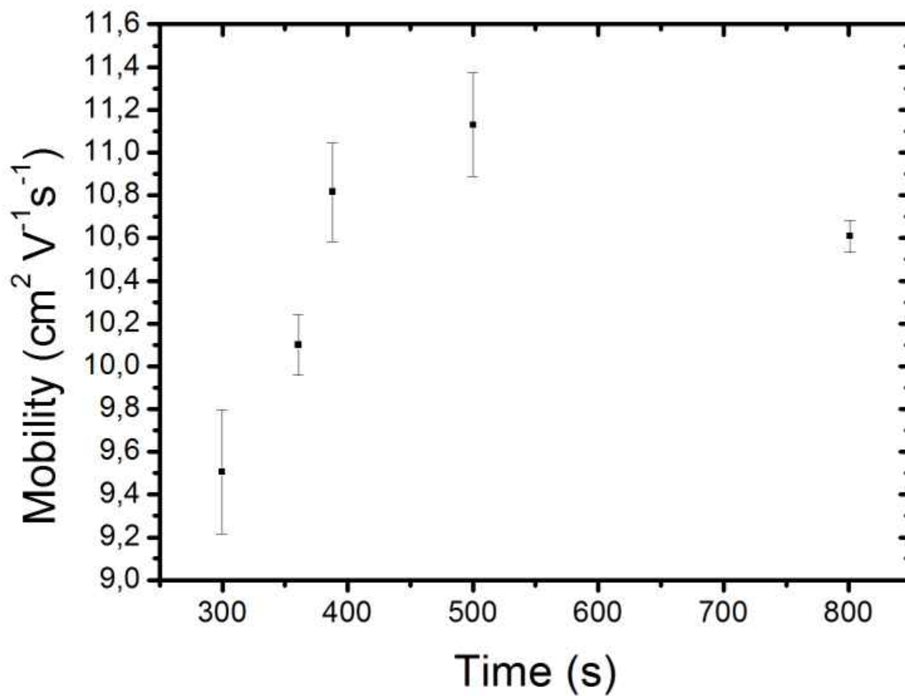


Figure 4.13: Mobility as a function of time

will be more “open”: the final result is a current increase at a given gate voltage under illumination compared to dark. Also, the threshold voltage variation is higher the lower the wavelength is, as is to be expected from what was seen in the responsivity measurements.

Seeing as the mobility didn’t vary substantially with time, it can be concluded that the increase in current is caused exclusively by the light-induced threshold voltage drop.

The curves also clearly show that:

- Devices respond very quickly to illumination: in all three cases the threshold voltage started shifting the moment the light was turned on.
- The shift caused by light is very close to linear, which means that it would probably keep happening for at least several minutes before eventually saturating.
- The curves are highly regular and with very low noise, which suggests that the devices are highly stable, at least in the timescale of seconds.
- The curves are all of similar shape, which suggests this is a common

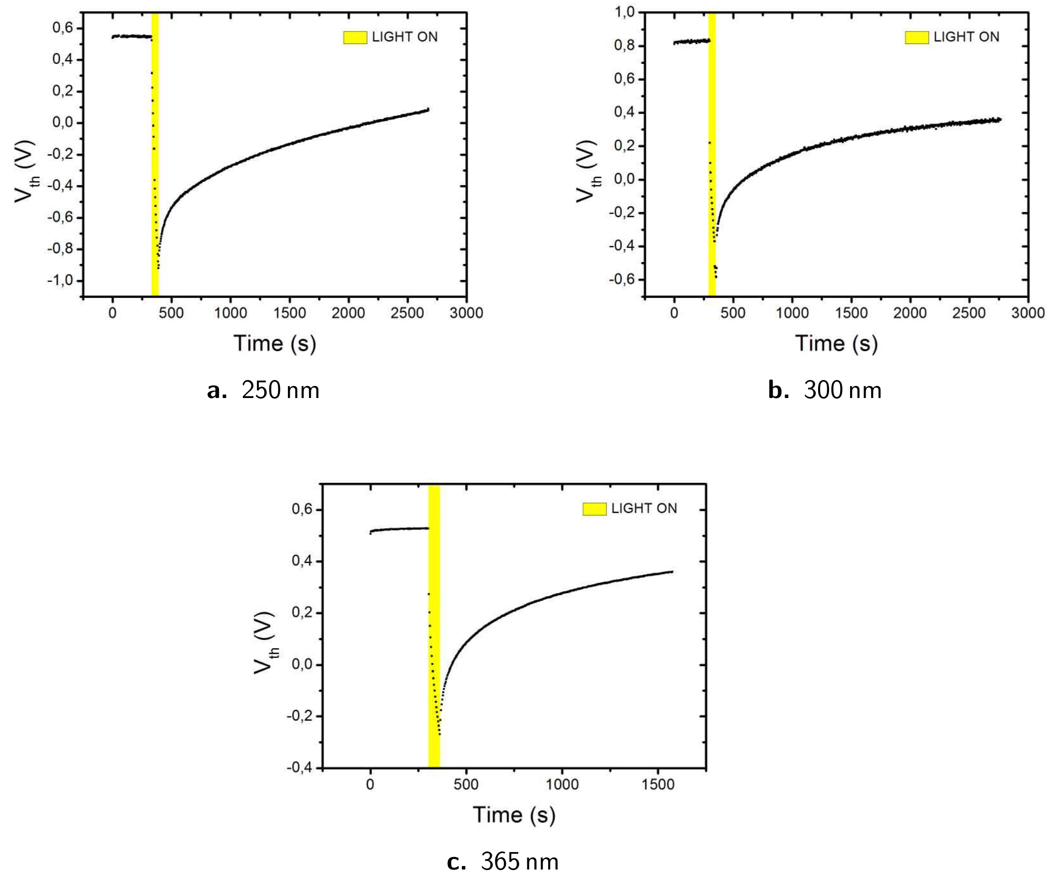


Figure 4.14: Threshold voltage curves at different wavelengths

behaviour of all working devices.

- It is important to note that after these devices were fabricated they were conserved in contact with air and at atmospheric pressure for around 3 months before measurements were performed. This suggests that these kind of devices can remain reliably functional for a long time even without a passivation layer.

All these results lead us to believe that these devices can be employed as reliable and stable UV sensor with a strong response.

A discussion focusing more on what these measurements tell us about the microscopic mechanisms that cause threshold voltage shift is reported in section 5.3 on page 65.

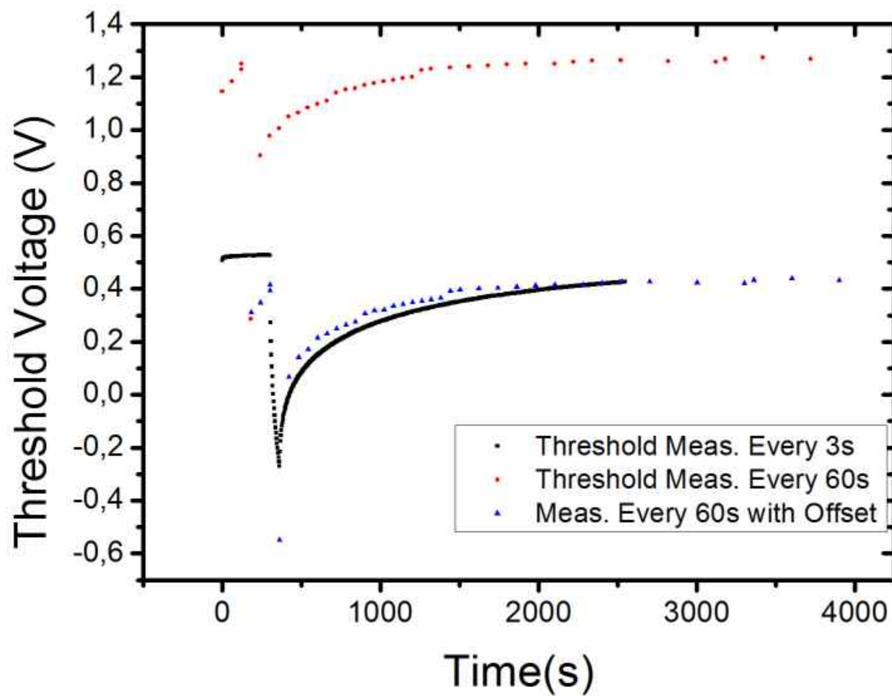


Figure 4.15: Comparison between different sampling rates

4.4.3 Effect of acquisition process

Before accepting these results, it must be established whether the measurement interferes with device response. For instance, frequent switching of gate voltage might force drift of charges in the dielectric, thus altering phenomena such as generation and recombination (which will be illustrated in the next chapter).

To see if effects such as these do occur, two threshold voltage over time curves with sampling rate of respectively one V_{th} measurement every 3 seconds and one every 60 were compared to see if there were any substantial variations.

Results are reported in figure 4.15. As said above, the important effect is threshold voltage shift, so the curve evaluated every 60 s can be shifted to overlap with the one evaluated every 3. While the overlap is not perfect, which is to be expected, as the 60 s curve has less points and thus is more irregular, the two curves don't show substantial differences in shape, which suggests the measurement doesn't interfere with any process that causes threshold voltage shift.

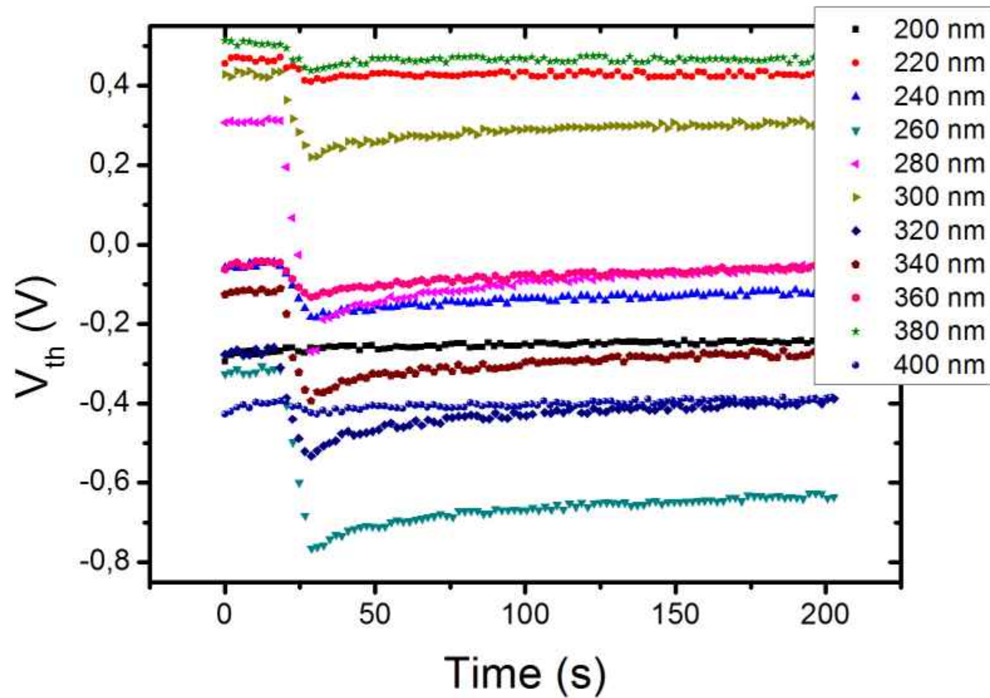


Figure 4.16: Threshold voltage curves for 10 s illumination at different wavelengths

4.4.4 Short term voltage shift rate

Figure 4.14 on page 54 shows that in the first seconds of illumination V_{th} shift grows linearly with time. In order to evaluate this time dependancy, threshold voltage versus time measurements were taken while exposing a device to illumination at wavelengths ranging between 400 and 200 nm, with a 20 nm step. The illumination time was only 10 s and the sampling rate was increased to once every 2 seconds.

Results are shown in figure 4.16. As can be seen, voltage drops are lines. The threshold shift rate can be obtained by extracting the slope from each fit.

It is reasonable (as will be shown in the next chapter) to assume that the threshold shift rate is directly proportional to incoming light intensity, (shown in figure 4.7 on page 48). Thus, a new value can be obtained, which will be called generation rate, that is independent of incoming intensity. The values obtained as a function of wavelength are shown in figure 4.17 on the facing page.

As can be seen, like the responsivity spectrum (figure 4.8 on page 49), the generation rate increases from 400 nm, peaks out and then increases again after 280 nm. A more thorough comparison will be shown in the next chapter.

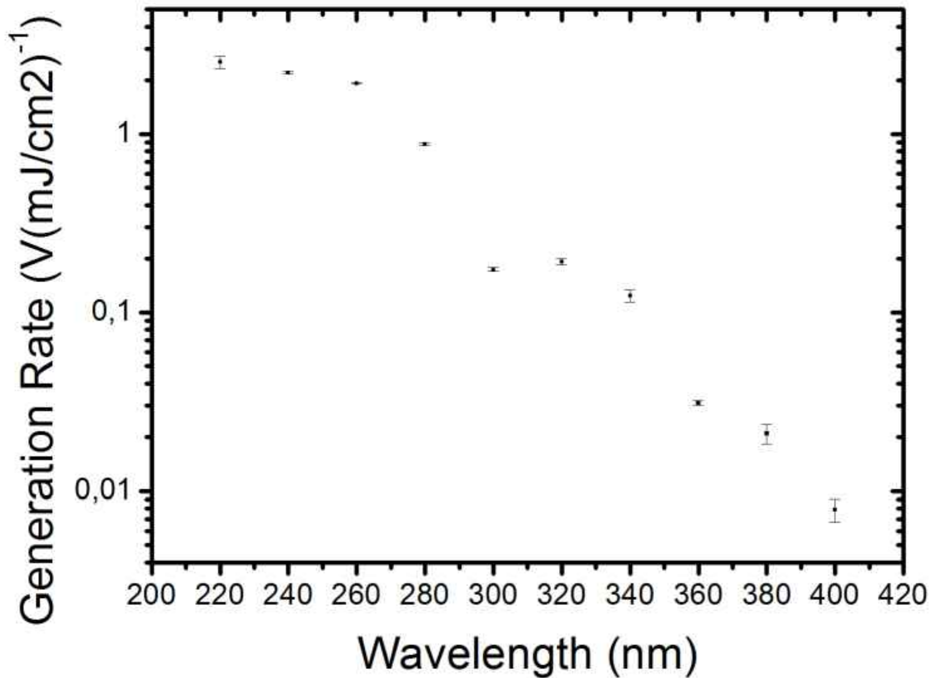


Figure 4.17: Generation rates normalized by intensity

4.5 Adiabaticity

One important behaviour of the device that must be assessed is whether or not it has a "memory" of previous light exposure. In other words, does the shape of a curve like the ones shown in figures 4.14 on page 54 at a certain time t depend exclusively on $V_{th}(t)$ or also on the device's previous illumination history? If the former is true, the threshold shift is said to be adiabatic.

To answer this question, we measured the threshold voltage in a device that was illuminated in 6 different instances for 10, 20, 30, 40, 50 and 60 s. Every illumination period was followed by a pause where the device was left in the dark for a few minutes, during which the threshold voltage shifted back, but not enough to return to the original threshold voltage. This way, it is possible to see if the present position of the threshold voltage decides the recombination process. Measurement results are shown in figure 4.18 on the next page.

The simplest way to test the adiabaticity is the following: every "tooth" in the curve starts at different threshold voltages. If the shift is adiabatic, the shape of each of these teeth should be different from the others. In order

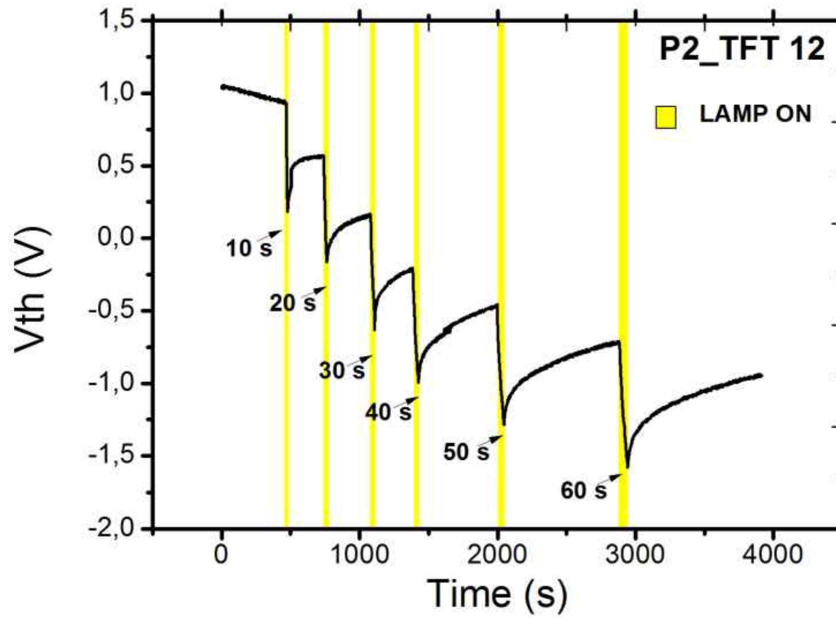


Figure 4.18: Curve for adiabaticity test: threshold voltage under consecutive illumination

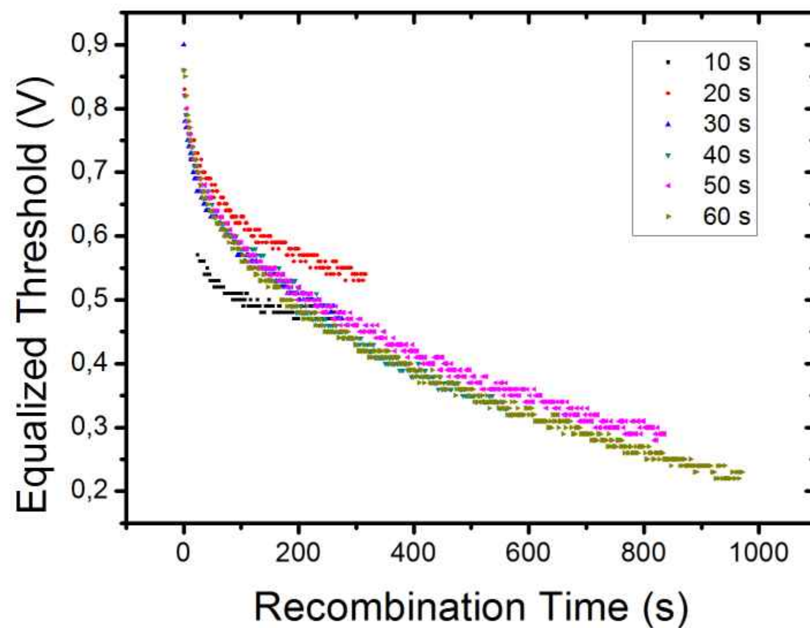


Figure 4.19: Recombination curves for the adiabaticity test, shifted for comparison

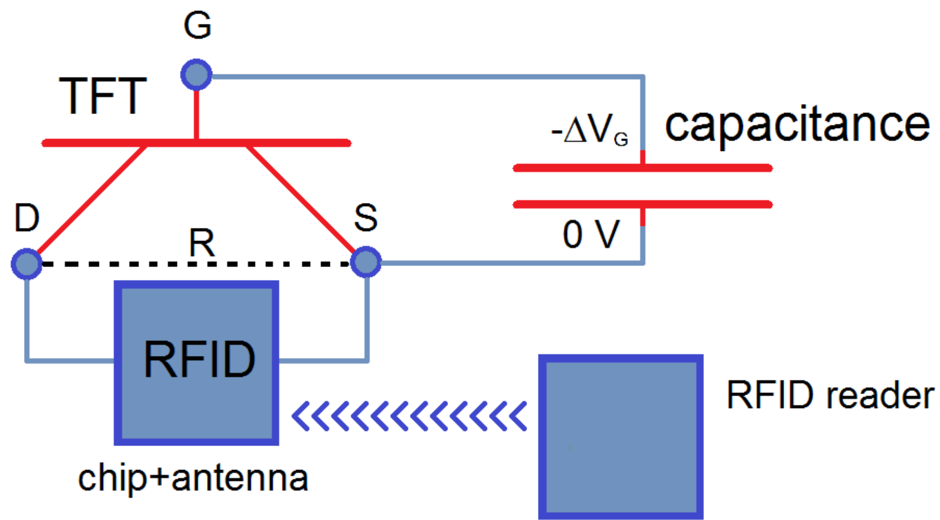


Figure 4.20: Circuit for the RFID setup

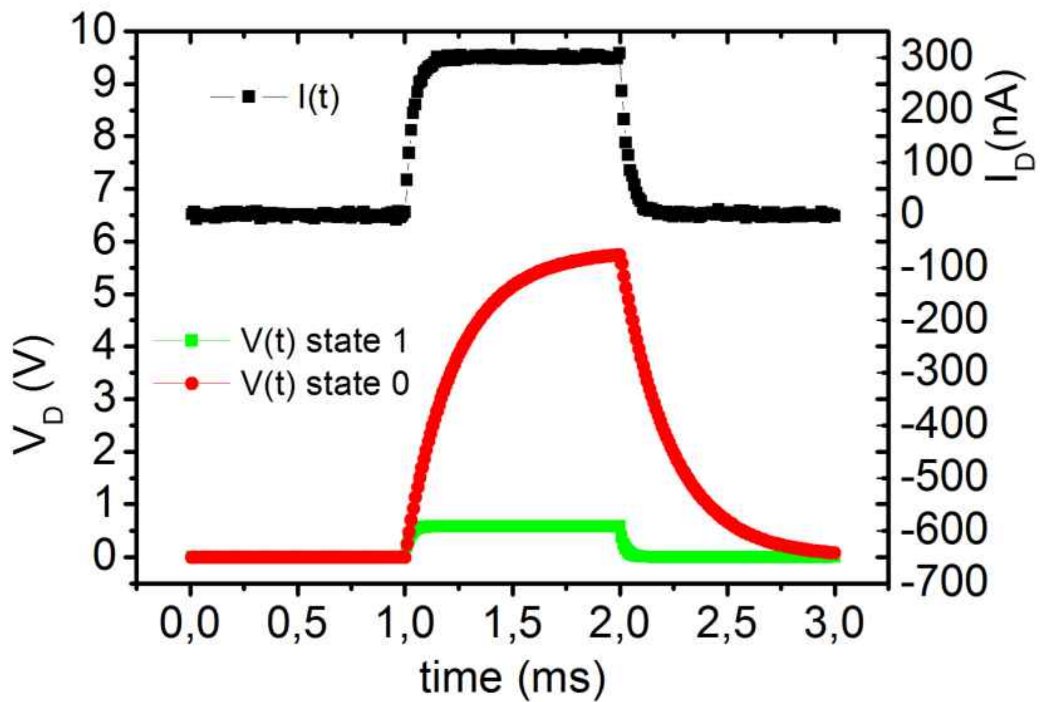
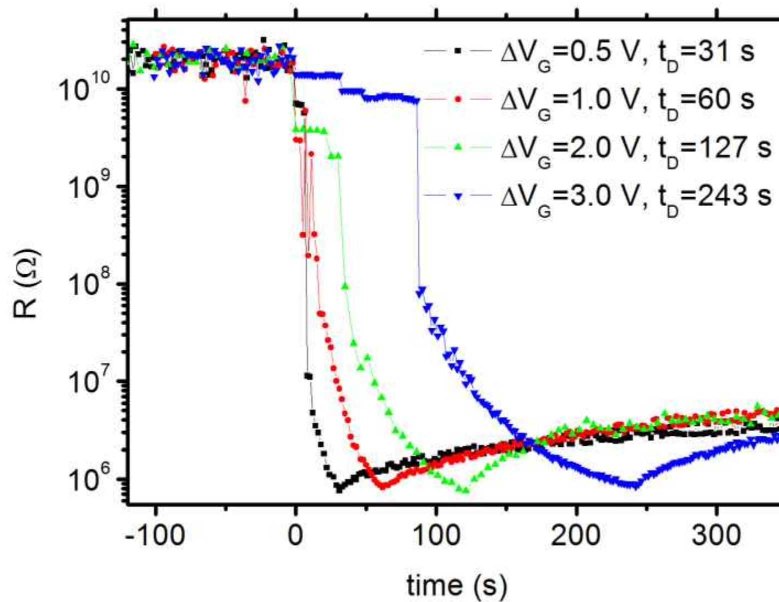
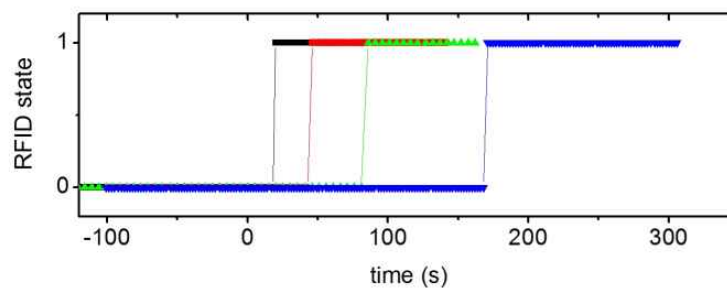


Figure 4.21: Variaton of voltage and current over time during resistance measurement processes in ”0” and ”1” states

to confront their shapes, they are all made overlap with each other. This comparison is shown in figure 4.19 on page 58, and as can be seen they overlap almost completely. The only exceptions are the ones after 10 and 20 s illumination, which can be caused by the variation scales being smaller and the curves noisier. This can lead to conclude that the shape of every partial curve remains the same no matter what the starting threshold voltage is or, in other words, that the device doesn't behave in an adiabatic way and that the way it shifts back is dependant only on light exposure.



a. Resistance over time



b. State over time

Figure 4.22: RFID circuit behaviour uder illumination at different starting gate voltages ΔV_G

Other, more "analytic" ways to check the same result are shown in the

next chapter, in section 5.4 on page 71.

What can be concluded is that, if light is interrupted, the threshold voltage will decay quickly for a short time, but part of the shift will be kept for longer period, no matter how significant it is compared to the original dark state. This suggests this kind of devices will be most suited for situation where it's necessary to monitor cumulative quantities, like for example radiation dose rate.

4.6 Practical application: RFID circuit

In this section, what has been found out so far is put to the test in a real life application. In particolar, the TFT device is used as part of a control circuit for a Radio-frequency Identification device (RFID).

RFID devices are antennae that can use the power from an electromagnetic signal to send a response signal of their own. This way RFIDs can be interrogated by a "reader" and give a reply based on their internal state [15].

In this experiment, the RFID model $SL3S$1203-1213 is used. It is controlled by a digital chip that injects 300 nA of current in 1 ms pulses and measures the potential needed to do so. As long as the resistance between the pins is higher than 20 MΩ a specific indicator on the chip will be in the logic state "0". Once the resistance goes below 2 MΩ the indicator will switch to the state "1".

Through the use of the TFT devices described in this thesis, the RFID chip and a capacitance (that in this case has a 1 μF capacity), it is possible to create a simple device capable of changing state when it's exposed to a certain amount of cumulative radiation (dose rate). In order to do so, said components are arranged like figure 4.20 on page 59: the capacitance is charged with enough voltage to keep the TFT channel closed and thus resistance R between the RFID pins is high. When UV light hits the TFT, charge generation lowers the threshold voltage. When it becomes lower than $-\Delta V_G$, the channel starts to open and R lowers until the chip goes to the state 1.

The functionality of this circuit is tested by exposing it to 300 nm UV light and measuring the resistance of the drain-source channel every 2 seconds. The resistance is extracted by measuring drain voltage and current. Every two seconds the RFID tries to inject current through the channel, and the current and voltage values look like the ones shown in figure 4.21 on page 59.

Knowing that the channel will behave as an RC circuit, the drain voltage

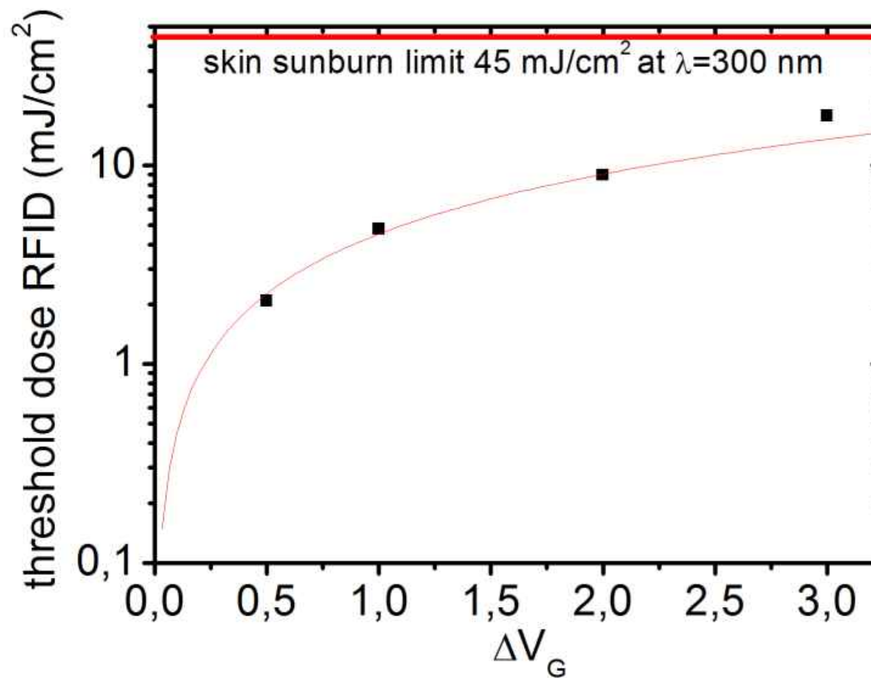


Figure 4.23: Dose rate needed to switch RFID state as a function of initial gate voltage, compared to the dose rate needed to cause sunburn at 300 nm

vs time can be fitted as

$$V(t) = I^{max} \cdot R \cdot \left(1 - e^{-\frac{t}{RC}}\right)$$

Where C is the capacity, R is the resistance and I^{max} is the current value at the maximum voltage provided by the RFID.

Results for different starting gate voltages (obtained by charging the capacitance to different values) are shown in figure 4.22a on page 60. For each of these starting gate voltages the state as a function of time is shown in figure 4.22b on page 60.

The exposure time needed to turn the RFID from 0 to 1 can be converted into total radiation dose by using the light intensity at 300 nm graphed as a function of starting gate voltage in figure 4.23. What can be seen is that the device is sensible enough that the dose needed to change threshold voltage by 2 V is one order of magnitude lower than the one needed to cause a sunburn.

5

Discussion

The goal of this chapter is to give a physical interpretation to some of the results reported in chapter 4. First, the shape of the responsivity curve will be used to identify the TFT components that play a role in light absorption. Then, an explanation is given for the behaviour of current increase after light exposure in TFT outputs. Finally, a model for generation and recombination processes will be presented and used to study the the threshold voltage shift with light exposure, with a focus on how trap states are created after illumination.

5.1 Origin of Responsivity spectrum

Going back to the results reported in section 4.3 on page 45, the first thing that can be noted in figures 4.8 and 4.9 on page 49 is that the responsivity starts increasing between 410 and 400 nm in depletion mode and between 400 and 390 in accumulation mode. Considering the GIZO band gap is around 3.0 eV (413 nm), it can be assumed that the increase in responsivity is caused by valence electrons being excited into the conduction band, thus increasing the carrier density [9]. Note that only electrons contribute to the conduction, because GIZO is an n-type semiconductor.

The presence of another peak starting at 280 nm suggests that light is absorbed by a second photoexcitation process accessible by photons of wavelength below 280 nm that corresponds to an energy above 4.4 eV. Looking at the way the device is composed, the other material that has a comparable bandgap is the Ta_2O_5 in the TSiO layers of the dielectric, which has a bandgap

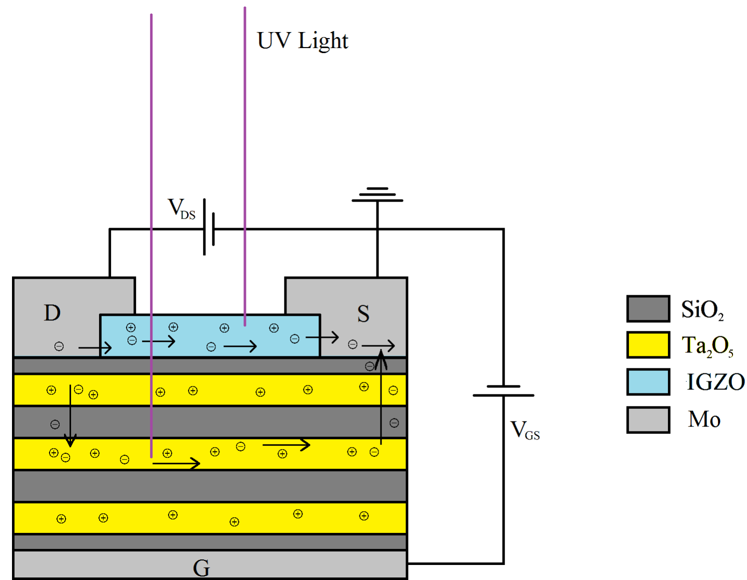


Figure 5.1: Illustration of the charge generation processes of both semiconductor channel and dielectric under UV light

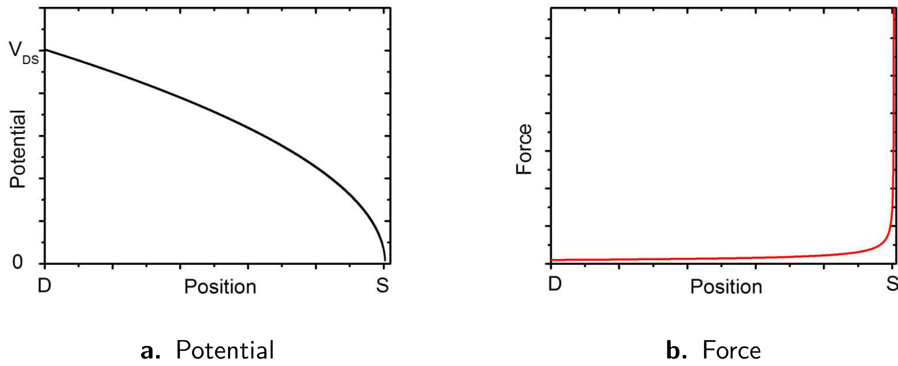
of around 4.5 eV [11].

How exactly can charge generation in the dielectric improve responsivity? Simple charge injection can be excluded, because Ta_2O_5 is mixed with SiO_2 and is separated from the IGZO channel by a layer of only SiO_2. On the other hand, SiO_2 and Ta_2O_5 are insulators, but also have higher electron mobility than hole mobility. This means that if electrons and holes are freed in the insulator, electrons will migrate towards the electrodes at a higher rate than holes. This difference would create a net electric charge in the dielectric, lowering the threshold voltage and thus increasing current in the channel. The mechanism is illustrated in figure 5.1

5.2 Effect of light on TFT output

In figure 4.11a on page 51 it was shown that for drain voltages closer to 0 current variation grew with gate voltage up until a value between 0 and 1 V, at which point it started dropping. It was also shown that this effect didn't apply when the incoming light was 250 nm.

One way to explain this behaviour is by reminding how photoconductivity works in n-type semiconductors, such as IGZO. When a photon beyond a certain energy threshold hits such materials, an electron will be excited from the valence to the conduction band, thus generating a hole-electron pair. In a



a. Potential **b.** Force

Figure 5.2: Electric potential and force distribution in a saturated channel

n-type semiconductor the electron will drift towards the drain contact, while the hole remains trapped and acts as a recombination centre for electrons. Once a photogenerated electron exits the channel, another one will be supplied by the source contact, until one of them will recombine with the hole. If the electrons are fast enough, many of them can traverse the channel before one of them recombines with the hole. This means that a single photon can virtually generate multiple charge carriers.

The number of carriers generated per photon can be thus defined as $G = \frac{\tau_s}{\tau_r}$ where τ_s is the carrier transit time and τ_r is the recombination time [7].

It can be shown that in saturation mode the potential is distributed as in figure 5.2a [8]. The electric force, which is the derivative of the potential, is distributed as in figure 5.2b: and is clearly mostly concentrated near the source, where the carriers enter the semiconductor.

Because of this, carriers are immediately accelerated to the maximum speed and transit time is minimized.

This results in the well-known fact that photoconductive gain, to which the observed current increase is linked, peaks when the device is in saturation.

The reason why this effect is not seen at 250 nm is that at that wavelength positive charge starts accumulating into the dielectric, lowering the threshold voltage and thus hindering the saturation condition.

5.3 A photoconductive model for threshold voltage shift

The decrease in threshold voltage during illumination can be linked to charge photogeneration processes. This phenomenon competes with charge recombination, that in turn tends to make the threshold voltage increase. Once light

is turned of the latter remains the only phenomenon present, which is why the rising curves in figures 4.14 on page 54 can be called recombination curves. This process must stop once the threshold voltage reaches pre-exposition levels.

Generally speaking, charge population (defined as carriers/cm^2) follows a relationship of the form [25]: $\dfrac{\partial\sigma}{\partial t} = G - R(\sigma)$, where G is the rate at which light generates hole-electron pairs and R is the carrier recombination rate. As said in previous sections, while photogenerated electrons drift towards the drain contact, holes remain trapped and act as recombination centres for electrons. This means that the more pairs are generated, the higher the chance for an electron to recombine with a trapped hole. As a result, recombination rate is expected to increase with charge density In particular, the photogeneration process causes the charge population to evolve in a form such as

$$\frac{\partial\sigma(t)}{\partial t} = G - \frac{\sigma(t)}{\tau_r(\sigma)}$$

where $\tau_r(\sigma)$ is the recombination time costant, that can be approximated by the phenomenological formula

$$\tau_r(\sigma) = \frac{\alpha}{\gamma}\left(\alpha \ln\left(\frac{\sigma_0}{\sigma(t)}\right)\right)^{\dfrac{1-\gamma}{\gamma}}$$

where σ_0 is the charge density in the dark, and α, γ are material specific parameters. This formula corresponds to a series of recombination centres distributed around a peak energy level.

Finding a solution for this differential equation can be complex, but in two cases it's highly simplified:

- *Case 1: Pure generation.* The moment illumination starts, the recombination rate is small enough to be neglected. This means that the charge density equation can be rewritten as $\frac{\partial\sigma(t)}{\partial t} = G$ and the charge density will linearly increase with time for small illumination periods.

- *Case 2: Pure recombination.* The moment illumination stops charge generation ceases to occur, thus $G = 0$. Using this condition, the equation becomes solvable. In particular, the equation is solved by a stretched exponential of the form $\sigma(t) = \sigma^{MAX} \mathrm{e}^{-\left(\frac{t}{\tau}\right)^{\beta}}$, where σ^{MAX} is the charge population values right before illumination is turned off.

How can charge photogeneration be linked with threshold voltage shift? Generally speaking, charge generation both in the dielectric and in the semiconductive channel should be considered, which would also mean that recombination mechanics should be modelled on a double distribution of trap states. On the other hand, positive charge on the dielectric results in an increase in negative carrier density in the channel, thus both phenomena could be considered as equivalent to a single negative charge accumulation phenomenon in the channel. The charge accumulation is then related to the threshold voltage shift by the dielectric capacitance:

$$\Delta V_{th}\left(t\right) = V_{th}\left(t\right) - V_{th}^{dark} = -C_i \sigma_{neg}\left(t\right)$$

where σ_{neg} is the equivalent carrier population in the channel, given by both the electrons generated in the channel and the positive charge generated in the dielectric.

This means that, instead of the charge density, negative threshold voltage shift $-\Delta$ V$_{th}$ can be used as an equivalent value.

Thus, for the linear regime we will have $\frac{\partial \Delta V_{th}}{\partial t} = G$ and for the pure recombination $\Delta V_{th}\left(t\right) = -\Delta V_{th}^{MAX} \mathrm{e}^{-\left(\frac{t}{\tau}\right)^{\beta}}$.

5.3.1 Photogeneration from threshold voltage shift rate

In section 4.4.4 on page 56 generation coefficient values were obtained by normalizing the threshold voltage shift rate by incoming intensity.

By the charge generation formula in linear regime shown above, now applied to threshold voltage, we have

$$-\frac{\partial \Delta V_{th}}{\partial t} = G$$

The G factor can be considered proportional to light intensity: if a photon has sufficient energy to generate a charge, it will do so with a certain probability, that will be the same for all the coming photons; thus the formula can be changed to

$$-\frac{\partial \Delta V_{th}}{\partial t} = gI\left(\lambda\right)$$

where $I\left(\lambda\right)$ is the incoming intensity per unit area at a certain wavelength.

Thus, to gain information about charge generation dynamics in the device, rates G must be divided by the intensity to obtain the source-independent rates g, which are the generation rates shown in section 4.4.4 on page 56.

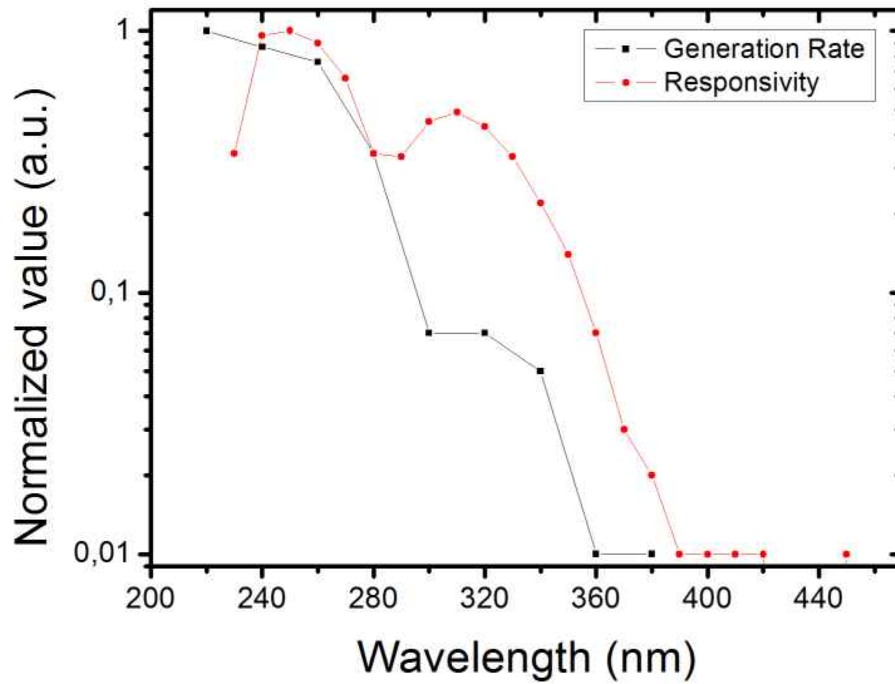


Figure 5.3: Comparison between generation rate and responsivity

These results can be compared to the responsivity values obtained in the previous chapter. To make results comparable, both generation rates and responsivities have been normalized to a range between 0 and 1 and shown in figure 5.3.

What can be seen is that generation rates simply increase with lowering wavelengths, while the responsivity curve has a peak-like shape. Other than that, the difference between the generation rates below and above 280 nm is higher than the difference between responsivities. This means that in the Ta_2O_5 the light is generating charges more efficiently than in the IGZO. This could be explained by the higher thickness of the dielectric. Differences between generation rates and responsivities above 280 nm could be considered a sign that the recombination time constants in IGZO are slower than ones in Ta_2O_5. As will be shown further, this does not seem to be the case. Another possibility, as will be shown further ahead, is that the states responsible for recombination are in an energy distribution that can vary greatly with the wavelengths that generated them.

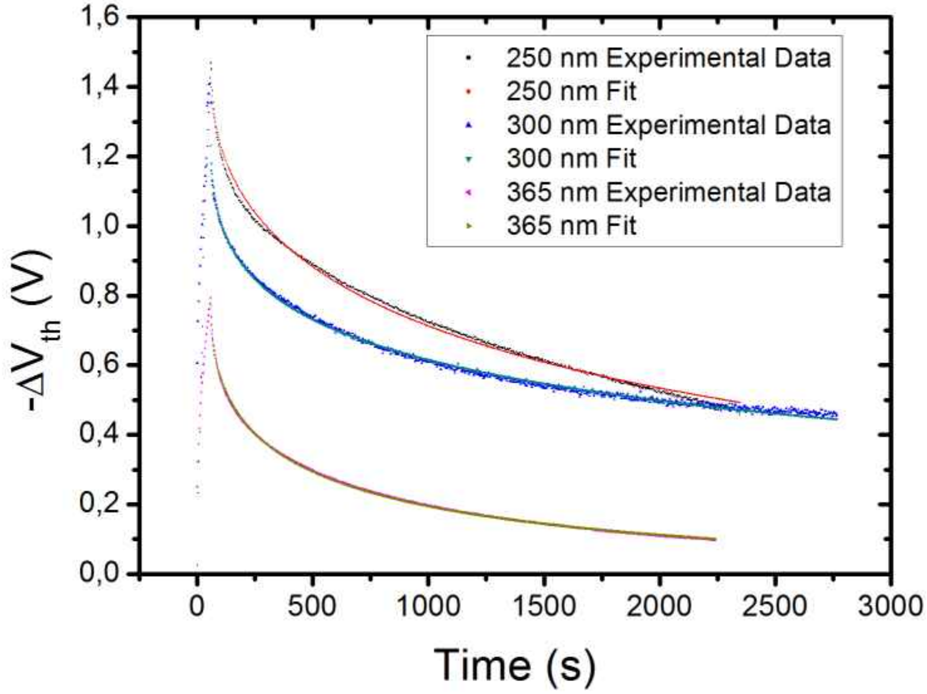


Figure 5.4: Fit of recombination curves at different wavelengths

5.3.2 Recombination process

To study recombination processes, we can again use the curves in figure 4.14 on page 54. We will proceed by extracting the $-\Delta \mathrm{V}_{th}$ versus time, and then fitting the recombination curves (the part of the curve after the light is turned off, where only recombination occurs).

As discussed above, the fitting formula will be:

$$-\Delta V_{th}\left(t\right) = -\Delta V_{th} t^{max} \mathrm{e}^{-\left(\frac{t-t^{max}}{\tau_r}\right)^{\beta}}$$

where t^{max} is the time the illumination is removed, which coincides with the maximum threshold shift.

Experimental and fitted curves are shown in figure 5.4. From these fits we can obtain the parameter $k2 = \tau_r^{-1}$ and β that best fit experimental curves. These values are shown in table 5.1 on the next page.

The two parameters together determine the shape of the trap distribution. In particular, as can be seen in figure 5.5 on the following page, τ_r determines at which time costant the distribution is centered and β is linked to the distribution width. In addition, stretched exponential functions with $0 < \beta < 1$ declines faster than a normal exponential when $t < \tau_r$ and then slower. In other

Table 5.1 – Best fit parameters for the recombination curves

Wavelength (nm)	k2 (s^{-1})	β
250	0,0005	0,4646
300	0,0006	0,3263
365	0,0022	0,4593

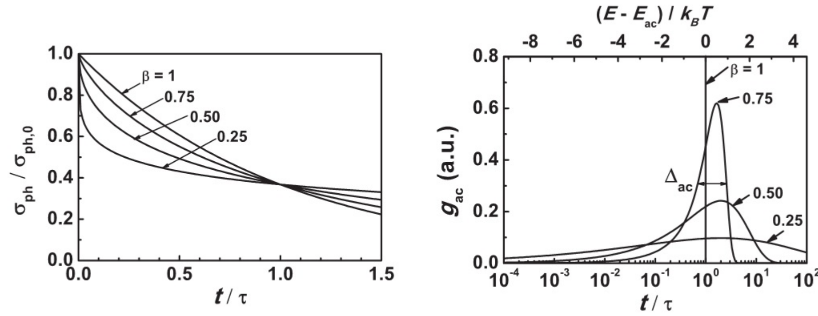


Figure 5.5: Relation between β parameter and trap distribution [25]

words, a stretched curve can account for traps with shorter time constants causing a rapid response when $t < \tau_r$ and ones with longer time constants acting on a longer timescale.

For what concerns the results obtained in this context, β values for 365 and 250 nm are very close to each other, while the 300 nm value is at 0.33. On the other hand, recombination time constants for 250 and 300 nm are on the order of 10^3 s, while the one at 365 nm is at around 500 s. The difference in recombination time constants between 365 and 250 nm can be explained by the fact light emission at 365 nm involves only the semiconductor channel. This could lead to the conclusion that traps in the semiconductor have a much shorter recombination time. This is to be expected, because in the semiconductor carrier mobility is higher and thus it's easier for carriers to reach traps and recombine.

The results at 300 nm are more difficult to understand: being below the band gap of Ta_2O_5 the recombination should behave similarly to the one from 365 nm light, but its recombination time is actually much closer to the one at 250 nm. The fact that the beta value is different might suggest that 300 nm light also excites electrons from deeper in the valence band, and holes created this way form a wider trap state distribution with overall slower acting traps.

Table 5.2 – Best fit parameters for the recombination curves in the adiabaticity test

t (s)	k2 (s^{-1})	β
10	0,0023	0,3224
20	0,0012	0,4216
30	0,0016	0,5932
40	0,0020	0,5871
50	0,0016	0,5215
60	0,0018	0,5395

As it has been said in the previous chapter, these measurements had to be taken on different devices, thus the possibility that different devices might have different parameters cannot be excluded, which might help explain the difference of β values in the 300 nm measurements.

5.4 Recombination model applied to adiabaticity curves

Another way the non-adiabaticity results shown in section 4.5 on page 57 can be verified is to graph $\frac{dV_{th}}{dt}$ as a function of V_{th}. If the shape of the curve depended only on the actual value of V_th, only a single curve should be seen in the graph (or, at least, the points should be highly clusteres). Such a graph has been plotted in figure 5.6 on the following page) .

What can be seen is that recombination curve derivative differs significantly from a single curve, thus confirming the non-adiabaticity of the process.

The non-adiabaticity of the threshold shift shows that the recombination curves after consecutive illumination all look similar to one another. For what has been said in the previous section about the relationship between recombination curves and trap states distributions, it can be argued that the latter is mostly determined by incoming light and not by the free carrier population, at least in the timeframe of a few hundreds of seconds. This also means that trap states don't actually reach an equilibrium configuration in the timescales investigated.

To see how recombination parameters change in a situation with shorter timeframes and consecutive illuminations, these curves have also been fitted with the same function used in the previous section. Results are shown in

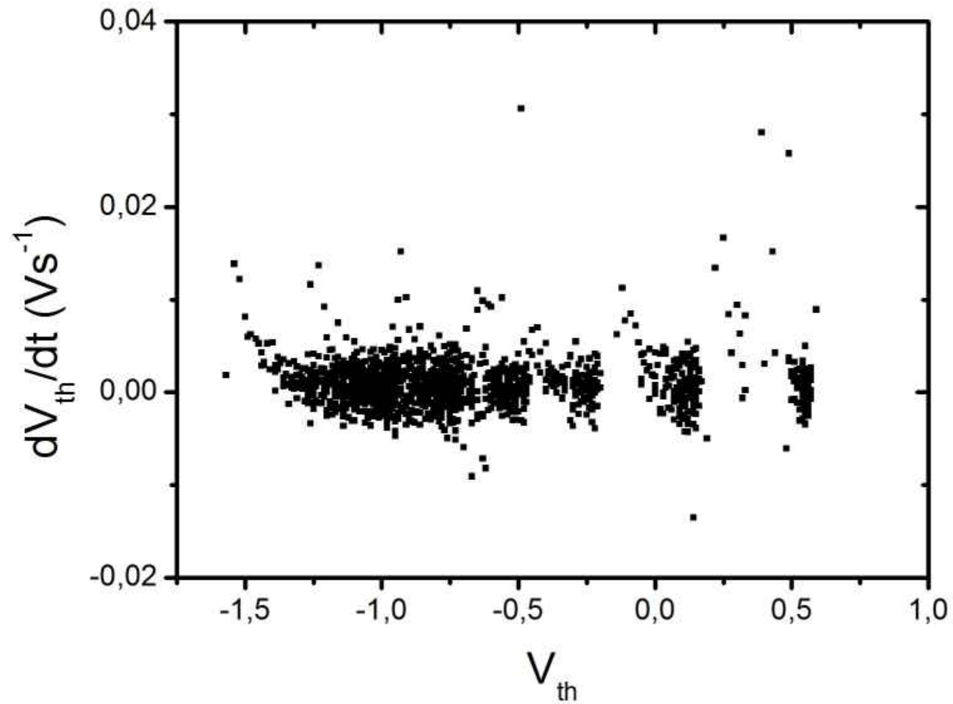


Figure 5.6: $\frac{dV_{th}}{dt}$ as a function of V_{th} of the adiabaticity curve

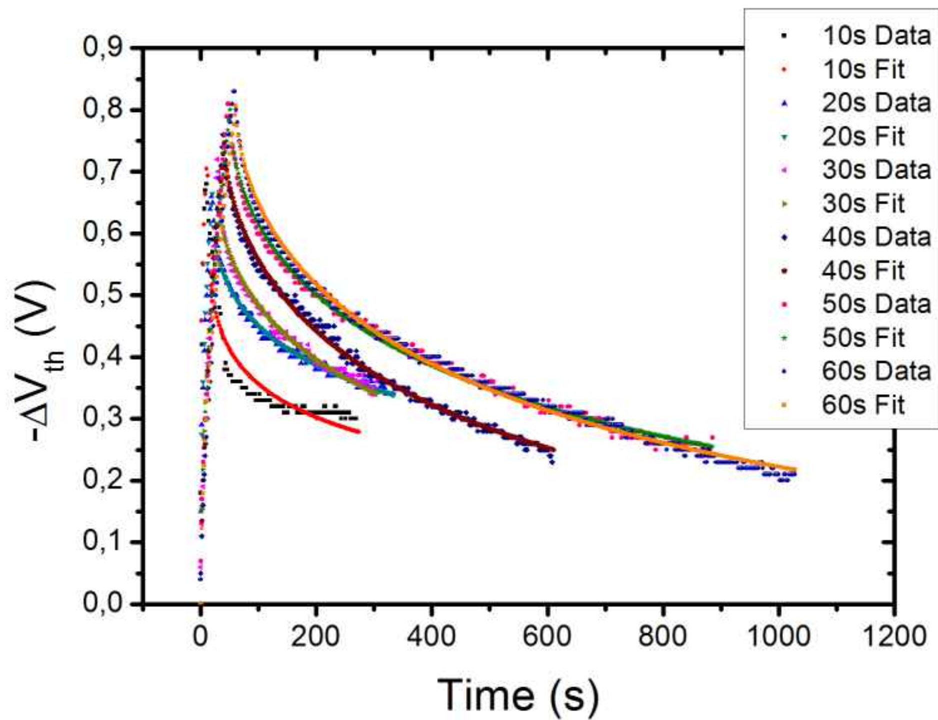


Figure 5.7: Fit for the adiabaticity recombination curves

figure 5.7 on the preceding page and in table 5.2 on page 71.

Parameters are similar among each other, which is another index of the fact that trap stated distribution remains similar at the end of every recombination. The only exception is the one at 10 s, but it might be because the fitting methods failed to follow the experimental curve because of its irregularity.

It can be easily noticed that the distribution parameters obtained in this situation differ profoundly from the ones obtained by the 300 nm in table 5.1 on page 70. In particular, in these measurements the β values are at around 0.5 (which are linked to a much more peaked distribution), and the recombination time constant is closer to the one obtained for 365 nm. This last difference is not necessarily relevant: as said before these last parameters have been extracted from shorter recombination periods, where traps with longer time constants haven't come in effect yet, and thus the distribution is shifted to lower values. This might also explain the difference in β values: for shorter recombination times, the best fit would have a higher β value because the distribution would be more peaked. For longer exposure times, the best fit would have a lower β parameter, because the distribution would get broader due to the states moving towards an equilibrium distribution (which is known as thermalization).

This suggests that the thermalization process could be monitored with the methods shown in this chapter by increasing the sampling rate and the measuring time, dividing the curve in slices and fitting each slice with different parameters.

6

Further work: improving contact flexibility by cosputtering

In order to evaluate actual device flexibility, the bending capabilities of similar devices were evaluated. Outside of the dielectric layer, which was made of parylene instead of SiO_2 / TSiO multilayer, devices investigated were the same as the ones fabricated in this work (see figure 6.1)

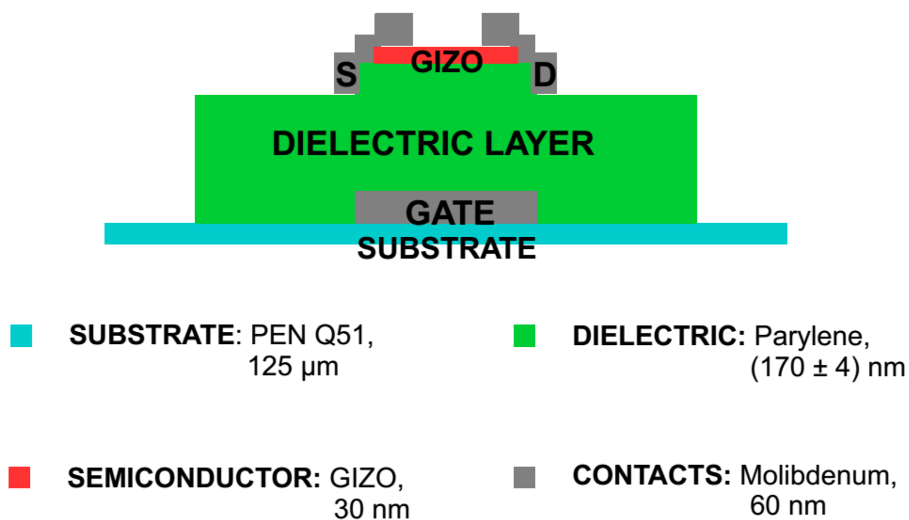


Figure 6.1: Schematics of the TFT investigated under bending capabilities

The test was performed by measuring the linear and saturation I-V char-

acteristic in the flat state and bent on different curvature radii. As can be seen in figure 6.2, the devices appear to keep their functionality up until 1.10 cm curvature radius, at which point they stop conducting entirely and result broken (they don't resume their functionality after the bending stops).

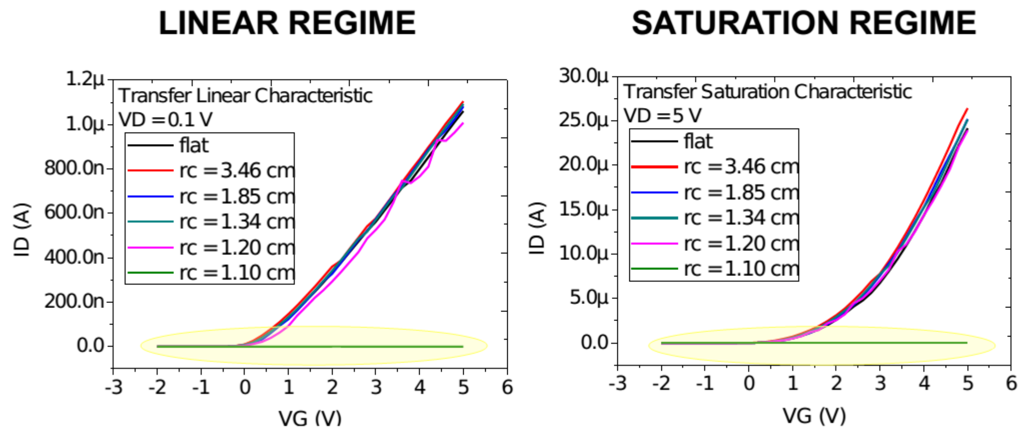


Figure 6.2: I-V characteristics for the TFT after bending at different curvature radii

With the use of Kelvin Probe Force Microscopy investigation, which allows to measure the electric potential of the device's different surfaces, it was possible to see that the breaking was entirely caused by a crack in the Molybdenium drain contacts that prevented current transmission (figure 6.3, provided by Ilaria Fratelli and Tobias Cramer).

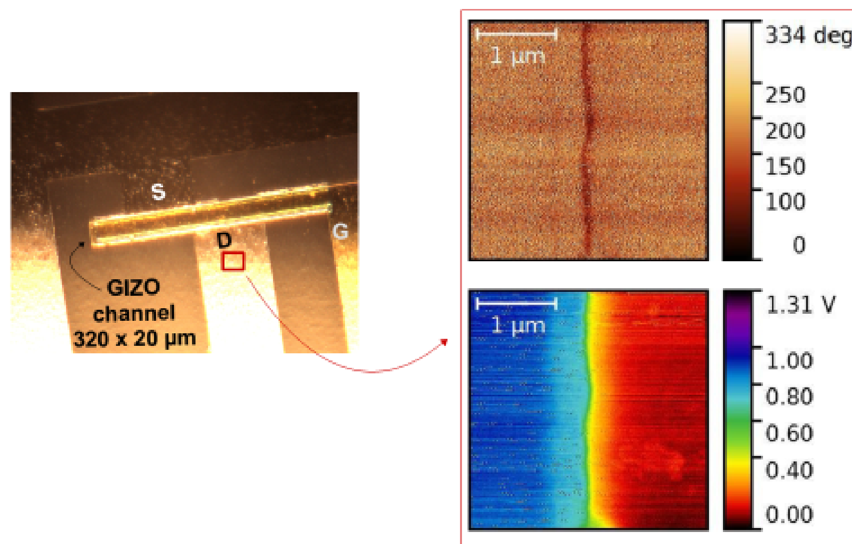


Figure 6.3: KPFM scans of the broken devices

This results indicates that molybdenium might not be the best suited

contact material in flexible electronics.

6.1 MoCr instead of Mo

Among the candidates present in literature, such as Aluminum [37] and Titanium-Gold [28], Chromium-doped Mo [39] was chosen as the most promising substitute. In general, different atomic proportions have been effectilvely used for this kind of application, for example $Mo_{0.8}$ $Cr_{0.2}$ [35]. In this work, it was decided to use $Mo_{0.85}$ $Cr_{0.15}$. To deposit the film,cosputtering was employed.

6.2 Co-sputtering deposition

Co-sputtering deposition consists in employing two different targets at the same time while performing magnetron deposition sputtering. As is shown in figure 6.4, the deposition machine used in this work could load up to four independently biased target, allowing to deposit different materials at different rates on a grounded substrate.

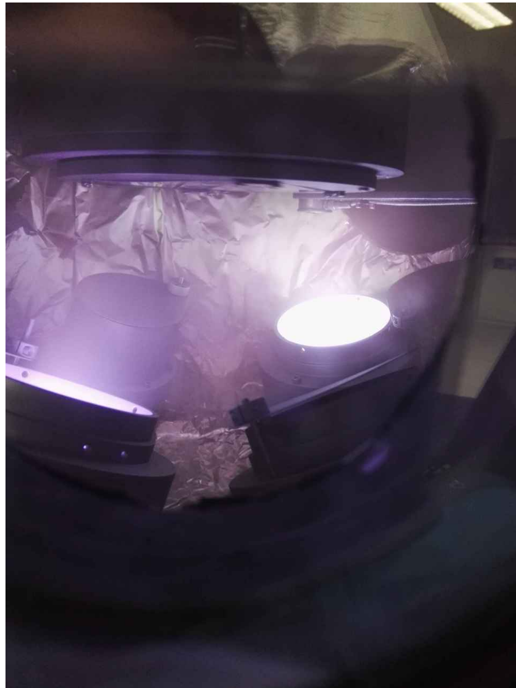


Figure 6.4: Cr (left) and Mo (right) targets during deposition. Plasma in the Mo target is excited at a higher RF power, which causes it to glow brighter

6.2.1 Relationship between deposition rate and biasing power

In order to obtain the desired proportion between Chromium and Molybdenium, it was necessary to evaluate deposition rates at different RF powers. In particular, both Mo and Cr films were deposited on a PEN substrate using RF biases at 125, 175 and 200 W. Deposition time was 20 minutes for all films. Before every deposition several spots were drawn on the substrate with a marker, so that after deposition they could be removed through liftoff, forming holes in the film. By investigating the edge of these holes with a profilometer, film thickness could be measured. Deposition rate is known to increase linearly with biasing power [14], which means three different thickness/power measurements are enough to extract the law that correlates them with a linear fit. The ticknesses obtained as a function of sputtering power is shown in figure 6.5

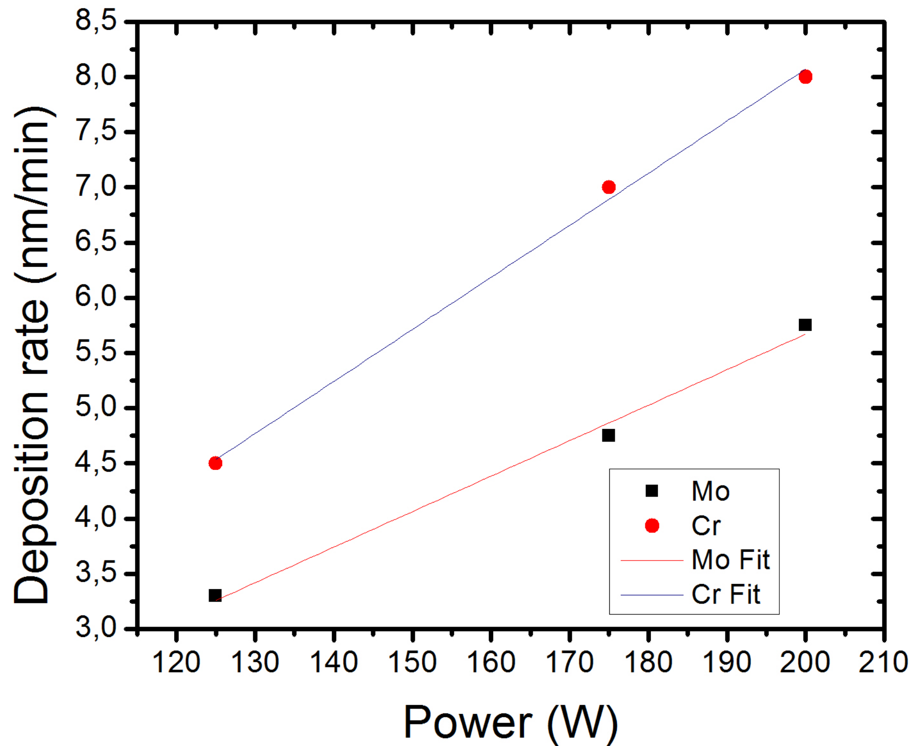


Figure 6.5: Deposition rate vs Sputtering power for Mo and Cr films

The relationships obtained between deposition rate r and power P are

$$r_{Mo} = \frac{\text{thickness}}{20'} = 0.032\,\frac{\text{nm}}{\text{min}}\frac{1}{W}P_{Mo} - 0.76\,\frac{\text{nm}}{\text{min}}$$

for Molybdenum films, and

$$r_{Cr} = 0.047\,\frac{\text{nm}}{\text{min}}\frac{1}{W}P_{Cr} - 1.36\,\frac{\text{nm}}{\text{min}}$$

for Chromium ones.

6.2.2 Calculating co-sputtering parameters

In order to obtain a film that is composed of 85% Mo atoms and 15% Cr atoms, the deposition rate must be converted from nanometers per minute (named r) to atoms per minute (named a). This can be achieved by using density ρ (10.28 g/cm^3 for Mo and 7.19 g/cm^3 for Cr) and molar mass m_{mol} (95.94 g/mol for Mo and 51.996 for Cr):

$$a = \frac{\rho}{\text{m}_{mol}}r$$

If we put P_{Mo} at 200 W, P_{Cr} can be obtained by solving the equation:

$$a_{Cr} = \frac{15}{85}a_{Mo} \Rightarrow$$

Which, including the relationship previously found by measuring thickness as a function of power, leads to

$$\frac{7.19\,\text{g/mol}}{51.996\,\text{g/mol}}\left(0.047\,\frac{\text{nm}}{\text{min}}\frac{1}{W}P_{Cr} - 1.36\,\frac{\text{nm}}{\text{min}}\right) = \frac{15}{85}\frac{10.28\,\text{g/mol}}{95.94\,\text{g/mol}}\left(0.032\,\frac{\text{nm}}{\text{min}}\frac{200\,\text{W}}{\text{W}} - 0.76\,\frac{\text{nm}}{\text{min}}\right) \quad \Rightarrow\ P_{Cr} \approx 46\,\text{W}$$

The deposition time needed to obtain a 50 nm thick layer (the same thickness used for the molybdenum contacts) can also be calculated as the sum of deposition rates from both targets at the chosen power, and is found to be approximately 8 minutes.

6.3 Bending tests

In order to test the flexibility of MoCr, a deposition was made on a PEN substrate which then was diced into stripes. One of these stripes was then bent on a bending cilinder of a 5mm radius, as shown in figure 6.6.

Figure 6.6: Scheme of the bending process

After the bending, a 1 cm x 1 cm square was cut from the stripe and its conductive features were characterized using Hall effect measurements and 4-contact method, and the compared to the ones obtained from a square that was not bended. The 4-contact method in particular allows to see changes in simmetry after bending: in particular, the increase of voltage drop in the bending direction will mean that the film was cracked because of it. The same kind of measurement was also performed on a Mo film to compare the performance. The results of the 4 contact measurements for Mo and MoCr, before and after bending are shown in table 6.1 on the facing page.

The contact positions and the bending direction are shown in figure 6.7 on page 83.

What can be seen is that after bending the MoCr film voltage drops along contacts 4-3 and 2-1 become higher than the ones along contacts 4-1 and 3-2. In particular, the simmetry factor (the ratio between 4-3 voltage and 4-1 voltage) grew from 1.14 to 11 after bending. This means that the current flowing in the bending direction is blocked by cracks perpendicular to it, as can also be seen by the microscope images shown in figure 6.8 on page 84, where the bent MoCr film shows cracks not present in the Mo one. The same effect is not seen in the molybdenum film, which would suggest that the MoCr film is more brittle than the Mo one.

Table 6.1 – 4-contact measurements for Mo and MoCr films

Mo – no annealed

Flat – current =3.4 mA				5mm bent – current =9.2 mA			
Contact	Voltage mV	Symmetry	Resist. Ω	Contact	Voltage mV	Symmetry	Resist. Ω
43	18.0	1.09	5.29	43	17.9	1.02	6.39
41	16.5	1.09	4.85	41	17.5	1.02	6.25
21	17.9	1.09	5.26	21	17.9	1.02	6.39
23	16.5	1.09	4.85	23	17.5	1.02	6.25

MoCr – no annealed

Flat – current =6.4 mA				5mm bent – current =1.9 mA			
Contact	Voltage mV	Symmetry	Resist. Ω	Contact	Voltage mV	Symmetry	Resist. Ω
43	19.1	1.14	2.98	43	18.7	11.17	9.84
41	21.8	1.14	3.41	41	1.7	11.14	.89
21	19.1	1.14	2.98	21	18.6	11.12	9.79
23	21.8	1.14	3.41	23	1.7	11.15	.88

In order to simulate the actual condition of the film in the TFT device, the measurement was repeated with two other strips after subjecting them to the same annealing process used in fabrication (180 °C for 1 hour). Results are shown in the left side of table 6.2 on the next page.

As can be seen, now both Mo and MoCr simmetry coefficients increase only slightly with bending. In accordance to this, microscope inspection shows no alteration in either film after bending (figure 6.9 on page 85).

In particular, the increase for the MoCr is even lower than the one for Mo. This means that annealing increases MoCr film flexibility. A possible explanation for this effect is that the difference in sputtering power between Mo and Cr causes atoms to reach the substrate at different energies, which means Mo atoms will penetrate the film much more than Cr ones. The cosputtered film might be inhomogeneous because of this and thus more brittle. The annealing process allows the film structure to stabilize, reducing inhomogeneity and greatly improving film flexibility.

Table 6.2 – 4-contact measurements for annealed samples (both with and without dielectric)

Mo - annealed

Flat – current =3.5 mA, Without dielectric				Flat – current =9.2 mA, With dielectric			
Contact	Voltage mV	Symmetry	Resist. Ω	Contact	Voltage mV	Symmetry	Resist. Ω
43	18.0	1.20	5.14	43	19.2	1.34	2.09
41	15.0	1.20	4.29	41	25.7	1.34	2.79
21	18.0	1.20	5.14	21	19.2	1.34	2.09
23	15.0	1.20	4.29	23	25.7	1.34	2.79
Bent 5 mm – current =3.1 mA, Without dielectric				Bent 5 mm – current =7.1 mA, With dielectric			
43	17.7	1.32	5.71	43	19.2	1.23	2.70
41	13.4	1.32	4.32	41	15.7	1.23	2.21
21	17.7	1.32	5.71	21	19.2	1.23	2.70
23	13.4	1.32	4.32	23	15.7	1.23	2.21

MoCr– annealed

Flat – current =8.5 mA, Without dielectric				Flat – current =10.9 mA, With dielectric			
Contact	Voltage mV	Symmetry	Resist. Ω	Contact	Voltage mV	Symmetry	Resist. Ω
43	19.1	1.02	2.25	43	19.1	1.10	1.75
41	19.6	1.02	2.31	41	17.4	1.10	1.60
21	19.1	1.02	2.25	21	19.1	1.10	1.75
23	19.6	1.02	2.31	23	17.4	1.10	1.60
Bent 5 mm – current =8.8 mA, Without dielectric				Bent 5 mm – current =9.2 mA, With dielectric			
43	19.2	1.05	2.18	43	19.1	1.18	2.08
41	20.0	1.05	2.27	41	16.2	1.18	1.76
21	19.1	1.05	2.17	21	19.1	1.18	2.08
23	20.0	1.05	2.27	23	16.2	1.18	1.76

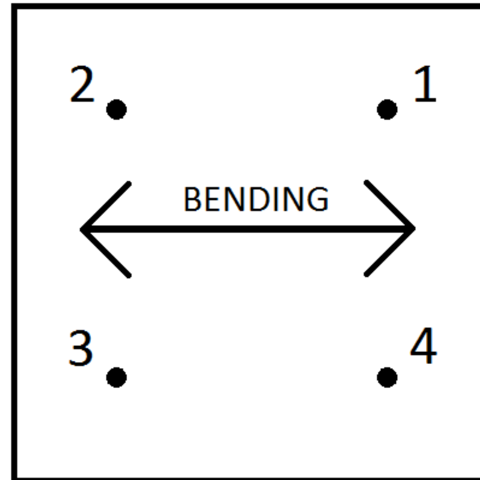
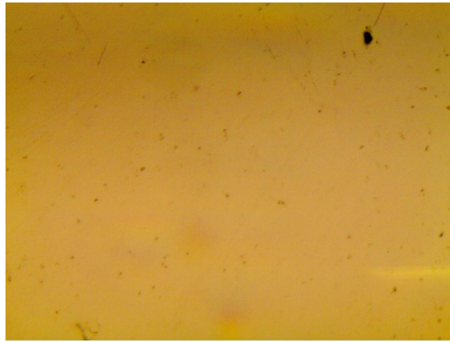


Figure 6.7: Scheme of the bending direction with respect to the contact numbers

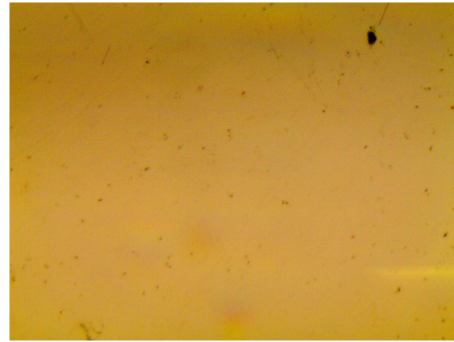
As a final test, another pair of Mo and MoCr films were deposited on top of the last three dielectric layer (from bottom to top: a SiO_2 layer deposited for 10 minutes, a TSiO layer deposited for 19 minutes and a SiO_2 one deposited for 20 minutes). The 4 contact measurements and the resistivity measurements are shown in the right side of table 6.2 on the preceding page. Microscope images are shown in figure 6.10 on page 86.

Compared to the results without dielectric, there is a slight increase in both simmetry coefficients, that can be caused by a mix of contact placement, which is manual, and some added stress from the dielectric thermal expansion.

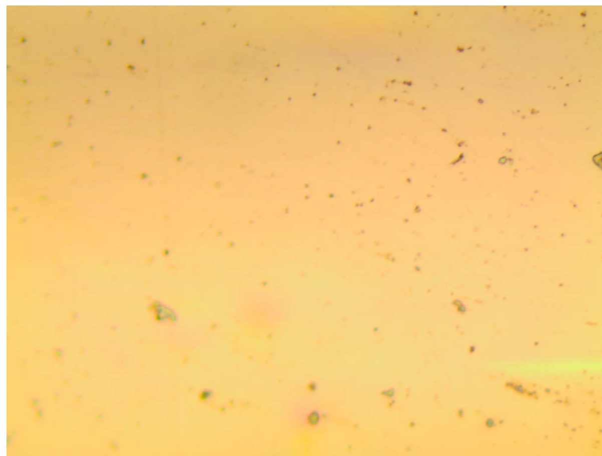
In addition, measurements of resistivity and Hall coefficient are shown in table 6.3 on page 87. They show that MoCr resistivity is half the one of Mo. In addition, when dielectric is present there is a sharp decrease in resistivity in both films. The reason is probably linked to the substrade morphology: the PEN is not planarized, while oxides are known to form smooth surfaces with deposition. This means that when the film is deposited directly onto PEN its texture will be rougher compared to when it's deposited on dielectric. With a rougher surface the electrons will need to travel along a longer path to reach a contact, which explains the increased resistivity.



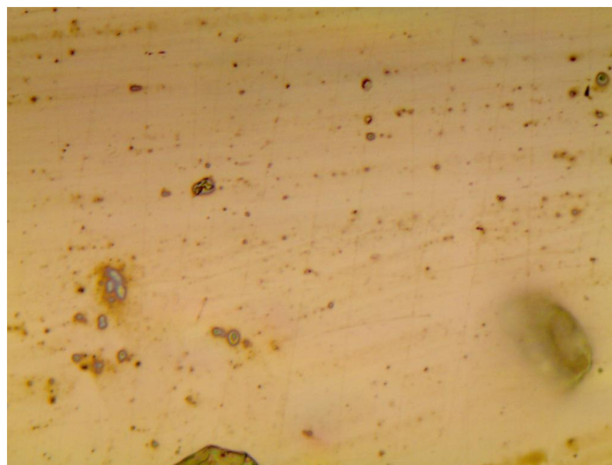
a. Mo film before bending



b. MoCr film before bending

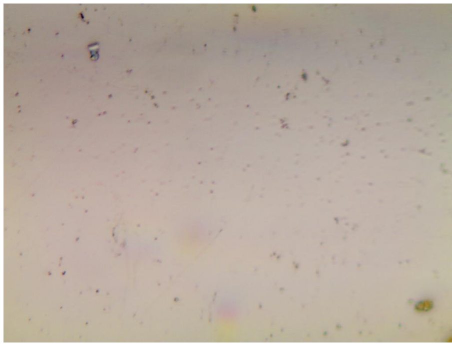


c. Mo film after bending

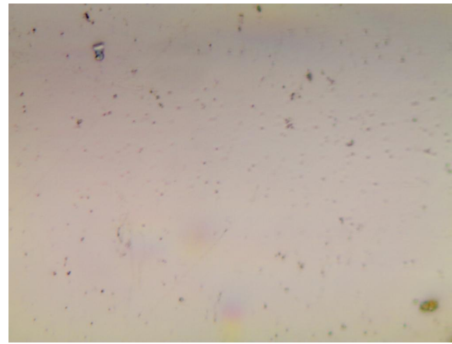


d. MoCr film after bending

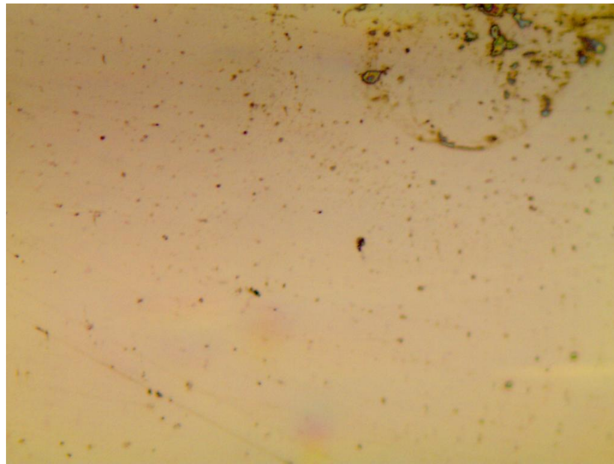
Figure 6.8: 1000x magnification optical images of flat and bent films



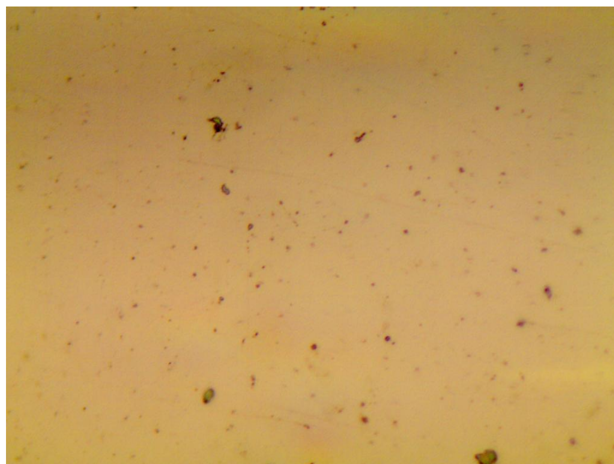
a. Mo film before bending



b. MoCr film before bending

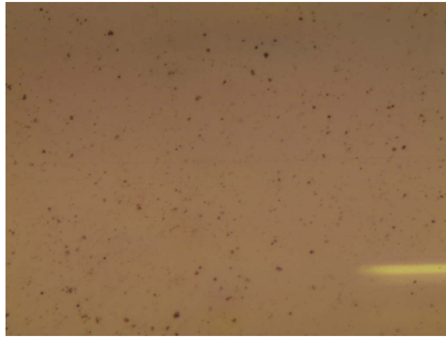


c. Mo film after bending

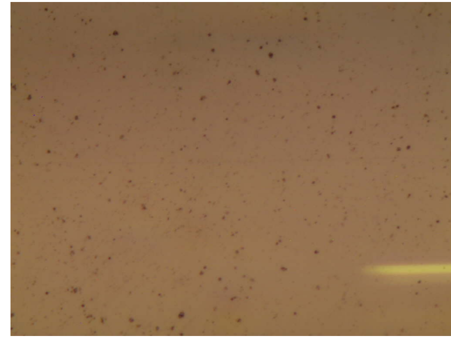


d. MoCr film after bending

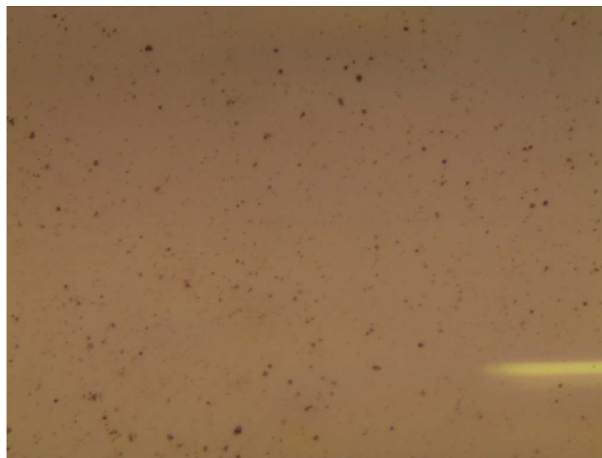
Figure 6.9: 1000x magnification optical images of flat and bent annealed films



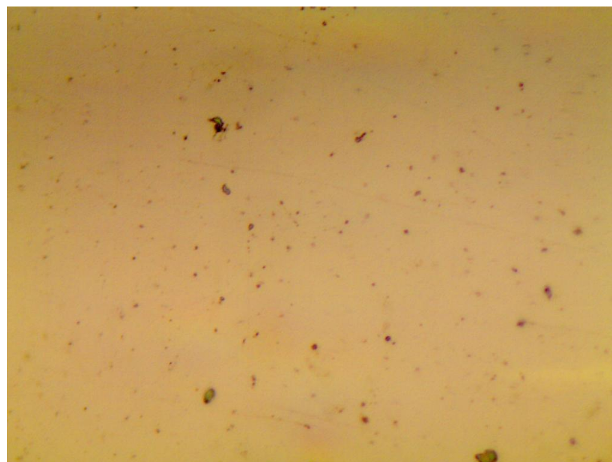
a. Mo film before bending



b. MoCr film before bending



c. Mo film after bending



d. MoCr film after bending

Figure 6.10: 1000x magnification optical images of flat and bent annealed films with dielectric

Table 6.3 – Bent Mo e MoCr

	Resistivity		Hall		Concentration	
	Sheet	Bulk	Coeff	Mobility	Sheet	Bulk
	Ω/sq	Ωcm	m^2/C	$cm^2/(Vs)$	cm^2	cm^3
Bent 5 mm – Annealed – Whitout dielectric						
Mo – Flat	21.2	1.06E-4	4.40E-4	0.207	1.42E+18	2,84E+23
Mo – Bent	22.6	1.13E-4	3.95E-4	0.175	1.58E+18	3.16E+23
MoCr – Flat	10.3	5.16E-5	9.85E-4	0.955	6.34E+17	1.27E+23
MoCr – Bent	10.0	5.02E-5	9.92E-4	0.987	6.29E+17	1.26E+23
Bent 5 mm – Annealed – With dielectric						
Mo – Flat	10.9	5.44E-5	8.10E-4	0.748	7.67E+17	1.53E+23
Mo – Bent	11.1	5.55E-5	8.10E-4	0.729	7.69E+17	1.54E+23
MoCr – Flat	7.09	3.54E-5	1.21E-3	1.710	5.15E+17	1.03E+23
MoCr – Bent	7.82	3.91E-5	9.70E-4	1.240	6.45E+17	1.29E+23

Conclusion

During the work of this thesis, the devices produced at CENIMAT and CEMOP proved to possess respectable mobility ($\mu > 10\,\mathrm{cm^2V^{-1}s^{-1}}$), clear on and off states and reliable characteristics. They have also proven to be fast reacting and stable UV sensors, that can be exposed for several minutes before saturation, with a regular and controllable response to light and with a potentially long lifetime. In addition, it was found that their response was non adiabatic, which makes the device capable of conserving traces of previous recent light stimula, making them highly suitable for employment in fields where the measurement of a total radiation dose over a long period of time is needed. By studying the responsivity curve it was possible to establish that illumination to wavelengths lower than 280 nm involves the Ta_2O_5 in the dielectric layer more than the a-IGZO channel. This feature can be an important information in the eventuality that a sensor in the far ultraviolet is needed. In particular, the obtained results suggest that in this case adding a small layer of Ta_2O_5 and changing the multilayer dielectric might improve responsivity even more by injecting extra charge in the device. Studying the effect of light on output it was also possible to confirm that the optimal working condition for the TFT is achieved when $V_{DS} = V_{GS}$, a condition which simulatenously maximizes responsivity and minimizes operation voltage.

By analyzing the generation and recombination processes it was possible to design a way to potentially observe the evolution of trap state distributions in both the dielectric and semiconductor channel. Also, although further measurements are needed, trap state distribution generated by light a wavelengths close to Ta_2O_5 gap (in this case 300 nm) seems to broaden significantly over the span of tens of minutes.

Finally, a possible way to solve the low bendability of Mo contacts by

substituting them with MoCr ones was explored. In particular, sputtering powers to obtain a MoCr film were found. Both Mo and MoCr films proved to be capable of bending at a 5 mm bending radius without cracking once deposited on a dielectric layer and annealed, but MoCr was ultimately shown to be the one with less alterations. In addition, MoCr proved to be more conductive than pure Mo.

In order to investigate this difference, new TFT devices should be produced with MoCr contacts, to see if the different materials causes any difference in the behaviour.

A

Appendix: TFT Modeling with Artificial Neural Networks

In this appendix a Multilayer Perceptron-based system for simulating the output of a TFT device is shown. As explained in the introduction, such models are essential for computer-aided design tools to simulate the behavior of integrated circuits, which in turn is important for circuit design flow [2]. After a brief introduction on neural networks, a description of two algorithms is given.

A.1 Neural networks

Artificial Neural Networks (ANNs) are computing systems inspired by interconnections that are part of the animal brains. With proper training and sufficient data, ANN can perform any kind of nonlinear modeling.

ANNs are composed of two basic units: neurons and synapses.

Neurons are functions that accept one input and emit one output value. In particular, two different types of neurons are usually employed: linear neurons, which only add a bias term to the input, and sigmoid neurons, whose output is $f(x) = \frac{e^{x+b}}{e^{x+b}+1}$ where x is the input and b is the bias.

Synapses connect neurons directionally, by turning the starting neuron output into the end neuron input. Every synapse has a weight value attached to it. In particular, the input x of a particular neuron will be the sum of every output x_j connected to it, weighted by the weight w_j of the respective synapse: $x = \sum_j x_j w_j$.

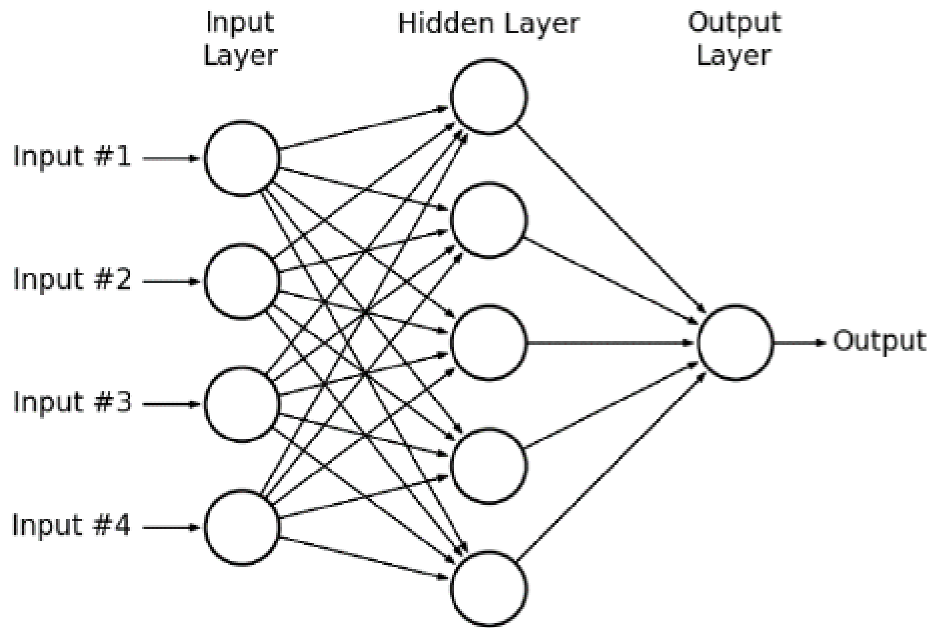


Figure A.1: Multilayer Perceptron

A.1.1 Multilayer Perceptrons

A particular ANN configuration is called Multilayer Perceptron (MLP, shown in figure A.1), which receives one or more input values and emits one or more output values. Its neurons are organized in three layers: an input layer, composed of linear neurons (where every neuron receives one output value), a hidden layer, composed by sigmoid ones and an output layer composed by linear ones (where every neuron outputs one of the MLP outputs). Every neuron of the input layer sends its output to every neuron in the hidden layer, and every neuron of the hidden layer sends its output to every neuron of the output layer.

A.1.2 Training process

By changing the weight value of every synapse, it is possible to modify ANN behaviour.

In order for the MLP to be capable of simulating any kind of function, a training dataset is required.

A training dataset consists of couples of input (training inpu) and output (target) values of the desired function.

Through an algorithm known as Backpropagation Training, weights are modified so that when the MLP is given the training inputs, it outputs

values that are as close as possible to the corresponding target values. This is performed by minimizing a cost function that represents the difference between target values and MLP output. Usually, Mean square error is employed.

MLP performance can then be checked by comparing its output with a different set of input-output pairs to that used in training.

A.2 Data acquisition and dataset preparation

This particular work focuses on modelling current-voltage characteristic. Thus, drain and gate voltage are the input values, while drain current is the output value.

To obtain a training and validation set, the I-V characteristic of one of the TFT devices was extracted. In particular, drain and gate voltage values ranged from 0 to 7 V with a step of 0.1 V.

During the training process this datased was then randomly split in half, with one half used to train the MLP and the other as validation set.

A.3 Implementation and training

Two different MLP-based architectures were tested in this work. Both were implemented and trained in python, using pybrain library.

A.4 First architecture: single MLP

In the first attempt, a single MLP with 2 input neurons 100 hidden neurons and 1 output neuron was trained for 50 epochs and evaluated. The architecture is shown in figure A.2 on the next page.

In order to quantify the distance between the validation or training target x_i^t and the MLP output x_i^o, the error function used was

$$E = \frac{1}{N}\sum_{i=1}^{N}\frac{|x_i^t - x_i^o|}{x_i^t}$$

Where N is the number of elements in the validation or training set. This value was the relative difference on average between the function we want to approximate and its MLP model.

Usually the mean square error would be used as an error function, but it also over-represents a small minority of outliers that vary greatly. It must be noted that this error function is only to gauge the overall performance

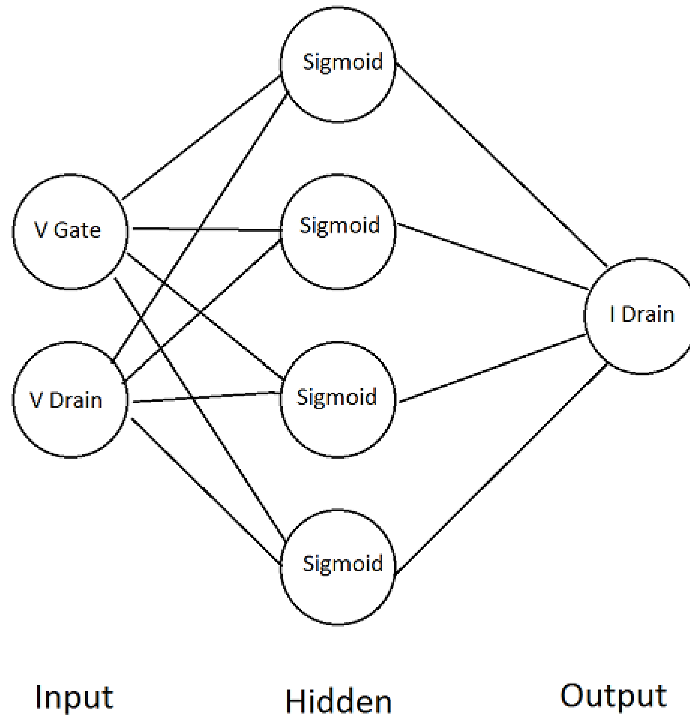


Figure A.2: Single MLP architecture

level of the system: the MSE function was still used as the cost function to minimize during the backpropagation training, as it is the most effective in that situation.

This error was evaluated on both the training set and the validation set, to see if there were noteble differences between the two values (for instance, a low training error and a high validation error would imply that the MLP fails to generalize what it learned on the training set).

A.4.1 Results

Results are shown in figures A.4a on page 97, A.5a on page 98, A.6a on page 99, A.7a on page 100, A.8a on page 101, A.9a on page 102 and A.10a on page 103. Validation and training error are both around 40-50%.

By looking at the resuts, it is clear that a single MLP approximates very well I-V characteristics with high gate voltage (see for example 7 V), but fails to approximate at lover voltages (see 0 V).

This is mostly because the system has to approximate currents that vary within roughly three orders of magnitude. Which means that the highest current values contribute much more strongly than the smallest ones. There are two possible ways of solving this problem. The first is to modify the cost

function used during training so that it's independent from the current value. On one side, this would surely improve approssimation for lower currents, but it might have compromised the entire training process. In particular, it's undeniable that lower current measurements are also more noisy, and changing the cost function might cause the MLP to try to learn random variation, thus hampering the training process.

A.5 Second architecture: Multiple MLPs

The other way is to keep the MSE cost function, but to reduce the range of current values that the MLP must learn by reducing the range of gate voltages it will work on. Of course, this would mean the model would be reliable in only a very specific situation (which would not be very useful).

In order to overcome this, a higher number of MLPs might be employed. For example, instead of having one MLP working from 0 to 7 V, one can employ 35 identical but distinct MLPs, in which the first one focuses on gate voltages from 0 to 0.2 V, the second one from 0.2 to 0.4 and so on.

Before implementing this new structure, one problem must be solved: what happens when the current value to approximate is at a gate voltage that is shared between the ranges of two MLPs e.g. 0.2 V, which is shared between the MLPs with the ranges 0-0.2 and 0.2-0.4 V? If only one of the two is chosen, there might be discontinuity when the gate voltage goes from below to above 0.2 V, as the MLPs that approximates the values change.

To solve this problem the architecture shown in figure A.3 on the next page has ben chosen: for every drain and gate voltage input all MLPs are activated. The final output will be obtained by weighting each MLP output by a gaussian-like function of the distance between its gate voltage range and the input.

The final input yf will be

$$y_f\left(V_{Drain}, V_{Gate}\right) = \frac{\sum_{j=1}^{n^\circ nets} f_j\left(v_{Gate}\right) y_j}{\sum_{j=1}^{n^\circ nets} f_j\left(V_{Gate}\right)}$$

where y_j is the j-th MLP output and

$$f_j\left(V_{Gate}\right) = \exp\left[-\frac{1}{2}\left(\frac{V_{Gate} - \bar{V_j}}{\sqrt{2}\frac{1}{4}\frac{MAX}{min}}\right)^2\right]$$

where $\bar{V_j}$ is the middle value of the voltage range for the j-th MLP, MAX

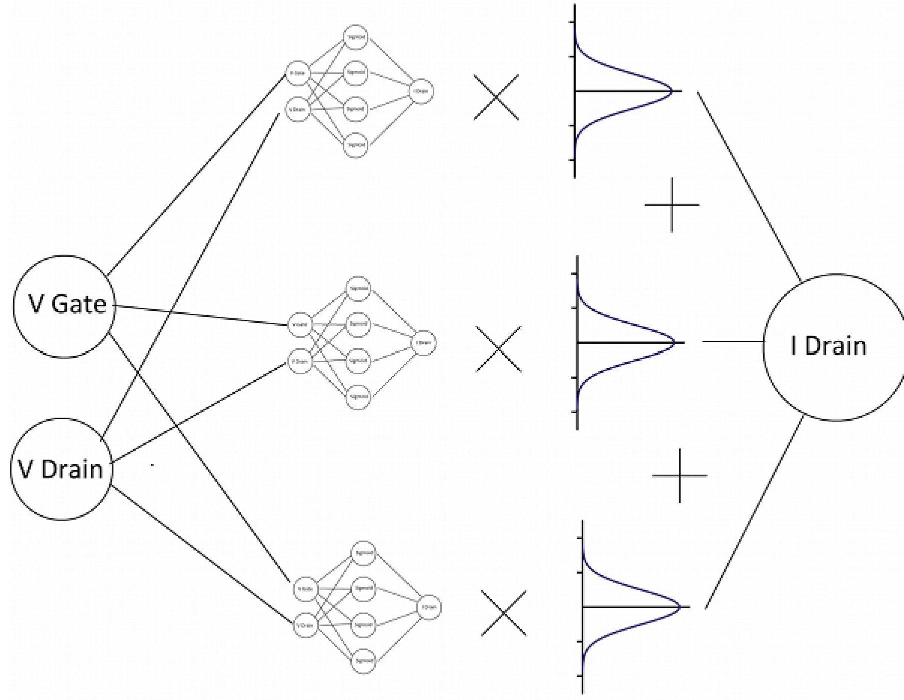


Figure A.3: Multiple MLP architecture

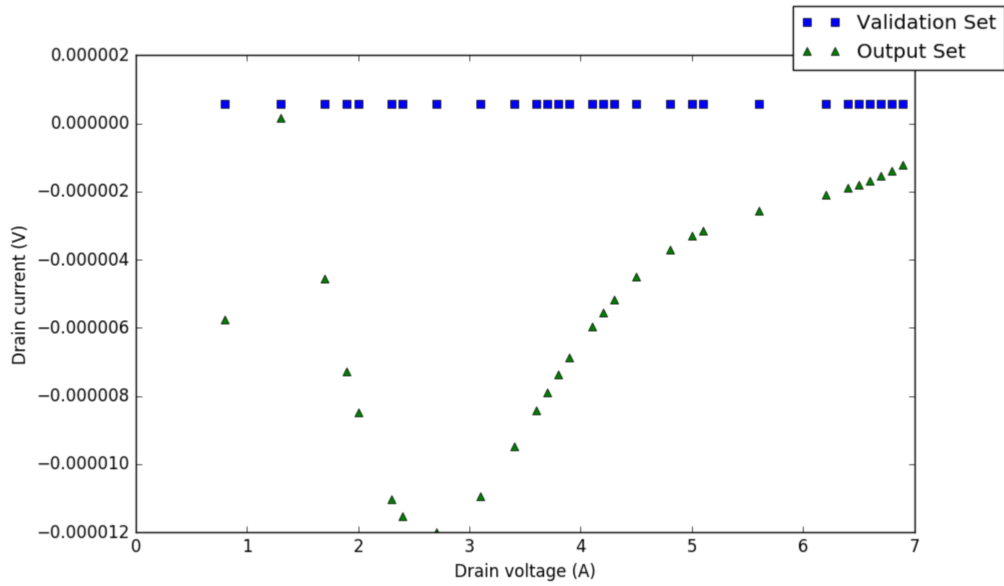
is the highest gate voltage in the dataset (in this case 7 V) and DIV is the number of MLPs.

With this solution if the input gate voltage is in the middle of a MLP's range, it will give the greatest contribution to the final output. The more the gate voltage moves towards another MLP's edge, the closer the final output will be to an average between the output of the two MLPs.

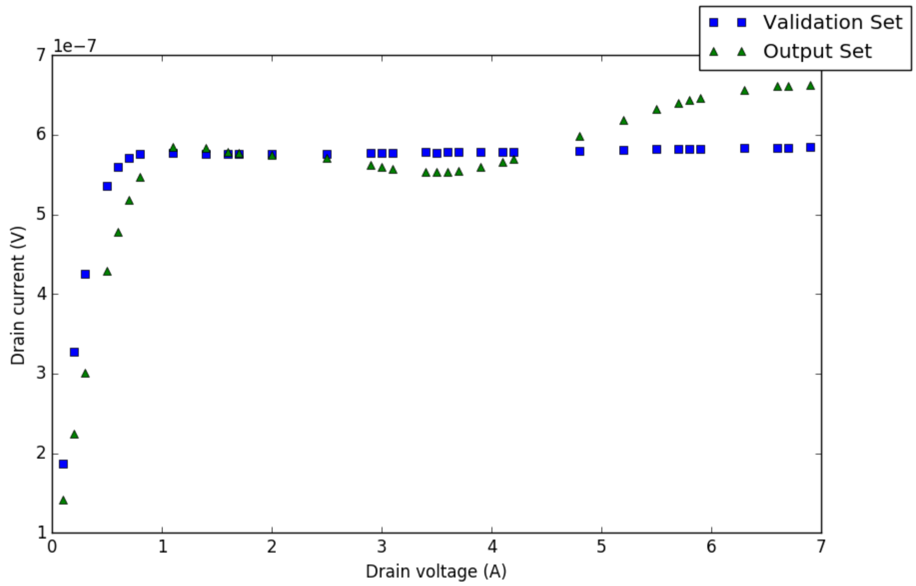
A.5.1 Results

Results are shown in figures A.4b on the facing page, A.5b on page 98, A.6b on page 99, A.7b on page 100, A.8b on page 101, A.9b on page 102 and A.10b on page 103. Training and gate errors are now around 5-6%, 10 times lower than the ones with the single MLP architecture.

By confronting the two outputs, it can be noted that the multiple MLP architecture is much more capable of following the shape of the current-voltage characteristic at low gate voltages, even though the fit is still not perfect, as can be seen in particular for the fit at 0 V.

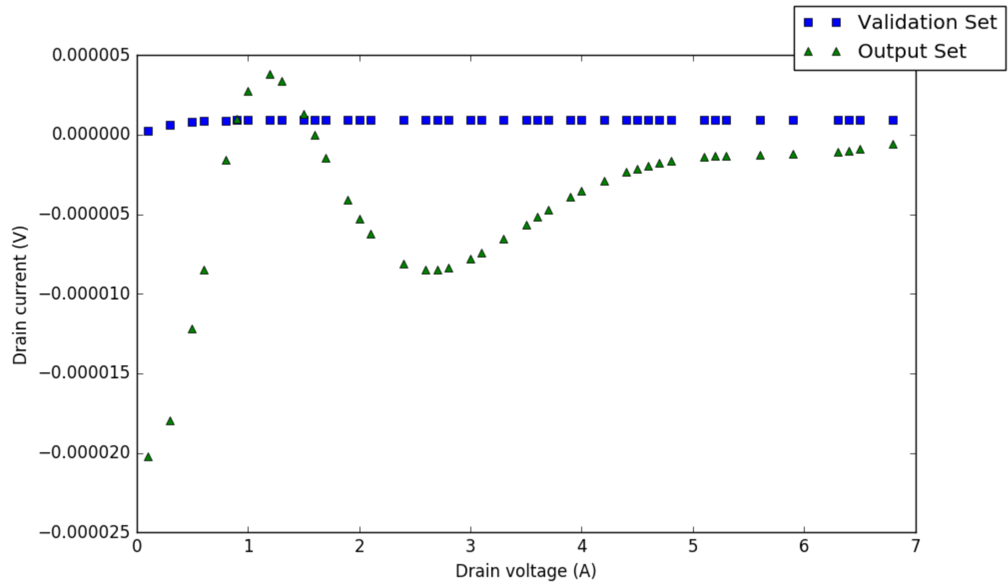


a. single MLP simulation

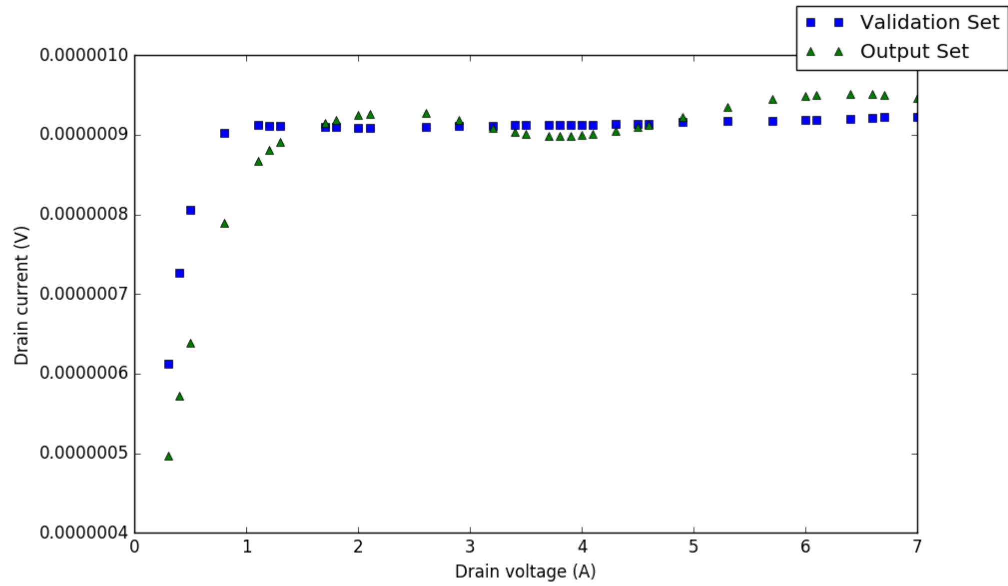


b. 35-MLP simulation

Figure A.4: Gate voltage $= 0.0V$

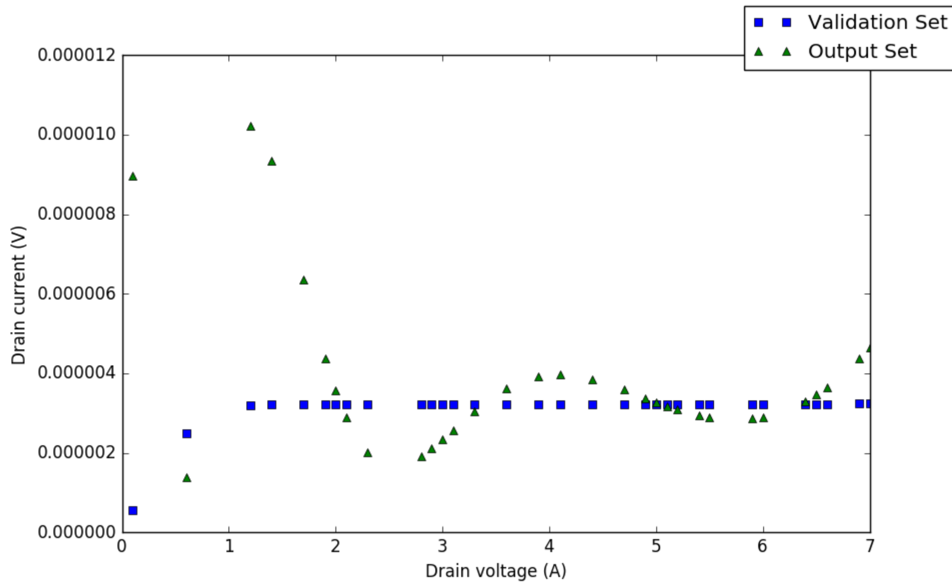


a. single MLP simulation

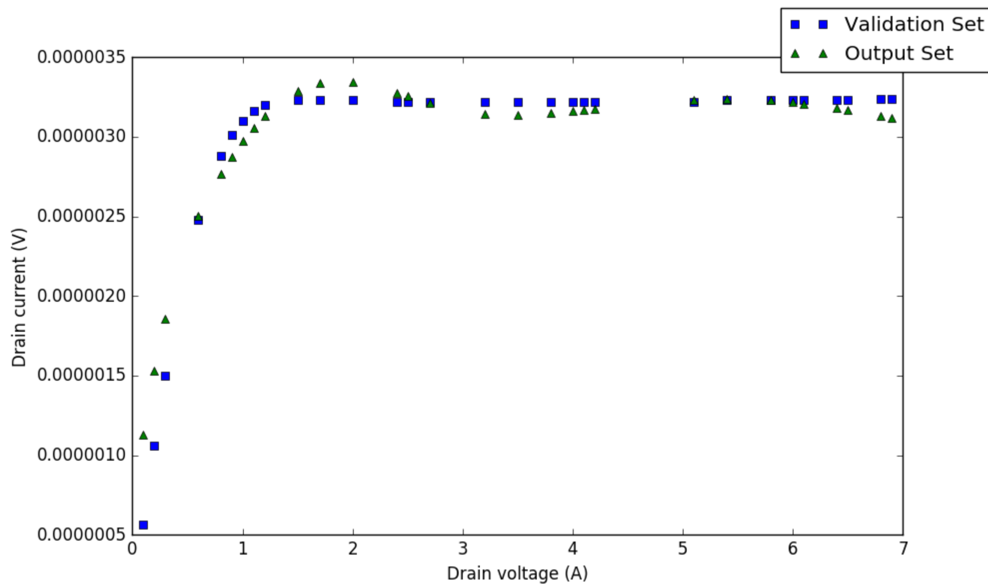


b. 35-MLP simulation

Figure A.5: Gate voltage $= 0.1V$

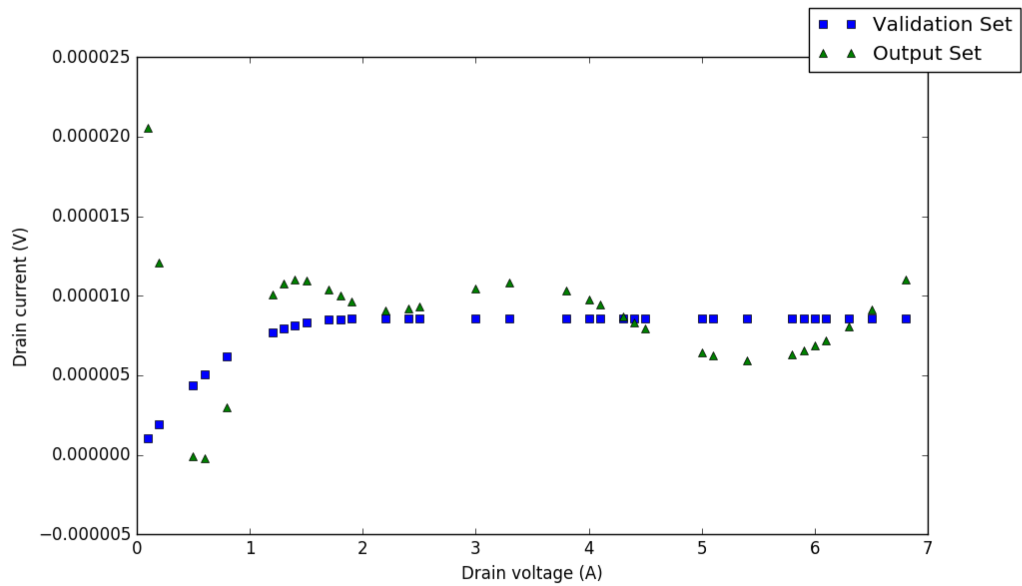


a. single MLP simulation

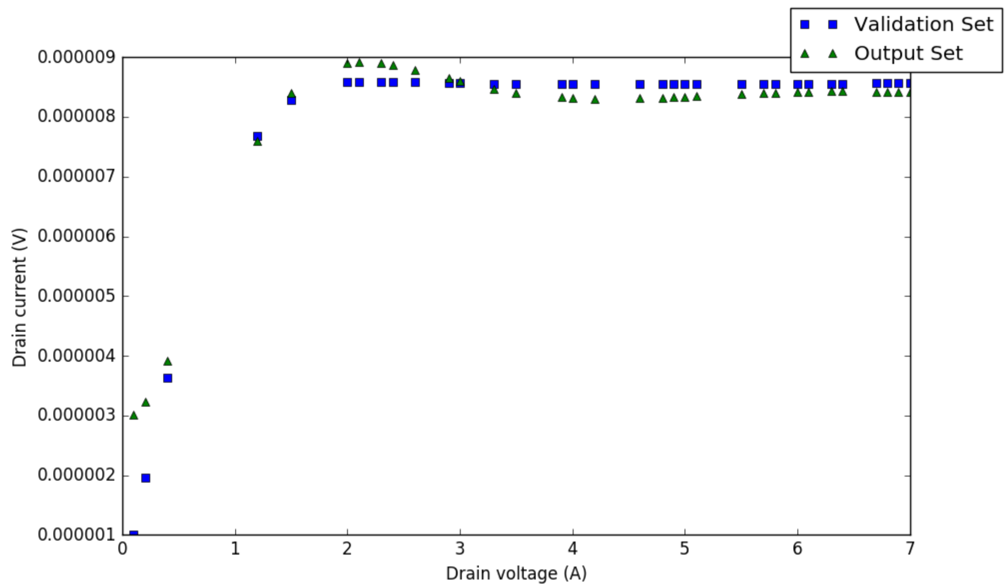


b. 35-MLP simulation

Figure A.6: Gate voltage $= 0.5V$

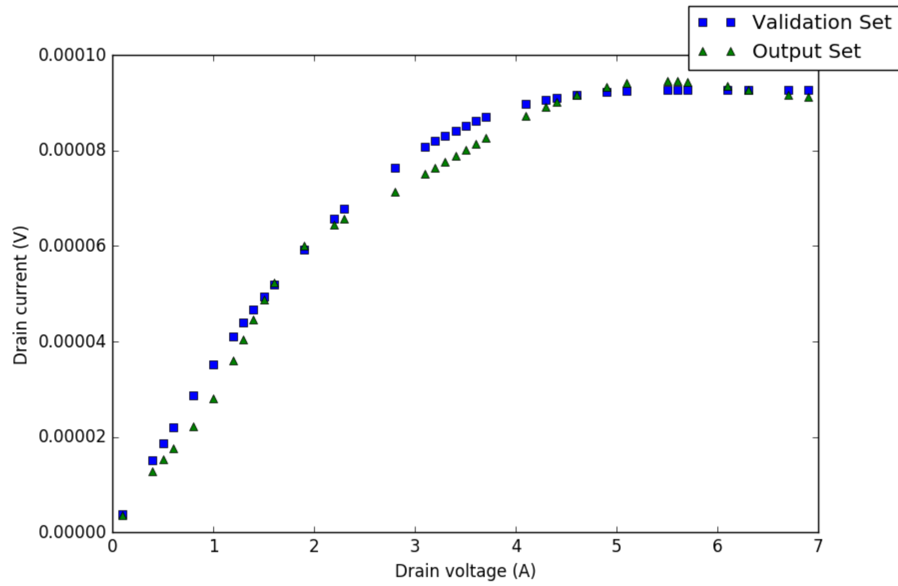


a. single MLP simulation

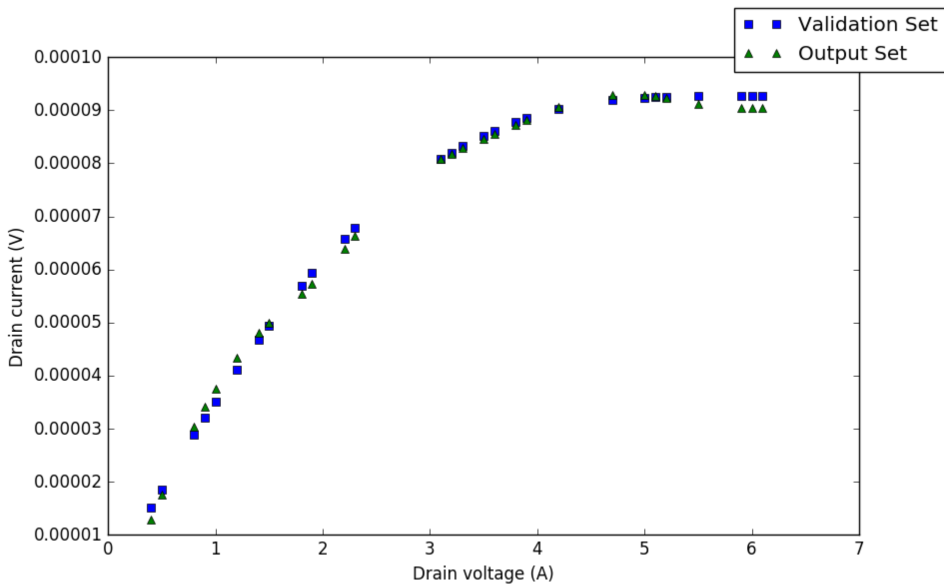


b. 35-MLP simulation

Figure A.7: Gate voltage $= 1.0V$

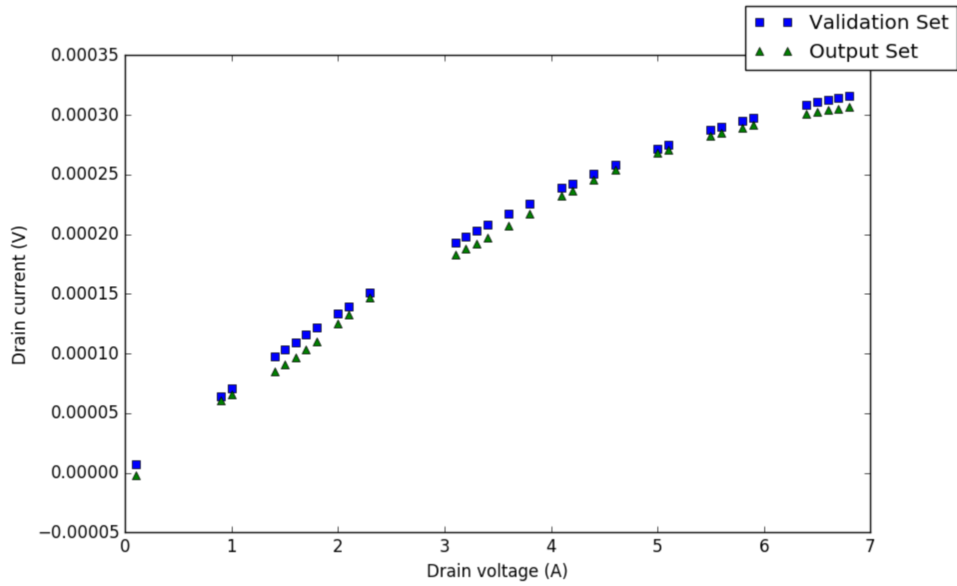


a. *single MLP simulation*

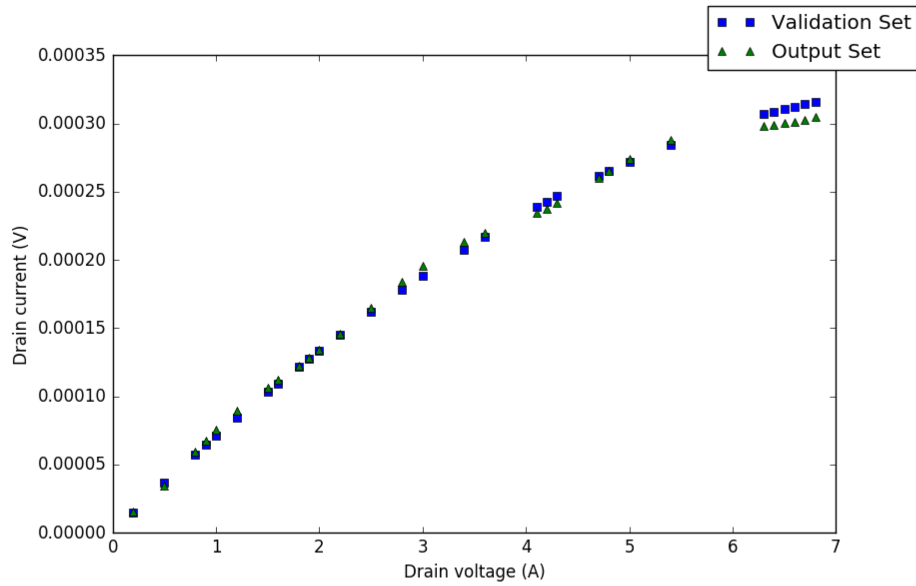


b. *35-MLP simulation*

Figure A.8: Gate voltage $= 3.5V$

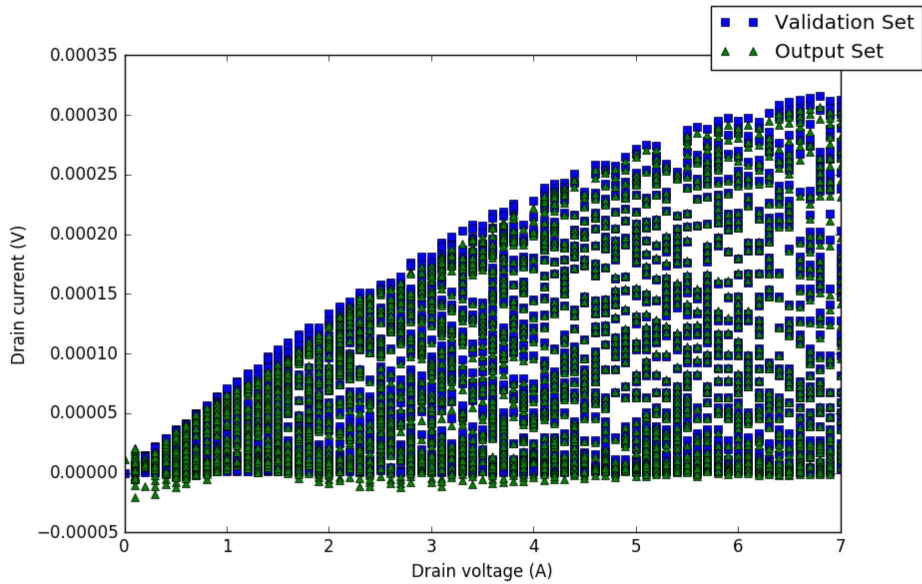


a. single MLP simulation

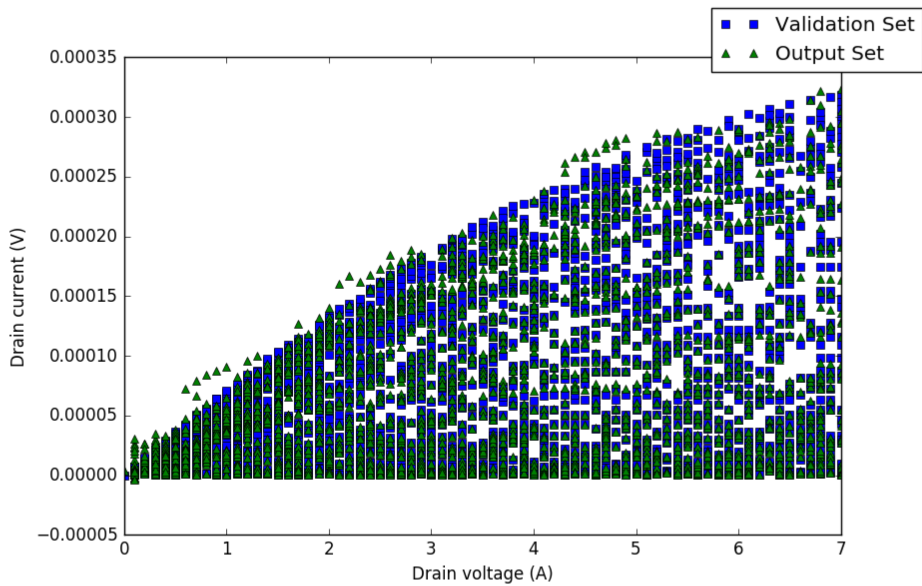


b. 35-MLP simulation

Figure A.9: Gate voltage $= 7.0V$ V



a. single MLP simulation



b. 35-MLP simulation

Figure A.10: All gate voltages

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