Postcycling Degradation in Metal-Oxide Bipolar Resistive Switching Memory

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***Abstract*— Resistive switching memory (RRAM) features many optimal properties for future memory applications that make RRAM a strong candidate for storage-class memory and embedded nonvolatile memory. This paper addresses the cycling-induced degradation of RRAM devices based on a HfO_2 switching layer. We show that the cycling degradation results in the decrease of several RRAM parameters, such as the resistance of the low-resistance state, the set voltage V_{set}, the reset voltage V_{reset}, and others. The degradation with cycling is further attributed to enhanced ion mobility due to defect generation within the active filament area in the RRAM device. A distributed-energy model is developed to simulate the degradation kinetics and support our physical interpretation. This paper provides an efficient methodology to predict device degradation after any arbitrary number of cycles and allows for wear leveling in memory array.**

***Index Terms*— Cycling-induced degradation, distributed-energy model, enhanced ion mobility, resistive switching memory (RRAM).**

I. Introduction

RESISTIVE switching memory (RRAM) attracts broad interests due to the high-speed operation [1], low-power consumption [2], [3], and nonvolatile retention [4], thus serving as a promising candidate for storage-class memory [5] and embedded nonvolatile memory [6]. To explore the applications of RRAM, switching variability [7], [9], [10], resistance fluctuation [11]–[13], and cycling endurance failure [14]–[16] need to be addressed and understood. It was shown that the endurance failure of bipolar RRAM is usually dictated by negative set, or breakdown during the reset process [16]. The cycling endurance was shown to be controlled by the largest voltage V_{stop} applied during the negative reset pulse. However, the RRAM device degradation during cycling before the endurance failure is far less understood.

This paper studies the cycling-induced degradation of HfO_2 RRAM device arranged in a one-transistor/one-resistor (1T1R) structure. We show that the cycling degradation leads to a decrease of several RRAM parameters, such as the resistance of the low-resistance state (LRS), the set voltage V_{set}, the reset voltage V_{reset}, and the corner voltage V_{corner}, defined as the voltage for which the switching speed becomes comparable with the inherent RC delay time in the 1T1R structure. The decrease of V_{corner} with the number of cycles N_C provides evidence for an enhancement of ion migration mobility with degradation. The increased ion mobility can be attributed to the decrease of energy barrier E_{A0} for defect migration in the switching region. We show that V_{stop} controls the cycling degradation rate as well as the endurance failure in our devices. The degradation effects are quantitatively explained by an Arrhenius-driven distributed-energy model, and our results suggest that V_{reset} and LRS resistance can serve as degradation monitor and endurance failure predictor for wear out leveling within the memory circuit.

A preliminary report of cycling degradation in HfO_2 RRAM was previously presented [17]. In this paper, we extend the previous report by elucidating the physical model for degradation based on the thermally activated defect generation mechanisms with distributed energy. We also evidence and support the capability to monitor degradation by tracking the reset voltage V_{reset} or the LRS resistance R. This methodology may enable stress-aware methods to predict and anticipate device failure in the memory array.

II. Experimental Samples and Setup

We characterized the RRAM devices consisting of a TiN bottom electrode, a Ti top electrode (TE) serving as an oxygen exchange layer, and an amorphous Si-doped HfO_2 switching layer [16]. The device size was 40 nm, and the HfO_2 thickness was 10 nm [16]. More details about the device stack in our samples can be found in [18]. As schematically shown in Fig. 1(a), the 1T1R structure was used for on-chip control of the switching processes. The transistor size in our test

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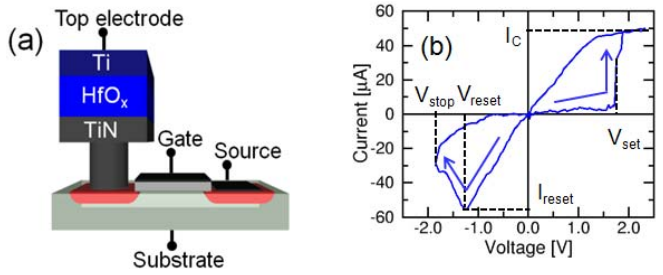

Fig. 1. Schematic of (a) 1T1R structure of our samples and (b) measured I–V curve during one cycle indicating LRS, HRS, and the definition of parameters V_{set}, V_{reset}, I_{reset}, and V_{stop}. The pulsewidth was $t_P = 1$ μs and the compliance current was $I_C = 50$ μA.

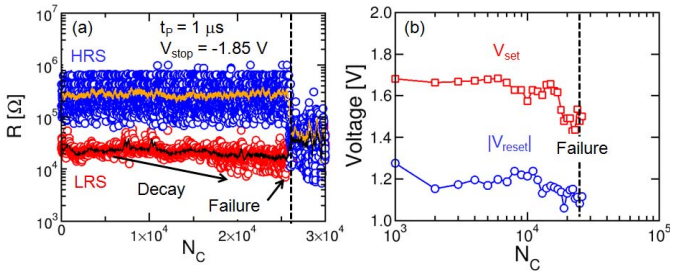

Fig. 2. (a) Measured R for HRS and LRS and (b) median switching voltages V_{set} and $|V_{\text{reset}}|$ as a function of N_C. Endurance failure takes place at $N_C \approx 2.5 \times 10^4$ due to the collapse of R window induced by negative set. LRS resistance, V_{set}, and $|V_{\text{reset}}|$ all decrease with N_C due to the cycling-induced degradation before failure.

structures was $W/L = 3/1.45$ μm, while the gate dielectric thickness was 15 nm. During the set transition, the current flowing in the RRAM element was limited to a maximum compliance current $I_C = 50$ μA by proper tuning of the transistor gate voltage, thus allowing to control the size of the conductive filament (CF) [19]. The gate voltage was adjusted to a larger value during the reset pulse to minimize the transistor resistance for minimum voltage drop. The large gate voltage during reset also helped keeping the forward bias at the transistor substrate-drain junction low enough to prevent excessive diode current.

To conduct the cycling experiment, an arbitrary waveform generator was used to apply voltage pulses to the TE of the device and to the transistor gate, while the voltage (V) and current (I) during set and reset cycles were monitored in real time by a digital oscilloscope [16]. The transistor source was connected to ground during all experiments. The bipolar voltage pulses applied to the TE during one cycle include a positive triangular pulse of voltage ($V_{\text{TE}} = 2.4$ V) for set transition, and a negative triangular pulse of voltage V_{stop} for reset transition, resulting in a typical I–V curve as shown in Fig. 1(b). In addition, positive and negative pulse with voltage ($V_{\text{TE}} = 0.5$ and -0.5 V) were applied for reading the LRS and high-resistance state (HRS) after set and reset transition, respectively. The read voltage polarity was chosen to minimize possible disturbs to the programmed state. As the read voltage was much smaller than set/reset voltages, we expect no impact of the read condition (read voltage amplitude and polarity) on cycling and degradation. The pulsewidth t_P was fixed to 1 μs for all applied pulses. The abrupt increase of current takes place at positive set voltage V_{set}, indicating the formation of a CF in correspondence of the set transition from HRS to LRS. On the other hand, the filament was dissolved under negative voltage, as evidenced by a more gradual reset transition from LRS to HRS starting from the reset voltage V_{reset}. The current in correspondence of the reset transition is referred to as the reset current I_{reset}.

III. Dependence on the Number of Cycles

We studied the degradation dependence on cycle number by the cycling experiments, where we monitored all I–V curves in real time. Fig. 2(a) shows the measured resistance R for LRS and HRS as a function of the number of cycles N_C

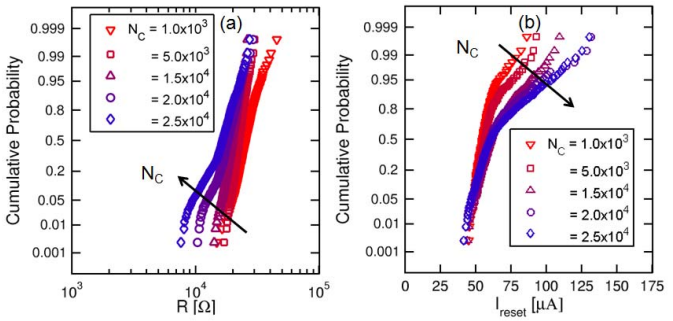

Fig. 3. Cumulative distributions of (a) measured R for LRS resistance and (b) corresponding I_{reset} at increasing N_C. Note the distribution tails at low R and high I_{reset}, which increase with cycling due to the device degradation.

for a typical cycling experiment at $V_{\text{stop}} = -1.85$ V. Data in Fig. 2(a) refer to a single device at increasing cycles, although other samples showed the same qualitative behavior. The resistance window is about $10\times$ between LRS and HRS until failure takes place at $N_C \approx 2.5 \times 10^4$. Failure appears as a sudden collapse of the LRS and HRS resistances to an intermediate state. In our previous work, we evidenced that failure is due to negative set, namely, a breakdown process taking place during the reset operation under negative voltage, where the resistance increases abruptly after reset [16]. Although other failure processes have been reported in the literature, such as stuck set and stuck reset states [14], [20], we always detected negative set as the failure event in our devices [16]. Even before failure, however, LRS resistance clearly decreases during the whole lifetime of the RRAM device, as evidenced by the median lines of R in Fig. 2(a). On the other hand, HRS resistance remains approximately constant before failure. Fig. 2(b) shows the median V_{set} and $|V_{\text{reset}}|$ as a function of N_C: V_{set} decreases from 1.65 to 1.45 V, while $|V_{\text{reset}}|$ decreases from 1.25 to 1.05 V.

To better understand the device degradation phenomena, we plot the cumulative distributions of LRS resistance at increasing N_C in Fig. 3(a). To guarantee a suitable statistical significance, each distribution contains the value measured within 10^3 switching cycles. For instance, for $N_C = 10^3$, we collected data from $N_C = 500$ to $N_C = 1500$. Similarly, for $N_C = 10^4$, we collected data from $N_C = 9500$ to $N_C = 10\,500$. Results show that the median value of R decreases with N_C,

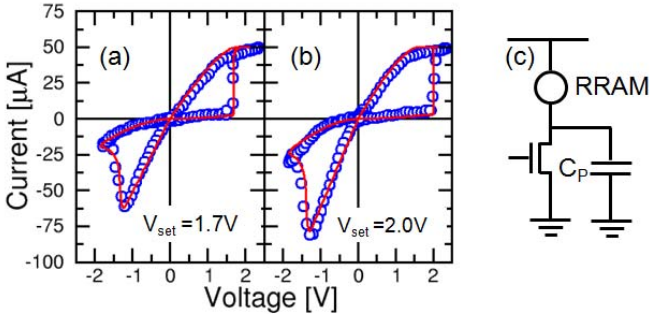

Fig. 4. Measured and calculated I–V curves corresponding to cycles in (a) main part of the distribution and in (b) distribution tail of Fig. 3 and layout of the 1T1R structure evidencing the parasitic capacitance C_P (c). Calculations (solid lines) agree well with the measured I–V curve (symbols). Cycles in the tail correspond to set at high V_{set} inducing current overshoot and a resulting low R and high I_{reset}.

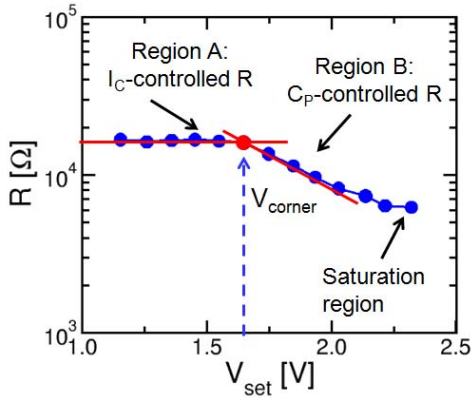

Fig. 5. Measured LRS resistance as a function of V_{set}, providing a definition of V_{corner}. As V_{set} varies due to stochastic switching, R shows two different behaviors: for low V_{set} (region A), set transition is controlled by I_C; thus, R remains independent of V_{set}. At high V_{set} (region B), the C_P-induced current overshoot takes place (see Fig. 4) as a result of the high switching speed at high voltage, thus causing relatively low R and correspondingly high I_{reset}.

as expected from Fig. 2(a). Most importantly, distributions show increasing tails for increasing N_C at low R, further supporting the device degradation. Fig. 3(b) shows the distributions of I_{reset} for the same cycles of Fig. 3(a): tails at high current occur in correspondence of low R tails, since a high I_{reset} is needed to dissolve the relatively large CF in the low R tail.

Fig. 4(a) and (b) shows the I–V curves collected for the same cells in the main part, corresponding to 50% (median) percentile [Fig. 4(a)], and in the tail [Fig. 4(b)] of the distribution. The median I–V curve shows a standard switching behavior with $I_{\text{reset}} \approx I_C$ [19]. On the other hand, the tail I–V curve shows a larger V_{set}, which is due to a deep HRS with high resistance, and a corresponding low R and high I_{reset} as a result of the current overshoot. In particular, the relatively high V_{set} causes a current overshoot, which results in a relatively low R and a correspondingly large $I_{\text{reset}} > I_C$. Although previous work has shown that much smaller overshoot effect can be attained in integrated 1T1R as opposed to the wire-bonded 1T1R structures [21], our data provide evidence for the overshoot effect in integrated $1T1R$ at particularly high V_{set}. The current overshoot in the distribution tail can be attributed to the parasitic capacitance C_P [19], [21], [22] in the $1T1R$ structure in Fig. 4(c). Calculated I–V curves in Fig. 4(a) and (b), which were obtained by an analytical model for set/reset processes [23] with $C_P = 30$ fF, closely accounting for the measured characteristics. We estimate that about 90% of C_P is due to the metal routing in our test structure, while the remaining 10% is contributed by the transistor. Note that data in Fig. 4(b) do not allow to directly evaluate the overshoot current during set transition, because we measured the transistor current at the source side, which does not include the capacitance discharge current [see Fig. 4(c)]. However, the overshoot current can be indirectly estimated by noting that I_{reset} is roughly equal to the maximum current during set transition; thus, we can argue that the overshoot current is approximately 80 μA in Fig. 4(b).

To further support the above explanation of the tail behavior, Fig. 5 shows the correlation plot of the LRS resistance R as a function of V_{set} for $N_C \approx 2 \times 10^4$. For the sake of clarity, only the average R is reported for each value of V_{set} considering 1000 consecutive cycles of a single RRAM device. Here, V_{set} and R were changing as a result of cycle-to-cycle variations, whereas N_C and the corresponding degradation state of the device can be considered approximately constant. Two regions can be distinguished in the correlation plot, namely, region A at low V_{set} and region B at relatively high V_{set}. The resistance R in region A is approximately constant and equal to the value expected from the compliance current, namely, $R \approx V_C/I_C$, where $V_C \approx 1$ V [19] as in the I–V curve of Fig. 4(a). On the other hand, region B corresponds to the distribution tails of Fig. 3, where R decreases with V_{set} as a result of the parasitic overshoot. The LRS resistance in region B is controlled by the parasitic capacitance C_P via the current overshoot as in Fig. 4(b). In region A, due to the relatively small V_{set}, the set transition takes place on a relatively long switching time t_{set}; thus, C_P is discharged at relatively low current levels below the I_C limit. Since t_{set} exponentially decreases at increasing V_{set} [24], [25], the set transition takes place within a relatively short time at high V_{set}. In this time frame, the current for the set transition is readily supplied by the capacitance C_P; thus, the device current can easily exceed the compliance current I_C. Current overshoot induces overgrowth of the CF, which is evidenced in the distribution tails at low R and high I_{reset} in Fig. 3. The difference between the regions A and B lies therefore in the different switching speed, which is slower than the RC time in A ($t_{\text{set}} > RC$) and faster in B ($t_{\text{set}} < RC$).

The different regimes in the R–V_{set} correlation plot allow to define the corner voltage V_{corner}, as the voltage marking the boundary between region A and B in Fig. 5. The corner voltage can thus be defined as the voltage V_{set} for which $t_{\text{set}} = RC_P$ thus marking the onset of region B for $V_{\text{set}} > V_{\text{corner}}$. Based on its definition, V_{corner} can be used as an additional monitor of the switching properties of the device and its degradation, similar to V_{set} and V_{reset}. Fig. 6(a) shows the average V_{set} as a function of R for $V_{\text{stop}} = -1.85$ V and increasing N_C for a single RRAM device. As N_C increases,

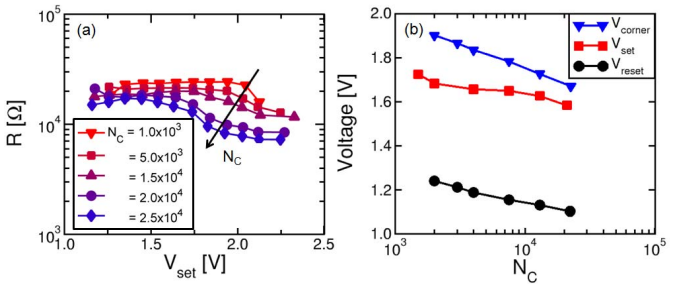

Fig. 6. (a) LRS resistance as a function of V_{set} for increasing N_C, and (b) average V_{corner}, V_{set}, and V_{reset} as a function of N_C. The R–V_{set} correlation indicates a decay of V_{corner} with a corresponding broadening of region B, hence of tails in Fig. 3, at increasing N_C. Degradation leads to a decrease of all the switching voltages, consistent with an increasing ion mobility in the active region.

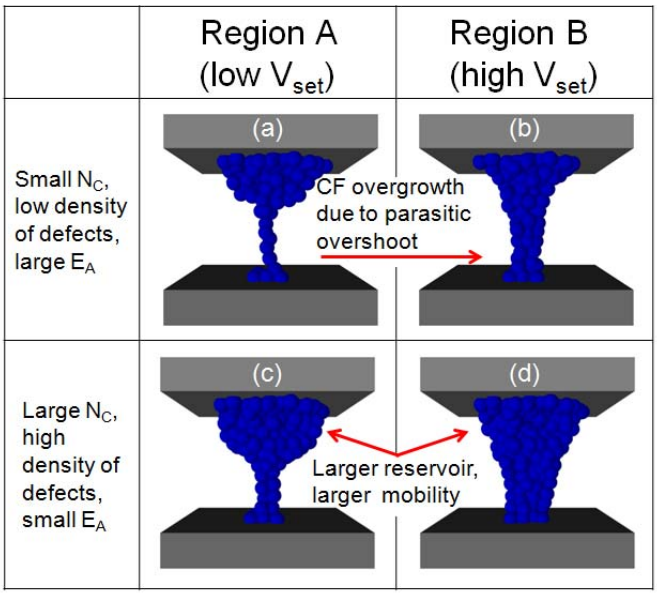

Fig. 7. Sketch of cycling-induced degradation effects for increasing N_C. At low N_C, (a) CF size of normal switching is well controlled by I_C in region A, while (b) relatively large CF is obtained by C_P-induced overshoot in region B. As N_C increases, (c) and (d) CF size in both region A and B, respectively, become larger because of the higher density of defects, e.g., oxygen vacancies, resulting in more migration paths and a correspondingly higher ion migration mobility.

R decreases in region A, consistently with Fig. 3(a), while V_{corner} decreases, thus causing the widening of region B. Fig. 6(b) shows V_{corner} extracted from Fig. 6(a) as a function of N_C, compared with V_{set} and V_{reset}, all showing a decaying behavior with N_C. Due to the decrease of V_{corner}, the RRAM device becomes more subject to parasitic overshoot, which thus accounts for the increasing tails at low R in Fig. 3(a). Since V_{corner} corresponds to a constant switching time, the decrease of V_{corner} provides evidence for the switching time becoming increasingly short at a given voltage with increasing N_C, as also supported by the decay of V_{set} and V_{reset}. We thus conclude that cycling degradation leads to a faster switching time, which we attribute to an enhanced ion migration.

IV. Physical Interpretation and Model

The cycling degradation phenomena in Figs. 2–6 are interpreted in terms of the defect generation model shown in Fig. 7.

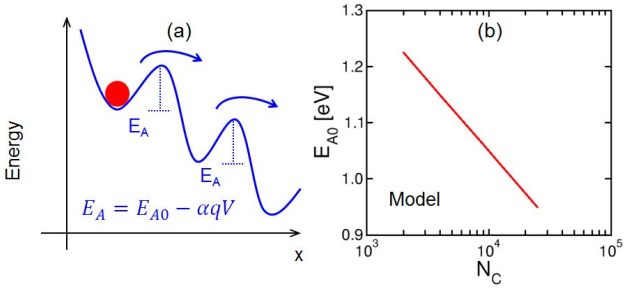

Fig. 8. Sketch of (a) energy barrier E_A for ion migration and (b) assumed E_{A0} as a function of N_C in our model for $V_{\text{stop}} = -1.85$ V.

Initially, relatively few defects are present in the active CF area; thus, the CF remains relatively small in region A [Fig. 7(a)], and larger in region B [Fig. 7(b)] as a result of the capacitive current overshoot. During cycling, repeated set/reset pulses cause the generation of additional defects (e.g., oxygen vacancies), thus increasing the defect reservoir at the TE side. The higher concentration of oxygen vacancies in the CF active region also causes an enhanced ion mobility [26]. This can be interpreted as the high oxygen vacancy concentration causing enhanced oxygen self-diffusion and lower migration barrier, which can be attributed to the larger available free space for ion migration and the weakening of local oxygen-cation bonds [26], [27]. As a result of the larger reservoir and higher mobility, the CF size after set transition in region A is increased after cycling in Fig. 7(c), thanks to the lower value of V_C, which reflects switching speed [19]. The larger CF in region A accounts for the decrease of R in Figs. 2(a) and 3(a) for LRS. In the presence of current overshoot at high V_{set}, the enhanced switching speed and the consequent decrease of V_{corner} result in even larger CF and lower R in the distribution tail in Fig. 7(d).

To model the degradation effects after cycling, we attributed the cycling-enhanced ion mobility to a decrease of the energy barrier E_{A0} controlling defect migration under an applied voltage, as shown in Fig. 8(a). Here, the energy barrier at a specific voltage is given by $E_A = E_{A0} - \alpha$ qV, where E_{A0} is the zero-voltage energy barrier and α is the coefficient describing voltage-induced barrier lowering [19]. Fig. 8(b) shows the assumed dependence of E_{A0} on N_C for a reference stop voltage $V_{\text{stop}} = -1.85$ V: E_{A0} decreases from 1.22 eV around 2×10^3 cycles to 0.95 eV around 2.5×10^4 cycles close to the failure. By introducing the decreasing E_{A0} in our analytical switching model [23], we simulated the I–V curves at increasing N_C and extracted LRS resistance R, V_{set}, and V_{reset} from the simulated I–V curves. Fig. 9 shows the measured and calculated I–V curves for $N_C = 1$ after forming process [Fig. 9(a)] and $N_C = 2 \times 10^4$ [Fig. 9(b)], indicating a decrease of V_{set} and V_{reset} at increasing N_C. The model can account for the I–V curves and for its dependence on N_C of the switching parameters, thus supporting our interpretation of enhanced ion migration in terms of decreased E_{A0}.

The analytical model also allows to calculate the correlation between LRS resistance and V_{set}, which we obtained by repeating the simulation of the I–V curve at varying V_{set},

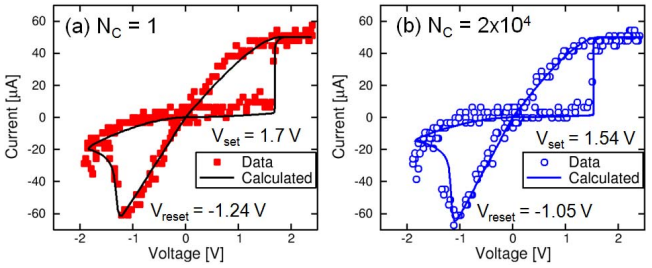

Fig. 9. Measured and calculated I–V curves for (a) $N_C = 1$ and (b) 2×10^4. Data indicate that cycling degradation causes a decrease of V_{set}, V_{reset}, and LRS resistance, the latter causing an increase of I_{reset}.

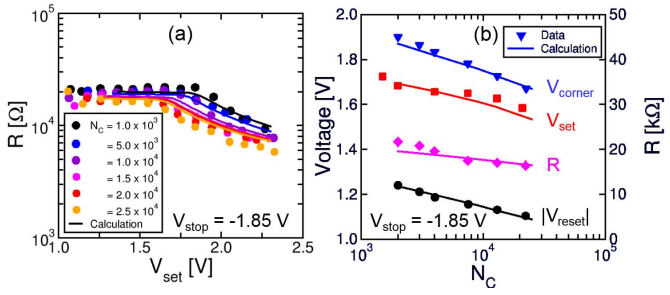

Fig. 10. (a) Measured and calculated correlation between the LRS resistance and V_{set} for increasing N_C, and (b) measured and calculated V_{set}, V_{reset}, V_{corner}, and LRS resistance as a function of N_C. Results in (a) and (b) were obtained with a physics-based analytical model of RRAM [23] with E_{A0} given in Fig. 8(b).

which was changed by assuming different initial values of the gap length in the CF to mimic the statistical variability of HRS in Fig. 5 [23]. Fig. 10(a) shows the measured and calculated R as a function of V_{set} at increasing N_C for $V_{\text{stop}} = -1.85$ V, indicating that the decreasing E_{A0} in our model can account for the decrease of V_{corner} with cycling. Fig. 10(b) shows the measured and calculated switching parameters, namely, V_{corner}, V_{set}, $|V_{\text{reset}}|$, and R as a function of N_C for $V_{\text{stop}} = -1.85$ V. Simulation results show that the model can well account for the decrease of the switching parameters with N_C, confirming the picture of an enhanced ion migration rate induced by cycling, and supporting our model for the prediction of RRAM degradation during cycling.

To further support our interpretation of RRAM degradation, we measured V_{set} and V_{reset} at variable pulsewidth t_P of the triangular set/reset pulse for increasing N_C. Fig. 11(a) schematically shows the pulse shape adopted for the experiments, where the sequences of triangular set/reset pulses were applied, and t_P was changed to monitor the sweep-rate dependence of the switching parameters. Fig. 11(b) shows the measured V_{set} and $|V_{\text{reset}}|$ as a function of t_P for increasing N_C. Both set and reset voltages decrease with t_P as a result of the time-voltage dependence of RRAM switching phenomena [19]. In addition, V_{set} and $|V_{\text{reset}}|$ decrease with increasing N_C due to degradation. Calculation results by our analytical model [23] in Fig. 11(c) show a similar dependence on t_P and N_C, thus further supporting the description of enhanced ion mobility by a decreased E_{A0} in Figs. 7 and 8.

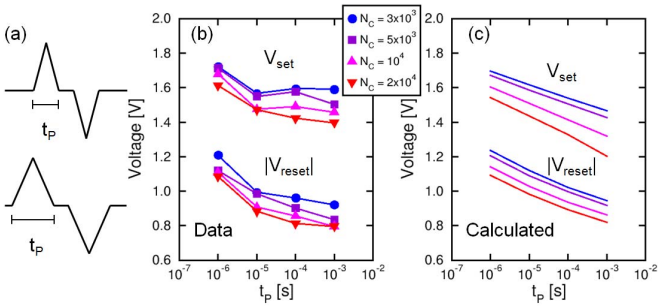

Fig. 11. Schematic illustration of the pulse shape for the experiments done at (a) variable t_P, (b) measured V_{set} and $|V_{\text{reset}}|$ as a function of t_P at increasing N_C and (c) corresponding calculation results.

V. Dependence on V_{stop}

Previous studies indicate that V_{stop}, namely, the maximum voltage in the negative reset operation, plays an important role in controlling endurance lifetime [16]. As V_{stop} is increased, the HRS increases, thus allowing to achieve a larger R window with less variability. On the other hand, the cycling endurance decreases with V_{stop} as a result of the negative set failure taking place during the reset operation.

To study the impact of V_{stop} on cycling-induced degradation, we analyzed the degradation of the switching parameters during cycling at various V_{stop}. Fig. 12 shows the average values of $|V_{\text{reset}}|$ [Fig. 12(a)], V_{corner} [Fig. 12(b)], and LRS resistance [Fig. 12(c)] as a function of N_C at the increasing values of $V_{\text{stop}} = -1.65$, -1.75, -1.85, and -1.95 V. All the parameters show an approximately linear decay with $\log(N_C)$, where the slope of the decay increases with $|V_{\text{stop}}|$. We define the *degradation rate* as the derivative of data in Fig. 12(a)–(c) with respect to $\log(N_C)$. Fig. 12(d) reports the degradation rate for $|V_{\text{reset}}|$, V_{corner}, and R, showing that all the degradation rates increase with $|V_{\text{stop}}|$. These results confirm the key role of V_{stop} in controlling RRAM degradation and failure.

VI. Modeling of V_{stop}-Dependent Degradation

To account for the degradation process taking place over several decades of N_C, we developed a model for the generation of defects with a distributed barrier E_D, as shown in Fig. 13(a). According to the model, defects are generated during set/reset cycling by a thermally activated process across multiple energy barriers with continuously distributed amplitude E_D. The defects with small generation barrier E_D [e.g., well 1 in Fig. 13(a)] are generated initially in the cycling, while the defects with high E_D [e.g., well 4 in Fig. 13(a)] are generated after a large N_C. In the model, the defect generation time τ obeys the Arrhenius law given by

$$\tau = \tau_0 e^{\frac{E_D}{kT}} \tag{1}$$

where τ_0 is a preexponential constant ($\tau_0 = 1$ μs), T is the local temperature in the CF region during set/reset, k is the Boltzmann constant, and E_D is a generic energy barrier within uniform distribution in Fig. 13(a). As N_C increases, the global time in (1) increases, thus defects with relatively high energy E_D start being generated because of the relationship between

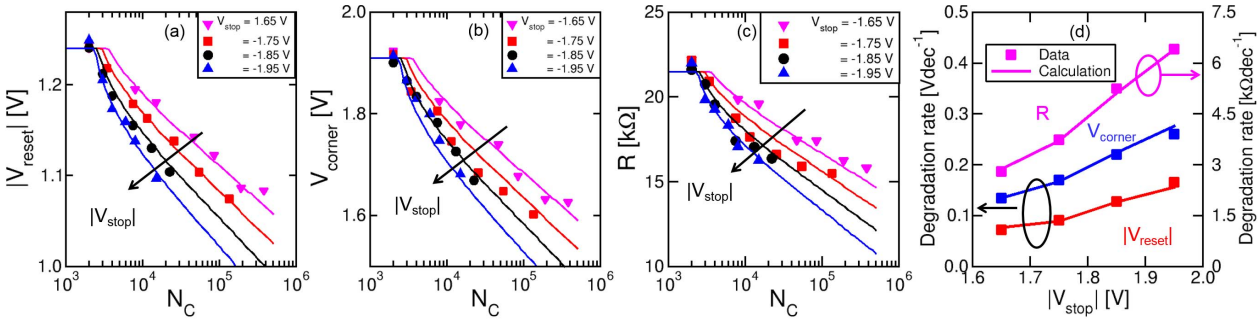

Fig. 12. (a) Measured and calculated $|V_{\text{reset}}|$, (b) $|V_{\text{corner}}|$ and (c) LRS resistance as a function of N_C at increasing V_{stop}, and (d) degradation rates for all the switching parameters as a function of $|V_{\text{stop}}|$. Results indicate that V_{stop} accelerates the degradation rates, supporting the key role of V_{stop} in RRAM degradation and failure.

generation time τ and energy barrier E_D in (1). The time-dependent defect distribution $g(E_D)$ is given by [28]

$$\frac{dg}{dt} = \frac{1-g}{\tau} \tag{2}$$

where t is the time measured during all the set/reset operations and τ is given by (1). In fact, given the thermally activated process described in (1), only the time during set and reset is effective for defect generation. The local temperature in the CF region can be evaluated by the analytical Joule heating formula given by [29]

$$T = T_0 + \alpha V^2 \tag{3}$$

where T_0 is the room temperature (300 K in our experiments) and α is a coefficient proportional to the ratio between effective thermal and electrical resistance in the CF region [16]. Local Joule heating during the set and reset processes accelerates the Arrhenius-driven defect generation. In particular, as $|V_{\text{stop}}|$ increases, T increases during reset, thus accounting for the role of V_{stop} in controlling the degradation rate. It should be noted that V_{stop} also causes a deeper HRS at the end of the reset operation, thus causing a relatively large V_{set} in the following set process [16]. The larger V_{set} causes a larger T during the set process, which also might induce more degradation based on (1)–(3). This highlights the role of V_{stop} in inducing higher local T both directly during the reset process, and indirectly during the set process.

Fig. 13(b) shows the calculated $g(E_D)$ at increasing N_C for $V_{\text{stop}} = -1.65$ V, obtained by the model in (1)–(3). In the calculation, we integrated (2) to evaluate $g(E_D)$ during all the set/reset cycles at variable V. Simulation results in Fig. 13(b) show that the defects at small E_D are first generated at small N_C, followed by the defects at high E_D for large N_C. By integrating the defect distribution $g(E_D)$, one gets the total defect density G, given by

$$G = \int g(E_D) dE_D \tag{4}$$

where $g(E_D)$ is integrated over the whole E_D-axis. The function G yields a figure of merit for the overall degradation in the CF region, and was assumed to be correlated with the value of E_{A0} dictating the energy barrier for defect migration during the set and reset processes. Fig. 13(c) shows the

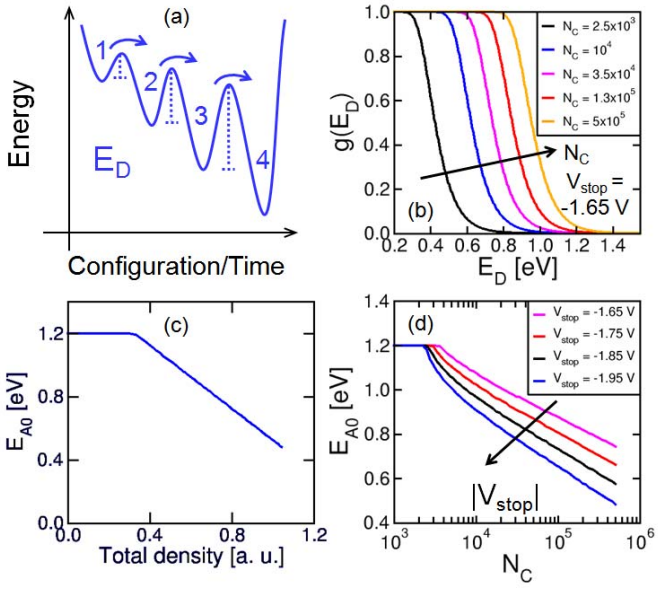

Fig. 13. Schematic illustration of (a) distributed-energy model for degradation, (b) calculated defect distribution $g(E_D)$ at increasing N_C for $V_{\text{stop}} = -1.65$ V, (c) calculated E_{A0} as a function of total defect density, and (d) calculated migration barrier E_{A0} as a function of N_C at increasing V_{stop}. The calculated E_{A0} can then be used in the analytical model of RRAM to compute the I–V characteristics for any degradation condition, namely, N_C and V_{stop} [23].

assumed piecewise-linear $E_{A0} - G$ correlation, which is based on the idea that a large value of G reflects a large degradation and large defect density in the CF area, thus corresponding to a relatively high ion mobility with low E_{A0}.

Fig. 13(d) shows the calculated E_{A0} as a function of N_C at increasing $|V_{\text{stop}}|$, obtained by (1)–(4). As $|V_{\text{stop}}|$ increases, E_{A0} decreases with increasingly steep slope, evidencing a faster degradation rate. By using the resulting E_{A0} obtained from the model in (1)–(4), one can calculate the I–V curve for the RRAM device at any degradation condition, namely, an arbitrary N_C and V_{stop}. For any value of E_{A0}, corresponding to a specific degradation state from Fig. 13, we performed simulations by using our analytical model for the set/reset processes [23]. By using this methodology, we calculated the switching parameters as a function of N_C. Fig. 12 shows the calculated $|V_{\text{reset}}|$ [Fig. 12(a)], $|V_{\text{reset}}|$ [Fig. 12(b)],

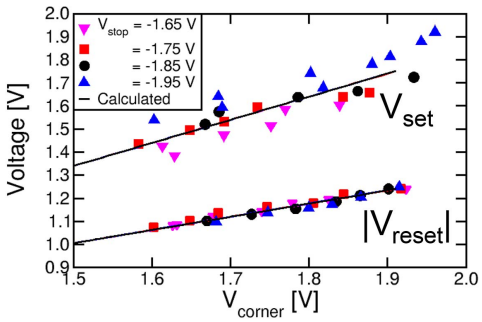

Fig. 14. Correlation of measured and calculated V_{set} and $|V_{reset}|$ as a function of V_{corner} at variable V_{stop}.

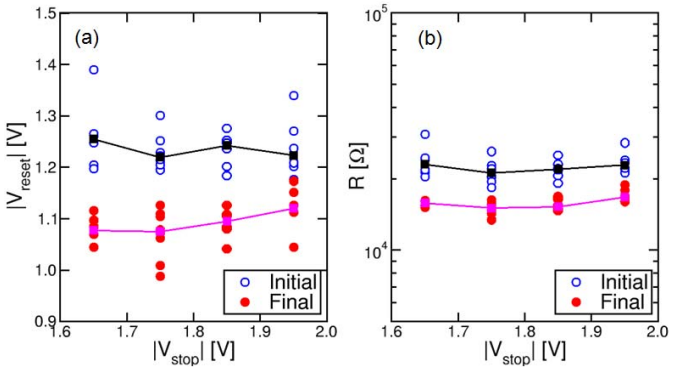

Fig. 15. (a) Measured V_{reset} and (b) LRS resistance as a function of V_{stop} for $N_C = 1$ (initial) and just before endurance failure (final), supporting V_{reset} and LRS resistance as reliable monitor for the prediction of failure.

and LRS resistance [Fig. 12(c)] as a function of N_C at increasing $|V_{stop}|$. Fig. 12(d) shows the corresponding degradation rates for all the parameters. Fig. 14 shows the correlation plot of measured and calculated V_{set} and $|V_{reset}|$ as a function of V_{corner}, where data and calculations were extracted from Fig. 12; results indicate a strong correlation among the switching parameters, irrespective of N_C and V_{stop} during degradation. Such a strong correlation supports our description of the degradation state in terms of a single parameter, namely, E_{A0} or equivalently G, in Fig. 13(d). In other words, the degraded state of the device can be described uniquely by the value of E_{A0}, irrespective of specific N_C and V_{stop}. These results support the accuracy of our model in predicting degradation of the I–V curves in RRAM after cycling.

VII. Degradation and Failure Monitors

Our results reveal that the RRAM switching parameters can be used as monitors of degradation, thus allowing to predict and anticipate device failure. To confirm this picture, Fig. 15 shows the initial ($N_C = 1$) and final values of $|V_{reset}|$ [Fig. 15(a)] and R [Fig. 15(b)] as a function of $|V_{stop}|$. For instance, $|V_{reset}|$ in Fig. 15(a) is around 1.25 V initially ($N_C = 1$), while its final value approaches 1.1 V at the end of device lifetime, i.e., just before endurance failure. Note that the endurance lifetime $N_{C,fail}$ changes by several decades by varying V_{stop} [16]. Despite this dramatic dependence of lifetime on V_{stop}, the critical values of V_{reset} and R do not show any significant variation, suggesting that the degradation state is approximately the same just before failure. Endurance failure can thus be considered as one of the degradation state along with other states in Fig. 12. By considering the I–V curve at any particular state of the device, one can thus anticipate how far the device is from the end of lifetime, without keeping track of the number of cycles and the value of V_{stop}. The latter, in particular, might change randomly from cycle-to-cycle if program-verify techniques are used, thus making indirect estimation of degradation quite difficult. The direct evaluation of one or more device switching parameters, e.g., V_{reset}, allows instead to anticipate device failure to distribute cycling for wear leveling in the memory array. For instance, V_{reset} and/or R could be monitored within one array block, where cells undergo a similar workload, for the purpose of monitoring average degradation and organize wear out leveling within the memory system. Similar system-level management algorithms are in fact becoming essential to maximize flash memory reliability, e.g., in solid-state drives [30], [31].

As a practical example of estimating the current endurance, we first note that $|V_{reset}|$ decreases linearly with log(t) between $N_{C0} = 2 \times 10^3$ and failure in Fig. 12(a). Thus, given V_{reset} at one specific point in life, we can evaluate the current cycle count as

$$\log(N_C) = \log(N_{C0}) + \frac{(V_{reset} - V_{reset,i})}{(V_{reset,f} - V_{reset,i})} \times [\log(N_{C,fail}) - \log(N_{C0})] \quad (5)$$

where $V_{reset,i}$ is the initial value of V_{reset}, $V_{reset,f}$ is the final value of V_{reset}, and $N_{C,fail}$ is the expected endurance lifetime, which depends on V_{stop}. Therefore, knowing the average operating V_{stop} for one particular product/operation, one can evaluate the average endurance lifetime $N_{C,fail}$, thus allowing to estimate the cycle count from (5). For instance, considering $V_{reset,i} = -1.25$ V and $V_{reset,f} = -1.1$ V in Fig. 12(a), and assuming $V_{stop} = -1.75$ V and $V_{reset} = -1.17$ V, we obtain $N_{C0} = 2 \times 10^4$ from (5), in good agreement with the linear fitting of V_{reset} in Fig. 12(a). This supports the ability to estimate degradation in RRAM devices based on the value of the switching parameters.

VIII. Conclusion

This paper addresses the cycling-induced degradation of RRAM devices and a new model to predict degradation effects as a function of the cycling conditions. We evidence that cycling degradation causes the decrease of V_{set}, V_{reset}, V_{corner}, and LRS resistance, as a result of an enhanced ion migration with reduced energy barrier E_{A0}. We show that the degradation rate increases with V_{stop}, which is consistent with previous results showing that endurance lifetime is controlled by V_{stop}. A distributed-energy Arrhenius model was introduced to model the V_{stop}-driven degradation kinetics. This paper indicates that device degradation and endurance failure can be predicted by monitoring the switching parameters during cycling.

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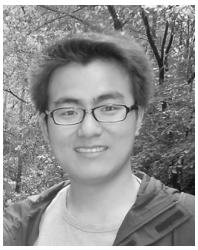

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