Instantaneous Conduction and Switching Losses in Two-level Voltage Source Inverters

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***Abstract*—A mathematical model is derived which allows to compute instantaneously the conduction and switching losses in two-level voltage source inverters (2L-VSIs) regardless of the employed modulation scheme. The model is based on the use of switching vectors applied to the considered VSI, taking into account the instantaneous conduction and switching losses of the semiconductor devices. The advantages of this method are, (i) it can be extended to any type of VSI and any modulation scheme, (ii) it can be applied to analyze the power losses of VSIs during any desired period, and (iii) it can be easily implemented in any kind of the simulation software (e.g. Matlab/Simulink).**

***Index Terms*—Power Diode, Power IGBT, Conduction Losses, Switching Losses, Model of 2L-VSIs, Instantaneous Losses of Semiconductor Devices.**

NOTATION

$\mathbb{N}, \mathbb{R}$: natural, real numbers. $\boldsymbol{x} := (x_1, \dots, x_n)^\top \in \mathbb{R}^n$: column vector (bold small letter), $n \in \mathbb{N}$ where "$^\top$" and ":=" mean "transposed" (interchanging rows and columns of a matrix or vector) and "is defined as", resp., $\mathbf{0}_n \in \mathbb{R}^n$: zero vector. $\boldsymbol{x}^\top \boldsymbol{y} := x_1 y_1 + \dots + x_n y_n$: scalar product of the vectors $\boldsymbol{x}$ and $\boldsymbol{y} := (y_1, \dots, y_n)^\top$. $\boldsymbol{A} \in \mathbb{R}^{n \times n}$: (square) matrix with n rows and columns (bold capital letter).

I. INTRODUCTION

The total power losses of semiconductor devices are divided into conduction and switching losses. The former can be obtained based on the voltage-over-current (v-i) characteristic of the semiconductor devices and the latter can be calculated by using the switching energy losses given in the data sheet. Many efforts have been done to compute power losses of voltage source inverters. One common method to find the power losses in VSIs has been presented in [1], [2]. This method is based on the key assumptions that the conduction losses in semiconductor devices are a function of the current(s) passing through the semiconductor devices, the time duration when the semiconductor is on or the duty cycle, the PWM modulation scheme and its modulation index, and the load power factor. Therefore, this method is suitable to calculate the *average* power losses of semiconductor devices in 2L-VSIs for a given (e.g. PWM) modulation scheme, but it can not be applied to other modulation schemes. The major obstacle is to find the duty cycle, because it depends on the implemented modulation schemes and the type of the employed voltage source inverter [3], [6]. Moreover, it is difficult or even impossible to propose a method to find the duty cycle for more sophisticated (e.g. flat-top) modulation schemes. A method which is independent of the duty cycle for a 2L-VSI has been reported in [7]. With this method, the phase voltage waveform is decomposed into square waves and its summation of the square waves with rising edge angle α_k. Therefore, the conduction power losses are a function of the current passing through the semiconductors, the load power factor and the rising edge angle α_k of the voltage square waves. This approach is independent of the employed modulation scheme and duty cycle, but the detection of the rising edge angle α_k of the occurring square waves is rather complicated. Another method is based on actual measurements of the semiconductor losses [8]. To do so, a clamped inductive load test is suggested to measure the switching power losses while a boost converter is used to measure the conduction losses in this converter topology. In contrast to the above mentioned approaches, we propose a simple method which allows an instantaneous computation of the power losses of the semiconductor devices in any VSIs topology. In this paper, we present the approach for a 2L-VSI. The power losses are obtained by using the *actual switching vector* $\boldsymbol{s}^{abc}(t) := (s^a(t), s^b(t), s^c(t))^\top \in \{0,1\}^3$ (with individual switching signal $s^x(t) \in \{0,1\}$ per phase $x \in \{a,b,c\}$) and the direction (positive or negative) of the actual phase currents $\boldsymbol{i}^{abc}(t) = (i^a(t), i^b(t), i^c(t))^\top \in \mathbb{R}^3$ (with individual current $i^x(t)$ of phase $x \in \{a,b,c\}$). For those switching signals $s^x(t) = 1$ which are one, the *conduction losses* are dissipated in the respective semiconductor device (and the free-wheeling diodes) which are "on" (during the interlock delay time). The *switching losses* can be computed by considering the transition of the switching signal $s^x(t)$ from one to zero (and vice versa) and the direction of phase current $i^x(t)$. Combining both ideas gives a method which allows to instantaneously compute the overall power losses in VSIs independently of modulation scheme and topology.

The paper is organized as follows: Section II introduces the mathematical model of the considered 2L-VSI. Section III proposes the mathematical models of the power losses of the semiconductor devices in 2L-VSIs based on the switching

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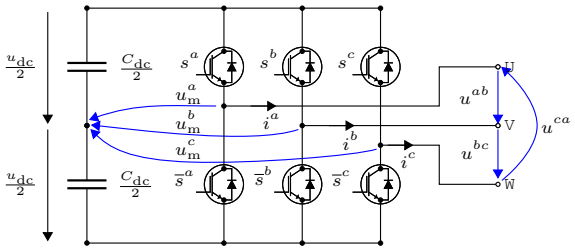

Fig. 1: *Electrical circuit of 2L-VSI with (virtually) split DC-link, IGBTs and free-wheeling diodes.*

vector. Section IV illustrates the method for a grid-connected 2L-VSI with LCL-filter and RL-load by simulation results.

II. Model of Two-Level Voltage Source Inverters

A mathematical model of the inverter must be established based on the actual switching vector $\boldsymbol{s}^{abc}(t) = (s^a(t), s^b(t), s^c(t))^\top$ and DC-link voltage $u_{\mathrm{dc}}(t)$. As depicted in Fig. 1, the switching value $s^x(t)$ and its negated value $\overline{s}^x(t) = 1 - s^x(t)$ (where $x \in \{a, b, c\}$) lead to the inverter leg voltage vector [11, Cha. 14]

$$\boldsymbol{u}^{abc}_{\mathrm{m}}(t) = \begin{pmatrix} u^a_{\mathrm{m}}(t) \\ u^b_{\mathrm{m}}(t) \\ u^c_{\mathrm{m}}(t) \end{pmatrix} = u_{\mathrm{dc}}(t)\big(\boldsymbol{s}^{abc}(t) - \tfrac{1}{2}\mathbf{1}_3\big) \in \{\pm\tfrac{u_{\mathrm{dc}}(t)}{2}\}^3,$$

where $\mathbf{1}_3 := (1, 1, 1)^\top$ is the unity vector. The output (symmetric) phase voltages $\boldsymbol{u}^{abc}(t)$ depend on the DC-link voltage and the switching vector as follows (see [10] or [11, Cha. 14])

$$\boldsymbol{u}^{abc}(t) = \begin{pmatrix} u^a(t) \\ u^b(t) \\ u^c(t) \end{pmatrix} = \tfrac{u_{\mathrm{dc}}(t)}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \boldsymbol{s}^{abc}(t). \quad (1)$$

Via the terminals U, V, and W, the voltages are applied to a connected load and lead to the phase currents $\boldsymbol{i}^{abc}(t) := (i^a(t), i^b(t), i^c(t))^\top$.

III. Instantaneous Power Losses in 2L-VSIs

The conduction losses in a 2L-VSI are caused by the turn-on resistance of the semiconductor devices while the switching losses are due to the commutation between the different switching states of the converter. The distribution and localization of the switching and conduction losses for 2L-VSIs are summarized in Tab. I and Tab. II, respectively.

A. Conduction losses

The vectors for the *conduction losses (cl)* of an IGBT and a diode are respectively given by

$$\boldsymbol{p}^{abc}_{\mathrm{cl,igbt}}(t) = \begin{pmatrix} R_{\mathrm{d,igbt}}\, i^a(t)^2 + U_{\mathrm{th,igbt}}|i^a(t)| \\ R_{\mathrm{d,igbt}}\, i^b(t)^2 + U_{\mathrm{th,igbt}}|i^b(t)| \\ R_{\mathrm{d,igbt}}\, i^c(t)^2 + U_{\mathrm{th,igbt}}|i^c(t)| \end{pmatrix}, \quad (2)$$

and

$$\boldsymbol{p}^{abc}_{\mathrm{cl,diode}}(t) = \begin{pmatrix} R_{\mathrm{d,diode}}\, i^a(t)^2 + U_{\mathrm{th,diode}}|i^a(t)| \\ R_{\mathrm{d,diode}}\, i^b(t)^2 + U_{\mathrm{th,diode}}|i^b(t)| \\ R_{\mathrm{d,diode}}\, i^c(t)^2 + U_{\mathrm{th,diode}}|i^c(t)| \end{pmatrix}, \quad (3)$$

TABLE I: Conduction losses (CL) in 2L-VSI. Conduction losses in the diodes are only during the interlock delay time (k is the generic discrete time).

$s^x[k]$	upper IGBT^x	lower IGBT^x	upper Diode^x	lower Diode^x
$i^x[k] \geq 0,\ x \in \{a,b,c\}$				
1	CL	-	-	-
0	-	-	-	CL
$i^x[k] < 0,\ x \in \{a,b,c\}$				
1	-	-	CL	-
0	-	CL	-	-

TABLE II: "Turn-on" and "turn-off" switching losses (SW-ON & SW-OFF) of IGBTs and reverse recovery losses (RR) of diodes in 2L-VSI (k is the generic discrete time).

$s^x[k-1]$	$s^x[k]$	up. IGBT^x	low. IGBT^x	up. Diode^x	low. Diode^x
$i^x[k] > 0,\ x \in \{a,b,c\}$					
0	1	SW-ON	-	-	SW-OFF
1	0	SW-OFF	-	-	-
$i^x[k] < 0,\ x \in \{a,b,c\}$					
1	0	-	SW-ON	SW-OFF	-
0	1	-	SW-OFF	-	-

where $R_{\mathrm{d,igbt}}$ and $R_{\mathrm{d,diode}}$ (in Ω) are the dynamic resistances, and $U_{\mathrm{th,igbt}}$ and $U_{\mathrm{th,diode}}$ (in V) are the threshold voltages of diode and IGBT, respectively. These parameters are usually available from the data sheet of the semiconductor(s). Note that the phase currents $i^x(t)$, $x \in \{a, b, c\}$ are approximately equal to the collector currents passing through the respective IGBTs (when turned on). Tab. I summarizes the location of the conduction losses in the 2L-VSI depending on the actual switching vector and phase current direction. To detect the direction of the phase currents, the Heaviside function and $\boldsymbol{d}(t)$ are introduced as follows

$$h(x) := \begin{cases} 1, & x \geq 0 \\ 0, & x < 0 \end{cases} \quad \text{and} \quad \boldsymbol{d}(t) := \begin{pmatrix} h(i^a(t)) \\ h(i^b(t)) \\ h(i^c(t) \end{pmatrix}. \quad (4)$$

Then, with the switching matrix

$$\boldsymbol{S}^{abc}(t) := \begin{bmatrix} s^a(t) & 0 & 0 \\ 0 & s^b(t) & 0 \\ 0 & 0 & s^c(t) \end{bmatrix}, \quad (5)$$

the *instantaneous conduction losses* $p^{abc}_{\mathrm{cl,2l\text{-}vsi}}$ (in W) of a 2L-VSI at a discrete time instant[1] k are given by

$$\begin{aligned} &p^{abc}_{\mathrm{cl,2l\text{-}vsi}}[k] = \\ &\boldsymbol{p}^{abc}_{\mathrm{cl,igbt}}[k]^\top \Big[\underbrace{\boldsymbol{S}^{abc}[k]\boldsymbol{d}[k]}_{s^x[k]=1 \text{ and } i^x[k]>0} + \underbrace{\big(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k]\big)\big(\mathbf{1}_3 - \boldsymbol{d}[k]\big)}_{s^x[k]=0 \text{ and } i^x[k]<0} \Big] \\ &+ \boldsymbol{p}^{abc}_{\mathrm{cl,diode}}[k]^\top \Big[\underbrace{\boldsymbol{S}^{abc}[k]\big(\mathbf{1}_3 - \boldsymbol{d}[k]\big)}_{s^x[k]=1 \text{ and } i^x[k]<0} + \underbrace{\big(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k]\big)\boldsymbol{d}[k]}_{s^x[k]=0 \text{ and } i^x[k]>0} \Big]. \end{aligned} \quad (6)$$

[1]Note that a discrete time instant $k \in \mathbb{N}$ approximates the actual time instant $t \approx k \cdot T_{\mathrm{s}}$ with a multiple of the sampling time T_{s}.

where $\boldsymbol{I}_3 := \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ and $\boldsymbol{p}^{abc}_{\mathrm{cl,igbt}}[k]$ and $\boldsymbol{p}^{abc}_{\mathrm{cl,diode}}[k]$ are the instantaneous loss vectors as in (2) and (3), respectively.

In the following, the formula (6) is explained in more detail. The four terms on the right-hand side in (6) describe the conduction losses in the IGBTs and the diodes, respectively; depending on the actual switching state $s^x(t)$ and the current direction (sign of) $i^x(t)$ for $x \in \{a, b, c\}$. At a given time $t = k$, assume that the upper switch of leg $x \in \{a, b, c\}$ is turned on, then $s^x[k] = 1$. Hence, the corresponding entry in $\boldsymbol{S}^{abc}[k]$ and $(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k])$ equal one and zero, respectively. The latter explains why the second and fourth term of the vectors on the right-hand side in (6) equal zero and vanish (independently of the current direction). If the current in phase/leg $x \in \{a, b, c\}$ is positive, i.e. $i^x[k] > 0$, it flows through the upper controllable switch (recall Tab. I). Hence, $h(i^x[k]) = 1$ and the corresponding row of $\boldsymbol{d}[k]$ equals one. This explains the first term on the right-hand side of (6). If the leg current is negative, i.e. $i^x[k] < 0$, it flows through the upper free-wheeling diode and $h(i^x[k]) = 0$. The corresponding row of $\boldsymbol{d}[k]$ equals zero and of $(\mathbf{1}_3 - \boldsymbol{d}[k])$ equals one. This explains the third term on the right-hand side in (6). The same reasoning can be applied when the lower switch of leg x is turned on. Then, $s^x[k] = 0$ (or $\overline{s}^x[k] = 1 - s^x[k] = 1$). The corresponding terms of $\boldsymbol{S}^{abc}[k]$ and $(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k])$ equal zero and one, respectively. Again, the first and third terms on the right-hand side of (6) vanish (independently of the current direction). If the leg current is negative, i.e. $i^x[k] < 0$, it flows through the lower controllable switch (recall Tab. I) and $h(i^x[k]) = 0$. The corresponding row of $(\mathbf{1}_3 - \boldsymbol{d}[k])$ is one. If the leg current is positive, i.e. $i^x[k] > 0$, it flows through the lower free-wheeling diode and $h(i^x[k]) = 1$. Hence, the corresponding row of $\boldsymbol{d}[k]$ equals one.

B. Switching losses

The switching losses (sw) can be calculated from Tab. II. From Tab. II, it should be observed that when a controllable switch turns on the opposite free-wheeling diode turns off and in both of them there are losses (switch-on and reverse recovery, respectively). The vectors of the turn-on and turn-off switching losses (sw-on & sw-off) of the IGBT and the reverse recovery losses (rr) of the diode are given by [9]

$$\boldsymbol{p}^{abc}_{\mathrm{sw\text{-}y,igbt}}(t) = \frac{f_{\mathrm{sw}} E_{\mathrm{sw\text{-}y}}}{I_{\mathrm{c\text{-}ds}}} \left(\frac{U_{\mathrm{ce}}}{U_{\mathrm{ce\text{-}ds}}} \right)^{1.49} \begin{pmatrix} |i^a(t)| \\ |i^b(t)| \\ |i^c(t)| \end{pmatrix}, \qquad (7)$$

and

$$\boldsymbol{p}^{abc}_{\mathrm{rr,diode}}(t) = f_{\mathrm{sw}} \frac{U_{\mathrm{r}} Q_{\mathrm{rr}}}{4\sqrt{I_{\mathrm{f\text{-}ds}}}} \left(\frac{U_{\mathrm{r}}}{U_{\mathrm{r\text{-}ds}}} \right)^{0.6} \begin{pmatrix} \sqrt{|i^a(t)|} \\ \sqrt{|i^b(t)|} \\ \sqrt{|i^c(t)|} \end{pmatrix}, \qquad (8)$$

where f_{sw} (in Hz) is the switching frequency, $E_{\mathrm{sw\text{-}y}}$ (in J) is the switching energy loss at the rated current $I_{\mathrm{c\text{-}ds}}$ (in A) and rated voltage $U_{\mathrm{ce\text{-}ds}}$ (in V), respectively, U_{ce} (in V) is the reverse voltage across the IGBT (when turned off). $I_{\mathrm{f\text{-}ds}}$ (in A) and $U_{\mathrm{r\text{-}ds}}$ (in V) are the forward current and the voltage for a specified reverse recovery charges Q_{rr} (in C), and U_{r} (in V) is the reverse voltage across the diode (when not conducting). All these parameters are usually given in the data sheet. Note that (7) describes the turn-on switching losses if $\mathrm{y} = \mathrm{on}$ and the turn-off switching losses if $\mathrm{y} = \mathrm{off}$.

To obtain the overall switching losses, the preceding and the actual (discrete) time instant $k-1$ and k are considered to determine when a change in the switching vector occurs (recall also Tab. II). Then, the directions of the phase currents $\boldsymbol{i}^{abc}[k]$ are used to find which semiconductor device is dissipating power due to switching. The *instantaneous switching losses* $p^{abc}_{\mathrm{sw,2l\text{-}vsi}}$ (in W) of a 2L-VSI at time instant k are given by

$$\begin{aligned} p^{abc}_{\mathrm{sw,2l\text{-}vsi}}[k] = \Big(& \boldsymbol{p}^{abc}_{\mathrm{rr,diode}}[k] + \\ & + \boldsymbol{p}^{abc}_{\mathrm{sw\text{-}on,igbt}}[k] \Big)^{\top} \Big(\underbrace{(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k-1]) \boldsymbol{S}^{abc}[k] \boldsymbol{d}[k]}_{s^x[k-1] = 0 \text{ and } s^x[k] = 1 \text{ and } i^x[k] > 0.} \\ & + \underbrace{\boldsymbol{S}^{abc}[k-1] (\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k]) (\mathbf{1}_3 - \boldsymbol{d}[k])}_{s^x[k-1] = 1 \text{ and } s^x[k] = 0 \text{ and } i^x[k] < 0.} \Big) + \\ & \boldsymbol{p}^{abc}_{\mathrm{sw\text{-}off,igbt}}[k]^{\top} \Big(\underbrace{\boldsymbol{S}^{abc}[k-1] (\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k]) \boldsymbol{d}[k]}_{s^x[k-1] = 1 \text{ and } s^x[k] = 0 \text{ and } i^x[k] > 0.} \\ & + \underbrace{(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k-1]) \boldsymbol{S}^{abc}[k] (\mathbf{1}_3 - \boldsymbol{d}[k])}_{s^x[k-1] = 0 \text{ and } s^x[k] = 1 \text{ and } i^x[k] < 0.} \Big). \end{aligned} \qquad (9)$$

(9) describes the turn-on and turn-off switching losses and reverse-recovery losses of a 2L-VSI depending on preceding $s^x[k-1]$ and actual $s^x[k]$ switching state and actual current direction $h(i^x[k])$ of each phase $x \in \{a, b, c\}$. To explain the model (9) in more detail, assume that, at the preceding discrete time instant $k-1$, the upper switch of leg x ($x \in \{a, b, c\}$) is turned off and that it is turned on at the following time instant k. Then, $s^x[k-1] = 0$ and $s^x[k] = 1$ (recall first line of Tab. II). Hence, the corresponding terms $\boldsymbol{S}^{abc}[k-1]$ and $(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k-1])$ equal zero and one, respectively. Analogously, the corresponding terms in $\boldsymbol{S}^{abc}[k]$ and $(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k-1])$ equal one and zero, respectively. If the current of leg/phase x is positive, i.e. $i^x[k] > 0$, it passes from the lower diode (at time $k-1$) to the upper controllable switch (at time k). Therefore, $h(i^x[k]) = 1$ and the corresponding row of $\boldsymbol{d}[k]$ equals one. This explains the first term on the right-hand side of (9). It can be seen that all the other terms on the right-hand side of (9) equal zero and vanish; either because of $(\mathbf{1}_3 - \boldsymbol{d}[k]) = 0$ (second and fourth term) or $(\boldsymbol{I}_3 - \boldsymbol{S}^{abc}[k-1]) = 0$ (third term). A similar argument holds true for the other terms if the lower controllable switch is turned on and/or the current direction is negative. To sum up: The first term in (9) corresponds to the first line of Tab. II, the second term in (9) to the third line of Tab. II, the third term in (9) to the second line of Tab.II and the fourth term in (9) to the fourth line of Tab. II.

C. Summary

To conclude this section: Equations (6) and (9) are mathematical models of the *instantaneous* conduction and switching losses of a 2L-VSI. The models depend on (i) *known* electrical

parameters of the power electronic devices (e.g. extracted from data sheets; recall (2), (3), (7) and (8)), (ii) the preceding and the actual switching state, i.e. $\boldsymbol{s}^{abc}[k-1]$ and $\boldsymbol{s}^{abc}[k]$, and (iii) the actual directions and magnitudes of the phase currents $\boldsymbol{i}^{abc}[k]$. Both equations can easily be implemented in any numerical simulation software and allow to calculate the *instantaneous* (and, clearly, *average*) power losses of 2L-VSIs.

IV. Simulation results

In this section, the computation of the instantaneous conduction and switching losses with the help of the proposed models (6) and (9) is illustrated, respectively. To do so, the grid-connected two-level voltage source inverter (2L-VSI) shown in Fig. 2 with the parameters collected in Tab. III is implemented in Matlab/Simulink. The system consists of the 2L-VSI model (1), an LCL-filter, an RL-filer and an ideal grid (with resistive-inductive behavior). Details of the dynamical models of the filters and the grid are omitted here due to space limitations but can be found in [10], [12].

At first, the proposed computation of the losses with (6) and (9) is compared to the averaging method presented in [1]. Therefore, the average power losses must be calculated. To do so, assume that there are $N_\mathrm{s} = T_\mathrm{p} f_\mathrm{sw} \in \mathbb{N}$ samples of the computed conduction and switching losses over one period T_p (in s) of the inverter output waveform with switching frequency f_sw; then, the average conduction and switching losses can be computed, respectively, as follows

$$P^{\mathrm{ave}}_{\mathrm{cl,2l-vsi}} = \frac{\sum_{k=1}^{N_s} p^{abc}_{\mathrm{cl,2l\text{-}vsi}}[k]}{N_\mathrm{s}} \tag{10}$$

and

$$P^{\mathrm{ave}}_{\mathrm{sw,2l-vsi}} = \frac{\sum_{k=1}^{N_s} p^{abc}_{\mathrm{sw,2l\text{-}vsi}}[k]}{N_\mathrm{s}}, \tag{11}$$

where $p^{abc}_{\mathrm{cl,2l\text{-}vsi}}[k]$ and $p^{abc}_{\mathrm{sw,2l\text{-}vsi}}[k]$ are as in (6) and (9), respectively.

In Tab. IV, the simulated results for (10) and (11) are summarized and compared with averaging computation methods from [1] for different load power factors φ between $-60°$ and $60°$. All results were obtained considering the exact identical conditions. Since the currents through the semiconductor devices change for varying load power factors, the conduction and switching losses will also change. The comparison in

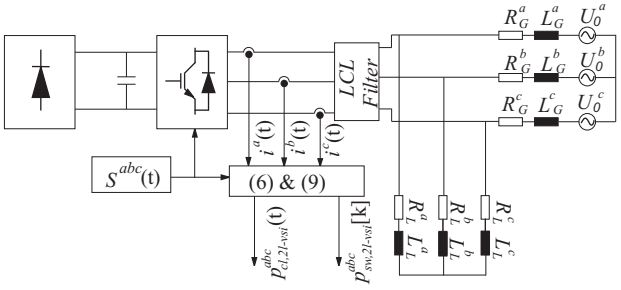

Fig. 2: *Model of the 2L-VSI connected to the resistive-inductive grid and RL-load via LCL-filter.*

TABLE III: Simulation data for system shown in Fig. 2

Component	values
LCL-filter	$L_{f1}^{a,b,c} = 6.2\,\mathrm{mH}$, $C_f^{a,b,c} = 2.2\,\mu\mathrm{F}$ and $L_{f2}^{a,b,c} = 1\,\mathrm{mH}$
Grid	$\hat{u}_0^{a,b,c} = 220\,\mathrm{V}$, $R_G^{a,b,c} = 0.1\,\Omega$, $L_G^{a,b,c} = 0.05\,\mathrm{mH}$ and $f_0 = 50\,\mathrm{Hz}$
RL-load	$R_L^{a,b,c} = 6.5\,\Omega$ and $L_L^{a,b,c} = 60\,\mathrm{mH}$ with load power factor $-\frac{\pi}{3} < \varphi < \frac{\pi}{3}$
2L-VSI	$u_\mathrm{dc} = 560\,\mathrm{V}$, $I_\mathrm{rated} = 40\,\mathrm{A}$ and $f_\mathrm{sw} \in [1,\ 20]\mathrm{kHz}$
Diode	$R_\mathrm{d,diode} = 7.7 \cdot 10^{-3}\,\Omega$, $U_\mathrm{th,diode} = 0.9\,\mathrm{V}$, $U_\mathrm{r} = 560\,\mathrm{V}$, $Q_\mathrm{rr} = 0.75 \cdot 10^{-6}\,\mathrm{A\,s}$, $I_\mathrm{f\text{-}ds} = 30\,\mathrm{A}$, $U_\mathrm{r} = 560\,\mathrm{V}$, $U_\mathrm{r\text{-}ds} = 400\,\mathrm{V}$
IGBT (IKW50N60DTP)	$R_\mathrm{d,igbt} = 12.5 \cdot 10^{-3}\,\Omega$, $U_\mathrm{th,igbt} = 0.8\,\mathrm{V}$, $U_\mathrm{ce} = 400\,\mathrm{V}$, $U_\mathrm{ce\text{-}ds} = 600\,\mathrm{V}$, $I_\mathrm{c\text{-}ds} = 50\,\mathrm{A}$, $E_\mathrm{sw\text{-}on} = 0.85\,\mathrm{mJ}$ and $E_\mathrm{sw\text{-}off} = 2.38\,\mathrm{mJ}$

TABLE IV: Comparison of computation as in [1] and proposed computation for sinusoidal PWM modulation and different power factors φ.

	proposed computation		computation as in [1]	
φ	$P^{\mathrm{ave}}_{\mathrm{cl,2l-vsi}}$ (in W)	$P^{\mathrm{ave}}_{\mathrm{sw,2l-vsi}}$ (in W)	$P^{\mathrm{ave}}_{\mathrm{cl,2l-vsi}}$ (in W)	$P^{\mathrm{ave}}_{\mathrm{sw,2l-vsi}}$ (in W)
$60°$	89.47	57.87	87.11	59.90
$30°$	90.65	58.44	88.20	60.50
$0°$	91.08	58.59	88.49	60.67
$-30°$	91.08	58.60	88.50	60.67
$-60°$	90.65	58.44	88.20	60.50

Tab. IV highlights the almost identical results of the averaging method from [1] and the proposed method in this paper.

Next, in Fig. 3, the *instantaneous* conduction and switching losses are illustrated for varying switching frequencies (while the other parameters are kept constant). Note that the conduction losses do not change significantly and have almost identical average values, while the switching losses clearly increase with increasing switching frequencies.

Another interesting feature of the loss models (6) and (9) is that the loss computation does not rely on the other system (such as LCL, RL or grid) parameters. The loss models in (6) and (9) only depend on the preceding and actual switching vector $\boldsymbol{s}^{abc}[k-1]$ and $\boldsymbol{s}^{abc}[k]$ and the actual phase current vector $\boldsymbol{i}^{abc}[k]$. Fig. 4 shows how the power losses change for varying modulation indices M_ind. Clearly, both conduction and switching losses increase for increasing modulation indices M_ind (since the current magnitudes increase).

Finally, Fig. 5 highlights another advantage of the proposed loss computation: The loss models (6) and (9) can be used for *any* modulation scheme. Fig. 5 shows the conduction and switching losses of a 2L-VSI for (a) sinusoidal pulse width modulation (SPWM), (b) third harmonic injection pulse width modulation (THIPWM) and (c) space vector pulse width modulation (SVPWM), respectively. If both, conduction and switching losses, are considered, it can be seen that SVPWM has the least power losses while THIPWM has the highest power losses among these three modulation schemes.

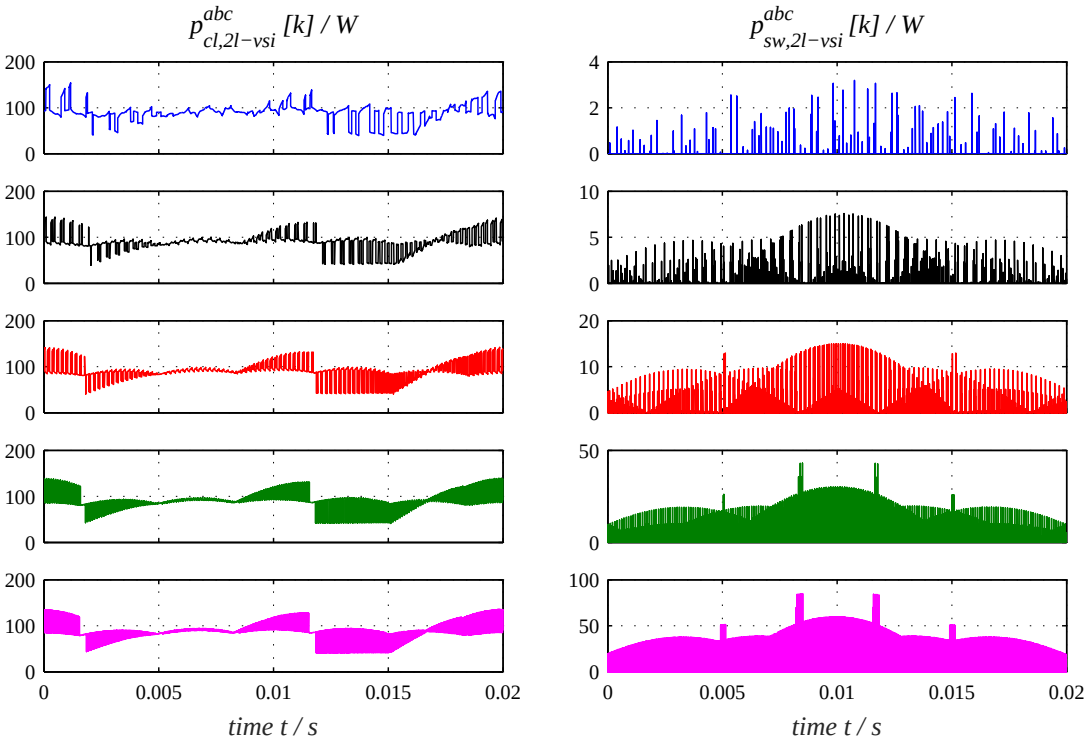

Fig. 3: *Conduction losses (left) and switching losses (right) of a 2L-VSI for different switching frequencies (from top to bottom):* $f_{\mathrm{sw}} = 1\,\mathrm{kHz}$, $f_{\mathrm{sw}} = 2.5\,\mathrm{kHz}$, $f_{\mathrm{sw}} = 5\,\mathrm{kHz}$, $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$ *and* $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$, *respectively.*

V. Conclusion

A simple method has been proposed to compute the instantaneous conduction and switching losses of two-level voltage source inverters (2L-VSIs). The proposed computation only depends on the preceding and actual switching vector, the actual phase current and the electrical parameters available from the data sheet of the employed semiconductor devices of the 2L-VSI. Firstly, a model of the 2L-VSI has been introduced depending on DC-link voltage and the actual switching vector. Then, the mathematical models of instantaneous conduction and switching losses were derived. The main advantages of the proposed method are (i) the losses can be computed independently of the used modulation schemes, (ii) both average and instantaneous losses can easily be obtained, and (iii) the proposed method can in principle be extended (ongoing research) to any inverter/converter topology comprising IGBTs and diodes.

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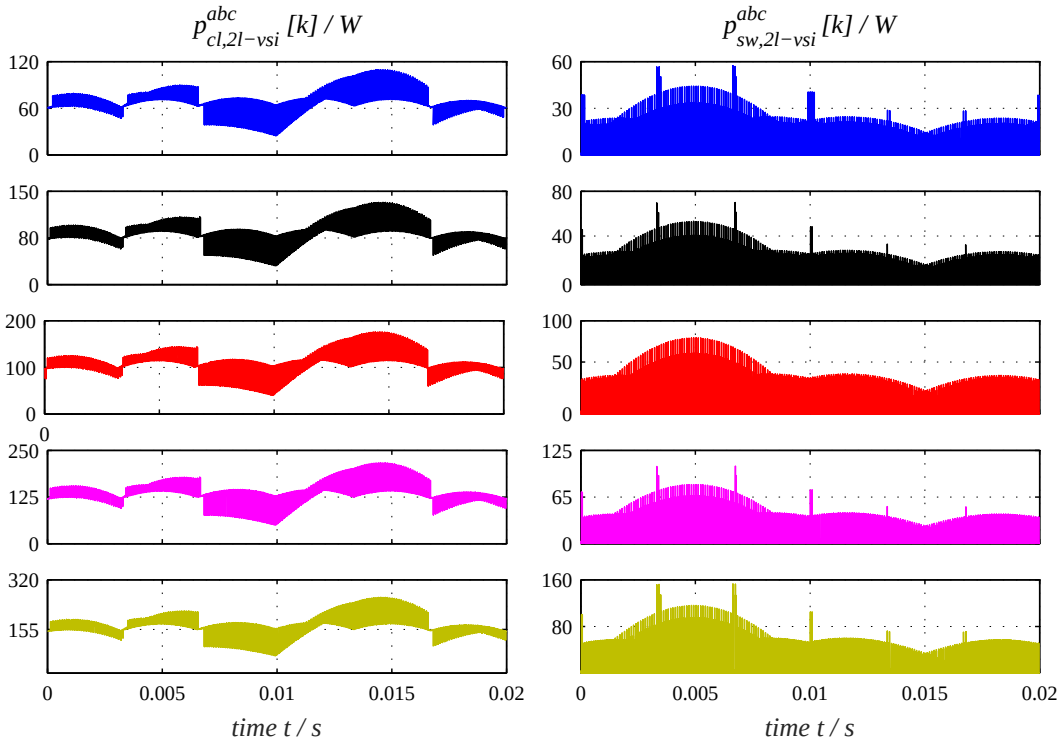

Fig. 4: *Conduction losses (left) and switching losses (right) of a 2L-VSI for different modulation indices* M_{ind} *(from top to bottom):* $M_{\text{ind}} = 0.5$*,* $M_{\text{ind}} = 0.6$*,* $M_{\text{ind}} = 0.7$*,* $M_{\text{ind}} = 0.8$ *and* $M_{\text{ind}} = 0.9$*, respectively.*

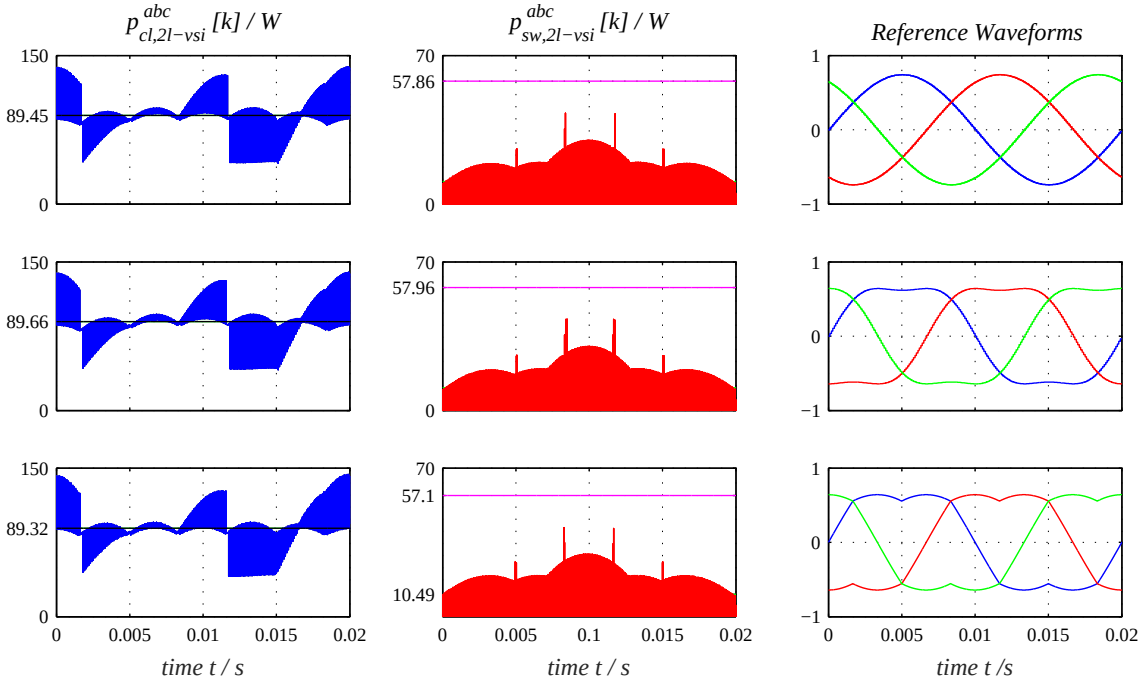

Fig. 5: *Conduction losses (left) and switching losses (middle) of a 2L-VSI for different modulation schemes (from top to bottom): SPWM, THIPWM and SVPWM with normalized reference waveforms (right), respectively.*