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32-channel time-correlated-single-photon-counting system for high-throughput lifetime imaging

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Time-Correlated Single Photon Counting (TCSPC) is a very efficient technique for measuring weak and fast optical signals, but it is mainly limited by the relatively "long" measurement time. Multichannel systems have been developed in recent years aiming to overcome this limitation by managing several detectors or TCSPC devices in parallel. Nevertheless, if we look at state-of-the-art systems, there is still a strong trade-off between the parallelism level and performance: the higher the number of channels, the poorer the performance. In 2013, we presented a complete and compact 32×1 TCSPC system, composed of an array of 32 single-photon avalanche diodes connected to 32 time-to-amplitude converters, which showed that it was possible to overcome the existing trade-off. In this paper, we present an evolution of the previous work that is conceived for high-throughput fluorescence lifetime imaging microscopy. This application can be addressed by the new system thanks to a centralized logic, fast data management and an interface to a microscope. The new conceived hardware structure is presented, as well as the firmware developed to manage the operation of the module. Finally, preliminary results, obtained from the practical application of the technology, are shown to validate the developed system. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4986049]

I. INTRODUCTION

Today, the ability of measuring faint and fast optical signals is a fundamental requirement for many different applications from life science, where dealing with *in vivo* analyses leads to the employment of non-invasive light measurements, to metrology, and to quantum communication.[1–3]

Among all the employed techniques, Time-Correlated Single Photon Counting (TCSPC)[4] is one of the most effective, due to its very high sensitivity and timing precision, which make it outperform traditional "analog" techniques. However, the main drawback of TCSPC is related to its long acquisition time, since the measurement has to be repeated many times until the statistics of the arrival time for the photons can be correctly reconstructed. This issue is even more crucial when acquiring an image, since it limits the scanning speed. To deal with this limitation, multichannel TCSPC systems have been developed in the past years, which are able to manage an increasing number of parallel detectors, aiming to reduce the overall acquisition time.

Nevertheless, if we look at state-of-the-art TCSPC systems, both reported in the literature and commercially available, a strong trade-off between level of parallelism and performance is noticeable: the higher the number of channels, the poorer the performance.[5–10] Even though multichannel systems have significantly increased the number of managed detectors up to several thousand, the count rate capability has not increased accordingly, and data management and download are still the main bottlenecks.

However, a few systems[11,12] have been developed aiming to break existing trade-off, increasing the number of detectors without impairing the performance.

The work done by Cuccato *et al.*[12] represents one of those systems. The module consists of a detection head, containing a 32×1 single-photon avalanche diode (SPAD) array designed with custom technology, connected to a TCSPC module, to time the arrival of each photon. The detectors have a 50-μm diameter and a 250-μm pitch. Regarding the dark count rate (DCR), more than 90% of the devices feature a DCR lower than 20 kcps at 25 °C. The TCSPC module had been designed using a scalable approach in order to be easily expanded to manage a higher number of detectors. The core of the module consists of four eight-channel TCSPC boards working in parallel, described in detail elsewhere.[13] Each board hosts two arrays of four Time-to-Amplitude Converters (TACs) connected to an array of eight high-performance 14-bit Analog-to-Digital Converters (ADCs). The on-board Field Programmable Gate Array (FPGA) handles histogram creation, managing the TACs' operation, reading ADC conversions and implementing the dithering technique. Each TAC has four selectable full-scale ranges (12.5 ns, 25 ns, 50 ns, and 100 ns) and the timing precision is lower than 63 ps FWHM, mainly limited by the jitter of the detector. The TCSPC module contains four eight-channel TCSPC boards working in parallel, to manage signals coming from the 32×1 SPAD array. An interface board connects the TCSPC boards to the detection head, routing the timing signals that are used to start the TACs' conversion, and to the Control Unit (CU) board, routing the Universal Serial Bus (USB)

differential lines to a USB HUB. The last one is used by the Personal Computer (PC) to sequentially communicate with the TCSPC boards in order to start/stop the measurement.

It had been developed as a proof of concept, to demonstrate that an increase in both performance and level of parallelism was feasible.

Since it is a proof of concept, this system presents also some significant limitations which make it unsuitable for imaging applications.

First of all, it does not feature a centralized management of the 32 TCSPC acquisition chains, and the host PC communicates with each individual TCSPC channel, in order to start/stop the measurement and download the recorded data. Since the TCSPC chains have to be accessed sequentially by the host PC, and since USB latency is unavoidable, this system cannot achieve a real-time synchronization of the overall acquisition, which is a crucial aspect for imaging applications.

A second limitation is that the system has not been conceived for scanning applications. It does not feature an interface for managing a microscope; therefore, it cannot acquire and manage synchronism signals coming from a scanning mirror stage. The two issues are interconnected, as a centralized logic able to communicate in parallel with the independent TCSPC boards is needed in order for the system to interface with a microscope.

Finally, the last problem is related to data management, which is a strong and unavoidable issue that all multichannel systems have to deal with when performing scanning. The main bottleneck of Cuccato's work is the limited bandwidth of the USB 2.0 connection, which poses a significant limitation in its employment for fast scanning applications.

Considering all these limitations, we decided to re-design the system, to move from a proof of concept to a high-performance TCSPC system suited for scanning applications.

In this paper, we presented the re-design of the 32×1 system. In Sec. II, the main hardware structure and the modifications are presented. In Sec. III, the developed firmware is described. In Sec. IV, experimental results achieved with the new system are presented. Finally, in Sec. V, conclusions are drawn.

II. HARDWARE STRUCTURE

A. Overall structure

In order for a system to be suitable for TCSPC scanning applications, several requirements have to be fulfilled. First it has to manage synchronization signals coming from the scanning stage of different microscopes. That means it should be able to interface with a microscope, decoding the signals sent by the scanning stage or providing it with the properly phased signals. On the other hand, it should be able to manage the acquisition, synchronously gating it when the scanning stage performs a carriage return and sorting the recorded photons into the corresponding pixels to build the image.

Second, it has to centrally manage the operation of the different TCSPC channels, making them work synchronously in parallel.

Finally, it has to manage the high amount of data to be transferred both inside the TCSPC module and towards the host PC. Two possible approaches for dealing with data management are (i) on-board frame histogram creation and (ii) time-tag operating mode. The first solution implies that the histograms for photon arrival times are built on-board and downloaded to the host PC at the end of each frame acquisition, whereas in the second case, the arrival time and the address of the triggered detector are recorded and directly downloaded to the host PC for each photon. The first solution is suitable for single acquisitions, not for scanning, since the memory download-and-erase time would limit the minimum frame time. On the other hand, in the time-tag mode, the maximum throughput affordable by the PC directly limits the maximum count rate, but it does not pose a limitation on the minimum frame time. For this reason, we decided to target the time-tag mode in the design of the new system.

B. New control unit

We completely re-designed the control unit, moving from a simple passive-HUB structure to a centralized-logic architecture, which makes the system suitable for TCSPC scanning applications that could not be addressed before. In Fig. 1, the structure of the new control unit is depicted.

A Spartan 6 FPGA by Xilinx is the central logic of the TCSPC system. It has to communicate with the four TCSPC boards in order to start/stop the acquisition and to download the recorded photons.

In order to fully exploit the conversion speed of the TAC, which can be connected to detectors counting up to 4 Mcps, data transfer from the TCSPC boards to the central FPGA has to be carefully designed. Considering the TACs operating at 4 Mcps, 14-bit conversions, 5-bit detector's address, each TCSPC board generates a throughput of 608 Mbits/s; therefore, the central FPGA has to manage an overall throughput up to 2.4 Gbits/s, in order not to limit the count rate. To fulfill such a large band requirement, we decided to employ the FPGA's GTP transceivers along with the 1.2 Gbits/s Aurora 8b/10b protocol by Xilinx for each connection. The designed Aurora lanes prevent the link between the CU and the TCSPC boards from limiting the count rate, but the central FPGA has

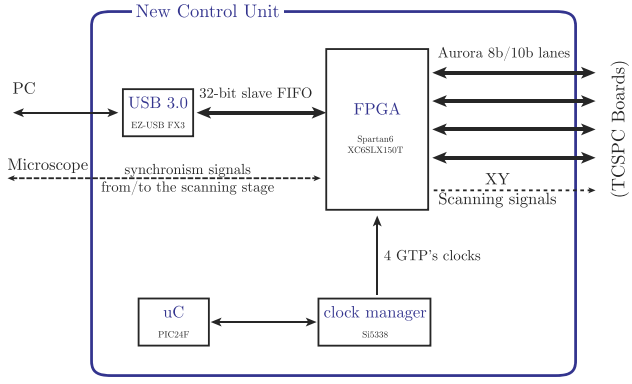

FIG. 1. Structure of the new control unit. Measurements done by the TCSPC boards are downloaded into the CU by means of four 1.2 Gbits/s 8b/10b Aurora lanes by Xilinx. The control unit collects recorded photons from an entire pixel and sends them to the PC through a USB 3.0 connection.

to properly deal with such a high throughput when managing the acquisition of the frame, sorting photons recorded in different pixels, and managing the communication with the host PC.

In order to not limit the count rate of the system, also the data transfer towards the host PC has to be taken into account. For this, a USB 3.0 connection has been chosen since it outperforms USB 2.0 and it is widely available. An EZ-USB FX3 device by Cypress manages the communication to the PC, handling the USB protocol, and communicates to the FPGA by means of a 32-bit parallel interface, called slave first-in-first-out (FIFO).

The central FPGA is also in charge of interfacing with a microscope, acquiring the synchronization signals provided by it, or directly driving the scanning stage. The central FPGA generates the properly phased signals to synchronize the operation of TCSPC boards with respect to each other and to synchronize the TCSPC measurement with the moving of the scanning mirror. Finally, a microcontroller manages the power-up of the system and configures a programmable clock generator which provides the FPGA's transceiver with the clock required for implementing the four 1.2 Gbits/s Aurora 8b/10b links.

III. FIRMWARE

Firmware has been developed for both the TCSPC boards and the control unit. The former ones have to perform the TCSPC measurement, timing photons synchronously with the scanning of the microscope, whereas the latter one has to collect all recorded photons and send them to the PC.

The main requirement was to perform a 256 × 256 scan image, with a pixel dwell time of 4 μs, 12-bit time resolution, and a maximum count rate of 4 Mcps/detector.

One issue that has to be faced when designing the system is the required throughput. Considering our application's requirements, if each photon were tagged with the 5-bit detector address, the data throughput toward the host PC would be 272 MB/s. All the generated data have to be collected by the PC and either stored onto a disk or processed in real-time. Managing such a high throughput is feasible but not trivial. For this reason, we decided to move to a different approach. Since the maximum required count rate is 4 Mcps and the pixel dwell time is 4 μs, a maximum of 16 photons can be recorded per detector per pixel (i.e., in a pixel dwell time). We decided to download a fixed number of events per detector per pixel, and this number has been set to 16. If the number of actual recorded photons by a detector is less than 16, additional fake photons are created for padding. Those padding photons are time-tagged with the longest time delay (0xFFF), which therefore cannot be employed for real conversions, and then discarded by the processing software. In this way, having a fixed number of events per detector, we can avoid tagging the address of the fired detector, since it can be inferred by the photon position inside downloaded data, i.e., the first 16 events will always be related to detector #1, the second ones to detector #2, and so on. If the 5-bit detector address is not carried out, the throughput to the host PC is 192 MB/s, which is 30% less than the previous one.

The main drawbacks of this approach are twofold. First, if the average number of actual recorded photons per pixel is less than 16, the throughput is higher than what is needed and therefore there is a waste in band communication. This happens for a detector rate less than 2.8 Mcps. If this were the case, the firmware could be easily modified to tag each photon with the corresponding detector's 5-bit address. Even if there is a lack of efficiency in the transmission for count rates less than 2.8 Mcps, it is worth noting that sending a fixed-dimension packet, independent of the count-rate, makes the transmission protocol and software post-processing simpler. The second limitation is that the 16-photon limit can cause a saturation of the acquired image. This is likely to be the case if the pixel scan time is greater than 4 μs. The limitation can be easily overcome by increasing the number of pixels per line and performing a pixel-binning in software post-processing. For instance, if the pixel dwell time is 8 μs, we can subdivide the line in 512 pixels (4 μs dwell time) instead of just 256. The acquired pixels are then binned two by two. At the end, the total number of effective pixels is again 256, but this time the equivalent threshold for the number of recorded photon is 32.

A. TCSPC board firmware

In Fig. 2, a block scheme of the TCSPC-board main FPGA's firmware is illustrated.

The main tasks that the developed firmware accomplishes are three: acquisition management, pixel handling, and data transmission.

As soon as the TAC asserts a STROBE, signaling that a valid conversion has been performed, the FPGA samples the corresponding ADC output, issues a reset to the TAC, compensates the sliding-scale dithering, and sets the bin size. The high-performance on-board ADC features a 14-bit resolution,[13] but the target application requires only 12 bits. We decided to let the user decide the bin size, i.e., which 12-bit subgroup to download per each ADC conversion. If the bin size is preserved, the 12 less significant bits are downloaded; if the bin size is doubled, bits from 12 to 1 are downloaded, whereas if the bin size is quadrupled, the 12 most significant bits are downloaded. The recorded photons are then saved into a First-In-First-Out (FIFO) memory, called channel FIFO. Inside the acquisition pipeline, also the number of recorded events is updated, to stop the recording process as soon as the 16-photon limit has been reached. The number of actual recorded events per pixel is also saved in a register to perform the padding.

Each TCSPC board employs two scanning signals coming from the control unit to synchronize the acquisition with the motion of the microscope's scanning mirrors. The first signal is the pixel clock, which times the photon recordings into pixels. The second one is an enable signal, which is used for gating the acquisition when the scanning mirror ends a line and performs a carriage return. The system is designed either to receive the synchronization signals from the microscope or to directly drive the scanning stage. In the target application, the microscope was the master of the scanning procedure.

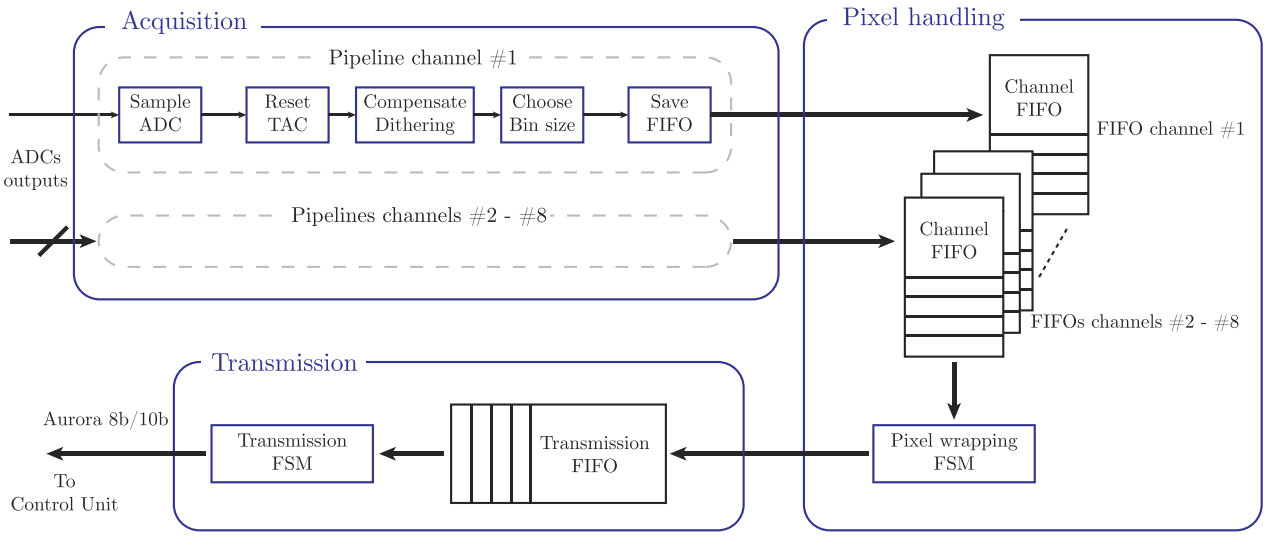

FIG. 2. Schematic representation of the firmware developed for the four eight-channel TCSPC boards. The firmware accomplishes three main tasks: acquisition management, pixel handling, and data transmission to the CU.

The second task performed by the TCSPC firmware is pixel handling. A Finite-State-Machine (FSM), called pixel wrapping FSM, is triggered by the pixel clock and groups all photons recorded during the previous pixel period. The FPGA downloads photons from each channel FIFO sequentially and saves them into another FIFO, called transmission FIFO. Before reading the channel FIFOs, the pixel wrapping FSM reads the content of the registers in which the actual number of recorded photons is saved, in order to download the effective number of events and perform the padding if necessary.

Finally, the transmission FSM manages the download to the control unit by means of the 1.2 Gbits/s Aurora 8b/10b lane.

B. Control unit firmware

In Fig. 3, the block scheme of the control unit FPGA's firmware is reported.

The main tasks of the developed firmware are threefold. First it has to collect recorded photons coming from the TCSPC boards, group them into corresponding pixels, and send them to the FX3. Second, it has to receive commands from the PC, decode them, and send them to the TCSPC boards. Third, it has to receive/send synchronization signals from/to the microscope and manage the generation of the synchronization signals for the TCSPC boards.

Photons recorded by each TCSPC board are stored in a FIFO called buffer 1 FIFO. As soon as an entire pixel is stored in this memory, the channel sorting FSM reads it, re-arranges the order of photons, and saves them into a second FIFO, called buffer 2 FIFO. The reason for the sorting is that the detector address its different from the TCSPC chain address due to challenges in Printed Circuit Board (PCB) layout, i.e., SPAD #1 is not routed to the first TAC of board #1. If a sorting is not done, the order of the recorded photons will not reflect the detector order. This is not an issue if the counts of different detectors are summed up, as in the case of the fluorescence lifetime imaging microscopy (FLIM) image reported in Fig. 6, but it is crucial if the photons recorded by different detectors have to be kept separated as in the case of spectrally resolved imaging, where each detector of the linear array is used to acquire a different wavelength. Obviously the sorting can be done in software, but we decided to implement it in firmware to simply the post processing done by the end user. For this, two different sortings have to be accomplished: the first one at single-board level, rearranging the channel order inside a single board, which is done by the channel sorting FSM, and the second one at the overall-board level, rearranging the board order, which is done by the pixel wrapping FSM. This FSM reads the buffer 2 FIFOs as soon as they contain all the photons recorded in a same pixel, performs the overall-board-level sorting, and saves them into the FX3 FIFO. If the FX3 FIFO has not enough space to store an entire pixel, all the photons are discarded. In this way, the download alignment is preserved, since it relies on the fact that a fixed number of photons have to be downloaded per each pixel. The pixel wrapping FSM adds a control word at the beginning of each pixel in which the pixel number and some error flags are stored. The PC software can therefore sort photons and reconstruct the image based on the pixel number reported by the control word. It is worth noting that if the PC exhibits latency, the FX3 FIFO saturates, and therefore some pixels can be lost. Some tests have been done acquiring several consecutive frames and most of them were intact. If a frame presents some missing pixels, even if typically less than 1% of the total, it is discarded by the acquisition software. Finally, the FX3 handling FSM manages the communication from/to the FX3 device, sending the recorded photons and saving the incoming commands.

The decoding FSM decodes the incoming commands, which are then sent to the TCSPC boards too, by means of the Aurora 8b/10b lanes, managed by the transmission FSM. As for the management of the scanning procedure, a synchronization FSM handles all the alignment process, and it is able both to send the driving signals to the scanning mirror stage of the microscope and to receive and process them.

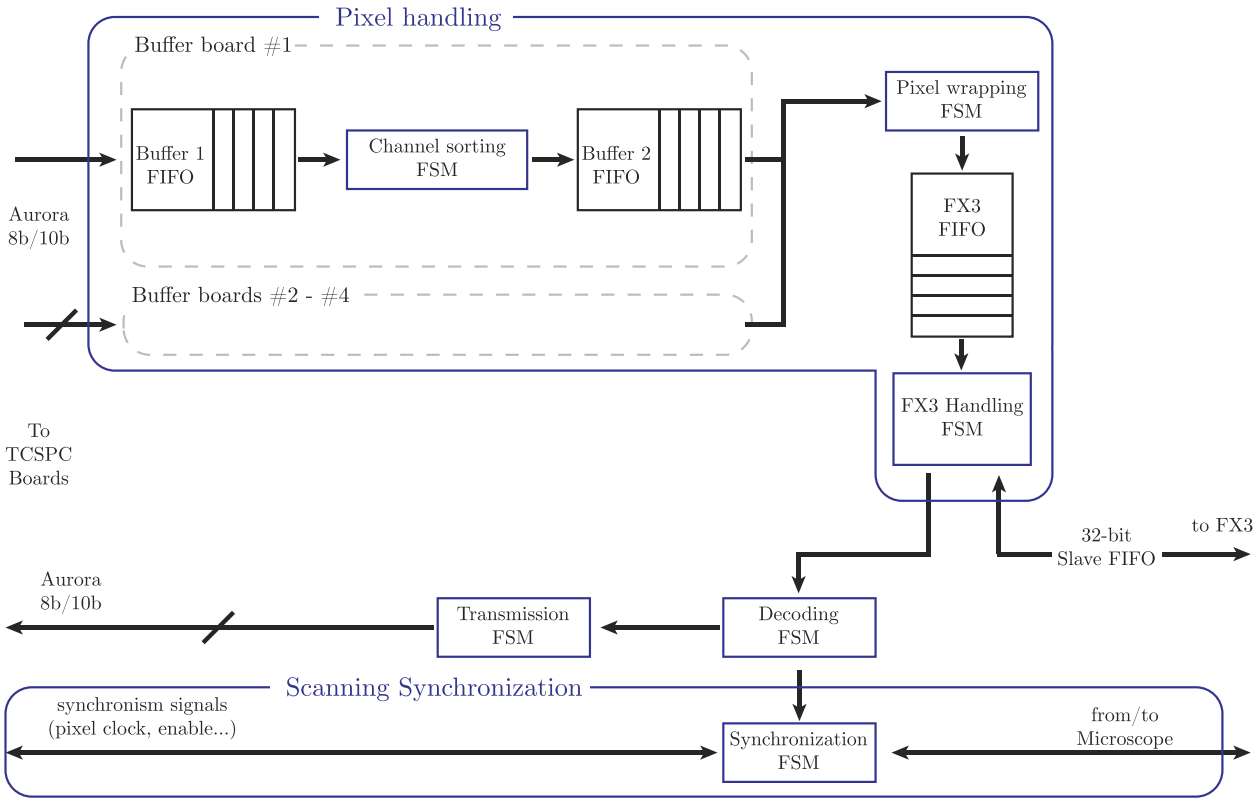

FIG. 3. Block scheme of the control unit firmware. The main tasks of the CU firmware are pixel handling, i.e., group the recorded photons into corresponding pixels, download data to the PC, receive and decode commands from the PC, and manage the synchronism signals for the scanning.

Regarding the targeted application, the microscope (a TCS SP8-X from Leica) is the master of the scanning procedure and it continuously scan 256 lines of the sample, each one composed by 256 pixels. The microscope has its own trigger box which generates the synchronization signals for the acquisition logic. These signals are essentially two: *line_active* and *frame_active*, whose active levels signal that the microscope is scanning a line and a frame, respectively (see Fig. 4).

The synchronization FSM captures those signals and generates 256 pixel-clock periods per each line, based on the pixel period duration selected by the user. A replica of the *line_active* is also generated (*enable_scan*) as an enable signal to gate the acquisition as soon as the scanning stage ends the line and performs a carriage return. Due to mechanical tolerances, the *line_active* signal could be not perfectly aligned with respect to the scanner position. Therefore, the acquired image would be off-centered and present a shift between adjacent lines if the bidirectional scanning mode is performed. Moreover, the lifetime image would be off-centered also with respect to the intensity image acquired by the microscope's internal detectors. To solve this issue, the synchronization FSM lets the user configure a fixed delay between the generated enable signal and the first pixel-clock edge of the line (Td in Fig. 4).

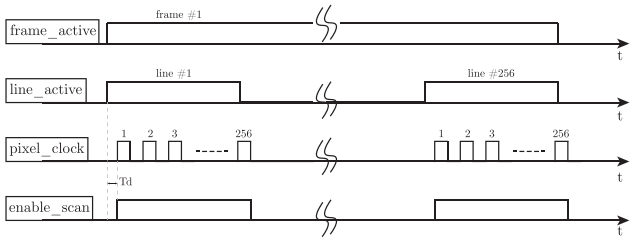

FIG. 4. Synchronization signals used during a scanning. *Frame_active* and *line_active* are output by the microscope and they are high when the laser is scanning a line and a frame, respectively. *Pixel_clock* and *enable_scan* are generated by the FPGA. The former is used to divide the acquisition into pixels and it is delayed by a finite time Td with respect to the *line_active* signal. The latter is synchronous with the pixel clock and it is a delayed replica of the *line_active* signal that is used by the TCSPC boards to gate the acquisition when the laser is performing a carriage return.

IV. EXPERIMENTAL RESULTS

The main goal of the project was to build a prototype that would be able to use fluorescence lifetime measurements to distinguish various stages of aggregation of alpha synuclein (aSyn) in cells. aSyn is a small, natively unstructured protein that can aggregate into insoluble structures that are toxic to neurons, a phenomenon closely linked to the pathology of Parkinson's disease.[14] Our system should enable the direct measurement of the efficacy of aggregation-inhibiting drugs. The developed system was tested at the Institute for Biomedicine (Eurac Research—Bolzano) to validate the design and prove its suitability for scanning applications.

The system was connected to a TCS SP8-X confocal laser scanning microscope from Leica. The 32 SPADs were used as one single detector by collecting the light coming from the same spot and grouping together the corresponding timing

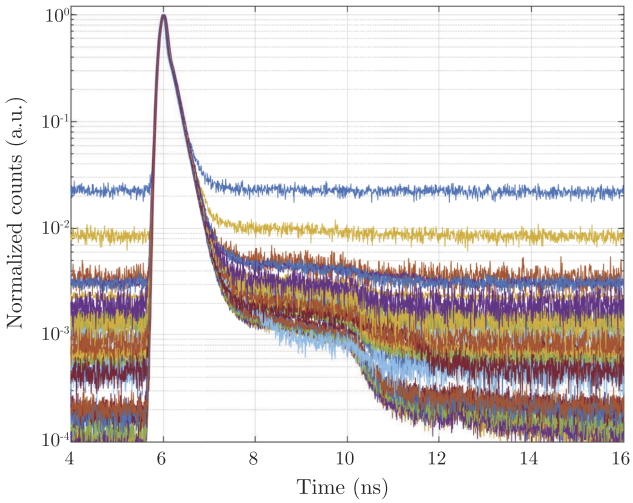

FIG. 5. IRFs of the 32 channels after compensating mismatches with the calibration procedure. The different SNR are due to variations in the detectors' dark count rates and to the non-uniform distribution of the light. The bump that is visible at 10 ns is due to optical cross talk, i.e., avalanches triggered by the secondary emission of photons of adjacent detectors.[16]

measurements to increase the count rate and therefore reduce the measurement time. In order to gather measurements done with different channels (SPAD + TAC), a calibration procedure is mandatory to compensate for mismatches, i.e., offsets and mean bin widths of the TCSPC chains are slightly different. We employed an offline calibration, done by software on the recorded events, based on the algorithm proposed by Peronio *et al.*[15]

We tested the validity of the calibration procedure by acquiring the instrument response function (IRF) of the system for all the 32 detectors. The laser source integrated in the SP8-X is a supercontinuum laser by NKT that was tuned at 488 nm with a repetition rate of 40 MHz and the full-scale range of the TACs was set to 25 ns accordingly. In Fig. 5, the 32 measured IRF are reported after being calibrated. As it can be seen, the alignment is good, i.e., the maximum shift among the peaks is less than the 63-ps jitter of the detectors; therefore, measurements performed with different channels can be effectively grouped together without significantly impairing the performance.

In order for the detectors to collect the light coming from the same spot, a proper beam shaping optical system has been used. The light coming from the pinhole of the microscope was focused onto the array by means of a cascade of four lenses: the first lens was used to collimate the divergent beam; the second and the third ones were coupled and used as a beam expander to make the section of the beam fit the linear dimension of the array; the last one is a cylindrical lens and it was used to focus the beam down to a dimension of ~50 μm only in one axis, to fit the dimension of the detector. It is worth noting that even if the fill factor of the linear array is limited to 16.11%, there is still a reduction in the measurement time by using 32 detectors in parallel. Moreover, the module has been conceived to work in conjunction with a microlens array, i.e., the pixel pitch has been set to 250 μm, to match a typical pitch of commercial lenses, which can increase the fill factor to 80%.

A Convallaria test sample from Leica was also imaged to characterize the system. The light impinging on the sample was filtered with the built-in acousto-optical tunable filter (AOTF) of the microscope selecting the 488-nm wavelength. The fluorescence light was directed through a pinhole, filtered with a 488-nm notch filter to remove residual laser light, and then focused onto the detector array.

Figure 6 shows 256 × 256 images obtained from the test sample. Both the intensity image (a) and the FLIM image (b), obtained after processing the acquired histograms with the FLIMfit software, are shown. Ninety frames were acquired and summed with a scan rate of 1 frame/s, which corresponds to a pixel dwell time of about 4 μs. The actual total dwell time was much less than 90 s (about 22 s) since the scanner spent most of the time in carriage returns; therefore, the mean download rate was also reduced by a factor of ~4, i.e., 50 MB/s, but the peak rate was about 192 MB/s, as expected. In this particular case, a slower scan could be performed instead of superimposing 90 frames, but in general our target was the possibility of resolving and analyzing different frames, in order to be able to study a temporal evolution of the sample conditions. In Table I, a summary of both the theoretical and the effective throughput is reported. Finally, two main lifetimes are visible in the sample: the first around 600 ps, whereas the second is around 2.3 ns.

In Fig. 7, two histograms are reported with the corresponding measured IRFs. Those histograms have been acquired in the two areas highlighted in Fig. 6(b) (white circles). A binning of 4 × 4 pixels has been performed.

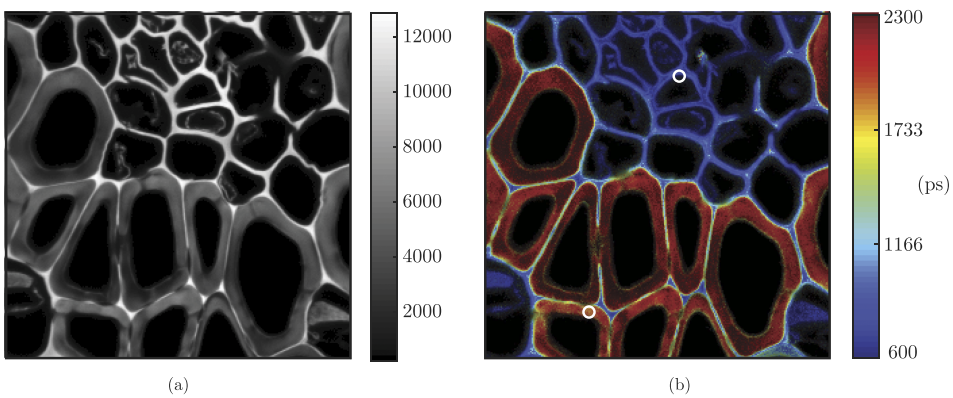

FIG. 6. (a) Intensity image, (b) FLIM image. Two main lifetimes are visible in the FLIM image: the first around 600 ps and the second around 2.3 ns.

TABLE I. Summary table of the throughput.

Pixel dwell time	4 μs
Image size	256 × 256
Theoretical frame rate (no carriage return)	4 frame/s
Theoretical throughput (no carriage return)	192 MB/s
Effective frame rate	1 frame/s
Effective average throughput	50 MB/s
Effective peak throughput	192 MB/s

Finally, in Fig. 8, to demonstrate the effectiveness of the system, a plot of the number of frames needed to acquire 1000 photons/pixel as a function of the number of detectors used in parallel is reported. The threshold of 1000 photons has been chosen to estimate the lifetime with an accuracy of few percent.[17] The blue line represents the actual scenario and it has been obtained with the following procedure. First, we selected a particular pixel of the image reported in Fig. 6(b) and extracted the average number of photons recorded per frame in that pixel by each detector. Then, we calculated how many frames were necessary to accumulate 1000 photons if (i) only SPAD #1 were used, (ii) SPAD #1 and #2 were used, (iii) and so on. The red line represents the ideal case, with the number of frames inversely proportional to the number of detectors working in parallel. In this case, we used the average number of counts recorded per frame by SPAD #1 to calculate the number of frames needed using only one detector. The other points of the plot were drawn by decreasing the number of frames proportionally with the number of detectors employed. The difference between the two curves is due to the fact that the light was not uniformly distributed over the SPAD array, and indeed the detector's count rate was higher in the central region and decreased moving towards the edges. As it can be seen, the system effectively reduces the measurement time. In this case, there is a reduction by a factor of 17, which can be further improved towards the limit of 32 by using better optics and a microlens array. It is worth noting that the effective increase in the recorded efficiency has been obtained by increasing the level of parallelism of both the detector and the timing electronics. For instance, the same gain is not

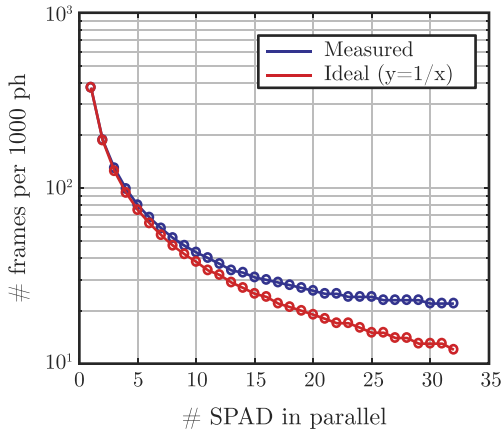

FIG. 8. Number of frames needed to acquire 1000 photons as a function of the number of detectors used in parallel. The blue line represents the actual scenario, whereas the red line represents the ideal scenario where the number of frames is inversely proportional to the number of detectors working in parallel.

achievable by only employing a SPAD with an area 17 times bigger. Indeed, the bigger SPAD would collect 17 times more photons, but the recorded number of events would not increase accordingly due to the finite dead time of both the detector and acquisition logic. Moreover, the count rate of the single detector has to be limited to avoid classic pile-up.

On the other hand, even a 17 times faster laser cannot increase the number of photons in the same way, since the recorded rate would be limited by the dead time also in this case. Moreover, a 17 times faster laser would also have a 17 times shorter period, which is too short for detecting a lifetime of few nanoseconds.

Conversely, an effective increase in the count rate can be obtained by increasing the parallelism level of the system in order to either strongly reduce the dead time[18] or manage several independent acquisition chains.[19] It is worth noting that both these last two solutions have been developed exploiting the CMOS technology to increase the level of integration, but they do not match the best state-of-the-art performance from neither the detector nor the timing electronics.

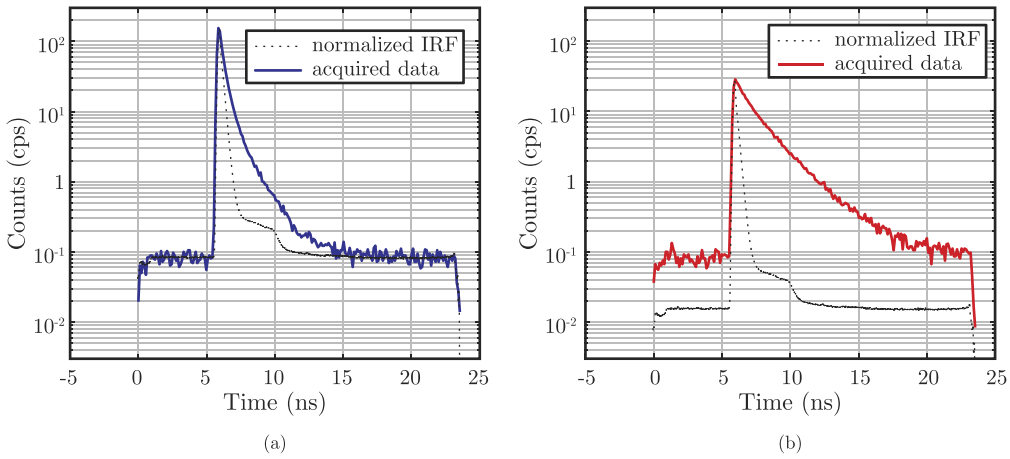

FIG. 7. Acquired histograms and normalized IRF for two different areas of the sample: (a) with a mean lifetime around 600 ps, (b) with a mean lifetime around 2 ns.

V. CONCLUSIONS

In this paper, we present the re-design of a 32×1 complete TCSPC module. The new module was developed specifically targeting scanning applications, which could not be addressed with a previously developed version, mainly due to a lack of a centralized architecture. The main goal of this work was to move from a proof of concept towards a system that could be effectively integrated in an imaging setup.

Preliminary tests with biological samples have been carried out at the Institute for Biomedicine at Eurac Research, and the results have validated the new system, which can therefore be routinely employed in life science scanning applications.

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