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INVESTIGATION OF SUPERCONDUCTING FAULT CURRENT LIMITER APPLICATION IN A POWER-DENSE MARINE ELECTRICAL NETWORK

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Abstract

Power-dense, low-voltage marine electrical systems have the potential for extremely high fault currents. Limitation of fault currents is very attractive in a marine vessel, particularly in terms of switchgear cost, size, and weight, and reducing damage at the point of fault. This study shows that superconducting fault current limiters (SFCLs), even with relatively small impedances, are highly effective at reducing prospective fault currents. For the marine system investigated, various possible SFCL deployment strategies were found to be effective, particularly at the bus-tie location which can limit the fault current to approximately half the unrestricted value with an impedance of 0.1Ω. However, the chosen fault current limitation scheme will depend significantly on the vessel's electrical topology, the fault current contribution of each of the generators, and the properties of the SFCL device.

1 Introduction

Superconducting fault current limiters (SFCLs) have the potential to facilitate the utilisation of highly power-dense, low-voltage electrical systems. This applies particularly to marine electrical systems, in which electrical power requirements for propulsion, auxiliary systems, and other loads are increasing. The necessary generation capacity at a given voltage level may result in fault currents such that procurement of appropriate switchgear is prohibitively expensive, or impossible; furthermore, there are increased safety concerns when fault currents become excessively high. The requirement for limits on voltage levels may be driven by the costs of employing crew with particular operating qualifications. Restriction of fault currents by other means – that do not add operational constraints during non-fault conditions – is therefore very attractive [1].

This paper presents a detailed study of the impact of SFCLs on fault currents in a marine electrical network. The vessel chosen for the case study is an offshore anchor handling/supply vessel with a relatively large installed generation capacity. The effectiveness of limiting fault current using resistive-type SFCLs with various resistance values is examined. Five SFCL location strategies are also compared. Based on the results presented, conclusions as to the effectiveness of SFCLs in this application are drawn, and suggestions for further investigation are made.

2 Case study marine system

The vessel has six synchronous generators supplying an electrical system which may be split to create two electrical subsystems, connected by a bus-tie circuit breaker. The system diagram is shown in Figure 1 which shows that four generators are 2.1MW units while the remaining two generators are of 4MW capacity. The 4MW generators are associated with local propulsion and thruster load, as well as being connected to the main switchboard. As depicted in Figure 1, the system is divided into two similar subsections with loads evenly distributed between them.

The principal loads in the system are motors used for different purposes such as propulsion and thrusters. Auxiliary loads are connected to both the 690V switchboard and to the 230V switchboard.

2.1 Model and analysis method

The electrical system modelling of the case study marine application has been carried out using PSCAD [3]. As is typical of AC marine electrical systems, it is ungrounded and has a nominal frequency of 60Hz. The individual components have been modelled as described below.

Generators: Two types of synchronous generators have been used during the modelling of system. Relevant generator data is provided in the Appendix. The generators' excitation control was implemented based on IEEE standard model AC1A, with parameters as suggested in [2]. A standard governor control system provided in PSCAD has been used to simulate the governor control systems. No authoritative data was available for the generator inertia. However it is believed that the mechanical system reaction time is much larger than electrical time constant; thus, the mechanical inertia will have little impact on fault current studies of the system and to the study of electrical dynamic behaviour of the system.

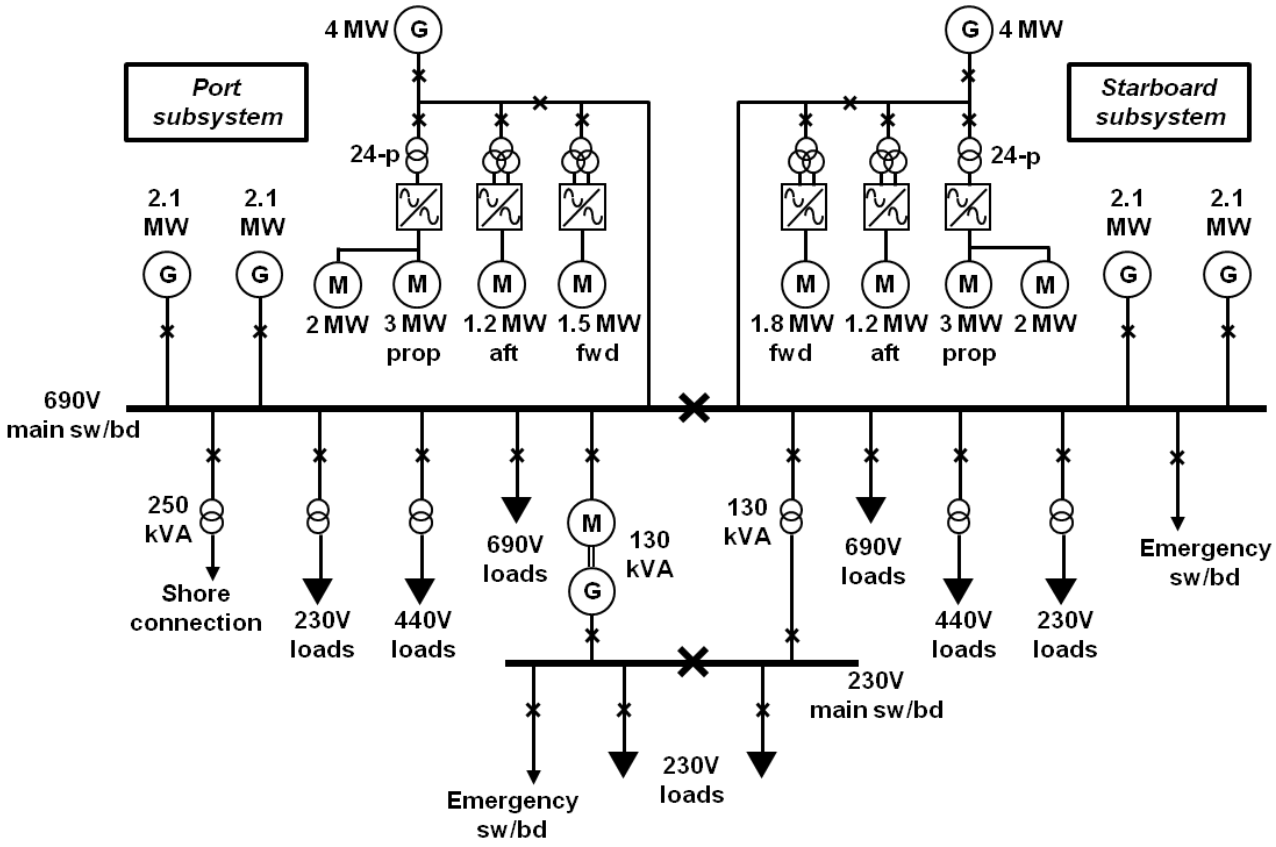

Figure 1: Marine electrical system

Cables: A pi-equivalent model of cables has been used during this investigation, with resistance of 83.9μΩ/m and reactance of 142.5μΩ/m. Cable lengths are illustrated in Figure 2.

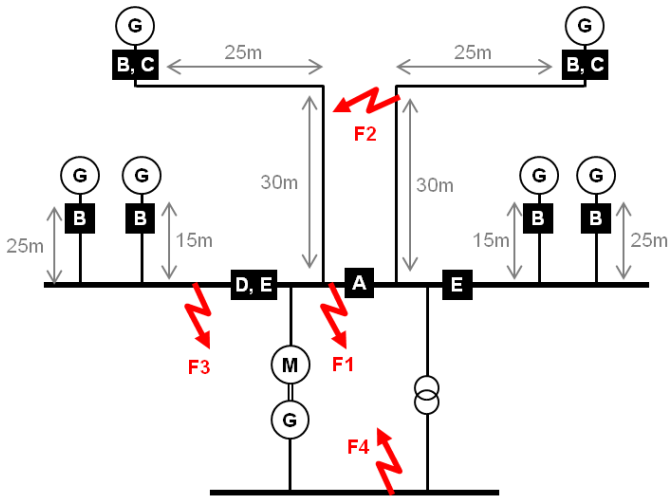

Figure 2: Fault locations, SFCL locations, and cable lengths

Transformer: Standard PSCAD transformer components have been used to model system transformers. The transformer shown in Figure 2 is configured as star-delta (delta on the 230V side), with the star-point ungrounded, and with 0.18pu positive sequence leakage reactance.

Load: Figure 1 shows presence of both static and dynamic loads. However, it can be seen that motors are connected through power electronic converters capable of providing a current control scheme. Therefore, with a current controlled scheme in place, pre- and post-fault currents of the drive systems remain unchanged, i.e., load current is controlled to 1 pu which allows motoring load to be modelled as static load, leading to simplified modelling and shorter simulation time. The motor-generator arrangement is assumed to be disconnected from the system; the 230V loads connected to the main switchboard are supplied via the parallel transformer. This assumption is valid for fault level studies because the motor is convertor-interfaced and would not contribute significantly to the fault current. The emergency generator, emergency switchboard, and shore connection are not considered in this study.

Faults: This paper considers the worst case scenario of three-phase to neutral faults, applied at the locations of interest (shown in Figure 2) with a negligible fault resistance value. Fault currents are calculated using the EMTDC simulation engine. It is assumed that the selected circuit breakers are capable of closing onto and breaking the maximum prospective fault current from one half of the electrical system. For this reason the bus-tie must be open for operation with full generation, unless fault current limitation is present.

SFCL model: A simple look-up table (Table 1) has been used to model a resistive SFCL; intermediate values are linearly

interpolated from the data in the table, as shown in Figure 3. The values are scaled to achieve the desired resistance, and time shifted such that the device operates at the time of the fault. The SFCL develops its full resistance value after 0.02 seconds. The recovery time is not modelled; it is assumed that the SFCL remains resistive during the post-fault period.

Time (seconds)	Resistance (Ω)
0.00	0.001
1.00	0.001
1.001	0.30
1.002	0.57
1.004	0.97
1.005	1.13
1.01	1.62
1.02	2.00
1.20	2.00
5.00	2.00

Table 1: SFCL resistance look-up table

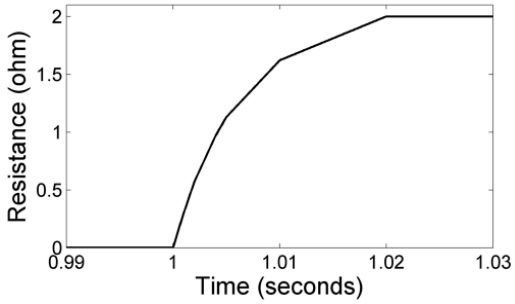

Figure 3: SFCL resistance characteristic

2.2 Fault level analysis

Table 2 lists the fault currents experienced at three different locations, with the bus-tie circuit breaker closed but without fault current limitation. For each location the peak make (first fault current peak after fault occurrence), peak break (third peak), and RMS break (RMS of fifth peak, an approximation of the true RMS break) values are provided.

	Fault current for each fault location (kA)		
	690V bus (fault F1)	Generator feeder (fault F2)	230V bus (fault F4)
Peak make	232.8	142.3	5.208
Peak break	115.08	82.52	5.169
RMS break	66.07	53.30	3.635

Table 2: Prospective fault currents

Figure 4, Figure 5, and Figure 6 illustrate the fault current for faults F1, F2 and F4, respectively. In each case, the fault occurs after 1 second, and is present for 0.1 seconds. For an electrical system with 16.4MW of generation capacity, a prohibitively high fault current is calculated. Fault F1 occurs at a voltage zero-crossing on phase A; hence phase A exhibits the highest peak fault current due to the increased DC component. Other point-on-wave fault times, where the fault does not occur on a voltage zero-crossing on any of the phases, result in a lower peak fault current (close to the manual peak symmetrical short-circuit calculation of 183kA). Fault F3 is not shown because it results in identical fault current as fault F2; however different results are obtained depending on the SFCL location(s), as shown in Section 3.1. The peak contribution is almost the same for each type of generator because the sub-transient reactance of the 2.1MW generator is smaller relative to the 4MW generator (see Appendix); however the RMS break values are lower for the 2.1MW generators. Note that generator feeder fault current (fault F2) is less than the bus-tie fault current (fault F1) due to the cable impedance between the locations which reduces the fault contribution from the four 2.1MW generators.

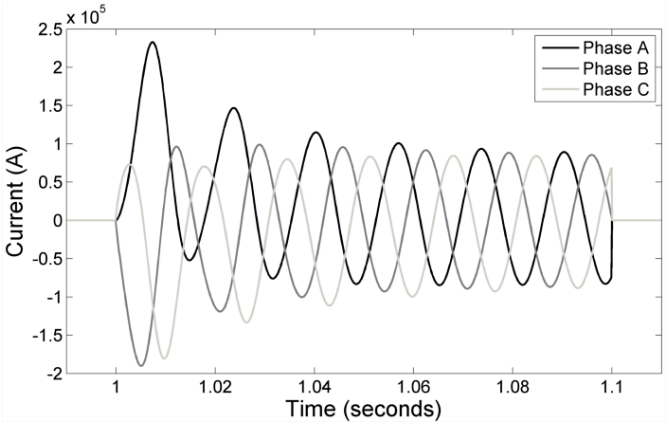

Figure 4: Fault on the 690V bus (F1)

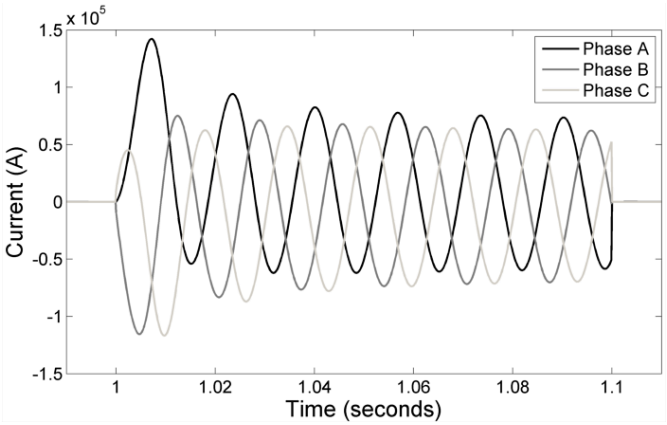

Figure 5: Fault on a 4MW generator feeder (F2)

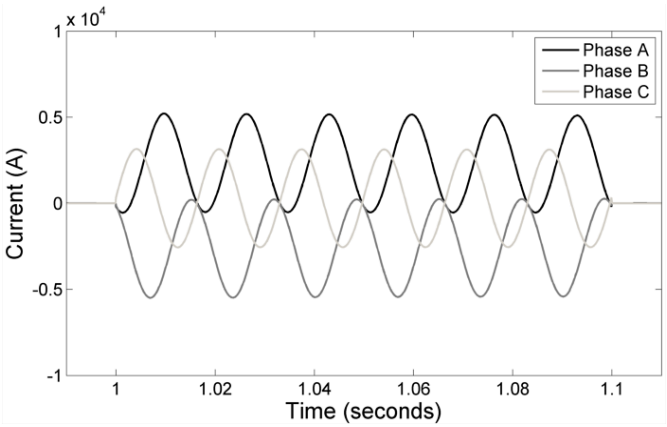

Figure 6: Fault on the 230V main switchboard (F4)

For fault F4, Figure 6 shows that the DC offset decays very slowly, after approximately several seconds, due to the increased X/R ratio caused by the transformer impedance. However, the potential for damage due to short circuits on the 230V distribution system are by comparison significantly lower – due to the additional transformer impedance in the current path – and are therefore not considered further in this paper.

2.3 Voltage and power perturbations

Figure 7 shows the voltage at the 690V bus during fault F1 at (t=1s) and fault F2 (at t=2s). The dips in voltage are clearly apparent. It is evident that the voltage starts recovering soon after faults are cleared. For the same fault conditions, Figure 8 illustrates the disturbance to real and reactive power at the output of the starboard 4MW generator.

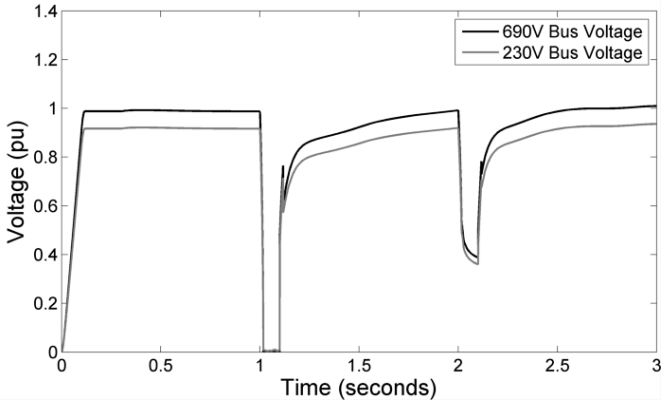

Figure 7: RMS bus voltages during faults at t=1s and t=2s

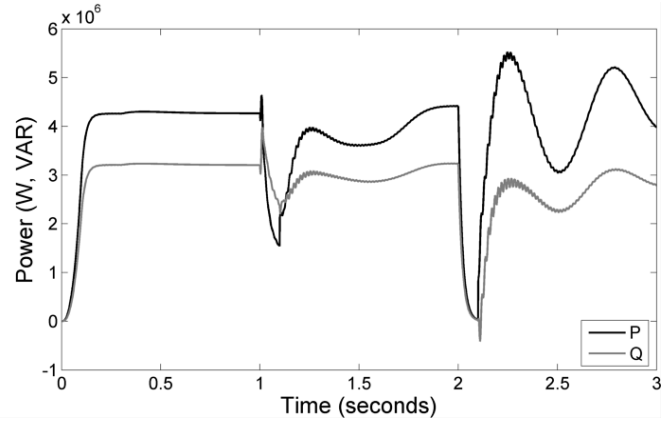

Figure 8: P and Q at the starboard 4MW generator during faults at t=1s and t=2s

3 SFCL deployment analysis

Figure 2 shows the potential SFCL deployment locations (A to E) that are considered in this paper. In particular, location strategy B involves placing SFCLs in series with every generator, whereas strategy C targets just the two 4MW generators.

3.1 Results for each SFCL location strategy

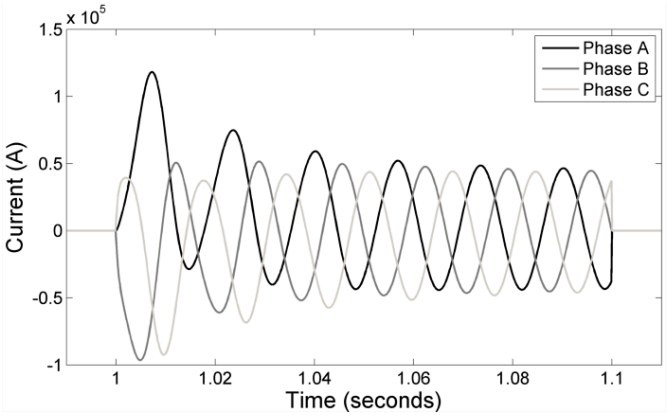

Figure 9: Fault current limitation for fault F1 at location A

Initially, each SFCL location strategy has been tested with an SFCL impedance of 0.2Ω, and a fault at the 690V bus-tie (fault F1). Table 3 compares the results and Figure 9 shows the fault current for location strategy A. By inspection of the system topology, location A has the potential to limit the fault current contribution from one "half" of system, regardless of the fault location. Table 3 confirms that peak make, peak break, and RMS break are all approximately halved, even for a relatively small SFCL resistance value. The main disadvantage of this approach is that a single SFCL device is required to be rated to handle the current caused by the fault, and hence the energy dissipated in the SFCL.

	Fault current for each location strategy (kA)				
	A	**B**	**C**	**D**	**E**
Peak make	118.4	48.02	167.8	159.2	86.82
Peak break	59.27	27.76	82.86	81.04	47.91
RMS break	34.36	19.01	44.54	48.56	31.55

Table 3: Comparison of SFCL location strategies

Location strategy B clearly limits the fault current contribution from all generators (except for faults across a generator's terminals), reducing the fault current to less than 30% of its prospective value. However, this is unlikely to be used in practice because the SFCLs may require post-fault recovery [4], necessitating all generation (except the emergency generator) to be removed from service. In addition, six separate fault current limiters are required.

Strategy C is a compromise of the advantages and disadvantages of strategy B. The result in Table 3 for peak make for this SFCL location strategy is relatively high, because of the relatively large peak make contribution from the 2.1MW generators.

3.2 Effects of different SFCL resistance and fault location

Figure 10, Figure 11, Figure 12 illustrate how SFCL resistance affects the peak make, peak break, and RMS break fault currents, respectively. It can be observed that in most cases, there is only a small reduction in fault current for resistance values greater than approximately 0.1Ω. For

location strategy B and with SFCL resistance greater than approximately 0.25Ω, the peak fault current contribution from each generator is typically below 2pu, relative to load current, and diminishes to less than load current after the first peak. Such severe fault current limitation could potentially lead to use of smaller, lighter, and cheaper switchgear.

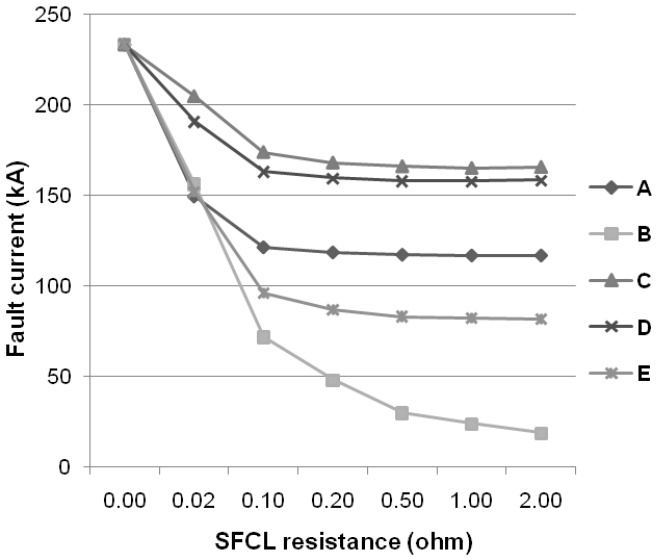

Figure 10: Peak make fault current for fault F1, for each SFCL location strategy

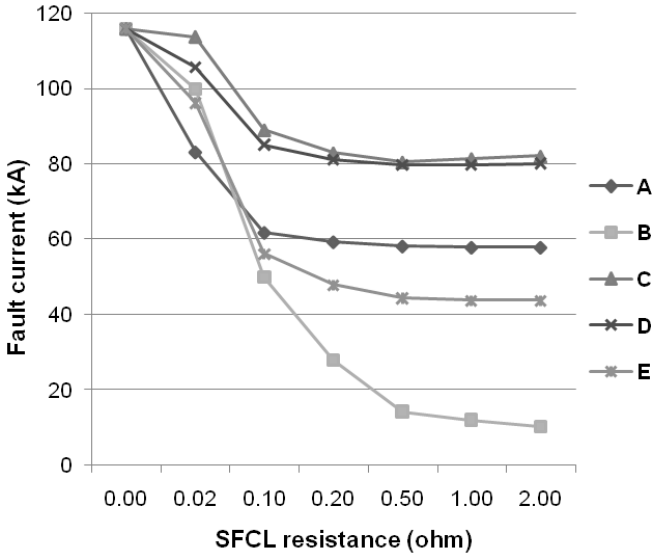

Figure 11: Peak break fault current for fault F1, for each SFCL location strategy

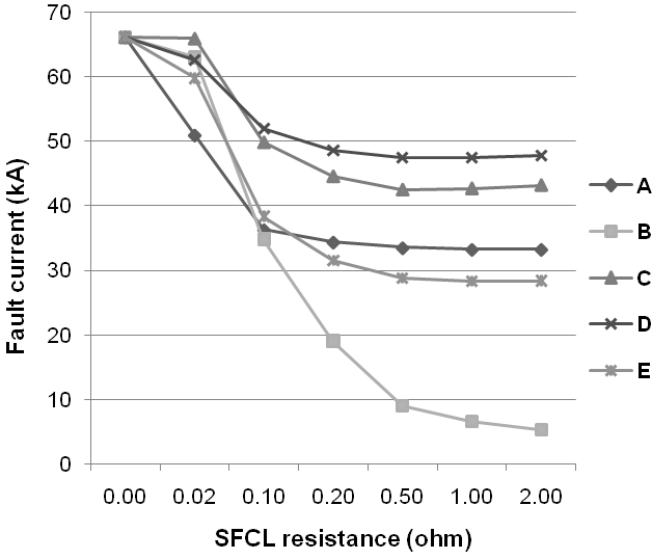

Figure 12: RMS break fault current for fault F1, for each SFCL location strategy

An SFCL at location D does offer very good current limitation for fault F3 for small impedances such as 0.2Ω: 77.78kA, 37.79kA, and 20.38kA (peak make, peak break, and RMS break, respectively). However, this location is "biased" towards faults on a particular side of the system (unlike an SFCL located at the bus-tie), and only limits approximately one third of the prospective fault current for a bus-tie fault (fault F1), as shown in Table 3.

	Fault current for SFCL resistance (kA)						
	0Ω	**0.02Ω**	**0.1Ω**	**0.2Ω**	**0.5Ω**	**1Ω**	**2Ω**
Peak make	232.8	151.5	95.75	86.82	82.92	82.00	81.64
Peak break	115.8	96.21	56.15	47.91	44.44	43.78	43.76
RMS break	66.07	59.75	38.37	31.55	28.78	28.35	28.37

Table 4: Comparison of SFCL resistance at location E, for fault F1

	Fault current for SFCL resistance (kA)						
	0Ω	**0.02Ω**	**0.1Ω**	**0.2Ω**	**0.5Ω**	**1Ω**	**2Ω**
Peak make	142.3	119.7	99.04	93.18	91.80	91.21	90.95
Peak break	82.52	77.83	60.05	53.63	53.08	52.69	51.31
RMS break	53.30	50.57	39.68	34.48	33.77	33.57	32.62

Table 5: Comparison of SFCL resistance at location E, for fault F2

By inspection, location strategy E has the potential to limit approximately half of the steady-state fault current for bus-tie faults. Table 4 shows that an SFCL resistance of approximately 0.2Ω is necessary to achieve this. In the case study system, a resistance of 0.2Ω also reduces the peak fault current by more than half of the unrestricted value due to the relatively small sub-transient reactance of the 2.1MW generators. However, this SFCL deployment strategy does not limit the fault contribution from either of the two 4MW generators, for faults at the bus-tie or one of the 4MW generator feeders (fault F1 or F2). In the latter case, relatively large values of SFCL resistance only trim

approximately one third off the fault current, as shown in Table 5.

3.3 Effects of SFCL on system voltage and power

The simulation in Section 2.3 was repeated to examine the effects an SFCL at location A has on voltage and power. Fault F1 is applied at t=1s, and the bus-tie circuit breaker is opened after approximately 80ms (depending on the individual phase current zero-crossings). This clears the fault from the starboard subsystem, and disconnects the SFCL from the circuit. The port subsystem must open further circuit breakers (at each of its three generator feeders) to clear the fault but this not considered further. The voltage dip and power perturbations are reduced considerably on the operational starboard subsystem, as shown in Figure 13 and Figure 14, respectively. In this situation, the SFCL can safely be bypassed to allow for recovery of the superconductor.

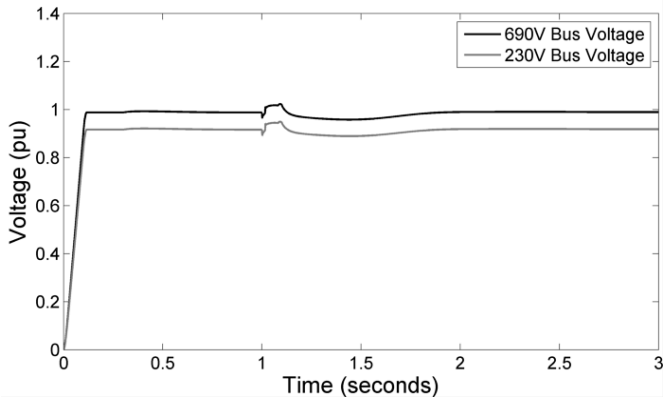

Figure 13: RMS bus voltages for fault F1applied at t=1s, with an SFCL

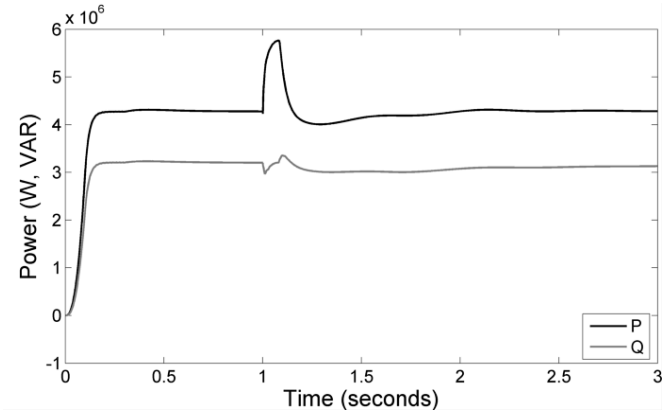

Figure 14: P and Q at the starboard 4MW generator for fault F1 at t=1s, with an SFCL

4 Conclusions

Power-dense, low-voltage marine electrical systems have the potential for extremely high fault currents. This study shows that SFCLs, even with relatively small impedances, are highly effective at reducing prospective fault currents. Severe limitation of fault currents is very attractive in a marine vessel, particularly in terms of: switchgear cost, size and weight; reducing damage at the point of fault; and, in the case study system, allowing the bus-tie to be closed even when all generation is in service. For the marine system investigated, various possible SFCL deployment strategies were found to be effective, particularly the bus-tie location. However, the chosen fault current limitation scheme will depend significantly on the vessel's electrical topology, and the fault current contribution of each of the generators.

Further work is required to select the most suitable deployment strategy from these alternatives, taking into account the physical parameters of the SFCL and its auxiliary equipment, and the corresponding naval architecture constraints of the vessel. Furthermore, investigation of the operational implications of SFCL deployment, such as supply restoration, is required. This should include both operational strategies which are required before and immediately after a fault (because, after operation due to a fault, SFCLs may not immediately be available due to the recovery period) and the requirements of the supporting infrastructure of the SFCL.

5 Appendix: generator model data

	4MW	**2.1MW**
Apparent power	5.4MVA	2.3MVA
Inertia constant	3.17s	3.17s
Armature resistance (Ra)	0.009pu	0.008pu
Xp	0.103pu	0.103pu
Xd	2.0pu	2.2pu
Xd'	0.21pu	0.205pu
Xd''	0.14pu	0.119pu
Xq	2.0pu	2.0pu
Xq''	0.14pu	0.119pu

Acknowledgements

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