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The Design of Re-writeable Ultra-High Density Scanning-Probe Phase-Change Memories

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Abstract— **A systematic design of practicable media suitable for re-writeable, ultra-high density (> 1Tbit/sq.in.), high data rate (> 1Mbit/s/tip) scanning probe phase-change memories is presented. The basic design requirements were met by a Si/TiN/GST/DLC structure, with properly tailored electrical and thermal conductivities. Various alternatives for providing re-writeability were investigated. In the first case amorphous marks were written into a crystalline starting phase and subsequently erased by re-crystallization, as in other already-established phase-change memory technologies. Results imply that this approach is also appropriate for probe-based memories. However, experimentally the successful writing of amorphous bits using scanning electrical probes has not been widely reported. In light of this a second approach has been studied, that of writing crystalline bits in an amorphous starting matrix, with subsequent erasure by re-amorphization. With conventional phase-change materials, such as continuous films of $Ge_2Sb_2Te_5$, this approach invariably leads to the formation of a crystalline 'halo' surrounding the erased (re-amorphized) region, with severe adverse consequences on the achievable density. Suppression of the 'halo' was achieved using patterned media or slow-growth phase-change media, with the latter seemingly more viable.**

Index Terms— **GeSbTe, phase-change materials, phase-change RAM, phase-change memories, scanning probe memories**

I. Introduction

The development of data storage and memory technologies continues apace, driven by the need to store ever-increasing amounts of data in ever-decreasing sized formats and with ever-decreasing power consumption. Magnetic hard disk systems and CMOS (NAND-type) 'flash' memories currently dominate the mainstream mass-storage sector. However, both of these technologies face technical challenges (the super-paramagnetic effect in hard disks and scaling limitations in flash memories) in following aggressive data storage roadmaps that foresee storage density (product) requirements of (for hard disks) around 1 Tbits/sq.in. by 2012 and 10 Tbits/sq.in. by 2015 [1]. It is therefore timely to investigate alternative storage technologies. One such alternative is scanning probe-based storage. The most well-known scanning probe-based approach to data storage is that of the IBM 'Millipede' system, where a thermo-mechanical probe is used to write, read and erase indentations in a polymer medium [2,3]. Other promising scanning probe-based technologies include those using ferroelectric storage media [4]–[7] and, the main concern of this paper, those using phase-change media where the material is switched from amorphous to crystalline phase (or vice-versa) using electrical current injected from a conducting tip [8]-[14].

Phase-change materials, usually based on chalcogenide alloys such as GeSbTe or AgInSbTe, have of course been used commercially in optical storage applications for over two decades. Their potential application as alternatives to silicon solid state memories in the form of the so-called PCRAM (phase-change RAM) devices is also a source of intense recent research [15]-[18]. In both optical storage and PCRAM device applications a particular attraction of phase-change materials is their re-writeability, since the basic storage mechanism of switching between amorphous and crystalline phases is inherently reversible. Indeed, an endurance of around 10^{12} cycles has been demonstrated [18]. Re-writeability is of course a most attractive feature of current mainstream mass-storage technologies, and if probe-based storage using phase-change materials is to find application in mainstream mass storage, it too should ideally be able to support re-writeability.

In 'conventional' phase-change memories, including phase-change optical disks and PCRAM devices, re-writeability is implemented using a crystalline starting phase into which an amorphous bit is recorded and subsequently erased (re-written) by re-crystallization [15, 19]. Thus it might seem that using a similar approach for probe storage, i.e. having a crystalline starting phase into which an amorphous bit is written by the probe tip and subsequently erased (re-written) by re-crystallization, should be feasible. However, the experimental writing of amorphous bits in a phase-change medium using electrical probe techniques has, to our knowledge, been reported only by one group of researchers (Tanaka's group at Hokkaido University - see [12]), whereas there are numerous reports of the successful writing of crystalline bits in an amorphous matrix (eg [8-11, 13, 20, 21]). This might imply that the writing of amorphous bits is 'difficult' experimentally. Furthermore, it should be noted that in Tanaka's case [12] the phase-change medium was protected

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from oxidation by being immersed in an inert liquid (3M, Fluorinert FC-43 – see [9]) and the writing tip contacted directly with the phase-change layer]). Obviously a liquid protective layer is not practicable for real storage systems. However, the design of a practicable medium that incorporates a solid overcoat (capping) layer meeting the electrical requirements for successful writing and reading while at the same time providing oxidation protection and wear resistance is not straightforward. Indeed in previous work, where the capping layer was a thin carbon film, excessive temperatures and (electric) fields were predicted to be produced in the overcoat layer during the writing of amorphous bits [13], and this may help to explain why so far no one has reported on the writing of amorphous marks in such 'practical' stack designs (we return to this point later). In this paper therefore we investigate a number of alternative approaches to providing a re-writeability function in electrical probe memories using phase-change media. We begin, in §II, by designing media stacks that allow the writing of both amorphous and crystalline bits to be achieved without generating excessive temperatures during the writing process, thus providing a sound basis for achieving re-writability. In §III the writing and re-writing (erasing) of amorphous bits into the stack designs of §II is investigated. In §IV potential barriers to achieving re-writeability by the writing and erasing of crystalline bits (into an amorphous starting phase) are described and methods that might overcome such barriers, specifically the use of patterned media and slow-growth phase-change materials, are investigated. Throughout the paper designs are driven by the requirement for achieving a high storage density – 1 Tbit/sq.in. and beyond - while at the same time using reasonable write voltages and delivering a practically viable data rate. Since probe memories are expected to operate using massively parallel 2-D arrays of active tips, such as in the IBM Millipede system with in the region of 1000 to 10,000 tips, data rates of around 1 Mbit per second per tip (potentially yielding system data rates in the region of 1Gbit/s to 10 Gbit/s) are reasonable - meaning that the entire write cycle should be completed in less than 1 μs.

II. SYSTEM ARCHITECTURE AND DESIGN OF A RE-WRITEABLE MEDIUM

The physical mechanisms that determine the write and read performance of scanning electrical probe memories using phase-change media involve electrical, thermal and phase-transformation processes. A comprehensive (pseudo-3D) computational (COMSOL Multiphysics^{TM}) model for all such processes, simultaneously solving the (time-resolved) Laplace equation, the heat conduction equation and the JMAK (Johnson-Mehl-Avrami-Kolmogorov) equation has been previously described in detail [13] and so is not repeated here. Rather, this previously described model is used here to assess the feasibility of various routes for providing re-writeability functionality in Tbit/sq.in. probe-based phase-change memories. It should be noted that the model incorporates realistic material properties, such as the experimentally observed temperature dependence of electrical resistivity of the crystalline phase and the temperature and field dependence of the amorphous phase (simulating the well-known threshold switching effect in amorphous chalcogenides [15]). Also the chalcogenide resistivity varies continuously across the solid/liquid transition, with a liquid phase value close to experimentally reported values [22].

The basic storage architecture being considered is shown in Fig. 1. This arrangement is broadly similar to previous studies [8, 13, 20, 21], with the active phase-change layer (here being $Ge_2Sb_2Te_5$ - referred to elsewhere in this paper as GST) being embedded in a tri-layer structure deposited on a silicon substrate and addressed by a conductive tip. However, some significant differences are introduced in the current design. The first major design change is the use of a so-called 'encapsulated-tip' for writing and reading. The encapsulated-tip combines excellent electrical conduction with wear properties and longevity vastly superior to the conventional metal coated silicon tips usually used for conductive AFM applications [23, 24]. It is important to note that in electrical probe recording the written bit size and the readout resolution are primarily determined by the tip electrical contact area, not the physical sharpness of the tip *per se*. Thus it is possible to utilize tips with a large physical contact area, to reduce the contact pressure (and so reduce tip and media wear), while at the same time maintaining high write and read resolutions by ensuring that the tip has a suitably small electrical contact area. In the encapsulated-tip design modeled here, a small, highly conductive PtSi region (here 20nm diameter) provides the electrical contact, and is surrounded by a relatively large (40 nm) insulating SiO_2 (encapsulating) cladding. Such tips have recently been fabricated by IBM and shown to maintain excellent conduction and sustain little wear after many meters of sliding contact [23, 24] as well as successfully writing crystalline bits in GST media [25]. The second major design change, elucidated in detail below, is the use of a medium specifically designed to allow for re-writing.

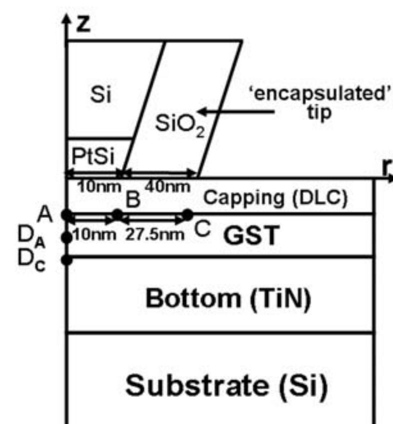

Fig. 1. Schematic of the re-writeable probe storage architecture comprising the encapsulated PtSi tip and a tri-layer storage medium. Points A to D are the locations at which maximum or minimum temperatures are specified in order to design the stack for the writing of both amorphous and crystalline bits, as explained in the text.

A storage medium that allows for re-writeability should meet a number of basic design requirements. Obviously it must be possible to write both amorphous and crystalline bits into the active phase-change layer. Such writing should be achievable without excessive temperatures being generated in the stack (particularly in the thin capping layer) and, for the writing of high densities, the thermal cross-talk between the bit currently being written and adjacent bits should not disturb said adjacent bits. Finally, the write voltage and pulse duration should be at reasonable levels to allow for low power consumption and high data rates. These basic design requirements have been used to define a set of maximum and minimum temperatures that should be achieved at various locations in the storage medium during the writing process.

For the writing of amorphous bits the temperatures in the GST layer (see Fig. 1) at points A (at the top of the GST layer and under the tip center), B (at the top of the GST layer and at the edge of the tip conductive region) and D_A (in the middle of the GST layer and under the tip center) should at least reach the melting temperature (here taken to be 620^0C) so that, when coupled with appropriate cooling rates, this region will solidify into the amorphous phase. Simultaneously with this requirement it is necessary to avoid excessive temperatures in the capping layer (or indeed anywhere in the stack). Here we choose a maximum temperature that should not be exceeded of 1000^0C (reflecting the thermal stability limit of DLC films - see later). Finally, to avoid thermal cross-talk affecting previously written bits, we place a maximum temperature requirement of 200^0C at point C in Fig.1 (i.e. at the top of the GST layer and 25 nm - one bit cell at 1 Tbit/sq.in. - away from the edge of a 25 nm diameter bit located directly under the tip center), ensuring that no crystallization of a previously written amorphous bit takes place. Note that it is not necessary for the entire thickness of the GST layer to be amorphized during the writing of an amorphous bit, since the huge (~ three orders of magnitude) difference between the resisitivities of the amorphous and crystalline phases ensures that good readout contrast is achieved so long as the top part of the GST layer is amorphized (and to require the GST layer to be amorphized over its entire thickness would lead to excessive temperatures in the capping layer).

To write crystalline bits in GST on sub-microsecond time scales requires minimum temperatures of around 300^0C to 400^0C [13, 26], even though the crystallization temperature measured on longer time scales (e.g. by DSC measurements) is typically 175^0C [27]. This is a reflection of the fact that the nucleation rate for GST is a maximum between 300^0C and 400^0C (see Fig. 12 and [15, 19]). Thus, for the writing of crystalline bits in this study the minimum temperature that should be reached at points A and B in Fig. 1 is taken to be 300^0C. Note that for a crystalline bit it is important, to ensure a usable readout signal, that the bit does extend through the whole GST thickness (since any un-transformed amorphous region under the tip would dominate the readout resistance). Thus a further requirement for the writing of a crystalline bit is that the temperature at point D_C in Fig. 1 (i.e. at the bottom of the GST layer and directly under the tip center) should exceed the crystallization temperature, and here we therefore also set a minimum temperature requirement of 300^0C.

Any re-writeable medium stack design must simultaneously meet the above maximum and minimum temperature requirements for the writing of both amorphous and crystalline bits. In previous work [13, 14, 28] it was found that the electrical and thermal conductivity of the capping layer, and its physical thickness, play a very important role in determining the efficacy of the writing process (in particular the maximum temperature achieved in the GST layer). 'Optimum' values for these parameters were found to lie in the range 10 $\Omega^{-1}m^{-1}$ to 100 $\Omega^{-1}m^{-1}$ (electrical conductivity), 0.1 $Wm^{-1}K^{-1}$ to 10 $Wm^{-1}K^{-1}$ (thermal conductivity) and 1 nm to 3 nm (thickness). Such electrical and thermal conductivities can be found in diamond like carbon (DLC) films that can also be deposited into very thin and smooth layers and exhibit very good tribological properties [29-31]. DLC films also possess good thermal stability. Indeed, DLC films have been shown to be thermally stable in bulk annealing experiments at temperatures up to 1000^0C [32, 33] (hence our choice of maximum temperature limit). In light of this we concentrate here on a restricted range of conductivity parameters for the capping layer corresponding to values appropriate for thin DLC films, and fix the thickness of the capping layer at 2 nm (based on the thinnest layer that might be fabricated reliably). For the underlayer, which acts as the return electrode for the potential applied to the tip, we require a good electrical conductivity coupled with a relatively modest thermal conductivity (the latter requirement to retain enough heat in the stack to meet the minimum temperature requirements). A good choice is likely to be TiN, which is already used as electrode material in PCRAM devices and can be prepared with a range of suitable thermal and electrical conductivities [15, 34-36]. Thus we restrict the parameter search for underlayer properties to those corresponding to typical TiN thin films. Taking all these restrictions into account, a parameter search for suitable values of the capping and underlayer properties has been carried out, focusing in particular on the role of thermal and electrical conductivity on the aforementioned temperature requirements at points A to D in Fig. 1. Results are shown in Fig. 2 and Fig. 3, for a fixed GST thickness of 10 nm (we shall return to the role of GST thickness later). Note that in all cases the write pulse duration is fixed at 200ns, including a 20 ns/50 ns rise and fall time for writing of amorphous/crystalline bits respectively. Such a write pulse duration should ensure that a 1Mbit/second data rate per tip is easily achieved, even allowing for the finite time needed for the tip to move on to the next bit location after writing the current bit.

Figure 2(a) shows the voltage required to achieve the GST melting temperature at points A, B and D_A in Fig. 1, as a function of the thermal conductivity of the capping layer, as well as the 1000^0C maximum temperature contour. Note that the 200^0C thermal cross-talk contour is outside the plot (i.e. occurs for voltages beyond 6 V). In Fig. 2(a) the electrical

conductivity of the capping layer was set to 50 $\Omega^{-1}m^{-1}$, while the underlayer has a thermal conductivity (K_{under}) of either 12 $Wm^{-1}K^{-1}$ or 3 $Wm^{-1}K^{-1}$ and an electrical conductivity of $5x10^6$ $\Omega^{-1}m^{-1}$, in line with typical values reported in the literature for TiN electrodes [34-36]. The values used for other relevant material parameters are given in Table I.

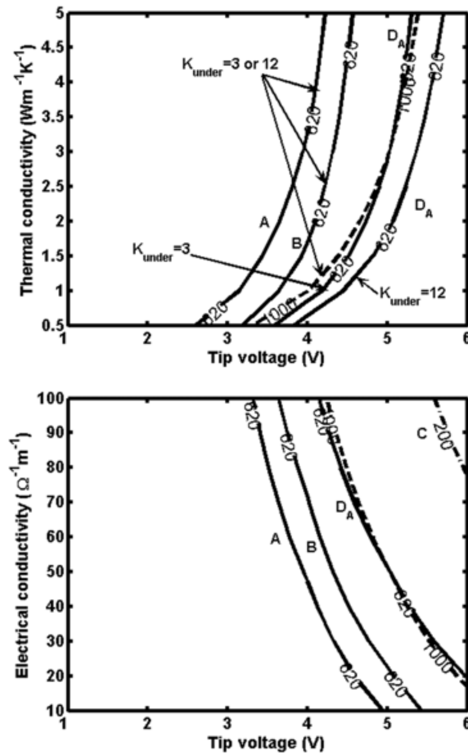

Fig. 2. Temperature contours for points A, B, C and D_A and a maximum of 1000^0C as a function of tip voltage, when writing an amorphous bit (in a crystalline starting phase) and: (a) (top) varying the thermal conductivity of the capping layer (for a fixed electrical conductivity 50 $\Omega^{-1}m^{-1}$ and with an underlayer electrical conductivity of 5 x 10^6 $\Omega^{-1}m^{-1}$ and thermal conductivity of either 3 $Wm^{-1}K^{-1}$ or 12 $Wm^{-1}K^{-1}$); (b) (bottom) varying the electrical conductivity of the capping layer (for fixed thermal conductivity 3 $Wm^{-1}K^{-1}$, and an underlayer electrical conductivity of 5 x 10^6 $\Omega^{-1}m^{-1}$ and thermal conductivity of 3 $Wm^{-1}K^{-1}$). The numbers on contour lines refer to the relevant temperature in ^{0}C. In all cases a 200 ns voltage pulse with a 20 ns rise/fall time was used, and the temperature was calculated after 180 ns (i.e. just before the voltage starts to 'turn off'). Thickness of capping and GST layer is 2 nm and 10 nm respectively.

For the TiN thermal conductivity of 12 $Wm^{-1}K^{-1}$ the contours for melting at point D_A and exceeding a maximum temperature of 1000^0C do not overlap, which would imply that in this case, whatever the thermal conductivity of the DLC capping layer (within the range studied) or the applied voltage, we could not write an amorphous bit that extends a significant depth into the GST layer without exceeding 1000^0C in the capping layer. However, reducing the thermal conductivity of the underlayer to 3 $Wm^{-1}K^{-1}$, still a reasonable value for actual TiN thin films (see [35] for example), moves the melting contour at D_A to lower voltages, such that all the maximum/minimum temperature requirements set previously for the writing of amorphous marks can now be met for moderate voltages and realistic values for the thermal and electrical conductivity of the DLC capping layer. Since thermal and electrical conductivity are usually linked (e.g. by the Wiedemann-Franz law in metals) we also show, in Fig. 2(b), the effect of changing the electrical conductivity of the capping layer on the temperature contours. It can be seen that increasing the electrical conductivity of the capping layer decreases the required write voltage amplitude to achieve a given temperature, and that a conductivity of around 40 $\Omega^{-1}m^{-1}$ and above should enable melting of the GST layer in the required region without exceeding 1000^0C in the capping layer. However, increasing the capping layer conductivity too much reduces the readout contrast (i.e. the normalized difference between the readout current between amorphous and crystalline bits – see [28]). The underlayer conductivity was also varied by an order of magnitude (from 0.5 x 10^6 to 5 x 10^6 $\Omega^{-1}m^{-1}$) and the temperature contours re-calculated (for fixed values of capping layer electrical and thermal conductivity of 50 $\Omega^{-1}m^{-1}$ and 3 $Wm^{-1}K^{-1}$ respectively, and fixed underlayer thermal conductivity of 3 $Wm^{-1}K^{-1}$), but the effects were negligible and are therefore not shown here.

TABLE I
Characteristic parameters in the simulations

	Tip probe		Capping	Recording	Bottom electrode	Substrate
	PtSi	SiO_2	C	GST (a/c)	TiN	Si
Thickness (nm)	N/A	N/A	2	5-25	40	150
Thermal conductivity ($Wm^{-1}K^{-1}$)	25	1.4	0.5-5	0.2/0.58	3 or 12	149
Electrical conductivity ($\Omega^{-1}m^{-1}$)	$3.3 \cdot 10^6$	$1 \cdot 10^{-12}$	10-100	See[1]	$5 \cdot 10^5$- $5 \cdot 10^6$	N/A
Density (Kgm^{-3})	12400	2200	2800	6150	5400	2330
Heat capacity ($JKg^{-1}K^{-1}$)	250	700	540	210	400	720

[1] See [13].

If we place a maximum limit of 5 V on the amplitude of the tip voltage, the results of Fig. 2(a) and 2(b) point to a medium stack design for the writing of amorphous bits, while not exceeding a maximum temperature of 1000^0C and a thermal cross-talk temperature of 200^0C, comprising a GST layer sandwiched between a TiN electrode with a thermal conductivity of 3 $Wm^{-1}K^{-1}$ and an electrical conductivity anywhere in the range 5 x 10^5 $\Omega^{-1}m^{-1}$ to 5 x 10^6 $\Omega^{-1}m^{-1}$, and a DLC capping layer with a thermal conductivity of 3 $Wm^{-1}K^{-1}$ and electrical conductivity from 50 $\Omega^{-1}m^{-1}$ to 100 $\Omega^{-1}m^{-1}$. Using these values we can now determine if the same stack is suitable for the writing of crystalline bits, and therefore whether it is likely to be useful for re-writeable applications (where many successive amorphous-crystalline transitions, or vice-versa, have to be supported). Results are shown in Figs. 3(a) and (b), where the role of thermal and electrical conductivity of the capping layer and the thermal conductivity of the underlayer on the temperatures achieved at points A, B

and D_C (in Fig. 1) is elucidated. It appears that the requirements for the writing of a crystalline bit can also be met by a Si/TiN/GST/DLC stack, with TiN and DLC thermal and electrical conductivities in the range already identified. For example, a DLC capping with thermal and electrical conductivities of 3 $Wm^{-1}K^{-1}$ and 50 $\Omega^{-1}m^{-1}$, coupled with a TiN electrode with thermal and electrical conductivities of 3 $Wm^{-1}K^{-1}$ and 5 x 10^6 $\Omega^{-1}m^{-1}$, is predicted to generate the requisite crystallization temperatures at points A, B and D_C for a 200 ns pulse with amplitude in the range 4 V to 5 V, pulse, while at the same time avoiding excessive (>1000^{0}C) temperatures in the capping layer.

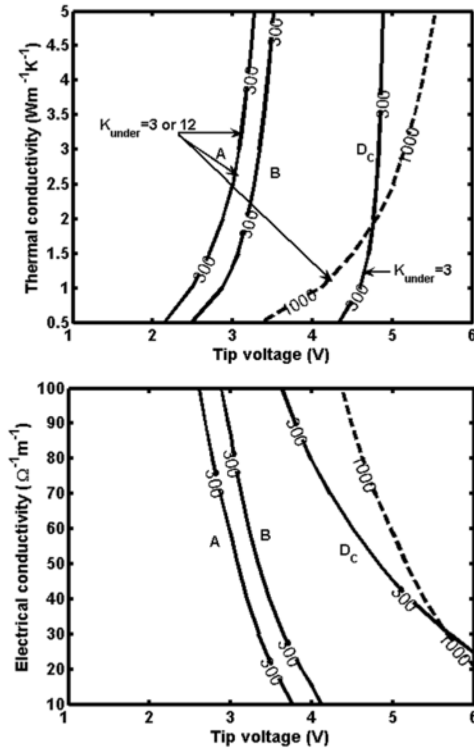

Fig. 3. Temperature contours for points A, B, and D_C as a function of tip voltage when writing a crystalline bit (in an amorphous starting phase) and: (a) (top) varying the thermal conductivity of the capping layer (for a fixed electrical conductivity 50 $\Omega^{-1}m^{-1}$ and with an underlayer electrical conductivity of 5 x 10^6 $\Omega^{-1}m^{-1}$ and a thermal conductivity of either 3 $Wm^{-1}K^{-1}$ or 12 $Wm^{-1}K^{-1}$); (b) (bottom) varying the electrical conductivity of the capping layer (for a fixed thermal conductivity of 3 $Wm^{-1}K^{-1}$, and an underlayer electrical conductivity of 5 x 10^6 $\Omega^{-1}m^{-1}$ and thermal conductivity of 3 $Wm^{-1}K^{-1}$).). The numbers on contour lines refer to the relevant temperature in ^{0}C. In all cases a 200 ns voltage pulse with a 50 ns rise/fall time was used, and the temperature was calculated after 150 ns (i.e. just before the voltage starts to 'turn off'). Thickness of capping and GST layer is 2 nm and 10 nm respectively.

In the discussions above, and the results of Figs. 2 and 3, the thickness of the GST layer was fixed at 10 nm. Having found 'optimum' values for the thermal and electrical conductivities of the capping and underlayer for this value of GST thickness, it is instructive to vary the GST thickness and note the effect on the various temperature contours. The GST thickness was therefore varied between 5 nm (possibly a minimum practicable value for reliable GST film fabrication) up to 25 nm and the temperature contours as a function of tip voltage re-calculated. For brevity the results are not shown here. However, it was found that for the writing of an amorphous mark the most noticeable effect was that the melting (620^{0}C) contour for point D_A moved to higher voltages and intersected with the 1000^{0}C maximum temperature contour for GST thicknesses above 10 nm (i.e. temperatures above 1000^{0}C were predicted in the capping layer for GST thicknesses bigger than 10 nm). For the writing of crystalline bits the most noticeable effect was that the 300^{0}C contour at point D_C moved to lower tip voltages as the GST thickness increased from 5 nm to 15 nm, but moved back to higher voltages again as the GST thickness increased above 15 nm. Thus, a 10 nm GST thickness does appear to be an 'optimum' choice. Now that a stack design and a range of material parameters have been determined that should allow for the writing of both amorphous and crystalline marks in practicable phase-change media, and real materials (TiN and DLC) whose properties fall within the said parameter ranges have been identified, we look in detail at the bit writing, erasing and re-writing process.

III. RE-WRITABILITY VIA AMORPHOUS BITS IN A CRYSTALLINE MATRIX

As already mentioned in §II, the writing of an amorphous mark requires that the temperature in the GST layer exceeds the melting temperature (620^{0}C) and that rapid cooling occurs to freeze the melted region into the amorphous phase. The cooling rates required for GST are typically quoted in the literature as being of the order of tens of degrees per nanosecond [34], while previous simulations by ourselves found a critical cooling rate of 37 ^{0}Cns^{-1} to be necessary [13]. Thus in this work amorphization is taken to occur in regions that experience temperatures in excess of 620^{0}C and also cool at rates greater than 37 ^{0}C ns^{-1}.

Before writing amorphous bits into the media stacks designed in §II, it is instructive (and serves as a useful test of our model) to first examine the writing of amorphous bits in the experimental set-up used by Tanaka et al [12] who, as previously mentioned, are to our knowledge the only group to have reported the writing of amorphous marks in GST using conductive AFM-type probes. Tanaka's medium comprised a relatively thick GST layer (20 nm to 500 nm), with a Pt underlayer electrode (50 nm thick) on a Si substrate. A home-made gold tip was used to apply the writing voltage and was in direct contact with the GST layer. There was no capping layer, but since GST readily oxidizes the entire tip-medium assembly was placed in an inert liquid for protection. Tanaka's system has been simulated using our model, and typical results, in this case for a 50 nm thick GST layer and a 1V, 100 ns write pulse are shown in Fig. 4. The model predicts an amorphous bit of approximately 80 nm in diameter to be formed, in close agreement to the experimentally observed values (in range 90 nm to 100 nm). The total energy required to write the amorphous bit (35 pJ) is also close to the

experimentally reported value (in range 10 pJ to 100 pJ). Interestingly the maximum temperature in the medium stack for this case is predicted to exceed the target figure of 1000^0C set in §II, and occurs in the GST layer itself. It should also be noted that Tanaka's group also managed to write significantly smaller amorphous bits (in the range 10 nm to 30 nm in fact) with smaller write pulse durations/pulse energies and thicker GST films, and in these cases the maximum temperature in the stack is reduced (e.g. shortening the 1V pulse to 5 ns predicts a 40 nm diameter amorphous bit in a 250 nm thick GST layer with a maximum temperature reached of 750^0C).

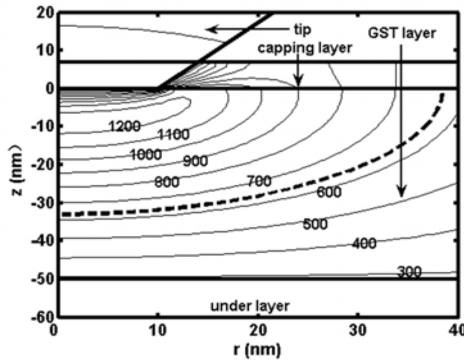

Fig. 4. Simulation of the writing of an amorphous mark into a Si/Pt/GST/Fluorinert (capping layer) media stack and tip arrangement from [12]. A 1 V, 100 ns write pulse with 20 ns rise/fall times was used. The figure shows the temperature contours just before the voltage pulse is turned off (i.e. at 80 ns) and (dotted line) the final amorphized region.

Now we turn our attention to writing amorphous bits into the medium stack designed in §II, namely a Si/TiN/GST/DLC structure with material properties for each layer as described in Table I and in which the starting phase of the GST layer is crystalline. Applying a 5 V, 200 ns write pulse (with 20 ns rise and fall times) produces the temperature distribution and final amorphous mark shape shown in Fig. 5. Note that the design requirement that the maximum temperature in the capping layer (indeed anywhere in the stack) remains below 1000^0C is met. Similarly the thermal cross-talk effect in this case is negligible, the temperature at the edge of any adjacent bit (point C in Fig 1) being only just over 150^0C. The final amorphous bit size, being around 25 nm at its widest point, also matches the requirements of a density of at least 1 Tbit/sq.in. The energy required to write the bit was 88 pJ, substantially less than in previous work (e.g. 300 pJ in [13]) and in the range observed experimentally [12].

To ensure re-writability, the bit of Fig. 5 must be capable of being re-crystallized and subsequently re-amorphized. If the bit can be fully re-crystallized, taking the medium back to its starting phase, then re-writability is assured. This is indeed seen to be the case, as shown in Fig. 6 where a 4 V, 200 ns (69 μA, 55 pJ) pulse (with a 50ns rise and fall time) re-crystallizes the entire amorphous mark (and smaller voltages re-crystallize only part of the mark). Note that the maximum temperature in the stack during the erasing never exceeds the GST melting temperature, thus re-crystallization is via the solid-state. Note also that the thermal cross-talk is negligible.

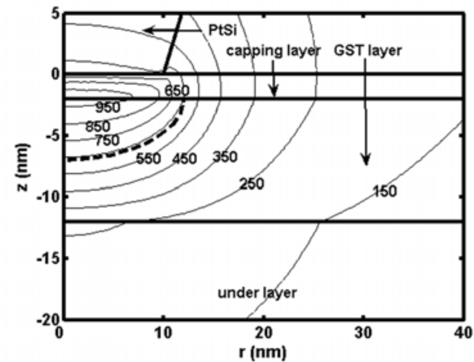

Fig. 5. Simulation of the writing of an amorphous mark into the Si/TiN(40nm)/GST(10nm)/DLC(2nm) stack designed in §II. A 5 V, 200 ns write pulse with 20 ns rise/fall times was used. The figure shows the temperature contours just before the voltage pulse is turned off (i.e. at 180 ns) and (dashed line) the final amorphized region.

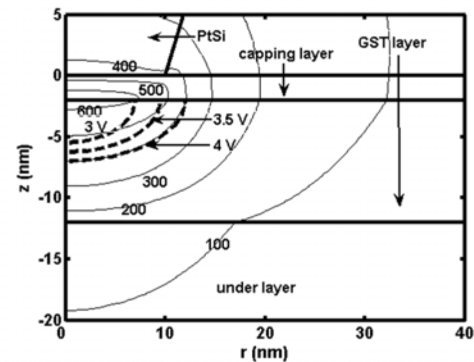

Fig. 6. Erasing (re-crystallization) of the amorphous mark of Fig. 5. A 200 ns erase pulse (50 ns rise/fall times) of various amplitudes was used. A 4 V amplitude completely erases the amorphous mark; voltages less than this partially erase the mark. Also shown are the temperature contours just before the 4 V pulse is turned off (i.e. at 150 ns).

As in previous studies [13, 28], and in line with other phase-change memory technologies, these simulations imply that re-writeable probe storage should be feasible by first writing amorphous bits into a crystalline starting phase, then erasing (re-writing) by re-crystallization. However, as already pointed out in §I above, the experimental writing of amorphous bits into a crystalline starting matrix using scanning electrical probes has been reported only once [12]. This may be because systematic attempts (e.g. by systematic variation of write pulse conditions over the full range) have not been widely made, or it may be that researchers have found it difficult to successfully write amorphous marks, but not reported such difficulties. On the other hand, there are numerous reports of successful writing of crystalline bits in an amorphous matrix (e.g. [8-11, 13, 20, 21]). In light of this it is sensible to also examine the feasibility of achieving re-writeability using crystalline bits written into an amorphous starting phase.

IV. RE-WRITABILITY VIA CRYSTALLINE BITS IN AN AMORPHOUS MATRIX

As already pointed out above, numerous groups worldwide have been successful in the writing of crystalline bits in an amorphous matrix. Some of our own results are shown in Fig.

7(a) where, for the first time as far as we are aware, a TEM cross-section is given of crystalline bits recorded into a medium stack similar to that designed in §II. In this case however an additional intermediary DLC layer above the TiN electrode was used, which can be helpful in avoiding migration of Ti ions into the GST layer and the formation of Ti-Te compounds, as sometimes seen in PCRAM devices [35]. In addition a conventional CAFM type tip was used, of the DLC coated Si variety and with a contact diameter of approximately 50 nm. A rather long (10 µs) and high amplitude (8V) write pulse was used to ensure the formation of a crystallized region easily observable in the TEM. The combination of a relatively large tip contact area and a high amplitude/long duration write pulse resulted in a large crystallized bit (~ 100 nm wide at the top of the GST layer and 80 nm at the bottom) that extends all the way through the GST layer. Also apparent from Fig. 7(a) is that in places the carbon capping layer has disappeared. This is likely due to very high temperatures generated in the capping layer as a result of the relatively high voltage and long duration write pulse. Indeed, simulation of the writing of crystallized marks into the media stack of Fig. 7(a) predicts temperatures in the capping layer in excess of 1500^0C, as shown in Fig. 7(b). Also shown in Fig. 7(b) is the predicted final mark size and shape, which is in very good agreement with that observed from the TEM image.

We now return to the main task of this section, examining the re-writeability of crystalline bits in the Tbit/sq.in. density regime. Prior to any analysis of the erasing (re-writing) of crystalline bits, the feasibility of recording crystalline bits using the media stack design of §II is demonstrated. Results are shown in Fig. 8, for a 4V, 200ns write pulse (with a 50ns rise/ fall time). As expected, the written mark size is dominated by the electrical contact size (the PtSi contact area) and a crystalline bit of approximately 25 nm in diameter is formed. The bit is roughly hemi-spherical and importantly, from a readout perspective (see [13, 28]), extends through the whole thickness of the GST layer. It is interesting to point out that the total energy required to write the bit shown in Fig. 8 was only 54 pJ (and the current was 67 µA), again, significantly less than the energy/bit reported previously [13] and in line with experiment [8, 9].

Attention is now turned to the erasing of crystalline bits. Erasing requires the temperature inside the bit to be taken above the GST melting temperature (620^0C) coupled with a rapid cooling to freeze the erased bit into the amorphous phase. For proper erasure it is also necessary that the matrix surrounding the recorded crystalline bit should remain amorphous, which, as shall be shown, is not a criterion that is easily met. Figure 9 shows the result of trying to erase the bit of Fig. 8 using a 5 V, 200 ns erase pulse (with 20 ns rise/fall times). It appears that it is feasible to obtain melting in at least the top portion of the pre-written crystalline bit, and to cool fast enough for this region to solidify in to the amorphous phase. The fact that only the upper part of the pre-written crystalline bit is erased is not in itself a barrier to the realization of a practical system since, as already pointed out, the large difference between the electrical conductivity of the amorphous and crystalline phases would ensure a large readout signal for such a case. However, the result in Fig. 9 also shows that an unwanted crystalline ring or 'halo' is formed around the erased region. The formation of such a ring is simply a result of this region being subjected to a temperature above the crystallization temperature but below the melting temperature during the erase process.

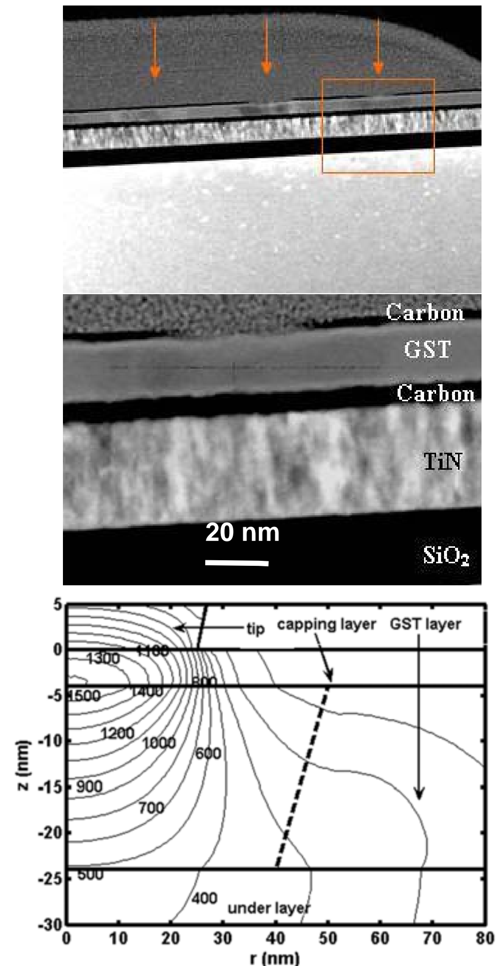

Fig. 7. (a) (top and middle) TEM cross-section of crystalline bits written into a Si/TiN(40nm)/DLC(10nm)/GST(20nm)/DLC(4nm) stack using a 50 nm diameter DLC coated Si tip and a 8 V, 10 µs write pulse. Location of written bits marked by arrows and crystalline regions show as darker contrast. Region in box in upper image is shown zoomed in the lower image. Note the disappearance of the DLC capping layer. (b) (bottom) Simulation of the writing of a crystalline bit into the medium stack of Fig. 7(a). The final crystallized region is delineated by the dashed line. Also shown are temperature contours just before the 8 V write pulse turns off (i.e. at 9.95 µs). Thermal conductivity of the DLC and TiN layers was taken to be 3 $Wm^{-1}K^{-1}$, electrical conductivity of the DLC layers was 50 $\Omega^{-1}m^{-1}$ and of the TiN layer was 5×10^6 $\Omega^{-1}m^{-1}$.

Such 'halo' effects have been observed experimentally in laser bit writing studies on similar materials [11] and are an ever-present feature so far in our simulations of the erasure of crystalline bits in probe storage systems. It should be pointed out that the 'halo' effect would result in a serious degradation

of both the readout signal and the achievable storage density. It might be tempting to use a higher amplitude erase pulse to try and increase the effectiveness of the erase (amorphization) process. However, as might be expected, this does not remove the crystallization 'halo', but simply shifts it laterally. Decreasing the fall time of the erase pulse also does not remove the 'halo' effect. Clearly an alternative approach to eliminate or suppress the crystal 'halo' effect is needed. Here we propose and investigate two such possible methods, namely (i) the use of patterned media and (ii) the use of a phase-change layer made from a slow crystal growth material.

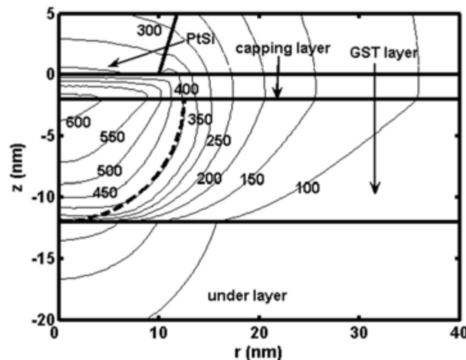

Fig. 8. Simulation of the writing of a crystalline mark into the Si/TiN/GST/DLC stack designed in §II. A 4 V, 200 ns write pulse with 50 ns rise/fall times was used. The figure shows the temperature contours just before the voltage pulse is turned off (i.e. at 150 ns) and (dashed line) the final crystallized region.

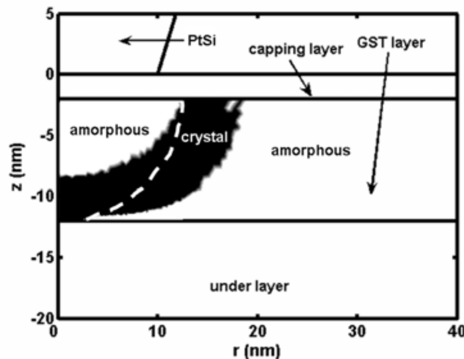

Fig. 9. Erasing (re-amorphizing) of crystalline bit of Fig. 8. A 5 V, 200 ns write pulse with 20 ns rise/fall times was used. A region underneath the tip (shown in white) is amorphized as desired, but a crystal 'halo' is also formed (shown in black). Extent of original crystalline bit is shown by dotted line.

A. Patterned Media

Suppression of the formation of the crystal 'halo' effect should be relatively straightforward using a patterned medium in which small phase-change regions are isolated from each other, preferably by some kind of thermal insulator. A potential geometry is shown in Fig. 10 where a 20 nm diameter cylinder of GST is embedded in an SiO_2 matrix. Extended to a checkerboard type pattern, such a geometry would yield a storage density approaching 1 Tbit/sq.in.. Kim et al [39] have already demonstrated experimentally the ability to induce switching in patterned GST media, both from the crystalline state to the amorphous state and back again. However, they used patterning on the micrometer scale and a very large (18 μm) tungsten tip.

Prior to investigating the re-writeability of patterned GST media, it is instructive to confirm that crystalline bits can indeed be written into the patterned region from an amorphous starting phase. A 4 V, 200 ns (61 μA, 48 pJ) write pulse, identical to that used for the continuous medium case crystallizes most of the patterned region, but leaves a small part untransformed, as can be seen in Fig. 10. Increasing the write pulse voltage amplitude (e.g. a 5 V, 200 ns pulse) or duration (e.g. a 4 V, 1 μs pulse) crystallizes the entire region. It should be noted that such a writing procedure in the patterned medium only needs to be carried out once, since thereafter (as we see below) switching between states is confined to the upper portion of the patterned region. Indeed, the process of setting all the patterned regions to the crystalline state is a form of initialization similar to that carried out in the manufacture of phase-change optical disks, and could similarly be carried out on the entire patterned medium assembly in one go by some 'bulk' heating process (such as in an oven or by scanned laser).

Having confirmed that crystalline bits can be written into a patterned medium (or induced by some bulk annealing procedure), attention is now turned to their erasure. Thus, a 5 V, 200 ns erase pulse, as used in the continuous case of Fig. 9, is applied and the resulting temperature distribution and final mark shape are shown in Fig. 11. It can be seen that the top part of the patterned crystalline bit is erased (amorphized), in similar fashion to the continuous media case. However, patterning has eliminated the crystalline 'halo' effect since the region in which the 'halo' would like to form has been replaced (in this case) with SiO_2. The fact that only the top part of the patterned region is amorphized is, as for the continuous media case, not a barrier to the realization of a practical system. Finally, to confirm re-writability the patterned bit of Fig. 11 the entire patterned region was returned to its original crystalline phase by a 4 V, 200 ns (62 μA, 50 pJ) pulse (result not shown).

It would seem, from the results presented in this section, that the use of patterned media could provide re-writeability when writing crystalline bits into an amorphous starting phase. However, in reality two practical problems remain. The first is that the patterning of media at the dimensions required for ultra-high density storage requires expensive state-of-the-art lithography, a technique not readily suited to the provision of relatively cheap mass storage media. Even if lithography at the nanoscale were to become much simpler and cheaper (e.g. by some of the nanoimprinting techniques currently being developed), there remains a fundamental problem with the use of patterned media in probe storage systems, a problem not often mentioned in the literature. For probe storage to be a viable technology requires the use of 2D probe arrays, with large numbers of probes within such arrays operating in parallel in order to provide sufficient write/read data rates. Each individual tip within such an array thus addresses its own data field, typically an area around 100 μm x 100 μm, as

in the original Millipede system [2, 3]. For tips to operate in parallel, they must each be properly and simultaneously located over the bits in their own fields. This is likely to be a major problem in patterned media, assuming tip array and patterned media are fabricated by separate lithographic processes, unless each tip has its own x-y actuation system, which would significantly increase the cost and complexity of array fabrication. Thus the viable use of patterned media with probe arrays seems problematic at present.

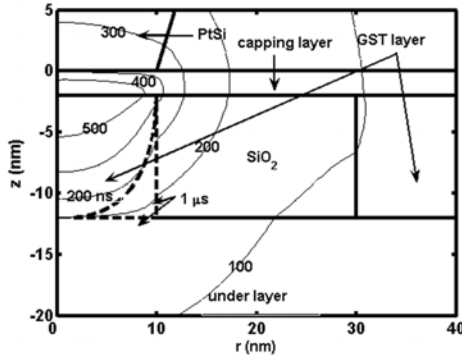

Fig. 10. Schematic of the patterned medium showing 20 nm GST regions isolated by 20 nm SiO_2 regions. Also shown is the predicted extent (dashed lines) of a crystalline mark written into an amorphous starting phase for a 4 V write pulse of 200 ns or 1000 ns duration. and the temperature contours just before the 1000 ns pulse is turned off (i.e. at 950 ns).

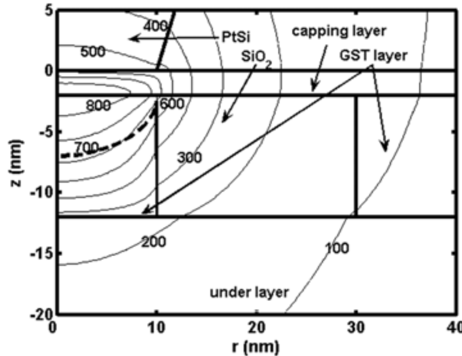

Fig. 11. Erasing (re-amorphizing) of a crystalline bit in the patterned medium of Fig. 10. A 5 V, 200 ns write pulse with 20 ns rise/fall times was used. The figure shows the temperature contours just before the voltage pulse is turned off (i.e. at 180 ns) and (dashed line) the final amorphized region.

B. Slow Crystal Growth Material

Due to the potential problems with patterned media (fabrication costs and tip array alignment issues) an alternative route to realize the erasing of crystalline bits is here investigated, namely the use of 'slow-growth' phase-change materials. Traditionally, at least in the case of optical storage, faster and faster crystallization materials have been sought to allow for faster and faster data rates. However, in probe storage systems the overall data rate is governed not only by the data rate per tip, but also by the number of tips operating in parallel in the 2D tip array. Thus, the data rate per tip can be relatively modest, and in this paper a target of 1Mbit/s has been used. At such relatively modest (compared to optical storage) data rates, having a phase-change material with a very fast crystallization speed is not really necessary. Therefore, it might be possible to prevent the formation of the crystalline 'halo' by using a material whose crystallization rate is too slow for crystallization to occur during an erase pulse.

The GeSbTe alloy considered so far in this work has a nucleation rate and growth velocity (which together determine the crystallization rate) typically as shown in Fig. 12 [21,26,41]. The maximum growth speed is around 1 ms^{-1}, at which rate a crystal boundary could move many nanometers during a typical erase pulse, undoubtedly contributing to the formation of the crystal 'halo'. In light of this a search for 'slow-growth' materials with a growth velocity at least ten times smaller than GST has been made; a suitable candidate appears to be $GeTe_6$ [21]. We thus investigate the potential of such slow-growth alloys with regard to providing re-writability when writing crystalline bits in an amorphous matrix.

In order to evaluate the performance of slow-growth materials, we need to replace the JMAK crystallization model used above, since it does not allow for separable nucleation and growth parameters. In light of this we use a classical nucleation and growth model, as often used for the simulation of phase-change optical disks and PCRAM devices (e.g [15, 19, 37, 40]). In short the nucleation rate I_{nuc} can be written as

$$I_{nuc} = \alpha \exp\left(-\frac{E_{an}}{k_B T}\right)\exp\left(-\frac{\Delta G_C}{k_B T}\right), \quad (1)$$

$$\Delta G_C = \frac{16\pi\delta^3}{3\Delta g^2}, \quad (2)$$

where α is a pre-factor, E_{an} is the activation energy for nucleation, ΔG_C is the excess free energy for the formation of a (energetically) stable crystal nuclei, δ is the interfacial energy, T is the temperature, k_B is Boltzmann's constant and Δg is the Gibbs free energy difference between the crystal and the supercooled liquid, given by [37]

$$\Delta g = \Delta H\left(\frac{T_m - T}{T_m}\right), \quad (3)$$

where T_m is the melting temperature and ΔH is the enthalpy of fusion. Once stable crystal nuclei have formed, they are assumed to grow at a velocity V_g given by [15, 19, 34]

$$V_g = V_0 \exp\left(-\frac{E_{ag}}{k_B T}\right)\left(1 - \exp\left(-\frac{\Delta g'}{k_B T}\right)\right) \quad (4)$$

where V_0 is a temperature dependent pre-factor, E_{ag} is the activation energy for growth, $\Delta g'$ is the free energy difference per atom between the amorphous and crystalline phase, with other terms as previously described.

For simulations using the nucleation-growth model, the region to be simulated is split into square tiles of size 1 nm x 1 nm, corresponding approximately to the minimum room temperature stable nucleus size in GST [13]. In each time step of the simulation the temperature in each tile is calculated, using the same electro-thermal model used above and the probability that a particular tile will nucleate is given by

multiplying the nucleation rate in (1) by the time interval and the (notional) volume of a tile. Once a tile has nucleated it may then grow with a velocity according to (4). Relevant parameters used in the simulations were taken from [41] and are: E_{ag} and E_{an} of 2.6 eV; $\delta = 0.1$ Jm^{-2}, $\Delta H = 1121$ Jm^{-3}, $T_m = 893$ K, $\alpha = 10^{56}$ m^{-3}K^{-1} and $V_0 = \beta.\exp[-0.8/(1-T/T_m)]$ ms^{-1} with β equal to 3.9x10^{19} (for GST) or 3.9x10^{18} (for slow-growth material).

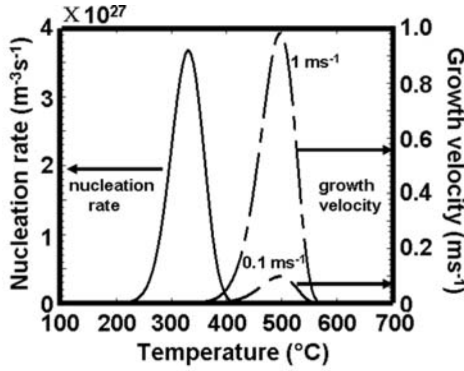

Fig. 12. Nucleation rate and growth rate as a function of temperature, for GST and for a notional 'slow-growth' material (taken from [21, 26, 41]).

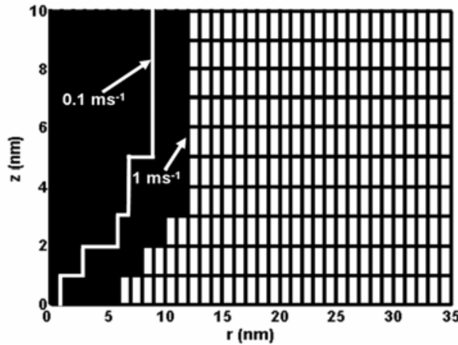

Fig. 13. Simulation, using nucleation and growth model, of the writing of a crystalline mark in the Si/TiN/GST/DLC stack designed in §II using GST with a 'standard' growth velocity and a notional 'slow-growth' material (white line). A 3.5 V, 200 ns write pulse with 50 ns rise/fall times was used.

To evaluate the potential performance of slow-growth phase-change media, we begin by confirming that a crystalline bit can be written into an amorphous starting phase. Results are shown in Fig. 13, for a 3.5 V, 200 ns write pulse and a maximum growth rate of 0.1 ms^{-1} and, for comparison purposes, a maximum growth rate of 1 ms^{-1}. As would be expected, the bit size for the slow-growth material is smaller. In Figs. 14(a) and 14(b) we compare the erase behavior of the 'standard' and slow-growth phase-change materials. For the 'standard' 1 ms^{-1} growth velocity material, the crystalline 'halo' is clearly evident (see Fig. 14(a)), but for the slow-growth case the halo is suppressed (see Fig. 14(b)), since there is not enough time during the heating/cooling cycle for it to grow in this case. It should be pointed out that apart from the maximum growth velocity, all other material parameters for the 'standard' and slow-growth phase-change materials are here taken to be the same. It should also be pointed out that the re-writing of a crystalline bit into the 'erased' (re-amorphized) configuration of Fig. 14(b) was straightforward with the same writing pulse (3.5 V, 200 ns) used to write the original crystalline bit of Fig. 13. During this re-writing process the residual parts of the crystalline 'halo' (circled in Fig. 14(b)) reached only moderate temperatures of around 190^{0}C. At such temperatures the growth velocity of the crystal phase is small, around 0.02 nm/s, so that a large number of (200 ns) re-write pulses would be needed for the residual 'halo' to grow a significant amount. Indeed ~ 2.5x10^8 re-write pulses, sufficient for most practical applications, would be needed per nm of growth. Clearly the indications are that slow-growth materials might indeed be suitable for re-writeable applications in which a crystalline bit is written into an amorphous starting matrix and then erased by re-amorphization. Materials with growth rates in the required range ($GeTe_6$) have been identified [21], but no results on their writing, reading and re-writing behavior yet reported.

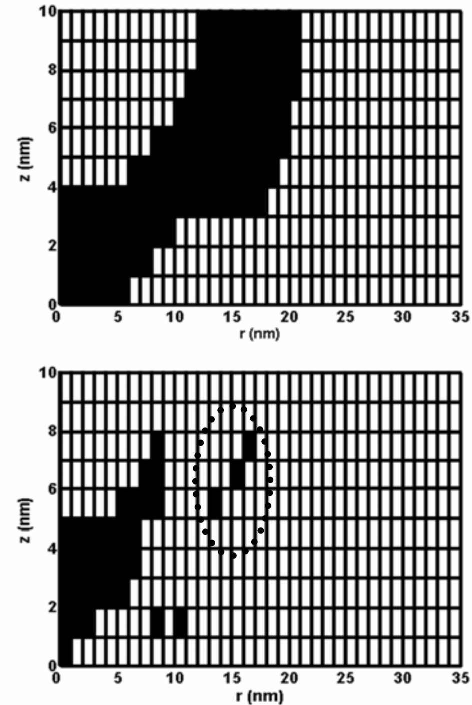

Fig. 14. Erasing (re-amorphizing) of the crystalline bits of Fig. 13 for (a) (top) standard GST (using a 5 V, 200 ns pulse) and (b) (bottom) a notional slow-growth material (using a 4.5 V, 200 ns pulse). Pulse rise/fall time was 20 ns in both cases. The suppression of the crystal 'halo' in (b) is clear although residues of it persist (circled).

V. DISCUSSION AND CONCLUSIONS

The design model presented above is relatively complex and uses wherever possible experimentally reported material parameters to ensure realistic results. However, as with most simulations there are some idealizations in the model, the consequences of which should be discussed.

Perhaps the most obvious idealization is the assumption of a perfectly flat medium surface. In reality although DLC films can be made very smooth indeed with rms roughness values as low as 0.1 nm reported [42] they are not entirely flat. In the case of non-zero surface roughness we might expect that the

area of contact between the tip and the medium would be reduced, with the knock-on effect of a reduced current flow (as compared to the perfectly flat case). It might also be expected that increasing the tip voltage could mitigate such a reduction in current. Indeed, we have performed some preliminary simulations of the effects of surface roughness by introducing a simple sinusoidal variation of the top surface of the capping layer that seems to confirm this expectation. For example, with a 1 nm amplitude/1 nm period surface roughness, both the amorphous mark of Fig. 5 and the crystalline mark of Fig. 8 can be reproduced (i.e. matched in size and shape) by simply increasing (from the 5 V and 4 V used previously) the write voltage to 7 V and 6 V respectively. Furthermore, this can be achieved without exceeding the maximum temperature 'limit' (of 1000^0C) in the capping layer. For significantly larger amplitude/period variations in roughness it becomes increasingly more difficult to write marks identical to those seen in Fig. 5 and Fig. 8, without excessive temperatures being generated. Another (related) idealization is that the tip-medium electrical contact resistance is here assumed zero, whereas in reality it is likely to be in the region of several kΩ up to a hundred kΩ or more, depending on the force exerted on the tip and the electrical and mechanical properties of the capping layer (see [43] for a discussion of such effects). However, we have found that contact resistances up to around 5 kΩ have little effect on the bit writing process (e.g. the bits of Fig. 5 and Fig. 8 can be written with the same 5V and 4 V pulses used previously), larger contact resistances (up to a few tens of kΩ) can be compensated for by an increase in write voltage (without excessive temperatures in the capping layer) while in the case of very high contact resistances (> 250 kΩ) it becomes increasingly difficult to write bits with reasonable voltages and without reaching excessive temperatures (> 1000^0C) in the capping layer.

It should also be pointed out that the simulations presented here have neglected any thermal boundary resistance (TBR) between the various layers of the stack. Experiments have shown [44-46] that typical TBR values for GeSbTe thin films and Si or SiO_2 substrates lie in the range 10^{-7} to 10^{-8} m^2K/W. Including such TBR effects into the simulations presented here however has little effect, apart from moving the temperature contours in Figs. 2 and 3 to slightly lower voltages. This is most likely because the TiN layer in the medium stack has a low conductivity (3 $Wm^{-1}K^{-1}$), so adding TBR simply makes it a slightly poorer thermal conductor.

Finally, we discuss possible oxidation of the DLC layer. As previously mentioned, DLC films have been shown to be thermally stable up to relatively high temps [32, 33], but such studies are usually carried out in an inert atmosphere or in vacuum. Heating DLC in air, as is the case in this paper, potentially leads to oxidation of the carbon, liberating CO_2. Indeed, experimental studies have shown the weight loss as a result of the oxidation of DLC films to be in the region of 3.8 μg $s^{-1}cm^{-2}$ at 600^0C [47]. At such oxidation rates and temperatures there would be virtually no effect on the DLC capping layer during the typical duration of a write pulse (e.g. if we assume a constant temperature in the capping layer of 600^0C during a 200 ns pulse the volume loss of DLC would amount to only 0.001 nm^3). However, at higher temperatures the oxidation rate is expected to increase significantly. For example, extrapolating the experimentally observed rate in [47] assuming an Arrhenius relationship infers a capping layer volume loss (for a 200 ns pulse) increasing to 0.3 nm^3 at 1000^0C and up to 16 nm^3 at 1500^0C. This might explain why the capping layer has 'disappeared' in the case of Fig. 7(b) (where the predicted maximum temperature in the capping layer is 1500^0C) and also supports our view that an appropriate maximum design temperature for the capping layer is around 1000^0C. We also note that oxidation of the carbon layer during the mark writing process may have contributed to the dearth of published results on the writing of amorphous bits, since a significant loss of carbon (caused by excessive capping layer temperatures in 'un-optimized' media stacks) would degrade the tip-medium contact, making it harder to reach the melting temperature in the phase-change layer.

In summary, a systematic design of practicable media suitable for re-writeable, ultra-high density (> 1Tbit/sq.in.) scanning probe phase-change memories has been presented. The basic design requirements were met by a Si/TiN/GST/DLC structure, with properly tailored electrical and thermal conductivities. Various alternatives for providing a re-writeability function were investigated. In the first case amorphous marks were written into a crystalline starting phase and subsequently erased by re-crystallization, the approach already used in phase-change optical disk memories and PCRAM devices. Our results imply that this method is also appropriate for probe-based memories. However, experimentally the writing of amorphous bits using scanning electrical probes has proved difficult, possibly due to excessive temperatures being developed in the capping layer in previous media stack designs (a problem that should be alleviated using the new designs presented in this paper). In light of this a second approach has been studied, that of writing crystalline bits in an amorphous starting matrix, with subsequent erasure by re-amorphization. With conventional phase-change materials, such as continuous films of $Ge_2Sb_2Te_5$, this approach invariably leads to the formation of a crystalline 'halo' surrounding the erased (re-amorphized) region, having severe adverse consequences on the achievable density. Suppression or elimination of this 'halo' was achieved by the use of patterned media. However, technical and commercial limitations of using patterned media with scanning probe arrays mean that such an approach is not particularly attractive. An alternative method for suppression of the 'halo' was therefore investigated, by using a slow-growth phase-change material. This worked well and may provide a viable route to providing a re-writeability function, assuming appropriate phase-change compositions can be found.

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