Terabit-Per-Square-Inch Data Storage Using Phase-Change Media and Scanning Electrical Nanoprobes

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***Abstract*—A theoretical study of the write, read, and erase processes in electrical scanning probe storage on phase-change media is presented. Electrical, thermal, and phase-transformation mechanisms are considered to produce a physically realistic description of this new approach to ultrahigh-density data storage. Models developed are applied to the design of a suitable storage layer stack with the necessary electrical, thermal, and tribological properties to support recorded bits of nanometric scale. The detailed structure of nanoscale crystalline and amorphous bits is also predicted. For an optimized trilayer stack comprising Ge_2 Sb_2 Te_5 sandwiched by amorphous or diamond-like carbon layers, crystalline bits were roughly trapezoidal in shape while amorphous bits were semi-ellipsoidal. In both cases, the energy required to write individual bits was very low (of the order of a few hundred picoJoules). Amorphous marks could be directly overwritten (erased), but crystalline bits could not. Readout performance was investigated by calculating the readout current as the tip scanned over isolated bits and bit patterns of increasing density. The highest readout contrast was generated by isolated crystalline bits in an amorphous matrix, but the narrowest readout pulses arose from isolated amorphous marks in a crystalline background. To assess the ultimate density capability of electrical probe recording the role of write-induced intersymbol interference and the thermodynamic stability of nanoscale marks were also studied.**

***Index Terms*—Electrical nanoprobes, GeSbTe films, phase-change films, phase-change recording, scanning probe data storage.**

I. Introduction

DATA STORAGE roadmaps are looking toward density targets of around 1 Tb/in^2 by 2008–2010. For magnetic hard-disk-based storage, because of the well-known superparamagnetic "limit," such a target requires significant research and development both in terms of recording materials and system design. In optical disk storage, due to the optical diffraction limit, achieving such a high storage density also remains problematic. It is therefore timely to investigate alternative storage technologies.

A key requirement for any viable alternative Tb/in^2 storage method is the ability to reduce the interaction volume between the "head," which is used for the writing and readout, and the storage medium. Such a tool can be found in scanning probe microscopy where a sharp scanning tip is used to detect and modify on the nanoscale some physical material property. Indeed, IBM has already demonstrated the concept in their "Millipede" system where a thermomechanical probe is used to write, read, and erase indentations on polymer media [1]. The relatively slow write/read process, which depends on the scanning speed, is compensated for by the parallel operation of more than a thousand tips. Such a thermomechancial approach is not the most power-efficient, since, to record a bit, the whole of the scanning tip is heated, which is a relatively large thermal volume compared to the bit volume. Furthermore, polymer media are not the most intrinsically overwritable media. If it were possible therefore to develop a method that uses intrinsically overwritable media and involves direct heating of only that material volume comprising the bit itself, significant benefits might result. The design and performance evaluation of such a system is the aim of this paper. While here the primary concern is a theoretical investigation and computational simulation, experimental results drawing on our findings have been published by co-workers [2]. Other experimental studies of electrical and thermal probe recording onto simple bare films of phase-change materials have also been reported [3]–[6].

Manuscript received June 4, 2005; revised August 17, 2005. This work was supported by the European Union Information Society Technologies Future Emerging Technologies Programme under InProM Project IST-2001-33065.

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Digital Object Identifier 10.1109/TNANO.2005.861400

II. Probe Storage System

A. Storage Architecture

Any storage system comprises a storage medium, write and read transducers, and associated electronics. An attractive medium for rewritable probe recording is one based on chalcogenide materials, such as GeSbTe or AgInSbTe alloys, which have been used for a range of data storage applications in recent years. The most prominent and widespread use of chalcogenides is of course in the rewritable phase-change optical memory disks, such as CD-RW and rewritable DVD formats [7]. Their use in nonvolatile, solid-state, electrical memories [e.g., the so-called ovonic unified memory (OUM) or phase-change RAM (PC-RAM)], is also generating much interest as they offer a possible replacement for conventional CMOS flash memory [8]. All of these memory applications rely on a reversible phase transformation between the amorphous and (poly)crystalline states. In optical disk memories, such phase transformations are brought about by heating with a focused laser beam; readout relies on the differing optical reflectivities of the two phases. In electrical phase-change memory devices, data are written or erased by resistive heating caused by a pulse of electrical current injected into the phase-change

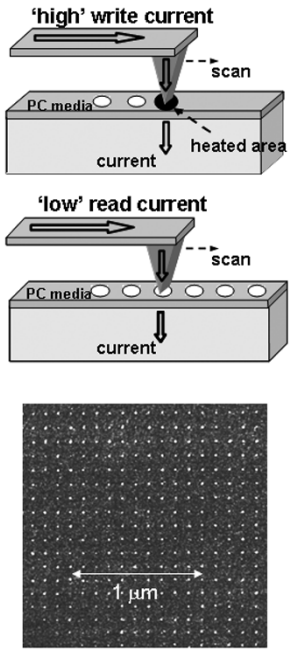

Fig. 1. Schematic of the electrical probe storage system using phase-change media, showing the recording process (top) and the reading process (middle). Also shown (bottom) are experimentally achieved 20-nm crystalline bits written into an amorphous GeSbTe layer in a trilayer stack (this experimental image was obtained by mapping the readout current versus position and is courtesy of Gidon *et al.* CEA-LETI Grenoble, Grenoble, France [2]).

layer. This latter concept may be extended to scanning probe memories by injecting a pulse of electrical current from the tip into the storage medium, resulting in phase transformations by Joule heating, with the readout relying on the differing electrical resistivities of the two phases. This basic scheme is illustrated in Fig. 1.

However, since phase-change materials are generally very sensitive to oxidation, they must be used with protection layers. These layers must present appropriate thermal and electrical properties, allowing the current to flow through the structure and a sufficient temperature increase in the phase-change layer to initiate the phase-change processes, while also supporting sufficiently fast cooling rates for amorphization to occur. Moreover, since the tip scans in contact with the storage medium, the uppermost layer should also be chosen so as to reduce tribological problems. Similarly, for both electrical and tribological reasons, it is prudent to coat the tip itself. Thus, a storage architecture such as that shown in Fig. 2 is envisaged, which comprises a multilayer storage medium on an Si substrate. In this paper, we choose a well-known phase-change material, the $Ge_2Sb_2Te_5$ (GST) alloy, as the active layer, while amorphous or diamond-like carbon films are chosen for the encapsulating layers.

B. Minimum Stable Bit Size

It is pertinent, before we undertake a detailed study of the performance of the proposed storage system, to ask whether nanoscale bits of the size required for Tb/in^2 densities and beyond are likely to be thermodynamically stable in phase-change media. This question can be addressed from the perspective of crystal nucleation and growth. For example, classical nucleation

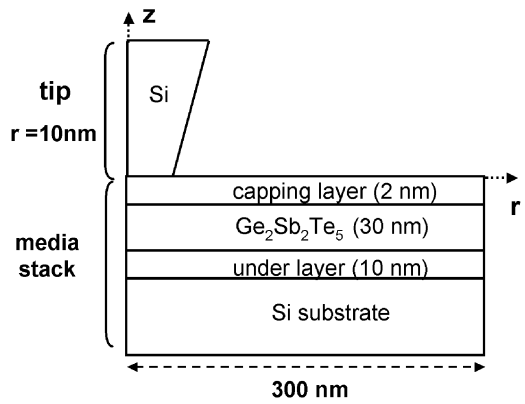

Fig. 2. Two-dimensional (2-D) section of the modeled system; cylindrical symmetry is assumed.

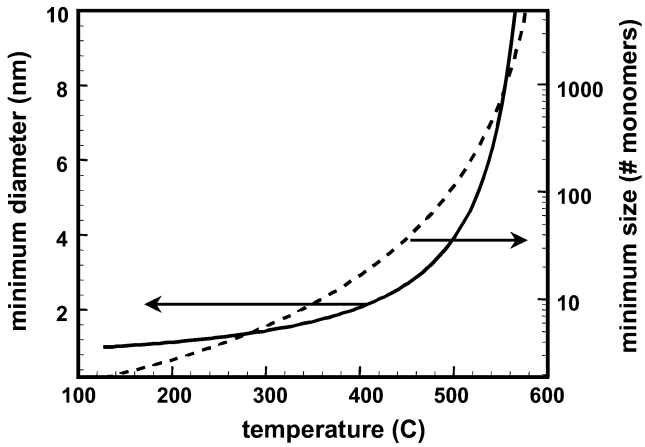

Fig. 3. Predicted minimum stable crystallite cluster size for $Ge_2Sb_2Te_5$ as a function of temperature.

theory can be used to evaluate the minimum stable crystallite cluster size (n_c) as a function of temperature. This minimum stable size results from a balancing of volume and surface energies present when a crystallite grows in an amorphous matrix and classically (for spherical crystallites) is well known to occur at a value

$$n_c = \frac{32\pi\nu_m^2\lambda^3}{3\Delta g^3} \tag{1}$$

where v_m is the volume of the crystalline "species" (which is a "monomer" of GST alloy in this case), λ is the interfacial surface energy density between the amorphous and crystalline phases, and Δg is the bulk free energy difference per monomer. The parameters in (1) have been previously estimated [9] and lead to a variation of the minimum stable crystallite size as a function of temperature, as shown in Fig. 3, where it can be seen that sizes of the order of 2–10 nm are stable over the typical operating temperatures of phase-change storage media. Furthermore, an estimate for the longevity of such nanoscale bits can be found by inspection of predicted crystalline growth rates and incubation times (the time to form a crystallite of critical size in amorphous material). The incubation time τ was estimated following the treatment by Kashchiev [10]

$$\tau = \frac{1}{\pi^3 n_c^{2/3}\gamma Z^2} \tag{2}$$

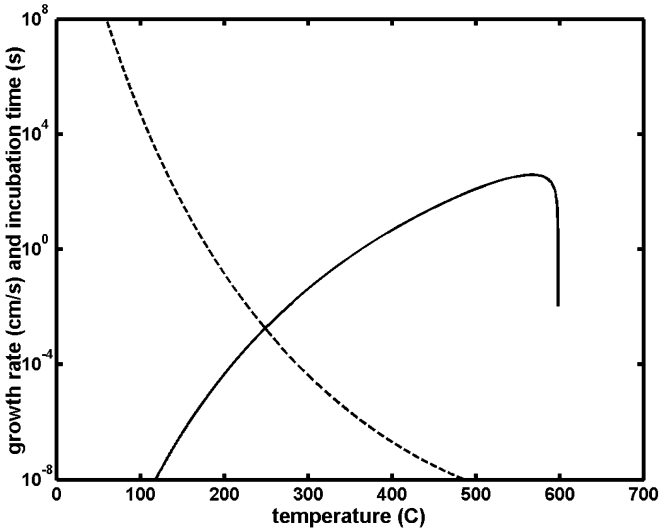

Fig. 4. Predicted incubation times (for the onset of crystallization: dotted line) and growth rates (for a 10-nm radius crystal cluster: solid line) versus temperature for $Ge_2Sb_2Te_5$.

where n_c is as given in (1), Z is the Zeldovich factor, and γ is the molecular jump frequency at the amorphous-crystalline boundary (for a fuller description of these terms, see [9] and [11]; for suitable values of the parameters pertaining to GST, see [9]). Growth rates were calculated according to the approximation of Kelton and Greer [12], assuming a crystal cluster size with radius 10 nm. Results are shown in Fig. 4, where it can be seen that predicted growth rates at moderate temperatures are very low and incubation times are long, so that nanoscale bits in both crystalline and amorphous phases of chalcogenides (or at least in the GST example used here) are predicted to be thermodynamically stable for very long times at archival temperatures.

III. Theoretical Model

The basic physical mechanisms that determine the operation of the scanning electrical probe memory proposed here involve electrical, thermal, and phase-transformation processes. An electrothermal process determines the current flow and resulting temperature distribution during write and erase cycles, with the final bit size and shape also dependent on material parameters, phase-change kinetics, and cooling rates. The readout process is purely electrical, but again depends on material properties and stack design.

The electrothermal processes were described by a system of coupled equations comprising the Laplace equation and heat diffusion equation

$$\nabla(\sigma \cdot \nabla V) = 0 \tag{3}$$

$$\rho C_p \frac{\partial T}{\partial t} - K \cdot \nabla^2 T = \sigma |E|^2 \tag{4}$$

where σ is the electrical conductivity, V is the electrical potential, and ρ, K, and C_p correspond to the density, the thermal conductivity, and the specific heat, respectively. Solving these equations determines the potential, current, heat generation rate, and resulting temperature throughout the storage medium. During writing, reading, and erasing, it was assumed that the tip was stationary above the storage medium. This approximation is not restrictive since, in scanning probe systems, even those designed for storage applications, the tip-medium relative velocity is small (for typical write pulses of a hundred nanoseconds or so, the tip moves only around 0.1 nm during the write cycle even for a fast probe scanning speed of 1 mm $\cdot$ s^{-1}). Thus, circular symmetry was assumed and a full three-dimensional (3-D) simulation reduced to two dimensions. All calculations were performed using a finite-element method in FEMLAB. The applied voltage was connected to the top of the tip (which is roughly equivalent to connecting to the cantilever on which the tip is mounted), while the bottom boundary of the Si substrate was maintained at ground potential. These two boundaries were kept at room temperature while all others were considered electrically and thermally insulated. Values of the parameters introduced in the model are given in Table I.

The electrical conductivity of GST is an important parameter in the model and is in general not constant but depends on temperature and the material phase. Furthermore, in the amorphous phase, there is a significant electric-field dependence of conductivity [13]. Many measurements of the temperature dependence of electrical conductivity of chalcogenides in general and GST in particular have been reported in the literature, with results usually conforming to an Arrhenius relation [14]. Hence, for the crystalline phase, we assumed an electrical conductivity of

$$\sigma_{\rm cryst}(T) = \sigma_{0_{\rm cryst}} \exp\left(\frac{-\Delta\xi_{\rm cryst}}{k_B T}\right) \quad \Omega^{-1}{\rm m}^{-1} \tag{5}$$

where $\sigma_{0\rm cryst}$ is a constant, $\Delta\xi_{\rm cryst}$ is the activation energy, k_B is Boltzmann's constant, and T is absolute temperature. In the amorphous phase, conductivity is described by

$$\sigma_{\rm am}(T,E) = \sigma_{0_{\rm am}} \exp\left(\frac{-\Delta\xi_{\rm am}}{kT}\right) \exp\left(\frac{E}{E_0}\right) \Omega^{-1}{\rm m}^{-1} \tag{6}$$

where $\sigma_{0\rm am}$ is a constant, $\Delta\xi_{\rm am}$ is the activation energy for amorphization, E is the electric field, and E_0 is a (constant) threshold field. The parameters σ_0, $\Delta\xi$, and E_0 were obtained from published values [15]–[18] and fitted to experimental data reported in the literature [14] and are also shown in Table I.

Turning to the study of crystallization, there are several approaches that could be used; for example, classical nucleation theory [19], [20], Johnson–Mehl–Avrami–Kolmogorov (JMAK) kinetics [21], [22], cellular automata approaches [23], [24], and rate-equation methods [9], [11]. For our purposes, and primarily as a tradeoff between complexity and computational efficiency, the JMAK approach was adopted, but with a modification to reflect the nonzero incubation time described in (2). Thus, the fraction of material crystallized as a function of time $\chi(t)$ is given by

$$\chi(t) = 1 - \exp(-x_e)$$

where

$$x_e = \left[\sum_t K_{\rm JMAK} \cdot (t - \tau)\right]^n, \qquad t > \tau \tag{7}$$

TABLE I
CHARACTERISTIC PARAMETERS USED IN THE SIMULATIONS

	Tip	Capping layer	GST (a/c)	Bottom electrode	Si substrate
Thickness (nm)		2	30	10	50
Density ρ (kg m^{-3})	2330	2800	6150	2800	2330
Heat capacity C_p (J kg^{-1} K^{-1})	720	540	210	540	720
Thermal conductivity K (W m^{-1} K^{-1})	149	100	0.2/0.58	100	149
Electrical conductivity σ (Ω^{-1} m^{-1})	10000	50	$\sigma_{am}(T,E)$ or $\sigma_{cryst}(T)$ as Eq. (4) or (5) with $\sigma_{0am}=1.88\text{x}10^4\ \Omega^{-1}$ m^{-1} $\Delta\xi_{am}=0.32$ eV $\sigma_{0cryst}=1.5\text{x}10^4\ \Omega^{-1}$ m^{-1} $\Delta\xi_{crys}=0.04$eV $E_0=5\text{x}10^7$ Vm^{-1} (unless stated otherwise)	100	100
Crystallization parameters			As in Eqs. (6)-(8) with n = 2.6 $\nu = 1.5\text{x}10^{22}$ s^{-1} $\xi_A = 2$eV		

where τ is given as in (2), t is the time elapsed, n is the Avrami factor, and K_{JMAK} is the crystallization rate given by

$$K_{\mathrm{JMAK}} = \quad \nu \exp\left(-\frac{\xi_A}{k_B T}\right) \tag{8}$$

where ν is a frequency factor and ξ_A is the activation energy for crystallization. Table I again summarizes the parameters used.

During the GST crystallization process, the electrical and thermal conductivities of the GST layer will change. To account for the variation of the properties of the material during the crystallization process, percolation theory (effective medium theory) can be used to track the changes in material properties as the transformation progresses [25]. Percolation theory shows that there is a sharp increase of the electrical conductivity as soon as the fraction of conductive material exceeds a certain percolation threshold, which is typically when 15%–20% of the material is transformed. During our calculations, therefore, the values of the electrical and thermal conductivities of GST (in a particular simulation cell) were changed from the amorphous to the crystalline values when the fraction of crystalline material exceeded 15%.

In order to amorphize the GST material, two conditions must be fulfiled. First, the temperature must reach the melting temperature, which, in the case of $Ge_2\,Sb_2\,Te_5$, is 630 °C. Second, there must be a very high cooling rate to prevent any recrystallization during the cooling process. In the literature, cooling rates greater than 10 °C · ns $^{-1}$ are often quoted as necessary for amorphization of GST [26]. For a more precise analysis, the modified JMAK approach of (7) was used here to calculate the fraction of crystallized material generated during cooling of any melted region.

IV. WRITE, READ, AND ERASE PROCESSES

A. Design of the Storage Stack Layers

Before proceeding with a study of the write, read, and erase processes themselves, it was necessary to design the capping layer and the underlayer to enable a sufficient temperature increase in the GST layer to amorphize or to crystallize the material, while at the same time yielding good tribological properties. To maintain good electrical contact while scanning and, at the same time, provide protection against wear and corrosion, amorphous or diamond-like carbon material was chosen for both the capping and underlayer. A parametric study was performed to find appropriate thickness and the electrical conductivity of these two layers, monitoring the maximum temperature in the GST layer when the system reached the steady state. For this study, the GST electrical conductivity was considered constant and equal to 1000 $\Omega^{-1} \cdot \mathrm{m}^{-1}$, and a 10-V potential was applied between the tip and substrate. The results are plotted in Fig. 5. The capping layer greatly influences the electrothermal process since the maximum temperature in the GST layer ranges from 100 °C to 2000 °C as the capping layer thickness and electrical conductivity are varied between 1–5 nm and between 1–100 $\Omega^{-1} \cdot \mathrm{m}^{-1}$, respectively. To achieve the required temperatures for crystallization and amorphization, a capping layer with a thickness of less than 3 nm and a conductivity greater than 30 $\Omega^{-1} \cdot \mathrm{m}^{-1}$ appears to be suitable. The underlayer plays only a minor role in the maximum temperatures achieved, with a variation of only 55 °C predicted for the range of thickness from 2 to 30 nm and conductivity from 100 to 1000 $\Omega^{-1} \cdot \mathrm{m}^{-1}$. Note, however, that the underlayer does play an important current limiting role by providing a finite series resistance to the system. Based on these results, the "optimum" thickness and conductivity of capping and underlayer were chosen as 2 and

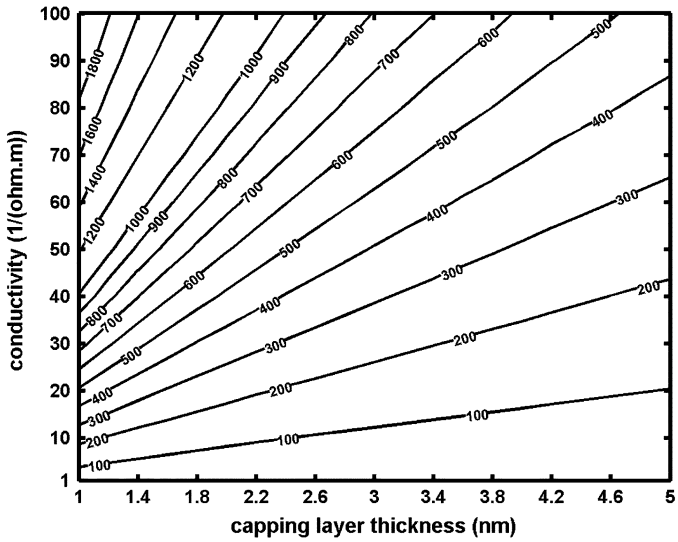

Fig. 5. Variation of maximum temperature in the GST layer as a function of capping layer thickness and electrical conductivity (contours show temperature in °C). A 10-V potential was applied to the tip and the GST conductivity was assumed to be constant at 1000 $\Omega^{-1}\cdot m^{-1}$.

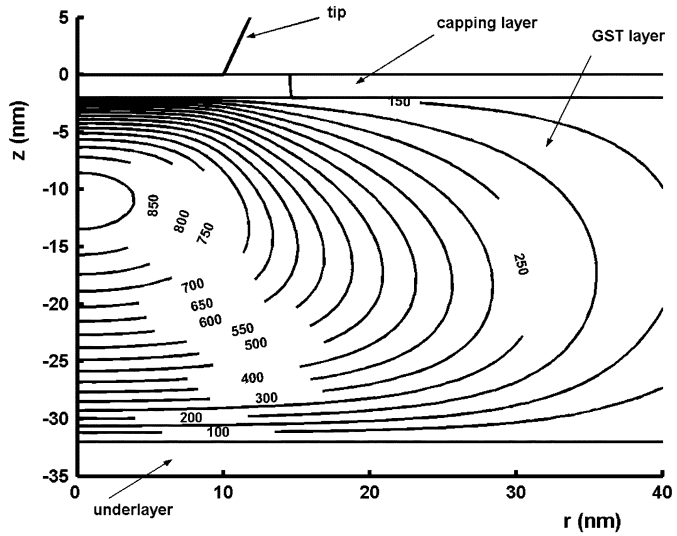

Fig. 6. Temperature distribution (°C) in an initially amorphous GST layer 100 ns after the application of a 10-V pulse (the result does not include modeling of the phase-change process itself).

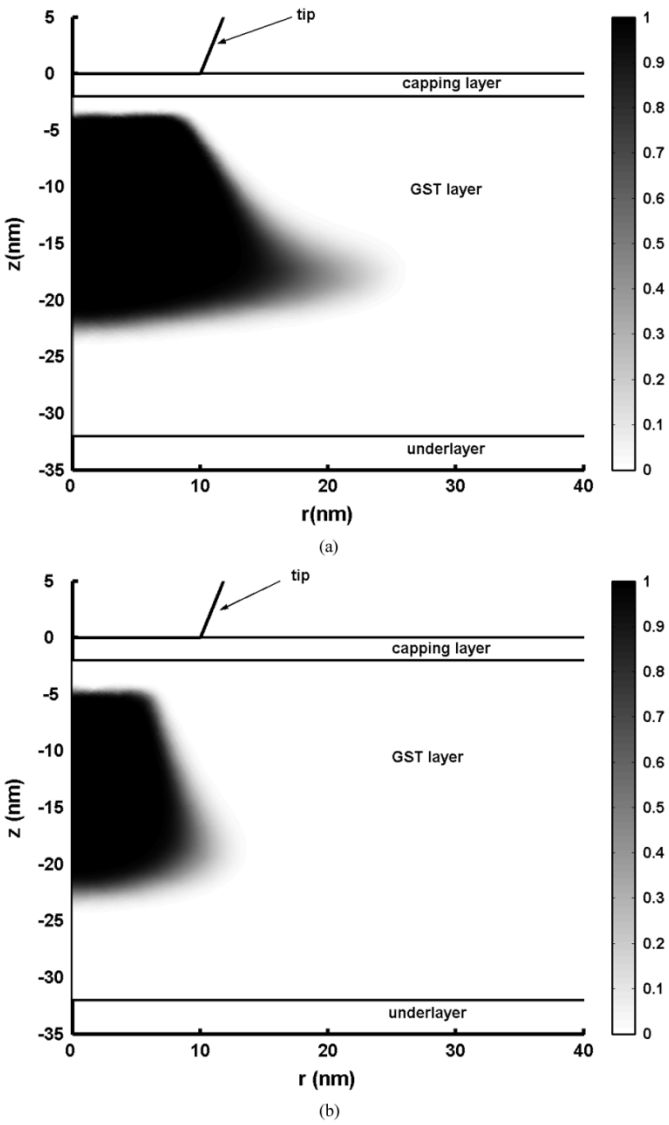

Fig. 7. Simulated written crystalline bits after the application of: (a) a 10-V (top) and (b) a 6.5-V pulse (bottom) of 200-ns duration. The grayscale refers to the fraction of crystallized material.

10 nm and 50 and 100 $\Omega^{-1}\cdot m^{-1}$, respectively. In practice, the conductivity of the carbon layers can be controlled by doping (e.g., with boron) during deposition.

B. Writing Process

There are two alternative writing strategies: writing crystalline bits in an amorphous matrix or amorphous bits in a crystalline background. Here, we consider each in turn.

In general terms, rapid crystallization of chalcogenides requires heating above the glass transition temperature (145 °C for GST). It can be shown, using (2) and (7), that a temperature of about 400 °C must be reached in order to fully crystallize ($\chi \approx 1$) amorphous GST in a few hundreds of nanoseconds (which is the kind of timeframe that is required to ensure reasonable data rates). A 10-V pulse of 200-ns duration was here found sufficient to reach such temperatures. The temperature distribution in the structure 100 ns after the application of such a pulse is shown in Fig. 6 (without introducing the phase-change process such that the GST layer remained amorphous throughout). The isothermal contours spread through the thickness of the GST layer, and a maximum temperature of 850 °C is reached approximately 10 nm below the top of the GST layer. Including the crystallization process in the simulation, as described by (7), results in the written bit shape as shown in Fig. 7(a); the bit follows the shape of the isothermal lines but does not permeate the whole thickness of the GST layer. The lateral spread of the written dot, particularly in the lower part of the GST layer, can be reduced by reducing the applied voltage, thus constraining the temperature distribution (and reducing the maximum temperature). A pulse of 6.5 V, for example, results in a written bit as shown in Fig. 7(b).

As already discussed, the electric-field dependence of the conductivity of amorphous GST plays a critical role in the crystallization process. Results presented so far assumed a threshold field E_0 of 5×10^7 V·m^{-1}. However, the maximum temperature reached by the GST layer is greatly dependent on E_0. From a critical field of 2×10^6 V·m^{-1}, the maximum temperature increases progressively until it reaches a maximum value of around 1000 °C for E_0 of 1.7×10^8 V·m^{-1}, after which it decreases sharply (since such high threshold fields are not achieved in the writing process). Naturally, the resulting crystallized area also depends on the value chosen for E_0, with the size of the crystallized region increasing as E_0 increases. However, except for very low values of the threshold field ($E_0 < 10^7$ V · m^{-1}), the general shape of the written bit is maintained, having a roughly trapezoidal shape and extending closer to the top boundary of the GST layer than to the bottom. Although the choice of an appropriate threshold field in chalcogenides has been discussed in the literature [13], [27], [28] (and suggests a value in the range 10^6–10^8 V·m^{-1}), the exact nature of the electric-field dependence is not known, and care should be exercised when interpreting results based on an arbitrarily chosen E_0.

The amorphization process requires heating above the melting temperature (630 °C for GST) together with rapid cooling. To achieve such temperatures, a writing pulse of 15 V was used here, again of 200-ns duration. Fig. 8(a) shows the resulting temperature distribution in the structure after 100 ns; the isothermal contours spread more laterally, and the hottest area is localized at the top of the GST layer. The shape of the resulting amorphous dot is thus expected to be different to that of the previous case.

Prior to any analysis to determine the actual shape and size of any written amorphous bit, we evaluated the effective cooling rate that had to be achieved to avoid recrystallization. For this, (7) was used to monitor the fraction of crystallized material $\chi(t)$ during the cooling process. The initial temperature of the whole GST layer was set at the melting point then cooled to ambient using a range of constant cooling rates (i.e., linear decrease in temperature). The results showed that a cooling rate in excess of about 37 °C · ns^{-1} is necessary to quench the GST layer into its amorphous phase. This is not out of line with values quoted in the literature [26]. Of course, in the real system, the cooling rate is not linear and depends on the layer structure, material properties, and sharpness of the trailing edge of the applied voltage pulse. To assess the influence of the pulse characteristics, we investigated three pulse shapes, two having exponential leading and trailing edges ($V(t) \propto (1 - \exp(-t/\tau))$) with fall times of 20 and 10 ns, respectively, whereas the third had linear leading and trailing edges and a fall time of 20 ns. The maximum applied voltage was in each case 15 V. The resulting maximum cooling rates obtained in the GST layer were 22 °C/ns, 45 °C/ns, and 85 °C/ns, respectively. Amorphization is therefore not expected for the first pulse (having an exponential fall time of 20 ns), but may be possible with either of the other pulses. However, further analysis showed that even the pulse with the 10-ns exponential trailing edge resulted in full recrystallization ($\chi = 1$) on cooling. The pulse with the linear trailing edge, however, resulted in complete amorphization (χ remained zero throughout cooling). These results are explained in Fig. 9, where the temperature and cooling rate in the GST layer (at a point directly below the tip and close to the capping layer interface) for these cases are shown. For the exponential trailing edge, as the temperature drops below melting, the cooling rate is only at 25 °C · ns^{-1} and, as a result, the GST material solidifies in the crystalline state. On the other hand, the linearly decaying voltage pulse exhibits a cooling rate in excess of the "critical" value of around 37 °C · ns^{-1} from the outset, with the temperature in the GST layer dropping significantly (to around 100 °C) before the cooling rate falls below the critical value. Therefore, full amorphization is to be expected in this case.

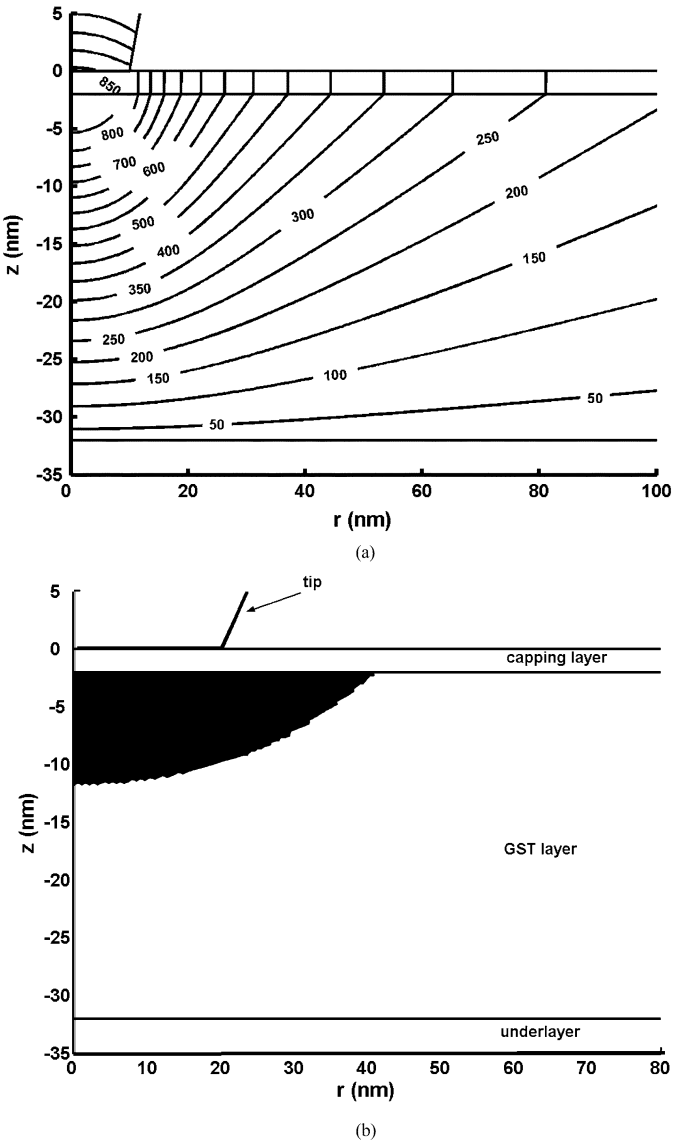

Fig. 8. (a) Temperature distribution (°C) in an initially crystalline GST layer 100 ns after the application of a 15-V pulse (result does not include modeling of the phase-change process itself). (b) Simulated written amorphous bit after the application of a 15-V pulse of 200-ns duration.

Having determined the conditions for amorphization, a 15-V pulse of 200-ns duration with a linear trailing edge of 20 ns was applied to the previously designed layer structure of Fig. 2. The resulting amorphous bit, shown in Fig. 8(b), is localized at the top of the GST layer and has a semi-ellipsoidal shape, which reflects the temperature distribution.

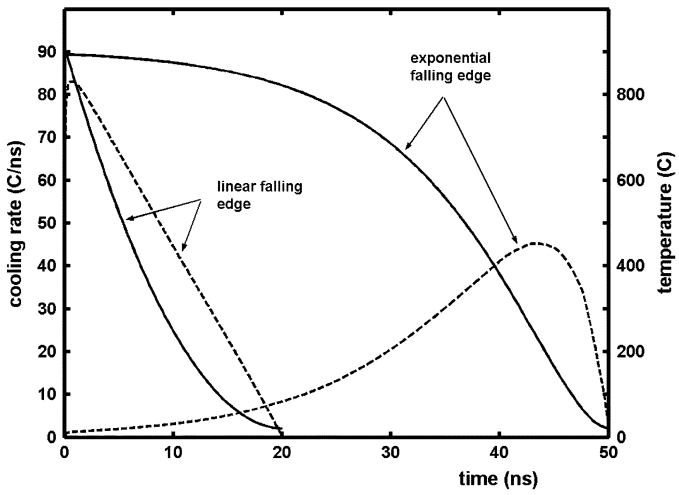

Fig. 9. Variation of the cooling rate (dashed line) and the temperature (solid line) with time, taken at a particular point at the top of GST layer just below the tip, during the cooling from 630 °C for an exponential decrease of the applied voltage and a fall time of 10 ns and a linear decrease of the applied voltage with a fall time of 20 ns.

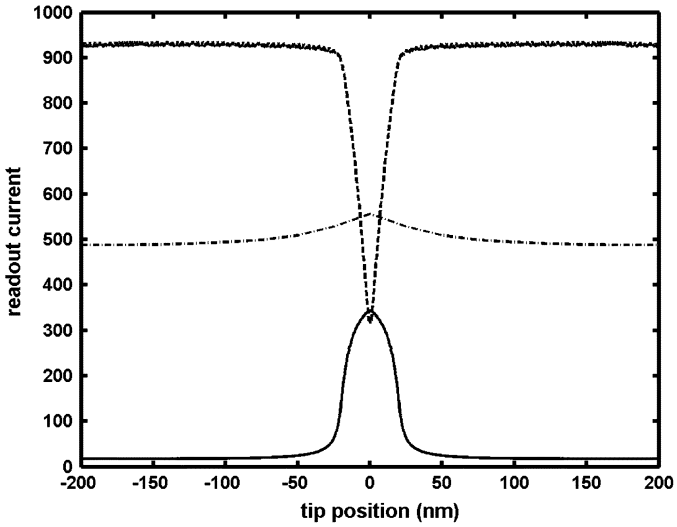

Fig. 10. Readout signals from a single dot in the three configurations: crystalline dot embedded in GST layer (dash–dotted line); crystalline dot through the whole thickness of the GST layer (solid line); and amorphous dot at the top of the GST layer (dashed line). The applied voltage is 4 V, and the electrical conductivity of the capping layer is 50 $\Omega^{-1} \cdot \mathrm{m}^{-1}$. Note that the readout current scale is in Amps per meter track width, and that results for the first case have been scaled by 10× to enable plotting on a single graph.

C. Readout Process

As was already discussed, the readout process relies on the vastly differing electrical conductivities of the amorphous and crystal phases of the GST layer. In the simplest readout process, as treated here, a constant voltage is applied between the tip and the substrate, and the resulting current provides the readout signal. The applied voltage is much reduced from that in the recording process, so that any heating is negligible.

To maintain computational tractability, the investigation of the readout process is here limited to two dimensions, which is equivalent to considering the cross-track dimension as being infinite. Written bit shapes were idealized versions of those revealed by the write process simulations presented above. Crystalline bits were thus assumed to be rectangular in shape, extending either throughout the whole GST layer or, as predicted by the recording simulations, being surrounded top and bottom by residual amorphous material. The amorphous dots were assumed to be semi-ellipsoidal and localized to the upper portion of the GST layer. The electrical conductivities of the crystalline and the amorphous states were considered to be constant and equal to 1000 and 0.1 $\Omega^{-1} \cdot \mathrm{m}^{-1}$, respectively. The tip was scanned over the written bit structures and the Laplace equation was solved at each tip position to determine the current flowing, with a constant voltage of 4 V being applied between tip and substrate. Fig. 10 represents the response of the system to a single 20-nm-wide bit for the three configurations. The three signals exhibit different average current levels, depending on the relative proportion of crystalline and amorphous material beneath the tip. Note that, for the 2-D analysis presented here, the signals correspond to readout current per unit length in the cross-track direction. A parameter that is often used to compare such signals with very different average values is the contrast. Defining the readout contrast in terms of maximum and minimum current values as $(I_{\max} - I_{\min})/(I_{\max} + I_{\min})$, the three configurations present readout contrast of 0.90, 0.07, and 0.50, respectively. The best configuration in terms of readout contrast is thus the crystalline dot spreading through the whole thickness of the GST layer. However, the width of the readout pulse is also important and plays a key role in determining the achievable readout resolution. Normalizing each readout pulse enables a direct comparison of pulse width, whereby the sharpest response (narrowest pulse) is obtained with the semi-ellipsoidal amorphous bit.

In a real system of course, a succession of data bits is readback and not just isolated marks. To study the effect of this on the readout signal, we calculated the readout current for a periodic series of 20-nm-wide crystalline (with the crystalline marks extending through the entire GST layer) or amorphous marks, which are separated by spaces ranging from 100 to 2 nm. The results are shown in Fig. 11, where the narrower pulses from the amorphous marks more than compensate for their lower contrast when bits are closely spaced. However, it should be noted that, if tracks are separated by crystalline regions (as would be the case for a crystalline starting matrix), then the intertrack region would act as a current-sink via the low resistance (compared with the amorphous mark) of the capping layer, thus reducing considerably the contrast observed here for the amorphous marks.

D. Erasing Process

A possible advantage of using phase-change materials in scanning probe memories is their inherent rewritability. To assess the capabilities in this respect of the scanning electrical probe memory proposed here, we performed studies of the erasing process where we tried to overwrite both crystalline and amorphous bits. The principle of the erasing process is based on the same electrothermal mechanism inherent to the writing process. A voltage pulse is applied to the tip and the coupled Laplace and heat equations [(3) and (4)] solved for the system, with phase transformations being described by (7) and (8) and

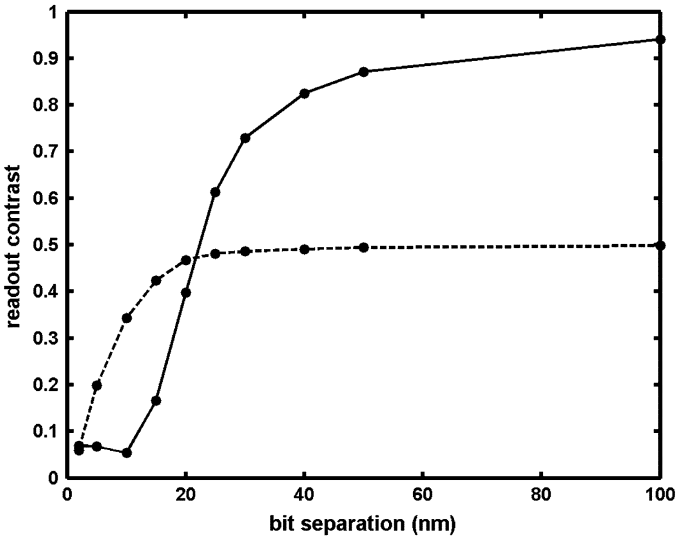

Fig. 11. Readout contrast as a function of bit spacing for (solid line) crystalline bits through the whole thickness and amorphous bits (dotted line) at the top of the GST layer. The size of the bits is maintained at 20 nm while the bit-to-bit spacing is varied.

GST conductivities by (5) and (6). The tip is assumed to be static over the center of any bit it is trying to erase.

The erasing process of a crystalline bit will be completed if it can be heated up to the melting temperature and subsequently cooled at a sufficiently high rate to result in amorphization. Naturally, this has to be realized without altering the phase (crystallizing) of any of the surrounding amorphous matrix. The first configuration considered is thus that of a trapezoidal crystalline bit surrounded on all sides by amorphous material and of 20-nm width at its upper boundary, which is 3 nm from the top of the GST layer [see Fig. 12(a)]. Electrothermal simulations showed that approximately 12 V was necessary to reach the melting temperature (630 °C) inside the crystalline bit. However, as shown in Fig. 12(a), the amorphous material surrounding the bit is also heated significantly (greater than 400 °C), and, once crystallization kinetics are introduced into the simulation, the crystallized region actually grows in size rather than being erased [see Fig. 12(b)]. This behavior remained much the same with different sizes and shapes of crystalline bits (embedded entirely within the amorphous matrix or spreading through the whole thickness of the GST layer). Thus, it appears that overwrite of crystallized marks by the electrical probe is problematic, at least for the layer structure proposed here.

To study the erasing of an amorphous bit, we considered primarily the semi-ellipsoidal bit shapes predicted by the write simulations. Erasure should be possible if the amorphous dot can be heated up to a temperature of approximately 400 °C, thus allowing its recrystallization in a few hundreds of nanoseconds, while the surrounding crystalline material can be kept below the melting temperature to prevent amorphization. Before considering any phase-change process, the temperature distribution was determined to see if these conditions might be met. The results obtained with a voltage of 10 V and a radius and thickness of the dot of 15 and 10 nm, respectively, are presented in Fig. 13(a); the temperature rise is well localized inside the dot, and the required temperatures of 400 °C or above in the

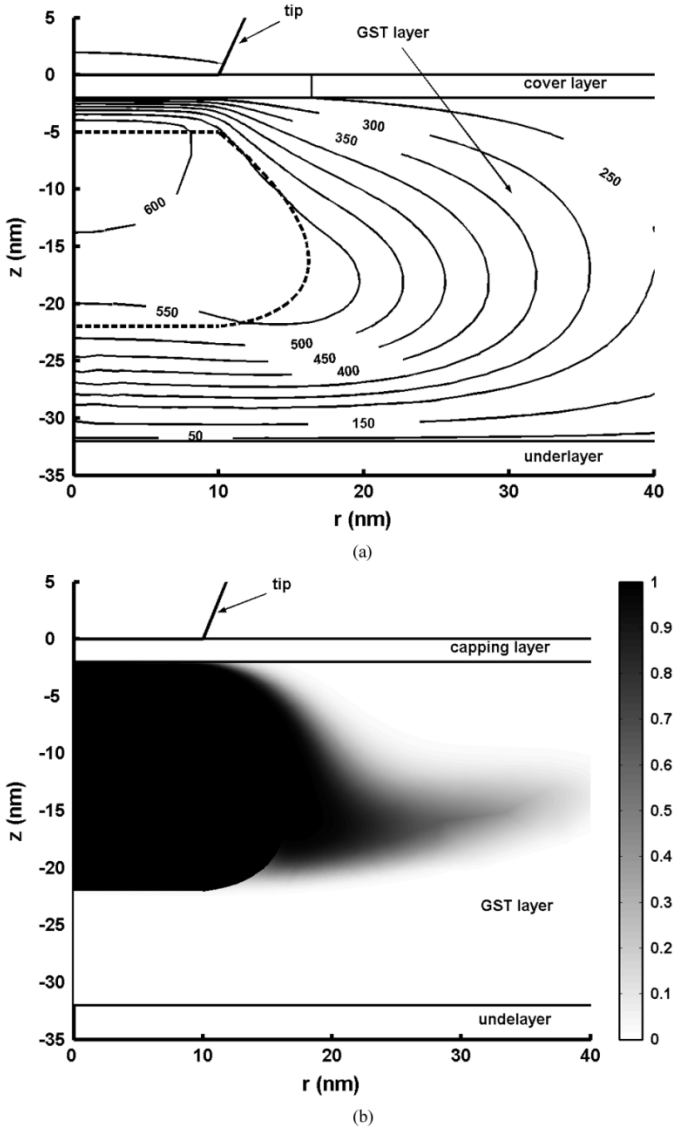

Fig. 12. Simulation results for the erasing of an isolated crystalline bit embedded in amorphous GST layer. (a) Temperature distribution 100 ns after the start of a 12-V pulse of 200-ns duration. (b) Fraction of crystalline material at the end of the erasing process. The position of the preexisting crystalline bit is shown by the dotted lines in (a) and a solid black region in (b). The grayscale refers to the fraction of crystallized material.

amorphous region are easily reached. Adding the phase-transformation kinetics to this simulation results, in this case, in recrystallization of all but the outer boundary of the amorphous bit [see Fig. 13(b)], since there the temperature only reached about 350 °C. Increasing the tip voltage slightly (or extending the pulse duration) resulted in complete erasure.

V. Discussion

The simulations presented have shown that it should be possible to write, read, and, under some circumstances, erase bits of nanometric size using a scanning electrical probe. The writing of both crystalline bits in an amorphous matrix or amorphous bits in a crystalline matrix should be possible. Since the electrical conductivities of amorphous and crystalline phases differ by several orders of magnitude, the electrothermal processes

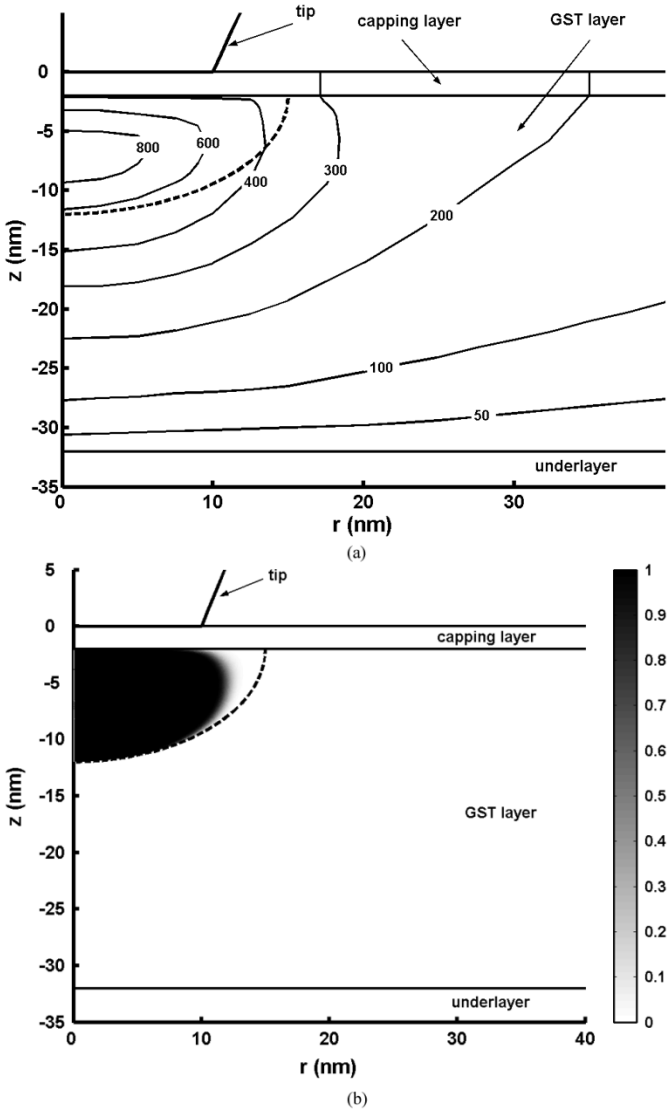

Fig. 13. (a) Temperature distribution (100 ns into a 200-ns 10-V pulse) during the erasing of an amorphous dot. (b) Fraction of crystalline material at the end of the erasing process of an amorphous dot for a 10-V pulse of 200-ns duration. The lateral radius of the original amorphous mark was 15 nm and the vertical depth of the mark was 10 nm; its position is shown by the dashed lines in (a) and (b). The grayscale refers to the fraction of crystallized material.

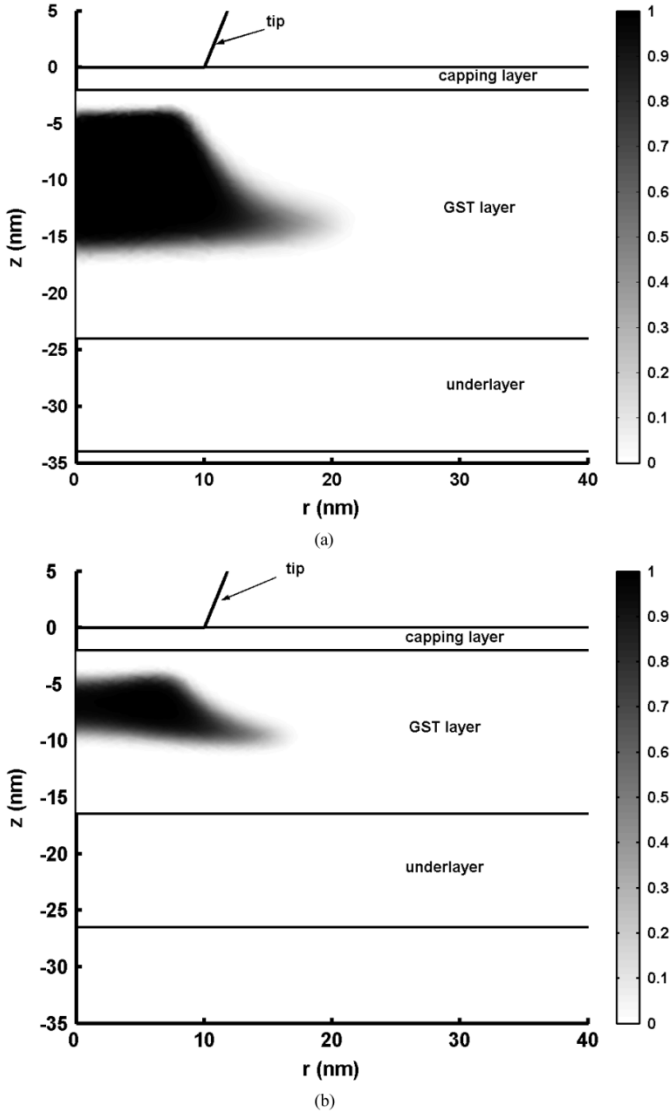

Fig. 14. Simulated crystalline bits in a trilayer stack for different GST layer thicknesses of (a) 20 nm and (b) 15 nm. A 10-V 200-ns write pulse is used in each case. For the result using a 30-nm GST layer, see Fig. 7. The grayscale refers to the fraction of crystallized material.

that take place during the writing process of crystalline and amorphous dots are very different in terms of the electric field and temperature distributions produced in the whole structure. The crystallization and the amorphization processes also differ in their respective temperature and voltage requirements. All of these aspects have repercussions on the size and shape of written bits and on the feasibility of erasability. All of these factors should be taken into account in trying to select which approach is most suitable for practical implementation. For example, during the writing of an amorphous bit, the magnitudes of the electric fields and temperatures in the capping layer are very high (for example, 900 °C and 14×10^9 V · m $^{-1}$ for the simulation presented in Fig. 8), and this may have adverse effects on the integrity and longevity of the storage medium in this case. In either writing scheme, we note that the power consumption is predicted to be extremely low, which may represent one of the major advantages of this electrical probe storage technique. Indeed, less than 100 (for 6.5 V) and 300 pJ (for 12 V) were needed to write a crystalline bit and an amorphous bit, respectively. This compares with around 1–10 nJ for the IBM Millipede system [1], [29].

An interesting result of the writing simulations is the prediction that neither a crystalline bit nor an amorphous bit extend throughout the entire 30-nm-thick GST layer used so far. This is seen subsequently to reduce the readout contrast ratio. It is therefore reasonable to ask if the storage layer stack design can be modified in some way so as to increase the depth of the recorded bits. A first suggestion might be to decrease the thickness of the GST layer. However, decreasing the layer thickness had little effect on bit shape, at least for the case of writing crystalline marks, as shown in Fig. 14. This is in part due to the properties of the carbon capping and underlayers that are characterized by a much higher thermal conductivity than the GST layer and act as good heat sinks. Thus, the bottom and/or the top of the GST

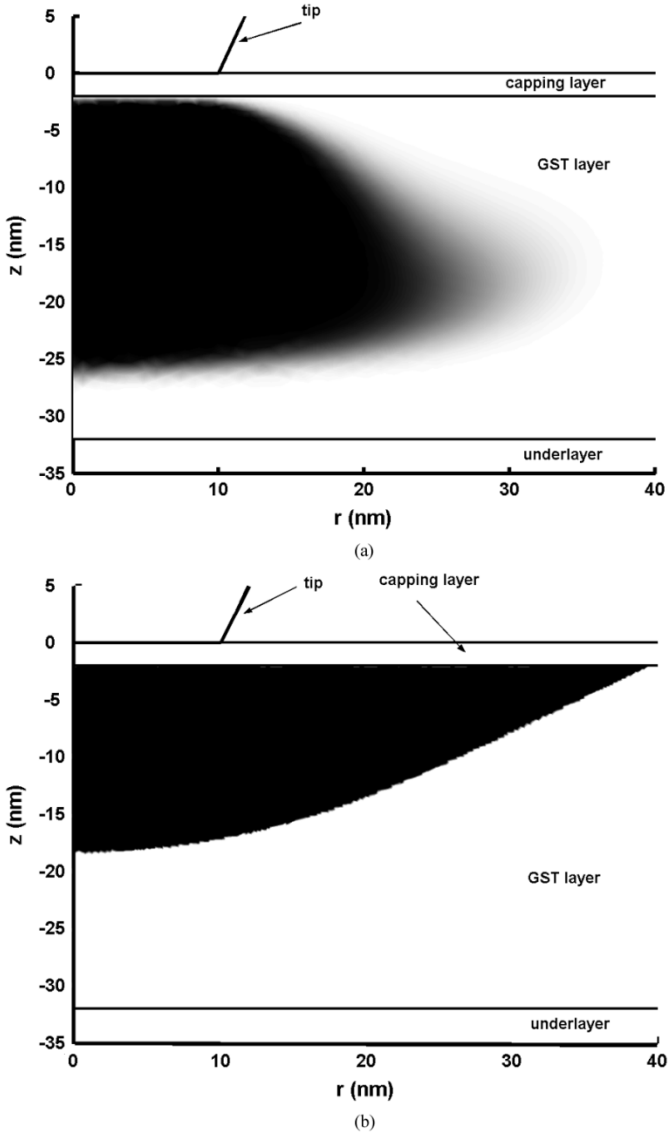

Fig. 15. Effect of the introduction of an additional 100-nm-thick thermal control underlayer on the vertical and lateral spread of: (a) crystalline bits and (b) amorphous bits. For the equivalent result without a thermal underlayer, see Figs. 7 and 8(b), respectively.

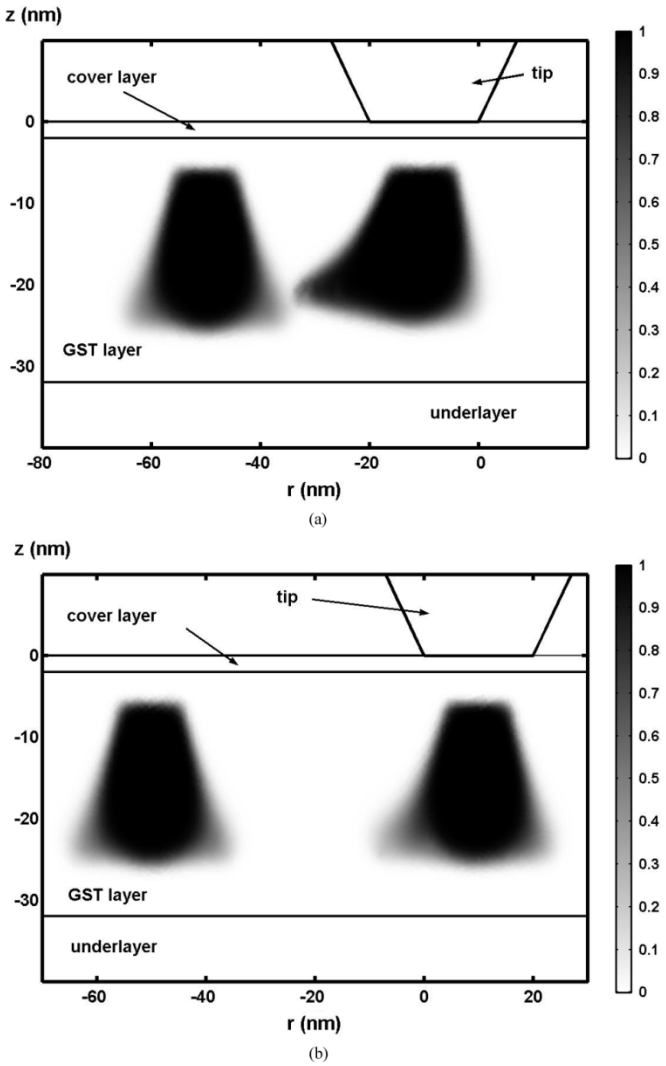

Fig. 16. Effect of write-induced ISI on recorded crystalline bit structure. (a) Effect of writing a second bit 40 nm away from a preexisting bit. (b) Result of increasing the spacing to 60 nm. A 6-V 200-ns writing pulse was used in all cases.

layer cannot be sufficiently heated up to initiate or sustain the crystallization in time scales required in this case.

An alternative approach to increase the spread of the dots through the thickness of the GST layer might be to reduce the heat dissipation via the carbon layers by introducing an additional layer with lower thermal conductivity between the bottom electrode and the substrate. However, this thermal layer should retain sufficiently high electrical conductivity so as not to reduce the current flows too much. These requirements can be satisfied by a crystalline GST layer that is sufficiently thick to remain permanently crystallized during the writing and erasing processes. Introducing such a layer (100 nm thick) did indeed increase the vertical extent of both the crystalline and amorphous dots, as shown in Fig. 15. The crystalline bit now reaches the top of the GST layer, while both amorphous and crystalline bits extend deeper into the GST layer. However, as would be expected, restricting the vertical heat flow increases the lateral heat flow, thus increasing the lateral size of the recorded dots.

In the simulations presented here, a dominant factor in determining the size of all written bits was the tip-sample contact area. Here, we used a 10-nm tip contact radius, and this resulted in bits that were at least 10 nm in radius, but usually more. Since the size and shape of the tip determines to a large extent the size and shape of the electrical field, and thus the nature of the resulting current flow, this is not unexpected. We did not, unlike some previous studies [3], [5], see here a very strong dependence of bit size on GST film thickness. However, our study includes the important contribution of capping and underlayers to the electrothermal process, while these previous studies have been on simple monolayers of GST.

While determination of the size of the smallest isolated bits that can be recorded with a particular storage system plays a critical role in determining the storage density that may be achieved, it is also important to consider the effects of intersymbol interference (ISI) during writing, i.e., how a previously

written mark affects the writing of a subsequent mark. This limits how closely marks may be spaced to each other, so also affecting achievable density. Fig. 16, for example, shows the effect of recording a crystalline bit separated from a preexisting mark by 40 and 60 nm. Clearly, to avoid any write-induced ISI requires a bit separation, in this case, of at least 60 nm. Such large separations will have a detrimental affect on storage density and will influence the proper choice of channel codes (e.g., a suitable RLL code).

System resolution will also depend on the resolution of the readout process. This again will depend a great deal on the size and shape of the readout probe contact area. However, the results presented here also show that the greatest readout contrast should be expected from crystalline bits written on an amorphous background, but that the readout pulse width is significantly narrower for amorphous bits on a crystalline background. This is directly a result of the different bit shapes and vastly differing conductivities in the two cases. Ultimately. of course, the readout resolution will be determined by the system signal-to-noise ratio; this requires a detailed understanding of the system noise, a study of which is beyond the scope of this paper.

VI. Conclusion

A physically realistic theoretical model of electrical probe recording on phase-change media, specifically $Ge_2\ Sb_2\ Te_5$ alloys, has been developed and includes electrical, thermal, and phase-transformation kinetics. The model has been used to design a storage medium that is practically feasible insomuch that it supports rapid crystallization and amorphization while at the same time incorporates protective layers for the GST material. The model has been used to investigate in detail, for the first time, the write, read, and erase processes in this novel type of probe storage format.

An optimum stack arrangement to allow for both crystallization and amorphization (hence both writing and erasing), while at the same time providing good readout performance together with suitable corrosion and tribological properties, was found to be a trilayer arrangement comprising an amorphous or DLC-type carbon underlayer of thickness of 10 nm and conductivity of 100 $\Omega^{-1} \cdot \mathrm{m}^{-1}$, a GST layer with thickness in the range 10–30 nm, and a capping layer of carbon with a thickness of 2 nm and conductivity 50 $\Omega^{-1} \cdot \mathrm{m}^{-1}$.

Using this storage medium structure, it was possible to record crystalline or amorphous marks with sizes in the range 10–30 nm, assuming a tip contact radius of 10 nm. The two types of marks have different shapes, with the crystalline mark being embedded in the GST layer and roughly trapezoidal, while the amorphous mark is semi-ellipsoidal and is located at the top of the GST layer. These differences reflect the different electric field and temperature distributions obtained in the initial amorphous or crystalline matrix. The writing of crystalline bits in an amorphous starting layer was strongly influenced by the electrical field dependence of the amorphous-phase electrical conductivity, that, in practice, probably arises due to avalanche or trap filling electronic processes [30]. The use of a thermal underlayer, which, in this instance, was a thick and "permanently" crystalline GST film, to modify the size and shape of the recorded bits, in particular to extend vertical bit dimensions further through the active GST storage layer, was also investigated. This indeed proved possible and led to a consequent increase in readout contrast, but at the expense of increased lateral spread of the written mark. The size of the tip contact area played a dominant role in determining the lateral size of all recorded marks and, hence, the achievable storage density. The simulations showed that the writing of both crystalline and amorphous bits requires relatively little energy of less than 100 and 300 pJ respectively. This is a result of the fact that the media is heated directly rather than indirectly by heat flow from a heated tip. It was found that direct erasure of individual amorphous bits was predicted to be feasible. Experimentally bits of the order of 15 nm in diameter have been successfully written and read repeatedly by coworkers in a storage layer based on the trilayer media designs presented here [2]. Other researchers have successfully recorded 10-nm crystalline marks, albeit with very limited stability [3]–[5].

Turning to the readout process, it was shown that the greatest contrast should be achieved with (isolated) crystalline marks in an amorphous background. However, the readout resolution, in terms of the readout pulse width, was superior for the case of an (isolated) amorphous bit in a crystalline background. This is a result of the vastly differing electrical conductivities of the two phases and its effect on the current flow, rather than on any significant difference in lateral bit dimensions in the two cases.

Finally, in terms of storage density, it was found that isolated bits in the range 15–30 nm in diameter were predicted to be routinely achieved in our proposed trilayer storage medium, for a tip with a contact diameter of 20 nm. Using 20-nm bits and a simple nonreturn-to-zero encoding scheme yields a storage density of over 1.5 Tb/in^2. Reducing the contact tip area is predicted to reduce the size of the written marks, and, from a thermodynamic point of view, marks as small as 5 nm in diameter are predicted to be stable. Thus, electrical probe recording on phase-change media should provide a feasible and practicable route to rewritable storage at Tb/in^2. densities and beyond.

Acknowledgment

The authors would like to thank all of their collaborators on this project for invaluable discussions, in particular S. Gidon, Y. Samson, and O. Bichet from CEA-LETI, Grenoble, France. The authors also thank S. Senkader, formerly with Exeter University but now with Oxford University, in particular for illuminating discussions concerning the results for Figs. 3 and 4.

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