Starved picowatt oscillator for remote sensor wake-up timer

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A sub-nanowatt oscillator is described. The oscillator is intended for a wake-up timer for remote sensors and hence trades frequency accuracy for reduced power consumption. It is constructed from a five-stage ring of inverters in which the switching speed is reduced using transistors that are always-off, or starved. Fabricated in a 0.35 μm process, the oscillator and its active load dissipate 80 pW at 1.5 Hz from a 1 V supply at 22°C.

Introduction: Remote, wireless sensors have been described for a variety of applications including in vivo medical diagnostics [1] and environmental monitoring [2]. These sensors are usually constrained by a tight power budget. For example, the small size of in vivo sensors limits their battery capacity; environmental sensors require low power for long field-lives. A typical remote sensor is idle most of the time, waking only occasionally to sample inputs, log or transmit data. In this regime, the wake-up timer (or watch-dog timer) is the only circuit that is always active and must, therefore, be designed for low power. On the other hand, the exact frequency at which it wakes is not necessarily critical.

A wake-up timer consists of an oscillator and a counter. To reduce overall power it is desirable to reduce leakage by keeping the component count low, and reduce dynamic power by keeping the switching frequency low. These two considerations suggest the use of a slow oscillator with only a few stages, and a small counter. The design described in this Letter adopts this approach.

Another design decision concerns the supply voltage of the wake-up timer. Both dynamic and static power decrease with decreasing supply voltage. Extremely low power at slow switching speeds is possible with a supply voltage close to, or lower than the threshold voltage of the transistors [3]; however, generating a reliable, low voltage supply is a challenge, especially if the generator itself must be low power. A benefit of the oscillator described in this Letter is that it achieves low power even at relatively high supply voltages and over a wide operating range. It is, therefore, suitable for systems in which the supply voltage is provided directly from a battery and there is no level shifting.

Many oscillators have been designed for high accuracy at low power. For example, crystal oscillators typically achieve 130 nW dissipation at frequencies of 33 kHz [4]; however, they do not scale down to hertz frequencies or picowatt power. Oscillators in which power consumption is the primary concern are presented in [5] and [6]. Both use ring oscillators in which the switching frequency is limited by high impedance circuit elements. The first, [5], limits the current between two oscillator stages to the gate leakage of a MOS transistor. The second, [6], places starved transistors in the pull-up and pull-down paths of the inverters.

The oscillator described in this Letter uses starved transistors as in [6] but arranged to improve robustness in the face of process and environment variations. We also consider the design of the driven gate at the output of the oscillator.

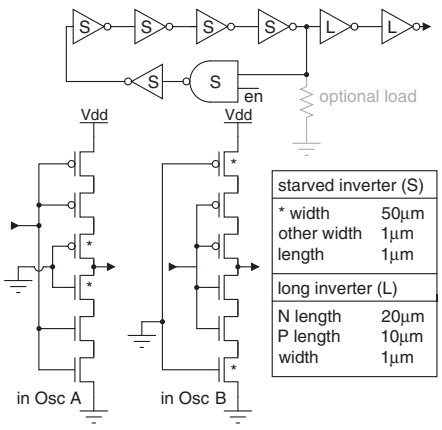

Fig. 1 *Oscillator, loaded by output buffers, (top) and the starved inverters used in Osc A and Osc B (bottom)*

Oscillator: The oscillators in Fig. 1 were fabricated in a 0.35 μm, 3.3 V logic process. A chip micrograph is shown in Fig. 2. Two variations were fabricated. In Osc A the starved NMOS transistors are connected to the inverter output nodes. In Osc B the starved NMOS transistors are adjacent the ground rail.

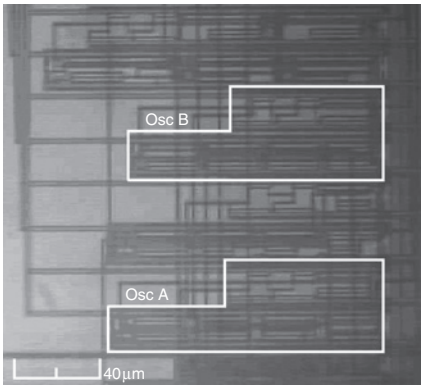

Fig. 2 *Micrograph of fabricated oscillators*

Figs. 3 and 4 show the performance of the fabricated oscillators compared with [5, 6] and simulation results. The fabricated circuit includes an analogue pad at the oscillator output. Although this is intended for measurement of the analogue output, it was observed that a 50 MΩ resistor connected to this pad improved oscillator performance at high supply voltages.

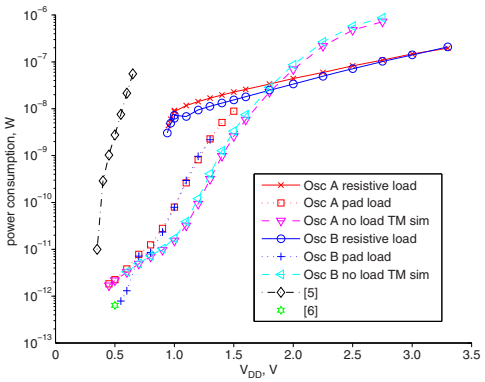

Fig. 3 *Power against supply voltage*

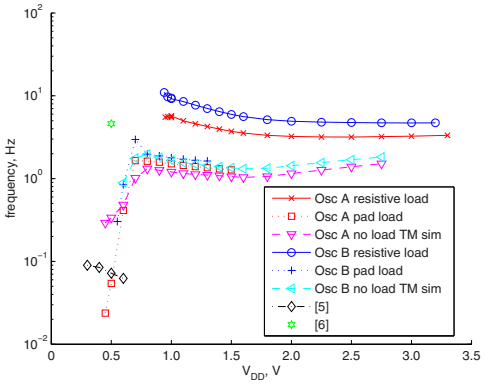

Fig. 4 *Frequency against supply voltage*

Unlike [6] our oscillators do not include starved PMOS transistors in the pull-up stack. This configuration permits operation at much higher voltages. A wide, always-on PMOS transistor was retained as it reduced power consumption by 20%. A further difference is the use of wide, rather than long transistors. The very low leakage in the 0.35 μm process was insufficient for oscillators using long, starved transistors.

In [6] it is claimed that the stack effect in the arrangement with starved transistors adjacent to the supply rails (as in Osc B) improves rise/fall times and reduces power. Fig. 3 shows a power saving for Osc B

under some load conditions; however, Fig. 4 shows that Osc A oscillates more slowly under the same conditions. The best choice will depend on the load circuit.

The ultra-low power oscillators in [5] and [6], and that described in this Letter, all use different feature sizes and their performance is reported over different operating voltages. Unlike [6], the new oscillator will work at 0.35 μm and has been demonstrated over variable supply voltages. Compared with [5], our design has superior operating range and significantly better power consumption characteristics at the cost of inferior temperature sensitivity.

Shaping load: If the output of the oscillator is used to drive a conventional CMOS logic gate directly, that gate can suffer high power dissipation owing to the short-circuit currents during the long oscillator rise and fall times. One solution is to use a Schmitt trigger and this approach is used in [5]. (In [6] the oscillator drives charge pump capacitors and hence the problem does not arise.)

Our oscillator uses a simple alternative, it is buffered with a static CMOS inverter with long transistors. The long transistors reduce short-circuit current and hence reduce static power dissipation at the cost of increased load capacitance and hence dynamic dissipation. Given the low switching frequency, lower total power is achieved with relatively long transistors. In our case 10 μm-long PMOS and 20 μm-long NMOS transistors were used.

The benefit of this approach over a Schmitt trigger is its robustness to process and environment variations. Under some conditions the oscillator may not exhibit rail-to-rail output voltage swing. Moreover, the threshold voltages of the Schmitt trigger can vary. These factors combine to constrain the valid operating conditions of the oscillator more tightly than the simple long-inverter buffer. Fig. 5 shows the different operating ranges for oscillators with a Schmitt trigger and long-inverter buffers. It also demonstrates the power savings of the long inverters, an average 49% decrease in total power dissipation.

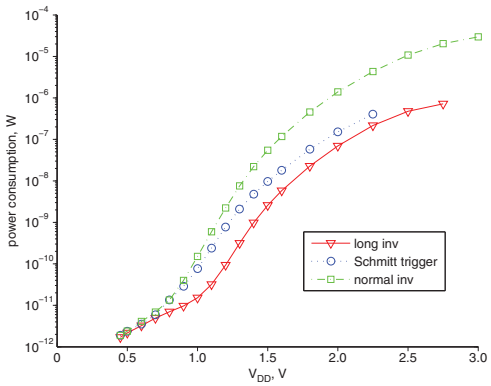

Fig. 5 *Simulation results of power against supply voltage for oscillators with long-inverter buffer and with Schmitt trigger at typical corner; no additional load included*

Conclusion: Ultra-low power oscillators have been presented that are suitable for wake-up timers in remote sensors. The oscillators were fabricated in an inexpensive 0.35 μm process and work over a wide range of operating conditions and supply voltages. They can, therefore, be operated directly from a battery without a DC level-shift circuit.

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One or more of the Figures in this Letter are available in colour online.

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