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THE DESIGN OF A HARDWARE SYMBOL TABLE
FOR USE IN AN ALGEBRAIC COMPUTER

BY
WILLIAM D. MCGEE

A Thesis
Submitted to the Faculty of Graduate Studies through the
Department of Electrical Engineering in Partial Fulfillment
of the Requirements for the Degree of
Master of Applied Science at the
University of Windsor

Windsor, Ontario

1966

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ABSTRACT

An algebraic computer has, as its machine language, algebraically oriented statements, and anglicized control, and input-output statements. The problem of gaining access to memory, by means of the symbolic addresses in the program, remains.

This Thesis presents three proposals for reducing translation time. All three solutions require a hardware table which is fast in its operation. This Thesis presents the design of a table utilizing electrically alterable, non-destructive read-out, magnetic devices.

ACKNOWLEDGEMENTS

The author wishes to express his thanks to Dr. P.A.V. Thomas, who supervised this work, for his helpful suggestions and guidance.

The author is grateful to the Research and Development Labs of Northern Electric Company Limited, in Ottawa, for supplying the cores used in this design.

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I. INTRODUCTION

Dr. P.A.V. Thomas of the Department of Electrical Engineering at the University of Windsor proposed, in 1964, a study of the feasibility of building an algebraic computer. The proposed machine would execute, directly, instruction similar to those comprising Fortran and Algol. The great advantage to having such a computer is that no compiling would be necessary and the program would be executed immediately after being loaded into memory.

One of the major design problems is the method of gaining access to memory. In this thesis, three possible solutions to the problem are described and the reasons for requiring a hardware table given. The remainder of the thesis is devoted to the design of the table and a prediction of its performance based upon the test results of a small model.

II. ALGEBRAIC COMPUTER

It is the nature of the proposed algebraic computer that it have, as its machine language, mathematical statements, such as $SUM = X + Y$, and anglicized control statements, such as GO TO 123, as found in Fortran - Algol type languages. With this property, compiling - the translation of algebraic statements into a series of conventional computer machine language instructions - is eliminated. However, the symbolic addresses, whether variable names, such as SUM, X and Y in the above example, or statement labels, such as 123 above, remain to be identified with actual memory locations. In conventional computers, a symbol table, which equates symbolic addresses to machine addresses, is created in memory and before execution begins, all symbolic addresses in the program are replaced by their machine address equivalents. This replacement consumes a considerable amount of time, a good deal of which is spent searching the symbol table.

The reduction of symbolic address replacement time, hereafter called translation, can be realized by either eliminating the need for translation altogether, or constructing a hardware table which will compare a symbolic address to the entire collection of symbolic addresses which occur in the program, and automatically give the assigned machine language address.

Three solutions to the problem are described
in Chapter III.

III POSSIBLE SOLUTIONS

3.1 Proposal 1: A Fast Translation Before Execution

One means of reducing translation time is a modification of the translation process of conventional computers. The difference is that the symbolic addresses and corresponding machine addresses are stored in a hardware table rather than in main memory. See Figure 1.

While the program is being read into main memory, the symbol table is constructed in the hardware table with a one to one correspondence between the symbolic addresses and machine addresses. Immediately after reading the program into main memory, the computer selects the symbolic addresses from the program sequentially and interrogates the table via the symbolic address register. The operation of interrogation automatically compares the contents of the symbolic address register (SAR) with every symbolic address in the symbolic address memory (SAM) simultaneously, and energizes only the machine address memory (MAM) read line which corresponds to an equal compare in the SAM. The result of the MAM read is the entering of the machine address equivalent to the symbolic address in SAR, into the machine address register (MAR).

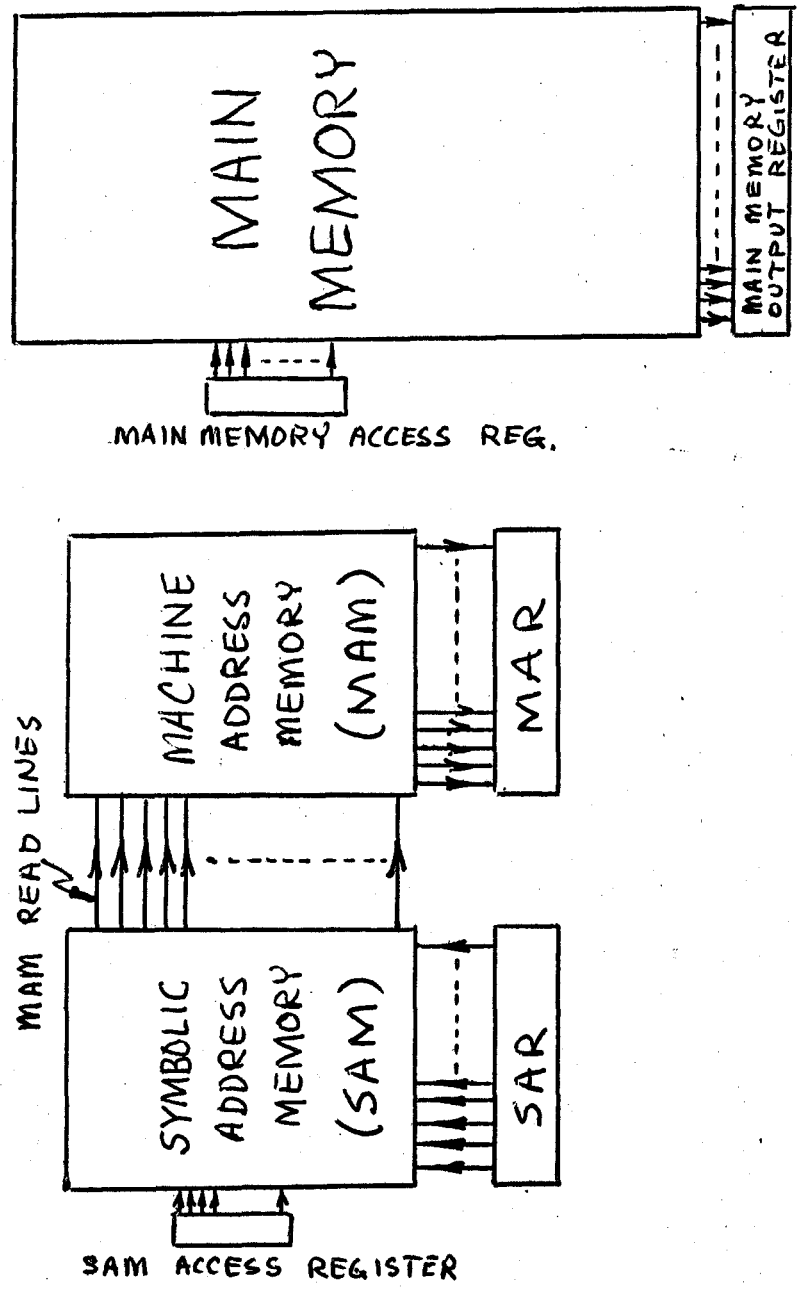


Fig. 1 The Hardware Symbol Table

The machine address is now entered into the program in main memory in place of the symbolic address.

Assume for the moment that the main memory is organized in 6-bit bytes, and that there are several bytes per word. Assume also that the main memory contains 4096 words. The memory is then addressable by a 12 - bit address, i.e. 2 bytes. All single character (1 byte) symbolic addresses must be converted to 2-byte machine addresses upon translation and thus an extra byte must be made available during storage of the program for the extra byte required. See Figure 2 for a flow chart of translation operation.

The SAM and MAM need only be large enough to accommodate the largest number of different symbolic addresses in the program. This number is considerably smaller than the number of words in main memory.

The use of the hardware table eliminates the need for searching through a symbol table one comparison at a time.

One disadvantage of this scheme is that the program stored in main memory no longer contains symbolic addresses, which are very useful in debugging the program.

This scheme requires logic capabilities beyond those involved in the execution of the program. In addition it requires a hardware table.

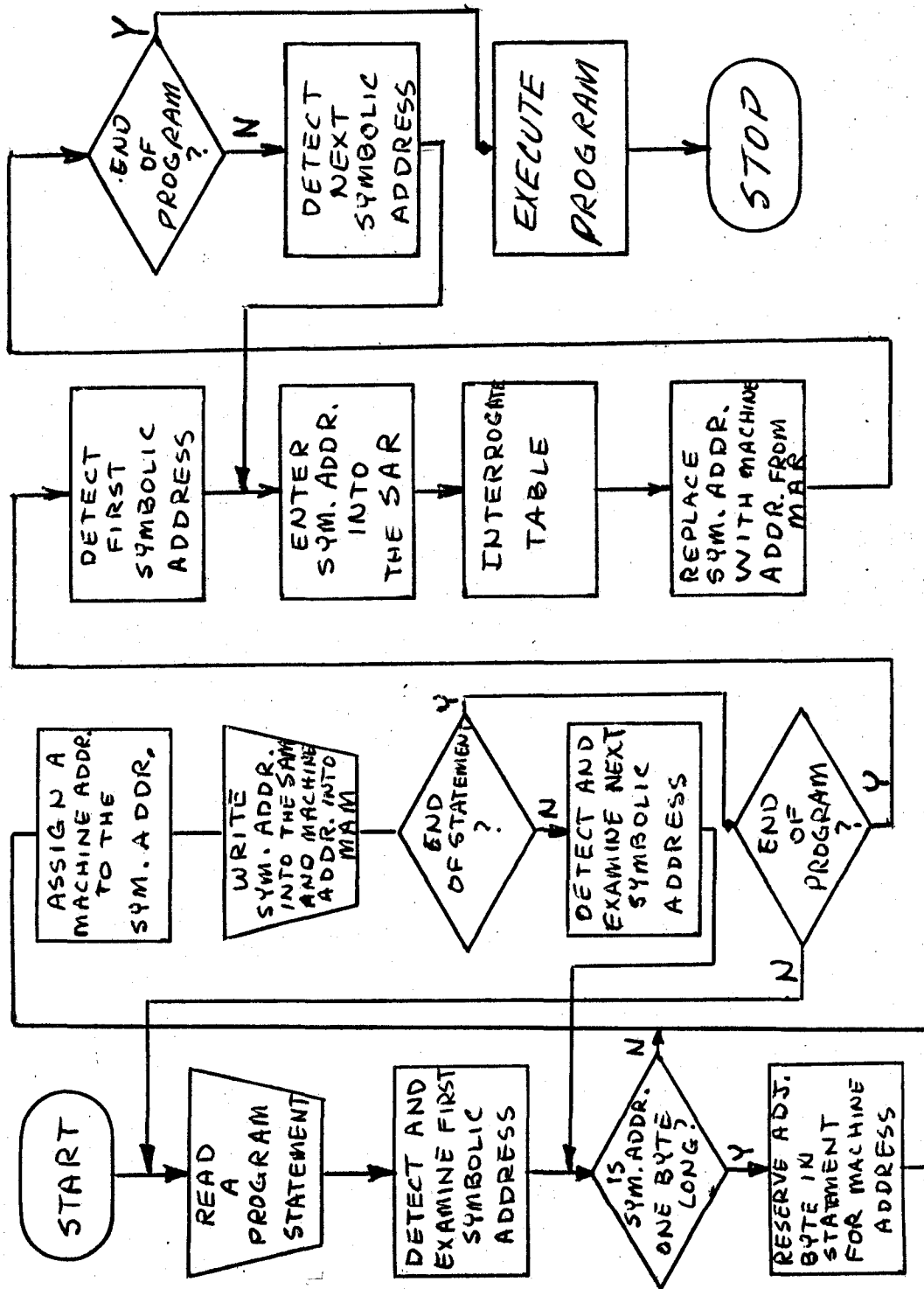


Fig. 2 Flowchart of Translation Process

3.2 Proposal 2: Access By Symbolic Address

Another method of reducing translation time is to have associated with the main memory, the symbolic address memory (SAM), as described in Proposal 1. In this scheme, there is a one to one correspondence between the words of the SAM and the words in the main memory. See Figure 3. In this scheme, no translation is necessary. Every word in main memory is accessible by its symbolic address which is assigned when the program is loaded. The main memory must also be accessible by conventional machine address means, because the program must be loaded and executed sequentially.

This system, comprising the symbolic address memory directly connected to the main memory, constitutes a hardware table, as described in Proposal 1.

The great advantage of this system is that no translation whatsoever is required. During the loading of the program into main memory, the statement labels are loaded in the SAM word corresponding to the word in main memory in which the statement starts. At the same time, variable names are loaded into the SAM starting at the last word and working back. The instant loading of the program is complete, execution can begin.

The great disadvantage of the system is in its inefficiency and cost. Only a small number of the

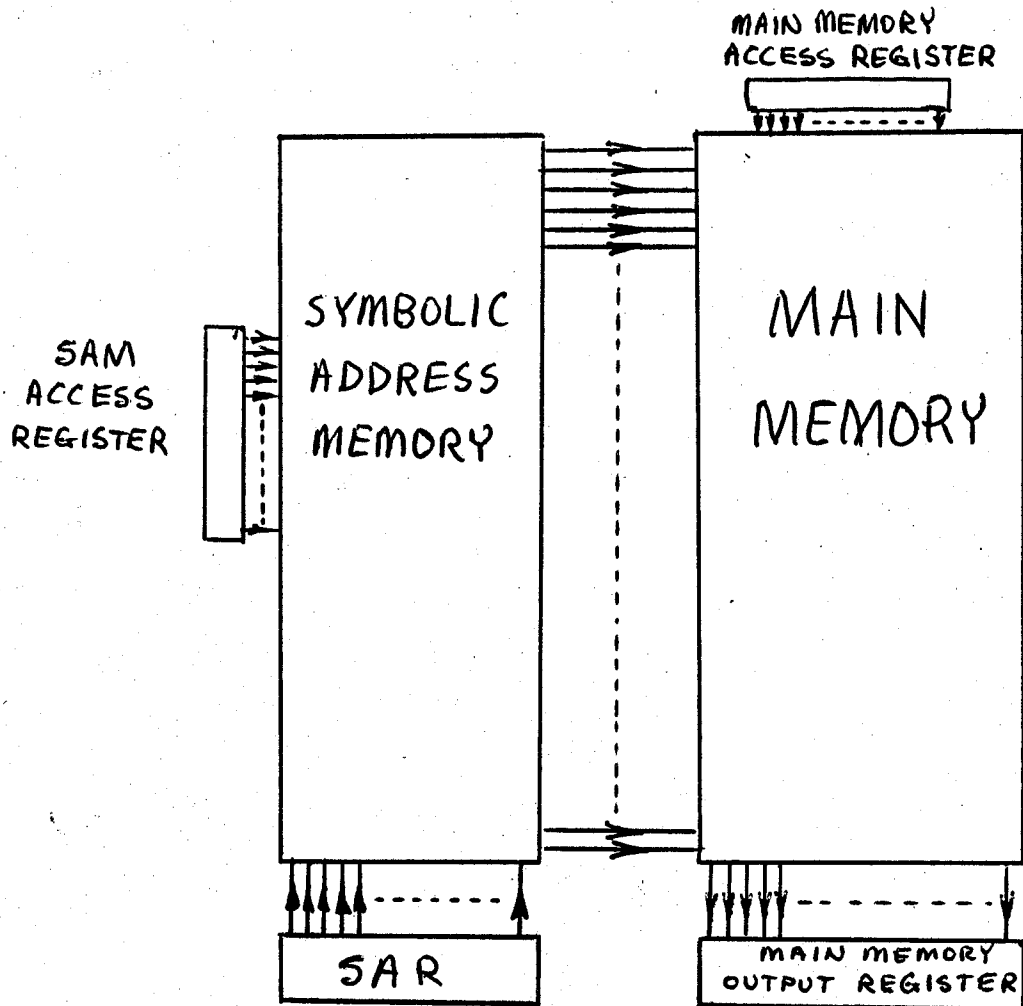


Fig. 3 Access By Symbolic Address

statements in a program have a label, thus a large percentage of the SAM is unused during execution of a given program. Because of its size, and the special circuitry required for its implementation, the cost of constructing this system would be very high.

3.3 Proposal 3: Fast Translation During Execution

A third method of solving the problem of reducing translation time is quite similar to Proposal 1. The system requires a hardware table as described in Proposal 1. The table is loaded with symbolic addresses and machine addresses as in Proposal 1; but, instead of replacing the symbolic addresses in the program, the table is consulted every time access to memory by symbolic address is required. The machine address is then used to retrieve or enter information into the main memory.

The symbolic addresses remain intact in the program but the symbol table must be interrogated every time a symbolic address appears for execution. While the time required to retrieve the machine address is small, the total time spent consulting the table can accumulate to a significant value.

3.4 Conclusions

All of the above proposals require some form of hardware table. Thus, it is the purpose of this thesis

to present the design of a hardware table, with the final choice of which of the above solutions to be incorporated into the proposed algebraic computer, left to its designer.

IV. SYSTEM DESIGN

4.1 Preliminary Specifications

The symbolic address memory must be of course capable of storage, but more specifically, must be of the electrically alterable non-destructive read-out (NDRO) type. The latter specification is necessary because the entire SAM is interrogated at once, and the information read from the SAM is not stored.

The SAM must also be capable of executing the Boolean function, EXCLUSIVE-OR. That is, the output of each SAM word must indicate whether or not the word is exactly the same as the contents of the SAR.

The machine address memory need not be of the NDRO type, although its use simplifies the read circuitry.

4.2 The Basic Unit - A Multiaperture Magnetic Device

A multiaperture magnetic core most closely fulfills the required specifications. Flip-flops are still too expensive to use on such a large scale, and the logic required to perform the exclusive-or function, would make the cost prohibitive.

There are several electrically alterable NDRO

magnetic devices available, one being the Biax. The element used in this design, is a multiaperture device developed by Northern Electric. See Figure 4. It consists of a major aperture, A1, and four minor apertures, A2, A3, A4 and A5. It is constructed so that the minimum cross sectional area of the legs, L2 and L3, about the minor apertures, is one-half the cross sectional area of the major legs (L1).

4.3 The Two Stable States

The two states of the core are called the blocked state and the unblocked state.

If the remanent flux in the core is everywhere in the same rotational direction about the major aperture, and of such a density as to saturate the core, then it is said to be in the blocked state. See Figure 5a.

If the remanent flux in the core is divided, such that half is directed clockwise about the major aperture, and half counterclockwise, and of such a density as to saturate the legs about the minor apertures, then the core is said to be in the unblocked state. See Figure 5b.

4.4 Interrogating The Core

The core is interrogated by an attempt to switch the direction of the flux about a minor aperture. The output winding is wound on the same leg as the interrogate

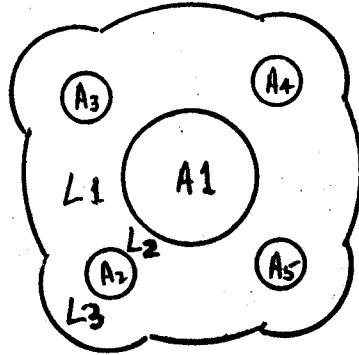


Fig. 4 A Multiaperture Magnetic Device

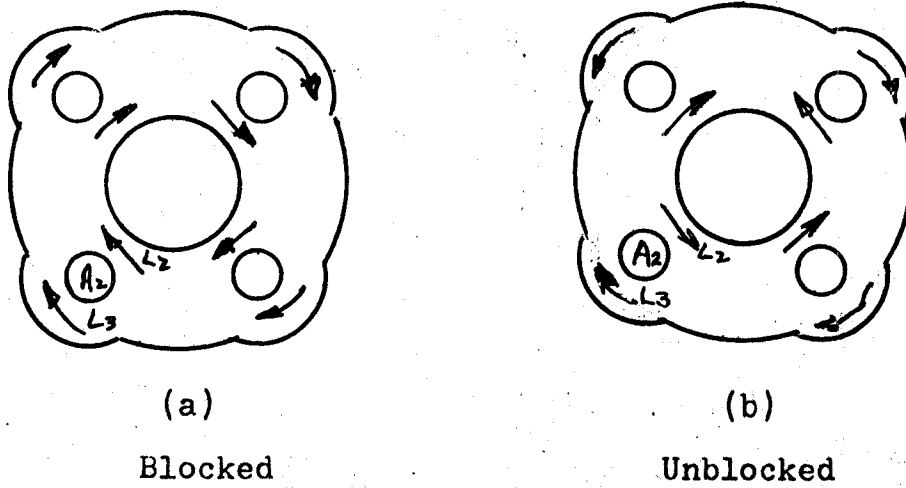


Fig. 5 The Two Stable States

winding (See Figure 6), so that if the attempt to switch is successful, then the change of flux induces a voltage in the output winding. If the attempt is unsuccessful, then there is no flux change and hence no output.

If the core is unblocked, as in Figure 5b, and an interrogating field of H_i is applied to leg L3, then the flux about the minor aperture A2 is switched and a positive voltage pulse appears at the output. The core is left in the unblocked state, but the flux about A2 is in the counterclockwise direction. If another interrogation of the core were made, the output would be zero; thus the flux direction about the minor aperture must be restored to its original state, i.e. the clockwise direction.

The restore field, which is of the same strength as the interrogation field, is applied by another winding on leg L3. The read cycle wave forms and core states for the unblocked case are shown in Figure 7.

If the core is blocked, as in Figure 5a, and the same read cycle is used, the field applied to leg L3 attempts to reverse the flux in L3. The flux in L2 is already saturated counterclockwise about A3, thus a different path must be found. The alternate is around the major aperture A1, a much longer path. If H_i is made large enough to reverse the flux around a minor aperture, when in the unblocked state, but not large

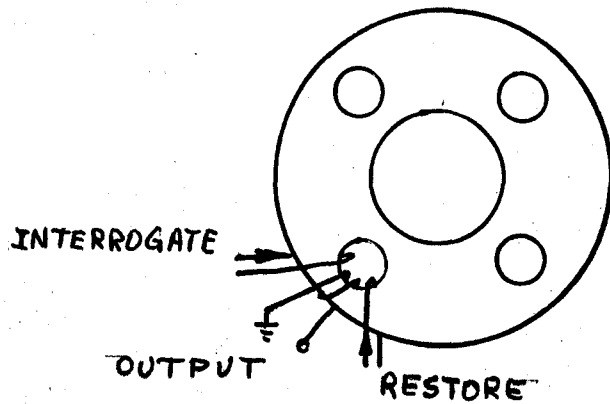


Fig. 6 The Interrogation, Restore, and Output Windings

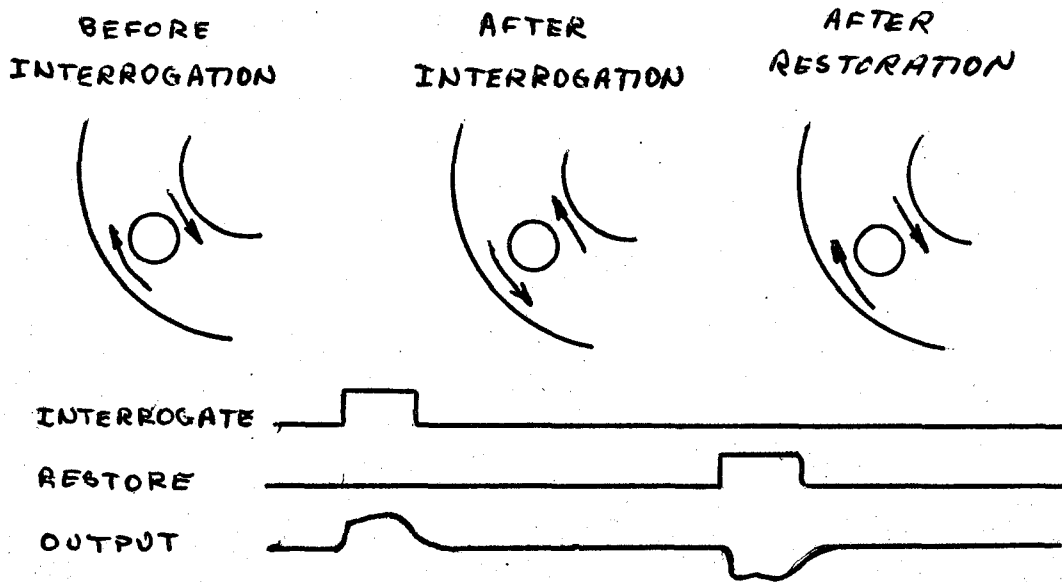


Fig. 7 Read Cycle - Unblocked Core

enough to produce a flux change around the major aperture, there is no flux change in L3 for the blocked core and hence no output. See Figure 8 for wave forms and states. Likewise, when the restore field is applied, there is no change of flux in L3 and the core is left in its original state - blocked

Both the blocked and unblocked cores give a noise output, because the hysteresis loop is not perfectly rectangular. See Figure 9. With the application of the interrogate field, there is a slight change of flux in the core, which produces a noise spike at the beginning of the pulse, and at the end. It is necessary, therefore, to operate the core with interrogate and restore fields which maximize the resolution between the two possible outputs. The optimum fields can be determined from the core characteristics.

4.5 Core Characteristics

A set of typical core output characteristics were collected in order to determine the optimum interrogation, restore and unblocking fields. The output characteristics are shown in Figure 10, and a discussion of them follows.

The core is set to the blocked state by the application of an mmf large enough to produce saturation in the same rotational direction about the major aperture throughout the core. This mmf was found to be approximately 1.5 amp.-turns minimum. To insure

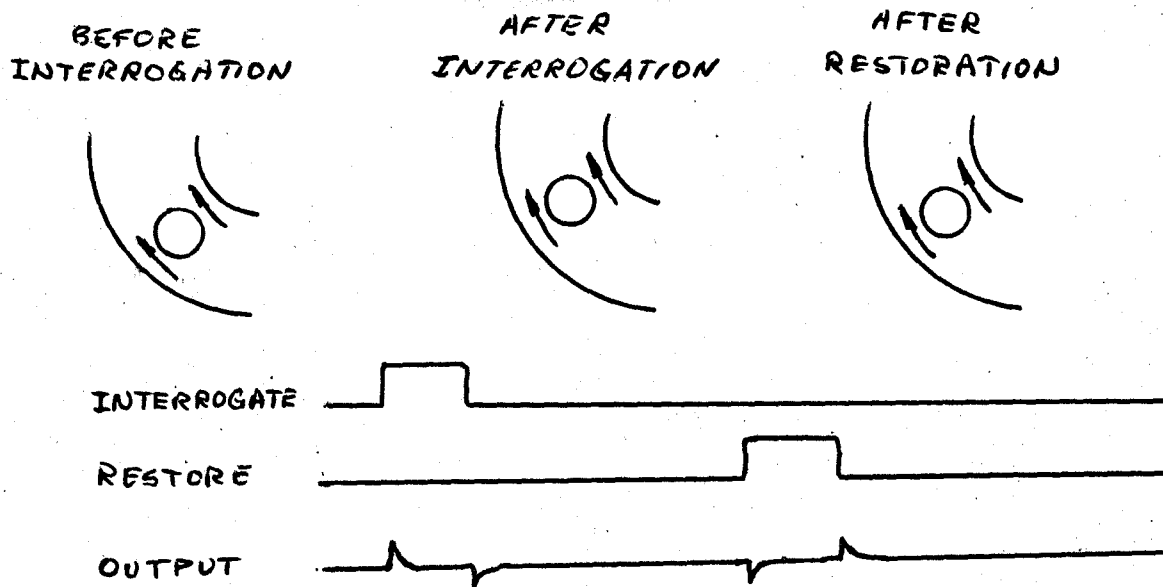


Fig. 8 Read Cycle - Blocked Core

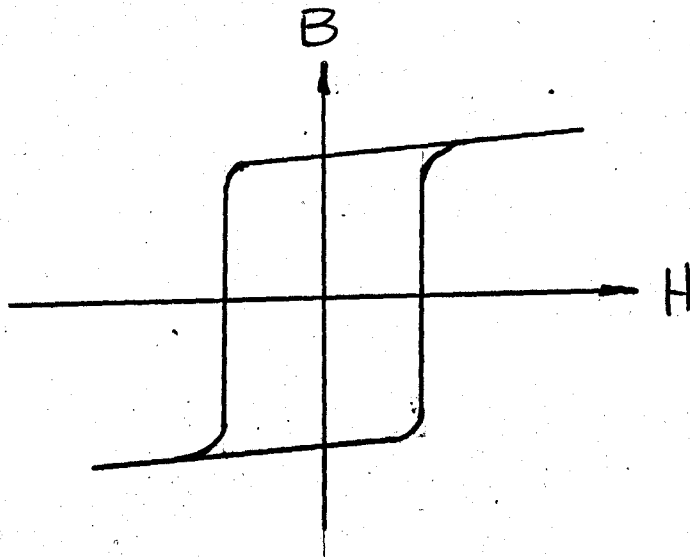


Fig. 9 Hysteresis Loop

blocking, a field of 2.0 amp.-turns is used.

The core is switched to the unblocked state by the application of an mmf to a minor leg, large enough to reverse the direction of half the flux in the core. The core characteristics show that the output is identical for unblocking fields of .6 amp.-turns or greater, as shown in Figure 10f through 10h. On this basis, the unblocking mmf is chosen to be .7 amp.-turns.

The core can be set to the unblocked state by the interrogation field, if it is large enough; thus the interrogation field must be kept low enough so as to have no effect on the flux about the major aperture, i.e. less than .4 amp.-turns.

An interrogation field of .35 amp.-turns is chosen in order to give a large and relatively flat output for an unblocked core, and a relatively small noise output for a blocked core. It is to be noted that 1.0 micorsecond after the interrogation field is applied, the noise output decays to approximately 10 mv. for a blocked core.

4.6 Machine Address Memory

The machine address memory (MAM) can be constructed of conventional toroid cores, although the use of non

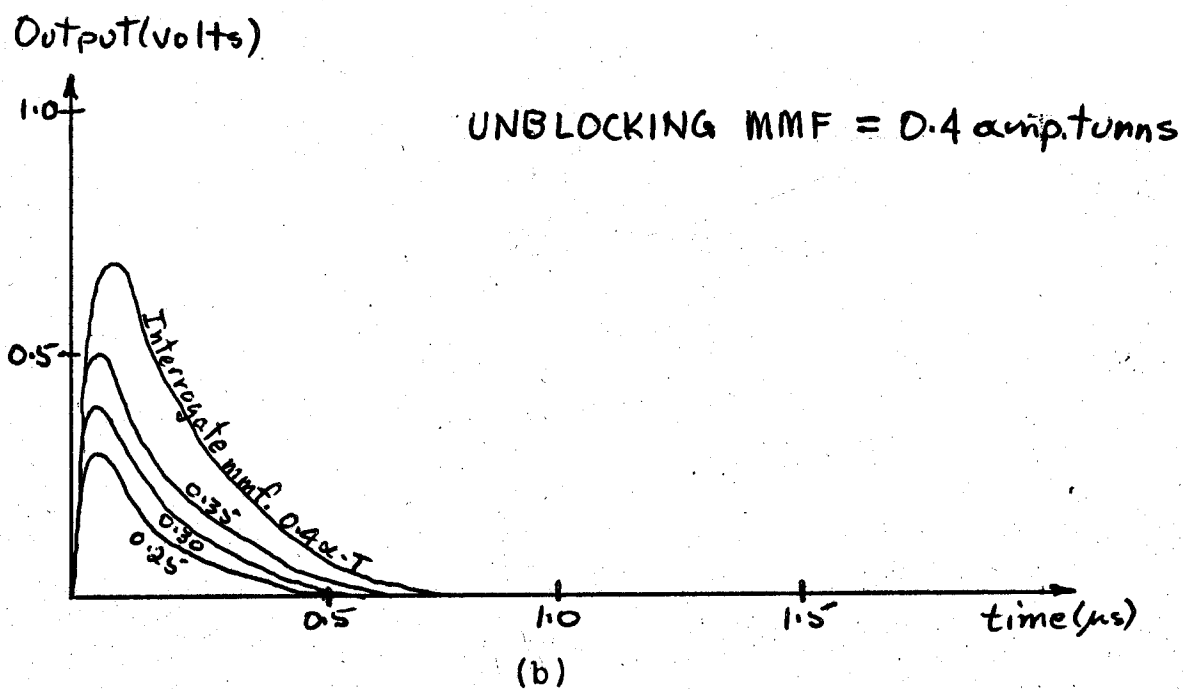
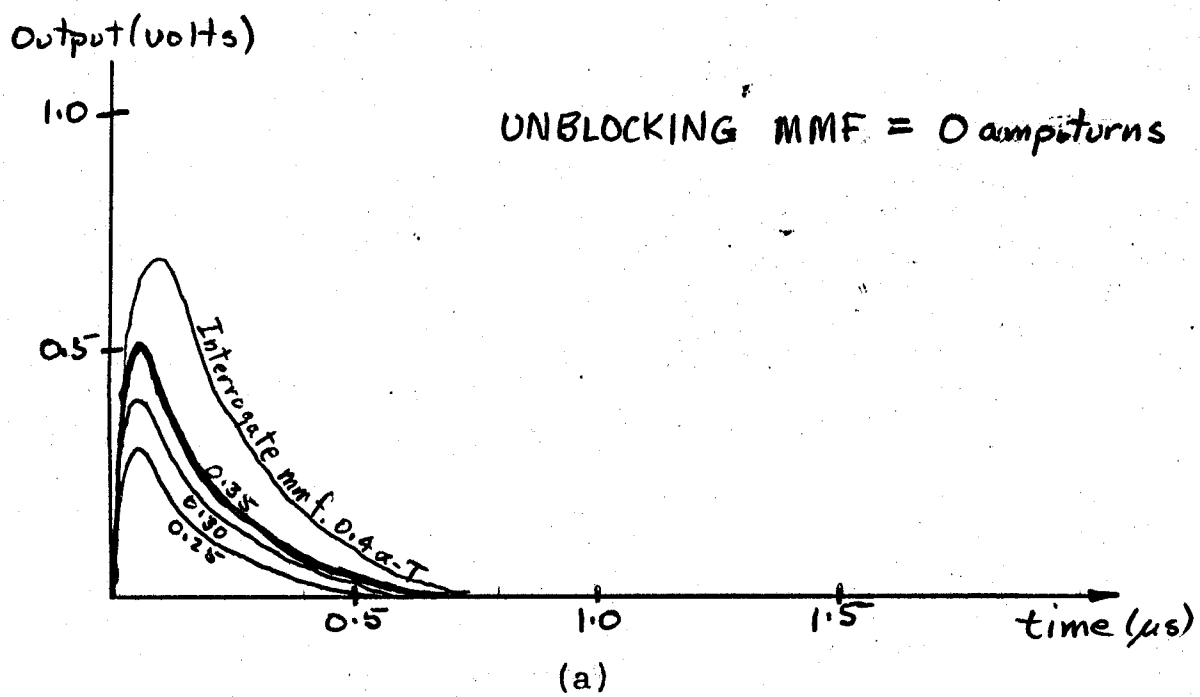


Fig. 10 Core Characteristics

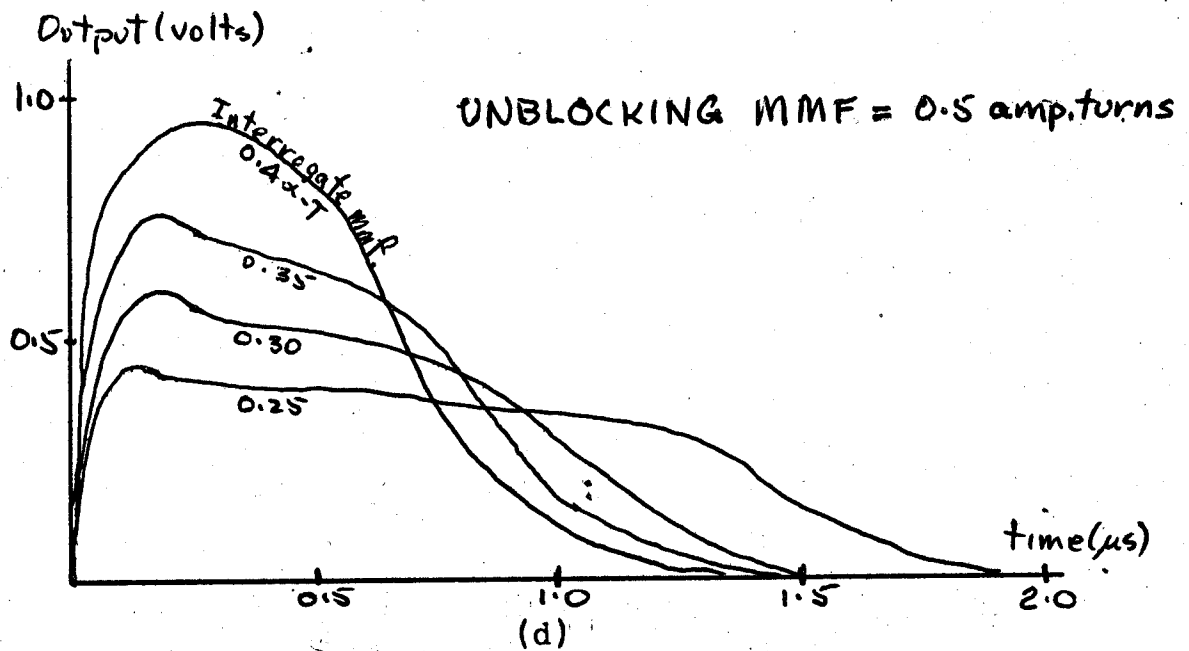
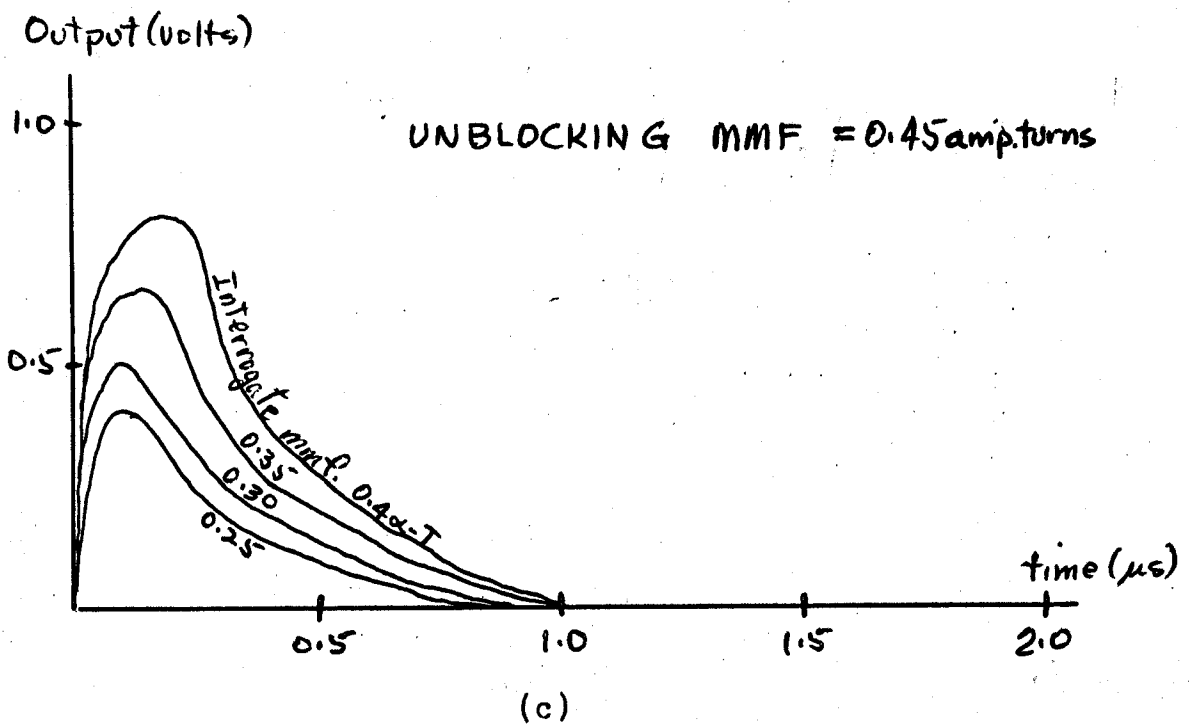


Fig. 10 (Cont'd) Core Characteristics

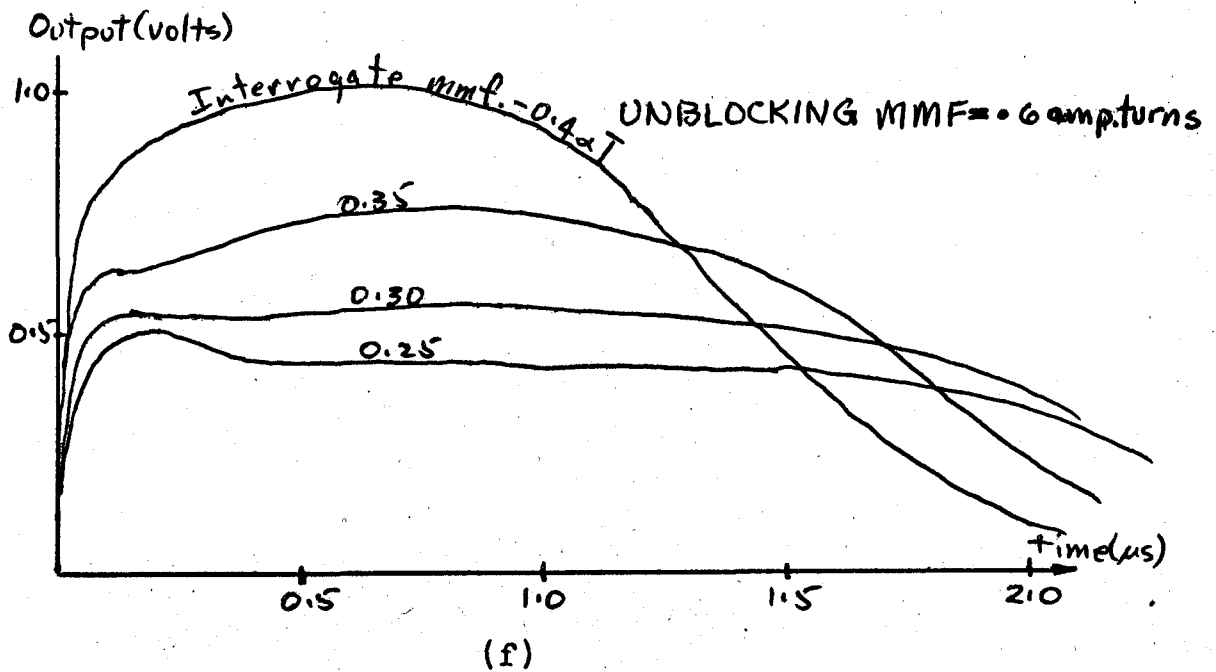
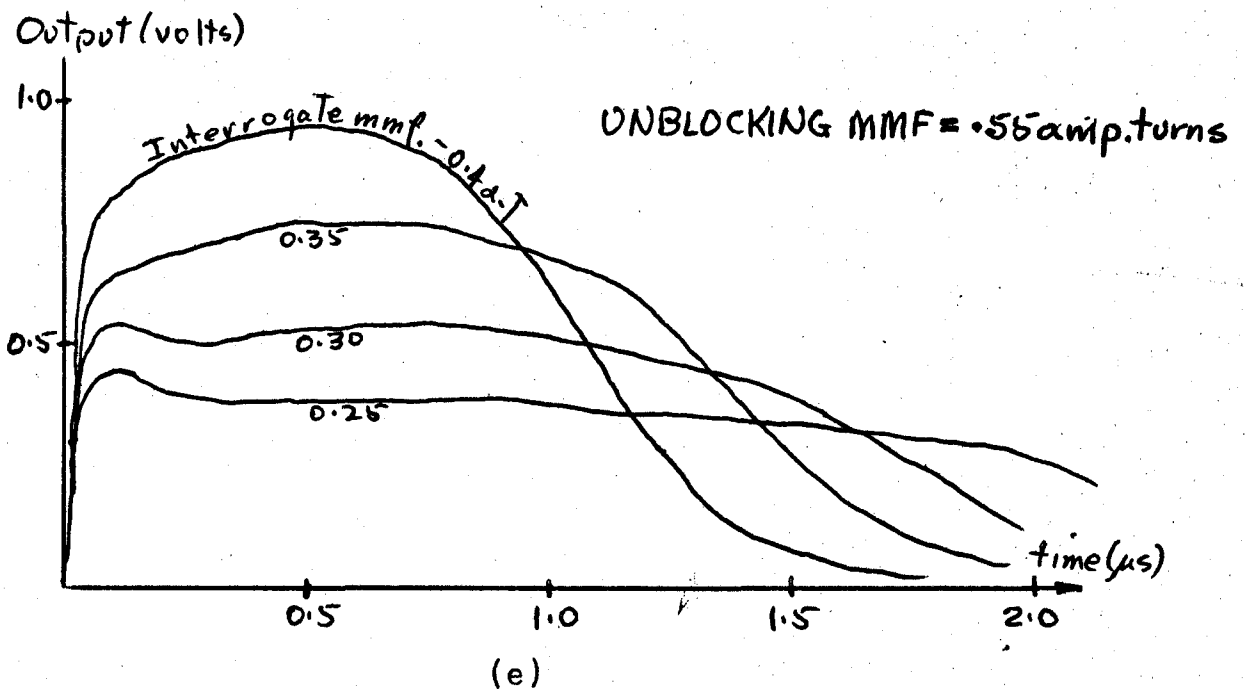


Fig. 10 (Cont'd) Core Characteristics

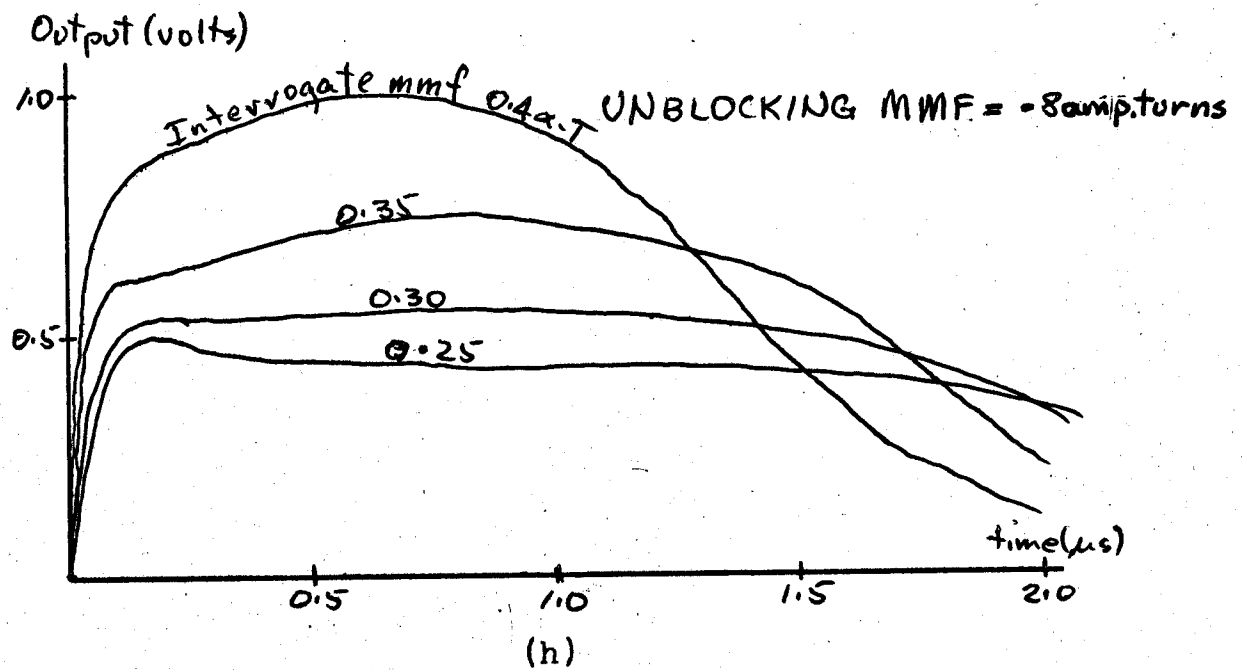
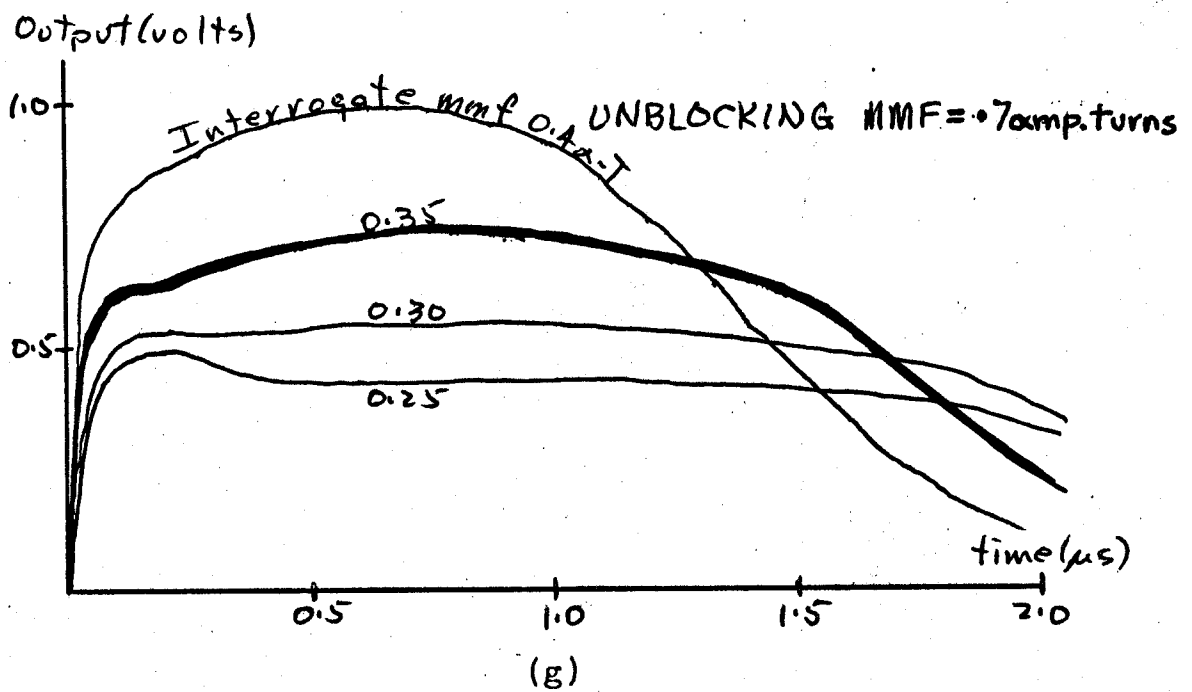


Fig. 10 (Cont'd) Core Characteristics

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destructive read-out element, such as the multiaperture device described above, eliminates the need to rewrite the information back into the memory after it has been read-out. The design of this part of the hardware table makes use of the NDRO element described in Section 4.4

It is the purpose of the SAM to select the word in the MAM which is to be read. The design of the SAM is given in a later section, so it is assumed here that a word has been selected.

Every bit in a given word is interrogated simultaneously by the same line, giving a parallel read-out of the entire machine address. See Figure 11. The bit output line passes through the same bit in every word of the MAM. Since only one word in the MAM is interrogated at one time, the output is naturally from the word interrogated. The output is either a logical '1' or logical '0' and has a shape as shown in Figure 10.

The output is sensed at a time after the noise pulse decays, i.e. at about .75 microseconds, to prevent the noise pulse from erroneously entering information into the machine address register.

4.7 Machine Address Memory Read Circuitry

When and only when there is complete coincidence between the contents of a SAM word and the contents of the SAR, is the corresponding MAM word to be read. Thus,

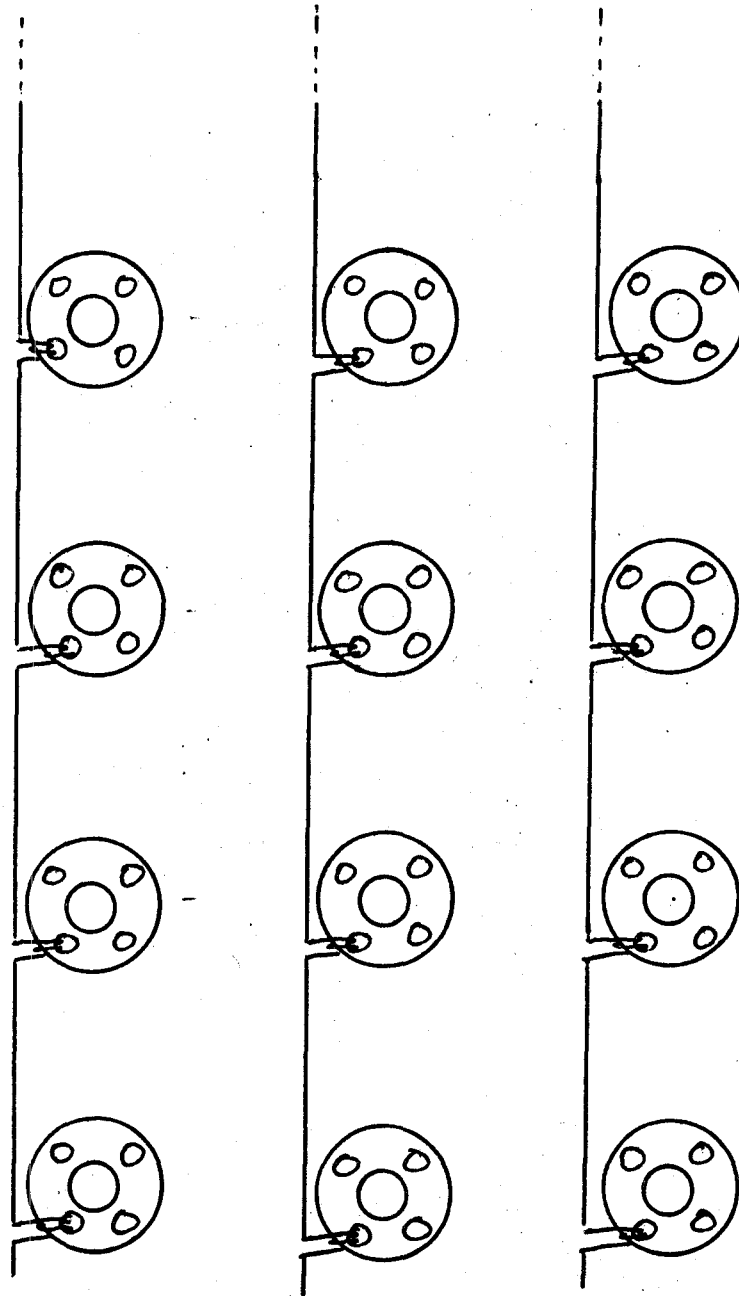


Fig. 11 Machine Address Memory Output Lines

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a criterion for the design of the SAM must be established on the basis of the demands of the read circuitry of the MAM.

Two possible means of achieving MAM read-out are shown in Figure 12. Pnp transistors are used for no other reason than they were more readily available at the time of the design.

A read transistor of Figure 12a requires that the SAM word output be negative, and of such a value as to overcome the positive bias on the base, and allow it to pass current through its corresponding MAM read line. Thus a threshold is determined, which can be exceeded only when the SAM output voltage is made up of the individual unblocked output of every interrogated core in the SAM word. Since the unblocked output can vary slightly from core to core, and since the output pulse is rounded, the resolution between the full output and the full output minus the output from one unblocked core, is quite small. For these reasons this criterion does not seem too promising.

Consider now Figure 12b. Here a read transistor is normally conducting because of the negative bias on the base. However, no current flows through any read line because the strobe transistor is normally non-conducting. When interrogation of the SAM occurs, assume that a positive voltage is induced in the output

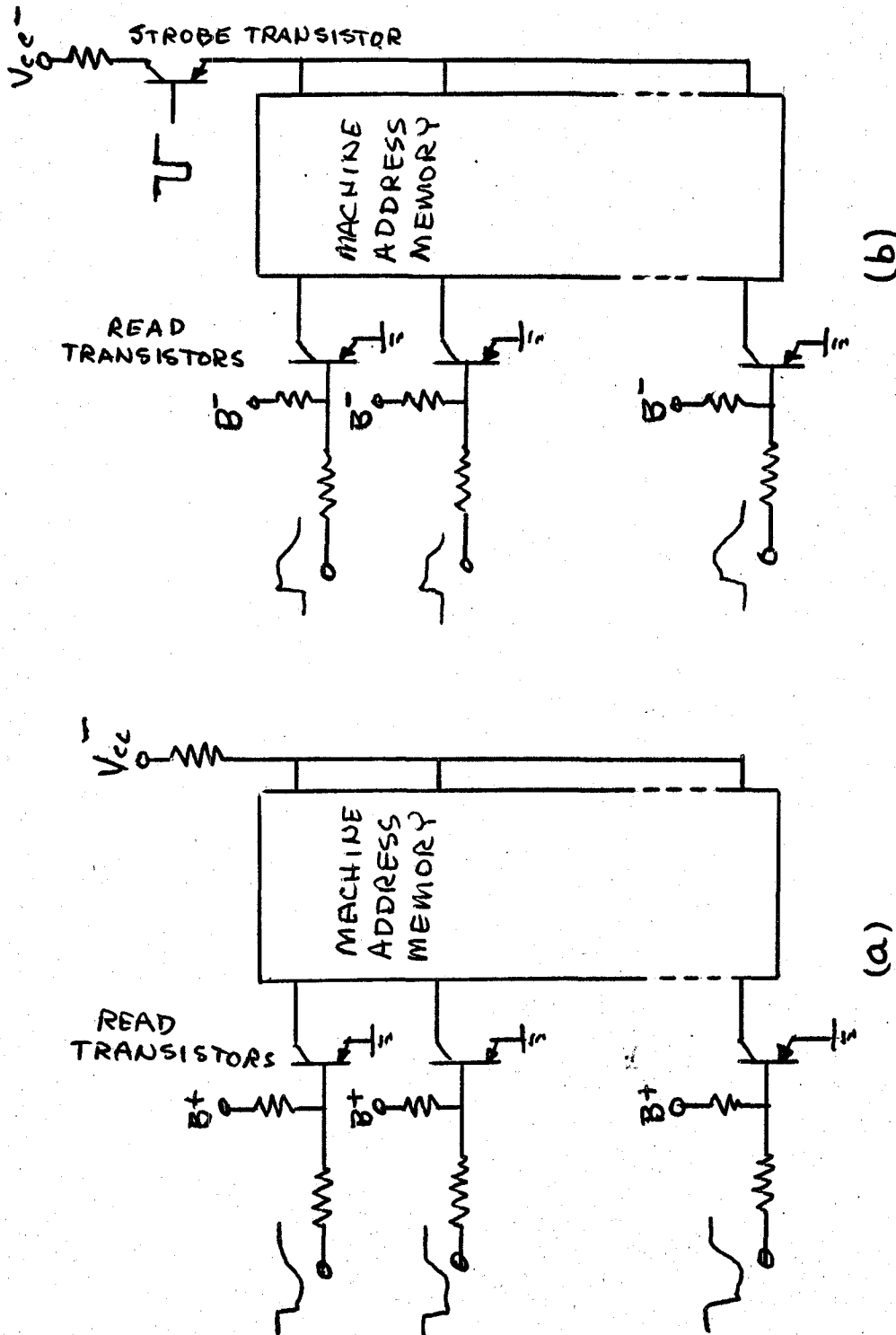


Fig. 12 MAM Read Circuitry

line wherever a disagreement occurs. In this case, the read transistor is cut-off for the duration of the output pulse. When no disagreement occurs, the output voltage consists only of the noise spike, which decays rapidly. Thus, during a portion of the output pulse time, the read transistor is biased negatively. If the strobe pulse is timed so as to make the strobe transistor conduct during the SAM output pulse, as shown in Figure 13, the negative power supply is then connected to the collectors of all the read transistors. Those cut-off by a positive output from the SAM will not pass current to its read line. That one which has not been cut off, passes current to interrogate the MAM. The resolution in this system is quite high. In the worst case, i.e. the output being from one unblocked core, the read transistor is cut off by the .7 volt output pulse.

The design of the SAM is based upon the requirements of Figure 12b, as described above.

4.8 Symbolic Address Memory

It is required that when there is perfect agreement between the contents of the symbolic address register and a word in the SAM, that the output be zero. When there is a disagreement in at least one bit, the output is to be positive.

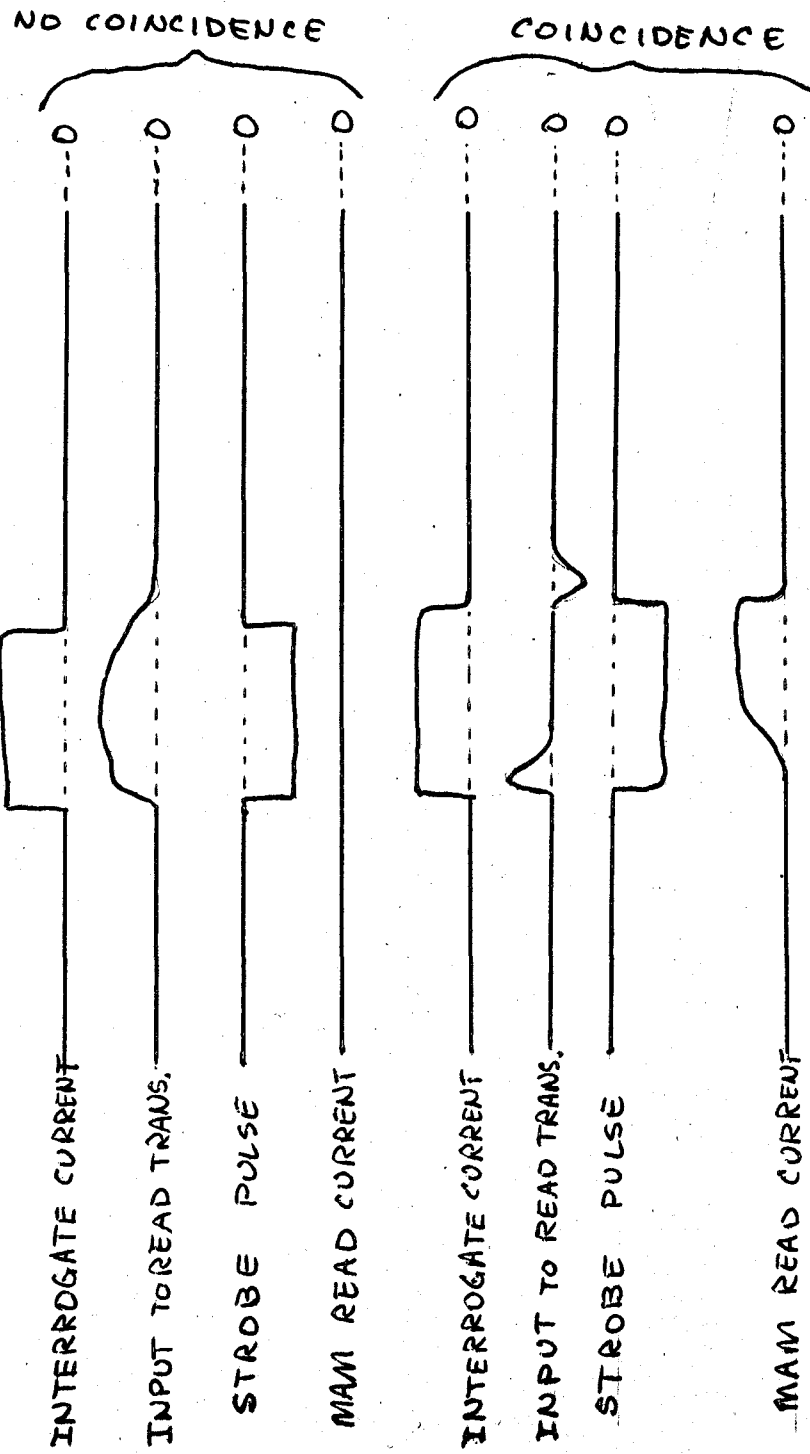


Fig. 13 Timing of Strobe Pulse

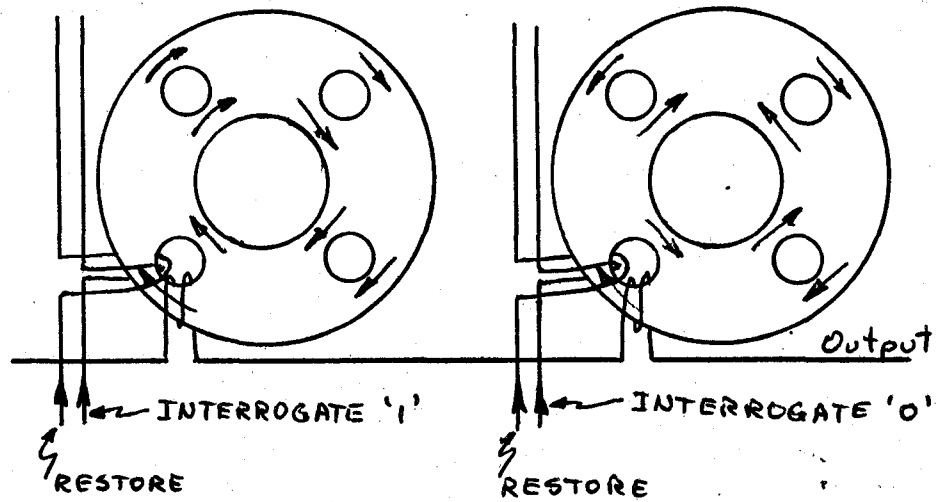
The core arrangement of Figure 14 stores one bit in SAM. A logical '1' is stored when the left hand core is blocked, and the right hand core is unblocked. A logical '0' is stored when the left hand core is unblocked, and the right hand core is blocked.

There are two interrogation lines, one called interrogate '1', the other interrogate '0' and one or the other is activated, depending on the value of the corresponding bit in the symbolic address register. If a '1' is stored and a '1' is interrogated the output is zero. However, if a '1' is stored and a '0' is interrogated then the output is a positive pulse. Likewise, when a '0' is stored and a '0' is interrogated, the output is zero. When a '0' is stored and a '1' is interrogated the output is a positive pulse.

This circuit performs the logical function exclusive-or, giving a '0' output when there is agreement, and a '1' output when there is a disagreement.

A word in the SAM consists of several bits, the number depending on the maximum character length of the symbolic address, and the number of bits required to code each character. Each bit in the word is interrogated according to its corresponding bit in the SAR. The bit output lines of the word are connected in series, so that output voltages contributed by the bits are summed. The series connection performs the Boolean Function OR.

A LOGICAL '1'



A LOGICAL '0'

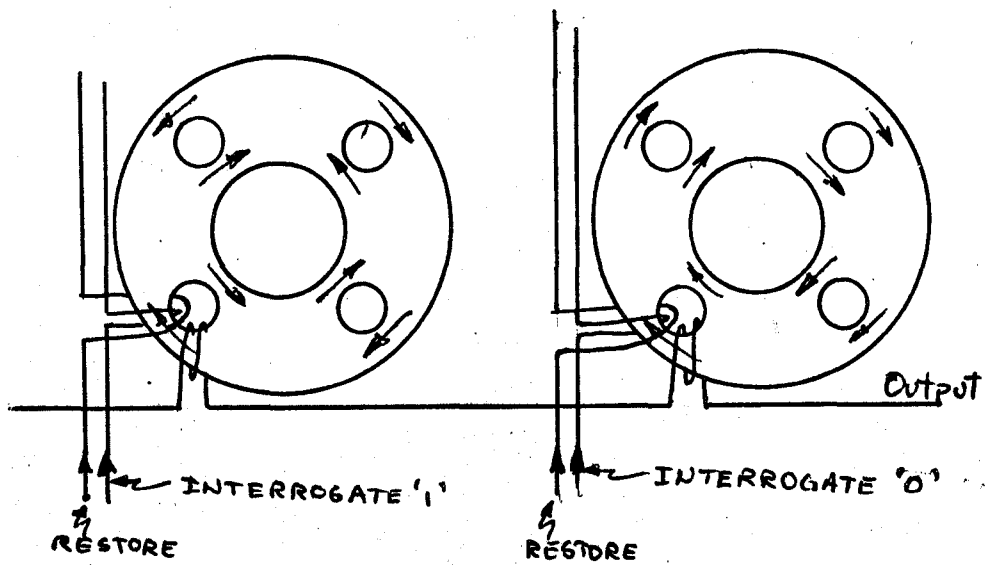


Fig. 14 Core Arrangement in SAM

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4.9 Writing Into The Symbolic Address Memory

Writing into the symbolic address memory is most easily accomplished by blocking all the cores and then unblocking all the required ones. The blocking winding is common to all cores in the memory because the writing is done only once, while the program is being stored in main memory, and there is no necessity for being able to change the contents, once the program is being executed.

The write circuit is shown in Figure 15. Before the program is loaded into main memory, all the cores are blocked. The correct word in the symbolic address memory is selected either by a standard linear selection circuit (a binary to n-imal decoder) or by the coincident current method. An unblocking field is applied to outer leg of every core in the word coincidentally, the inhibit field, of the same strength as the unblocking field is applied according to the contents of the symbolic address register. If a logical '1' is to be written, then the inhibit '1' field is applied and inhibit '0' is not. In this manner, the left hand core remains in the blocked state and the right hand core becomes unblocked. See Figure 16. The opposite is done for writing a '0'. See Figure 17 for waveforms.

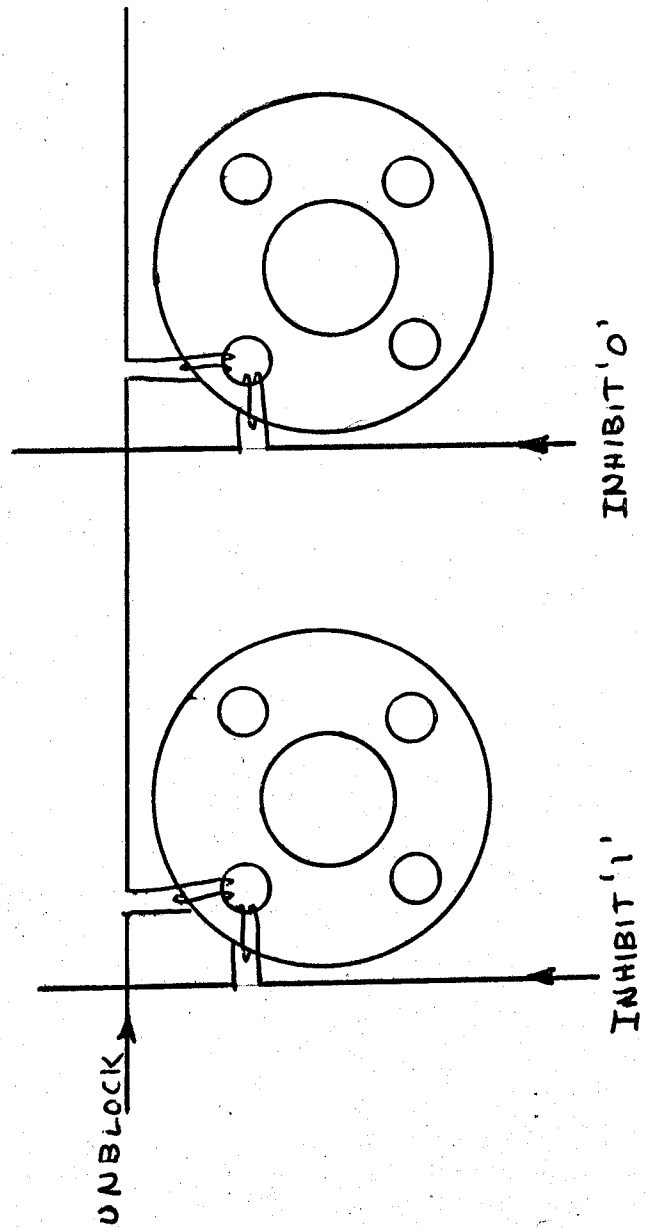


Fig. 15 SAM Write Circuit

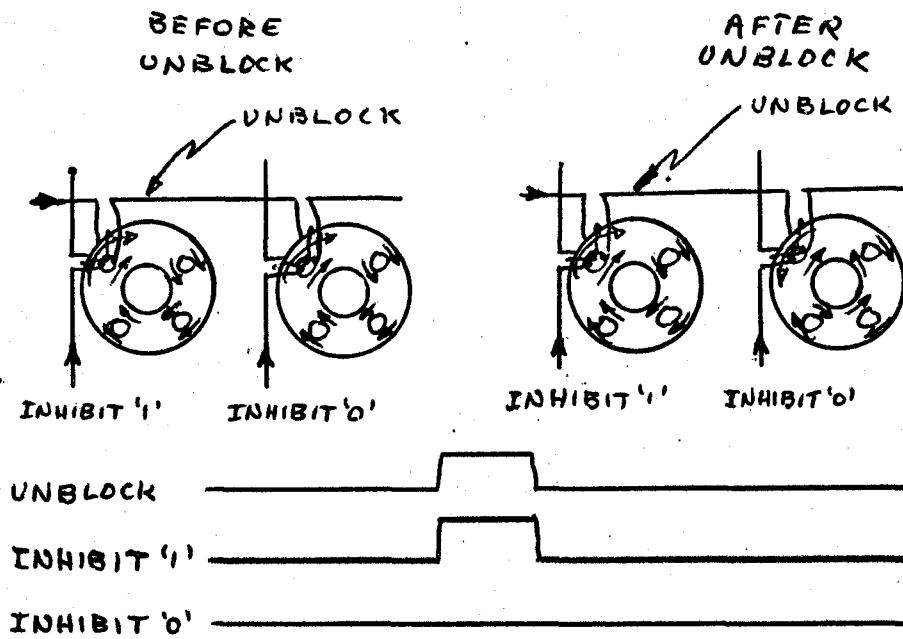


Fig. 16 Writing a '1'

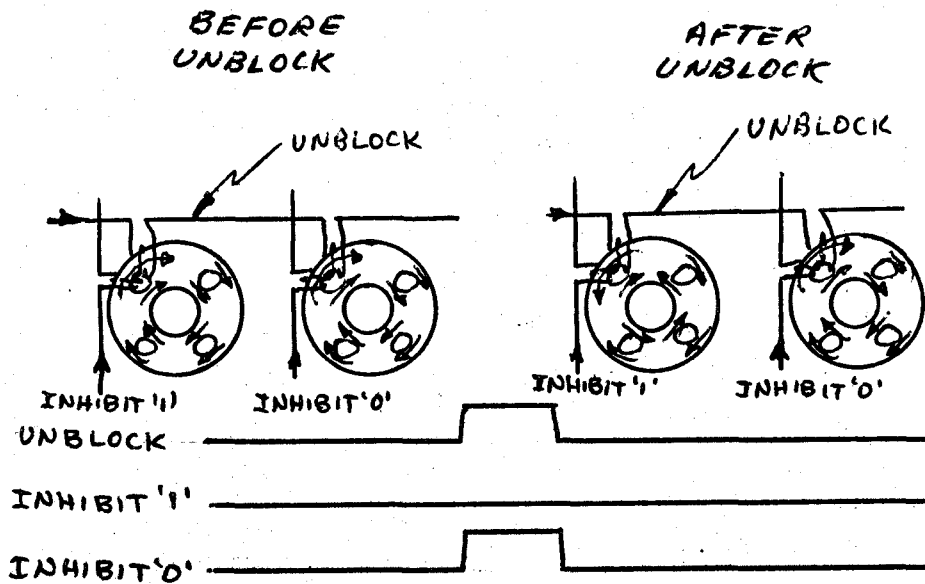


Fig. 17 Writing a '0'

4.10 The Inhibit Winding

The inhibit winding is shown in Figure 18. Consider the cores which are affected by this field although not selected. If the wire were simply passed through the minor aperture, the field would unblock the core. However, if the field is concentrated in the outer leg by making one loop, as in Figure 18, then only one-half the current is required, and the field induced in the inner leg only one-half the unblocking field. Thus, the inhibit field only affects the flux in the outer leg of the cores, and, in the case of blocked cores tends to saturate the leg in the direction in which it is already saturated. Thus there is no change. In the case of an unblocked core, the flux around the minor aperture is saturated in the clockwise direction but the core remains unblocked. See Figure 19 for wave forms and core states.

4.11 Writing Into The Machine Address Memory

The similar writing procedure is followed in the machine address memory as in the symbolic address memory. All the cores are initially blocked (at the same time as in the SAM). The unblocked line from each word in the symbolic address memory is wired to the corresponding word in the machine address memory. See Figure 20.

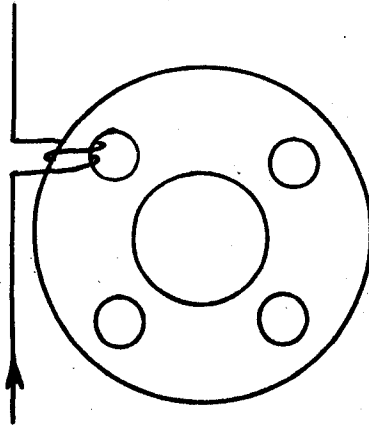


Fig. 18 The Inhibit Winding

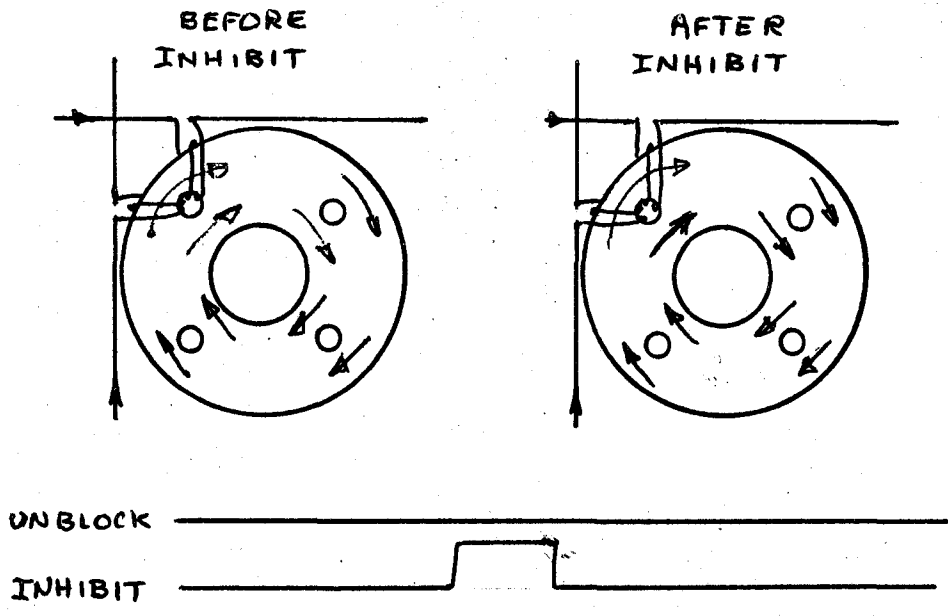


Fig. 19 Effect of Inhibit on Non-selected Cores

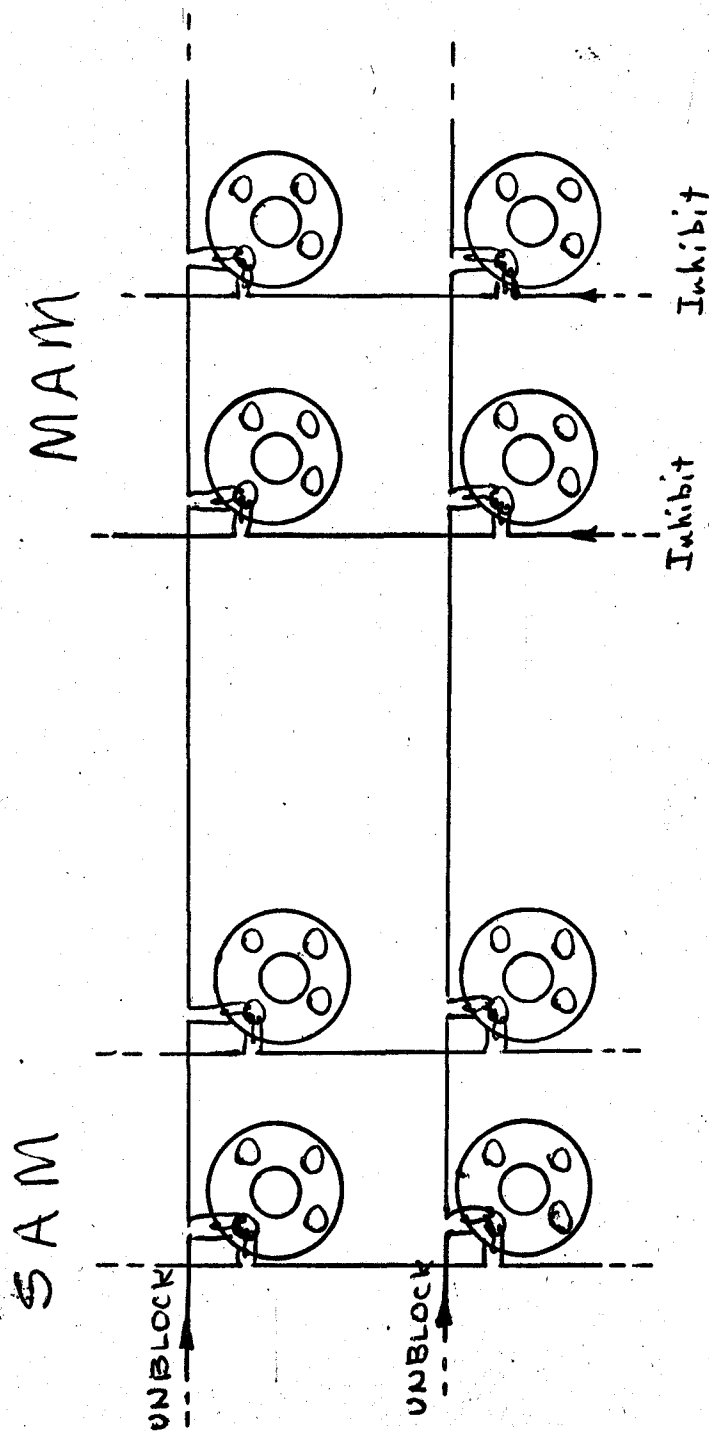


Fig. 20 Common Unblock Line

In writing '1' the inhibit field is not present and thus the core becomes unblocked. In writing a '0', the inhibit field is present and inhibits the core from becoming unblocked. Thus when the memory is interrogated a '1' is represented by a positive output, and a '0' by zero output.

4.12 Restoring The Machine Address Memory

The machine address memory also must be restored, after interrogation, to return the unblocked cores to their original state. A common restore line can be used for the entire machine address memory.

V. THE TEST MODEL

The circuit of Figure 21 was constructed to give an indication of the operational effectiveness of the design.

Two negative pulses T_0 and T_1 , of 2.5 microsecond pulses, duration and separated by 2 microseconds, were used to drive the circuit.

To enter information into this three bit word, first all six cores were first blocked by turning SW1 to block and all others to OFF, and starting the pulse train. Then certain cores were unblocked using the unblock and inhibit windings as described in section 4.8.

The word was then interrogated and restored continually with pulses T_0 and T_1 , respectively. The pulse T_0 was used to operate the strobe transistor. The effective read current was measured by observing the voltage on the collector of the strobe transistor.

The outputs for different numbers of disagreements in what was stored and what was interrogated, are shown in Figure 22.

It is seen that when there is complete coincidence, that is, when all interrogations are of blocked cores, the effective read current flows. If this wire was in fact wound on the minor aperture of a core, the core

Note:
 All transistors 2N3644;
 T_1 occurs 2 μ sec. after T_0 ;

WINDINGS:
 Block-5 turns; Interrogate-1 turn; Restore-1 turn
 Unblock-2 turns; Inhibit-2 turns; Output-2 turns

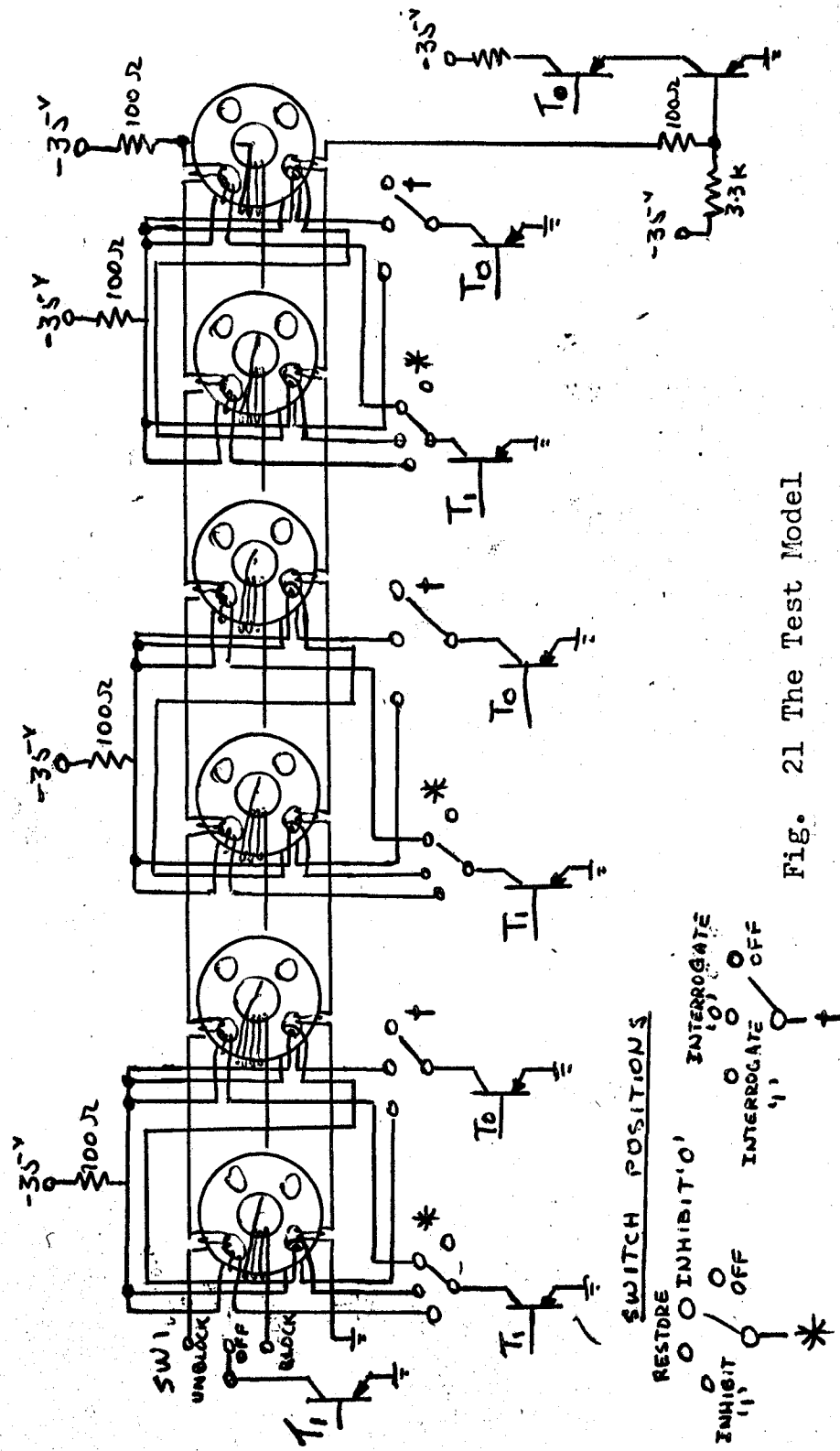


Fig. 21 The Test Model

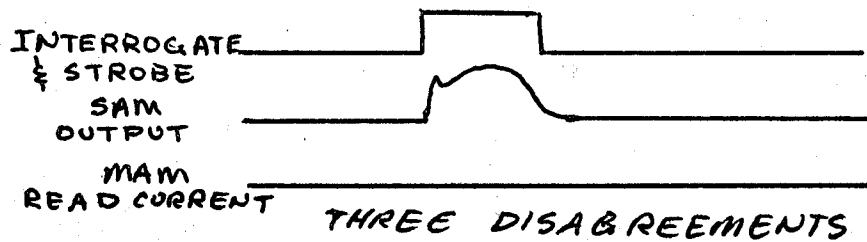
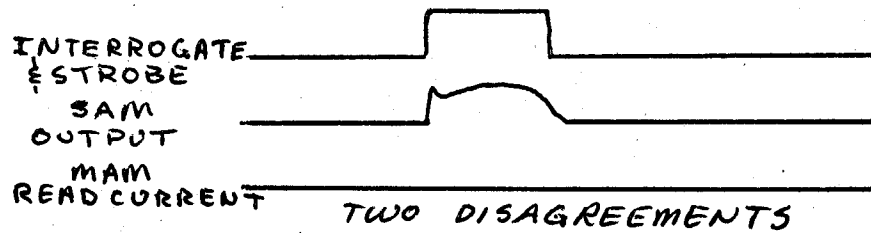
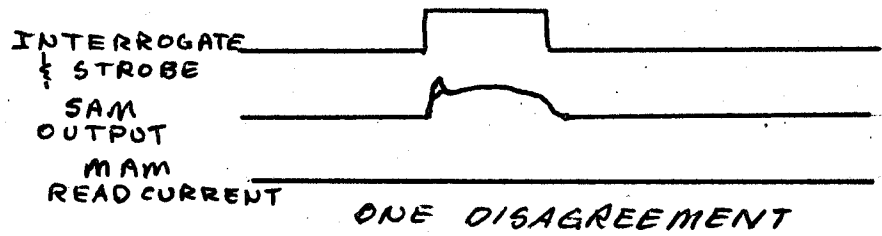
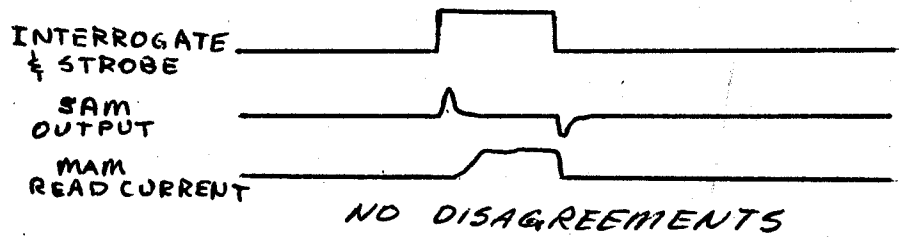


Fig. 22 Test Waveforms

would be read.

For all other cases, that is, where there is at least one disagreement, no current flows. Thus the aim of the design is achieved.

VI. RECOMMENDATIONS AND CONCLUSIONS

Before a complete hardware symbol table is constructed, it would be desirable to build a one word test model with the required number of bits. That is, if the maximum length of the symbol is 6 characters, and each character is coded with 6 bits, then the total number of bits required to code the symbol is 36. Problems, not encountered on the small model built here, may be present on a full scale model.

The results described here show that the basic design is sound and since the interrogation of the table is in parallel mode, its operation is quite fast, compared to the interrogation of a symbol table stored in the main memory.

The use of this hardware symbol is not restricted to an algebraic computer, but could be used in conventional computers to reduce translation time.

This Thesis then presents a contribution to the technology of modern electronic computers.

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VITA AUCTORIS

- 1941 Born in Toronto, Ontario.
- 1960 Completed Grade XIII at Walkerville Collegiate Institute, Windsor, Ontario.
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