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The graphic display of computer memory data.

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THE GRAPHIC DISPLAY
OF
COMPUTER MEMORY DATA

By

Satish P. Agrawal

A Thesis

Submitted to the

Faculty of Graduate Studies

through the Department of Electrical Engineering

in partial fulfilment of the requirements for the

Degree of Master of Applied Science at the University of Windsor.

Windsor, Ontario

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ABSTRACT

This thesis presents the logical design of a peripheral unit to display the contents of the memory of a computer on a cathode ray tube.

The peripheral unit is constructed with 3C and DEC logic modules and it incorporates a magnetostrictive delay line memory, two shift registers, two counters, comparator unit and gating. The peripheral unit obtains 12 bit word information from the computer and stores it in a delay line memory at the proper address. It can display up to 61 words simultaneously upon request. The contents of these words are displayed on the cathode ray tube as vertical voltage displacements.

This thesis includes a complete set of logic diagrams of the peripheral unit, which utilizes NAND logic, and the software support.

ACKNOWLEDGEMENT

The author wishes to express sincere appreciation to Dr. P.A.V. Thomas, who supervised this work, for his helpful guidance and advice.

Acknowledgement is also due to the National Research Council of Canada for financial assistance provided for this project.

TABLE OF CONTENTS

INTRODUCTION

This thesis describes a method of generating a graphic display for a computer memory using a cathode ray oscilloscope.

The display of the computer memory contents can be carried out by one of two different methods. One method is to have the data loaded into a buffer register of one of the channels of the D to A Converter from the memory with the help of programming. The analogue output voltage of the standard converter will give a voltage corresponding to the data in the memory (Ref. No. 1). This output voltage can be stored on the cathode ray oscilloscope but, in this method the cathode ray oscilloscope must have its own storage capability.

As an alternative method, a circulating serial memory is used to store the information from the computer memory. The information from this circulating serial memory can be displayed on the cathode ray oscilloscope by using the D to A Converter at the required time. (Ref. No. 4).

This thesis describes the latter method of graphic display. The advantage of the second method

is that it does not need a cathode ray oscilloscope with storage capability.

By programming, the contents of the memory are transferred in parallel from the accumulator to an input shift register in the peripheral unit using controlled gating. The peripheral unit is synchronized with the computer instructions by means of Input/ Output command pulses.

From the shift register the information is transferred serially to a delay line with the help of properly timed shift pulses. These shift pulses are generated in the peripheral unit. From the delay line, information flows serially to an output shift register and then in parallel to a Digital to Analogue Converter (D to A Converter) at the proper time by using appropriate gating. This Digital to Analogue Converter gives an output voltage according to the information stored. This output voltage is connected to the vertical input of a cathode ray oscilloscope. The time base of the cathode ray oscilloscope is also synchronized with the output of a word counter which provides the horizontal displacement on the screen. Brightness modulation is also applied to emphasise the required information.

CHAPTER I - PDP 8/S INPUT/OUTPUT

Digital Equipment Corporation's Programmed Data Processor 8/S (PDP - 8/S) is designed for use as a small scale general purpose computer.

The PDP - 8/S is a one-address, fixed word length, serial computer using a word length of 12 bits plus parity and two's complement arithmetic. It has facilities for instruction skipping and program interruption as functions of input/output device conditions.

Flexible, high capacity, input/output capabilities of the computer allow the operation of a variety of peripheral equipment. Equipment of special design is easily adapted for connection onto the PDP - 8/S system. The computer is not modified with the addition of peripheral devices.

Interface circuits for the processor allow bussed connections to a variety of peripheral equipment. Each input/output device is responsible for detecting its own selection code and for providing any necessary input or output gating. Individually programmed data transfers between the processor and

peripheral equipment takes place through the processor accumulator. Standard features of the PDP - 8/S allow the peripheral equipment to perform certain control functions such as instruction skipping and a transfer of program control when indicated by a program interrupt.

PROGRAMMED DATA TRANSFER

The bussed system of input/output transfers imposes the following requirements on the peripheral equipment. (Ref. No. 1).

I. The ability of each device to sample the select code generated by the computer during IOT instruction and when selected, to be capable of producing required sequential IOT command pulses. Circuits which perform these functions in the peripheral device are called device selectors (DS).

II. Each device receiving output data from the computer must contain gating circuits at the input of a signal information into the register when triggered by a command pulse from the DS.

III. Each device which supplies input data to the computer must contain gating circuits at the output of the transmitting register.

IV. Each device should contain a busy/ready flag (flip-flop) and gating circuits which can pulse the computer input/output skip bus upon command from the DS when the flag is set in the binary 1 state to indicate that the device is ready to transfer another item of information.

Figure 1* shows the information flow within the computer which effects the programmed data transfer with input/output equipment. All instructions stored in core memory as a program sequence are read into the memory buffer register (MBR) for execution. The transfer of the operation code in the three most significant bits (bits 0, 1, and 2) of the instruction into the instruction register (IR) takes place and is decoded to produce appropriate control signals. The computer, upon recognition of the operation code as an IOT instruction, enters a 10 micro-second cycle and enables the IOP generator to produce time sequenced IOP pulses as determined by the three least significant bits of the instructions (bits 9, 10, and 11 in the MBR). These IOP pulses and the buffered output of the select code from bits 3 - 8 of the instruction word in the MBR are bussed to device selectors in all peripheral equipment.

* All figures are given in an Appendix, 21 to 34.

DEVICE SELECTOR

Bits 3 through 8 of an IOT instruction serve as a device or sub-device select code. Bus drivers in the processor buffer both in binary 1 and 0 output signals of MBR 3-8 and distribute them to the interface connectors for bussed connection to all device selectors. Each DS is assigned a select code and is enabled only when the assigned code is present in the Memory Buffer Register (MBR). When enabled, a Device Selector (DS) regenerates IOP pulses as IOT command pulses.

CHAPTER II - PERIPHERAL UNIT - CONTROL

In the peripheral unit both 3C modules and DEC modules are used. Figure 2 shows the block diagram for the peripheral unit.

When the device is selected by the correct select code, three command pulses are generated by the Device Selector (DS). These three command pulses allow four commands to be executed with the circuit shown in Figure 3.

Program controlled command pulses do the following things in the peripheral unit. (Ref. No. 2).

I. The IOT_2 in first instruction resets the memory address counter.

II. The IOT_2 in second instruction opens the gates between Input Shift Register and Accumulator.

III. The IOT_4 turns the write flag on.

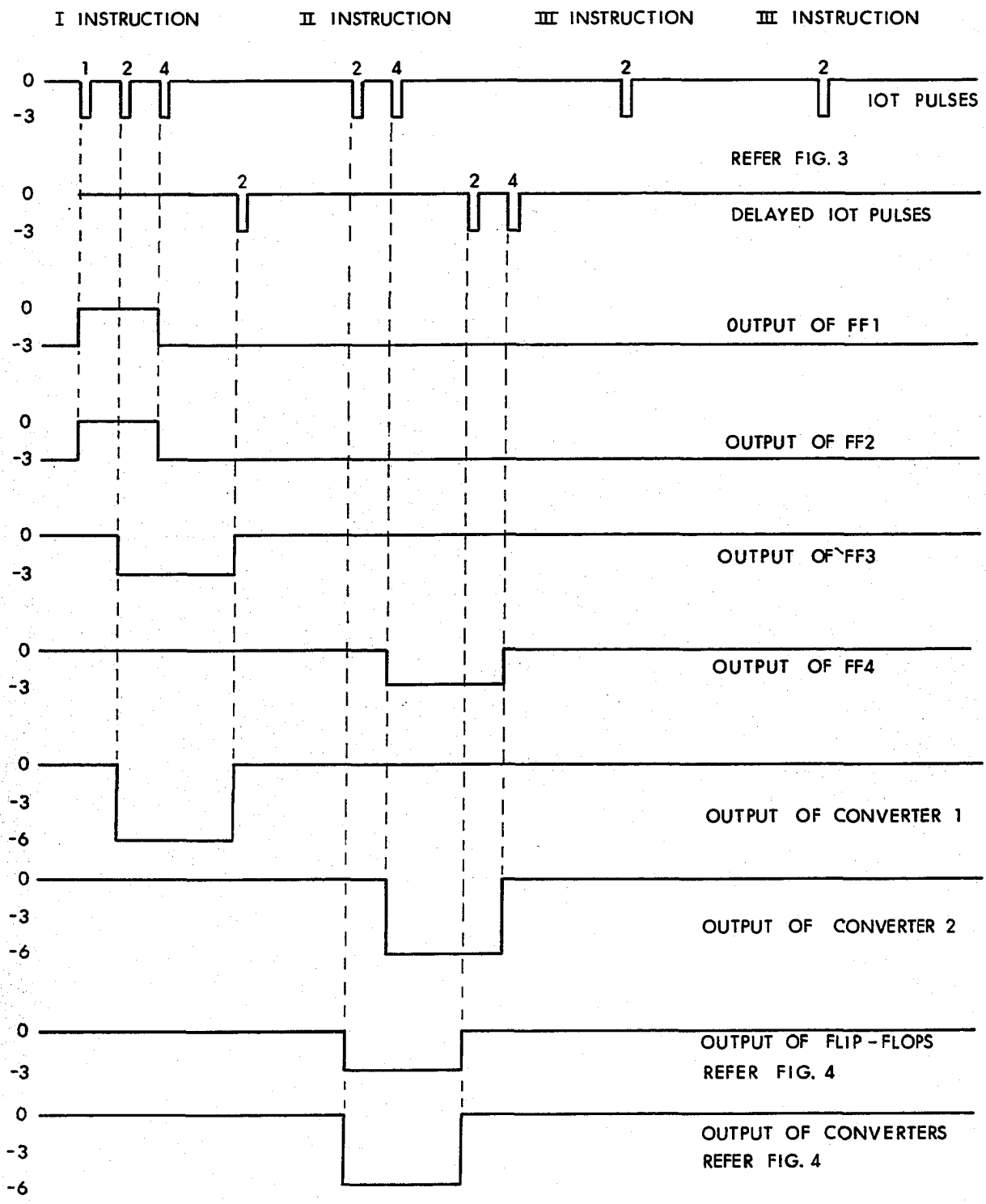
The compare unit compares the contents of the M.A. Counter and Word Counter. On match and while the write flag is on, the Compare Unit generates logic '1' output at time pulse T_0. This output and pulse train T_1 - T_{12} are gated and used for shifting information from

Input Shift Register to Serial Memory. The entry of information to Serial Memory is gated with the output of the Compare Unit. Pulse train T_1 - T_{12} is also used to shift information from The Serial Memory to the Output Shift Register. The time pulse T_{13} increases the contents of the Word Counter by binary 1. Pulse T_{13} opens gating between the Output Shift Register and the Digital to Analogue Converter and also turns off the write flag which gives a signal to Computer to start the next cycle. Time pulse $\overline{T}_{14}$ turns off the Compare Unit.

Standard logic levels of the PDP - 8/S and DEC modules are -3V to OV and the pulse width is 100 nano seconds. The standard logic voltage levels for the 3C modules are -6V and OV and the pulse width is 2.5 micro-seconds. Therefore, when signals are fed from the PDP - 8/S to the 3C moduels, the voltage levels and width of pulses must be changed accordingly.

GATING BETWEEN ACCUMULATOR (AC) & SHIFT REGISTER (SR)

As IOT pulses are generated by the Device Selector (DEC module) and fed to 3C modules, the width and level for these pulses must be converted accordingly. For this conversion delays, flip-flops, and voltage converters are used as shown in Figure 3 and 4. The process is described in the following waveform diagram.



WAVEFORM DIAGRAM Figure

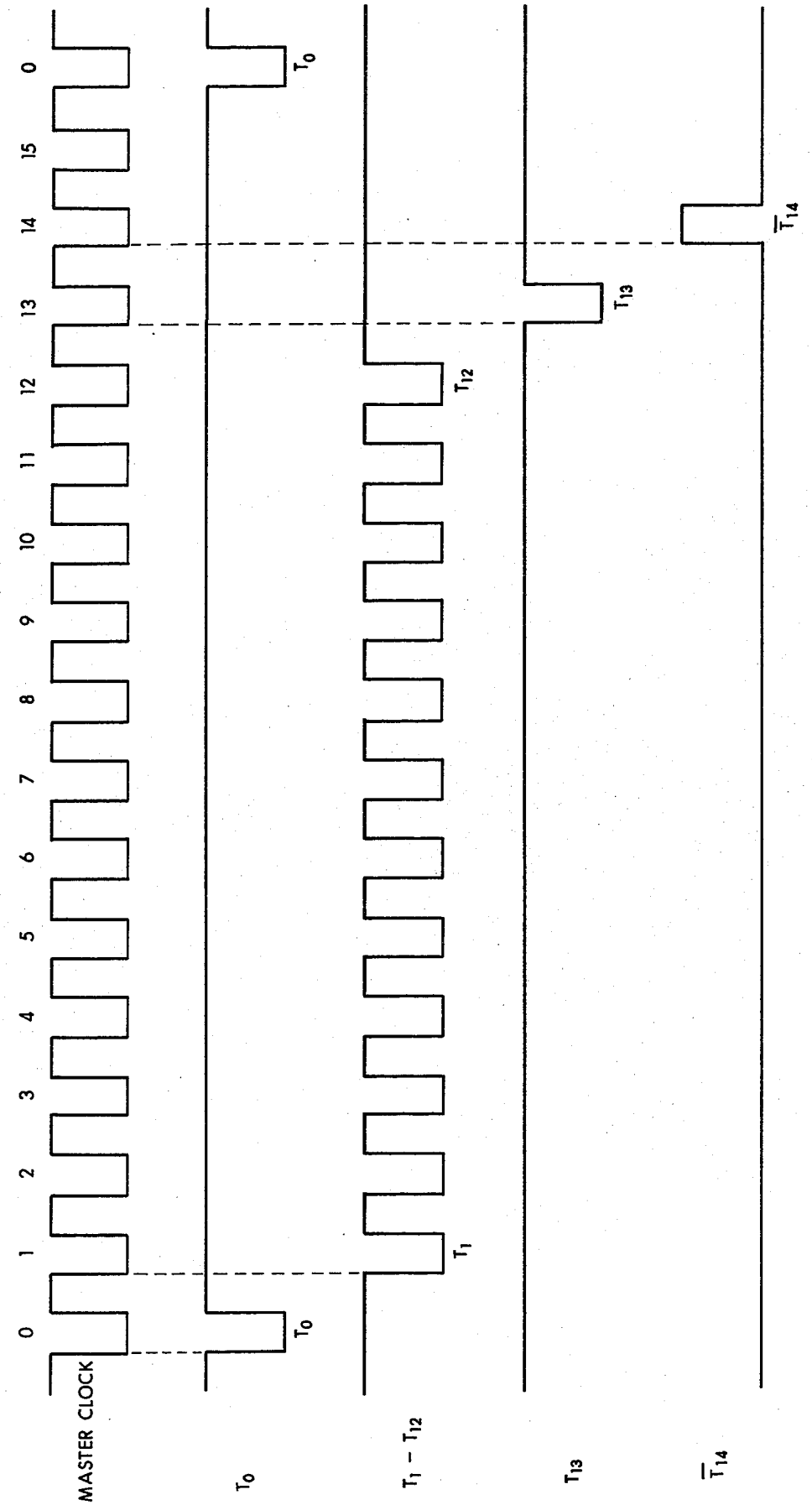
The first instruction in the program selects the device and generates three pulses: (a) IOT_1, resets the flip-flop FF_1 and FF_2. (b) IOT_2, sets the flip-flop FF_3. The delay IOT_2 resets the flip-flop, FF_3. The output of FF_3, after voltage conversion, clears the memory address counter. (c) IOT_4, sets the flip-flop FF_1 and FF_2.

IOT_2 in the second instruction is used to transfer information from the AC to the Input Shift Register. To convert the voltage level and with of the signals, the same principle is used. IOT_2 in the third instruction is used to test the skip flag. There is no conversion needed for this as it moves in only DEC modules.

The IOT_2 pulse opens the NAND gates and sets or resets the flip-flop according to the information in the AC. After a delay of 3 micro-seconds, produced by the delay unit, the same IOT_2 is used to clear all the flip-flops. The output of each flip-flop is connected to a negative output converter, which converts the voltage levels to -6V and 0V. Each output of the converters corresponding to a '1' sets a flip-flop of the input SR. The method used is shown in Figure 4.

TIMING UNIT

A timing unit provides separate timing signals T_0, T_{13} and $\overline{T}_{14}$ and also a pulse train T_1 - T_{12}. This is clarified in the following figures:



TIME-CONTROLLED PULSES

Figure

These time pulses are generated by means of a Bit Counter, Master Clock and decoders as shown in Figure 5.

The master clock, operating at a frequency of 200 KHZ, supplies a continuous train of 2.5 microsecond pulses, T. A four stage bit counter counts the pulses, T, in order to provide a binary count of zero to fifteen, as shown in Figure 6 together with the waveforms. The desired timing pulses are then generated using the logic given in the diagram in Figure 7.

DELAY LINE MEMORY ADDRESSING

A 6-stage word counter counts the words in the delay line. As the delay line has a capacity of 61 words of 16 bits at the frequency of 200 KHZ the word counter counts in binary from 0 to 60.

A 6-stage memory address counter MA gives the memory address. The number in it is compared with the number in the word counter by the compare unit. In this way the word is stored in the delay line serial memory at the correct place.

The diagrams for this addressing are shown in Figures 8, 9 and 10.

SHIFT REGISTER

There are two shift registers in the peripheral unit. One is used for parallel data input and converts to a serial output for the delay line and the other has a serial input from the delay line and parallel output to the digital-analogue converter.

Both shift registers are of 12 bits and have the capability of right shifting. The shifting pulses clear all the bits of the input register. For both shift register the pulse train T_1 - T_{12} are used as shifting pulses. The details are shown in Figure 11 for the input register and Figure 12 for the output register.

DELAY LINE STORE

The recirculating magnetostrictive delay line is an intregal element of the S-PAC system that stores serial binary data. Magnetostrictive delay lines are passive electromechanical devices capable of delaying electrical signals. They reduce the velocity of an electrical signal by converting it to an acoustic wave and then reconverting it to an electrical signal. The delay line pack includes AND gating logic for entering information into the memory and a flip-flop to provide both assertion and negation outputs, as shown in Figure 13.

The delay line stores 61 data words of 12 bits each of which is separated by four spacer bits to make up a word of 16 bits. The data words appear in serial mode at the output of the delay line with the least significant bit coming first, and are recirculated to form a continuous, sequential access memory.

Bits appear at the output of the delay line at the rate of 200 K bits per second, or 5 micro-seconds apart. The delay line has a delay of 4,880 micro-seconds and stores 976 bits of information, (ie. 61 words of 16 bits each). (Ref. No. 3).

DIGITAL TO ANALOGUE CONVERTER

To convert binary information into analogue information three module types A601 are used as shown in Figure 14.

D to A Converter receives the 8 least significant bits from the output shift register as binary information in parallel and generates a coresponding analogue output voltage, ranging from 0V to -10V. Therefore, when all the 8 input bits have logic '1' the output voltage is zero volts and when all the 8 input bits have logic '0' the output voltage is -10V. This implies that the least significant bit of 8 input bits has an effect on output voltage of 0.04 volts, ie. 1 part in 256, which

is sufficient accuracy on CRO. The T_1 - T_{12} pulse train is used to shift the information and the T_{13} pulse is used to transfer the binary information from output shift register to the D to A Converter. To supply a reference voltage supply of -10V to the D to A Converter a DEC module type A702 is used. The corresponding analogue output voltage is fed to the vertical deflector of the cathode ray tube.

CHAPTER III - SOFTWARE SUPPORT & RESULTS OBTAINED

Software for displaying the contents of memory of the computer is minimal being only required to check the freedom of the peripheral unit and transfer the data from AC to the peripheral unit.

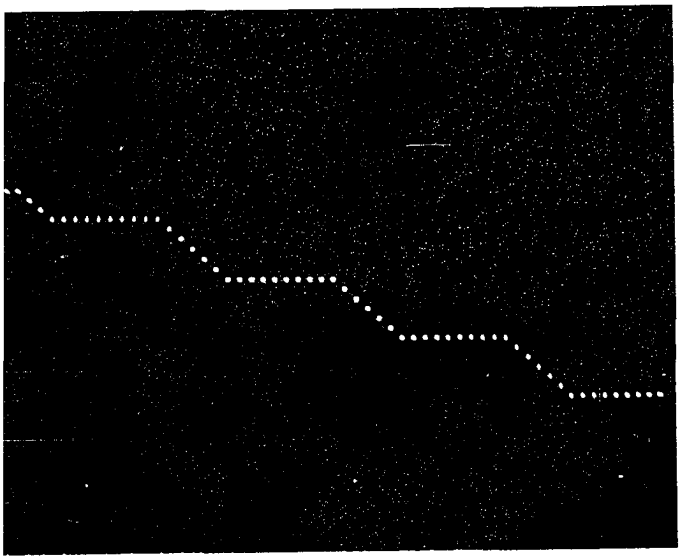
In the particular instance the device code 44 has been used and the appropriate instructions are as follows:

6447	Initialize M.A. Counter and control cycle.
6446	Load display buffer and set flag
6442	Skip if display flag = 1.

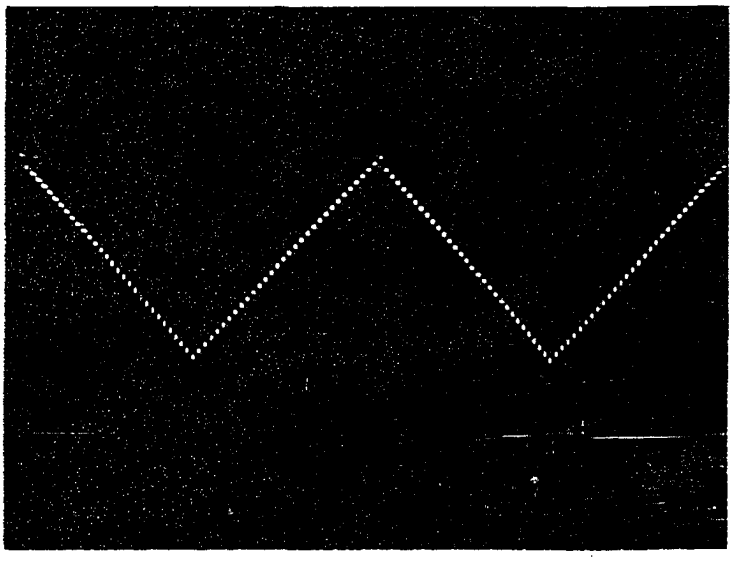
A typical program for display 61 values of data is shown below :

```
                    *4ØØ
ØØØØ      6447      6447
ØØØ1      73ØØ      CLA CLL
ØØØ2      122Ø      TAD INDEX
ØØØ3      3Ø1Ø      DCA Z 1Ø
ØØØ4      73ØØ      INITL,CLA CLL
ØØØ5      141Ø      TAD I Z 1Ø
ØØØ6      6446      6446
ØØØ7      6442      6442
ØØ1Ø      52Ø7      JMP.-1
ØØ11      2217      ISZ N
ØØ12      52Ø4      JMP INITL
ØØ13      72ØØ      CLA
ØØ14      1221      TAD N1
ØØ15      3217      DCA N
ØØ16      74Ø2      HLT
ØØ17      77Ø3      N,-75
ØØ2Ø      ØØ77      INDEX,477
ØØ21      77Ø3      N1,-75
                    *5ØØ
```

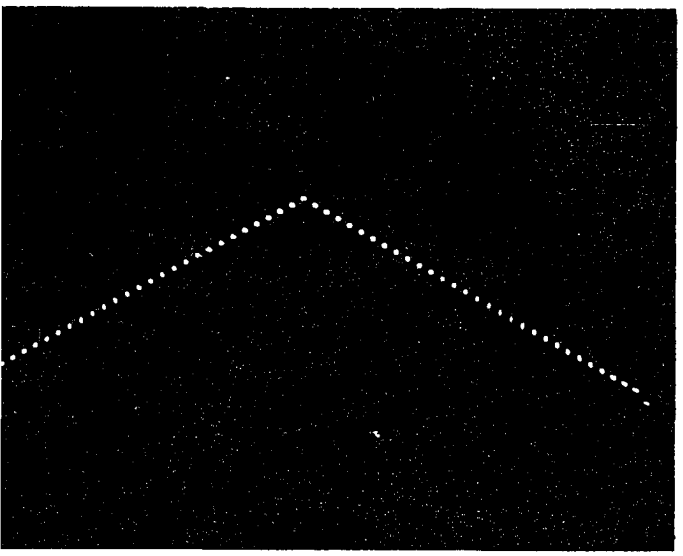
The results obtained for a series of values of data are shown in the following photographs for the above particular programs, photograph 2 shows that in memory location 500 the least 8 bits are logic'1'. Therefore, the output from the D to A Converter is OV. Then contents of each next location is reduced by a certain number which gives incrementing negative voltage with respect to time. When all 8 bits are logic '0' the contents of memory start increasing by a certain number until all bits are again at logic '1'. In this photograph 2 cycles are shown. In photograph 3 the data has the same nature as in photograph 2. In photograph 4 the contents is increasing by a certain number and after a half cycle it again starts from the beginning. In this way any type of memory content can be displayed on the CRO.



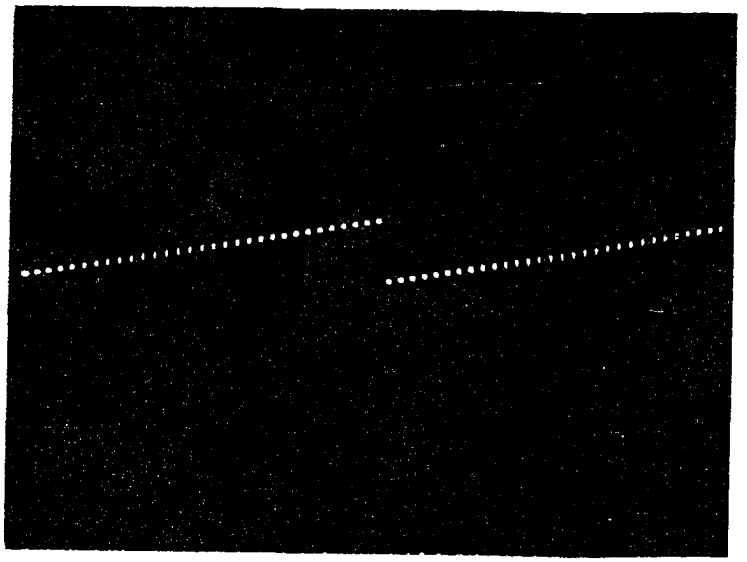
Photograph 1



Photograph 2



Photograph 3



Photograph 4

Photographic Results

CONCLUSIONS AND RECOMMENDATIONS

A peripheral unit to display the computer memory content has been constructed and tested. It is felt that the design achieves its goal of displaying a table of values stored in a computer memory. If a large serial memory could be used in the peripheral unit a greater part of memory could be displayed on the screen at any time. Also by using modules of one manufacturer only, this design would be less complicated and hence cheaper.

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L. C. Hobbs
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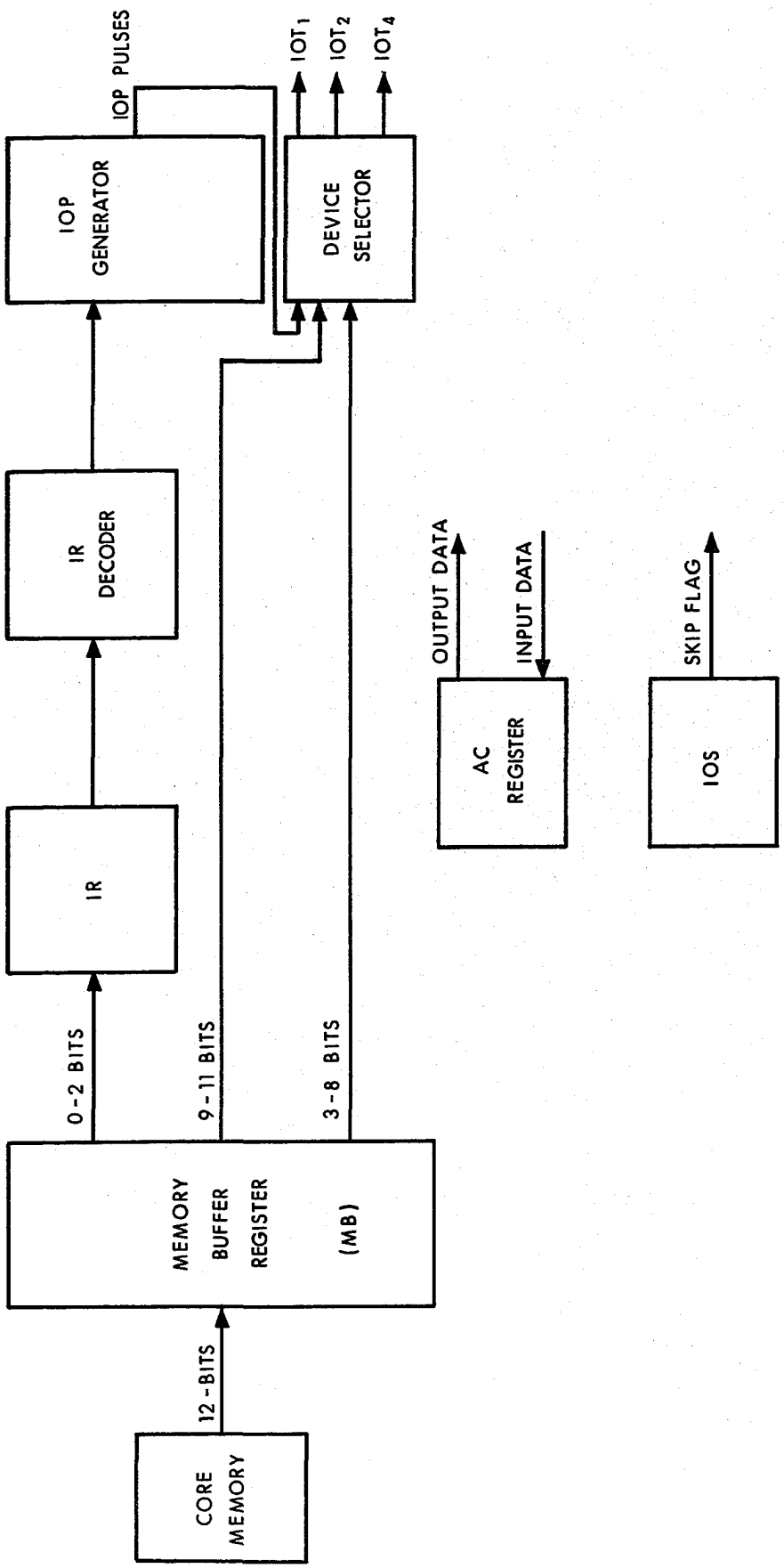


INFORMATION FLOW WITHIN THE COMPUTER

Figure 1

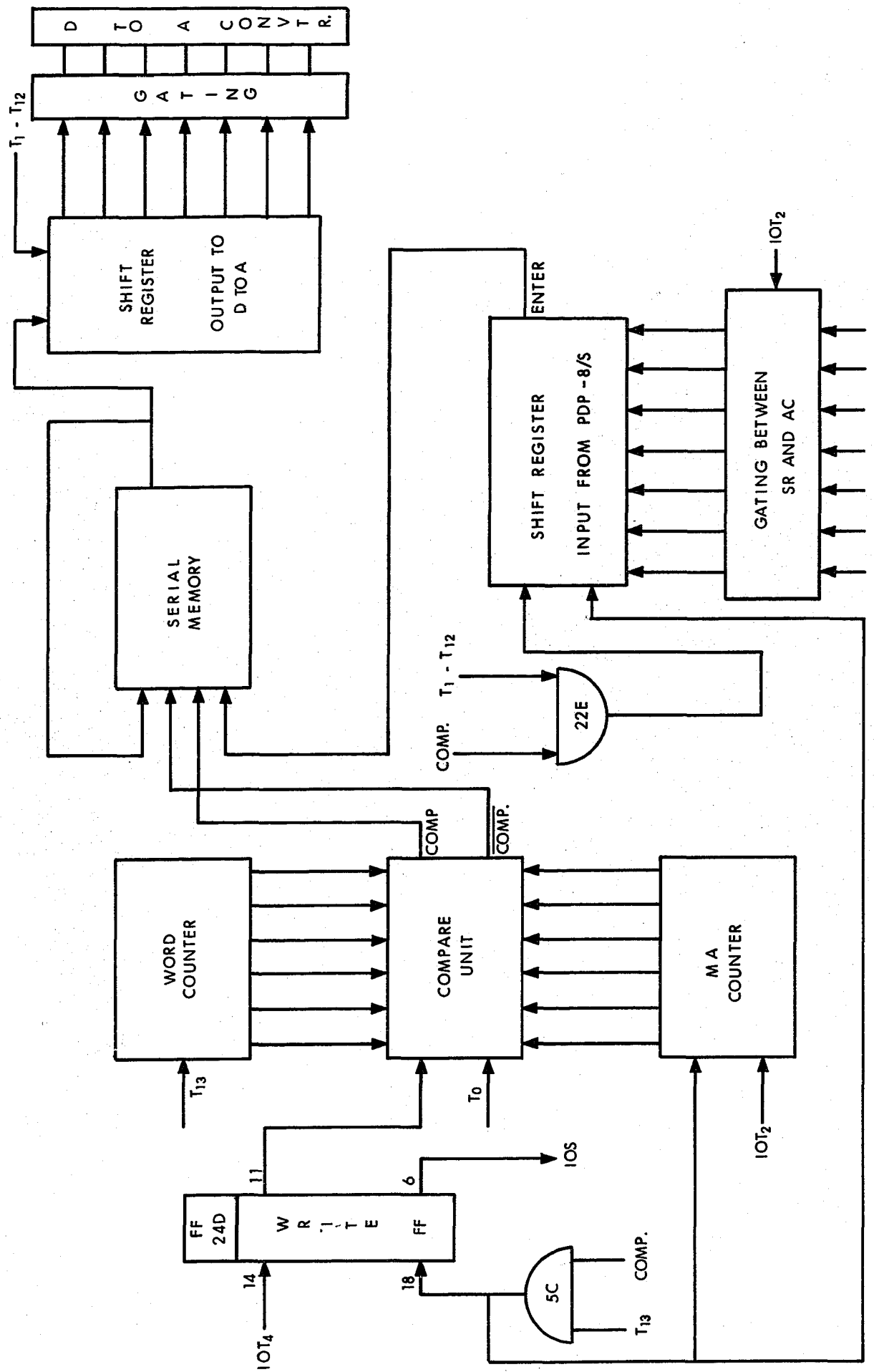


Figure 2

BLOCK DIAGRAM OF PERIPHERAL UNIT

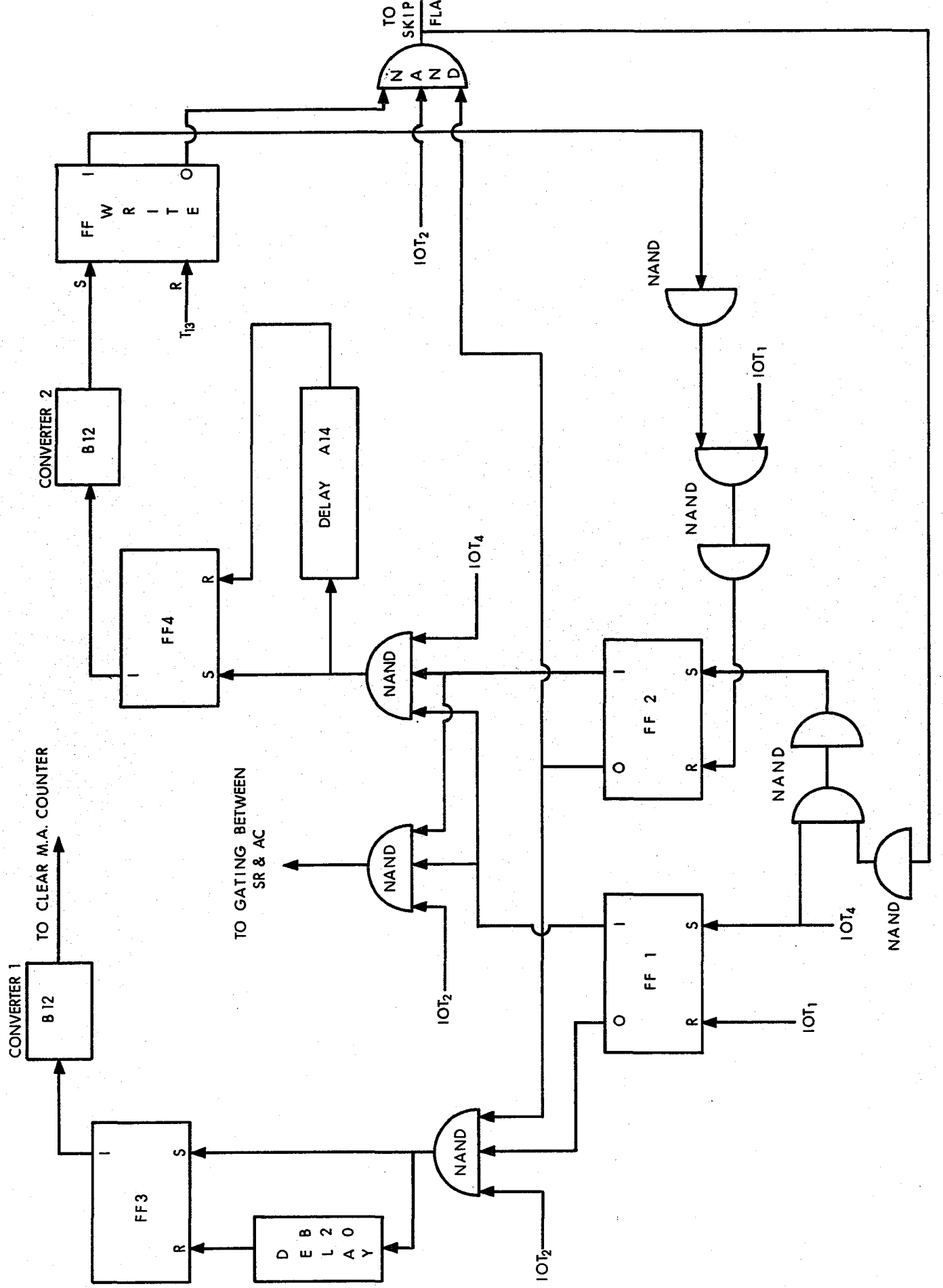
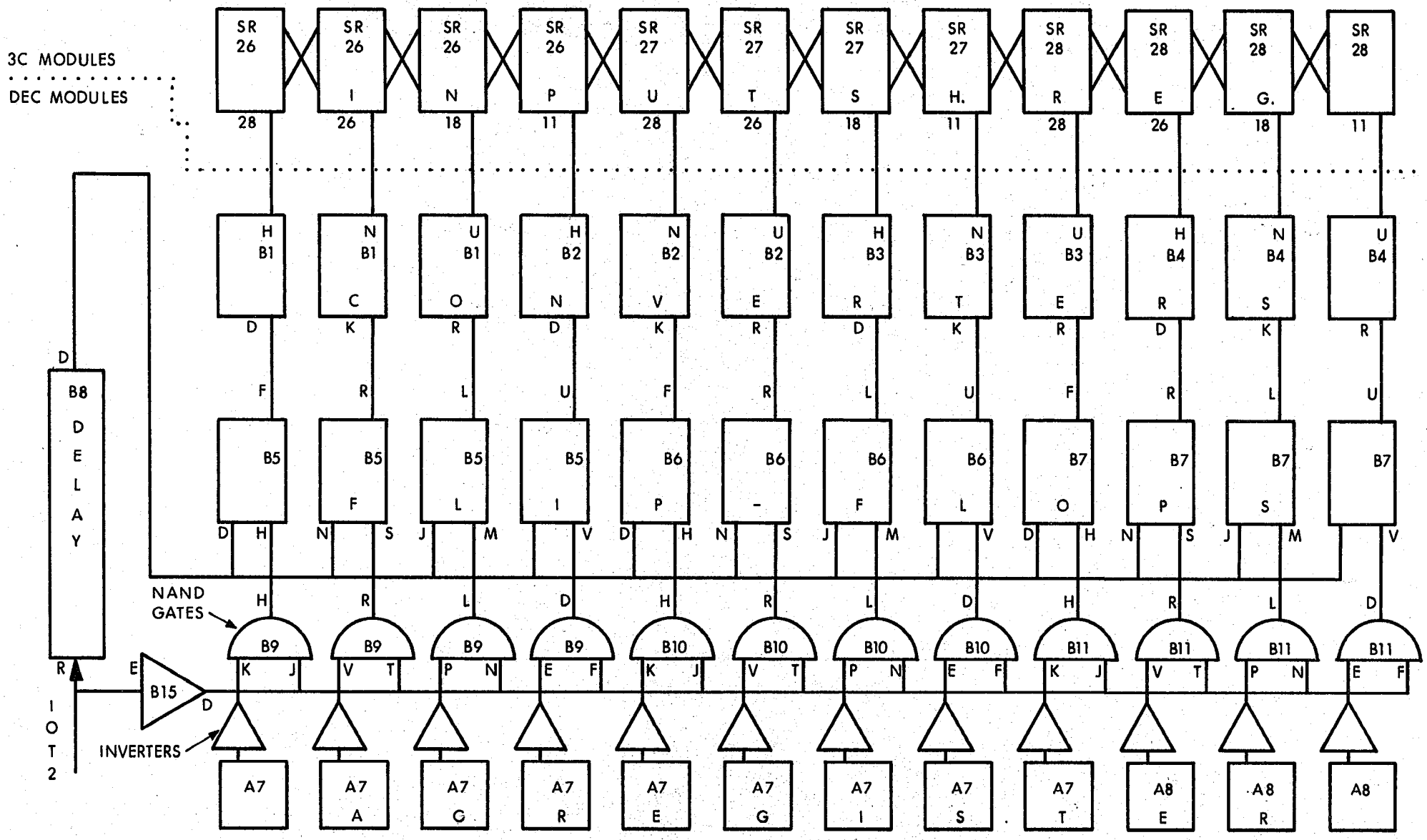


Figure 3



GATING BETWEEN PDP 8/S AND PERIPHERAL UNIT

Figure 4

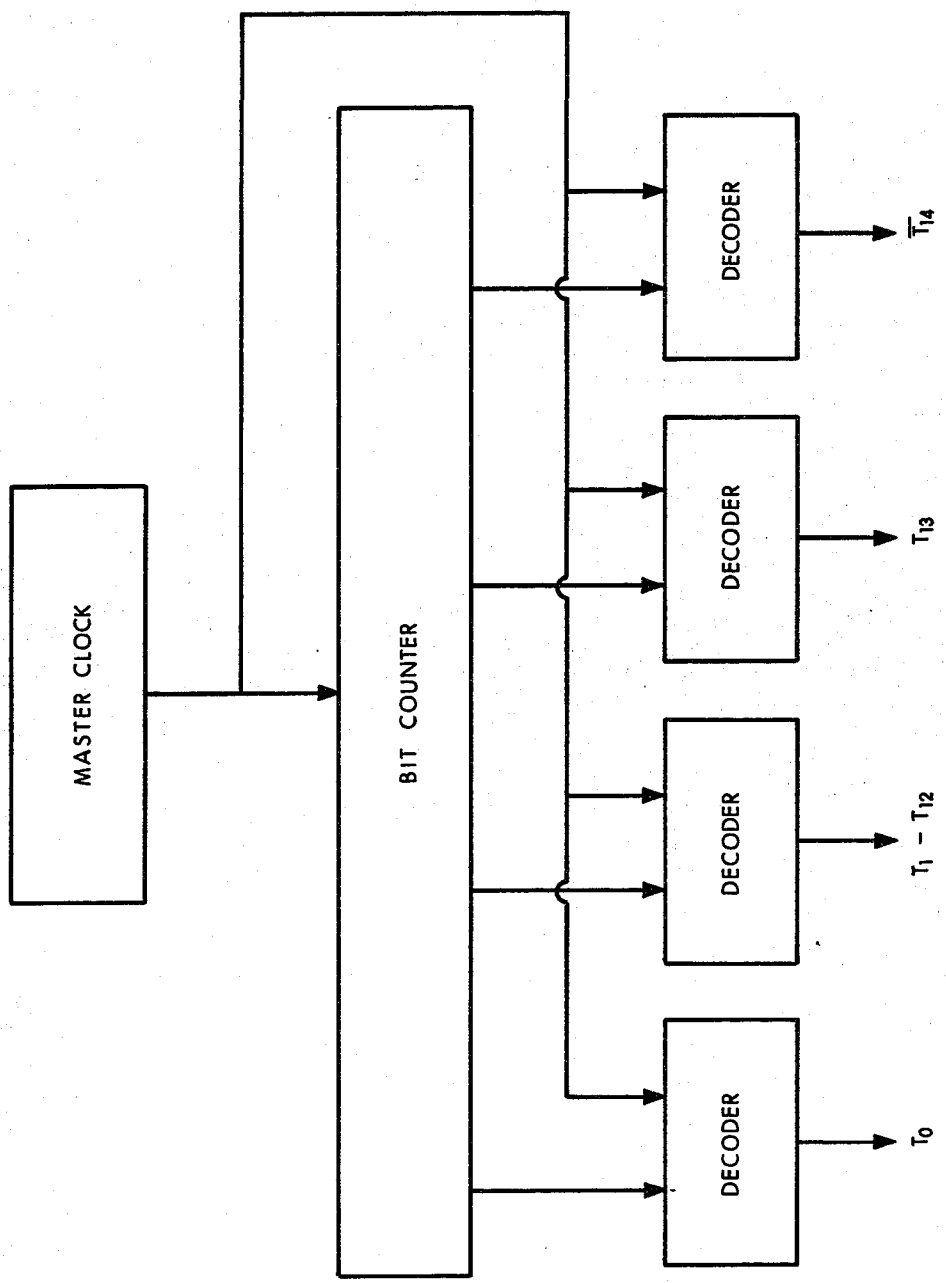
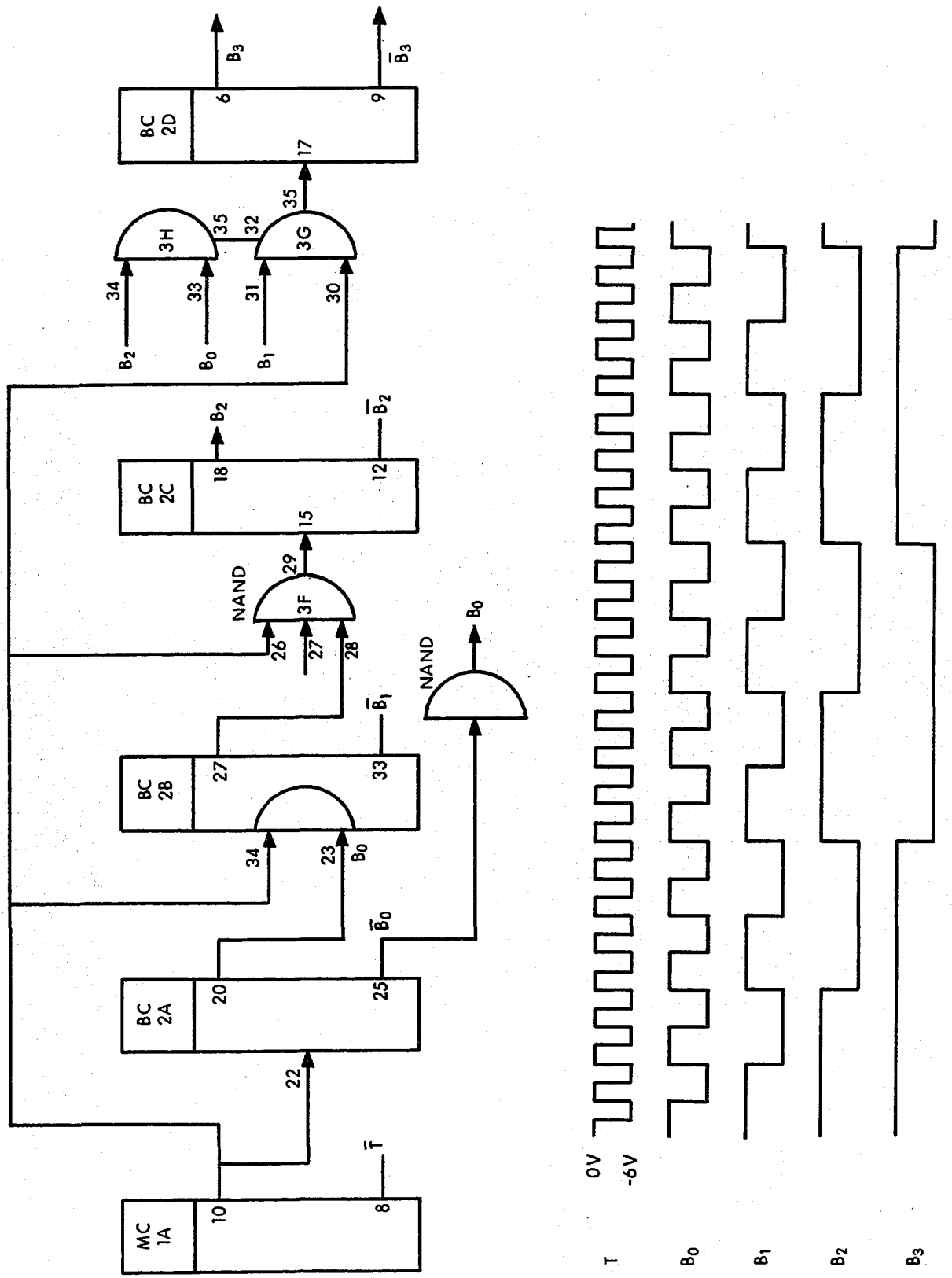


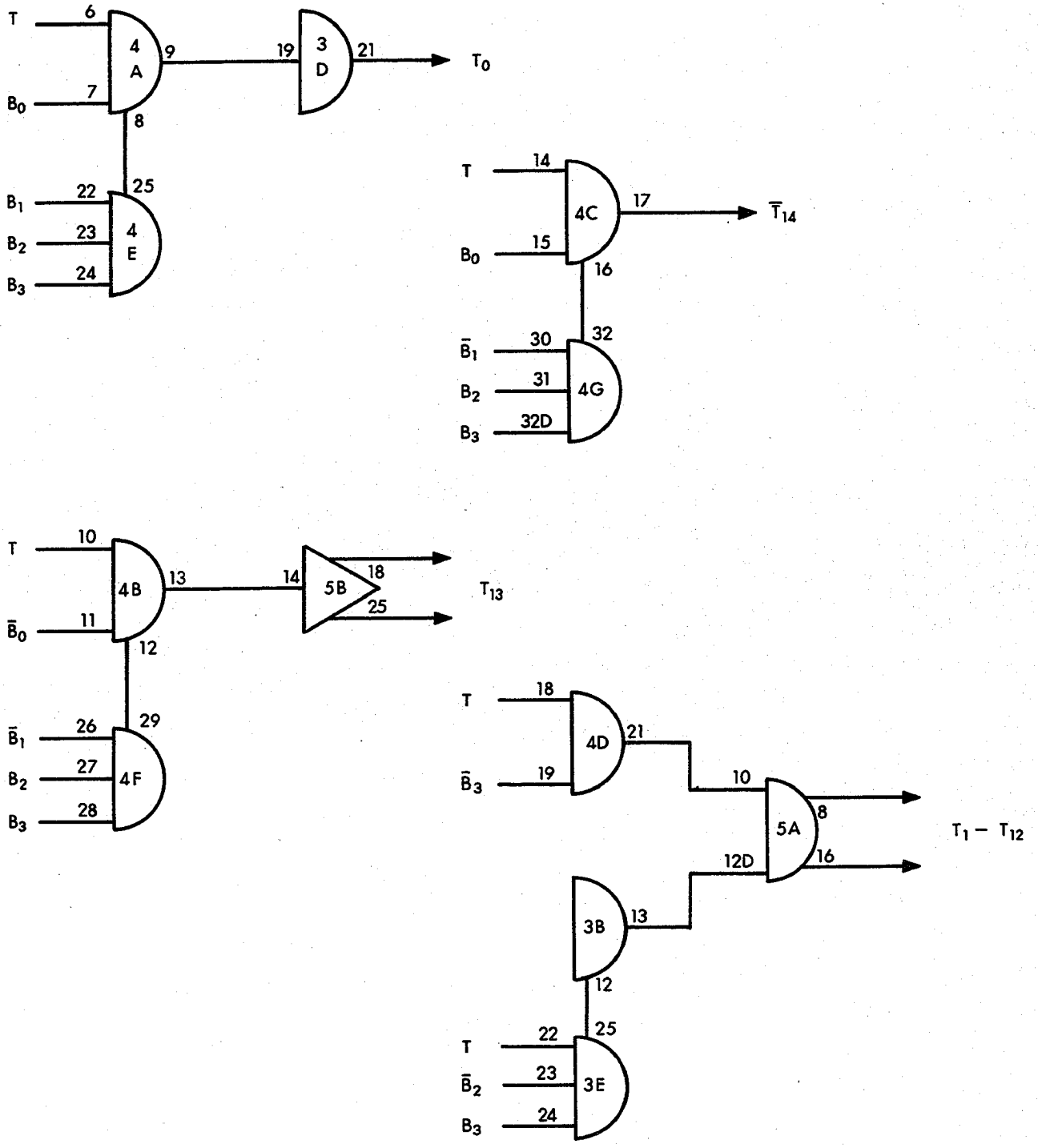
Figure 5

BLOCK DIAGRAM OF TIME CONTROL UNIT



BIT COUNTER

Figure 6



TIMING UNIT

Figure 7

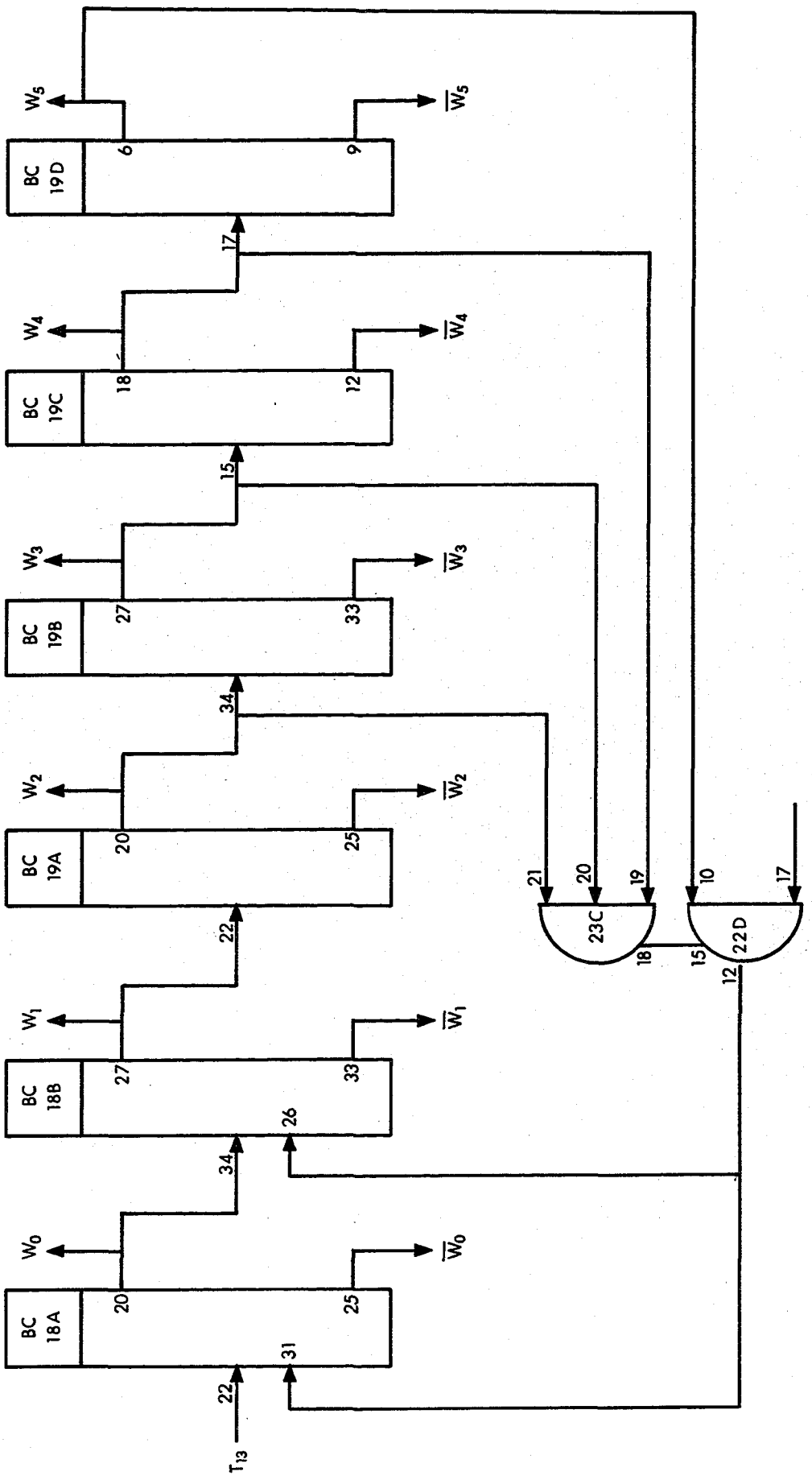
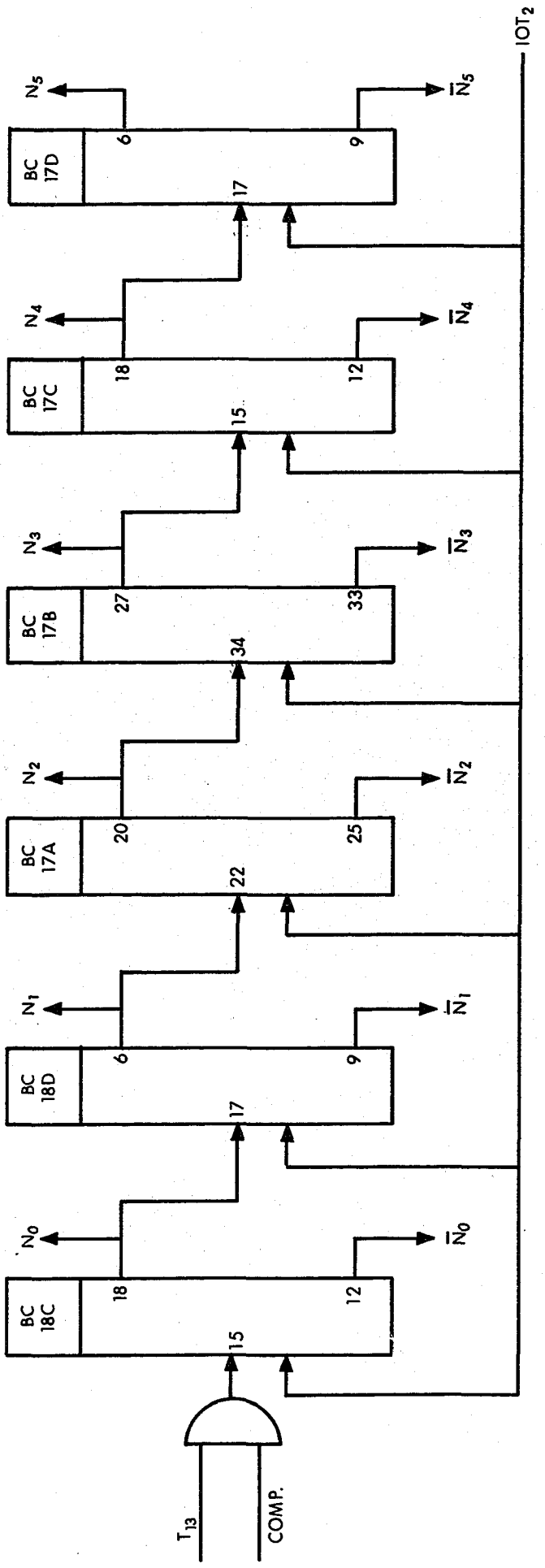
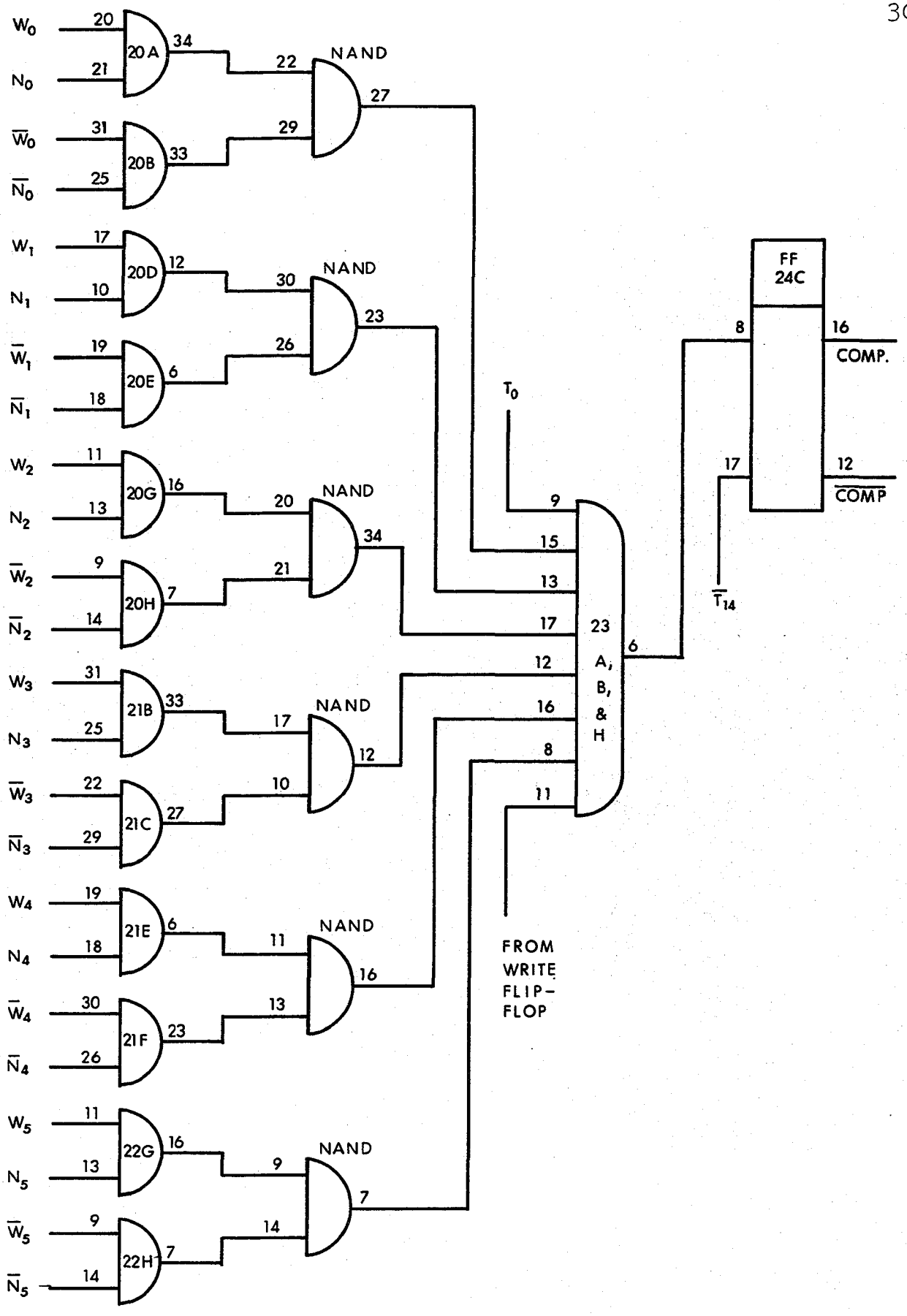


Figure 8

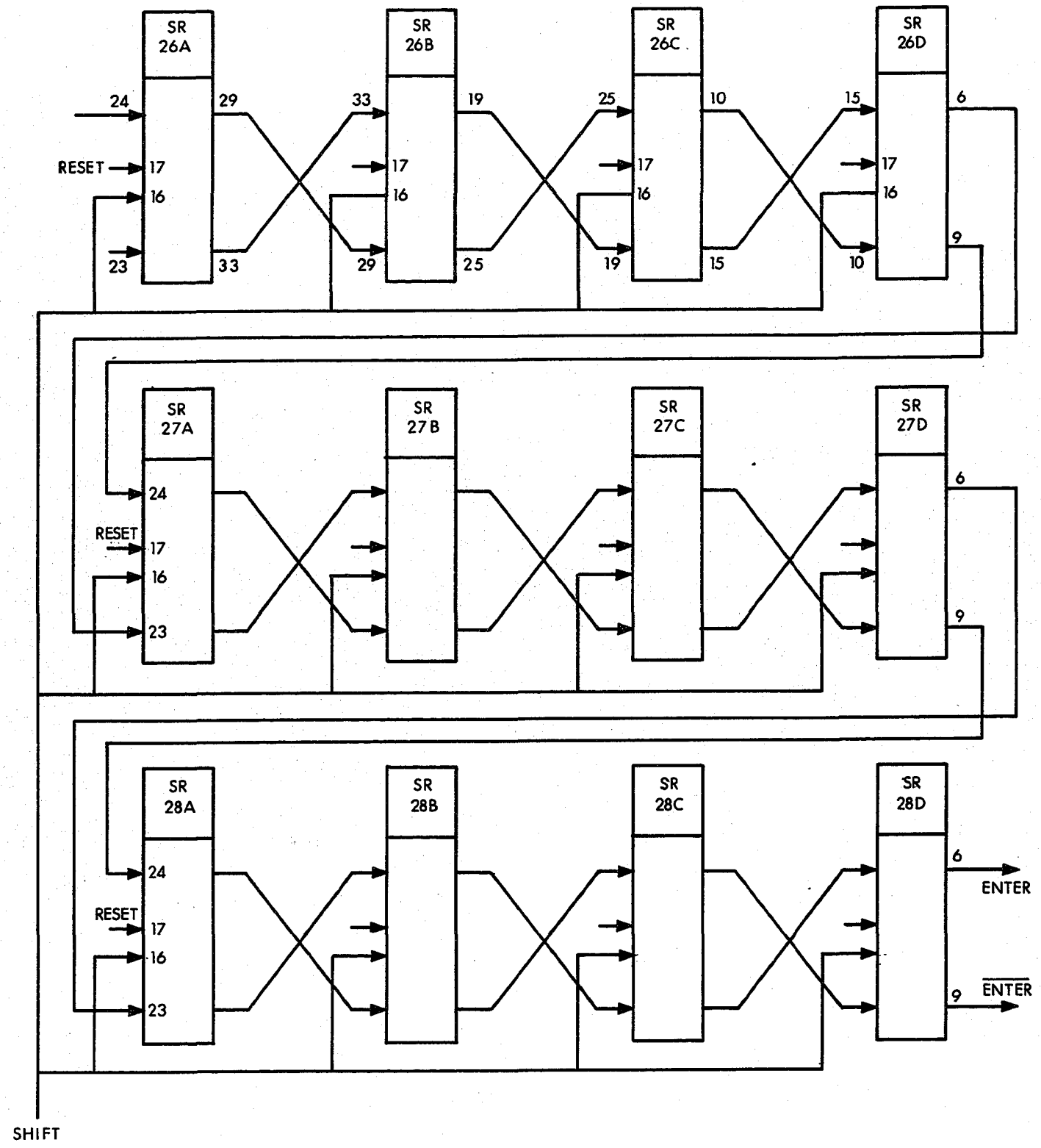


M.A. COUNTER

Figure 9

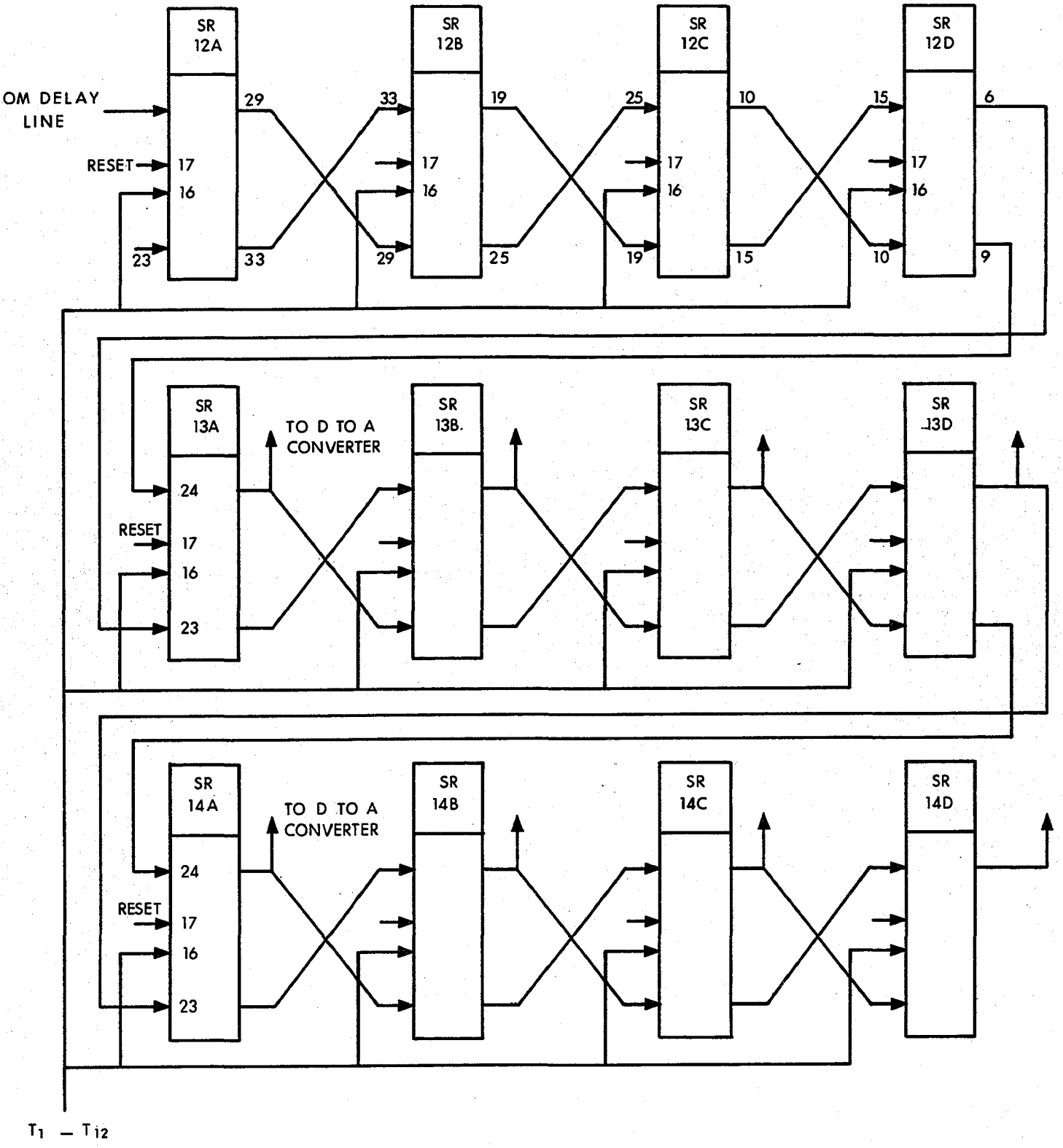


COMPARE UNIT Figure 10



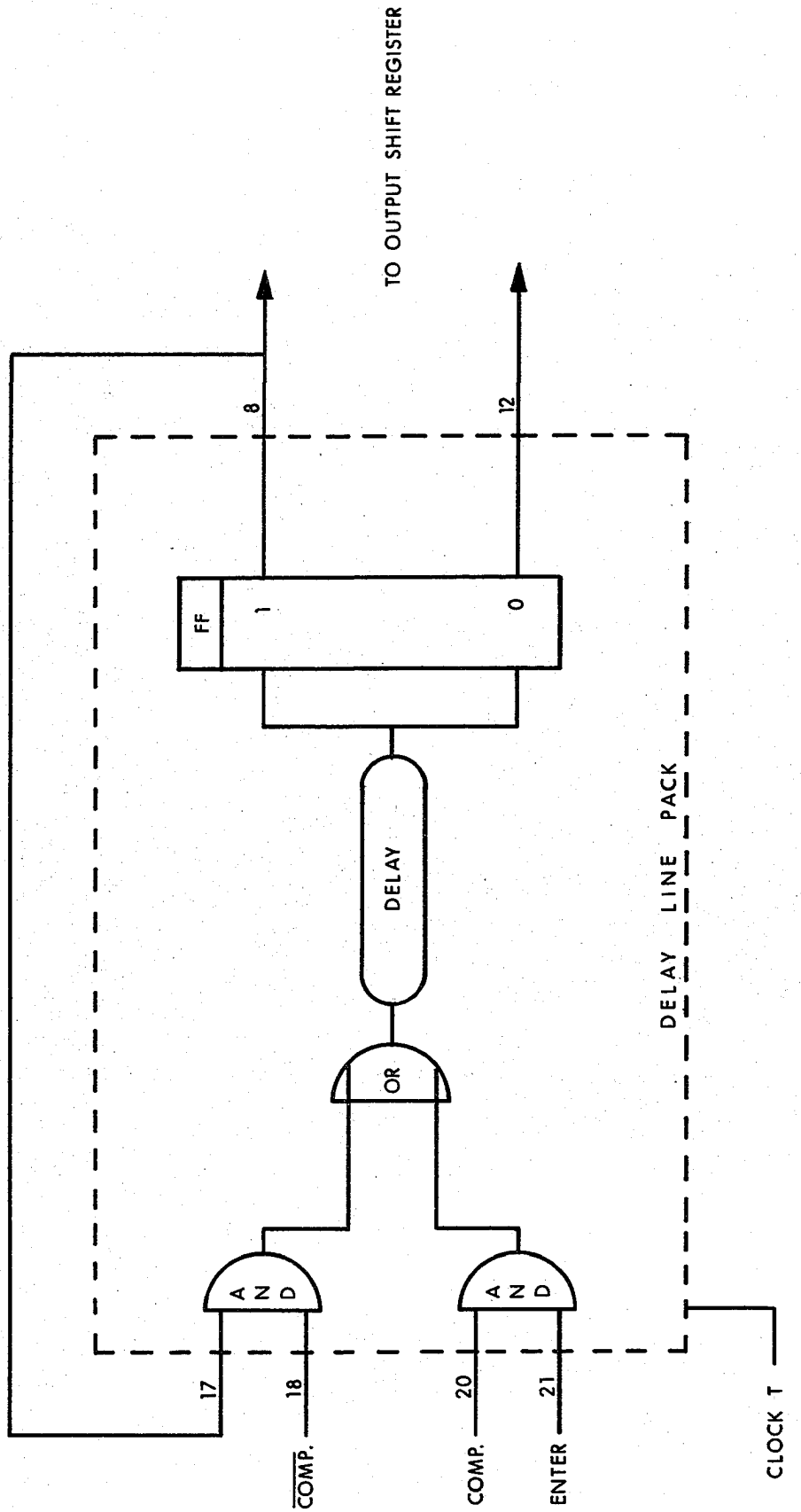
INPUT SHIFT REGISTER

Figure 11



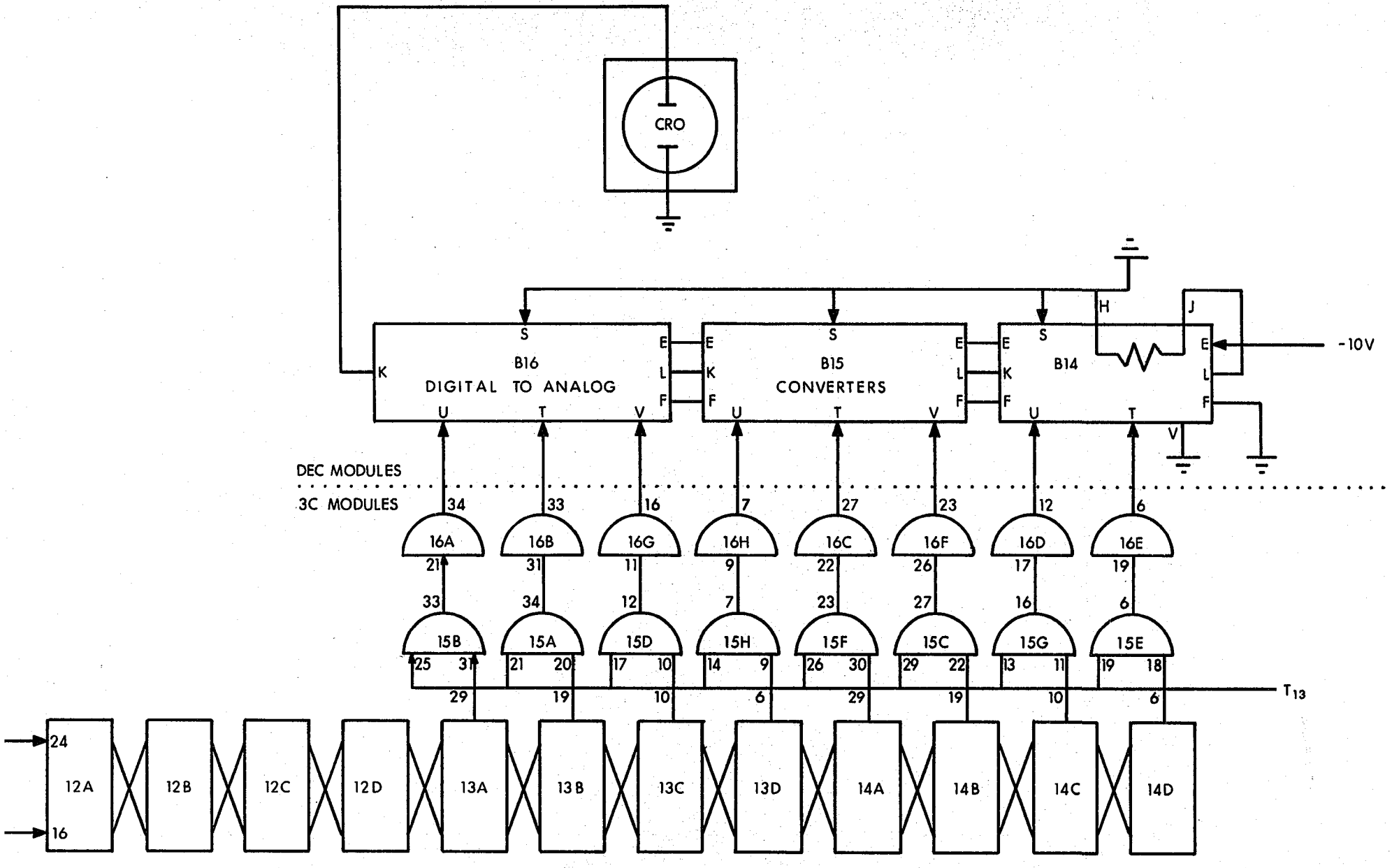
OUTPUT SHIFT REGISTER

Figure 12



DELAY LINE STORE

Figure 13



DIGITAL TO ANALOG CONVERSION

Figure 14

VITA AUCTORIS

1944	Born on October 3rd, in Mathura, INDIA
1961	Completed High School at K.R. Inter College, Mathura, INDIA
1962	Completed B.Sc. (Part I) at B.S.A. College, Mathura, INDIA
1966	Graduated from Engineering College, Dayal Bagh, Agra, INDIA, with degree of B.Sc. (Engg) in Electrical Engineering.
1969	Candidate for M.A.Sc. Degree in Electrical Engineering at the University of Windsor, Windsor, (Ontario), Canada.