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A Low Temperature Co-fired Ceramic (LTCC) Interposer Based Three-Dimensional Stacked Wire Bondless Power Module

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A Low Temperature Co-fired Ceramic (LTCC) Interposer Based Three-Dimensional Stacked Wire Bondless Power Module

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by

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Abstract

The objective of this dissertation research is to develop a low temperature co-fired ceramic (LTCC) interposer-based module-level 3-D wire bondless stacked power module. As part of the dissertation work, the 3-D wire bondless stack is designed, simulated, fabricated and characterized. The 3-D wire bondless stack is realized with two stand-alone power modules in a half-bridge configuration. Each stand-alone power module consists of two 1200 V 25 A silicon insulated-gate bipolar transistor (IGBT) devices in parallel and two 1200 V 20 A Schottky barrier diodes (SBD) in an antiparallel configuration. A novel interconnection scheme with conductive clamps and a spring loaded LTCC interposer is introduced to establish electrical connection between the stand-alone power modules to connect them in series to realize a half-bridge stack. Process development to fabricate the LTCC based 3-D stack is performed.

In traditional power modules, wire bonds are used as a top side interconnections that introduce additional parasitic inductance in the current conduction path and prone to failure mechanism under high thermomechanical stresses. The loop inductance of the proposed 3-D half-bridge module exhibits 71% lower parasitic inductance compared to a wire bonded module. The 3-D stack exhibits better switching performance compared to the wire bonded counterpart. The measurement results for the 3-D stack shows 30% decrease in current overshoot at turn-on and 43% voltage overshoot at turn-off compared to the wire bonded module. Through measurements, it has been shown that the conducted noise reduces by 20 dB in the frequency range 20-30 MHz for the 3-D stack compared to the wire bonded counterpart.

A simulation methodology using co-simulation techniques using ANSYS EM software tools is developed to predict EMI of a power module. Hardware verification of the proposed simulation

methodology is performed to validate the co-simulation technique. The correlation coefficient between the measurement and simulation is found to be 0.73. It is shown that 53% of the variability in the simulation can be explained by the simulated result. Moreover, the simulated and measured amplitudes of the EMI spectrum closely match with each other with some variations due to round-off errors due to the FFT conversion.

Acknowledgements

I would like to convey my sincere gratitude and appreciation to my research advisor Dr. Simon S. Ang for his unconditional support and advice throughout my dissertation work. I wouldn't have completed the dissertation work without the support that Dr. Ang has provided me throughout the years of my degree.

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Lastly, I want to mention about my parents, Shekhar Dutta and Ava Dutta. They always encouraged and motivated me to pursue a Ph.D. degree. They have always been the greatest inspiration and support of my life. Whatever I am as a person today, it is due to their support and affection from the very day I was born.

Dedication

This dissertation research is dedicated to my parents, Shekhar Dutta and Ava Dutta. They have been the greatest source of inspiration and support of my life.

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List of Published Papers

Chapter 7 consists of a published IEEE paper with the following citation:

A. Dutta and S. S. Ang, "Electromagnetic Interference Simulations for Wide-Bandgap Power Electronic Modules," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 757-766, Sept. 2016.
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Chapter 1 Introduction

1.1 Background and Motivation

With the advent of fast switching wide bandgap semiconductor devices, such as silicon carbide and gallium nitride, power packaging has become a challenge [1]-[12]. The theoretical limits of wide bandgap devices, for example, silicon carbide exhibit hundred times faster switching speed, four times higher operating temperature, ten times higher blocking voltage, five times higher current density, lower switching losses compared to their silicon counterparts [13]. However, packaging technologies, new materials available to package wide bandgap devices are the primary preventive factors in achieving these high theoretical limits. The existing packaging technologies for silicon devices are not optimized for silicon carbide, as such, newer optimized packaging technologies need to be investigated to utilize the full potential of wide bandgap devices.

High voltage and high current power modules require several power semiconductor devices/modules to be connected in series and parallel to achieve the specific rating for an application. However, series and parallel connection of several devices require larger substrate area that introduces parasitic inductance, unbalanced current/voltage sharing, unequal operating temperature between the devices in the package. Moreover, connecting several power modules in series and parallel introduces additional DC bus inductances that are undesirable to achieve optimum switching efficiency of the power devices/modules. Failure to address these aspects from a packaging standpoint can give rise to reliability issues and reduce the life cycle of the devices and the power modules [14].

In traditional power module packaging approach, wire bonds are used as top side (gate/emitter for IGBTs, gate/source for MOSFETs, anode for diodes) electrical connection for power semiconductor devices [15]. Wire bonds introduce additional parasitic inductance in the current conduction loop and prone to mechanical failure at high operating temperatures due to thermomechanical stresses [16]-[18].

Press-pack packaging technology from ABB excludes wire bonds from the power module structure. Instead of wire bonds, the top side interconnection is achieved by pressure contact using spring pin. The spring pins are placed directly on the top side electrode pads to make direct contact [19]-[21]. However, due to the coefficient of thermal expansion (CTE) mismatch, different thermal and mechanical properties, the contact materials become subject to high thermomechanical stress and strains during operation. Due to high junction temperature and a wide range of temperature variations, these mechanical interfaces become fatigued and the metallization on the electrode pads on the devices gradually wear away, termed as fretting [22]. This ultimately results in the failure of the power devices.

In this dissertation research, a module-level press-pack structure is proposed. In the proposed module-level press-pack structure the semiconductor devices are attached to the power substrate using flip-chip die attach method as opposed to direct spring contacts on the electrode pads of the devices to avoid fretting in device level press-pack. A half-bridge module-level press-pack structure is realized using two stand-alone power modules each consisting of a switching position to represent the high and low side switching positions of a half-bridge power module.

1.2 Objective of Dissertation

The objective of this dissertation research is to design and develop a novel module-level three-dimensional (3-D) wire bondless half-bridge stack for semiconductor devices. Design, simulation, fabrication, and characterization of the 3-D wire bondless stack are performed as part of this dissertation research. The characterization of the 3-D wire bondless half-bridge power module is performed and compared with the characteristics of a traditional wire bonded power module in terms of parasitic inductance, switching performance, and electromagnetic interference (EMI) response.

The module level 3-D wire bondless half-bridge stack is in general based on the following:

a) The 3-D stack consists of two wire bondless stand-alone power modules. Each stand-alone wire bondless modules represent a switching position (high and low side) of the half-bridge module consists of two 1200 V 25 A silicon IGBT devices in parallel with two 1200 V 36 A Schottky barrier in an antiparallel configuration.
b) The two stand-alone wire bondless power modules are connected in series with a novel interconnection technique.
c) The interconnection between the two stacked modules will be achieved through:
    i. An array of spring loaded mechanical contacts embedded into low temperature co-fired ceramic (LTCC) substrate [24].
    ii. Conductive clamps to establish electrical connection between both sides of DBC copper metallization.
d) Top and bottom holding frames to hold the stand-alone wire bondless power modules [24].

In addition to the module level 3-D stack, the scope of this dissertation research will incorporate the development of a simulation methodology and hardware validation of the methodology to predict the electromagnetic interference in the design phase of the power module using ANSYS EM tools. A correlation study will be performed to correlate the simulation and measurement.

1.3 Organization of Dissertation

This dissertation research is organized in the following way:

In Chapter 2, the design of the 3-D wire bondless half-bridge stack is presented. The detailed design process using various software platforms are illustrated. In Chapter 3, the electrical, thermal simulation results for the 3-D wire bondless half-bridge stack are presented. Parasitic inductance of the 3-D stacked module is extracted for all current conducting paths. The effect of connector placement on parasitic inductance is investigated and optimum connector placement to minimize loop inductance is performed. High voltage simulation to validate the 3-D stack structure is performed. Thermal simulations are also presented. In Chapter 4, a comparison between the proposed 3-D wire bondless half-bridge power module and a traditional wire bonded power module is performed in terms of parasitic inductance and switching performance. It is shown through simulations using co-simulation techniques that the proposed 3-D wire bondless power module exhibits better switching performance compared to a wire bonded power module. In Chapter 5, the detailed process flow is presented to fabricate the proposed 3-D wire bondless half-bridge stacked power module. In Chapter 6, the characterization of the proposed module is performed. Double pulse test is carried out to characterize the switching behaviors of the proposed power module and compare the results with switching performance of a traditional wire bonded power module. EMI response of the proposed power module is compared with the traditional power module. The static characteristic of the power modules is measured to

investigate the influence of packaging on device characteristics. High voltage leakage current measurement is performed to investigate the insulation resistance to validate the power module architecture. In Chapter 7, a simulation methodology to predict electromagnetic interference in the design phase of a power module is proposed. The simulation methodology incorporates co-simulation technique using ANSYS EM tools to predict EMI [23]. The simulation methodology is validated by hardware measurements. In Chapter 8, conclusions for this dissertation research is drawn and some possible proposed future work is listed to set the direction for continued research.

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Chapter 2 Design of 3-D Wire Bondless Half-Bridge Stacked Power Module

In this chapter, the detailed design of the module level 3-D wire bondless half-bridge stacked power module is presented. The proposed wire bondless 3-D half-bridge power module consists of several individual components. The primary building blocks for the proposed 3-D stack are as follows:

i. Two wire bondless power modules
ii. Spring loaded low temperature co-fired ceramic (LTCC) interposer
iii. Top and bottom holding frames
iv. Clamping screws

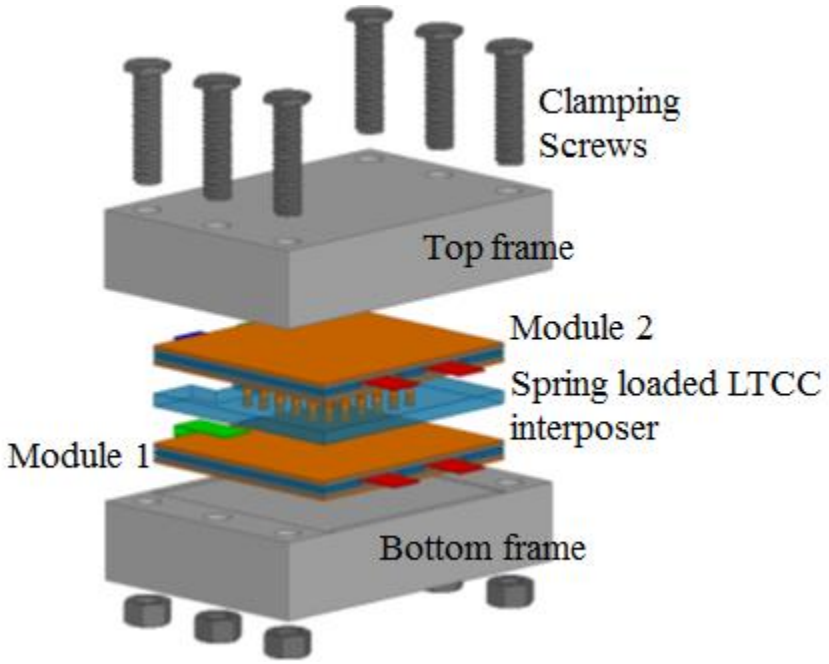

Fig. 2.1. Exploded view of the 3-D stacked wire bondless power module

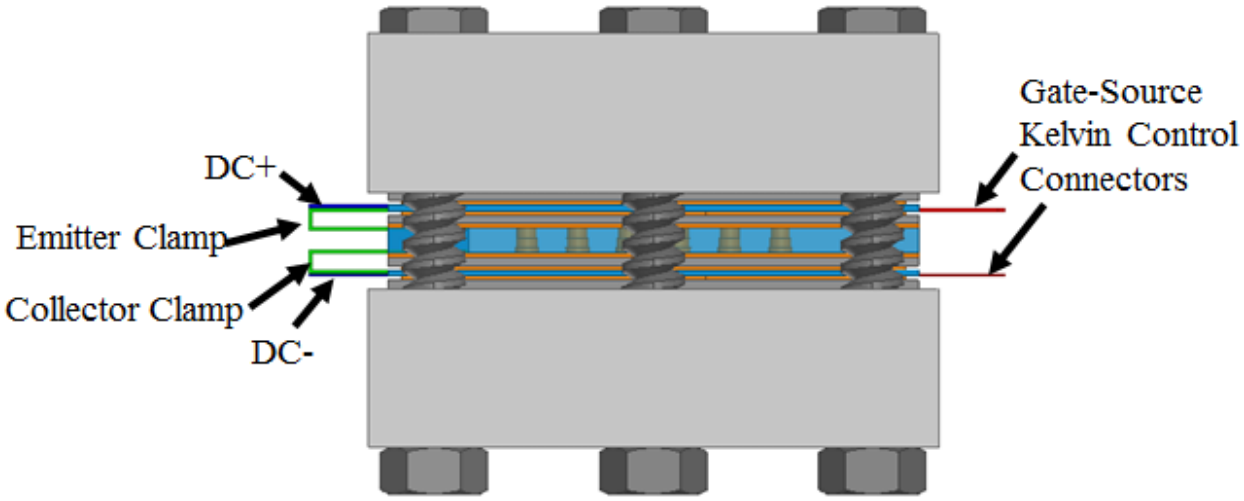

Fig. 2.2. 3-D rendition of the proposed 3-D power module stack

Fig. 2.1 and Fig. 2.2 represent the exploded view and 3-D rendition of the proposed power module structure respectively. As shown in Fig. 2.2 , modules 1 and 2 are stand-alone power modules in the 3-D stack. The stand-alone power modules each consist of a switching position having two Si-IGBT devices from ABB (Part no. 5SMX12E1280) in parallel with two SiC Schottky barrier diodes from Wolfspeed (Part no. CPW4-1200-S020B) in an anti-parallel configuration. As such, modules 1 and 2 form the high side and the low side switching positions for a half-bridge topology. The paralleling of the power devices is performed inside each stand-alone module to increase the current handling capability. The two power modules are series-connected using a novel interconnection scheme to achieve the half-bridge power module configuration [2]. A two-step interconnection scheme is followed to interconnect the power module. At first, clamped interconnections are used to route the emitter and collector of the power modules to the outside copper metallization of the direct bond copper (DBC) substrate. Subsequently, a spring-loaded LTCC interposer is used to make the interconnection between the

collector and the emitter of the two power modules to connect them in series to form a half-bridge power module [2].

Fig. 2.3 represents the 3-D rendition and the side view of the interconnection scheme used to achieve series connection between the bottom (module 1) and top (module 2) modules. In the proposed interconnection scheme, two conductive clamps, namely emitter, and collector clamps are used to route the electrical connection from the inner copper layer of top DBC of module 1 to the bottom DBC of module 2 [2]. The entire loop from DC+ to DC- starts from the collector (Green) of the top module (module 2). The emitter clamp (Blue) of module 2 routes the emitter of the devices placed in the top module (module 2) to the outer layer of the bottom DBC of module 2 [2]. The collector of the bottom module (module 1) is also routed to the outer copper layer of the top DBC of module 1 using a similar collector clamp (Green) [2]. The electrical connection between the emitter of module 2 and collector of module 1 is achieved by a low temperature co-fired ceramic (LTCC) interposer embedded with spring loaded mechanical contacts [2]. The conductive clamps used to route the electrical connections are machined out of thin copper sheets. Mill-max spring loaded pins (Part No. 0965-0-15-20-80-14-11-0) are used as mechanical contacts for the proposed interconnection [1]. As such, a series connection is achieved between modules 1 and 2 to realize a wire bondless half-bridge 3-D stacked power module.

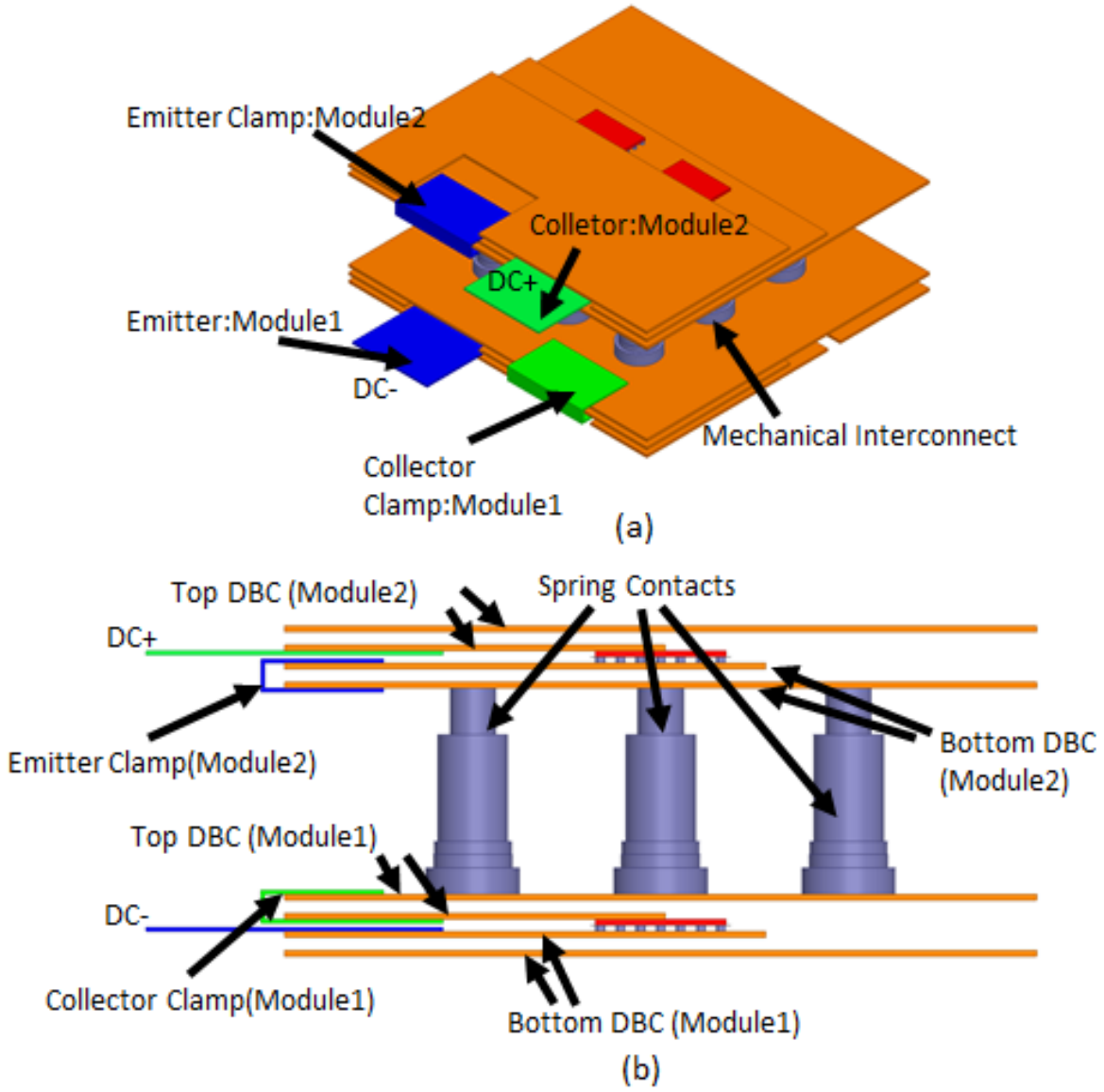

Fig. 2.3. (a) 3-D rendition of the interconnection scheme for the 3-D power module stack [2], (b) side view of the interconnection scheme (only conducting objects are shown in figure for simplicity)

For optimum parasitic design, electrical routing for the current conduction paths plays a vital role. For the wire bondless power module, the electrical routing of the gate, emitter, and collector are achieved using through hole conductive vias on LTCC substrate. The electrical routing for the current conduction paths is designed in such a way that the forward and the return current

paths are overlapped on top on each other and in opposite direction. The overlapping antiparallel current paths reduce the magnetic fields generated through current conduction by magnetic field cancellation [2]-[4]. As such, reducing the overall parasitic inductance of the current conduction loops to achieve optimum parasitic inductance. Fig. 2.4 represents the anti-parallel current path configuration for the 3-D power module stack. The total inductance

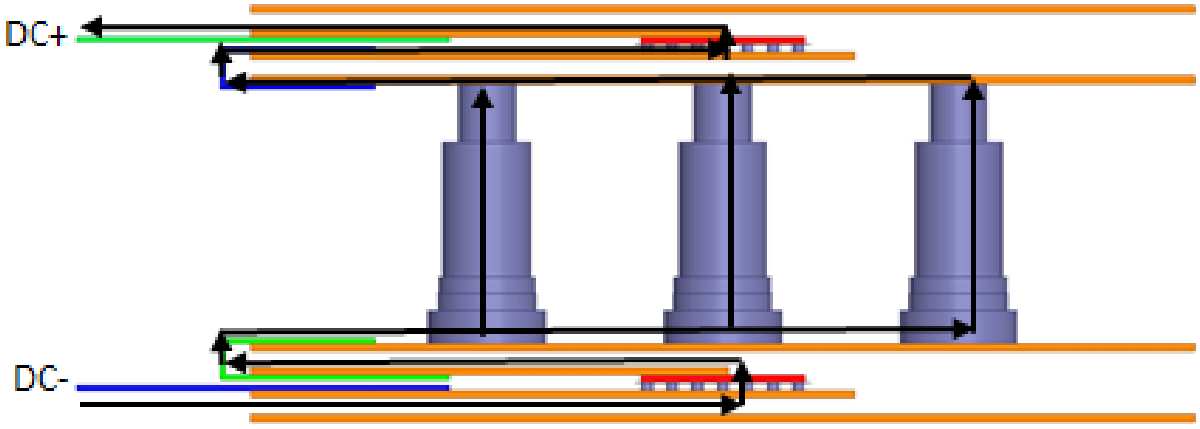

Fig. 2.4. Antiparallel current path configuration for the proposed 3-D power module stack [2]

of the loop consisting of an overlapping antiparallel current path depends on the self-inductance of each conductor and the mutual inductance between the conductors.

Fig. 2.5. Current conduction loop of an overlapping current path separated by a dielectric

Fig. 2.5 represents a current loop consisting of an overlapping current path separated by a dielectric layer of thickness, d. The total loop inductance can be given by the following:

$$L_{total} = L_1 + L_2 - 2M_{12} \qquad (2.1)$$

where, L_1 = self-inductance of top conductor, L_2 = self-inductance of bottom conductor, M_{12} = the mutual inductance between the top and bottom conductor. Fig. 2.6 shows that as the dielectric separation between the top and the bottom conductors increases the mutual inductance decreases between the conductors, as such, the overall loop inductance increases.

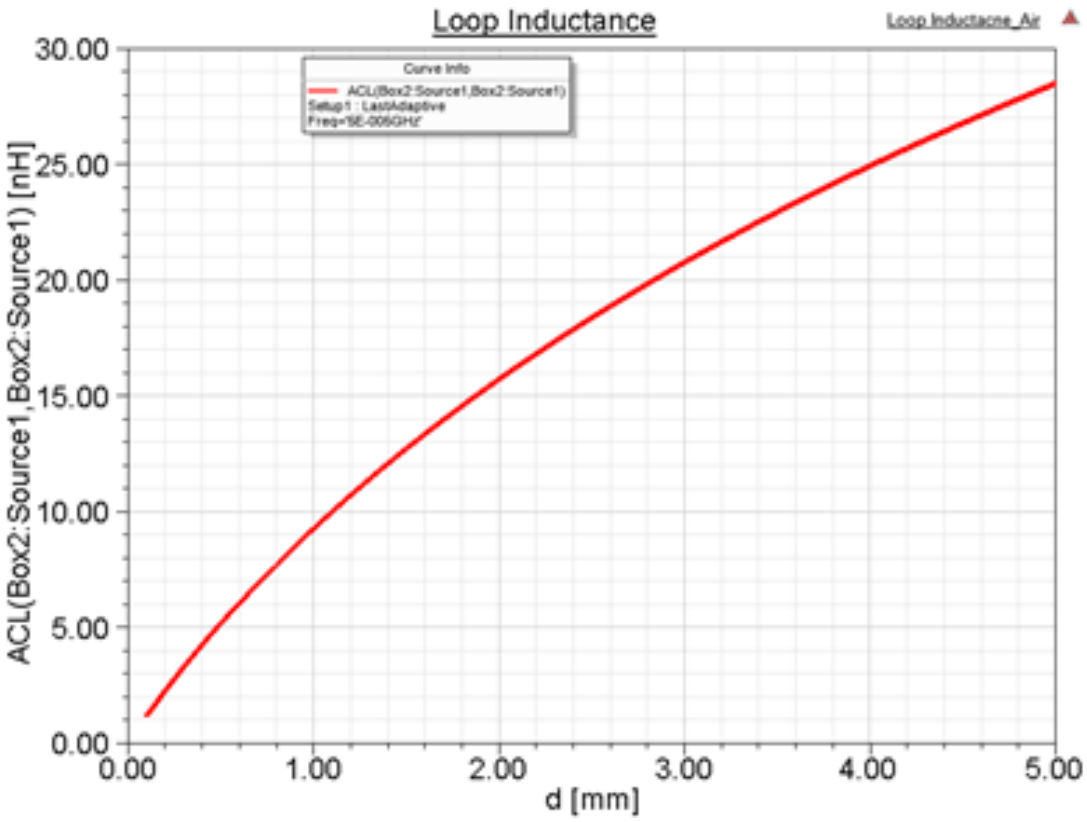

Fig. 2.6. Loop inductance vs. dielectric separation

In traditional wire bonded power modules, the current conduction paths are generally coplanar having all the current conduction loops in a single layer. On the contrary, 3-D power modules

can utilize multilayer current conduction paths. As such, the forward and return current paths can be routed leveraging the multilayer design freedom offered by multilayer laminate substrates to design an antiparallel current path configuration to reduce parasitic inductance by mutual coupling. This theoretically cancels out the effect of opposing current.

Fig. 2.7 and Fig. 2.8 represent the direction of current flow of an overlapping forward and the return path and a single layer current path respectively. In Fig. 2.7, the dimensions of the forward and return current path are assumed to be 20 mm × 10 mm and 26 mm ×10 mm respectively. The single layer current path is assumed to be 20 mm ×10 mm. The parasitic extraction simulation performed in ANSYS Q3D yields 1.9 nH and 5.9 nH for the overlapping and the single layer current paths respectively. As such, an antiparallel forward and current path configuration is implemented to design the proposed wire bondless 3-D half-bridge power module stack.

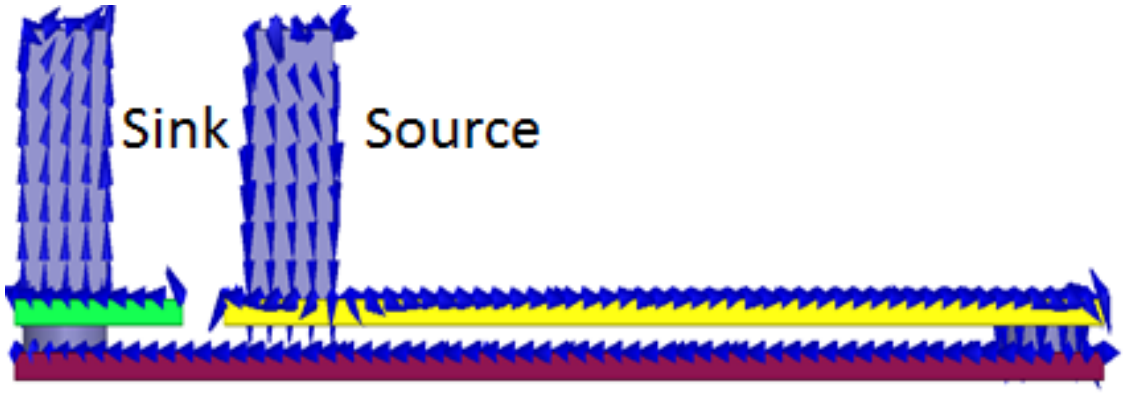

Fig. 2.7. Overlapping forward and return current path [3]

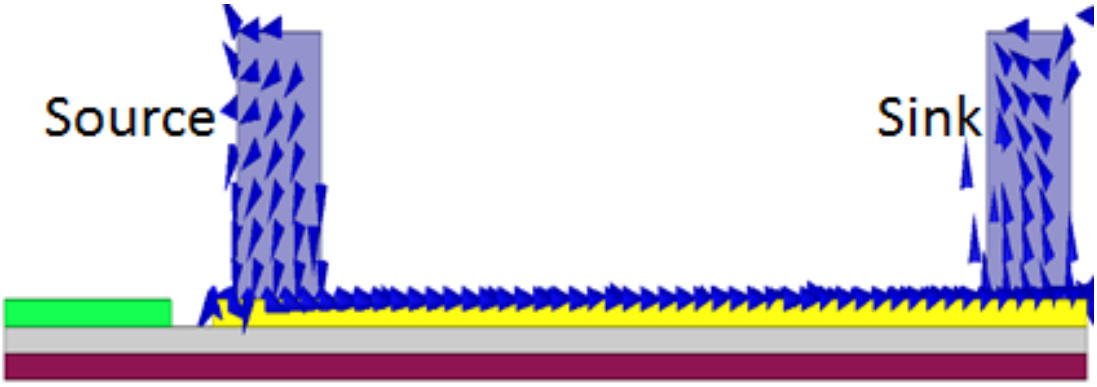

Fig. 2.8. Single layer current path [3]

In the subsequent sections, the design process for the stand-alone wire bondless power modules along with the other components necessary to build the 3-D stack will be discussed in detail.

2.1 Design of Wire Bondless Power Module

The design and fabrication of wire bondless power module is an integral part of the proposed 3-D power module stack. In this section, the detailed design approach for the wire bondless power module will be discussed.

Fig. 2.9 (a) and (b) show the graphical representation of the stand-alone wire bondless power modules and the exploded view of the power module respectively. The dimension of the wire bondless power module for the proposed 3-D stack is 42.5 mm×40.1 mm. As can be seen, the power module consists of top and bottom direct bond copper substrates. The LTCC interposer in between the top and bottom direct bond copper substrates acts as a semiconductor device carrier. The electrical routings for the semiconductor devices are achieved by through hole vias and screen printed metallization patterns on a low temperature co-fired ceramic (LTCC) substrate. The LTCC interposer with the devices is solder attached to the top and bottom DBCs to route the gate, emitter and collector region. The input/output and the Kelvin connections terminals are achieved by copper connectors machined out of thin copper sheets.

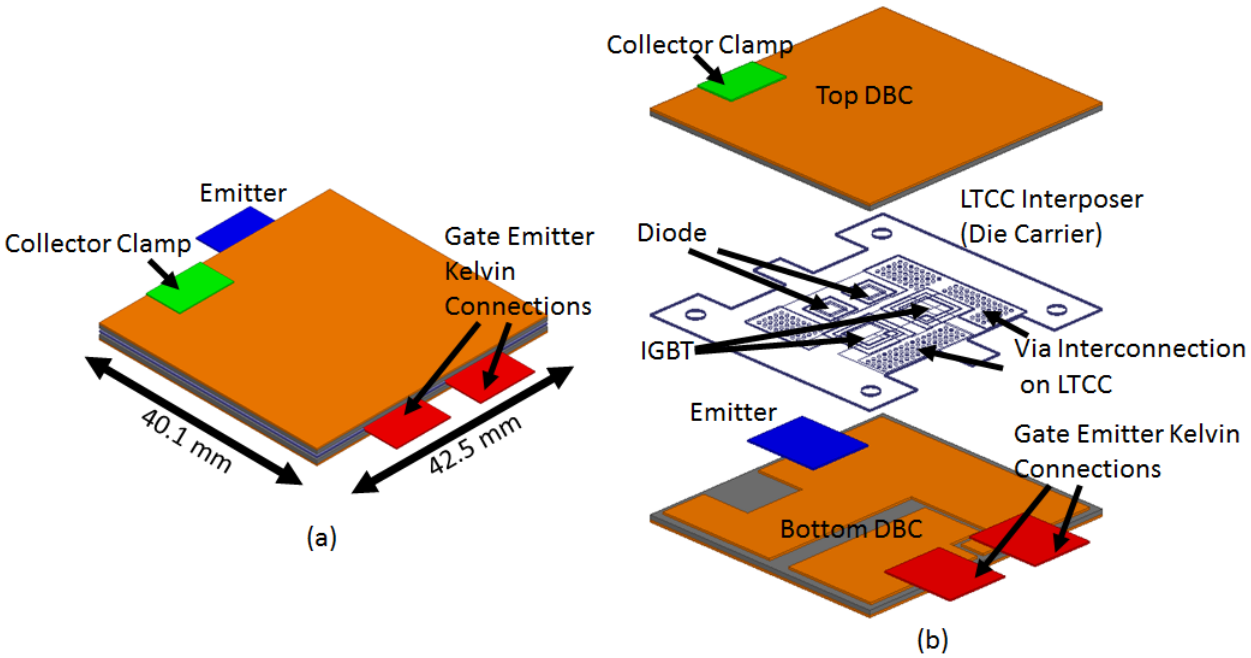

Fig. 2.9. (a) 3-D rendition of the wire bondless power module, (b) exploded view of the wire bondless power module

2.2 LTCC Die Carrier Interposer Design

LTCC interposer in between the top and bottom DBCs is designed as a multilayer substrate. As mentioned earlier, the LTCC interposer in the proposed wire bondless power module acts as the semiconductor device carrier and also provides electrical isolation between the emitter, collector of Si-IGBTs and anode, cathode of SiC Schottky barrier diodes.

DuPonts™ GreenTape™ 951 is used to prepare the die carrier substrate. The x, y, z shrinkages need to be considered in the design phase of the substrate to accommodate any shrinkage after firing. The manufacturer provided x, y shrinkages are 12.7% and z shrinkage is 15% [4]. In total, there are four layers in the designed LTCC interposer as shown in Fig. 2.10. The first layer as shown in Fig. 2.10 (a) holds the cut-outs for the Si-IGBT and SiC diodes. Layer 2, as shown in Fig. 2.10 (b), holds the metallization for attaching the Si-IGBT devices. Also, layer 2 acts as a

cavity extender to increase the cavity depth to match the thickness of the SiC diode. The interconnections between the multilayer LTCC are achieved by through hole vias. Layer 3, as shown in Fig. 2.10 (c), is used as the diode attachment layer. Fig. 2.10 (d), represents the back-side metallization for direct solder attachment of LTCC substrate to the bottom DBC substrate. Fig. 2.11 shows the exploded view of the multilayer LTCC interposer. Fig. 2.12 shows the dimension of each layer of the LTCC die carrier in mm.

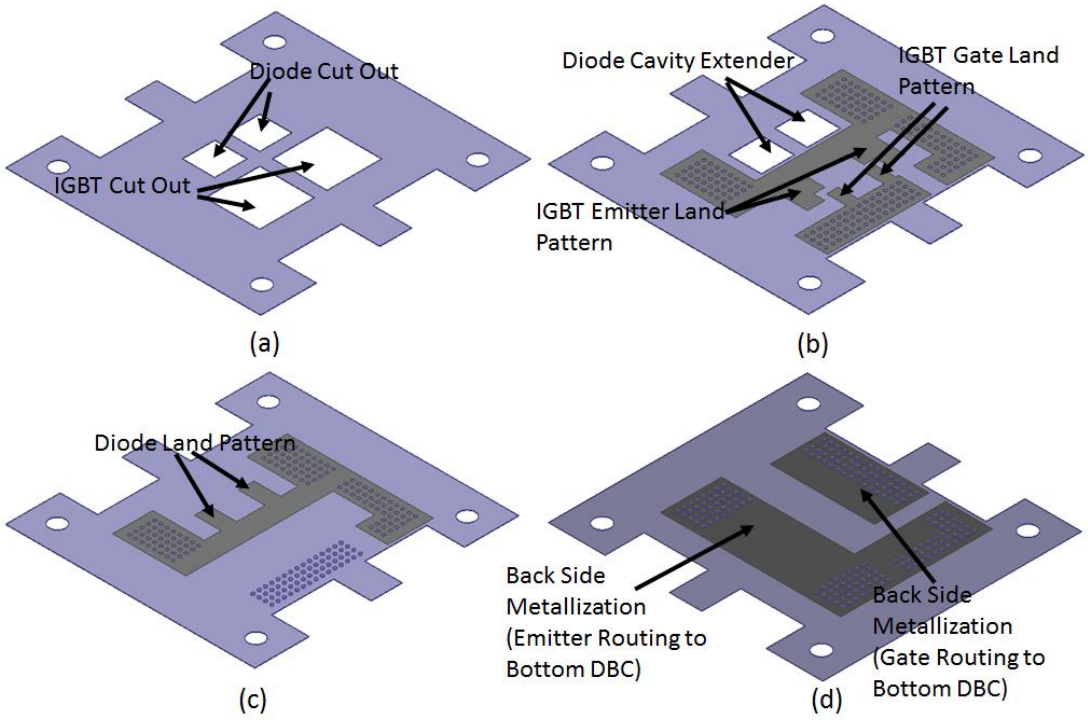

Fig. 2.10. (a) Layer 1, device cutout (b) layer 2, metallization for attaching Si-IGBTs (c) layer 3, metallization for SiC diode attachment (d) layer 4, back side metallization for direct solder attachment to bottom DBC

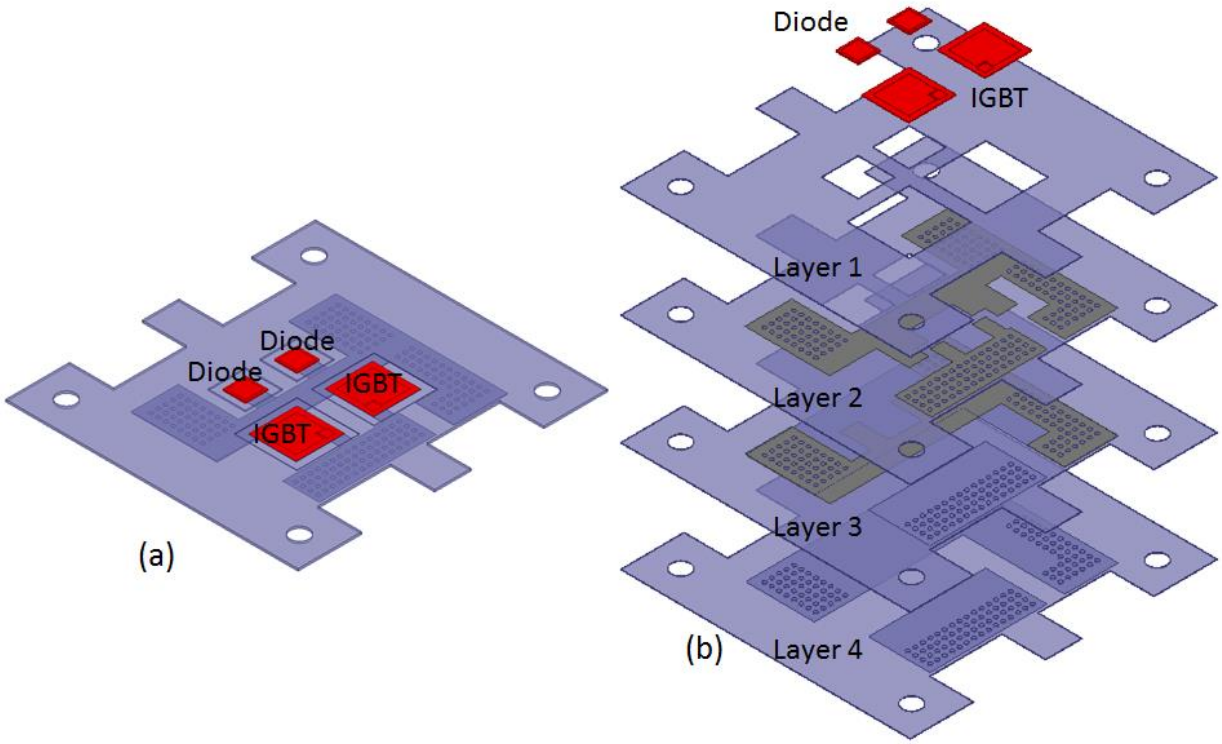

Fig. 2.11. (a) LTCC die carrier interposer with device placement shown (b) exploded view of the multilayer LTCC interposer

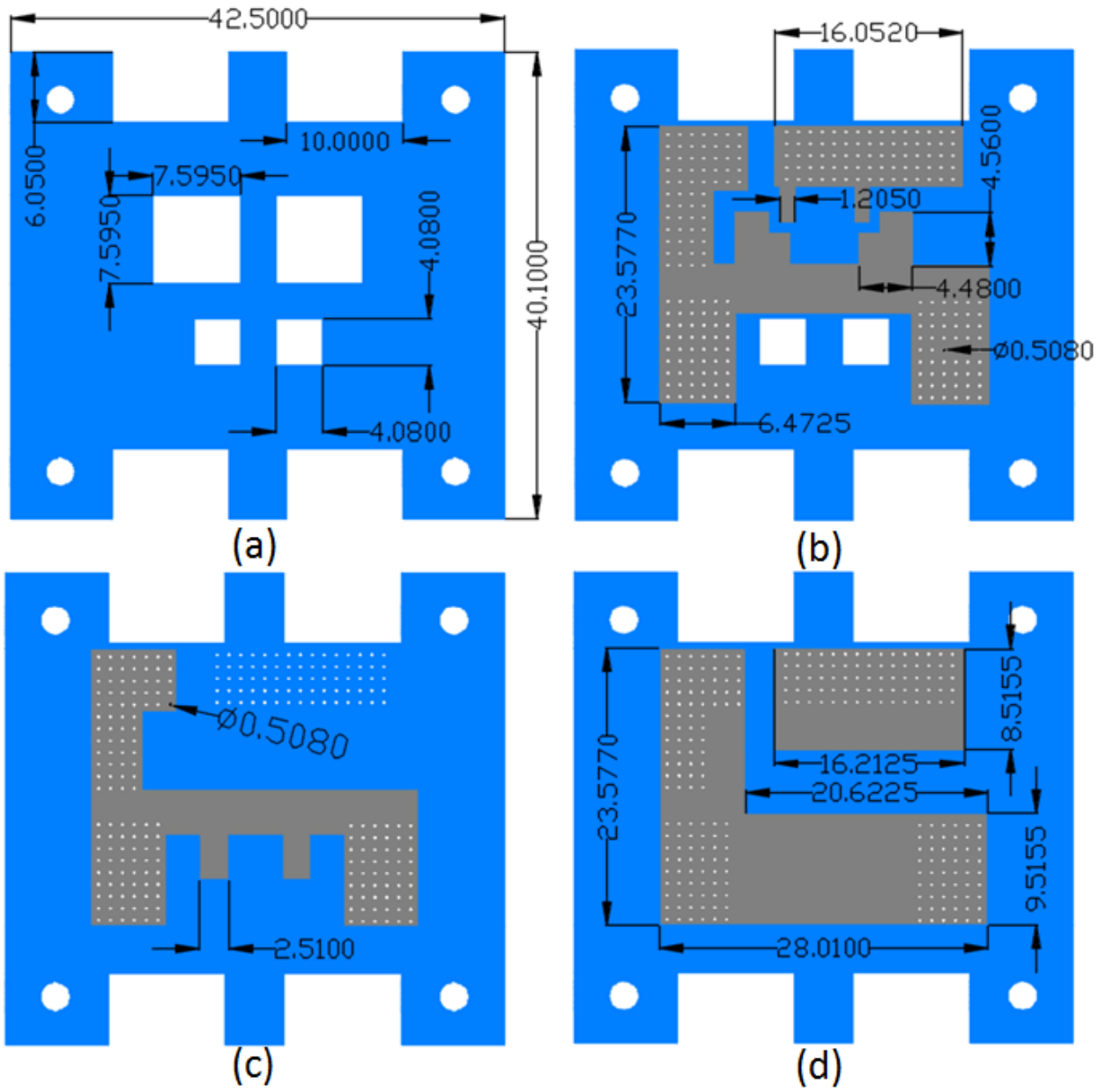

Fig. 2.12. Dimensions in mm for LTCC interposer (a) layer 1 (b) layer 2 (c) layer 3 (d) layer 4

The inconsistent device thickness for the Si-IGBT and SiC Schottky diode pose a significant challenge to design and fabricate the cavities on the LTCC interposer with different thicknesses. The thicknesses of the Si-IGBT and the SiC diode are 140 µm and 377 µm, respectively. In order

to facilitate direct solder attachment for the collector of the IGBT and cathode of the diode with the

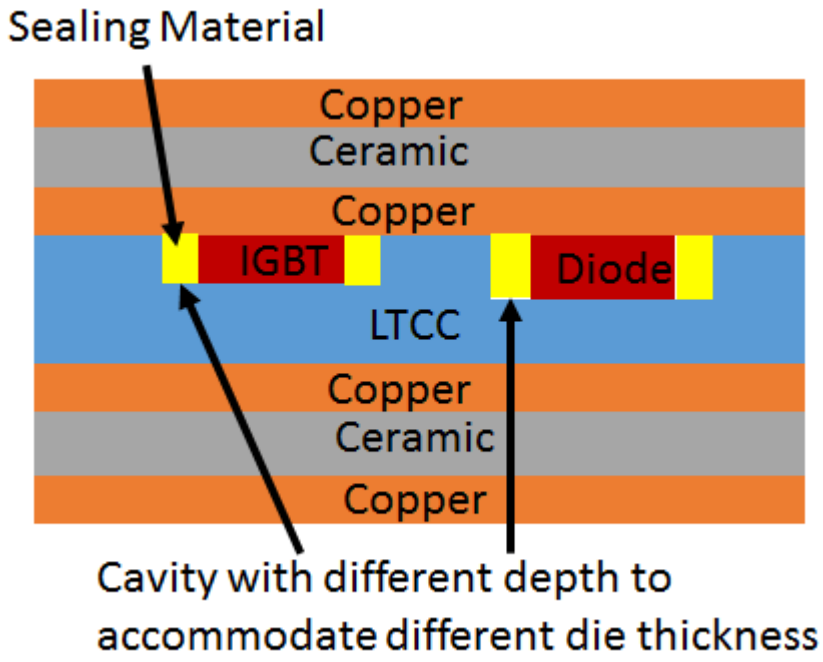

Fig. 2.13. Illustration of LTCC interposer with different cavity depths

top DBC substrate, the semiconductor devices must be on the same level and flashed with the top surface of the LTCC interposer. Fig. 2.13 shows the graphical representation of the side view of the LTCC interposer with different cavity depths for Si-IGBT and SiC diode that are sandwiched between the top and bottom DBCs. In order to accommodate the different die thickness, different combinations of 4.5 mils, 6 mils and 10 mils LTCC 951 GreenTape™ is used to achieve the desired cavity depths. The z-direction shrinkage of the LTCC 951 GreenTape™ is about 15% after firing [4]. As such, the shrinkage of the tapes is considered during the design process of the interposer.

In order to fabricate the multilayer LTCC interposer, each layer is first prepared separately. Subsequently, the layers are laminated together to form the multilayer interposer. The fabrication of the LTCC interposer will be discussed in details in Chapter 5.

2.3 Top and Bottom DBC Design

The top and the bottom direct bond copper substrates are directly soldered attached to the LTCC device carrier. The gate and, emitter of the Si-IGBT devices are routed to the bottom DBC and the collector is attached to the top DBC. The top and bottom DBC conductors are designed using 12 mils Cu/ 25 mils Al_2O_3/ 12 mils Cu substrate. In addition to electrical routing, DBC substrates act as good thermal spreader for the proposed design, as such providing cooling mechanism from both sides of the devices.

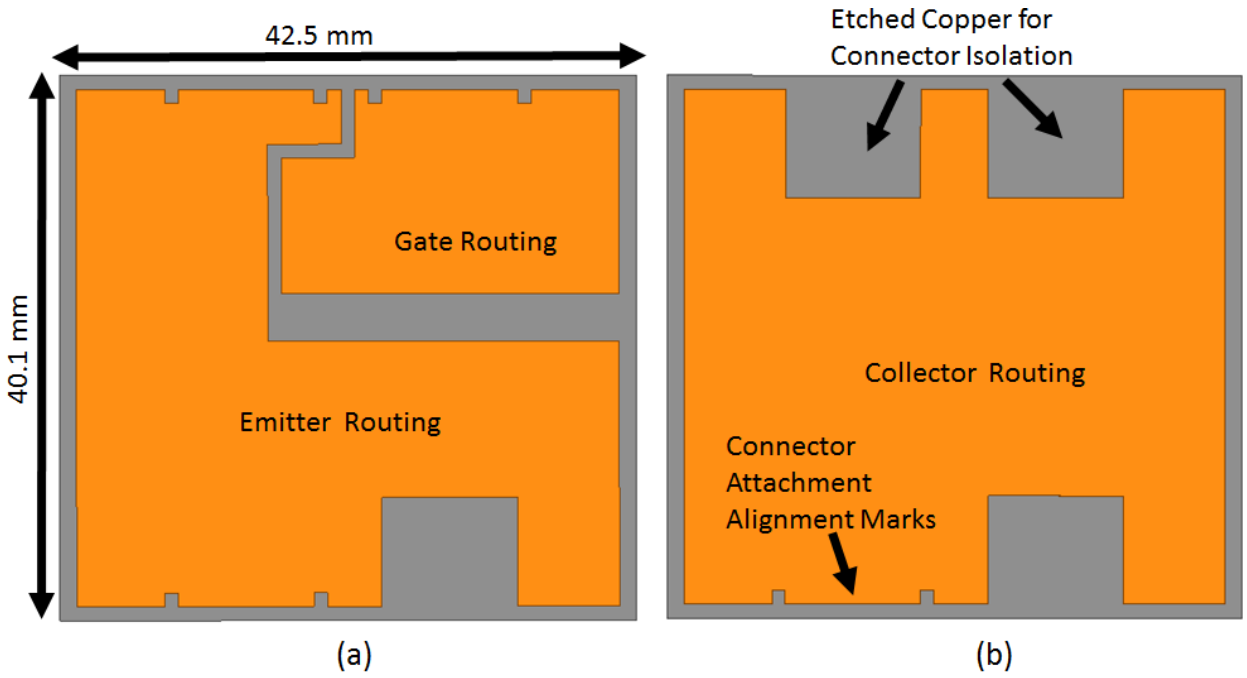

Fig. 2.14. (a) Layout of bottom DBC (b) layout of top DBC

Fig. 2.14 (a) and (b) show the layouts of the bottom and top DBC substrates respectively. As can be seen, the bottom DBC layout contains the gate and emitter routing pads. The gate, emitter, and the collector connectors are solder attached to the DBC. The connector alignment marks are etched during the fabrication process and taken into consideration while designing the DBC substrates to facilitate connector attachment later in the fabrication process flow. Also, the copper is etched from the top DBC where the gate and emitter connectors are attached on the bottom DBC. Similarly, copper is etched from the bottom DBC where the collector connector is attached on the top DBC. As such providing electrical isolation to avoid any shorting between the top and bottom DBC substrates.

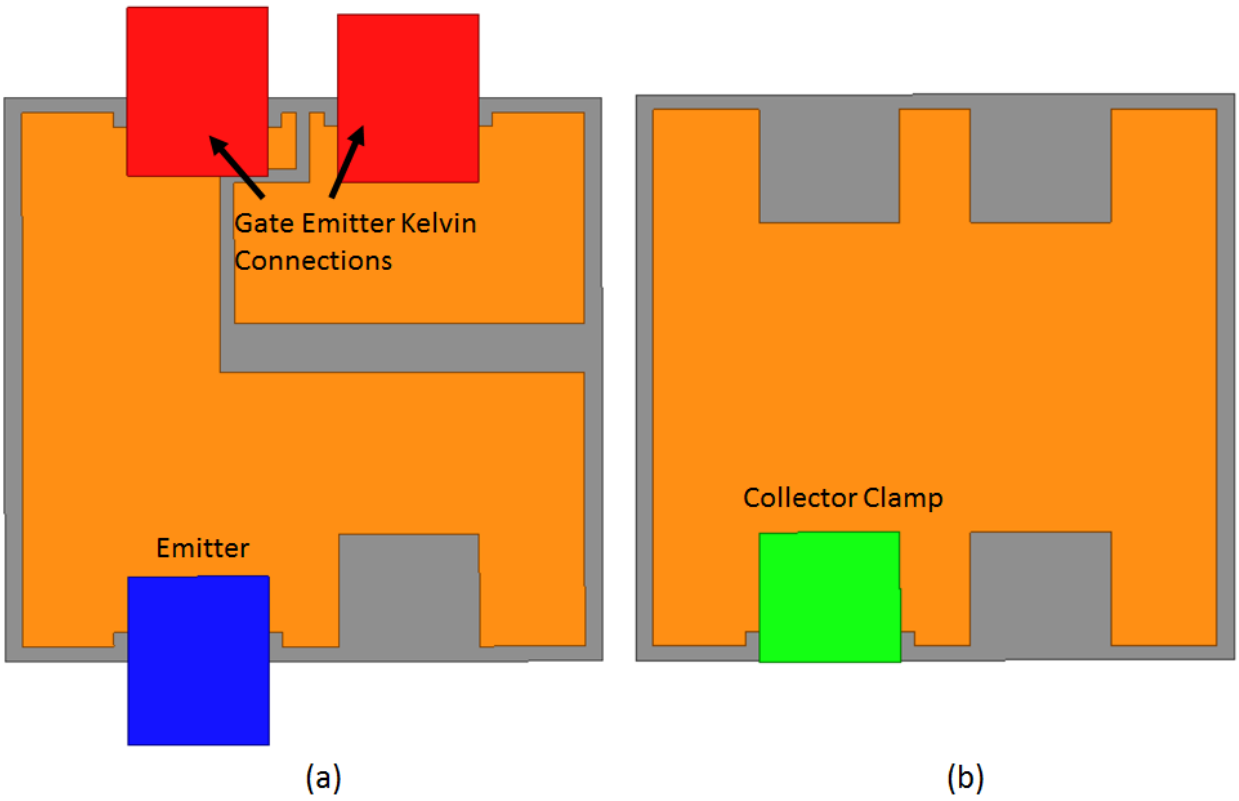

Fig. 2.15. (a) Bottom (b) top DBC substrate with gate, emitter, collector and Kelvin connectors

2.4 Spring Loaded LTCC Interposer Design

In the proposed power module, a spring loaded LTCC interposer is used to establish interconnections between the top and bottom stand-alone power modules to form the 3-D half-bridge stacked power module. The spring loaded LTCC interposer provides a better mechanical compliance to the 3-D stacked power module structure. The LTCC fixture that holds the spring-loaded pins is designed using AutoCAD. Fig. 2.16 shows the design of the LTCC fixture in AutoCAD.

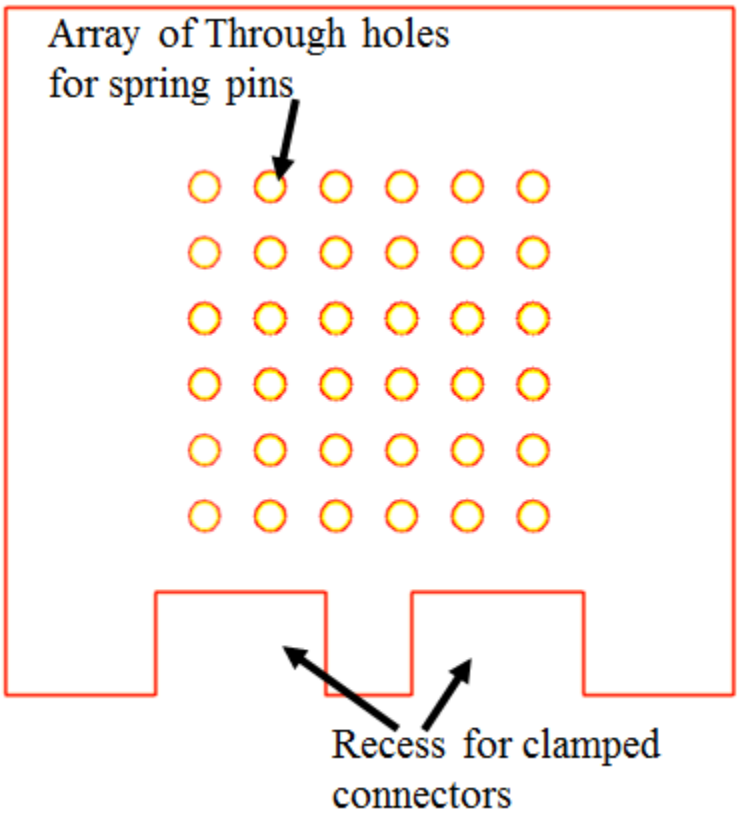

Fig. 2.16. LTCC fixture designed in AutoCAD

The LTCC interposer is fabricated by populating an LTCC fixture with spring-loaded pins. The spring-loaded pins used to fabricate the interposer are manufactured by Mill-Max (Part No. 0965-0-15-20-80-14-11-0) [1]. Each spring-loaded contact is gold plated with a plating thickness of 0.508 µm and carries 3 A of continuous current [1]. An array of 36 paralleled spring loaded contacts are used to fabricate the interposer to ensure a higher current handling capability of the interposer. The spring-loaded contacts are rated to endure 1,000,000 cycles [1]. The total height of each spring-loaded pins is 2.54 mm with a maximum stroke of 0.61 mm [1]. The total thickness of the LTCC interposer is designed to be 1.93 mm to ensure the utilization of the maximum stroke of the spring-loaded pins to fabricate the module-level 3-D structure. The spacing between the spring-loaded pins is designed to be 3.83 mm. The hole diameter on the LTCC fixture is designed to be slightly bigger than the diameter of the spring-loaded pins to easily populate the fixture with the spring pins. Fig. 2.17 represents the side view of the LTCC interposer showing all the critical dimensions.

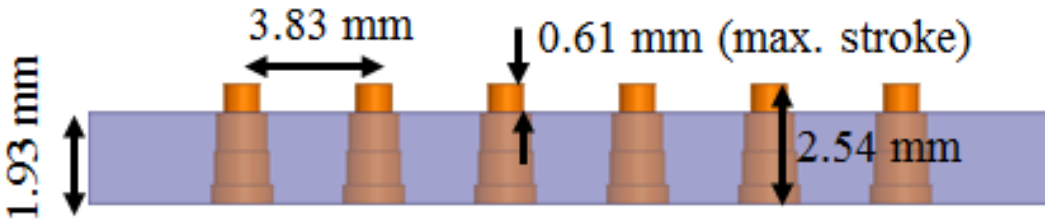

Fig. 2.17. Side view of the LTCC interposer with critical dimensions (mm)

2.5 Chapter Summary

In this chapter, the detailed design of the module-level 3-D wire bondless half-bridge stacked power module is presented. The design aspect of each individual components of the stack is

addressed. The detailed layouts of the stand-alone power modules are presented. The novel interconnection technique used to electrically interconnect the two stand-alone power modules to realize a half-bridge power module is discussed in detail. The anti-parallel forward and return current path technique to reduce inductance by magnetic field cancellation is discussed.

2.6 References

[1] "Mill-Max: 0965-Spring-Loaded Pin". *Mill-max.com*. N.p., 2017. Web. 6 May 2017.

[2] A. Dutta and S. S. Ang, "A 3-D stacked wire bondless silicon carbide power module," *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Fayetteville, AR, 2016, pp. 11-16.

[3] Dutta and S. S. Ang, "Electromagnetic interference simulations of power electronic modules," in *Integrated Power Packaging (IWIPP), 2015 IEEE International Workshop on*, 2015, pp. 83-86.

[4] E. Hoene, A. Ostmann and C. Marczok, "Packaging very fast switching semiconductors," in *Integrated Power Systems (CIPS), 2014 8th International Conference on*, 2014, pp. 1-7.

[5] Low temperature co-fired ceramic system, DuPont™ GreenTape™, DuPont™, November 2009

Chapter 3 Simulations of the Wire Bondless 3-D Half-Bridge Stack Power Module

In this chapter simulation studies of the 3-D wire bondless half-bridge stack are performed. Electrical and thermal simulations are performed to investigate the feasibility of the 3-D wire bondless power module structure. Stray parasitic inductance induced by the packaging has a significant impact on the switching behavior of the power devices [1]-[8]. In order to achieve fast, efficient switching performance of the power modules, it is necessary to minimize the parasitic inductance in the power module. In general, DC bus inductance, common source inductance, and gate-source loop inductance are of primary importance and needs to be optimized for optimum switching performance. Depending on the placement of the supply terminals, input/output terminals, Kelvin connection pins, the stray inductance associated with each device can be different within a power module [9]. The imbalance in stray inductance is more prominent in power modules where paralleling and a series connection of several power devices/modules are necessary in order to achieve high current and voltage handling capability, respectively.

In the proposed 3-D half-bridge power module stack, careful design considerations are given to optimize the parasitic inductances of the power module. The parasitic extraction of the 3-D half-bridge stack is performed using ANSYS Q3D parasitic extraction tool. ANSYS Q3D implements quasi-static 3-D electromagnetic field solver based on methods of moments (MoM) and finite element method (FEM) to extract the resistance, inductance, capacitance and the conductance parameters for 3-D and 2-D geometries, respectively [10]. In order to extract parasitic parameters between two terminals on the layout, the current conducting path is defined by assigning source and sink excitations on the terminals. ANSYS Q3D implements an adaptive meshing to refine the mesh. A frequency sweep is performed to extract the parasitic parameters at various

frequencies. In this chapter, frequency dependent parasitic inductance and resistance associated with the various current conducting nets of the 3-D stack will be extracted and subsequently, measurement results for the parasitic inductance will be discussed to validate the simulated parasitic results.

3.1 Equivalent Parasitic Model for 3-D Half-Bridge Stack

An equivalent parasitic inductance map of the proposed 3-D half-bridge power module is shown in Fig. 3.1, where the inductance associated with collector/emitter/gate and anode/cathode of the Si-IGBT and SiC Schottky diodes are shown. In Fig. 3.1, L_{HC1}/L_{HC2} and L_{HDC1}/L_{HDC2} are inductances for the current path starting from the DC+ terminal to the collector of the two paralleled high side Si-IGBTs and cathode of the two anti-paralleled high-side SiC Schottky diodes, respectively. L_{HE1}/L_{HE2} and L_{HDA1}/L_{HDA2} are inductance associated with the current path from the emitter of the high-side paralleled Si-IGBTs and anode of the anti-paralleled SiC diodes to the load terminal. Similarly, L_{LC1}/L_{LC2} and L_{LDC1}/L_{LDC2} are inductances associated with the current path from load terminal to the collector and cathode of the low side paralleled Si-IGBTs and anti-paralleled SiC diodes, respectively. L_{LE1}/L_{LE2} and L_{LDA1}/L_{LDA2} are inductances associated with the current path starting from the emitter and anode of the low side Si-IGBTs and SiC diodes to the DC- terminal. Also, L_{HG1}/L_{HG2} and L_{LG1}/L_{LG2} are gate inductances associated with the high-side and low-side paralleled Si-IGBTs respectively. A frequency dependent parasitic extraction is performed within a frequency range of 1 kHz to 100 MHz for each of the inductance parameters shown in Fig. 3.1.

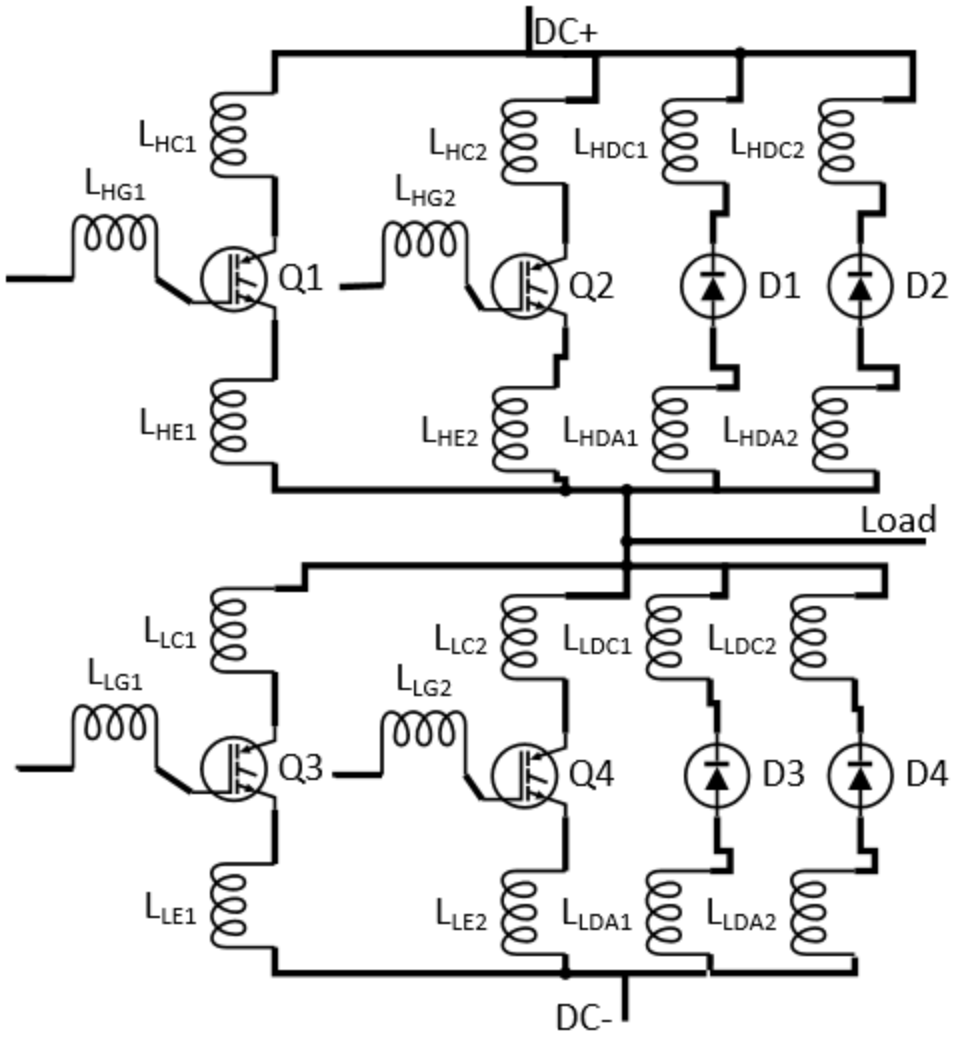

Fig. 3.1. Equivalent inductance map of the proposed 3-D half-bridge stack power module

3.2 DC+ Inductance of 3-D Stack

Fig. 3.2 corresponds to the DC+ inductance associated with the proposed 3-D stack half-bridge module. The DC+ net includes the path starting from the DC+ terminal to the collector of the IGBTs and cathode of the anti-parallel diodes for the high-side switching position. These inductances are defined as L_{HC1}, L_{HC2}, L_{HDC1} and L_{HDC2} in Fig. 3.1. In order to extract the parasitic inductance and resistance between the DC+ terminal and the collector and cathode of

the high-side IGBTs and diodes, the DC+ terminal is assigned as sink excitation and four source excitations are assigned at very close proximity to the collector of the paralleled IGBTs and cathode of the anti-paralleled diodes on the layout. Fig. 3.3 shows the frequency dependent plots of the parasitic inductance and resistance corresponding to the DC+ net. As can be seen, the parasitic inductance decreases with frequency while the parasitic resistance increases with increasing frequency.

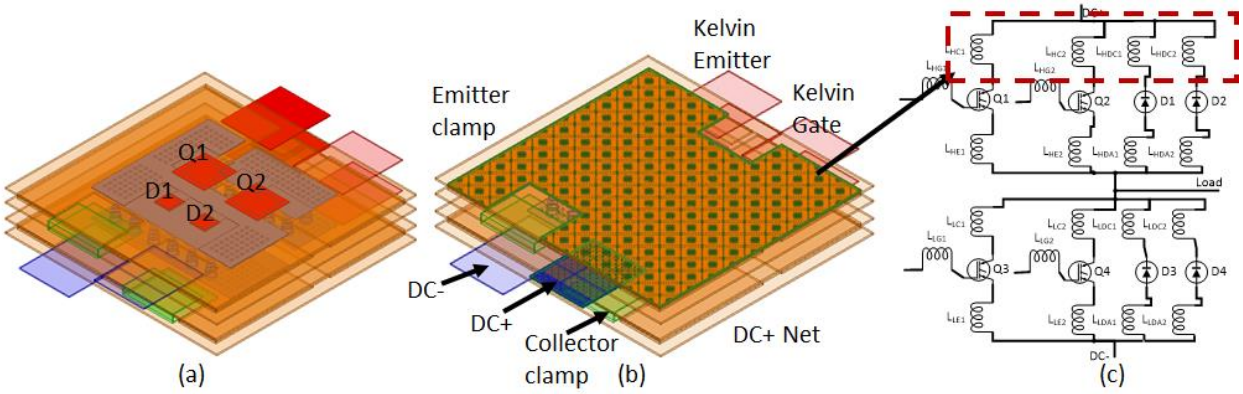

Fig. 3.2. DC+ inductance associated with the 3-D stack power module

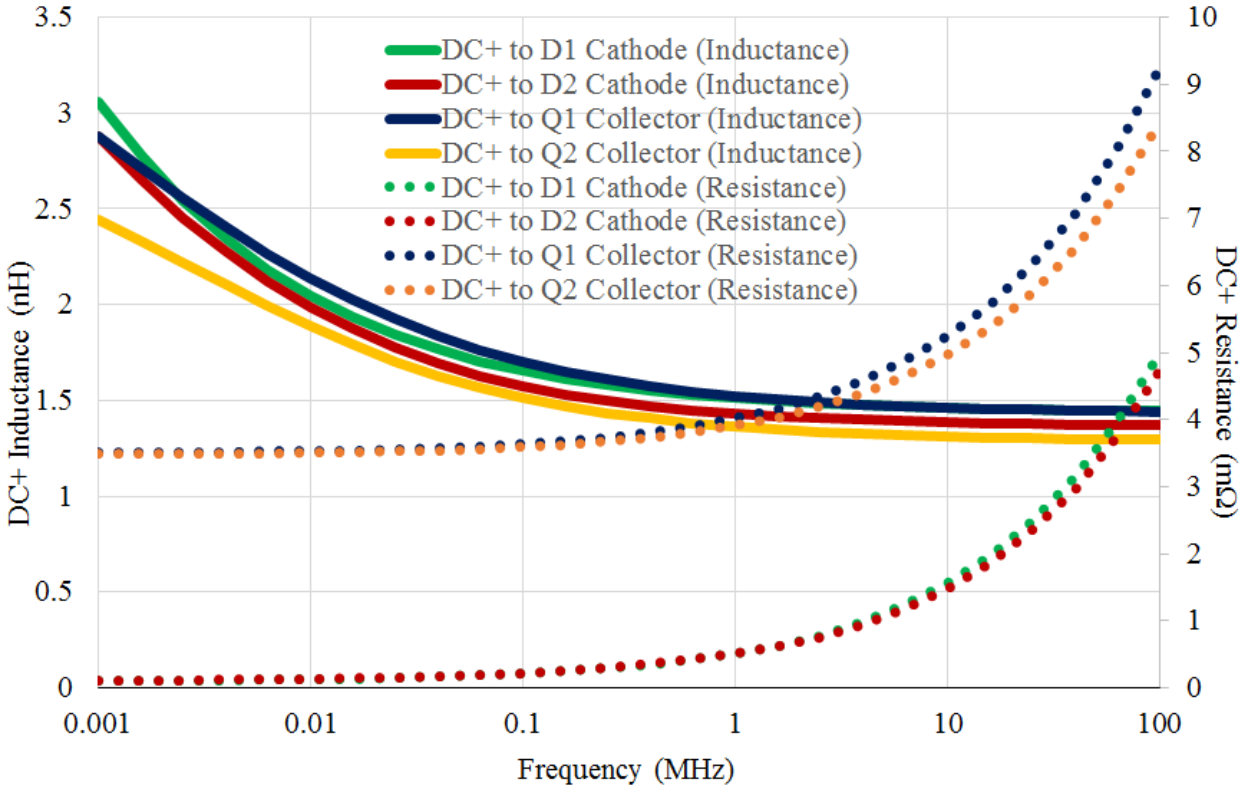

Fig. 3.3. Frequency dependent parasitic inductance and resistance for DC+ net of the 3-D stack power module

3.3 DC- Inductance of 3-D Stack

The DC- net includes the current path starting from DC- terminal to the emitter of the IGBTs and anode of the antiparallel diodes for the low-side switching position. These inductances are

defined as L_{LE1}, L_{LE2}, L_{LDA1}, and L_{LDA2} in Fig. 3.1. Fig. 3.4 shows the current conducting net associated with the DC- net. Fig. 3.5 plots the frequency dependent inductance and resistance corresponding to the DC- net. As can be seen, the parasitic inductance decreases with frequency while the parasitic resistance increases with increasing frequency.

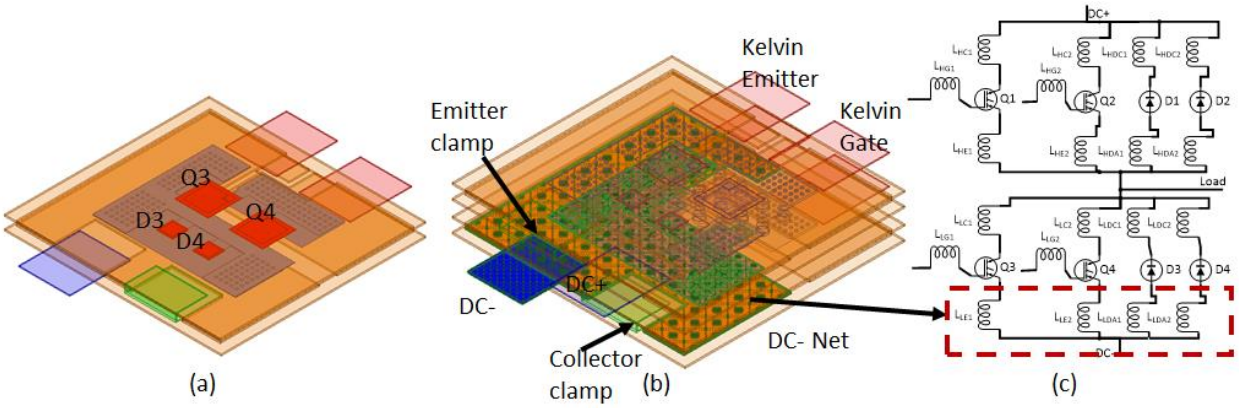

Fig. 3.4. DC- inductance associated with the 3-D stack power module

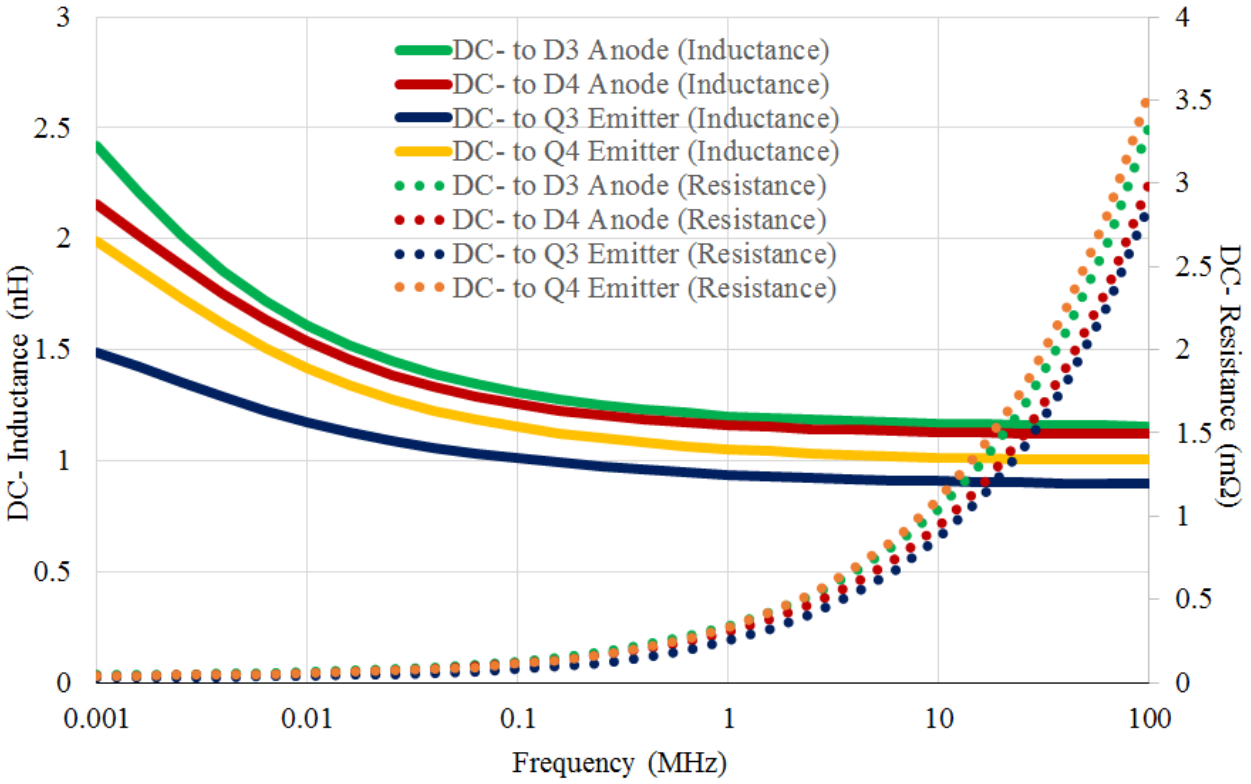

Fig. 3.5. Frequency dependent parasitic inductance and resistance for DC- net of the 3-D stack power module

3.4 Common Source Inductance of 3-D Stack

Two common emitter inductance paths are associated with the half-bridge module. One common emitter inductance path is between the load/output terminal to the high-side devices and the other path is associated with the load/output terminals to the low-side devices. Fig. 3.6 represents the common emitter inductance associated with the 3-D stack. L_{HE1}, L_{HE2}, $L_{HDA1,}$ and L_{HDA2} as defined in Fig. 3.1 are common emitter inductances associated between the load/output terminals to the high-side devices. Additionally, L_{LC1}, L_{LC2}, $L_{LDC1,}$ and L_{LDC2} are common emitter inductances associated between the load/output terminal to the low-side devices as shown in Fig. 3.1. The frequency dependent inductance and resistance plots for the common source net associated with the high and the low side devices are shown separately in Fig. 3.7 and Fig. 3.8,

respectively. As can be seen, both the parasitic inductance for high and low side devices decreases with frequency while the parasitic resistance increases with increasing frequency.

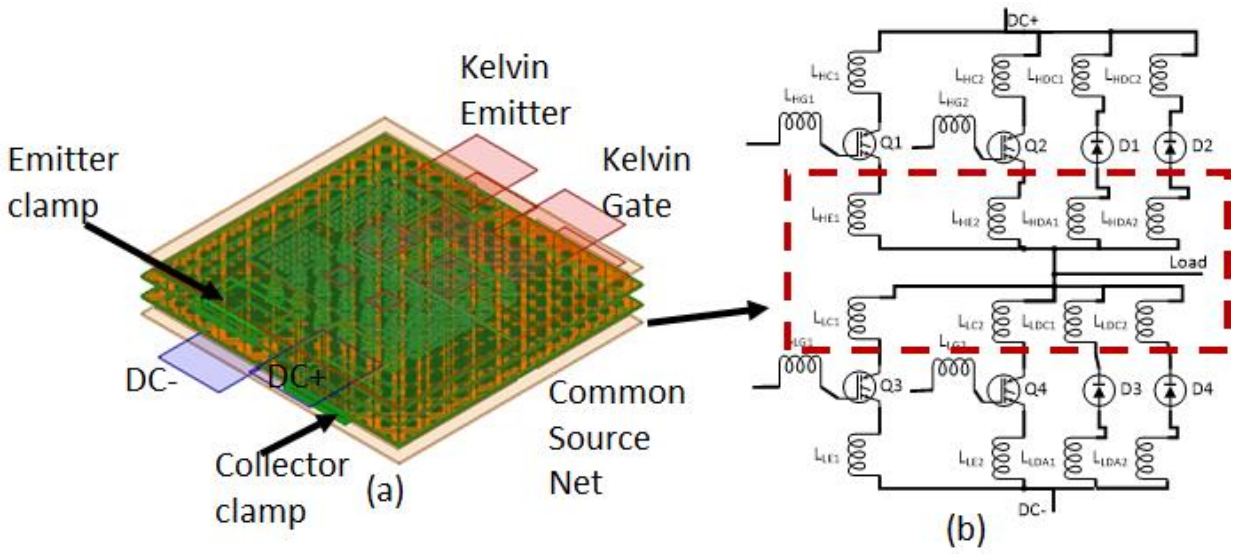

Fig. 3.6. Common source net associated with the 3-D stack power module

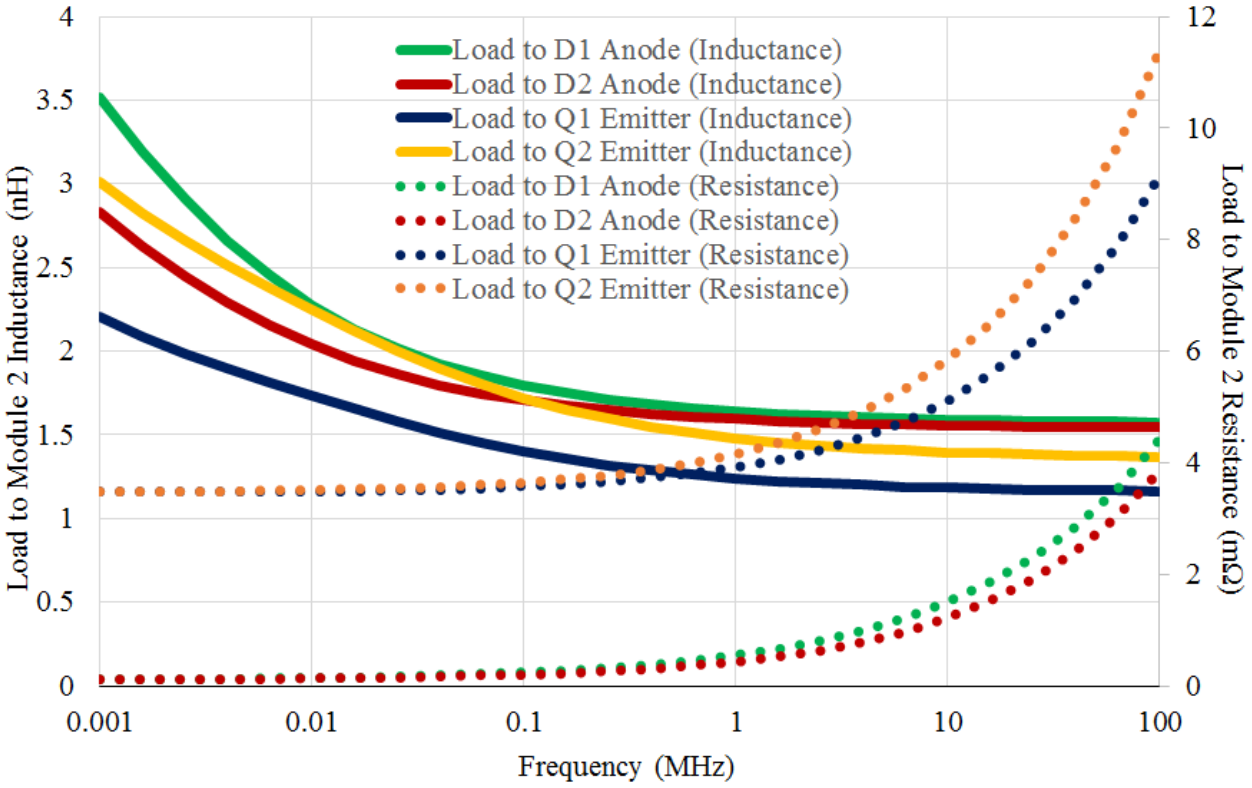

Fig. 3.7. Frequency dependent parasitic inductance and resistance for common emitter net for the high-side devices of the 3-D stack power module

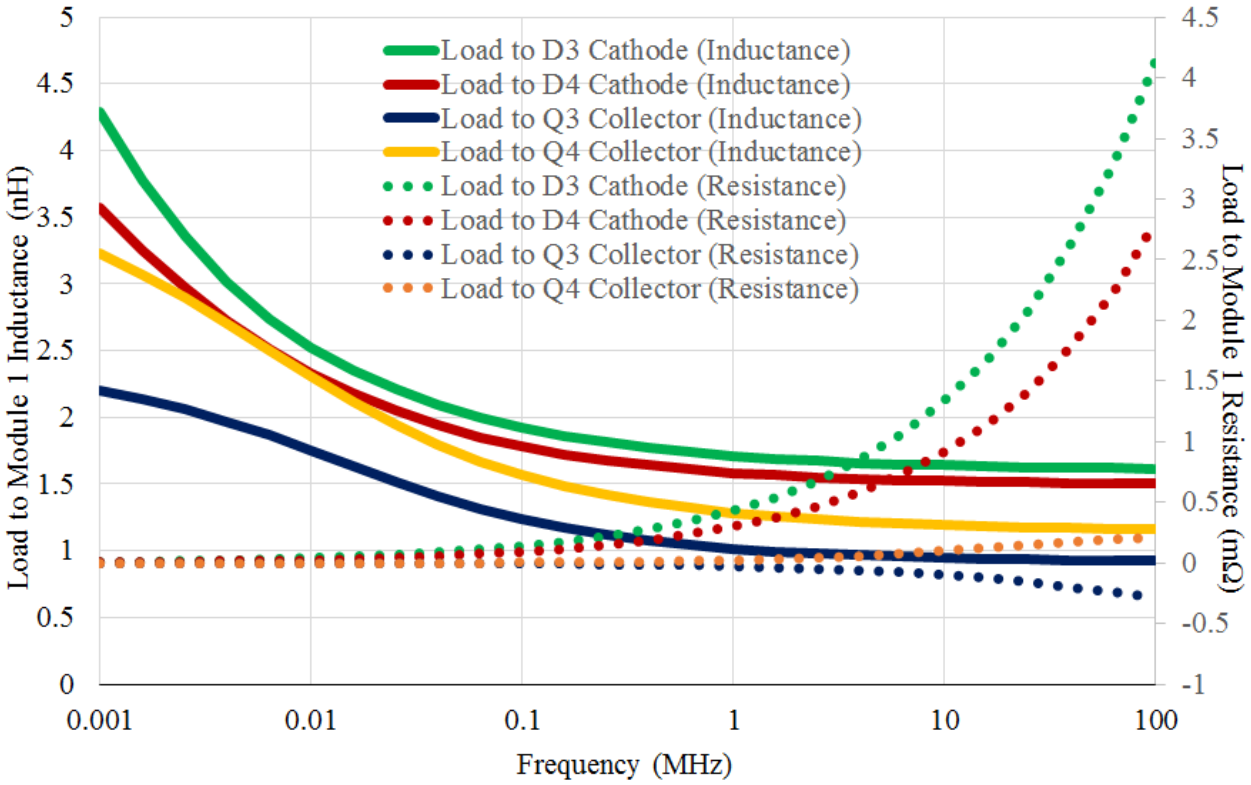

Fig. 3.8. Frequency dependent parasitic inductance and resistance for common source net for the low-side devices of the 3-D stack power module

3.5 Gate Loop Inductance

The gate inductance of the power module is associated with the path starting from the Kelvin gate terminal to the gate of the device. Fig. 3.9 show the gate net associated with the stand-alone power module. As the power modules are identical the gate net associated with the high-side devices, Q1 and Q2, respectively, are shown in Fig. 3.9. Fig. 3.10 plots the frequency dependent inductance and the resistance associated with the gate net of the stand-alone power module.

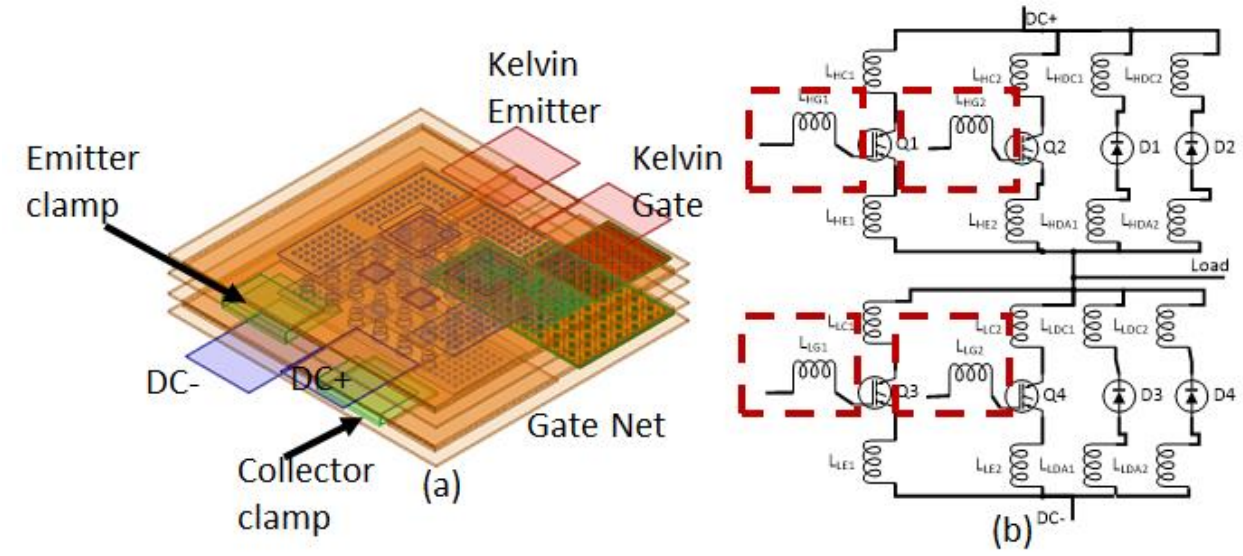

Fig. 3.9. Gate net of the 3-D stack power module

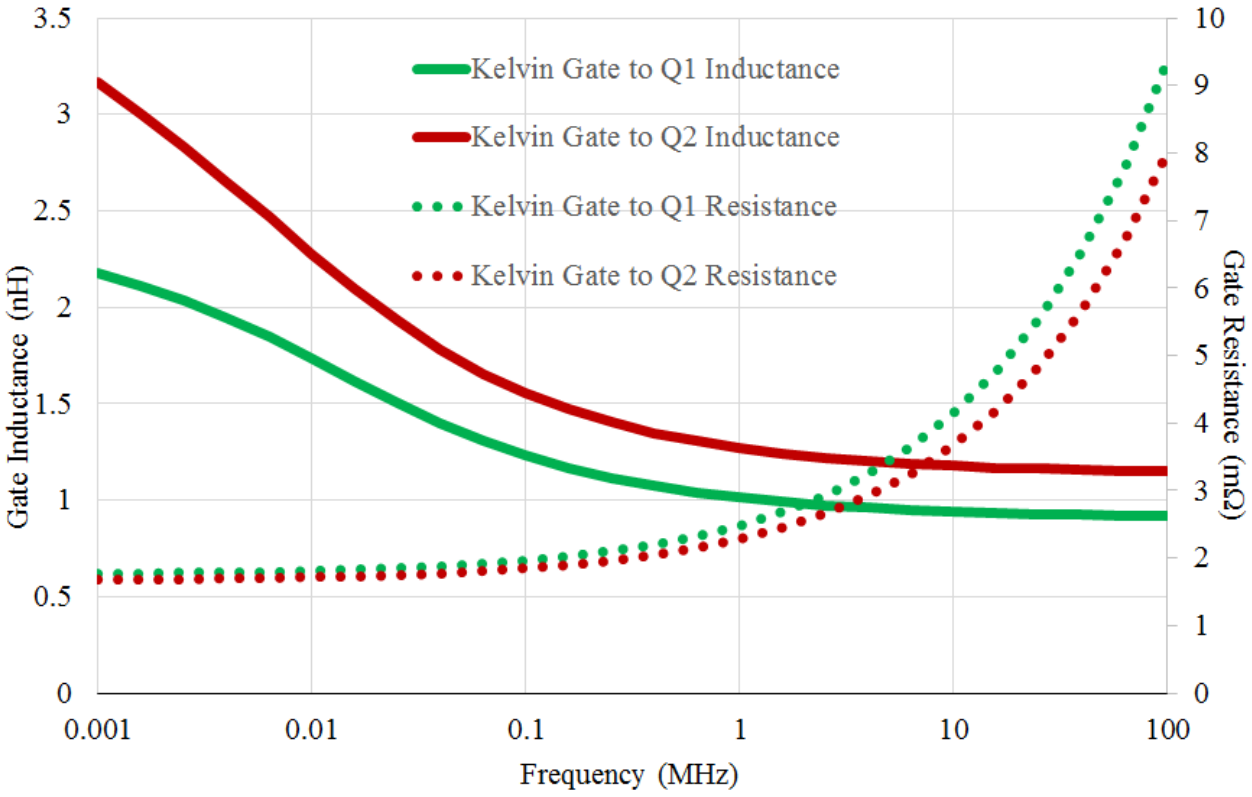

Fig. 3.10. Frequency dependent parasitic inductance and resistance of gate net of the 3-D stack power module

3.6 DC+ to DC- Loop Inductance

The overall loop inductance that is associated with the path has a significant effect on the switching behavior of the power module. As such, the loop inductance should be minimized. As discussed earlier, an anti-parallel current path configuration is implemented to layout the forward and return current paths, the resultant partial current cancellation helps reduce the overall parasitic inductance of the loop. There are two commutation loops associated with the half-bridge stack. One loop includes the high-side IGBT devices and the low-side anti-parallel diodes. The other loop includes the low side IGBT devices and the high side anti-parallel diodes. Fig. 3.11 shows the loop inductance net for the 3-D module stack. Fig. 3.12 plots the frequency dependent inductance and resistance associated with the loop.

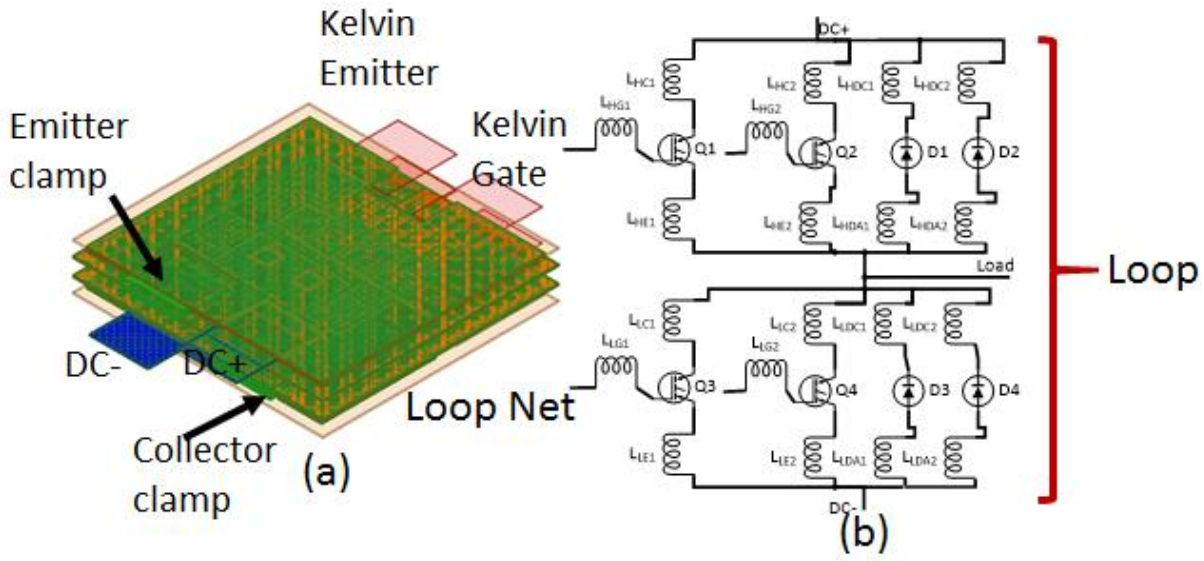

Fig. 3.11. DC+ to DC- loop net for 3-D half-bridge stack power module configuration

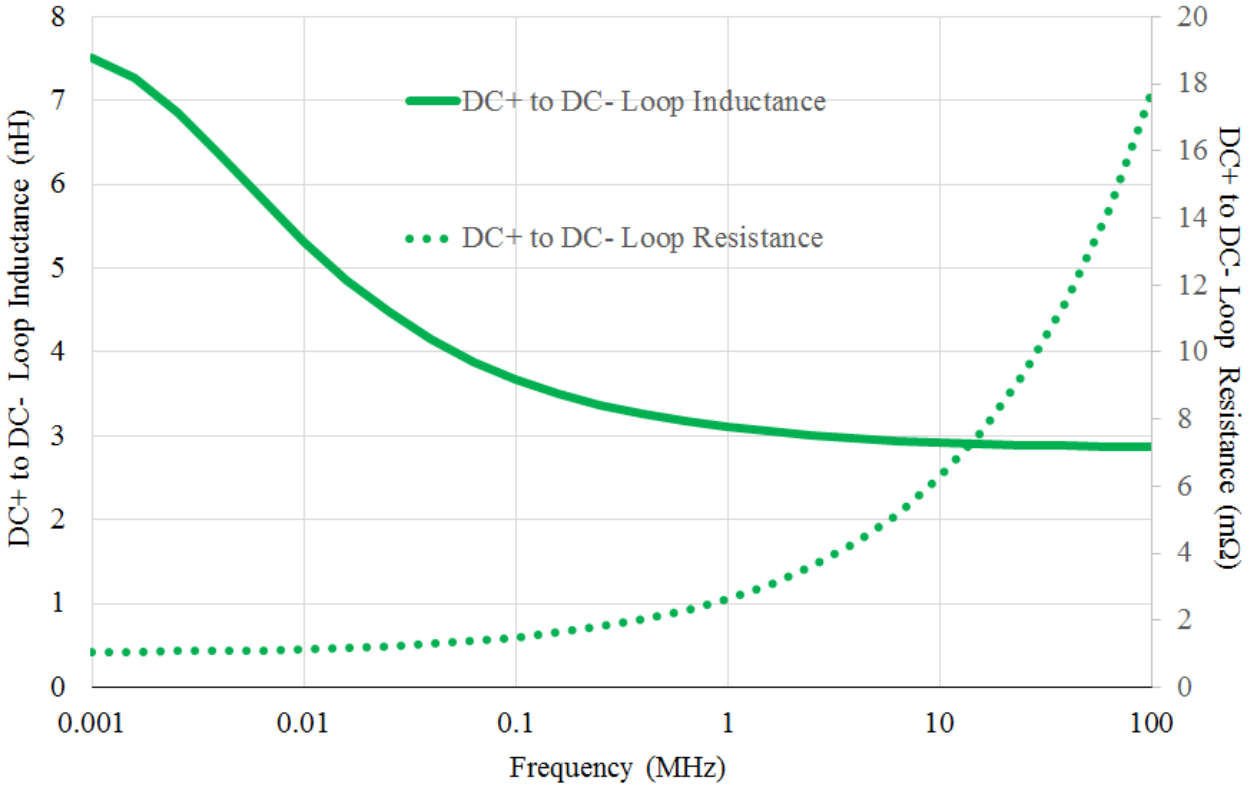

Fig. 3.12. Frequency dependent inductance and resistance for DC+ to DC- loop net of the 3-D half-bridge stack power module

3.7 Effect of Connector Placement on Parasitic Inductance

The placement of the DC+ and DC- terminals along with the conductive clamps play a significant role in reducing the overall loop inductance of the 3-D stack. The parasitic inductance is primarily dependent on the physical distances between the interconnections on the layout. Parasitic simulations followed by surface current density plots are examined to determine the shortest current path between the DC+ and DC- terminals to optimize the loop parasitic inductance. Three cases as shown in Fig. 3.13, Fig. 3.14 and Fig. 3.15 are investigated. In each case, the loop start from the DC+ terminal goes through the emitter and collector clamps to the DC- terminal, and vice-verse, however, the three cases are differentiated by the physical distance

between the interconnections. In case 1, the DC+/collector clamp is placed at the opposite side of the DC-/emitter clamp as shown in Fig. 3.13. In case 2, DC+ and the collector clamp of the bottom stand-alone module are placed opposite side of the module. Similarly, the DC- and the emitter clamp is placed at the opposite side. Case 2 is represented in Fig. 3.14. In case 3, the DC+/collector clamp and DC-/emitter clamp is placed on the same side of the module as shown in Fig. 3.15. In these figures, L1-L6 represent the different conducting layers in the 3-D stack. The conduction path of the loop is marked with black arrows. As can be seen from Fig. 3.13 and Fig. 3.14, the current conduction paths in L3 and L4 layers are in the same directions for both cases 1 and 2. As such, the anti-parallel current path configuration is partially violated for L3 and L4 layers in both cases 1 and 2. On the contrary, as can be seen from Fig. 3.15, by placing the DC+/collector clamp and DC-/emitter clamp on the same side of the 3-D stack, the anti-parallel current path configuration is maintained throughout the conducting loop. As such, the current path configuration follows an anti-parallel path configuration in each layer along the conducting path from the DC+ to DC- terminal.

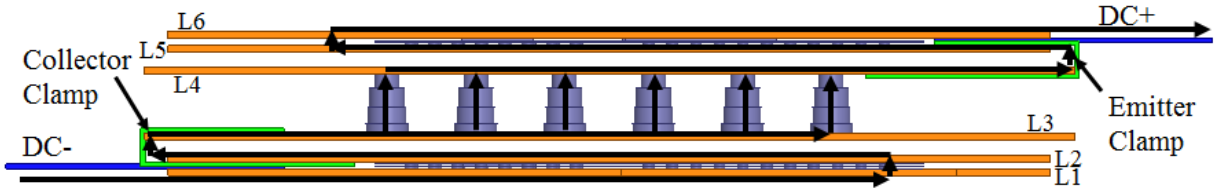

Fig. 3.13. Connectors placed opposite to each other (case 1)

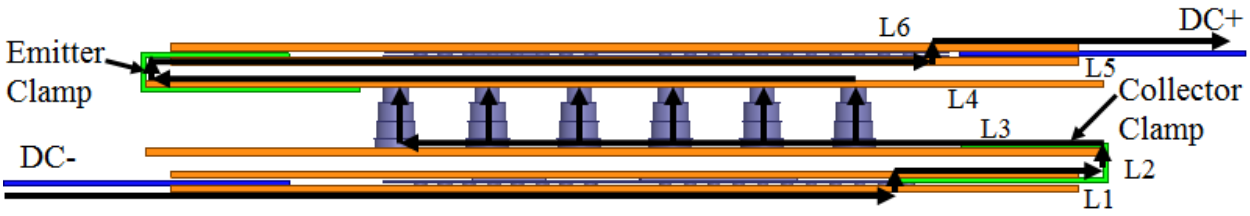

Fig. 3.14. Connectors placed opposite to each other (case2)

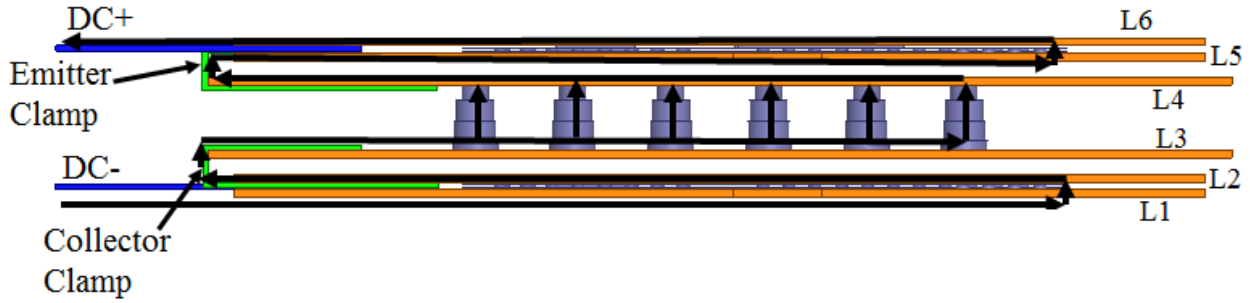

Fig. 3.15. Connectors placed on the same side of the module (case 3)

Fig. 3.16, Fig. 3.17 and Fig. 3.18 represent the surface current density plots corresponding to the connector placements configurations in cases 1, 2 and 3 as shown in Fig. 3.13, Fig. 3.14 and Fig. 3.15 respectively. The surface current density for the connector configurations in case 1 and case 2 mostly follow the same current density pattern. From the current density plots shown in Fig. 3.16 and Fig. 3.17, it can be observed that the surface current density is more uniform for case 1 and case 2 connector configurations. However, for case 3, as can be seen from Fig. 3.18, the surface current density is mostly concentrated in the vicinity of the terminals and the conductive clamps. As such, the spring contacts closer to the DC+, DC- and the conductive clamps are subject to higher surface current density due to proximity to the shortest current conduction path compared to the other spring contacts placed at a further distance from the connectors. The placing of the connectors along with the anti-parallel current path provides a very low loop inductance path between the DC+ and DC- terminals. The parasitic inductance simulation for all

three cases is performed by assigning source and sinks terminals between the DC+ and DC- terminals. The frequency dependent parasitic simulation plots are shown in Fig. 3.19. As can be seen from Fig. 3.19, the parasitic simulation for case 3 connector placements shows a significant reduction of parasitic loop inductance as compared to cases 1 and 2. Case 2 exhibits the highest parasitic inductance of the three configurations as the physical length between the interconnections are the longest. Placing the connectors as in case 3 configurations can achieve a 4.5 nH decrease in loop inductance compared to the other two configurations.

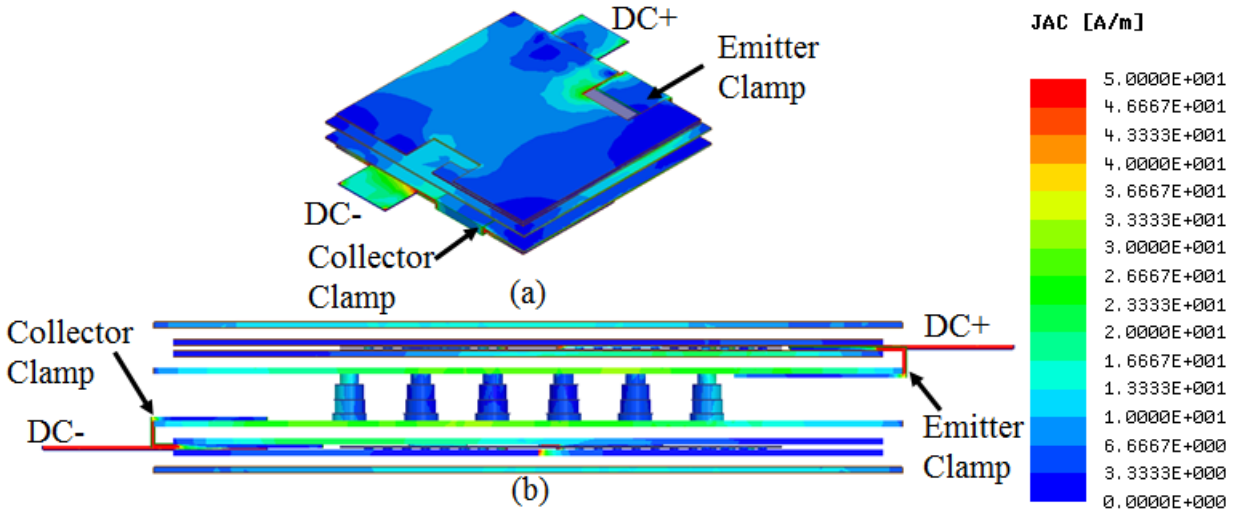

Fig. 3.16. Surface current density with connectors and conductive clamps placed opposite to each other (case 1)

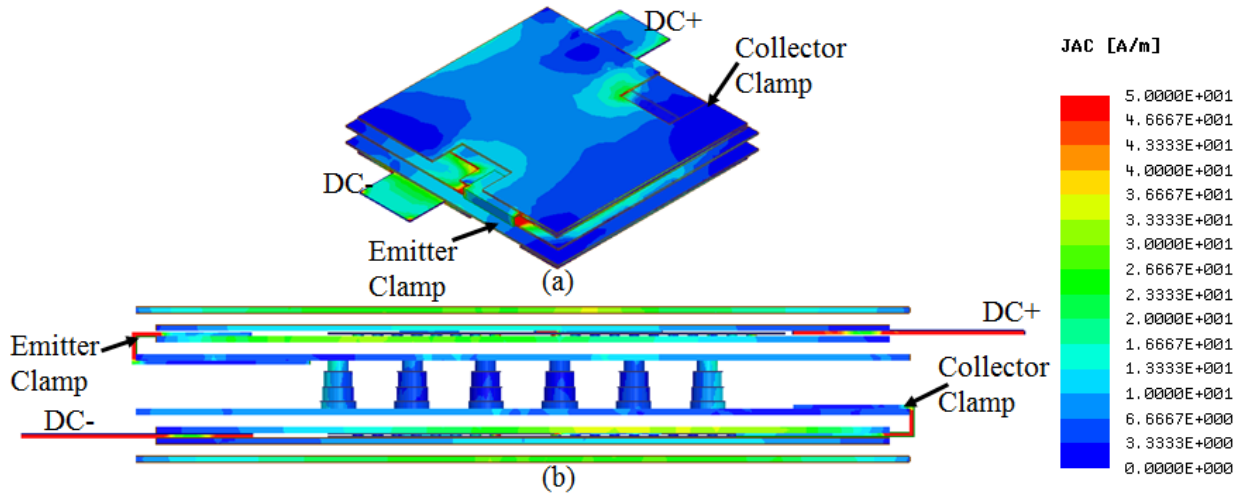

Fig. 3.17. Surface current density with connectors and conductive clamps placed opposite to each other (case 2)

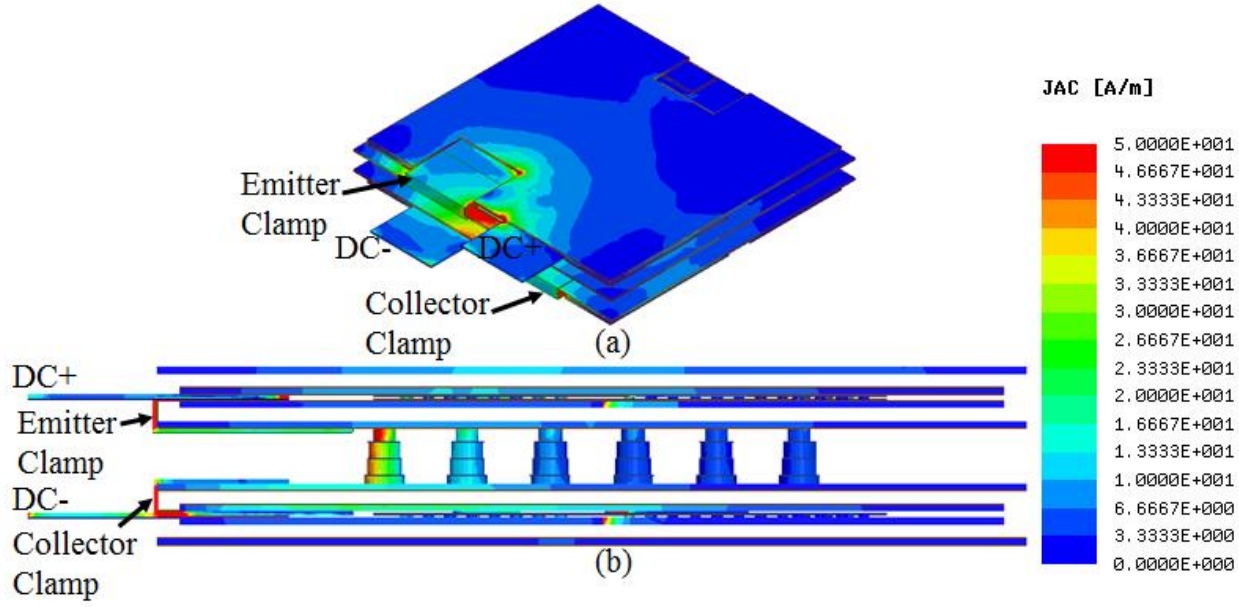

Fig. 3.18. Surface current density with connectors placed on the same side (case 3)

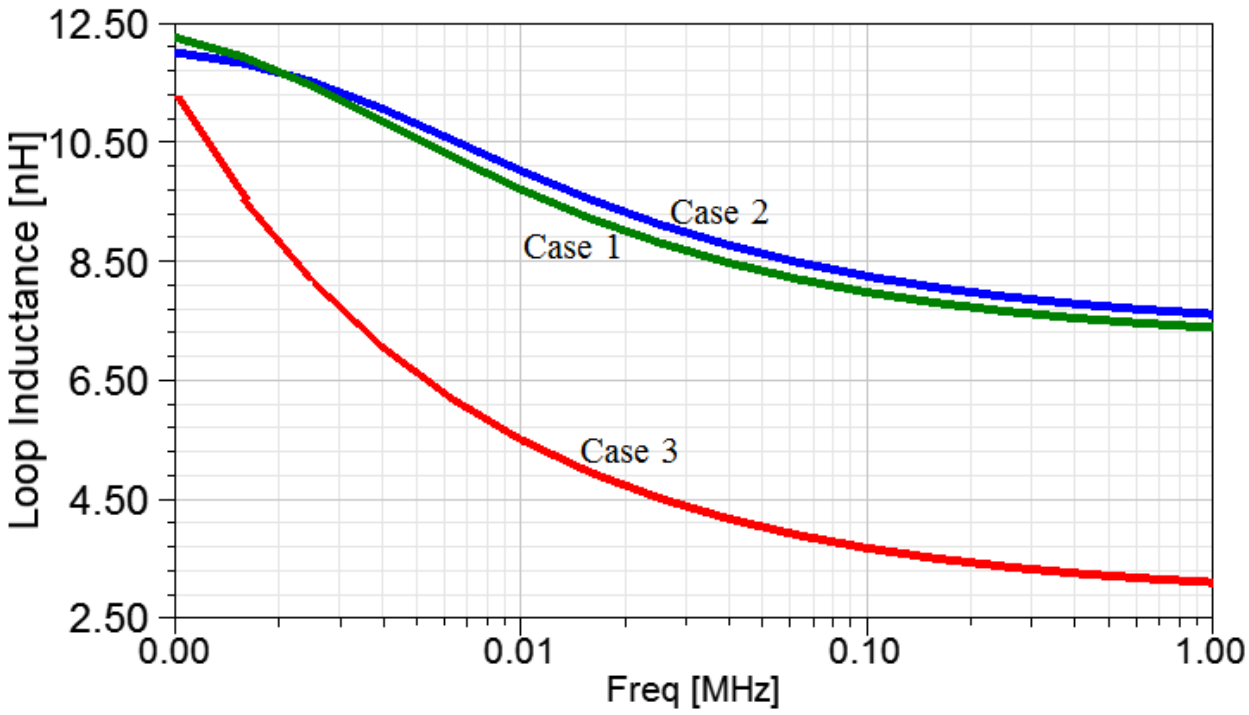

Fig. 3.19. Comparison of DC+ to DC- loop parasitic inductance between cases 1, 2 and 3

3.8 Measurement of Parasitic Inductance

Parasitic inductance measurement is performed in order to validate the parasitic inductance extracted from Q3D simulations. In order to verify the simulation with the parasitic measurement, the loop inductance between the collector and emitter terminal of the stand-alone power module is first simulated using ANSYS Q3D. Fig. 3.20 represents the conducting net between the collector-emitter of the stand-alone power module. Fig. 3.21 plots the frequency dependent parasitic inductance and resistance between the collector and emitter of the stand-alone power module.

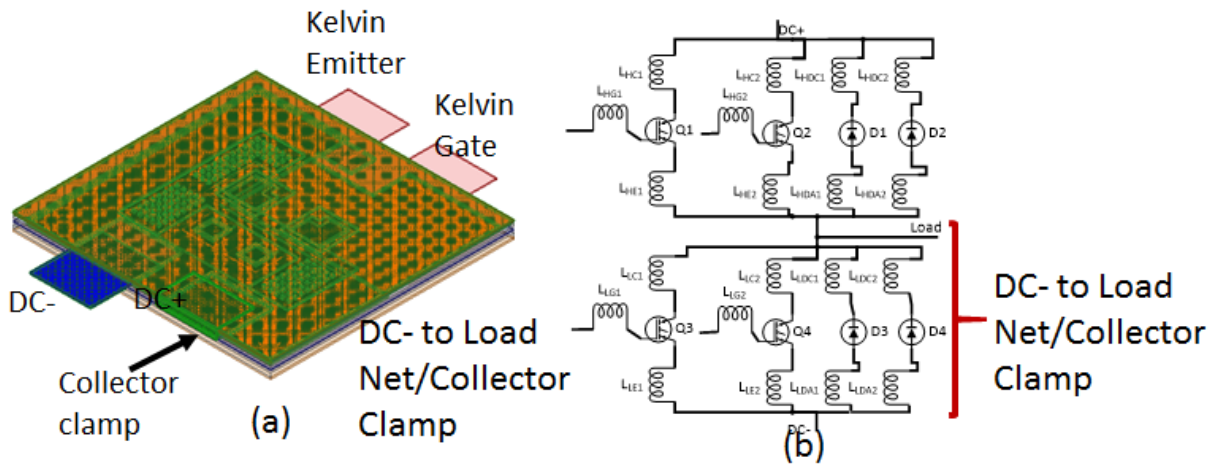

Fig. 3.20. DC terminal to load loop net (stand-alone modules)

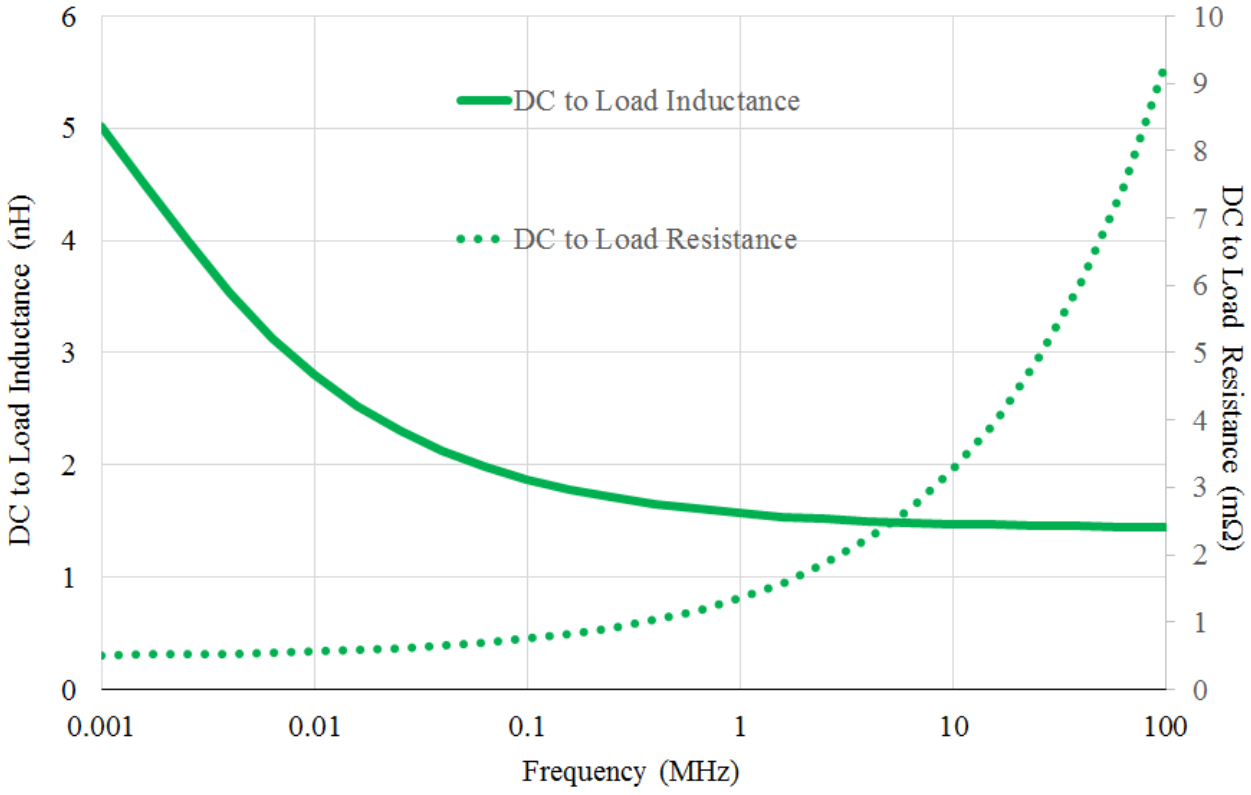

Fig. 3.21. Frequency dependent inductance for DC to load loop net

The parasitic inductance measurement is performed using an HP 4284A precision LCR meter. In order to perform parasitic inductance measurement, a continuous path is required between the two measurement points on the device under test (DUT). As such, a dummy stand-alone power module is fabricated for the measurement. For the dummy sample, a conductive dummy device is attached to short the collector and emitter terminals of the dummy module. Fig. 3.22 represents the dummy module fabricated for the inductance measurement. The emitter and collector terminal leads of the stand-alone power module are inserted into a text fixture (HP 160474) to perform the inductance measurement as shown in Fig. 3.23. The inductance measurement is performed at nine frequency points between the range 10 kHz to 1 MHz. The inductance measurement is performed at a constant current level

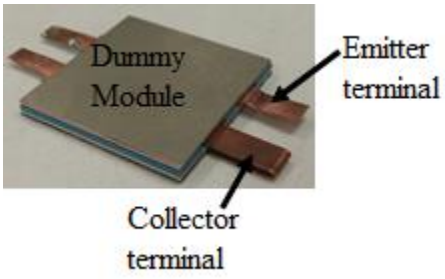

Fig. 3.22. Dummy module fabricated for inductance measurement

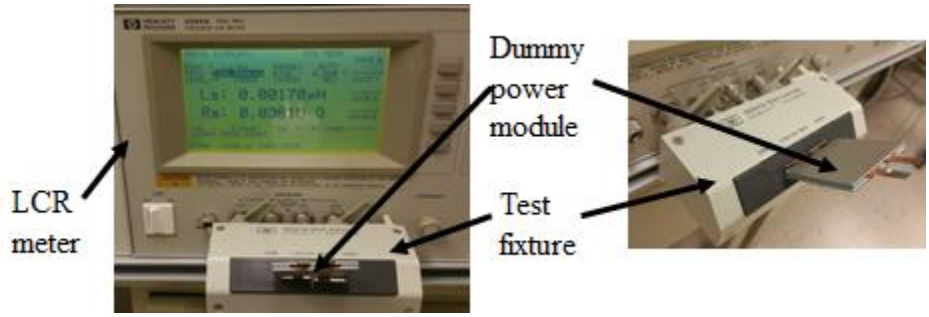

Fig. 3.23. Test setup for the inductance measurement using HP 4284A LCR meter and HP 160474 test fixture

of 100 mA. The constant current level is set during the measurement to avoid any variation that may otherwise occur due to different current levels at different measurement frequencies. In order to ensure repeatability of the measurement data, several measurements are taken and compared to each other. It is observed that the parasitic inductance data slightly varies depending on the contact point between the lead and the test fixture. However, the variation between the different sets of measurements are less than 0.5 nH at desired frequency range.

Fig. 3.24 shows the comparison between the simulated and two sets of measured parasitic inductance of the collector-emitter loop of the stand-alone power module. As can be seen, the simulated results closely match the measured parasitic inductance results validating the parasitic extraction simulations performed in ANSYS Q3D.

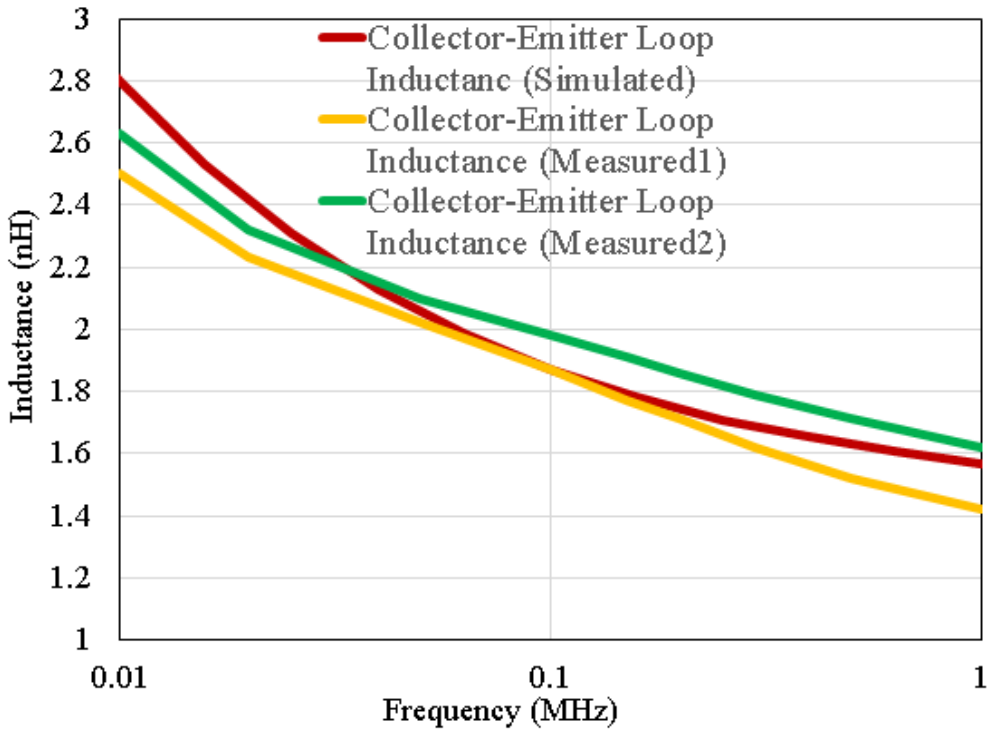

Fig. 3.24. Comparison between simulated and measured parasitic inductance of collector-emitter loop of stand-alone power module

3.9 High voltage simulation

For high-voltage power modules, the dielectric voltage breakdown generally occurs at the die edge and in the connector lead regions. For high voltage devices edge terminations plays a significant role in increasing the voltage breakdown capability [11]-[13]. From a packaging point of view, proper material selection, passivation, and encapsulations around the die edge significantly increase the voltage breakdown capability of the power module [14]. In order to investigate the capability of the proposed 3-D stack as well as the individual stand-alone power module to withstand high voltage breakdown, electrostatic simulation is performed using ANSYS MAXWELL. The purpose of the simulation is to verify if the materials used in the 3-D stack can withstand the dielectric breakdown due to the electric field generated from the applied voltage. Moreover, it is carried out to observe the critical voltage breakdown points inside the 3-D structure as well as the stand-alone modules. To simulate the high voltage breakdown capability, the dielectric permittivity for all the materials is assigned in ANSYS MAXWELL. A voltage excitation of 1.2 kV is assigned at the collector and emitter terminals are assigned as ground excitation as shown in Fig. 3.25.

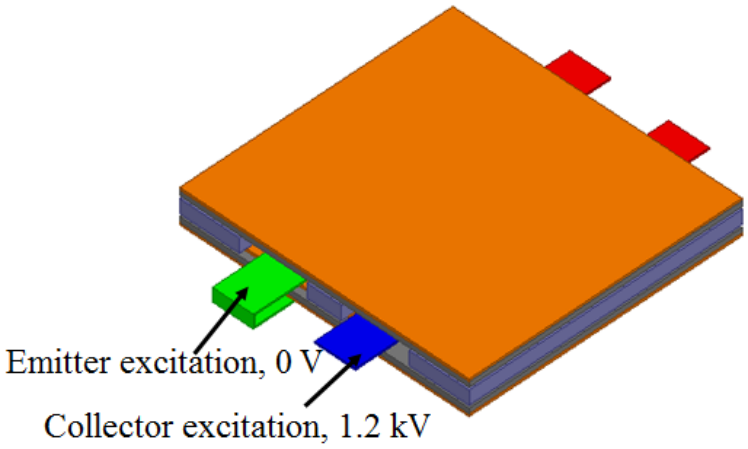

Fig. 3.25. High voltage simulation setup for wire bondless power module

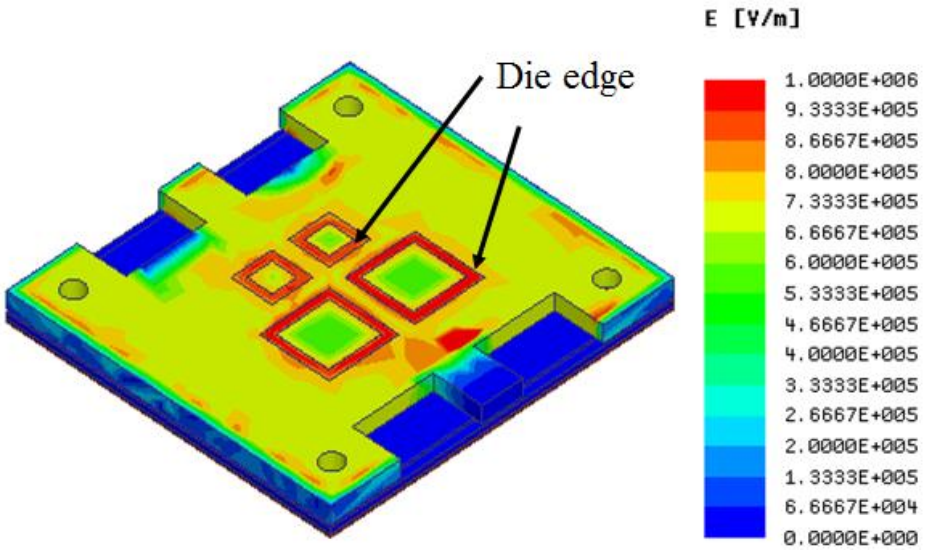

Fig. 3.26. Electric field simulation under 1.2 kV applied voltage

Fig. 3.26 shows the surface plot of electric fields inside the stand-alone power module. The highest electric field in the order of 1 MV/m can be observed at the die edge as shown in Fig. 3.26 for an applied voltage of 1.2 kV. In order to investigate the effect of higher applied voltages, similar simulations were performed applying different voltage levels. The phenomenon

of the highest electric field occurring at the edge of the die remains consistent for different applied voltages. The highest electric fields corresponding to the applied voltage level are listed in Table 3.1. According to the manufacturer's datasheet, LTCC Green Tape™ 951 provides voltage breakdown capability greater than 1000 V/25µm [15]. The thickness of the LTCC die carrier interposer is 1.7 mm. As such, the LTCC die carrier interposer with 1.7 mm thickness provides 40 MV/m dielectric voltage breakdown capability to the stand-alone power module. Commercially available epoxy materials can withstand breakdown voltages of 10-25 kV/mm [16]. Moreover, Al_2O_3 ceramic substrates show voltage breakdown capability of 16 MV/m. It can be seen from Table 3.1, at an applied voltage of 15 kV the highest electric field between the die edge and the edge encapsulation is 17 MV/m. As such, with proper selection of semiconductor devices, encapsulation and passivation around the die edge the structure of the wire bondless stand-alone power module have the potential to withstand significantly higher applied voltages.

Table 3.1. Electric field level at different applied voltage

Applied voltage	Highest Electric Field (MV/m)		
	Die Edge Encapsulation	LTCC	DBC (Al_2O_3)
1.2 kV	1 MV/m	0.66 MV/m	0.00015 MV/m
6.5 kV	6 MV/m	4 MV/m	0.00061 MV/m
10 kV	9.6 MV/m	7 MV/m	0.0009 MV/m
15 kV	17 MV/m	10 MV/m	0.0017 MV/m

In order to verify the proposed 3-D stack structure for its voltage breakdown capability, a voltage excitation of 15 kV is applied to the DC+ and DC- terminals of the stacked modules as shown in Fig. 3.27. The electrostatic simulation results in Fig. 3.28 shows that significantly high electric field in the order of 8 MV/m exists at the interface between LTCC interposer and the bottom and top power modules. The edge termination of the DBC substrates plays a significant role in reducing the high electric fields at both interfaces. The edge terminations for the DBC substrates are not considered for the electrostatic simulation in Fig. 3.28. However, Fig. 3.29 shows the electric field simulation with 2 mm edge termination of copper on both sides of the DBC substrates. As can be seen from Fig. 3.29, the electric field at the edge as well as at the interface is in the order of 1MV/m which is significantly lower than the design without the edge termination of the DBC substrates.

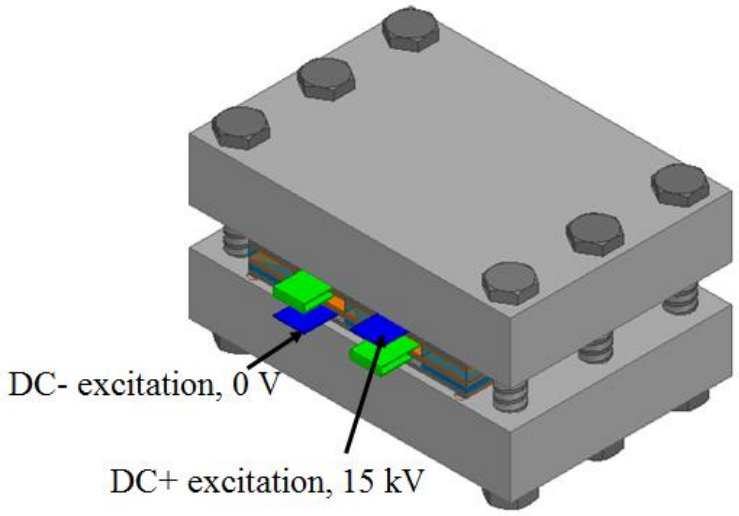

Fig. 3.27. High voltage simulation setup for 3-D stack

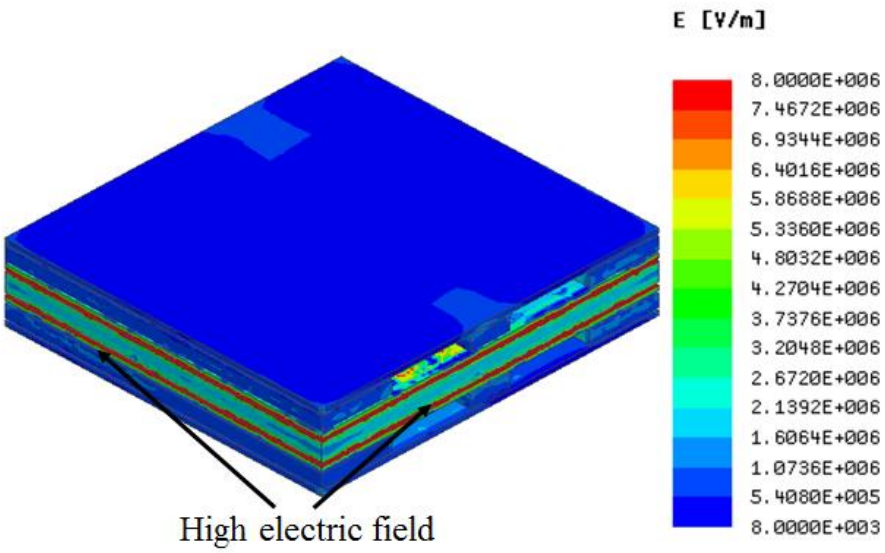

Fig. 3.28. Electric field simulation without edge termination

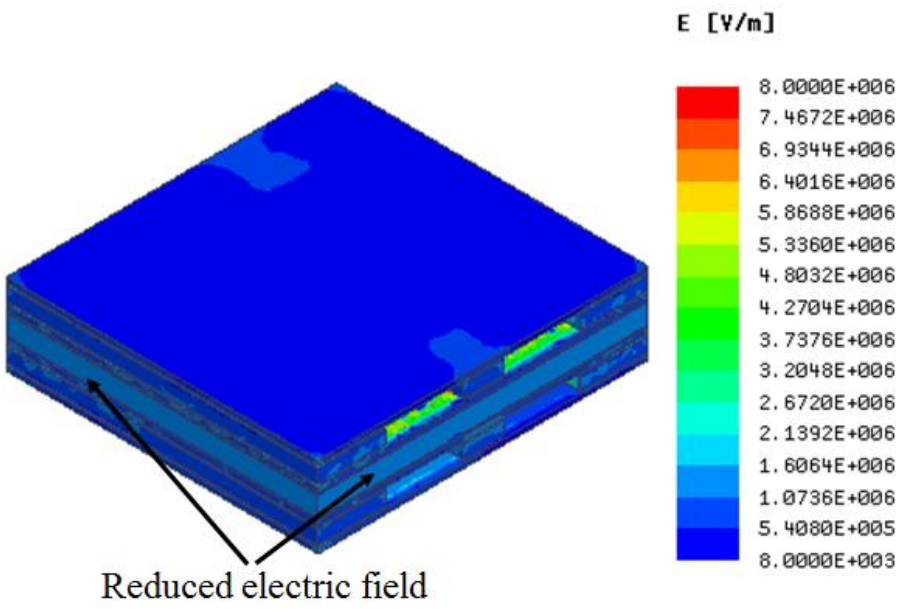

Fig. 3.29. Electric field simulation with 2 mm edge termination

3.10 Thermal Simulations

Thermal simulations are performed on the proposed 3-D wire bondless half-bridge stacked power module using SOLIDWORKS. The stand-alone power modules are effectively double-sided cooling modules with top and bottom DBC substrates. The stack structure is built in such a way that active thermal management can be incorporated to effectively cool each stand-alone power module on the stack from both sides, top and bottom. For the thermal simulation of the stack, the followings are considered:

i. It is considered that the top and bottom holding frames of the 3-D stacked power module consist of water-cooled aluminum blocks
ii. The spring loaded LTCC interposer has liquid microchannels embedded inside it
iii. Force water at 0.001 Kg/s is assumed to flow through all the liquid channels

Fig. 3.30 represents the liquid microchannels embedded inside the spring loaded LTCC interposer.

Fig. 3.31 shows the top and bottom aluminum blocks with liquid channels that are assumed in this thermal study. Fig. 3.32 correspond to the thermal model of the 3-D wire bondless half-bridge stacked power module that is used for the thermal simulations.

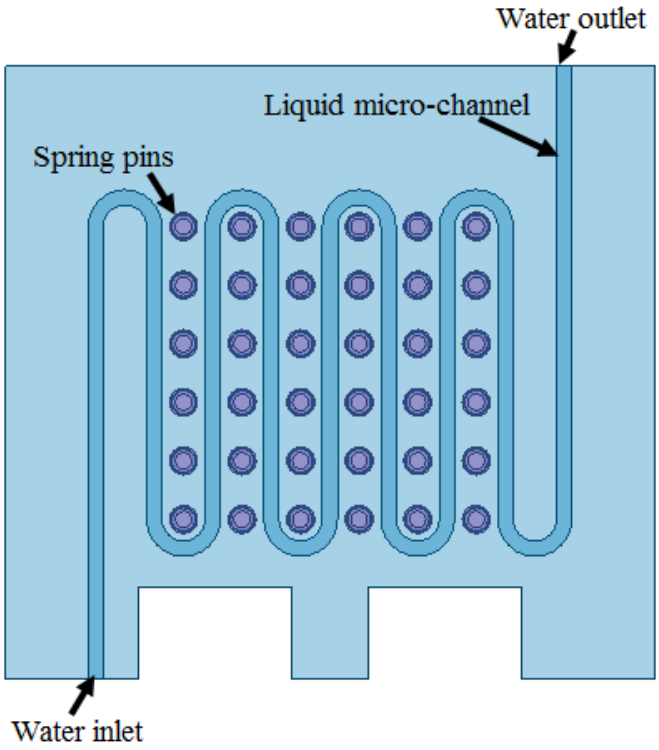

Fig. 3.30. Liquid microchannel embedded into the spring loaded LTCC interposer

In order to perform thermal simulation on the stacked power module, conduction and switching losses are calculated from the manufacturers provided datasheet parameters using standard power dissipation formulas [17]-[18]. The worst-case power dissipation is considered. For switching loss calculation, the operating switching frequency is considered to be 20 kHz. The DC bus voltage and the collector current are considered to be 600 V and 25 A, respectively, for the switching loss calculation.

The total power loss for the IGBT and diodes are considered for the simulation. The total power loss is the summation of conduction loss and the switching loss. The conduction loss for the IGBT devices depends on the on-state resistance and the maximum current rating of the devices. The conduction loss for the SiC Schottky barrier diodes depends on the rated current and the forward voltage drop of the diode. The conduction losses for the Si-IGBT and the SiC Schottky barrier diodes are calculated as 37.5 W and 60 W respectively. The switching loss for the IGBT devices depends on the turn-on and turn-off switching energies. The turn-on and turn-off switching energies are taken from the datasheet at rated voltage and current levels. At an assumed switching frequency of 20 kHz, the switching loss for the IGBT device is calculated to be 126 W. As such, the total power loss for the Si-IGBT and SiC Schottky barrier diode is calculated to be 163.5 W and 60 W respectively. The switching loss for the Schottky barrier diode is negligible and ignored for this simulation.

A two-step process is applied to perform the thermal simulation. The process is as follows:

i. Flow simulation is performed using SOLIDWORKS Flow Simulation package to determine the convection coefficient provided by the water flow inside the liquid microchannels
ii. The convection coefficient thus found from the flow simulation is applied as a convection boundary condition in the SOLIDWORKS thermal simulation using a seamless process.

In order to set up the flow simulation, the model geometry is first imported into SOLIDWORKS. Subsequently, materials assignment is performed using the materials library of SOLIDWORKS. User-defined material properties are assigned for LTCC die carrier substrates and the spring loaded LTCC interposer. Also, user-defined properties are assigned to SiC Schottky barrier diodes. At the start of the flow simulation, in order to define the liquid flow region, LIDS are

assigned at both ends for all three liquid channels. Once the LIDS are assigned, the boundary condition for the flow region is set by defining the water flow rate. The water flow rate for this thermal simulation is defined as 0.001 Kg/s. The water inlets as shown in Fig. 3.30 and Fig. 3.31 are assigned as inlet mass flow boundary condition with a flow rate of 0.001 Kg/s. The water outlets as shown in Fig. 3.30 and Fig. 3.31 are kept at environmental pressure boundary condition. Subsequently, the flow simulation is performed to determine the convection provided by the liquid water flow inside the liquid channels.

After the flow simulation is performed, the thermal simulation is set up. For thermal simulation, thermal loads are applied to the Si-IGBT devices and the SiC Schottky barrier diodes. Heat power of 163.5 W and 60 W are assigned for the Si-IGBT and the SiC Schottky barrier diodes respectively. In order to assign the convection coefficient for thermal simulations, the flow simulation results are imported to the thermal simulations and assigned as a convection coefficient boundary condition. A curvature-based mesh is introduced for the thermal simulations.

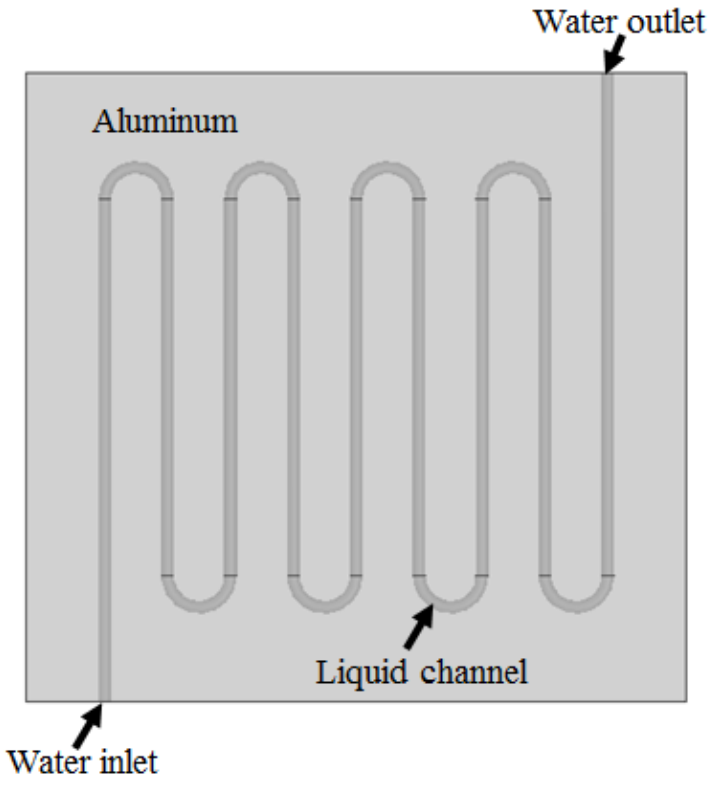

Fig. 3.31. Top and bottom aluminum block with liquid channel showing inlet and outlet

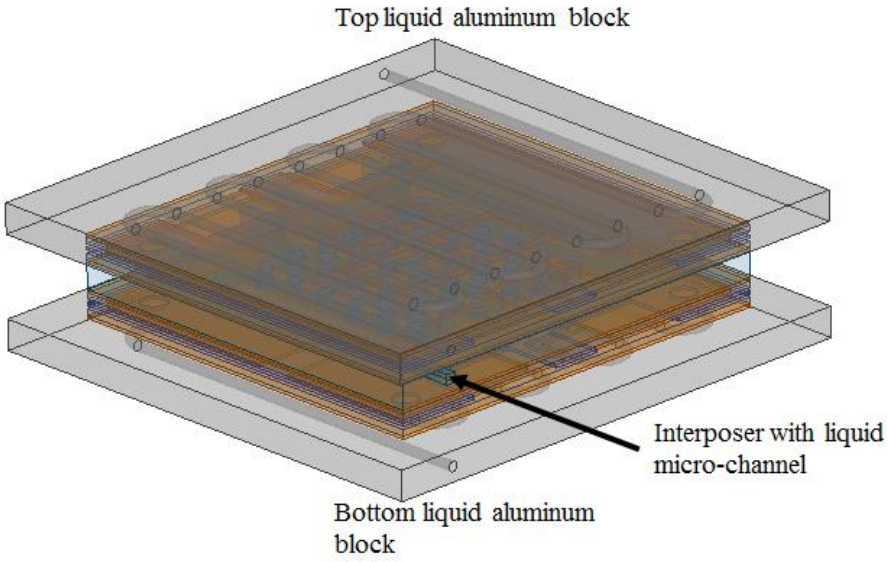

Fig. 3.32. Thermal simulation model for 3-D wire bondless power module with liquid channels

Fig. 3.33 shows the thermal simulation result with free air convection. The convection coefficient assigned for the simulation in Fig. 3.33 is 10 W/m^2K. This simulation is performed to study the effectiveness of the designed microchannels.

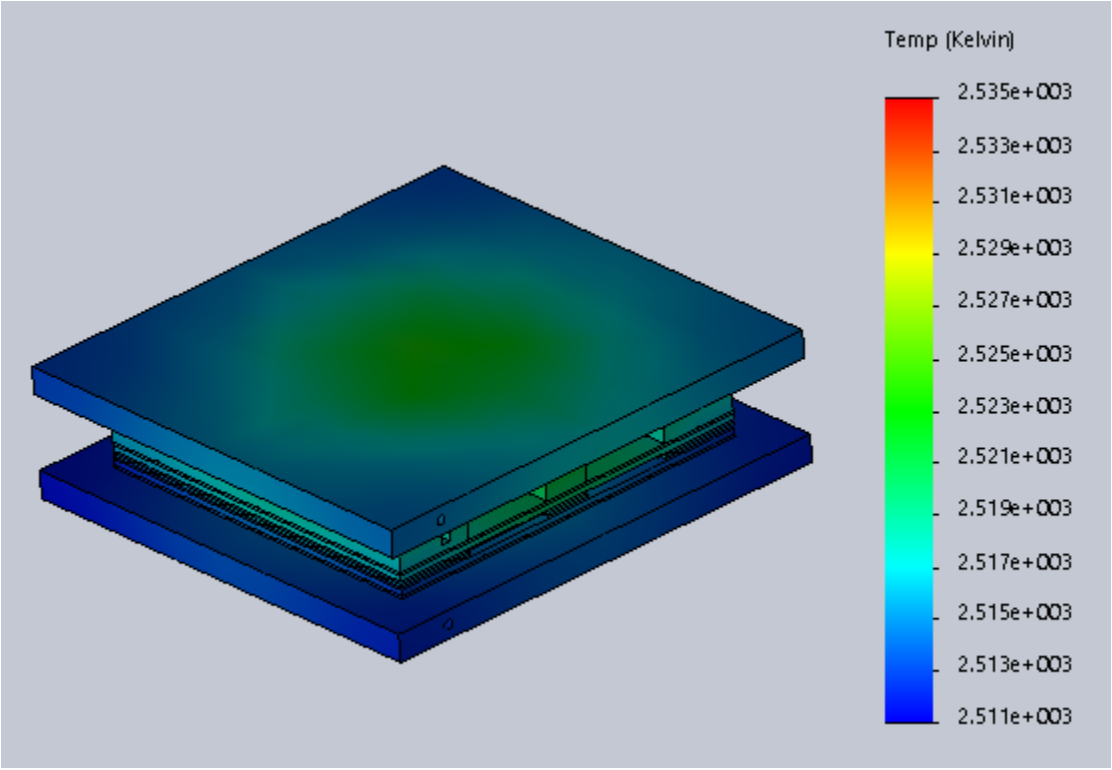

Fig. 3.33. Thermal simulation without liquid microchannel convection

Fig. 3.34 and Fig. 3.35 correspond to the junction temperature of the devices with applied convection coefficient from the SOLIDWORKS flow simulation. As can be seen from both the thermal contour plots the maximum junction temperature for the worst-case power dissipation is 483.58 K (209.85 °C).

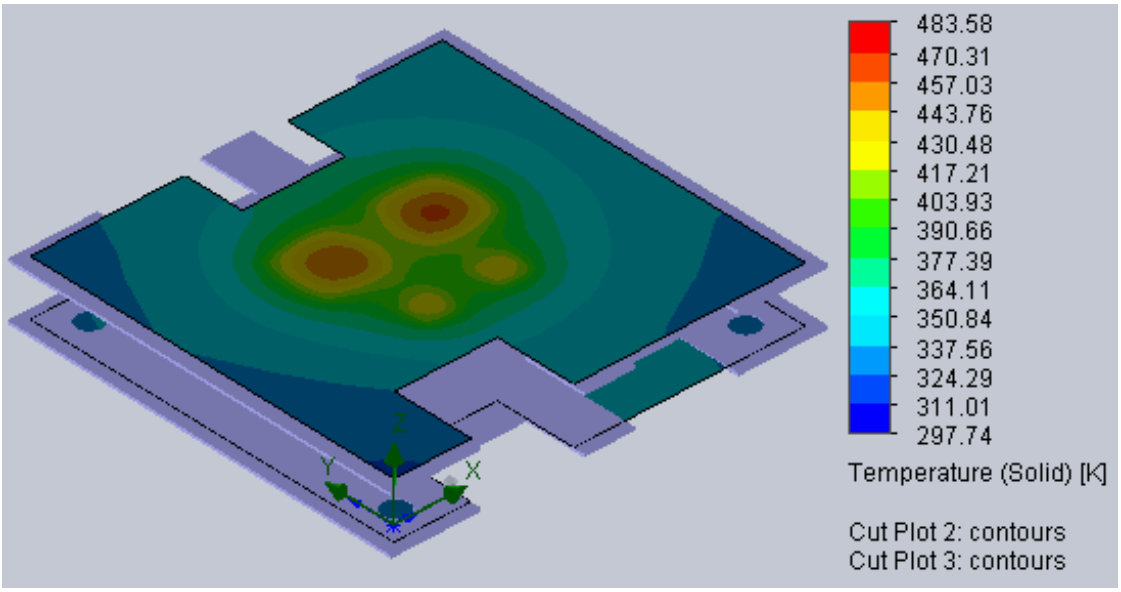

Fig. 3.34. Junction temperature of top module

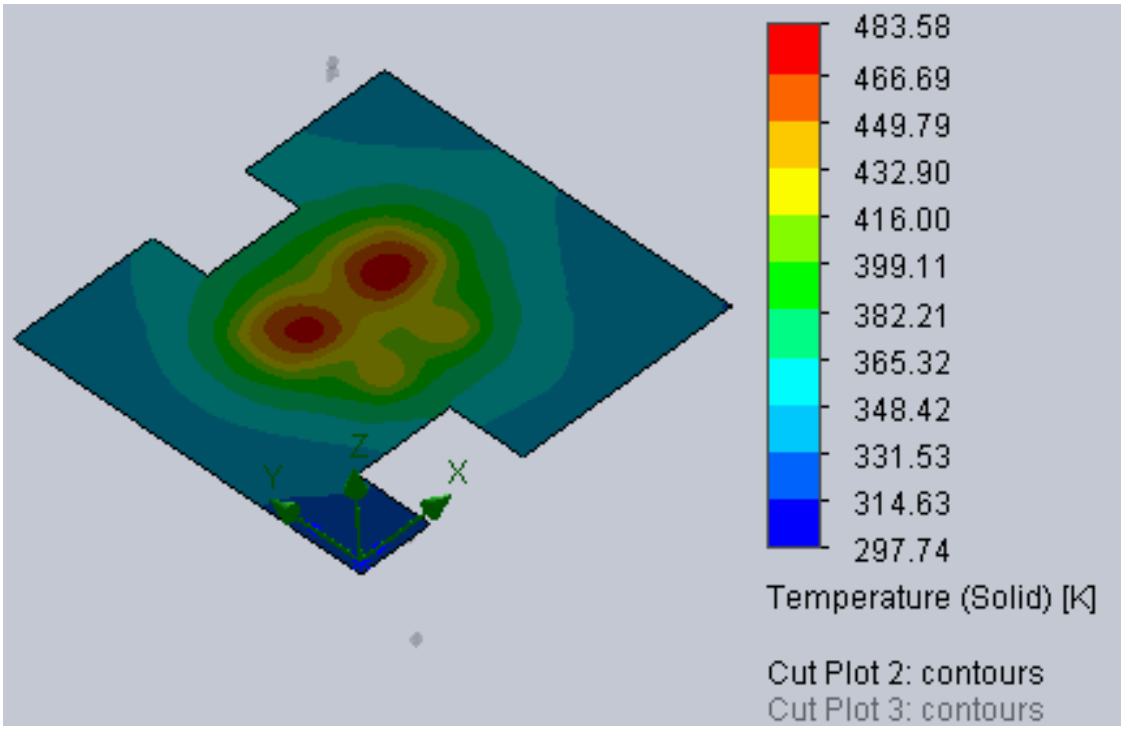

Fig. 3.35. Junction temperature of bottom module

Fig. 3.36 plots the heat transfer coefficient of different microchannel blocks. As can be seen from Fig. 3.36, the heat transfer coefficient of the top and bottom aluminum blocks with liquid

channels are very close to 1000 W/m^2K which is in the range of forced water convection. It can also be observed from Fig. 3.36 that the heat transfer coefficient is lower for the LTCC with liquid microchannel compared to the aluminum blocks. It is due to the low thermal conductivity of LTCC compared to aluminum. Heat transfer is more efficient through a highly thermally conductive material as is the case in aluminum. Fig. 3.37 shows the flow trajectory of the water flow in the microchannel. As can be seen, the pressure drop in water flow is about 22 kPa between the inlet and outlet of water. Fig. 3.38 shows the temperature couture of water inside the channel.

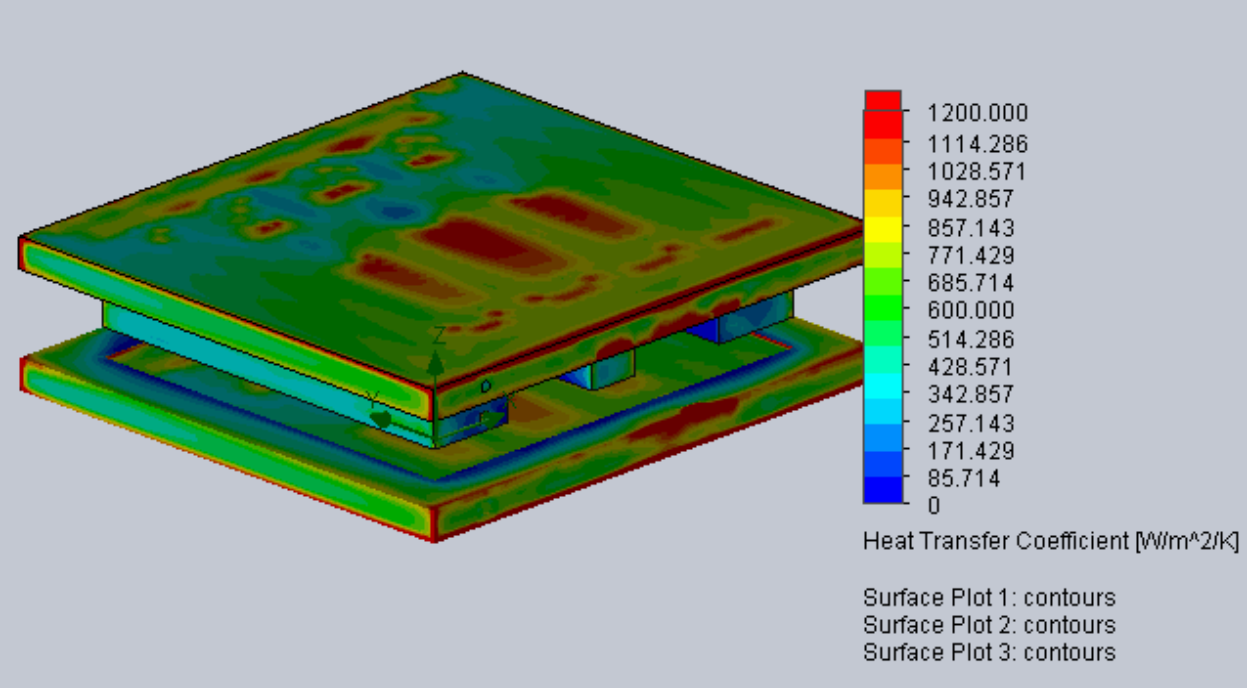

Fig. 3.36. Heat transfer coefficients of the liquid micro-channels blocks

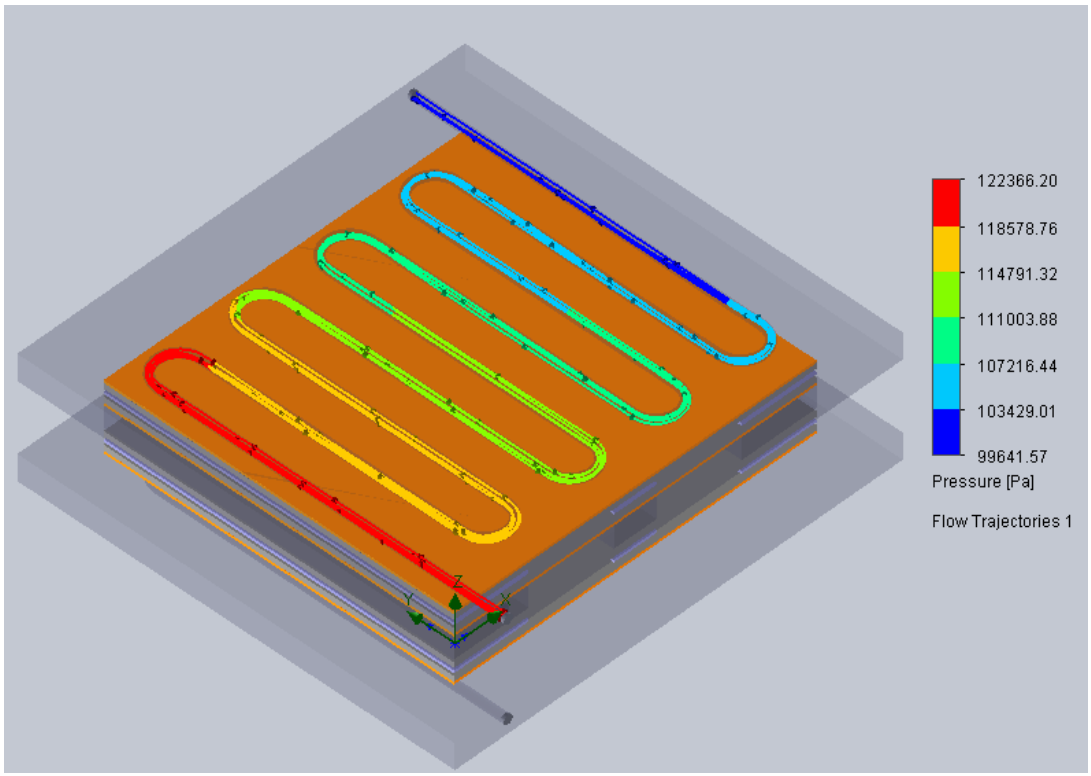

Fig. 3.37. Change of pressure along the fluid flow direction

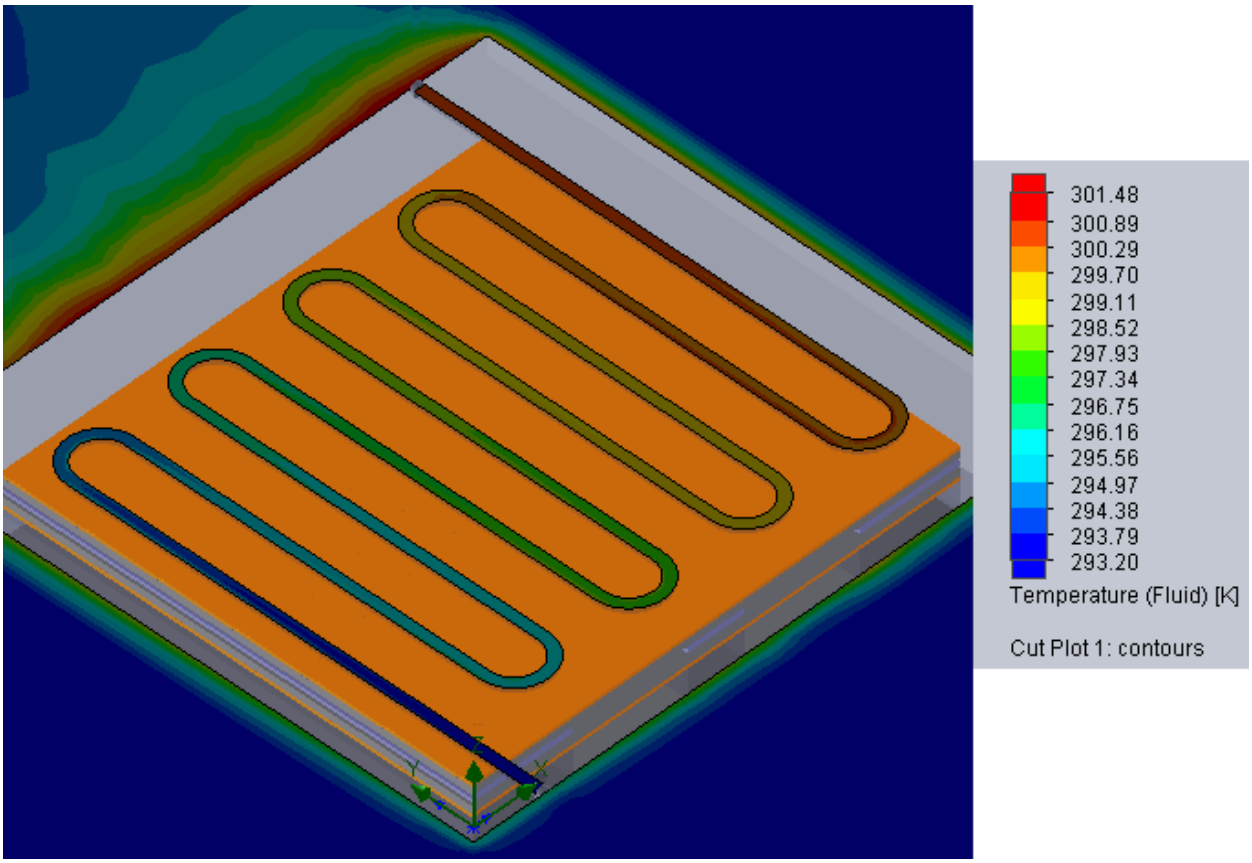

Fig. 3.38. Fluid temperature contour of liquid microchannel

3.11 Chapter Summary

In this chapter, the electrical simulations of the proposed wire bondless 3-D stack are presented. Frequency dependent parasitic inductance of the critical current conducting paths is extracted using ANSYS Q3D parasitic extractor. From the simulations, it is observed that the critical parasitic inductance for all critical path remains below 3 nH in the frequency range of 0.1 kHz to 100 MHz. Moreover, the overall loop inductance of the wire bondless 3-D stack is less than 5 nH in the frequency range 10 kHz to 100 MHz. The parasitic inductance measurement is performed using an impedance analyzer to validate the parasitic inductance simulations performed in Q3D. The frequency dependent inductance measurement shows a high degree of similarity with the simulated parasitic inductance values. The effect of the placement of the input/output and the

load terminals on parasitic inductance are discussed. The design with optimum parasitic inductance is chosen. High voltage electrical isolation simulations are also performed to determine the voltage breakdown capability of the 3-D stack. It has been shown through simulations that, with proper device and materials selection the 3-D stack can withstand significantly high applied voltage. It is also observed, that the electrical field intensity can be greatly reduced by proper edge termination of the top and the bottom DBC substrates of the stand-alone power modules. Thermal simulations are also performed to investigate the feasibility of the 3-D wire bondless half-bridge power module.

3.12 References

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Chapter 4 Parasitic and Switching Characteristics Comparison of Wire Bondless 3-D Stack and Wire Bonded Power Module

The parasitic inductance introduced by the packaging of semiconductor devices affects the switching performance of the devices. In traditional power electronic modules wire bonds are widely used as top side electrical interconnection for the semiconductor device. However, wire bonds introduce additional undesirable parasitic inductance into the current paths. For fast and high-frequency switching, the additional inductance in the current commutation path results into overshoot and ringing in switching waveforms of the semiconductor devices. Wire bondless integration of power semiconductor devices to reduce the parasitic inductance in power module is currently being researched [1]-[6].

The parasitic inductance extraction for the 3-D stack is discussed in Chapter 3. In this chapter, the parasitic inductance of the wire bondless 3-D stack will be compared to its wire bonded counterpart. Subsequently, a switching simulation process flow will be discussed to compare the switching performance of the proposed wire bondless 3-D half-bridge stack with that of the traditional wire bonded half-bridge power module. In order to perform the switching comparison, a wire bonded power module is designed with the same set of devices used to design the 3-D stack.

4.1 Parasitic Inductance Comparison

In order to compare the parasitic inductance of the wire bondless 3-D stack to a wire bonded half-bridge module, a wire bonded half bridge module is designed and parasitic extraction is performed in ANSYS Q3D. Fig. 4.1 represents the design of the wire bonded half-bridge power module. The devices used in the wire bonded power module are the same as the devices used in

the wire bondless 3-D stack. The top and bottom switch of the half-bridge power module consists of two paralleled Si-IGBT devices from ABB (Part no. 5SMX12E1280) with two SiC Schottky barrier diodes from Wolfspeed (Part no. CPW4-1200-S020B) in an anti-parallel configuration. Conducting nets are assigned to extract the parasitic inductance and compare it with the wire bondless 3-D stack. Fig. 4.2 represents the conducting nets of the wire bonded power module. Fig. 4.2 (a) corresponds to the DC+ net. The DC+ net is assigned to extract the parasitic inductance between the DC+ terminal and the collector and cathode of the high-side IGBT and Schottky diodes respectively. The DC- net as shown in Fig. 4.2 (b) corresponds to the inductance path between the DC- terminal to the emitter and anode of the low side IGBT and the diodes, respectively. The common emitter net of the wire bonded module is shown in Fig. 4.2 (c). The common emitter net represents the inductance path between the load terminal to the emitter and anode of the high-side IGBTs and diodes, respectively. Additionally, another set of common emitter inductance is associated with the load terminal to the collector and cathode of the low-side IGBTs and diodes, respectively. The gate loop inductance between the Kelvin terminal and the gate of the high-side IGBT devices are shown in Fig. 4.2 (d). Fig. 4.2 (e) correspond to the emitter loop between the Kelvin emitter terminal and the emitter on the high-side IGBT devices. Fig. 4.2 (g) shows the gate loop between the Kelvin gate pin and the gate of the low-side IGBT devices. Fig. 4.2 (g) shows the Kelvin emitter loop for the low-side devices.

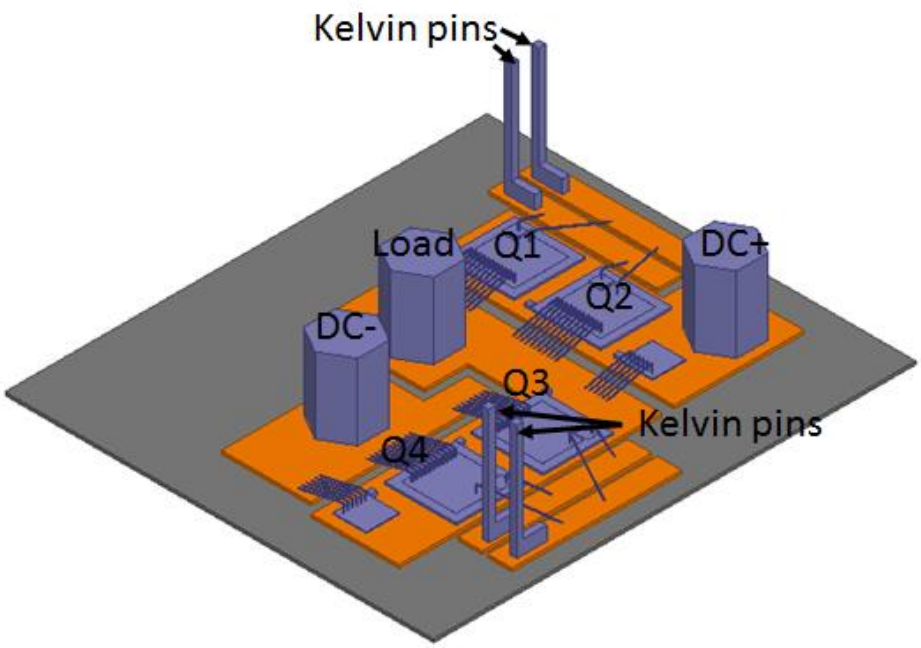

Fig. 4.1. Wire bonded half-bridge power module

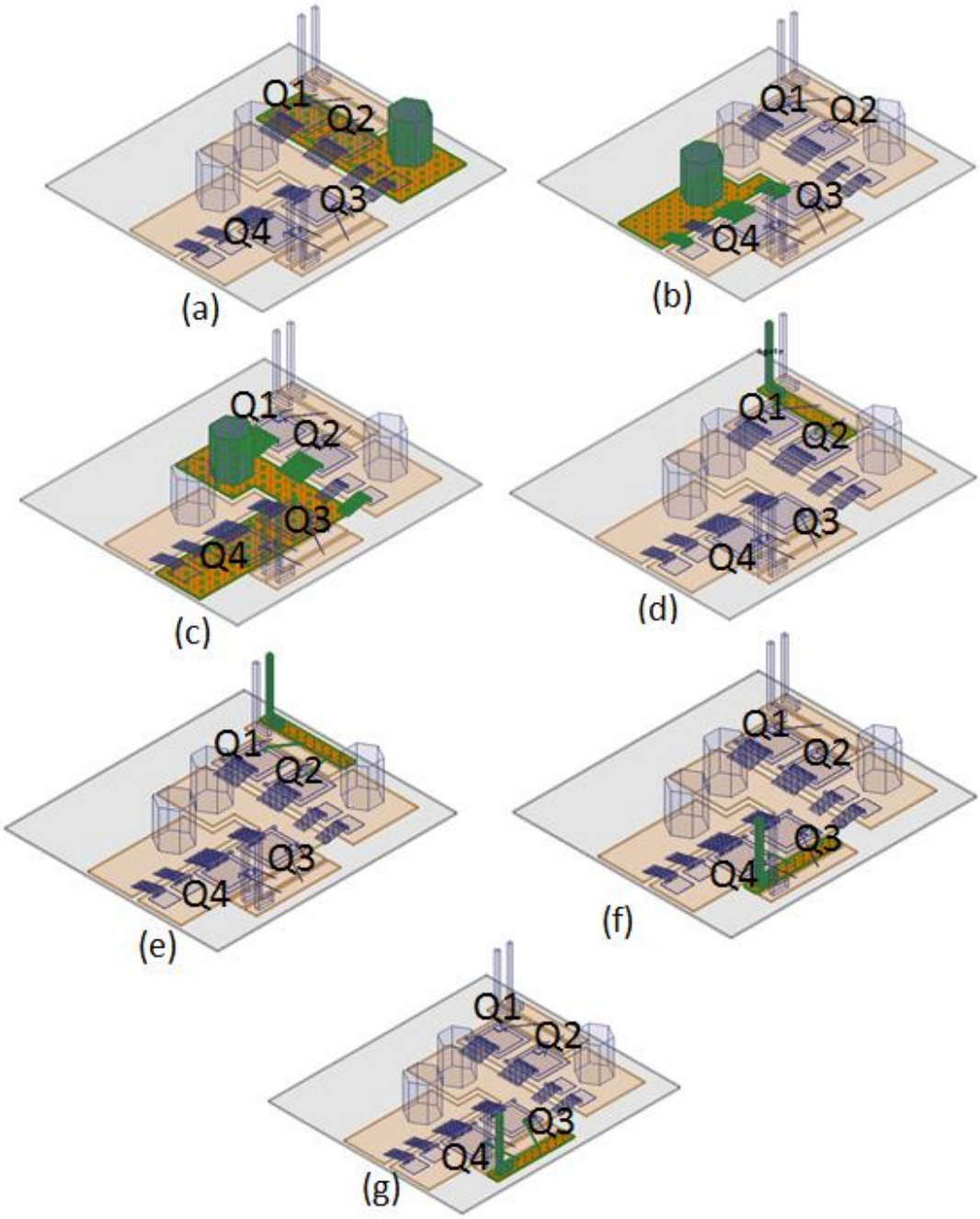

Fig. 4.2. Conducting nets of the wire bonded half-bridge module

4.2 DC+ Inductance Comparison

Fig. 4.3 shows the comparison of the DC+ inductances between the wire bondless 3-D stack and the wire bonded half-bridge power modules. The comparison shows the DC+ inductances between the DC+ terminal to the collector of two paralleled high-side IGBT devices. It is evident

from Fig. 4.3 that the collector inductance for the high-side IGBTs in the wire bonded power module is much higher compared to the devices of the wire bondless 3-D stack. As shown in Fig. 4.3, the collector inductance for the paralleled high-side IGBT devices for the wire bondless module is below 3 nH for the entire frequency range. However, the collector inductance for the paralleled high-side devices for the wire bonded power module is 5.9 nH and 8.9 nH at 100 kHz. Also, the parasitic inductance imbalance between the devices in the wire bonded module is higher compared to those for the wire bondless 3-D stack.

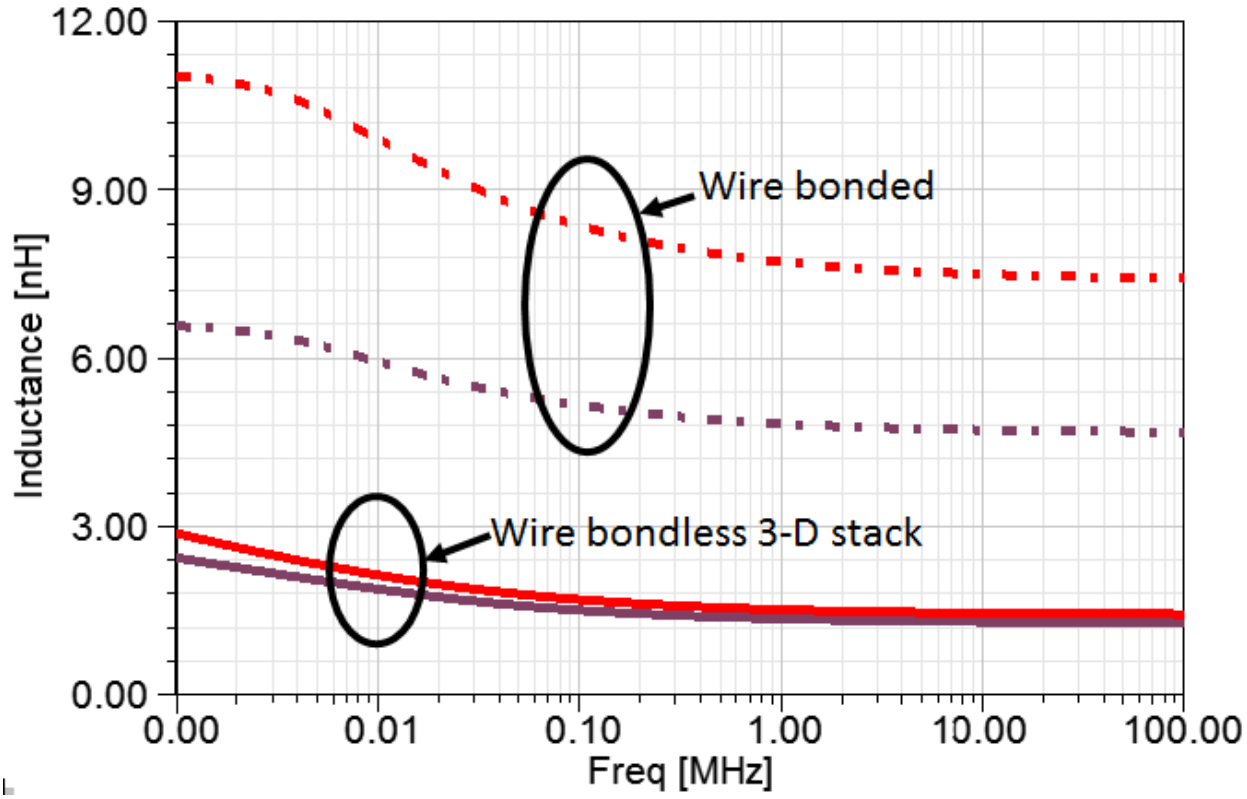

Fig. 4.3. DC+ parasitic inductance comparison between 3-D stack and wire bonded half-bridge

4.3 DC- Inductance Comparison

Fig. 4.4 presents the comparison between the emitter inductances from the DC- terminal to low-side paralleled devices for the wire bondless 3-D stack and the wire bonded half-bridge power module. Similar to the DC+ inductances discussed in section 4.2, the devices in the wire bonded

module exhibit much higher parasitic inductance compared to those of the devices in the wire bondless 3-D stack. Moreover, the parasitic imbalance between the power devices in the wire bonded module is higher. As can be seen from Fig. 4.4, the emitter inductances of the two paralleled low-side IGBT devices are less than 2 nH for the entire frequency range. However, the inductance for the wire bonded devices is 7 nH and 8 nH at 100 kHz.

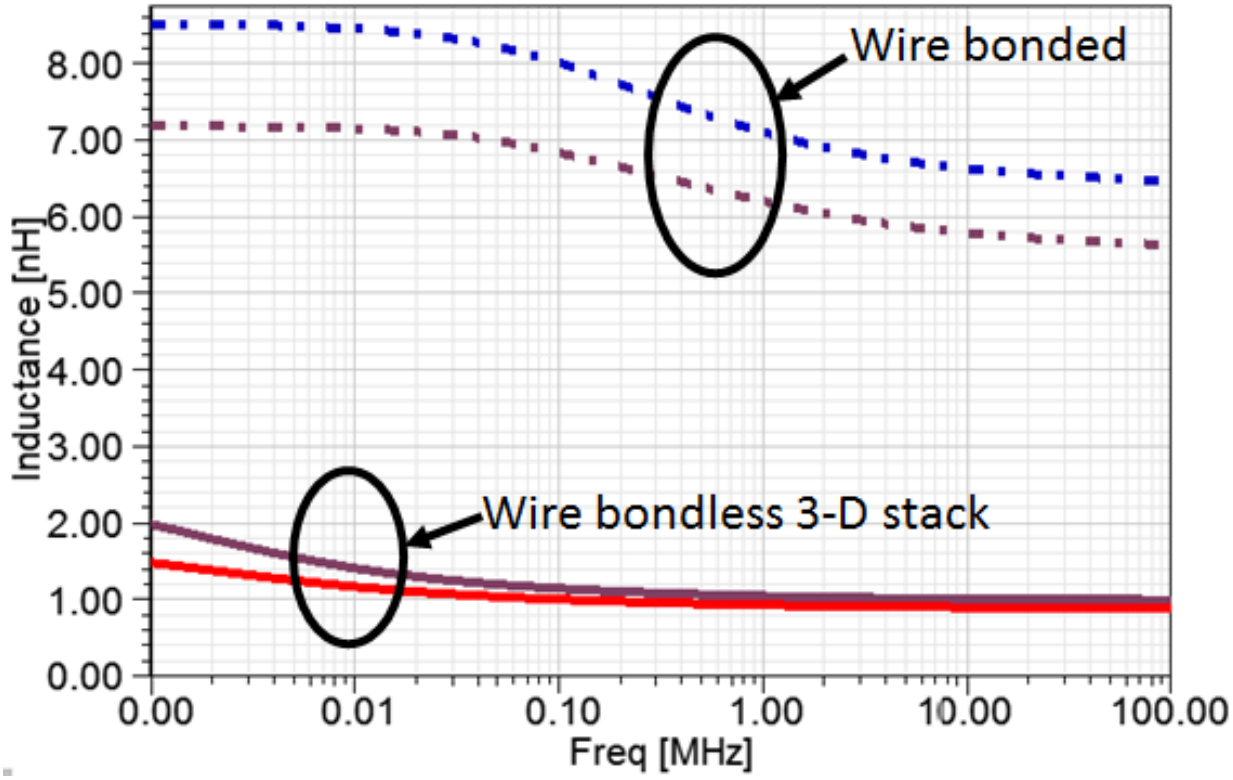

Fig. 4.4. DC- parasitic inductance comparison between 3-D stack and wire bonded half-bridge

4.4 Common Emitter Inductance Comparison

Fig. 4.5 plots the comparison of the common emitter inductances associated with the wire bondless 3-D stack and the wire bonded half-bridge module. The common emitter inductances are associated with the emitter and the collector inductances of the high-side and the low-side devices, respectively, from the load terminal of the power module. As can be seen from Fig. 4.5,

the common emitter inductance is less than 3 nH for the IGBT devices in the wire bondless 3-D stack. However, the common emitter inductances are much higher for the wire bonded devices. Also, the parasitic imbalance is lower in wire bondless stack compared to the wire bonded modules, similar to the DC+ and DC- inductances discussed in sections 4.2 and 4.3.

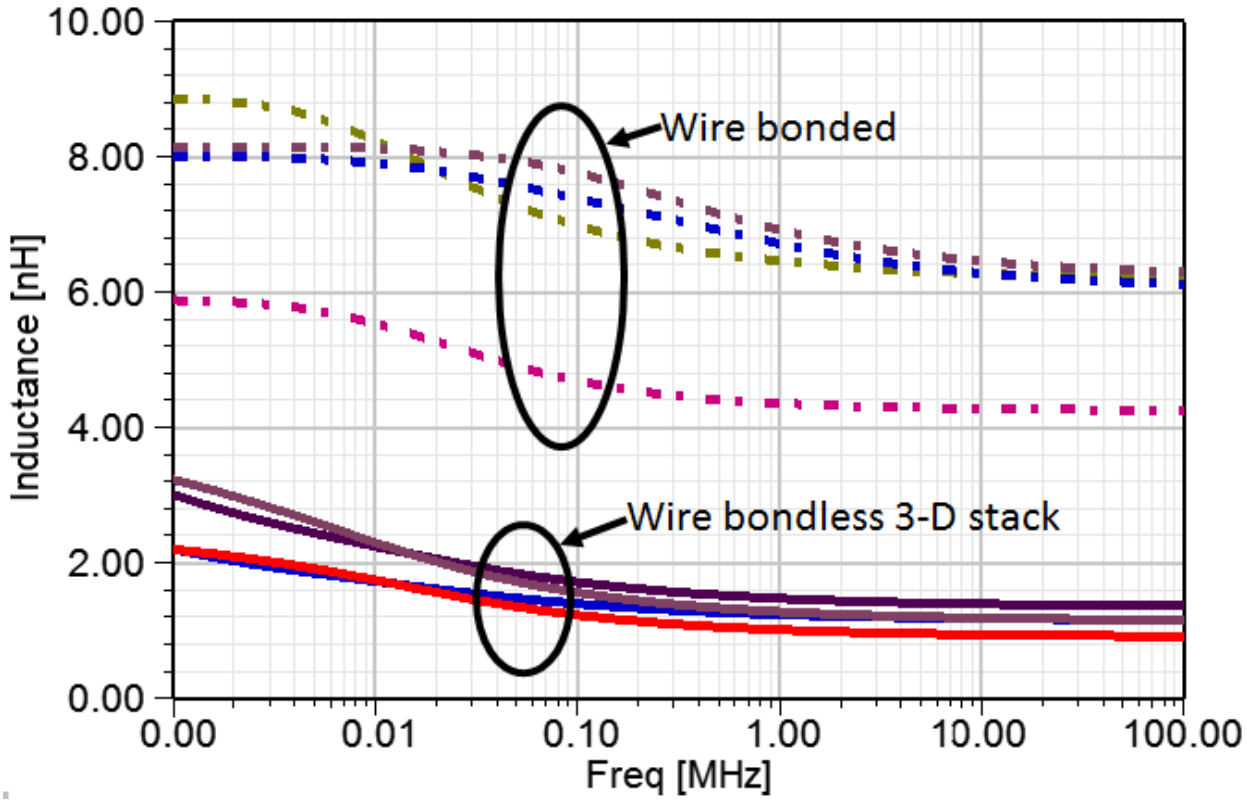

Fig. 4.5. Common emitter parasitic inductance comparison between 3-D stack and wire bonded half-bridge

4.5 Gate Loop Inductance Comparison

Fig. 4.6 plots the parasitic inductance comparison of the gate loop for the wire bondless 3-D stack and the wire bonded half bridge module. As can be seen from Fig. 4.6, the gate loop inductance for the wire bonded module is much higher compared to that of the wire bondless 3-D stack. Also, the inductance is highly balanced for the gate loop for the wire bondless 3-D stack.

For the wire bondless 3-D stack, the gate loop inductance is less than 4 nH over the frequency range. However, for the wire bonded counterpart the gate loop inductances are 10 nH and 15 nH at 100 kHz for the two paralleled IGBT devices.

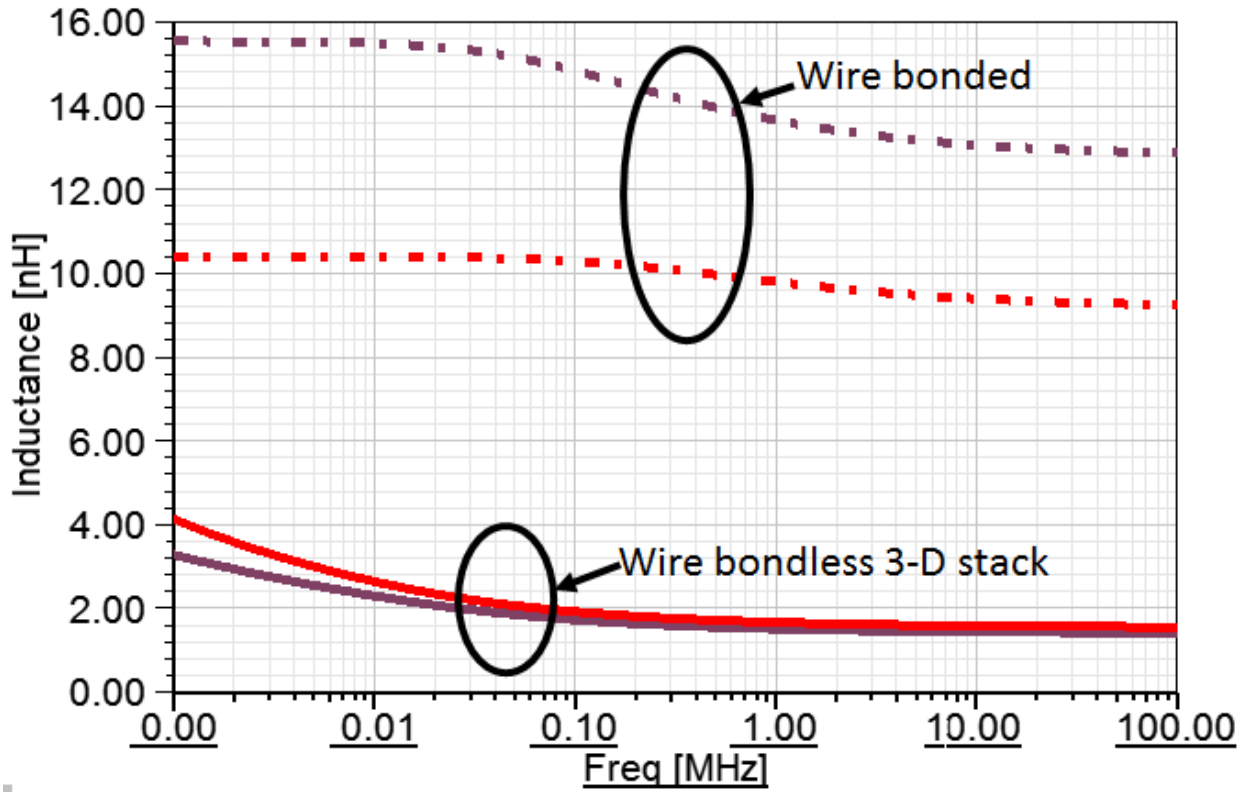

Fig. 4.6. Gate loop parasitic inductance comparison between 3-D stack and wire bonded half-bridge

4.6 DC+ to DC- Loop Inductance Comparison

Fig 4.7 compares the overall loop inductance, i.e., from DC+ terminal to DC- terminal, of the wire bondless 3-D power module to the wire bonded half-bridge module. As can be seen from Fig 4.7, the overall loop inductance for the wire bondless 3-D stack is considerably lower than that of the wire bonded power module. As discussed earlier, an anti-parallel current path configuration is implemented to reduce the overall loop inductance of the 3-D module utilizing

overlapping forward and return current paths on top of each other with opposing direction. As such, the magnetic field generated by the forward and return current paths partially cancels out each other to reduce the overall loop inductance. On the contrary, for a coplanar wire bonded power module, it is difficult to compensate the magnetic field generated by the current-carrying traces. From Fig 4.7, the parasitic inductance of the wire bondless 3-D stack and the wire bonded power module is 4 nH and 14 nH, respectively, at 100 kHz, that corresponds to about 71% of parasitic inductance reduction at 100 kHz for the 3-D power module.

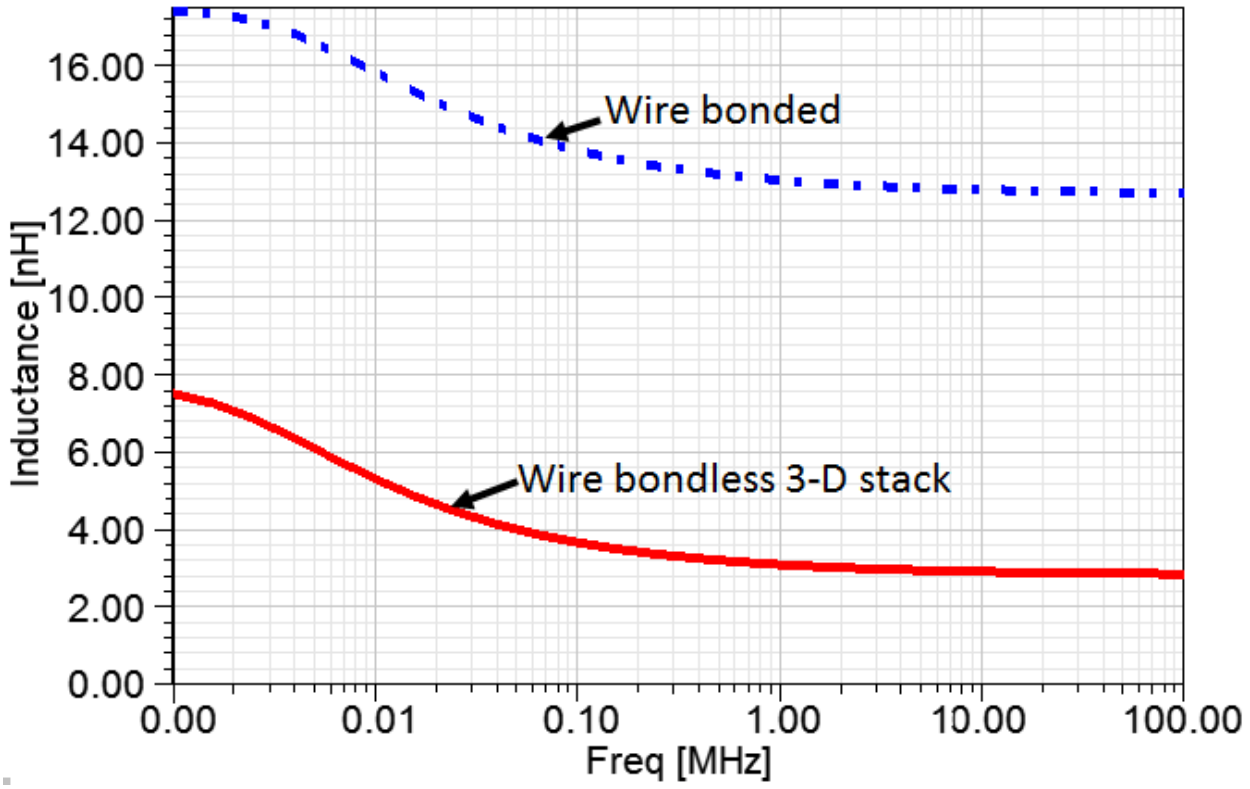

Fig 4.7. DC+ to DC- loop inductance comparison between the 3-D stack and the wire bonded power module

4.7 Simulation flow

A co-simulation approach is taken to perform the switching simulations for the wire bondless 3-D stack and the wire bonded half-bridge module. The design and layout of the power module are performed in ANSYS Q3D [7]-[9]. Subsequently, frequency dependent parasitic parameters associated with various current conducting nets are extracted in ANSYS Q3D [7]-[9]. Following the parasitic extraction, switching simulation is performed in ANSYS SIMPLORER. In order to build the circuit schematic in ANSYS SIMPLORER, the frequency dependent parasitic model is dynamically linked to ANSYS SIMPLORER. Additionally, the devices that are used in designing the power module are characterized using the ANSYS SIMPLORER's device characterization tool using the manufacturers provided datasheet [7]-[9]. Following the device characterization, the circuit schematic for the switching simulation is built around the frequency dependent parasitic model using the characterized devices [7]-[9]. Fig. 4.8 represents a graphical view of the simulation approach taken to simulate the switching behaviors of the 3-D stack and the wire bonded power module.

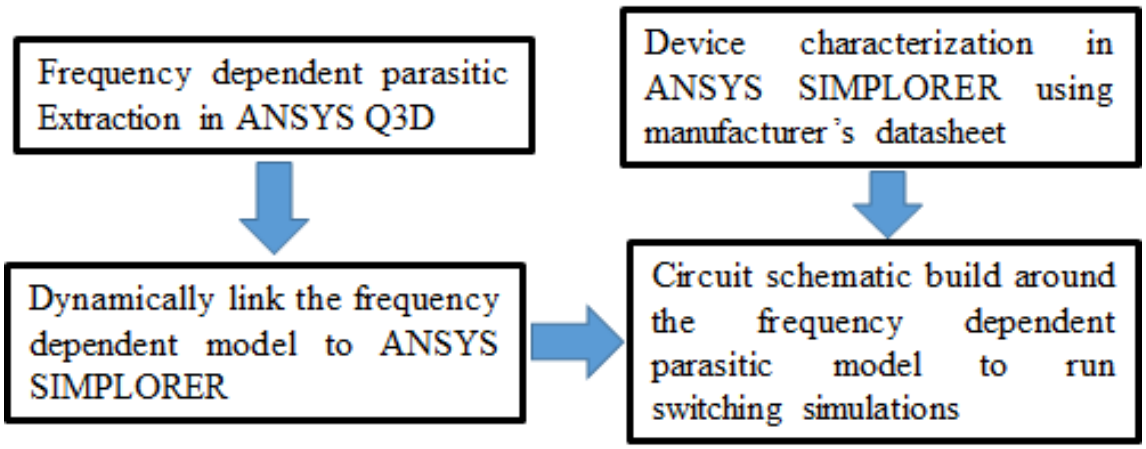

Fig. 4.8 Simulation process flow to simulate the switching behavior of the power module

4.8 Device Characterization

The device characterization for the switching simulations is performed using ANSYS SIMPLORER's inbuilt device characterization tool. In ANSYS SIMPLORER, Si-IGBT device from ABB (Part no. 5SMX12E1280) and SiC Schottky barrier diodes from Wolfspeed (Part no. CPW4-1200-S020B) are characterized using manufacturer's datasheet in order to use these devices to build the switching circuit around the frequency dependent parasitic model, dynamically coupled from ANSYS Q3D, to perform switching simulations. The dynamic measurement characteristics and the nominal operating conditions from the manufacturer's datasheet are given as inputs to perform device characterization in ANSYS SIMPLORER.

In order to characterize the Si-IGBT devices, measurement conditions for the dynamic characteristics are first specified according to the manufacturer's datasheet. According to the Si-IGBT (ABB, Part no. 5SMX12E1280) datasheet, all measurement characteristics values are performed in accordance with the IEC 60747-9 standard. The total turn-on time (t_{on}) is the summation of turn-on delay ($t_{d(on)}$) and the rise time (t_r). The turn-on (t_{on}) time is defined as the time between the gate voltage (V_{GE}) has raised to 10 % of its final value and the collector current

(I_C) has raised 90% of its final value. The total turn-off time (t_{off}) is the summation of the turn-off time delay ($t_{d(off)}$) and the fall time (t_f). The turn-off (t_{off}) time is defined as the time between the gate voltage (V_{GE}) has dropped to 90% of its initial value and the collector current (I_C) has dropped to 10% of its initial value. The turn-on energy (E_{on}) is defined as the time between the gate voltage (V_{GE}) has raised to 10% of its final value and the collector-emitter voltage (V_{CE}) has dropped to 1% of its initial value. Similarly, the turn-off energy (E_{off}) is defined as the time between the gate voltage (V_{GE}) has dropped to 90% of its initial value and the collector current (I_C) has dropped to 1% of its initial value. The measurement conditions are listed in Table 4.1.

The nominal operating point conditions are also provided as inputs for the device characterization. According to the Si-IGBT datasheet, the nominal operating point voltage and current are 600 V and 25 A, respectively. The turn-on and turn-off gate-emitter drive voltage are 15 V and -15 V, respectively. According to the datasheet, the input and reverse transfer capacitance, for the Si-IGBT are 1.9×10^{-9} F and 8×10^{-11} F respectively. The nominal operating point conditions are listed in Table 4.2.

Table 4.1 Switching Energy Measurement Conditions

Start Time		End Time	
$t_{(on)}$	10% rising V_{GE} (0 to V_{GE_max})	$t_{(on)}$	90% rising I_C
$t_{(off)}$	90% falling V_{GE} (V_{GE_max} to 0)	t_{off}	10% falling I_C
E_{on}	10% rising V_{GE} (0 to V_{GE_max})	E_{on}	10% falling V_{CE}
E_{off}	90% falling V_{GE} (V_{GE_max} to 0)	E_{off}	1% falling I_C

Table 4.2 Nominal Working Point Values (Si-IGBT)

Parameter	Description	Value
V_{CE} nom	Nominal Collector-Emitter Blocking Voltage	600 V
I_C nom	Nominal Collector Current	25 A
T_j nom	Nominal Reference Temperature	25 °C
V_{gap}	Band Gap Voltage	1.11 V
R_{ds}	Collector-Emitter On-State Resistance	60 mΩ
V_{GE} on	On-Switch Gate-Emitter Drive Voltage	15 V
V_{GE} off	Off-Switch Gate-Emitter Drive Voltage	-15 V
C_{in}	Input Capacitance	1.9×10^{-9} F
C_r	Feedback (Miller) Capacitance	8×10^{-11} F

In order to perform the device characterization, several data points are obtained from the manufacturer's datasheet using the built-in sheet scan capability in SIMPLORER. Subsequently, these data points are fitted in SIMPLORER to perform the devices characterization. Fig. 4.9 shows the fitted transfer characteristic of the IGBT at two different temperatures, 25 °C and 150 °C, at an operating condition of V_{CE}=20 V. As can be seen, the SIMPLORER fitted data match the data points from the data sheet very well.

Fig. 4.10 shows the fitted on-state characteristic of the Si-IGBT at 25°C and 150°C for gate-emitter voltages, V_{GE}= 20 V.

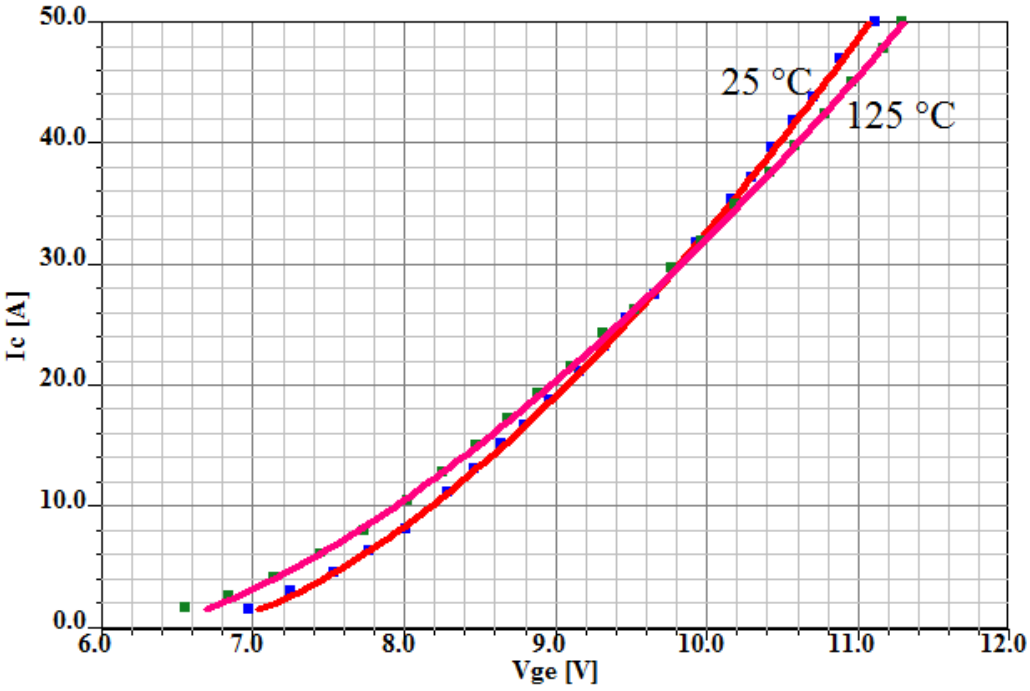

Fig. 4.9. Transfer characteristics of Si-IGBT fitted in ANSYS SIMPLORER

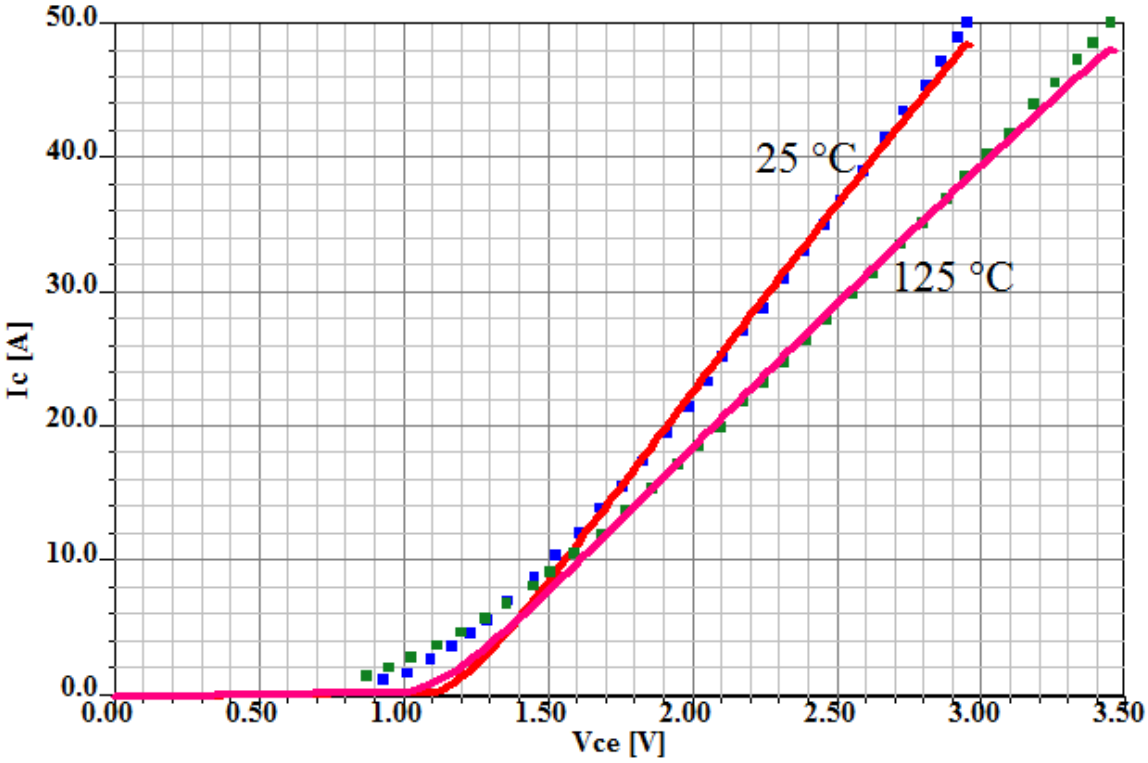

Fig. 4.10. Output characteristics of Si-IGBT fitted in ANSYS SIMPLORER

The turn-on and turn-off energies and switching times are fitted against the nominal working point values listed in Table 4.3. Table 4.3 shows the switching energies and times from the data sheet and the fitted values against the nominal working points in SIMPLORER for two different temperatures, i.e. 25 °C and 150 °C. The fitted values are very similar to those from the data sheet.

Table 4.3 Switching Energy and Time

Parameter	From Data Sheet		Fitted Value in SIMPLORER	
	25 °C	150 °C	25 °C	150 °C
E_{on}	2.5 mJ	3.8 mJ	2.506 mJ	3.802 mJ
E_{off}	1.5 mJ	2.5 mJ	1.499 mJ	2.489 mJ
T_{on}	205 ns	205 ns	239 ns	204.4 ns
T_{off}	475 ns	535 ns	476 ns	536.2 ns

Table 4.4 lists the nominal working point data for the SiC Schottky barrier diode that are given as inputs to SIMPLORER. Fig. 4.11 shows the fitted forward characteristics and Fig. 4.12 shows the junction capacitance characteristics for the Schottky barrier diode used in the module. The forward characteristics of the diode are fitted for two different temperatures at 25 °C and 175 °C. A nominal point fitting is performed for the diode characteristics with a goal setting of reverse recovery charge of Q_{rr} = 0.13 µC. The extracted reserve recovery charge from SIMPLORER is Q_{rr} = 0.1301 µC, which is very similar to the manufacturer's datasheet values.

Table 4.4: Nominal Working Point Values (SiC Schottky Barrier Diode)

Parameter	Description	Value
V nom	Nominal Blocking Voltage	1200 V
I nom	Nominal Current	20 A
T_j nom	Nominal Reference Temperature	25 °C
DI nom	Nominal Current Slope di/dt	2e8 A/s
V_{gap}	Band Gap Voltage	3.2 V

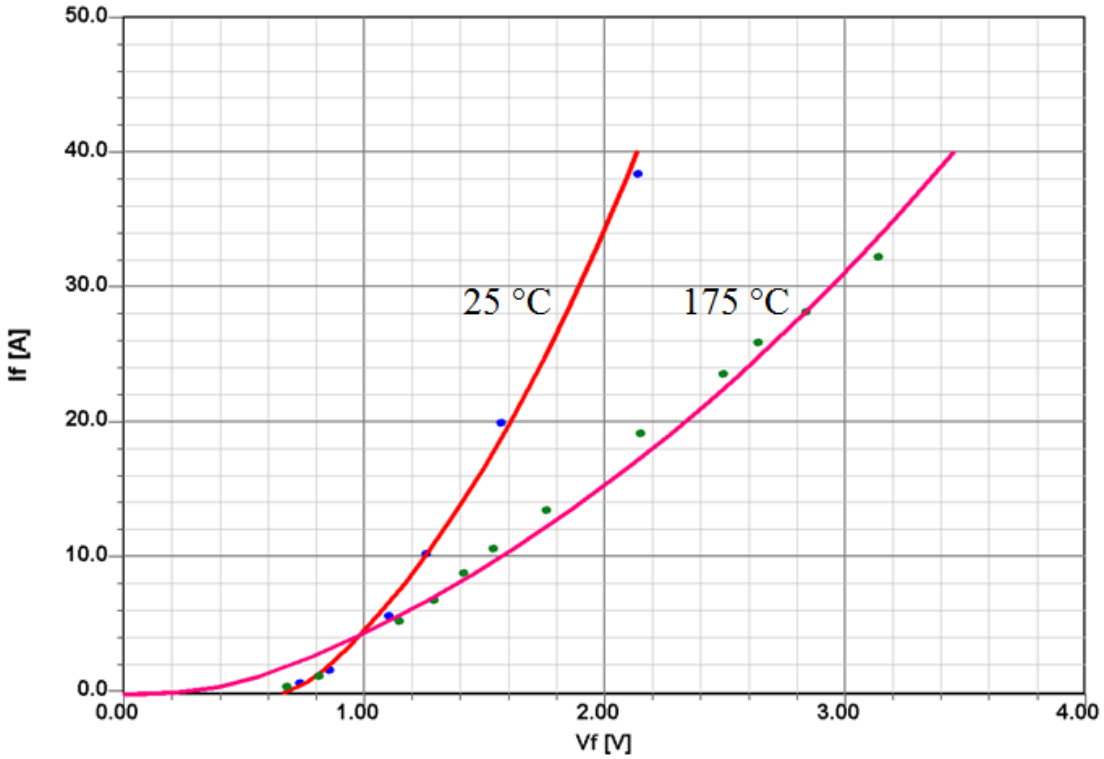

Fig. 4.11. Forward characteristics of SiC Schottky barrier diode fitted in ANSYS SIMPLORER

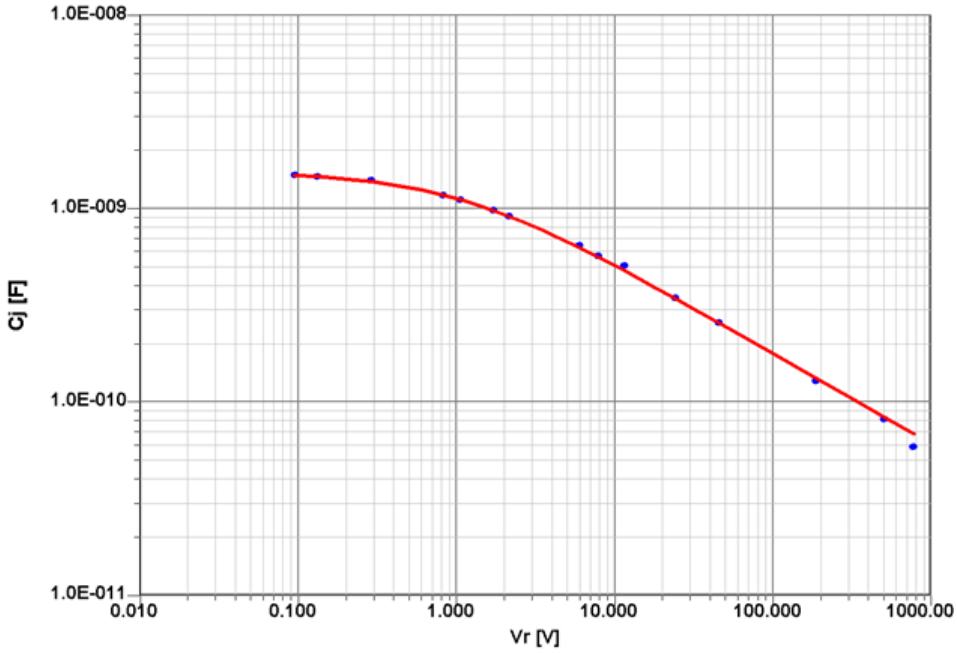

Fig. 4.12. Junction capacitance of SiC Schottky barrier diode fitted in ANSYS SIMPLORER

4.9 Dynamic Coupling of Parasitic Model to ANSYS SIMPLORER

In order to perform the switching simulations in ANSYS SIMPLORER, the frequency dependent parasitic model from ANSYS Q3D is dynamically coupled to ANSYS SIMPLORER using sub-circuit state-space model [7]-[9]. The dynamic coupling results in a parasitic RLC circuit model with several pins representing various nodes/terminals of the module layout. The device models, power supplies, loads are connected at these pins and the simulations are performed. Fig. 4.13 and Fig. 4.14 represent the frequency dependent parasitic model that is dynamically coupled to ANSYS SIMPLORER from ANSYS Q3D [7]-[9]. As can be seen from Fig. 4.13 and Fig. 4.14, the pins correspond to various nodes of the layout of the wire bonded and wire bondless 3-D stack, respectively.

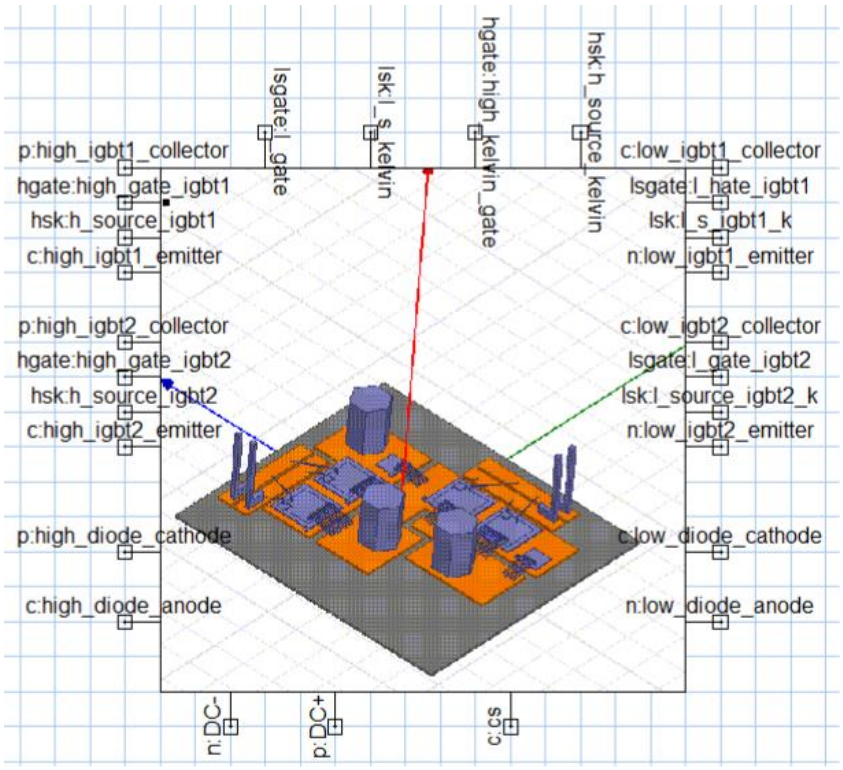

Fig. 4.13. Frequency dependent parasitic model for wire bonded half-bridge power module

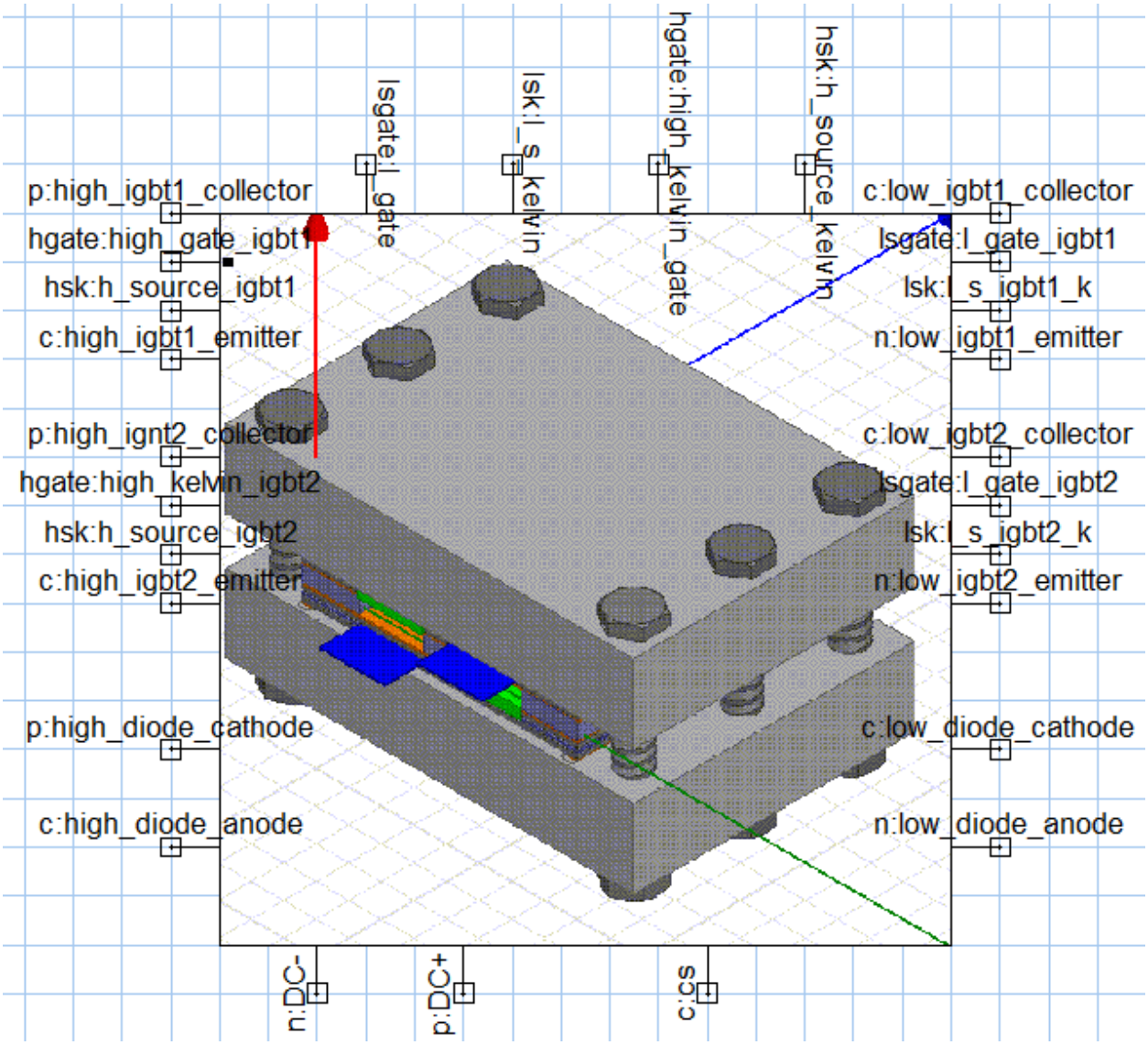

Fig. 4.14. Frequency dependent parasitic model for the 3-D half-bridge stack

Fig. 4.15 and Fig. 4.16 represent the switching circuit built around the frequency dependent parasitic model for wire bonded and wire bondless 3-D stack, respectively. For the switching simulation, a clamped inductive load switching circuit is built around the frequency dependent parasitic model.

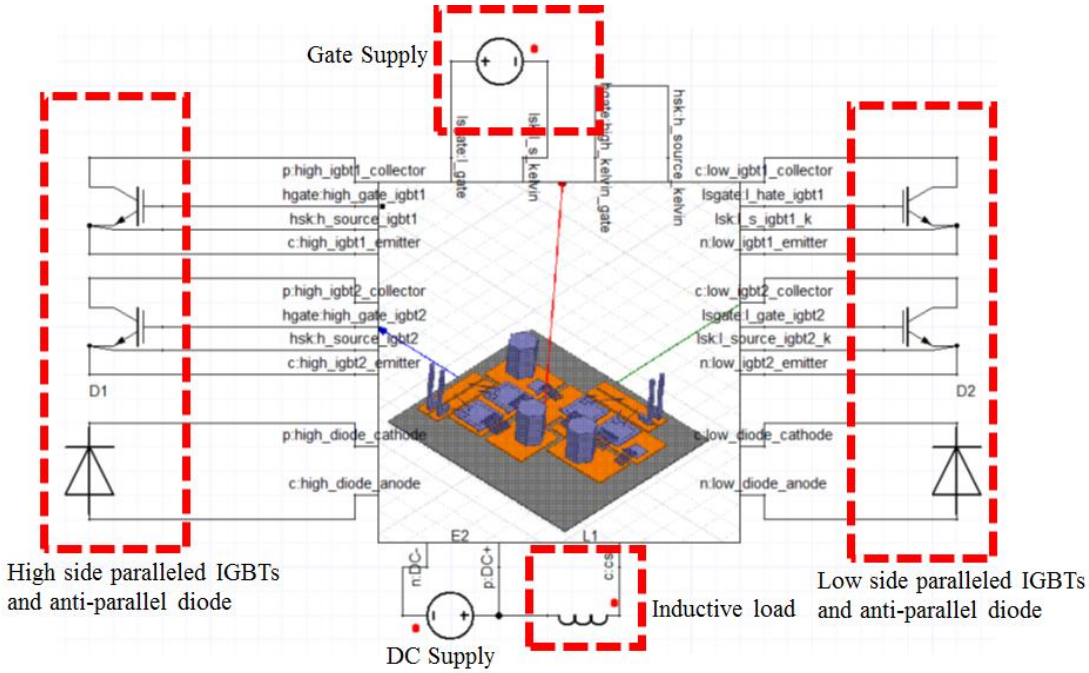

Fig. 4.15. Switching circuit of the wire bonded module build around the parasitic model

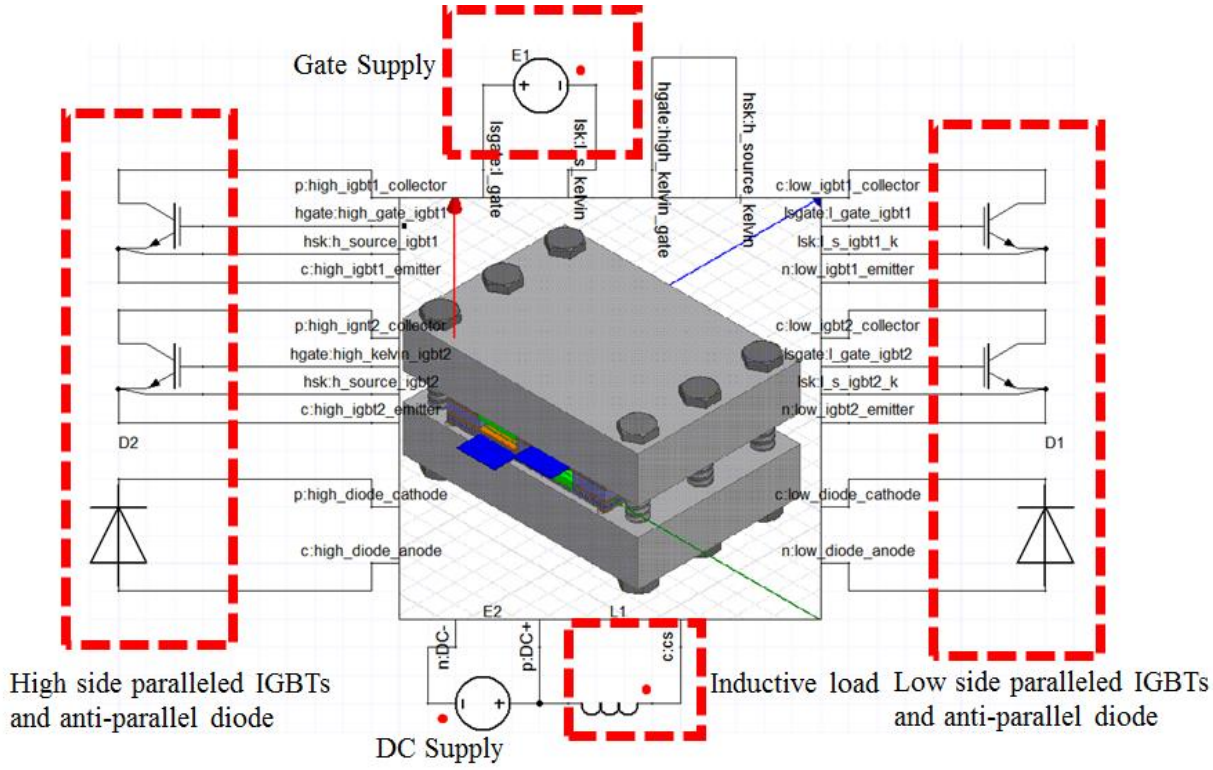

Fig. 4.16. Switching circuit of 3-D stack built around the parasitic model

4.10 Switching results

The input bus voltage is set at 600 V for all simulations. A gate voltage of -5/+15 V is applied to the gates of the Si-IGBTs. Clamped inductive switching simulation is performed to investigate the switching characteristics of both the wire bondless 3-D stack and the wire-bonded power modules. Fig. 4.17 (a) shows the turn-on characteristics of the 3-D stack and the wire-bonded power modules. As can be seen, the turn-on gate voltage for the wire bonded module has a voltage overshoot. The peak voltage is 22 V along with parasitic ringing. The gate voltage waveform for the wire bondless 3-D stack shows no significant overshoot and ringing at turn-on. The voltage and current waveforms of the wire bondless 3-D stack at turn-on, as can be seen from Fig. 4.17 (a), shows a significant reduction in ringing compared to those of the wire bonded module. Also, the current sharing between the two paralleled Si-IGBT devices is uniform for the

wire bondless 3-D stack. The current sharing imbalance between the paralleled devices is 3 A for the wire bonded module with considerably large settling time for the parasitic ringing. The settling time for the turn-on voltage for the wire bonded and the wire bondless 3-D stack is 16 ns and 10 ns respectively. Moreover, the settling time for the current ringing at turn-on for the wire-bonded and the wire-bondless 3-D stack is 532 ns and 68 ns, respectively. From Fig. 4.17 (b), it can be observed that the voltage overshoot of the wire bonded module is higher compared to that of the wire bondless 3-D stack. Also, no significant turn-off current ringing is observed for the wire bondless 3-D stack. The settling time for the turn-off current ringing for the wire bonded module is 484 ns which are considerably higher than that of the wire bondless 3-D stack.

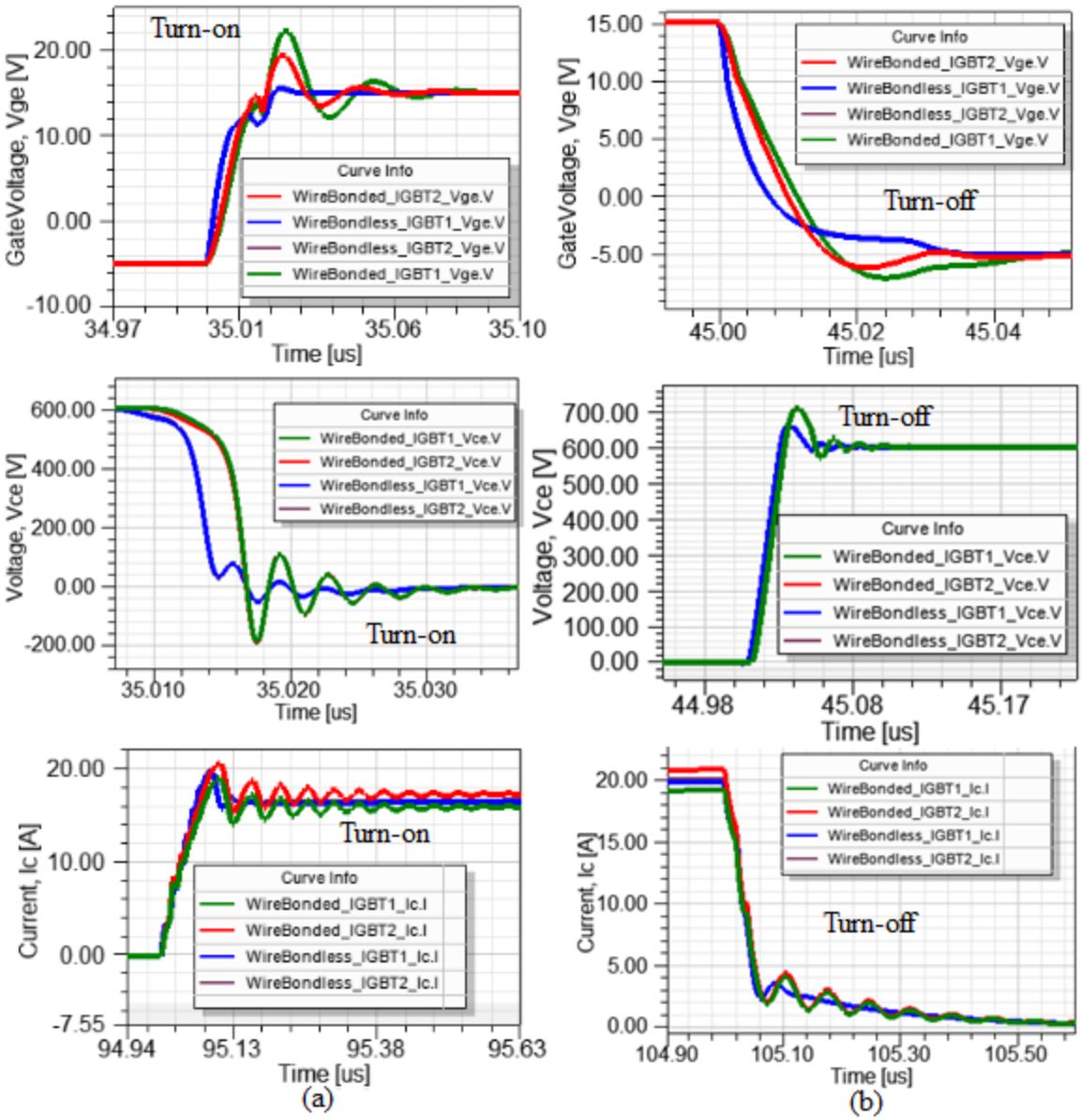

Fig. 4.17. Simulated waveforms of the 3-D stack power module compared to the wire bonded power module

4.11 Summary

In this chapter, a wire bonded half-bridge power module is designed and its frequency dependent parasitic inductances are extracted using ANSYS Q3D. The parasitic inductance of the wire bondless 3-D stack and the wire bonded module are compared. It is seen that the wire bondless

3-D stack exhibits significantly low parasitic inductance compared to the wire bonded half-bridge module. The frequency dependent parasitic inductance for all critical nets comparing the two modules are presented. Subsequently, a systematic co-simulation technique using ANSYS EM tools is presented to perform switching analysis of the two power modules. Clamped inductive switching is performed in order to investigate the performance improvement in switching behavior of the wire bondless 3-D stack compared to that of the wire bonded half-bridge power module. Significant performance improvement such as reduction of turn-on/turn-off voltage and current ringing, overshoot, the shorter parasitic ringing settling time is observed for the wire bondless 3-D stack.

4.12 References

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Chapter 5 Fabrication of the Wire Bondless 3-D Half-Bridge Power Module

In this chapter, the detailed fabrication process for the proposed 3-D stack will be discussed. The fabrication of the half-bridge 3-D stacked power module require several fabrication steps to be followed. As part of the dissertation work, an extensive process development and optimization is carried out to establish a reliable, time efficient and cost effective fabrication process to fabricate the proposed 3-D stacked module. The process flow, thus developed as part of this dissertation research, can act as a baseline that can be followed and implemented to investigate, fabricated and further develop newer 3-D power module structures.

The process development for the half-bridge 3-D stacked power module is performed using 1200 V 25 A silicon IGBT devices from ABB (Part no. 5SMX12E1280) and 1200 V 20 A silicon carbide Schottky barrier diodes (Part no. CPW4-1200-S020B) from Wolfspeed. The half-bridge stack consists of a high side and a low side switching position with each switching position having two silicon IGBT devices in parallel with two Schottky barrier diodes in an antiparallel configuration. In the proposed approach, two stand-alone wire bondless power modules, each consisting of a switching position, are stacked on top of each other with help of a low-temperature co-fired ceramic (LTCC) based spring loaded interposer along with clamped interconnections to connect the high side and the low side stand-alone modules in series to form the half-bridge 3-D stack. As discussed earlier, the 3-D stack consists of several individual components, which are fabricated separately and subsequently assembled together to form the wire bondless 3-D half-bridge stacked power module.

5.1 Fabrication of Stand Alone Wire Bondless Power Module

The stand-alone wire bondless power modules of the proposed 3-D stack consist of a top and a bottom side direct bond copper (DBC) substrate separated by an LTCC interposer. The LTCC interposer also acts as a power device carrier. The main processing steps for the wire bondless power module are as follows:

I. Die top surface preparation
II. Top and bottom direct bond copper (DBC) preparation
III. Low temperature co-fired ceramic (device career) preparation
IV. Application of sealing material

In the subsequent sections, the detailed processing steps to fabricate the 3-D wire bondless half-bridge power module are presented.

5.2 Die Top Surface Preparation

The top surface metallization for commercially available SiC MOSFET (gate and source) /diodes (anode) and Si-IGBT (gate and emitter) /diodes (anode) are generally aluminum (Al) which is more compatible with wire bonds. In the proposed 3-D wire bondless half-bridge power module, flip-chip die attachment method is adopted to attach the power semiconductor devices. As such, in order to use these power devices in the proposed 3-D wire bondless power module and facilitate direct solder attachment to the top and bottom conductors, the top die surface must consist appropriate material system compatible with top surface attachment method. Two possible processes to prepare the top die surface are undertaken. In the first approach, a nano-silver paste is sintered onto the gate and the emitter electrodes of the bare die with the help of a silver based conductive epoxy (EPO-TEK® H20E) as a buffer layer. A Kapton mask is used to

screen print a layer of silver based electrically conductive epoxy (EPO-TEK® H20E) on top of the aluminum surface of the die. After the epoxy is cured, a layer of nano-silver paste (NBE's nanoTach) was screen printed using a Kapton mask on top of the epoxy followed by silver sintering. The complexity of this process is high since the process needed to be carried out on small individual bare dies. Also, it is observed that the process yielded uneven finished surface making it a non-viable option for flip-chip die attach process. Also, the electrical and thermal conductivity of the conductive silver based epoxy is lower compared to the evaporated metallization. As such, the epoxy based buffer layer provides added thermal resistance and might be concern from a reliability standpoint. As such, this approach is not pursued in this research.

In the second approach, a material system of titanium (Ti)/ nickel (Ni)/ silver (Ag) is evaporated on the die top surface using an e-beam evaporator.

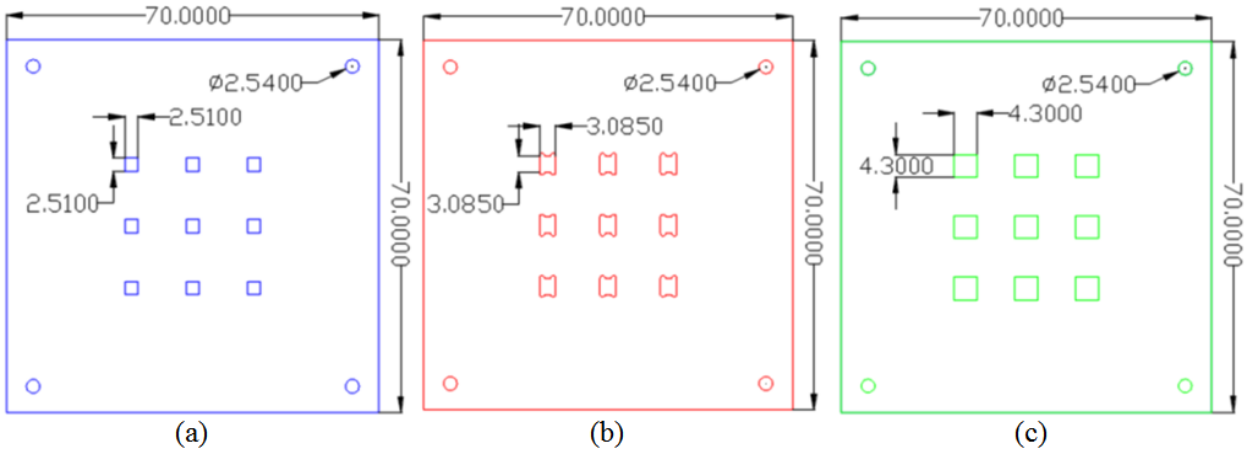

Fig. 5.1. AutoCAD design (a) Kapton mask, (b) bottom Aluminum fixture, (c) top Aluminum fixture for E-beam evaporation on SiC diode

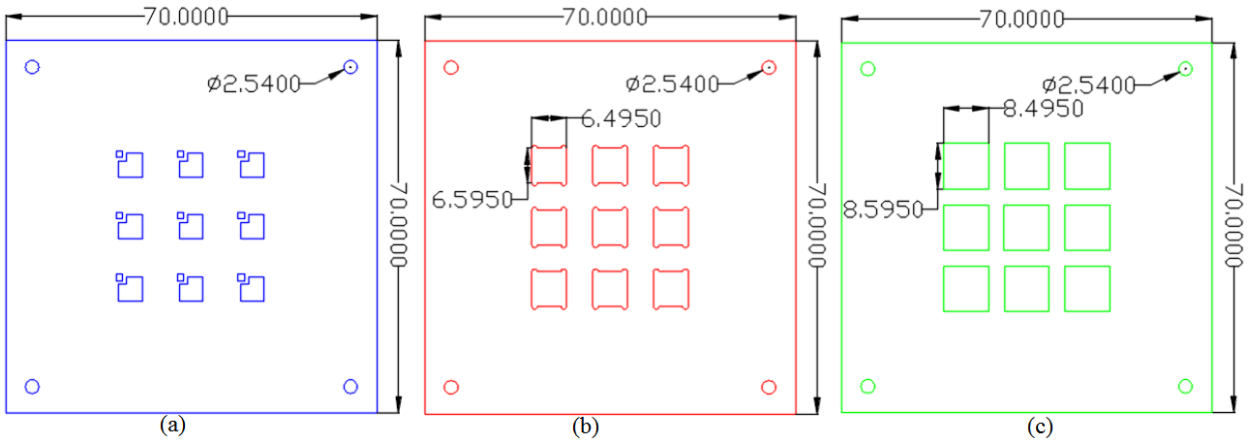

Fig. 5.2 AutoCAD design (a) Kapton mask, (b) aluminum bottom frame, (c) aluminum top frame for E-beam evaporation on Si-IGBT

Thin film deposition of Ti/Ni/Ag metallization stack is performed on individual Si-IGBT and SiC Schottky barrier diodes to facilitate top surface attachment. In order to hold the individual devices in place, an aluminum (Al) fixture is designed using the AutoCAD. The aluminum fixture consists of a top and a bottom holding frame. A Kapton mask is also designed in order to protect the surfaces where thin film metallization is not required to prevent shorting between the gate and emitter electrodes of the Si-IGBT devices. Fig. 5.1 and Fig. 5.2 show the AutoCAD designs for the Kapton mask, and the top and bottom aluminum fixtures designed for evaporation. The Kapton mask is punched using a punching machine (MP-4150 SL) with a 20 mils mechanical punch. The top and bottom aluminum fixtures are machined using a CNC milling machine (Model 3501). Fig. 5.3 and Fig. 5.4 show the punched Kapton and the fabricated aluminum fixture. The cavity depth is machined to be as close as possible to the thickness of the power devices, i.e., 140±20 µm and 377±20 µm for Si-IGBT and SiC diode, respectively. In order to prepare the devices for evaporation, the devices are placed inside the cavity on the bottom aluminum fixture. Subsequently, the Kapton mask and the top aluminum fixture are

placed on top of these devices. The alignment of the entire assembly is performed under the microscope and achieved using four corner screws with 4-40 thread diameter. The alignment of the IGBT devices with the Kapton mask is highly critical due to the very narrow isolation gap between the gate and emitter electrodes. In order to avoid any shorting between the gate and emitter electrodes, the opening of the emitter region on the Kapton mask is designed to be 20% smaller than the emitter region of the IGBT device. Fig. 5.5 shows the evaporation assembly for the Si-IGBT devices.

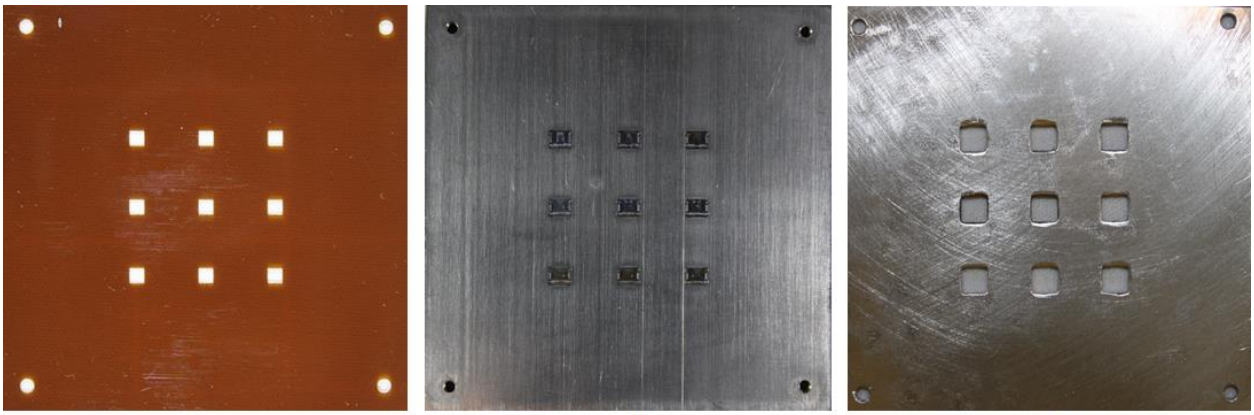

Fig. 5.3. (a) Kapton mask, (b) bottom Aluminum fixture with cavity, (c) top Aluminum fixture with device cutouts for thin film deposition on Anode of SiC Schottky barrier diodes

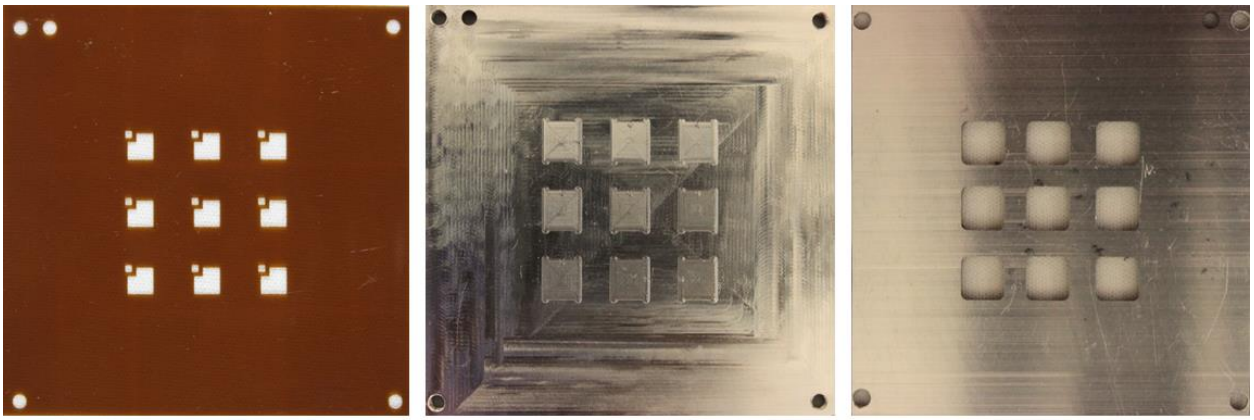

Fig. 5.4. Kapton mask, (b) bottom Aluminum fixture with cavity, (c) top Aluminum fixture with device cutouts for thin film deposition on gate and emitter of Si-IGBT devices

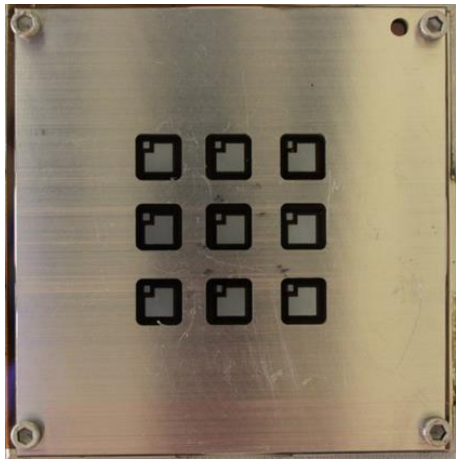

Fig. 5.5. Assembly used for Ti/Ni/Ag E-beam evaporation on gate and emitter of Si-IGBT devices

The process parameters for E-beam evaporation are very critical in order to achieve good adhesion to the aluminum top surface metallization of the power devices. The bottom metallization for the Si/SiC power devices is Ti/Ni/Ag. In order to maintain material compatibility between the top and bottom metallization, a Ti/Ni/Ag material system is chosen for the top surface. Also, having the same material system for the bottom and top metallization

reduces the coefficient of thermal expansion (CTE) mismatch between the top and bottom metallization for the flip-chip die attachment. Titanium (Ti) is used as an

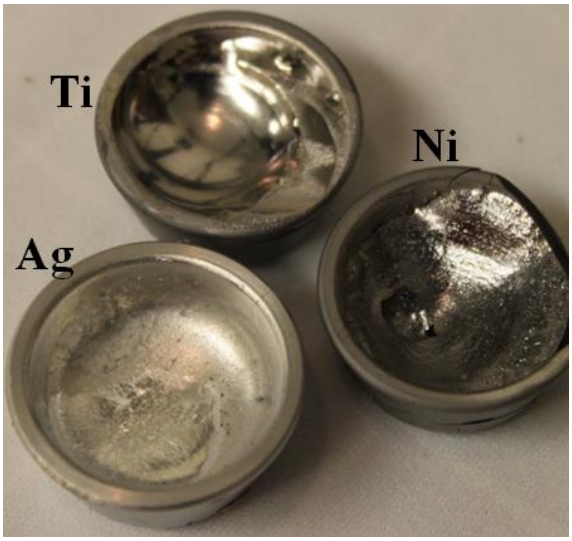

Fig. 5.6. Glass coated graphite and Molybdenum (Mo) crucibles used for Ti/Ni/Ag deposition

adhesion layer for the top aluminum surface. The material crucibles are first indexed inside the E-beam evaporator and the devices inside the aluminum fixture along with the Kapton mask as shown in Fig. 5.5 is placed upside down on the sample holding base with help of a Kapton tape. Glass coated graphite crucibles are used for the Ti and Ni evaporation and molybdenum crucible is used for Ag evaporation. For material deposition, the crucibles are first warmed up for 3 minutes by passing a current through the crucible. These currents used are 0.012 A, 0.01 A and 0.008 A for Ti, Ni and Ag respectively. After warming up the crucibles for 3 minutes, the current is gradually increased until a deposition rate of approximately 1 Å/s is achieved. It has been observed that the deposition rate of titanium has a very critical impact on the adhesion of the evaporated layers. Lower deposition rate (< 1 Å/s) for Titanium resulted in a better overall adhesion of the evaporated material system. The desired thickness for the Ti adhesion is 100 nm.

The deposition thicknesses for both Ni and Ag are 1 μm. The process parameters used for Ti/Ni/Ag evaporation is listed in Table 5.1. During the evaporation of Ni, it is observed that if the e-beam is too focused on the crucible it is difficult to melt all the Ni pallets uniformly. Moreover, if the beam is too focused it penetrates and cracks the crucible through the bottom. In order to resolve the issue, a higher frequency beam with higher lateral and longitudinal beam width is used to cover the crucible entirely to warm up and melt the Ni pallets uniformly to evaporate Ni. Fig. 5.6 shows the glass coated graphite and molybdenum crucibles used for the Ti/Ni/Ag metal deposition. Fig. 5.7 shows the silicon IGBT device with Ti/Ni/Ag evaporation on the gate and emitter electrodes.

Table 5.1. Process Parameters Used For Ti/Ni/Ag Evaporation

Material	Desired Thickness (μm)	Turbo Current (A)	Base Pressure (mbar)	Warmup Current (A)	Deposition Current (A)	Deposition Rate (Å/s)
Titanium (Ti)	0.1	0.30	4×10^{-7}	0.012	.0113	0.8
Nickel (Ni)	1	0.30	3×10^{-7}	0.01	0.131	2.8
Silver (Ag)	1	0.30	5.4×10^{-7}	0.008	0.199	2.8

Fig. 5.7. Silicon IGBT device with Ti/Ni/Ag evaporated on the gate and emitter electrodes

In order to examine the adhesion strength of the deposited metals on the aluminum surface, an initial tape test is performed. A Kapton tape is used to perform the adhesion test. Following the process parameters listed in Table 5.1, all the nine Si-IGBT devices as shown in Fig. 5.5 passed the initial tape test. However, the adhesion test failed for samples evaporated with a higher deposition rate (>1.5 Å/s) for the titanium layer. In order to further examine the adhesion strength of the deposited metal layers, die shear test is performed using a DAGE 4000 series die shear tool. Dummy devices are prepared to carry out the die shear test. Evaporation of the same material system is performed on a silicon wafer using the same process parameters as shown in Table 5.1. The silicon wafer is subsequently diced to a 2.75mm ×2.75 mm pieces to be used as die shear samples.

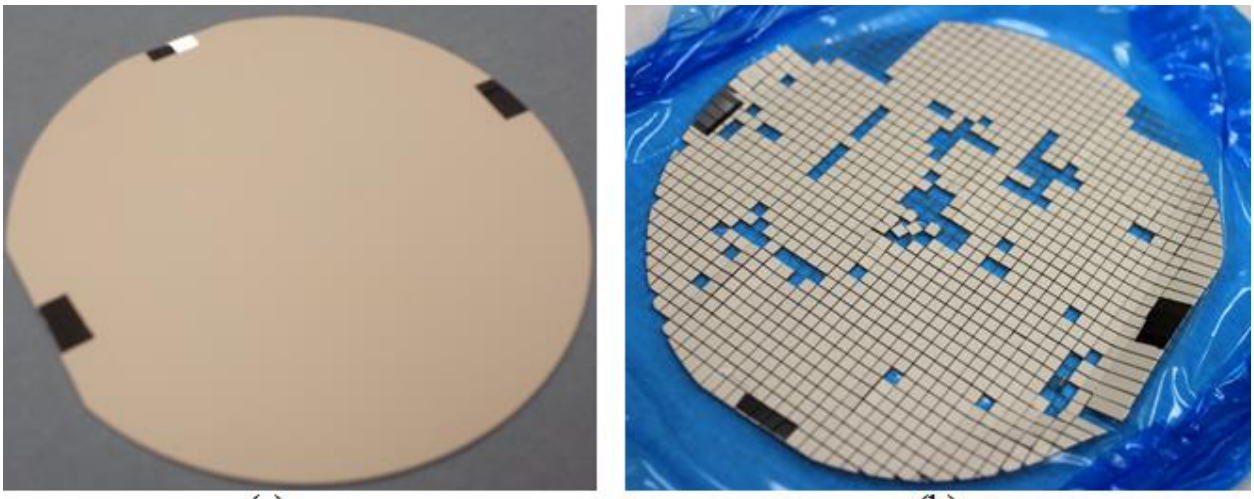

Fig. 5.8. (a) Silicon wafer with Ti/Ni/Ag evaporation to prepare dummy devices for die shear test, (b) diced 2.75 mm ×2.75 mm dummy devices

In order to carry out the die shear strength test, the dummy devices are attached to a nickel plated DBC substrate using SAC 305 solder paste in a Sikama reflow oven. Subsequently, the die shear test is performed using the DAGE 4000 series die shear tester. The die shear height for the test is set at 20 µm above the DBC substrate. Ten samples are prepared and subsequently sheared to measure the bond strength. Fig. 5.9 plots the shear strength in Newton (N) with respect to the die shear distance. Fig. 5.10 plots the die shear strength of the ten samples in MPa. As can be seen from Fig. 5.10, the die shear strength of the ten samples are relatively uniform and vary between 41-50 MPa. As such, it can be concluded that the approach taken to evaporate Ti/Ni/Ag to prepare the top surface of the IGBT and Schottky barrier diodes for flip chip attachment is valid and reliable.

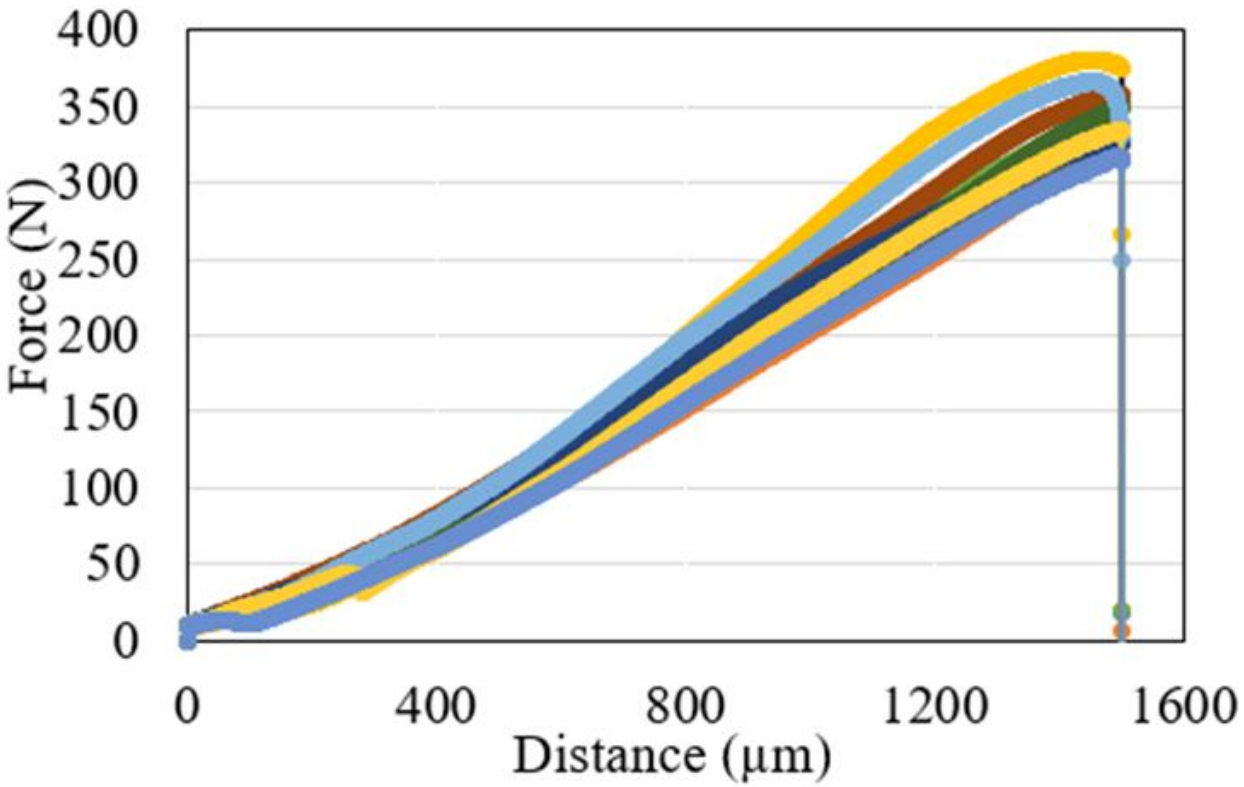

Fig. 5.9. Die shear strength for ten samples

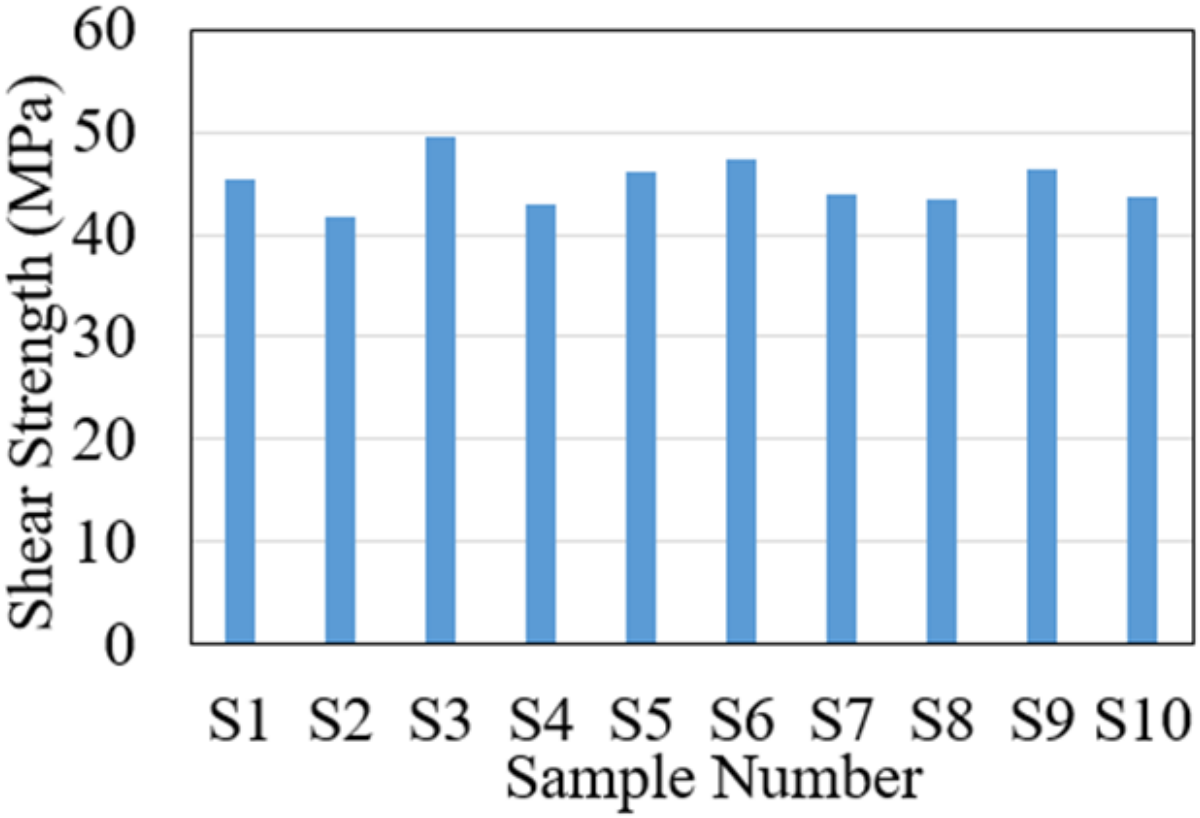

Fig. 5.10. Die shear strength in mega pascle (MPa) for ten samples

5.3 Top and bottom direct bond copper (DBC) preparation

The proposed stand-alone power module of the 3-D stack consists of top and bottom DBC substrates. As discussed earlier, the DBC substrates are used to route the gate, emitter and the collector of the semiconductor devices to the input/output and the Kelvin terminals to facilitate module operation. Aluminum oxide (Al_2O_3) DBC is used for these power modules. The DBC substrate consists of a 25 mil Al_2O_3 layer sandwiched in between two 12 mil copper layers on either side. The DBCs are patterned using dry film photolithography, and subsequently, diced into the desired dimensions using a dicing saw. The main process steps to pattern the DBC substrate is as follows:

i. Step 1: Cleaning the DBC in ultrasonic acetone bath

ii. Step 2: Cleaning the DBC in a10% hydrochloric (HCl) acid bath

iii. Step 3: Nickel (Ni) plating the DBC

iv. Step 4: Perform dry film photolithography to develop the desired pattern on the DBC

v. Step 5: Chemical etching to transfer the desired electrical routing on the DBC and subsequently strip the dry film photoresist

vi. Step 6: Dice the DBC substrates according to the desired dimension

The preparation of the DBC substrates starts from cleaning the 5.5” ×7.5” copper DBC in an acetone ultrasonic bath for 5 minutes. Either side of the DBCs are cleaned, and subsequently, rinsed and dried thoroughly. After the ultrasonic cleaning, a 10% hydrochloric acid (HCl) is used to remove the oxide on the copper plate and clean the DBC. Fig. 5.11 shows the ultrasonic acetone and the 10% HCl cleaning setup used for cleaning the DBC substrates.

Fig. 5.11 (a) Ultrasonic acetone clean of DBC, (b) 10% HCl clean of DBC

After cleaning the DBC, nickel (Ni) plating is performed to prevent oxidization of copper. Also, Ni-plating provides a better surface wetting for the solder. Fig. 5.12 shows the Ni-plating setup

used for plating a 5.5” ×7.5” copper DBC. The copper DBC is placed between the positive and negative electrodes and placed inside the nickel plating bath. A DC power supply (HP 6651A) is used to set the voltage at 7.9 V and current at 2.13 A for the nickel electroplating. The nickel plating is performed for 25 minutes to yield a 2-3 µm of nickel on top the copper on the DBC. Fig. 5.13 (a) and (b) show a DBC before and after nickel plating.

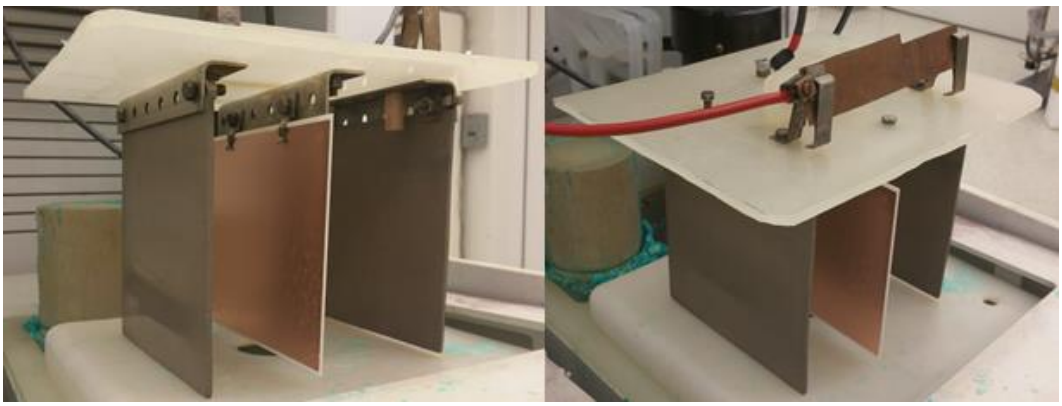

Fig. 5.12. Nickel plating setup

Fig. 5.13. (a) Bare copper DBC substrate, (b) nickel plated DBC substrate

After Ni-plating the DBC, a dry film photoresist process is carried out to pattern the copper on the DBC. In order to apply the photoresist, the DBC is first placed on a hot plate to warm up for a minute. The hot plate temperature is set at 100 °C for this purpose. The warm up of the DBC is required prior to the application of photoresist to prepare the surface for a better adhesion with the photoresist. A negative photoresist is applied on either surface of the DBC substrate using a dry film laminator. Following the application of the photoresist on one side, the DBC is again warmed up following the same procedure for application of the photoresist on the other side. After applying the photoresist on both surfaces of the DBC, it is set aside for 15 minutes to promote better adhesion of the photoresist to the DBC surface. Subsequently, a photomask is placed on top of the photoresist to expose the photoresist under an ultraviolet light for 2 minutes in order to transfer the desired pattern to the photoresist. After transferring the pattern, the DBC is again set aside for 15 minutes for the pattern to develop before developing the photoresist. Fig. 5.14 and Fig. 5.15 show the photomask used to pattern the top and bottom DBC substrates, respectively. The negative photoresist under the transparent portion of the photomask cross-links when exposed to UV light. As such, the transparent portion of the photomask remains on the DBC surface after development. However, the dark portion of the photomask remains unexposed under UV light cannot cross-link. As such, the photoresist from the unexposed part dissolves during development and facilitates chemical etching process to etch the metal away from those portions of the DBC.

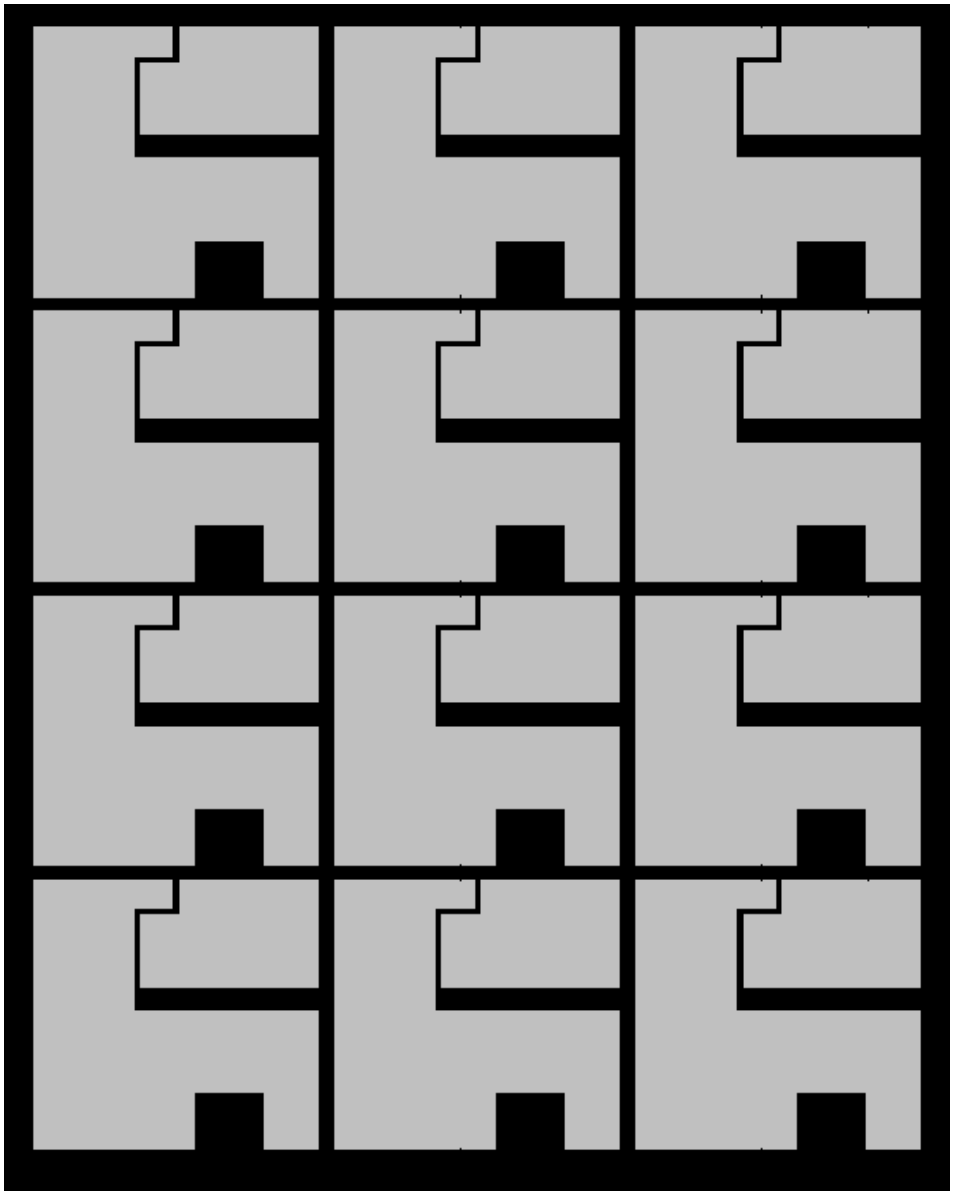

Fig. 5.14. Negative photomask used to pattern the bottom DBC of the stand-alone power module

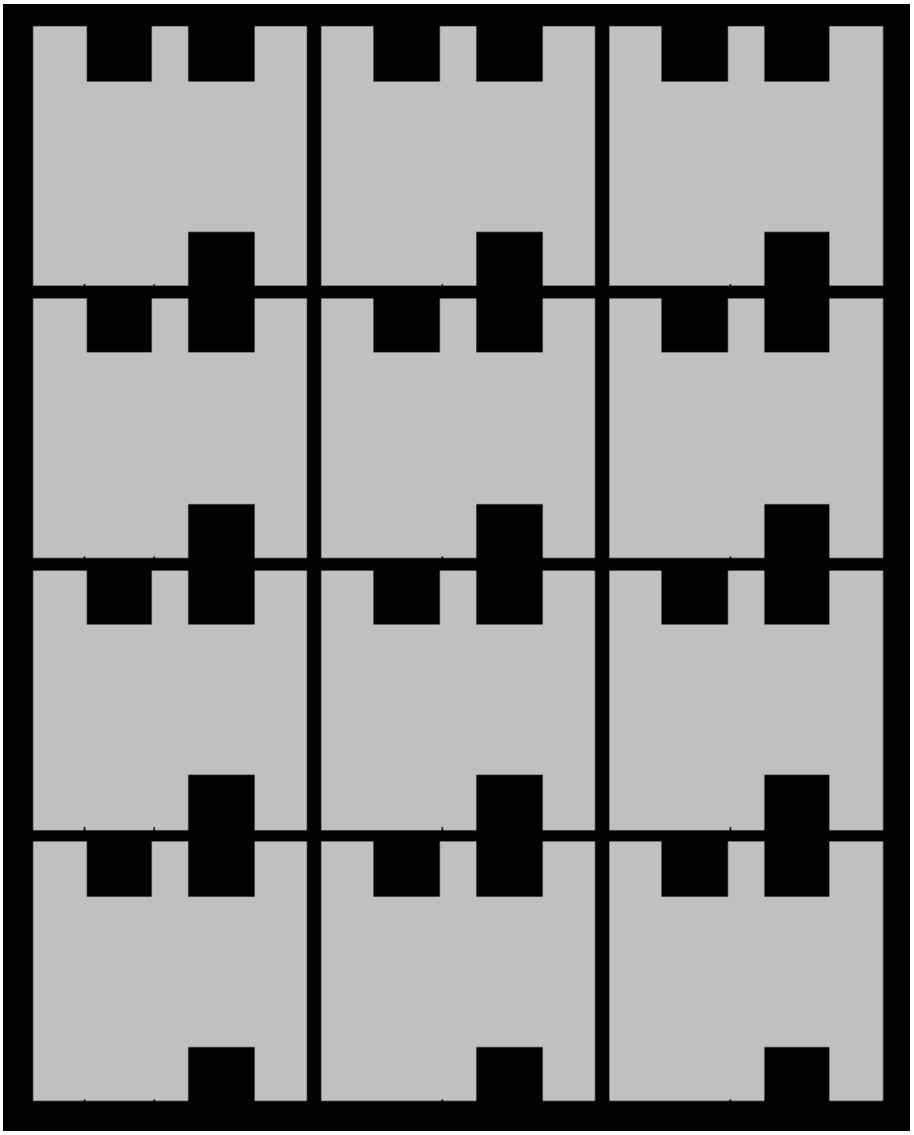

Fig. 5.15. Negative photomask used to pattern the top DBC of the stand-alone power module

After exposing the photoresist under UV light, a sodium carbonate developer solution is used to develop the photoresist. The development process takes about 5 minutes. Before immersing the DBC inside the developer solution the protective Mylar is removed from the top of the photoresist surface to expose the photoresist to the developer solution. After the photoresist is developed, the DBC is rinsed with warm water to remove any dissolved photoresist residues from the DBC surface. Subsequently, a chemical etching process is performed using a ferric

chloride solution in a Chemcut Spray Etcher to etch and pattern the DBC substrate. The ferric chloride etchant temperature is set at 125 °C for the etching process. Fig. 5.16 shows the Chemcut Spray Etcher equipment used for the chemical etching of the copper on DBC substrate. After etching, the remaining photoresist is stripped off using a stripper solution. Fig. 5.17 and Fig. 5.18 shows the dicing saw and the diced top and bottom DBC substrates respectively.

Fig. 5.16. Chemcut spray etcher for chemical etching of DBC

Fig. 5.17. K&S dicing saw used for dicing the DBC substrates

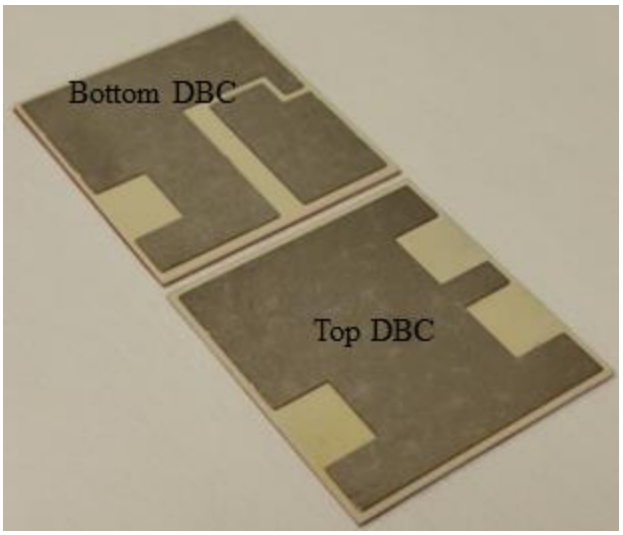

Fig. 5.18. Bottom and top DBC of the stand-alone power module

5.4 Connector attachment

After the top and bottom DBCs are patterned and diced as shown in Fig. 5.18, connector terminals are attached to the DBCs using a solder reflow process. As discussed earlier, gate-emitter Kelvin connectors, emitter/emitter clamp, and collector/collector clamp are used to route the gate, emitter, and collector of the paralleled devices outside to facilitate the module operation. The connectors used for the proposed power modules are custom designed and machined out of a 1 mm thick copper sheet. The reflow process is carried out in a Sikama reflow oven using Pb95Sn5 solder paste. The four step Sikama reflow process is as follows:

i. Ramp to soak temperature
ii. Preheat/soak
iii. Peak reflow temperature
iv. Cooling ramp down

The process starts by ramping up the temperature to the preheat/soak temperature. The assembly then kept in the preheat/soak region for 60-120 seconds before ramping up the temperature to a

peak temperature. The temperature ramp rate used to ramp the temperature to the peak temperature is generally 1-3 °C/s. Generally, the entire assembly is held at the peak temperature for 45-60 seconds for the solder to turn liquid and the reflow occurs. After the reflow of the solder, the entire assembly is cooled down with a ramp rate of 2-4 °C/s.

In order to carry out the connector attachment with solder reflow, a graphite fixture is designed and machined. The graphite fixture consists of a base and a top lid as shown in Fig 5.19 (a). The DBC substrate is placed on the base graphite and subsequently, solder paste is applied on the regions where the connectors are to be attached. After the application of the solder paste, the copper connectors are placed on top of the solder paste and the top graphite lid is placed on the entire assembly. The top graphite lid is secured to the base graphite fixture by six screws as shown in Fig 5.19 (a) to hold the sandwiched assembly securely to prevent the connectors from moving away from its desired place during the reflow process. Fig 5.19 (b) shows the top and bottom DBC substrates after the connectors are attached. Fig. 5.20 shows the reflow profile for Pb95Sn5 solder paste used to perform the connector attachment on the top and bottom DBC substrates.

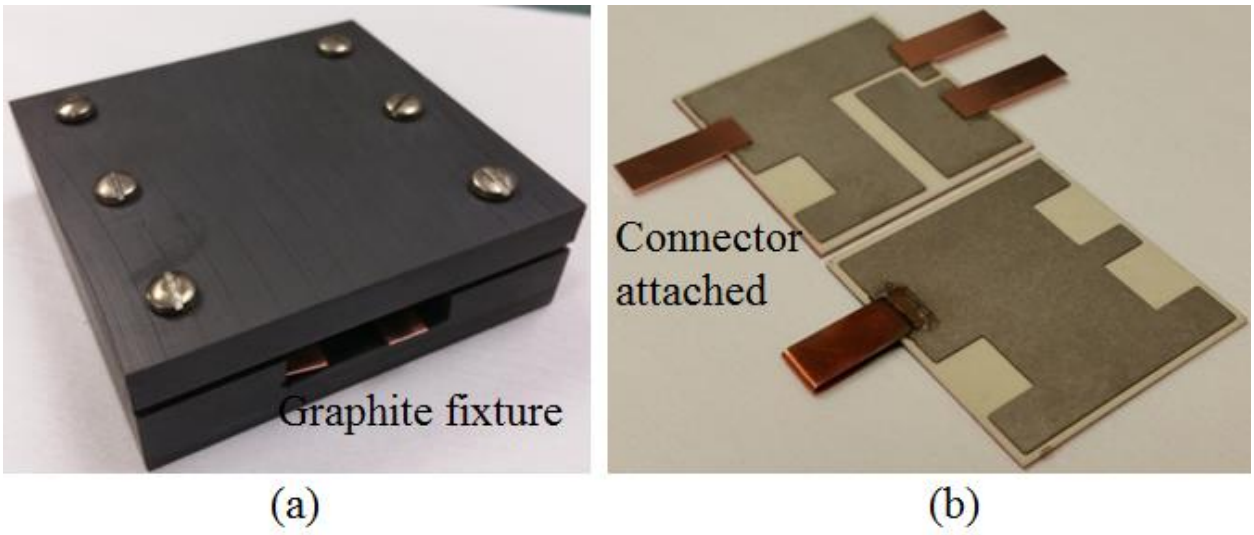

Fig 5.19. Graphite fixture for solder reflow, (b) connectors attached to the DBC

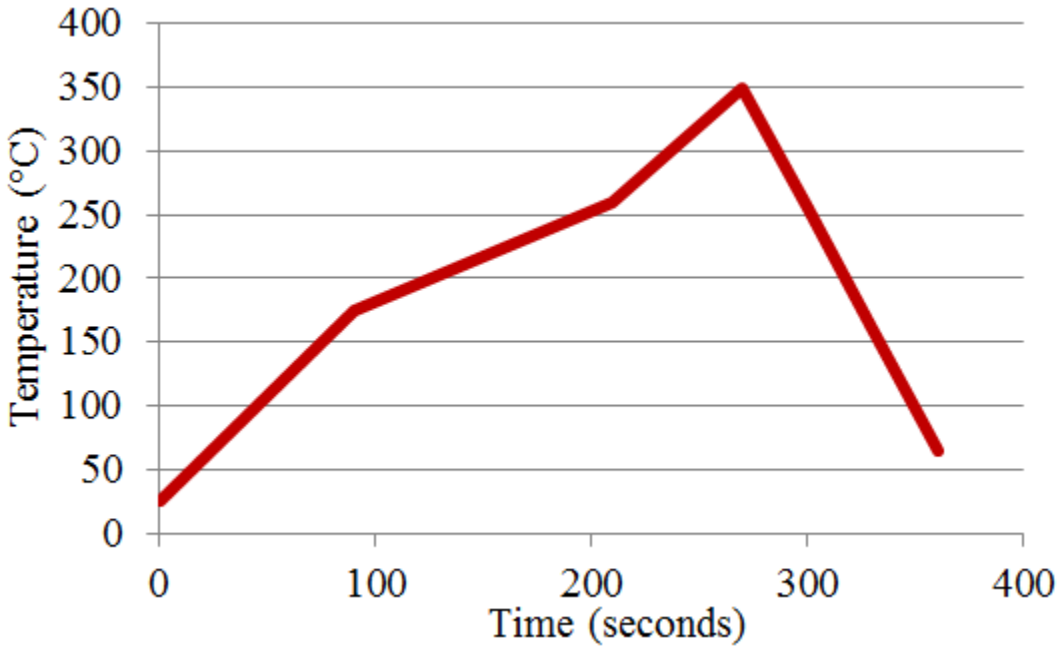

Fig. 5.20. Reflow profile used for connector attachment

5.5 Low temperature co-fired ceramic (LTCC) device carrier preparation

Low temperature co-fired ceramic (LTCC) is used as the semiconductor device carrier in the proposed stand-alone power modules. The multi-layer design freedom offered by the LTCC process flow is utilized to fabricate very low inductance wire bondless stand-alone power modules to be stacked on top of each other using the spring loaded LTCC interposer and clamped interconnections to form a half-bridge power module. There are several steps associated with the fabrication of the LTCC device carrier. The major steps are as follows:

i. Punch profile creation for each layer of LTCC tapes
ii. Precondition the LTCC tape
iii. Creating device cut-outs and interconnection vias on LTCC tape
iv. Metallization on LTCC using screen printing
v. Lamination of the identical LTCC layers
vi. Lamination of different LTCC layers
vii. Firing the laminated LTCC

5.6 LTCC punch profile creation

In order to create the LTCC punch profile, the LTCC die carrier design is imported to AutoCAD from ANSYS Q3D. The transfer of the design is performed by exporting the ANSYS Q3D design as .sat file format. The .sat file is a standard ACIS text file containing all the information of the 3-D geometry. The .sat file is imported to AutoCAD environment using import command in AutoCAD. Each layer of the multi-layer 3-D LTCC die carrier is imported to AutoCAD. The LTCC die carrier as discussed in Chapter 2 consists of four different layers. The fabrication of the four different layers is performed separately. Subsequently, the four layers are laminated

together to form the LTCC die career. Fig. 5.21 corresponds to the four different LTCC layers imported to AutoCAD. Fig. 5.22 shows the LTCC die carrier design in AutoCAD with each separate layer overlaid on top of each other. After importing the multi-layer design, a punch profile is created in AutoCAD to punch the LTCC tapes to fabricate each individual layer. Fig. 5.23 shows the punch profile for all the four layers of the LTCC. The alignment marks for all the layers are performed when designing the punch profile to align the different layers of LTCC when lamination of the identical or different layers is performed later in the LTCC process flow.

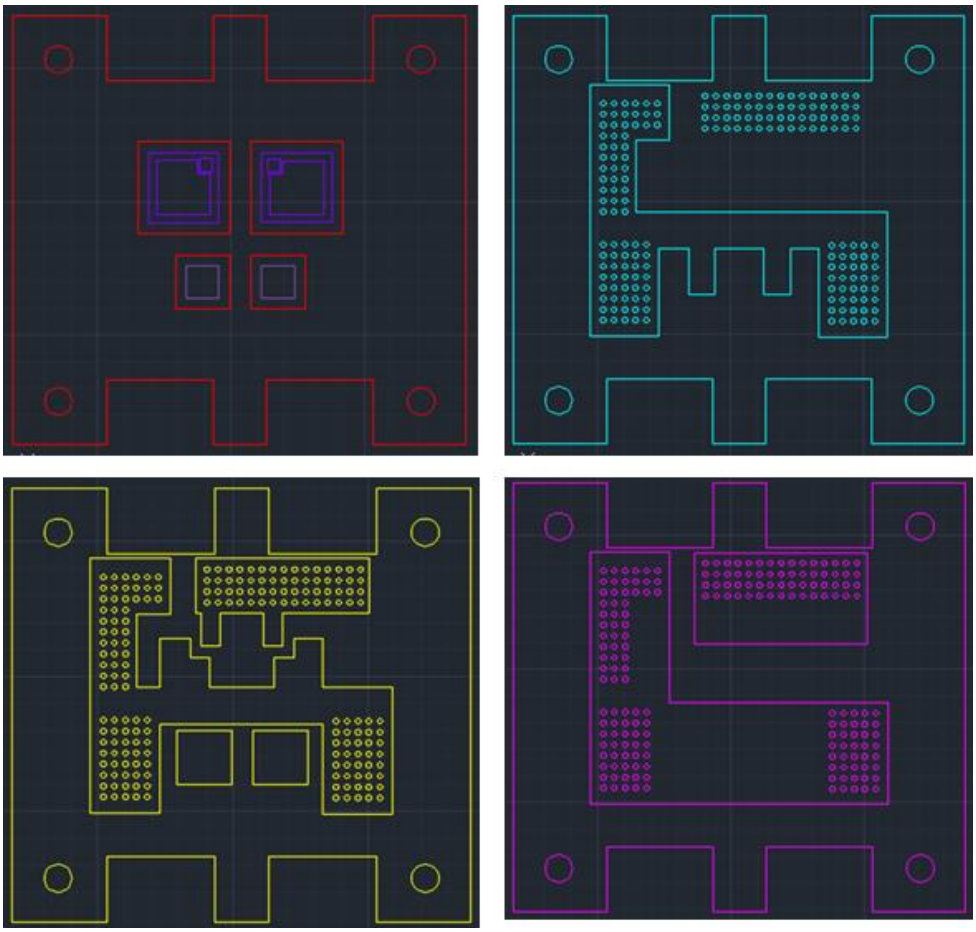

Fig. 5.21. AutoCAD drawing of different layers of the LTCC die carrier

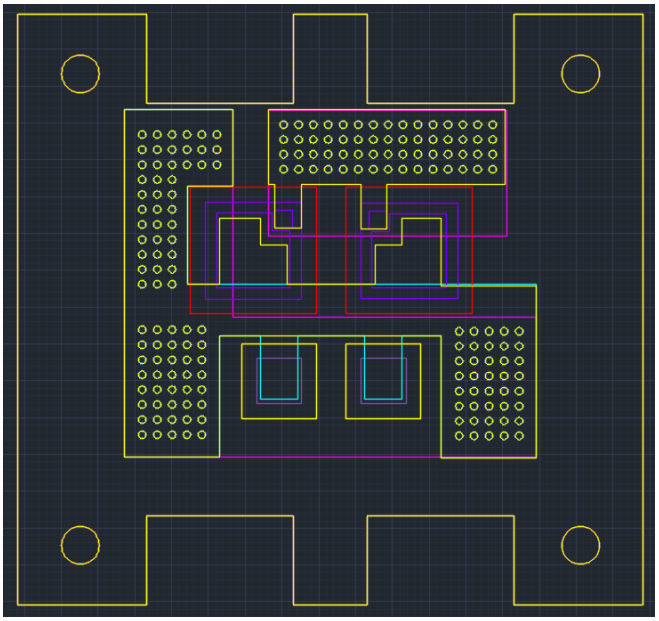

Fig. 5.22 AutoCAD drawing of multi-layer LTCC overlaid on top of each other

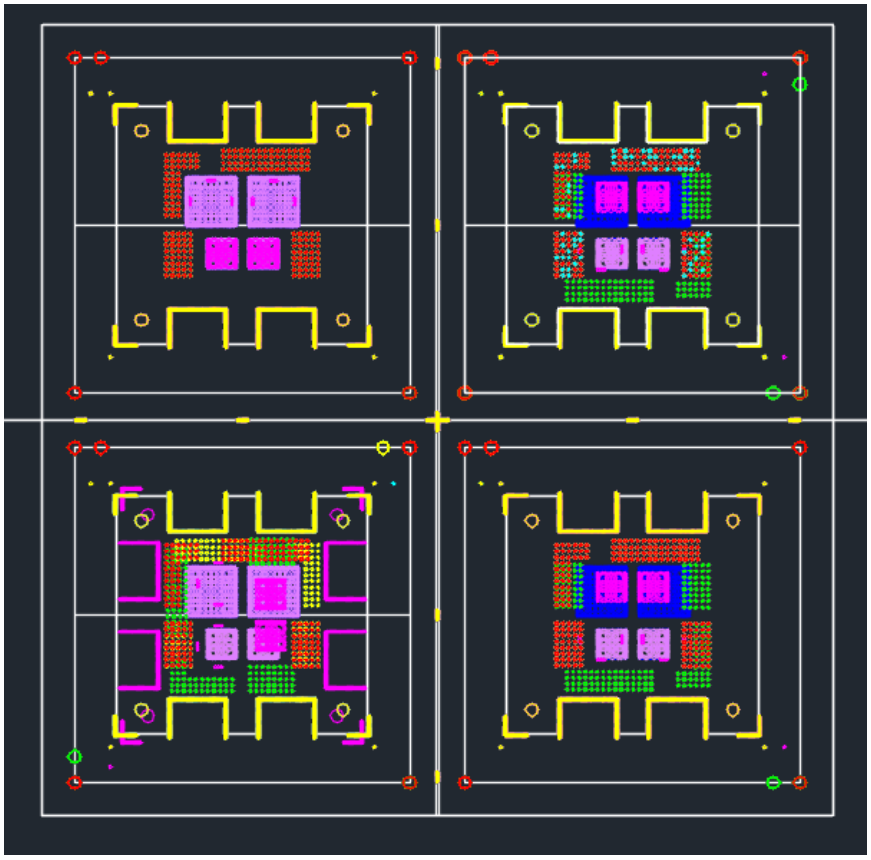

Fig. 5.23. Punch profile design in AutoCAD for punching vias and cavities on LTCC

5.7 Precondition of the LTCC tapes

Before creating device cut-outs and via punching, the LTCC green tapes are preconditioned for 10 minutes at 80 °C inside an oven. The preconditioning of the LTCC green tapes is generally performed to remove the protective Mylar from the LTCC tape later in the process. The Mylar of the LTCC tapes acts as a via fill mask and are not removed until the vias are filled with thick film paste and dried inside an oven. However, the protective Mylars are removed before the lamination process.

5.8 Creating device cut-outs and vias

The punch profile is used to create via holes and device cut-outs on the LTCC GreenTape™. The vias are punched using a 10 mils via punch in a multi-punching machine (MP-4150 SL). Fig. 5.24 show the multi-punching machine used for punching vias and cut out cavities for the devices. Fig. 5.25 shows a 6”×6” LTCC 951 GreenTape™ after via and cavity formation. Each of the layers of the multi-layer LTCC device carrier is punched according to the punch profile created for each layer.

Fig. 5.24. Via punch equipment

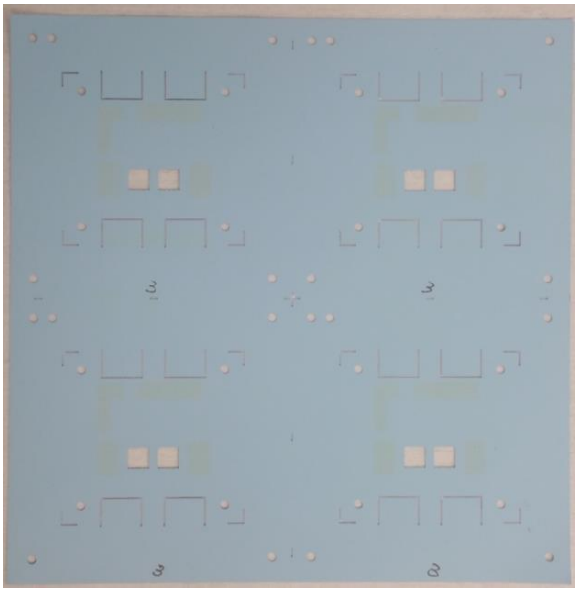

Fig. 5.25. 6”×6” LTCC GreenTape™ after via punch and formation of device cutout

5.9 Via fill and conductive metallization printing

After the vias and cavities are punched, they are filled with silver based conductive via fill paste. DuPont's 6141 via fill paste is used to fill the vias. In order to fill the vias, a via fill mask is used to protect the GreenTape™ from getting contaminated with the paste. The via fill mask is punched on an LTCC Mylar. A smooth surface made out of an aluminum block is used as a base to hold the LTCC tape and the mask using four alignment pins at the corner. A parchment paper is used underneath the LTCC tape to make sure it absorbs any extra amount of via fill paste to avoid spreading of the paste underneath and keep the LTCC GreenTape™ from getting contaminated. A squeegee blade spreader is used to fill the vias with a conductive silver paste. Fig. 5.26 shows the via fill setup used to fill the vias with conductive silver paste.

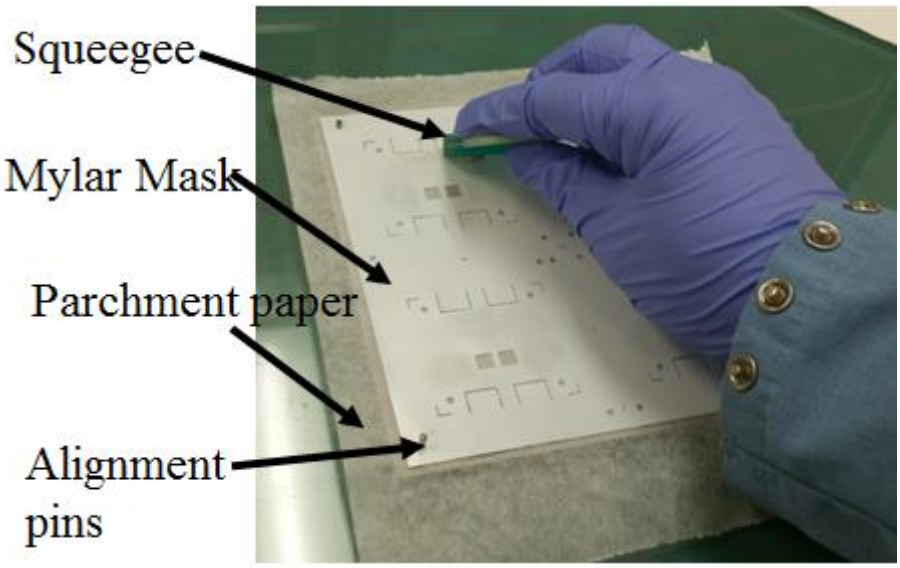

Fig. 5.26. Via fill process using a squeegee

After filling the vias the conductive paste is dried inside an oven for 10 minutes at 80 °C. Subsequently, metallization pads are created on the LTCC GreenTape™ using screen printing. Fig. 5.27 shows the screen used to print the metallization on LTCC. DuPont's 6146 silver-

palladium (Ag-Pd) based solderable co-fire paste is used to print the metallization on LTCC. The metallization on each LTCC layers is performed separately. Fig. 5.28 shows the screen printer used to print the metallization on the LTCC GreenTape™. The tape to be printed is kept on the platform beneath the screen and the platform vacuum is turned on to hold the tape in place. The alignment between the tape and the screen is performed using alignment marks placed on the tape and the screen. After the alignment is performed, the screen printable paste (DuPont's 6146) is applied onto the edge of the screen openings on top of the screen. Subsequently, the squeegee is used to print the paste on the LTCC tape. After the metallization, the printed silver paste on the LTCC GreenTape™ is dried inside an oven for 20 minutes at 80 °C before the lamination process. In order to maximize the LTCC GreenTape™ utilization four layers are designed on a single 6"×6" tape. After the metallization is dried the 6"×6" GreenTape™ are cut to separate each of the four individual layers using a slide cutter as shown in Fig. 5.29. Fig. 5.30 shows all the four individual layers laminated together to fabricate the LTCC die carrier substrate.

Fig. 5.27. Screen used to print the metallization of the LTCC GreenTape™

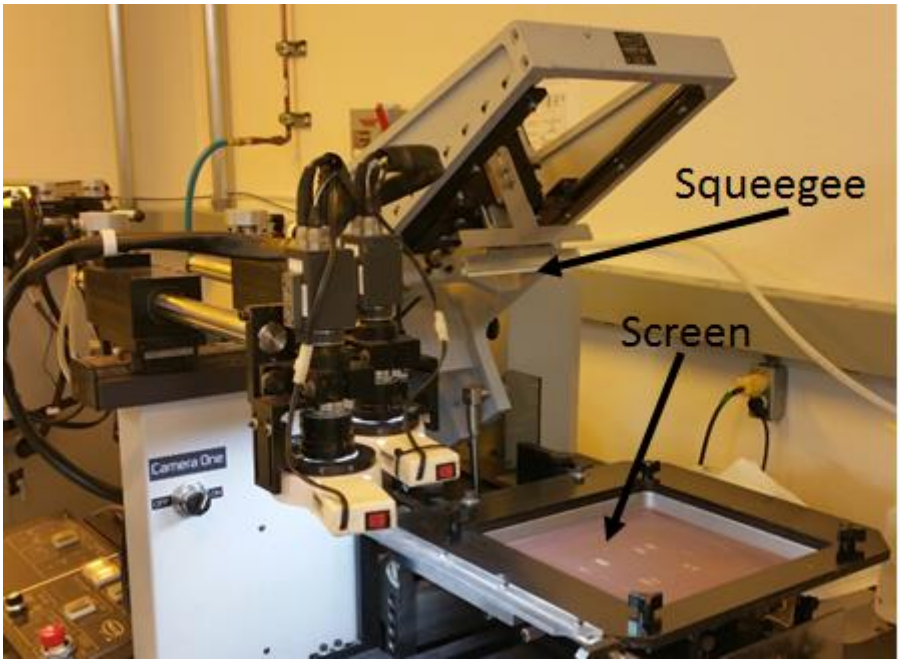

Fig. 5.28. Screen printing of LTCC metallization

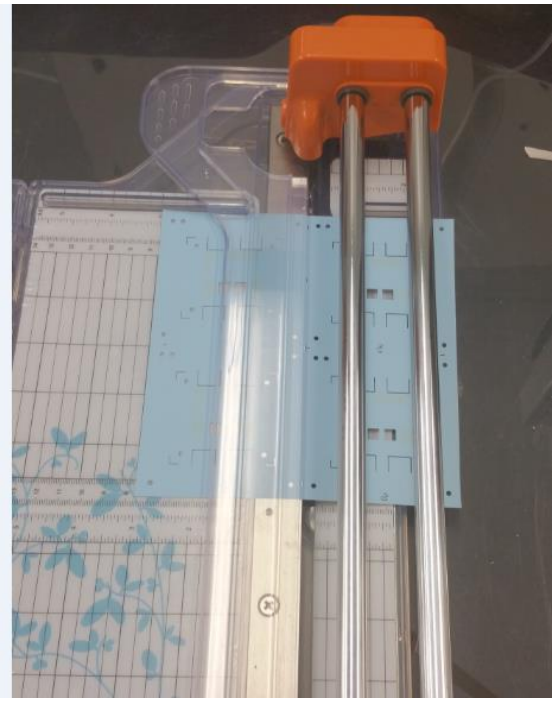

Fig. 5.29. Edge cutter used to separate the different layers of LTCC tapes from a 6”×6” GreenTape™

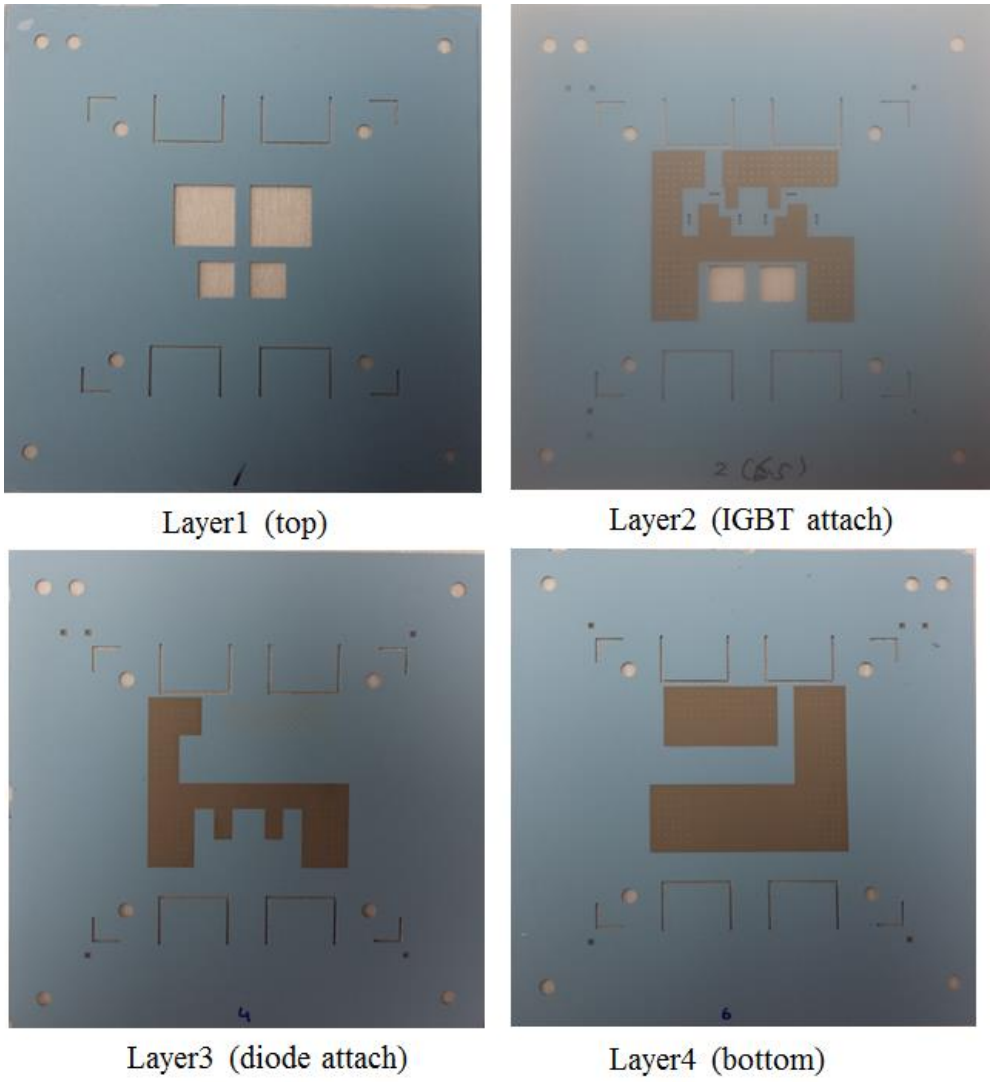

Fig. 5.30. Different layers of multi-layer LTCC die carrier

5.10 Lamination

In order to accommodate different die thickness of the IGBT and Schottky barrier diodes, the cavity depths on the LTCC die carrier substrate need to be controlled. The cavity depth on the LTCC die carrier is controlled by combining different thickness LTCC GreenTape™. The x, y, z shrinkage of the LTCC GreenTape™ are taken into account when designing for the cavity dimensions. The thicknesses of the Si-IGBT and Schottky barrier diodes are 140 µm and 377 µm

respectively. In order to accommodate the die thicknesses of the Si-IGBT and Schottky barrier diode, the following combination of tapes are used

i. The top layer (layer 1), according to Fig. 5.30, is fabricated using three 4.5 mils tapes to accommodate the IGBT die thickness. As can be seen from Fig. 5.30, layer 1 consists of cavities for both IGBT and diode devices.
ii. The IGBT attach layer (layer 2), according to Fig. 5.30, consist of one 6.5 mil tape. As can be seen from Fig. 5.30, layer 2 consists of cavities to accommodate the diode die thickness. The total diode die thickness is achieved by the combined cavity depths on layer 1 and layer 2. The metallization on layer 2 is used to attach the Si-IGBT devices.
iii. The diode attach layer (layer 3), according to Fig. 5.30, consists of one 10 mils tape. The metallization on Layer 3 is used to attach the Schottky diodes.
iv. The bottom layer (layer 4), according to Fig. 5.30, consist of one 10 mils tape. The metallization printed on bottom layer is used to solder the LTCC substrate to the bottom DBC later in the process.
v. Also, in between layers 3 and layer 4, one additional 10 mils layer tape with only conductive vias is added to provide higher rigidity to the LTCC die carrier substrate.

The lamination process to fabricate the LTCC die carrier substrate is carried out in several steps to ensure higher uniformity of the substrate. First, the identical layers with cavities are laminated together at a higher pressure. Secondly, all the layers with cavities are laminated at a reduced pressure. At the last step of lamination, all the other layers along with the layers with the cavities are combined and laminated together at a lower pressure than in the second step. The lamination sequence followed to fabricate the LTCC die carrier is as follows:

i. At the first step of lamination, three 4.5 mils tapes with cut outs for the Si-IGBT devices and the Schottky barrier diodes are laminated together at a pressure of 3000 PSI to form layer 1.

ii. The second step of lamination is performed to laminate layer 1(already laminated in the first step) with layer 2. The layers 1 and 2 are laminated with a pressure of 2500 PSI.

iii. In the third step, the remaining layers are laminated together with previously laminated layers 1 and 2 (from the second step of lamination) with a pressure of 2000 PSI.

The lamination of the LTCC GreenTape™ layers is performed using an isostatic press. The LTCC GreenTape™ are first stacked up on an aluminum base using alignment screws at four corners as shown in Fig. 5.31. In order to avoid direct contact between the LTCC GreenTape™ and the aluminum base, a top and bottom Mylar sheets are used to protect the tapes. After stacking all the desired layers for lamination, a top aluminum base, identical to the bottom base, is placed over the entire assembly. Fig. 5.32 shows the entire assembly with the stacked LTCC GreenTape™ layers sandwiched in between two aluminum bases.

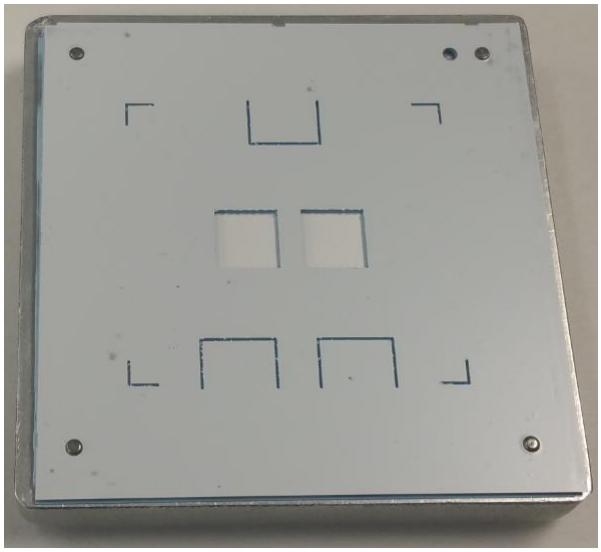

Fig. 5.31. Stacked LTCC GreenTape™ in preparation for lamination process

Fig. 5.32. LTCC GreenTape™ sandwiched between two aluminum bases

The entire assembly is then wrapped with a latex as shown in Fig. 5.33. After wrapping the assembly with latex, it is put inside (bags) and vacuumed sealed using AUDIONVAC VM 101H, shown in Fig. 5.34, vacuum sealing machine. The isostatic press is applied on the assembly inside a water bath. In order to make sure that water is not leaked inside and ruin the LTCC

tapes, the entire assembly is vacuum sealed four times using four bags. The vacuum sealed assembly is shown is Fig. 5.35. The vacuum sealed assembly is subsequently placed inside the isostatic press as shown in Fig. 5.36. The water bath is kept at 70 °C and a 10-minute lamination cycle is used to laminate the GreenTape™ assembly.

Fig. 5.33. LTCC GreenTape™ assembly wrapped in latex in preparation for lamination

Fig. 5.34. AUDIONVAC VM 101H vacuum sealer

Fig. 5.35. Vacuum sealed LTCC GreenTape™ assembly to carry out lamination process

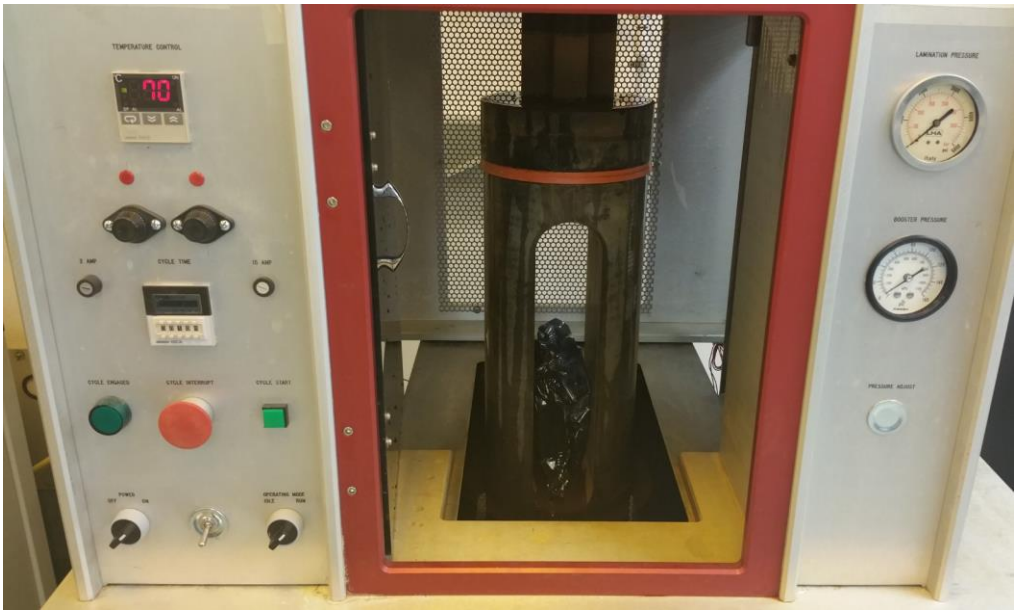

Fig. 5.36. Isostatic laminator used for laminating LTCC GreenTape™

5.11 Co-firing

After the lamination process, the LTCC die carrier is fired inside an oven. The laminated LTCC GreenTape™ is placed on an Al_2O_3 ceramic substrate and kept inside an oven for firing. The firing process involves the following steps:

i. The oven temperature is first ramped up to 350 °C. The ramp rate is kept at very low. The laminated tape is kept for 2 hours at 350 °C to make sure all the organic compounds on the GreenTape™ is burned out before the temperature is ramped up to the firing temperature of LTCC.

ii. After the burn-out of all the organic compounds, the temperature of the oven is ramped up to the firing temperature of LTCC. The firing of the LTCC is performed at 850 °C for 15-20 minutes.

iii. After the LTCC is fired, the oven temperature is ramped down to room temperature. The ramp down of the oven temperature is performed very slowly to reduce thermally induced stress on LTCC during ramp down.

The entire firing and the cool down cycle takes approximately 8-10 hours. Fig. 5.37 represents the LTCC die carrier substrate after the firing process. Subsequently, the fired LTCC is diced using a dicing saw to yield the LTCC die carrier. Fig. 5.38 shows the LTCC die carrier substrate after dicing.

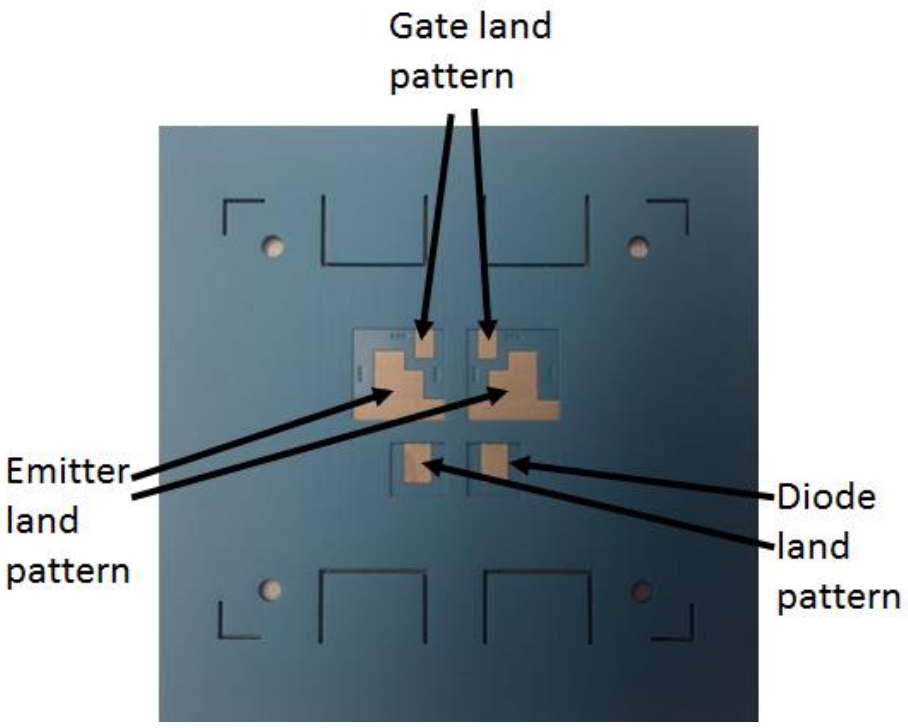

Fig. 5.37. LTCC die carrier after the firing process

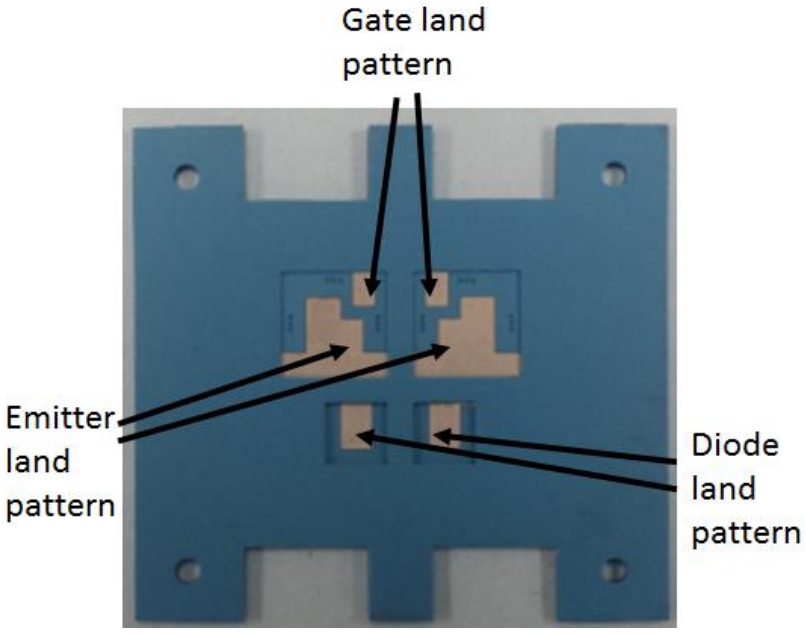

Fig. 5.38. Diced LTCC die carrier

5.12 Stand-alone Power Module Fabrication

After all the necessary components, such as die top surface preparation, top and bottom DBC substrate preparation, connector attachments and the LTCC die carrier preparation is completed the stand-alone power modules are fabricated. In order to fabricate the wire bondless power module, the semiconductor devices are attached to the LTCC substrate first. A flip-chip die attachment using Pb95Sn5 solder ball is performed to attach the power devices onto the LTCC die carrier. In preparation to the die attach, the LTCC substrate is cleaned using isopropyl alcohol (IPA). The alignment between the flip chip die and the land pattern on LTCC is performed using an MRSI-503M flip-chip bonder. Fig. 5.39 shows the flip chip bonder used to align the die with the land pattern on LTCC. Subsequently, the solder reflow is performed to do the flip-chip attachment of the devices inside a Sikama reflow oven. In order to prevent any movement of the devices during the reflow process, a graphite fixture is used to hold the devices in place. Fig. 5.40 (a) shows the exploded view of the die attach assembly. After the die attach, the edges of the cavities on the LTCC die carrier is filled with Nusil R-2187 two-part silicone elastomer and cured at 150 °C for 15 minutes. Fig. 5.40 (b) shows the LTCC die carrier with the attached Si-IGBT and SiC Schottky barrier diode devices. Once the die attach on the LTCC is performed, the wire bondless power module is assembled. The top and the bottom DBC is attached subsequently. The LTCC with the attached semiconductor devices is placed in between the top and bottom DBC substrates to do the attachment. Solder paste is applied on the metallization at the both top and bottom interfaces between the LTCC and DBC substrates. The entire assembly is placed inside a graphite fixture. The bottom DBC substrate is placed on the base of the bottom graphite fixture first as shown in Fig. 5.41. After that SAC 305 solder paste is applied on the DBC where the LTCC die carrier should be attached to route the gate and the

emitter contacts of the devices to the bottom connectors attached to the bottom DBC substrate. Subsequently, the LTCC die carrier is placed on top of the bottom DBC as shown in Fig. 5.41. After that SAC 305 solder paste is applied on the collector metallization of IGBT and cathode metallization of Schottky barrier diodes. After applying the solder paste, the top DBC substrate is placed to attach the DBC to the devices to route the collector of the devices to the connector attached to the top DBC substrate as shown in Fig. 5.41. After placing the top DBC substrate a top graphite fixture is placed and the entire assembly is tightly secured using six screws as shown in Fig. 5.42. Subsequently, the entire assembly is reflowed in a Sikama reflow oven to attach the DBC substrates to the LTCC die carrier to fabricate the stand-alone power module. Fig. 5.43 represents the reflow profile used for the solder attachment. Fig. 5.44 represents the wire bondless stand-alone power module consisting of a switching position fabricated to build the module-level 3-D half-bridge stack.

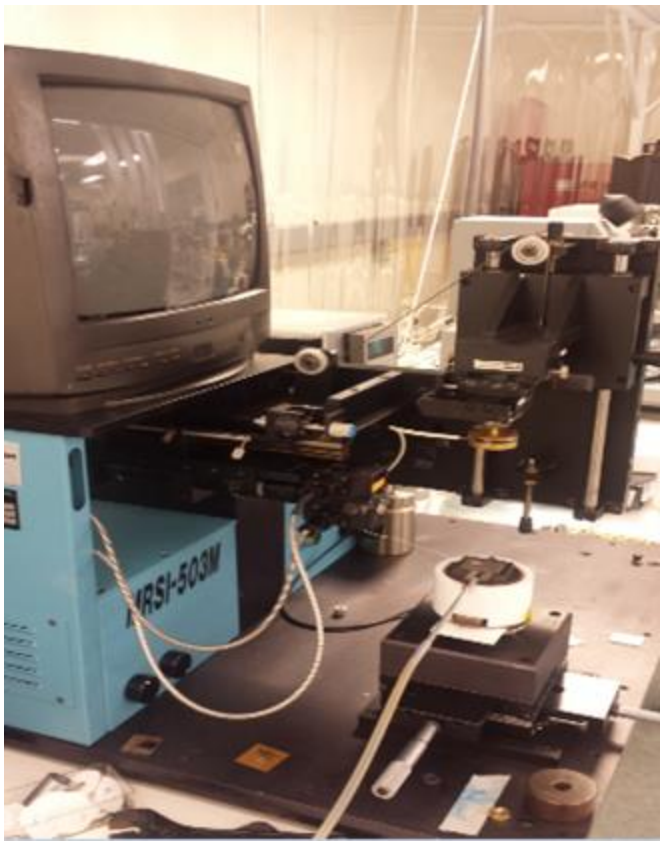

Fig. 5.39. MRSI-503M flip-chip bonder

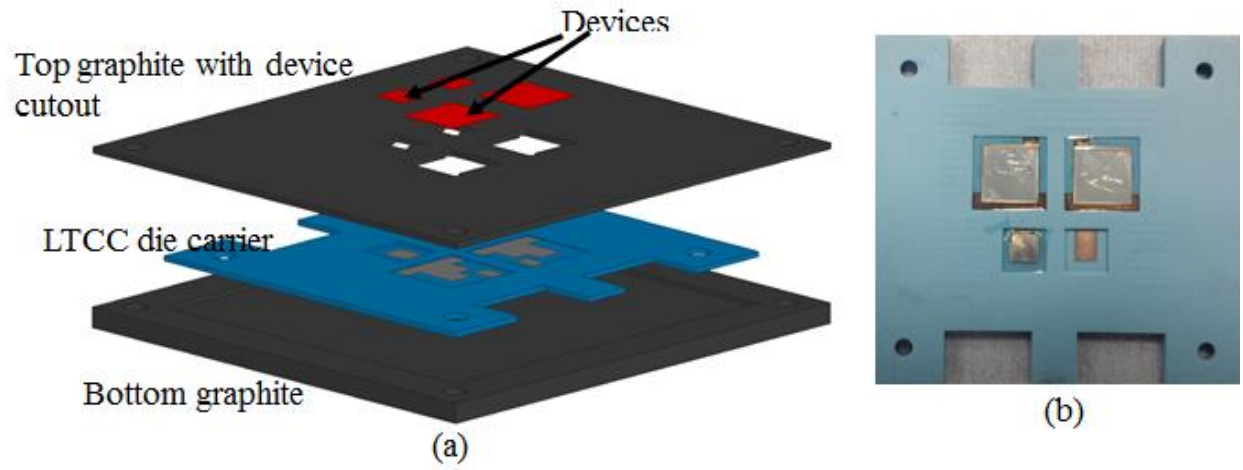

Fig. 5.40 (a) Exploded view of the die attach assembly on LTCC die carrier substrate (b) LTCC die carrier with attached Si-IGBT and SiC Schottky barrier diodes

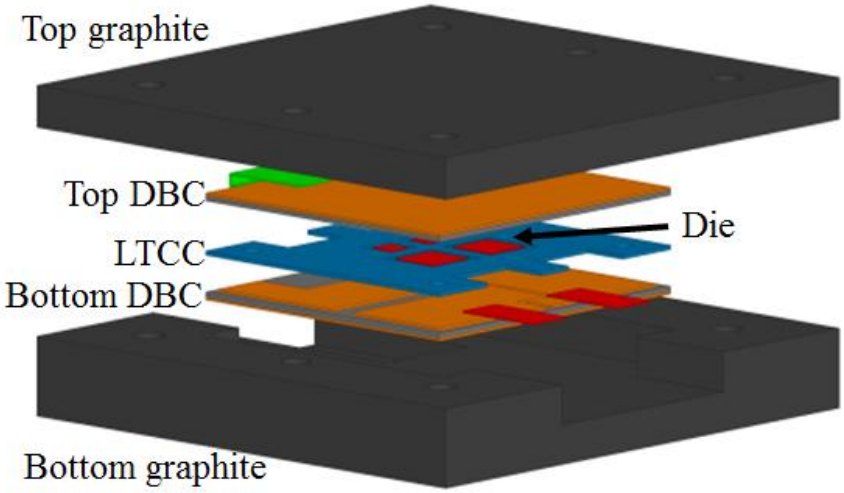

Fig. 5.41. Exploded view of the assembly to fabricate the stand-alone power modules

Fig. 5.42. Fixturing used to fabricate the stand-alone power module

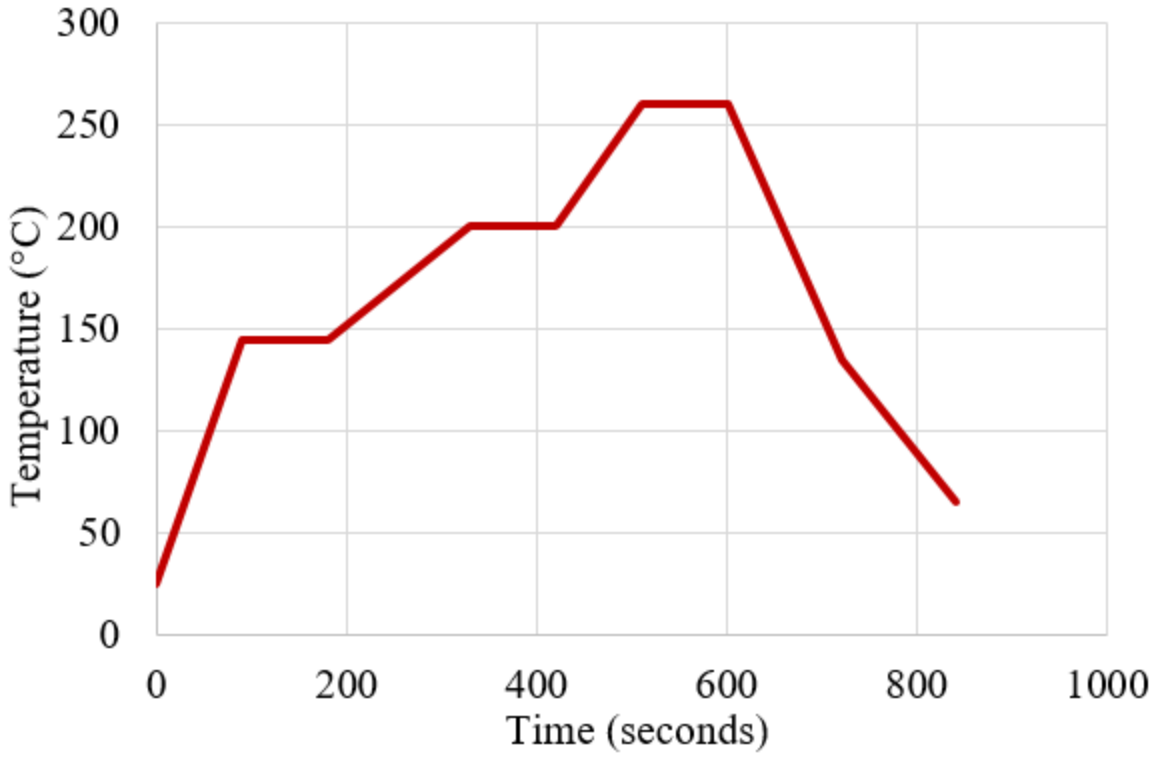

Fig. 5.43. SAC 305 reflow profile used for attaching the top and the bottom DBC substrate with the LTCC die carrier

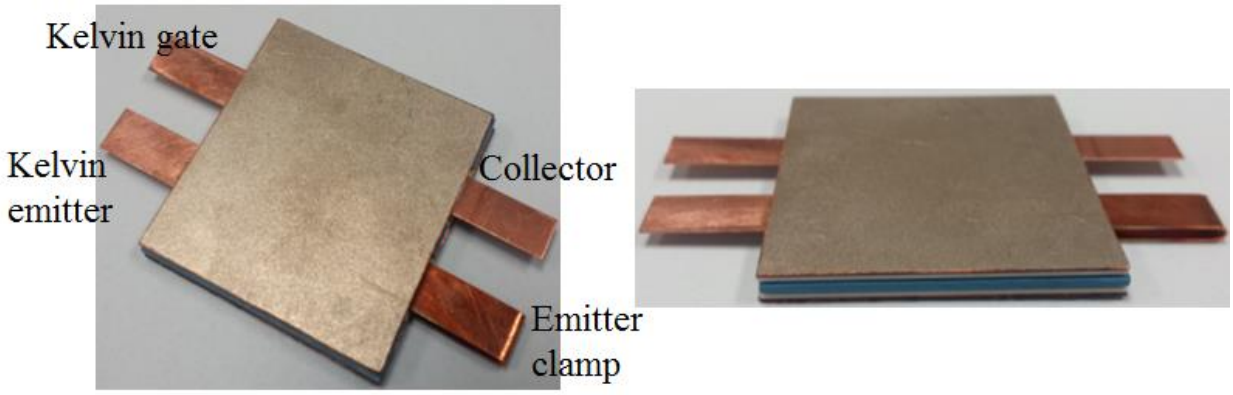

Fig. 5.44. Fabricated stand-alone power module showing all the terminals

5.13 Spring Loaded LTCC Interposer

In the proposed power module, a spring loaded LTCC interposer is used to establish interconnection between the top and the bottom stand-alone power module to form the 3-D half-bridge stacked power module. The spring loaded LTCC interposer provides better mechanical

compliance to the 3-D stacked power module structure. The LTCC interposer is fabricated by populating an LTCC fixture with spring-loaded pins. The spring-loaded pins used to fabricate the interposer are manufactured by Mill-Max (Part No. 0965-0-15-20-80-14-11-0) [1]. Each spring-loaded contact is gold plated with plating thickness of 0.508 µm and can carry 3 A of continuous current. An array of 36 paralleled spring loaded contacts are used to fabricate the interposer to ensure the higher current handling capability of the interposer. The spring-loaded contacts are rated to endure 1,000,000 cycles. The total height of each spring-loaded pins is 2.54 mm with a maximum stroke of 0.61 mm. The total thickness of the LTCC interposer is designed to be 1.93 mm to ensure the utilization of the maximum stroke of the spring-loaded pins to fabricate the module-level 3-D press-pack structure. The spacing between the spring-loaded pins is designed to be 3.83 mm. The hole diameter on the LTCC fixture is designed to be slightly bigger than the diameter of the spring-loaded pins to easily populate the fixture with the spring pins. Fig. 5.45 represents the side view of the LTCC interposer showing all the critical dimensions. Fig. 5.46 shows the fabricated LTCC interposer populated with spring-loaded spring pins.

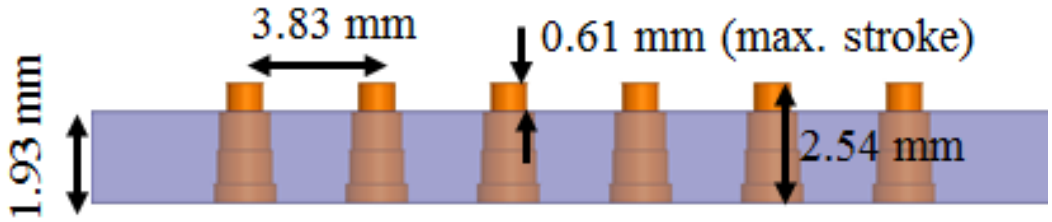

Fig. 5.45. Side view of the LTCC interposer with critical dimensions (mm)

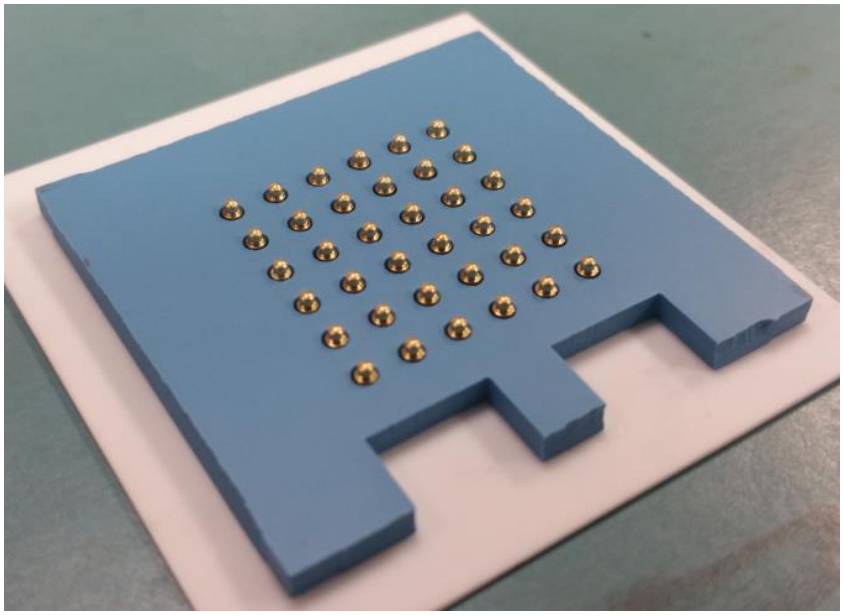

Fig. 5.46. Fabricated LTCC spring-loaded interposer

5.14 Assembly of 3-D Module-Level Press-Pack Stack

The module-level press-pack stack is assembled after all the individual components of the 3-D stack are fabricated and machined separately. As discussed earlier, the 3-D module-level press-pack consists of two wire bondless power modules. The two wire bondless power module is stacked on top of each other using the LTCC spring-loaded interposer sandwiched in between each other. The entire stacked power module assembly is placed inside a top and bottom holding frame using six clamping screws. The clamping force can be calculated using the spring constant of each spring-loaded pins according to Hooke's law:

$$F = kx \qquad (5.1)$$

Where, F is force in N, k is spring constant in N/m and x is the displacement of the spring from its relaxed position.

According to the manufacturer date sheet, each spring pins have a spring constant of 2252 N/m. As discussed earlier, the spring-loaded interposer consists of 36 spring loaded pins in a parallel configuration. The total spring constant for ‘n’ parallel connected springs is given by:

$$k_{eq} = k_1 + k_2 + \cdots + k_n \qquad (5.2)$$

As such, the total spring constant offered by the 36 springs connected in parallel is 81072 N/m.

According to the manufacturer’s datasheet, the mid-stroke of the spring-loaded pins are 0.3 mm Assuming the two stand-alone power modules are clamped up to the mid stroke of springs, the total clamping force can be calculated from Hooke’s law as 24.7 N.

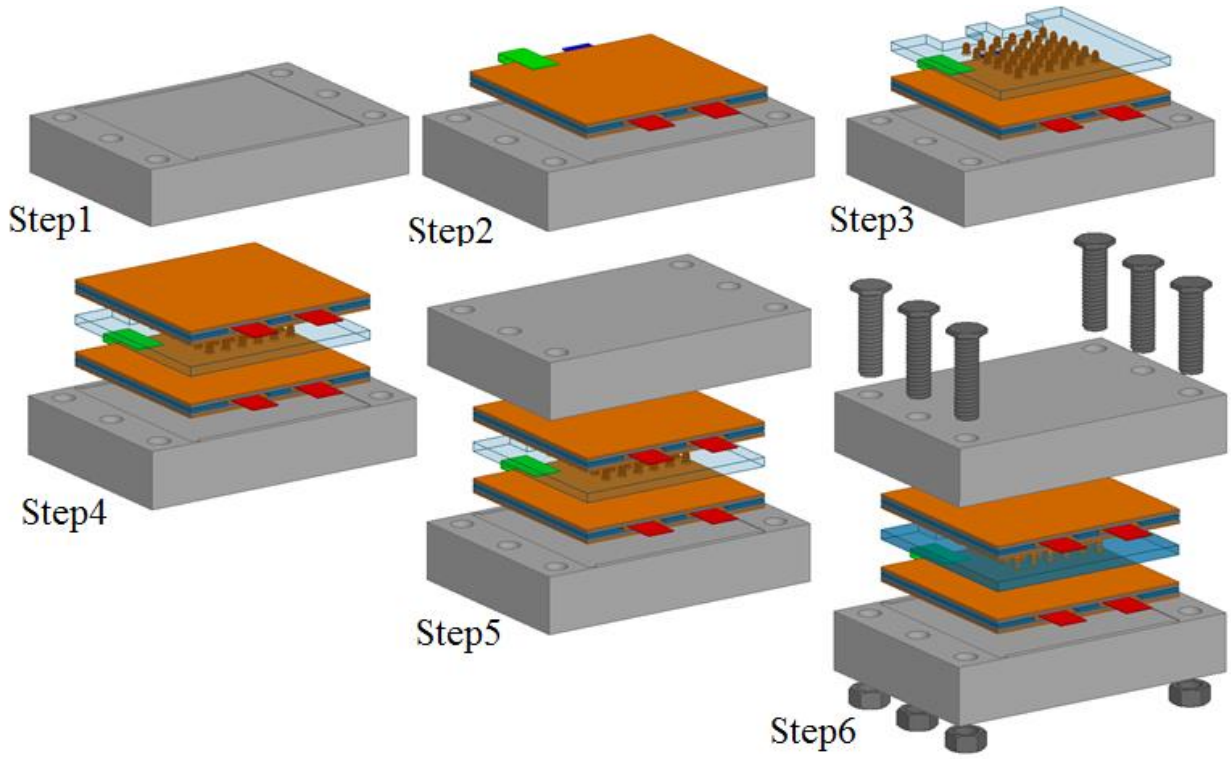

Fig. 5.47. Chronological step by step representation of the process to assemble the 3-D module-level half-bridge power module stack

Fig. 5.47 represents chronological steps to assemble the 3-D module-level press-pack stacked power module. Fig. 5.48 represents the fabricated 3-D module-level stacked half-bridge power module.

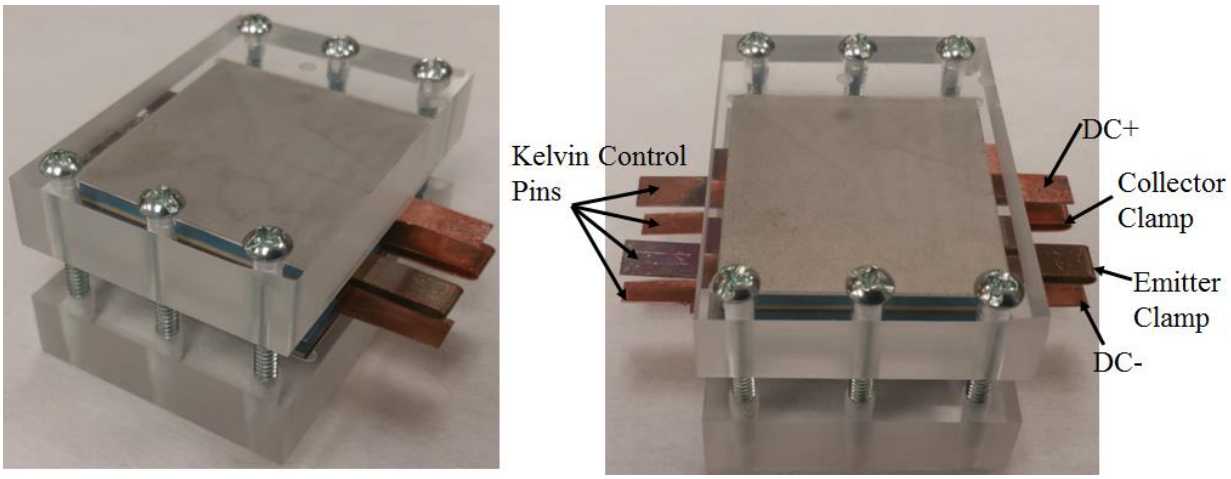

Fig. 5.48. Fabricated prototype of the 3-D module-level half-bridge stack

5.15 Summary

In this chapter, the detailed fabrication process of the 3-D module-level half-bridge stacked power module is discussed. There are multiple process steps to fabricate the 3-D power module. The fabrication process for all the individual components of the 3-D power module is discussed. The detailed LTCC process flow to fabricate the LTCC die carrier and the LTCC interposer is discussed. The connector and devices attachment processes are explained and the process parameters and the process steps are listed. Also, the assembly process to assemble the 3-D power module is discussed. Several 3-D module levels half-bridge stacks are successfully fabricated.

5.16 References

[1] "Mill-Max: 0965-Spring-Loaded Pin". *Mill-max.com*. N.p., 2017. Web. 6 May 2017.

Chapter 6 Characterization of 3-D Wire Bondless Half-Bridge Power Module

In this chapter, the characterization of the 3-D wire bondless half-bridge power module stack is performed. The switching characteristics of the fabricated 3-D stacked power module are characterized using double pulse test. Subsequently, the switching performance of a wire bonded half-bridge module is measured and compared to the switching performance of the 3-D stacked half-bridge power module. The static characteristics of the packaged devices are performed using a curve tracer to investigate the effect of packaging approach on the static characteristics of the devices. The wire bondless and a wire bonded module are compared in terms of their electromagnetic interference (EMI) response. Reliability assessment of the power module is performed using thermal cycling. Also, leakage current measurement under high reverse voltage is measured for the fabricated power module.

6.1 Switching Characteristics of the 3-D Stacked Power Module

Double pulse test is performed to characterize the switching performance of the 3-D wire bondless half-bridge stack. The double pulse test measurement setup includes the power module under test, a DC capacitor bank to provide low inductance DC bus, gate driver board, Pearson current monitor to monitor the drain current waveform, a load inductor, power supplies, function generator, digital oscilloscope. Fig. 6.1 shows a double pulse test circuit to characterize the switching performance of the power module. A function generator is used to create a double pulse signal to turn on and turn off the device under test. The first pulse of the double pulse signal establishes the desired current level in the load inductor. The turn-off instance of the first pulse creates current in the free-wheeling diode and the turn-off characteristics of the device under test are observed. The second pulse is usually on for a very short time. During the turn-on

event of the second pulse, the reverse recovery of the free-wheeling diode occurs and the turn-on characteristics of the device under test is observed. The module is tested at 150 V DC bus voltage and the pulse duration is adjusted to set the maximum collector current to 5 A. Fig. 6.2 shows the double pulse test setup for the 3-D stack power module. As can be seen, DC capacitor bank is used to minimize the DC bus inductance. However, the bus bars that connect the DC terminals of the 3-D stack power module to the DC capacitor bank outputs introduce an additional 18 nH of inductance. In order to measure the switching current, a current transformer with toroid magnetic core is used in the power loop as shown in Fig. 6.2. A function generator is used to provide the gate pulse required to turn on the IGBT devices. The test condition for the double pulse test for the 3-D stack is listed in Table 6.1.

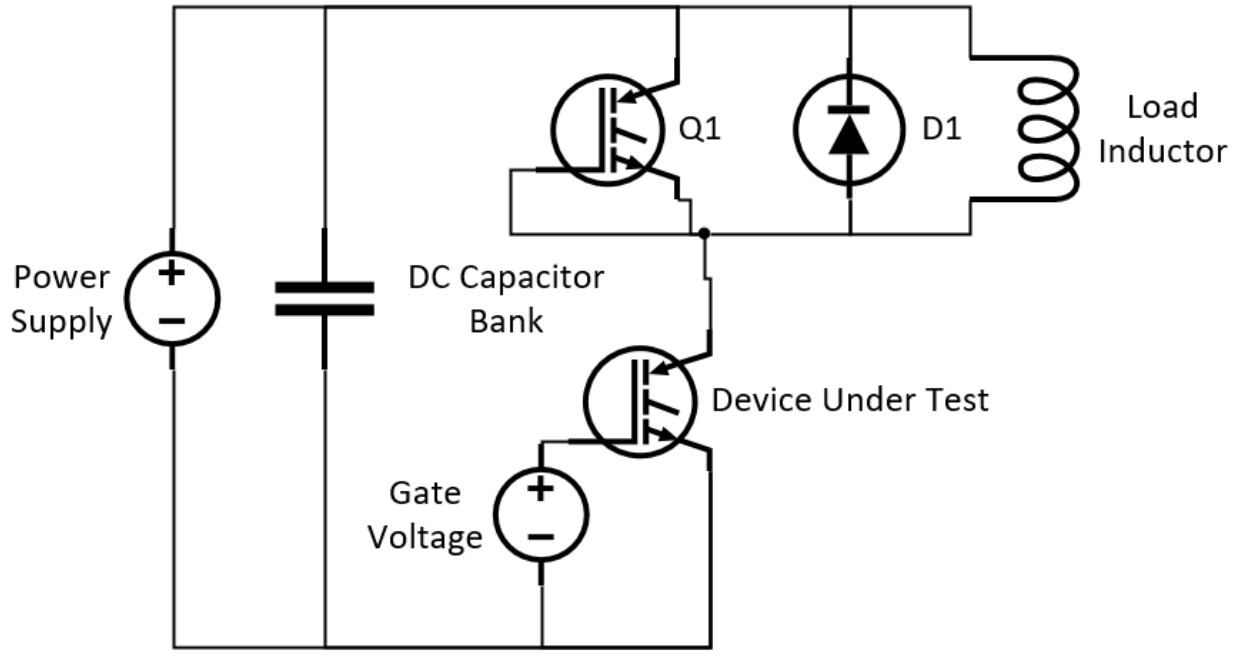

Fig. 6.1. Double pulse test circuit

Table 6.1. Double pulse test condition for 3-D stack

Gate voltage, V_{GE}	-5/+15 V
Gate resistor, R_G	6.65 Ω
DC bus voltage, V_{DC}	150 V
Maximum collector current, $I_{Cmax.}$	5 A

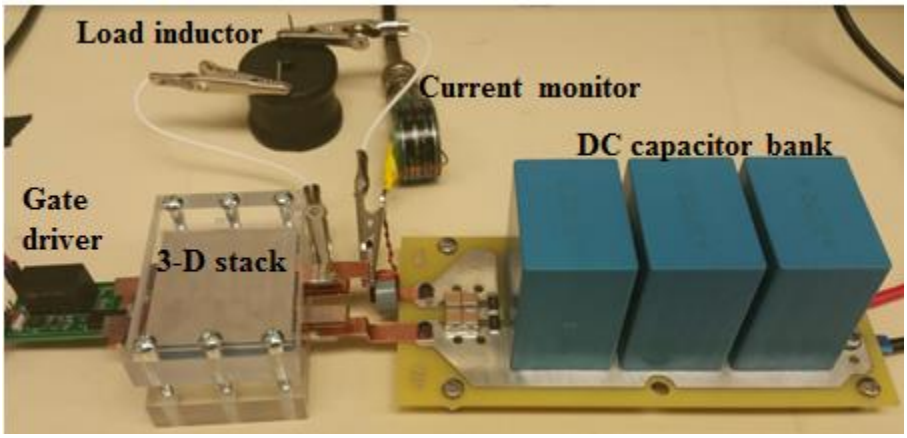

Fig. 6.2. Double pulse test setup for switching test

Fig. 6.3 and Fig. 6.4 shows the turn-on and turn-off switching waveforms for the wire bondless 3-D stack power module. As can be seen from Fig. 6.3 no significant turn-on current ringing is observed in the switching waveform. Also, during the turn-off event as shown in Fig. 6.4 the voltage overshoot is negligible. As such, verifying lower inductance of the wire bondless 3-D stack power module.

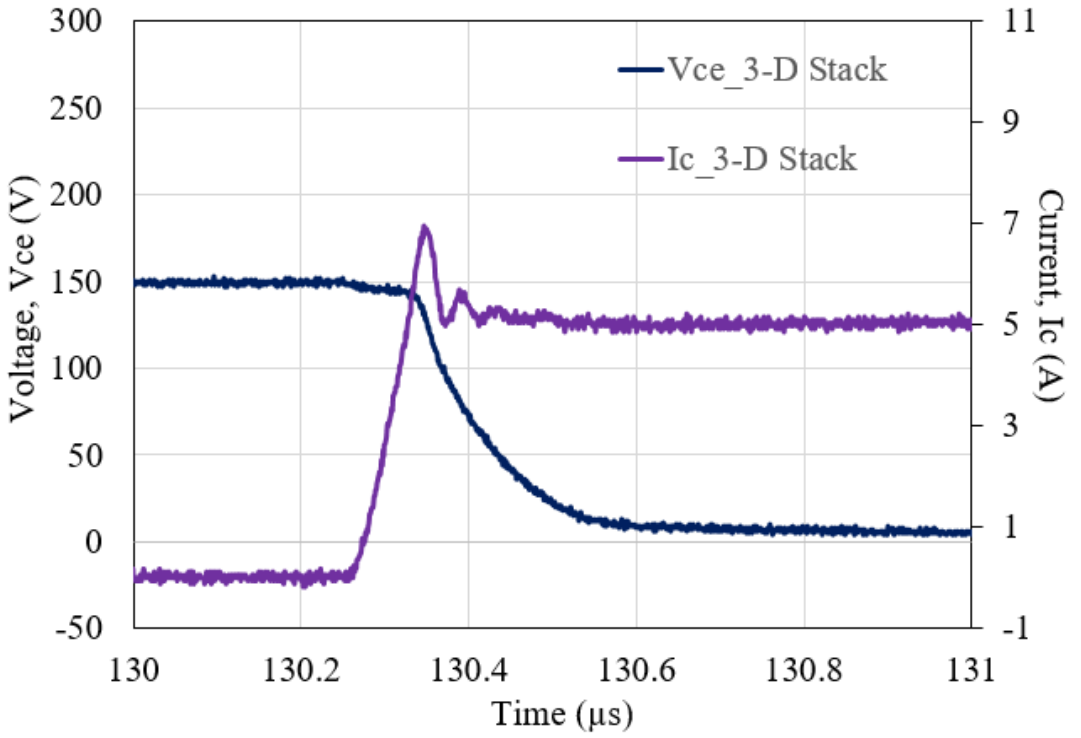

Fig. 6.3. Turn-on current and voltage waveform of the wire bondless 3-D stack (measured)

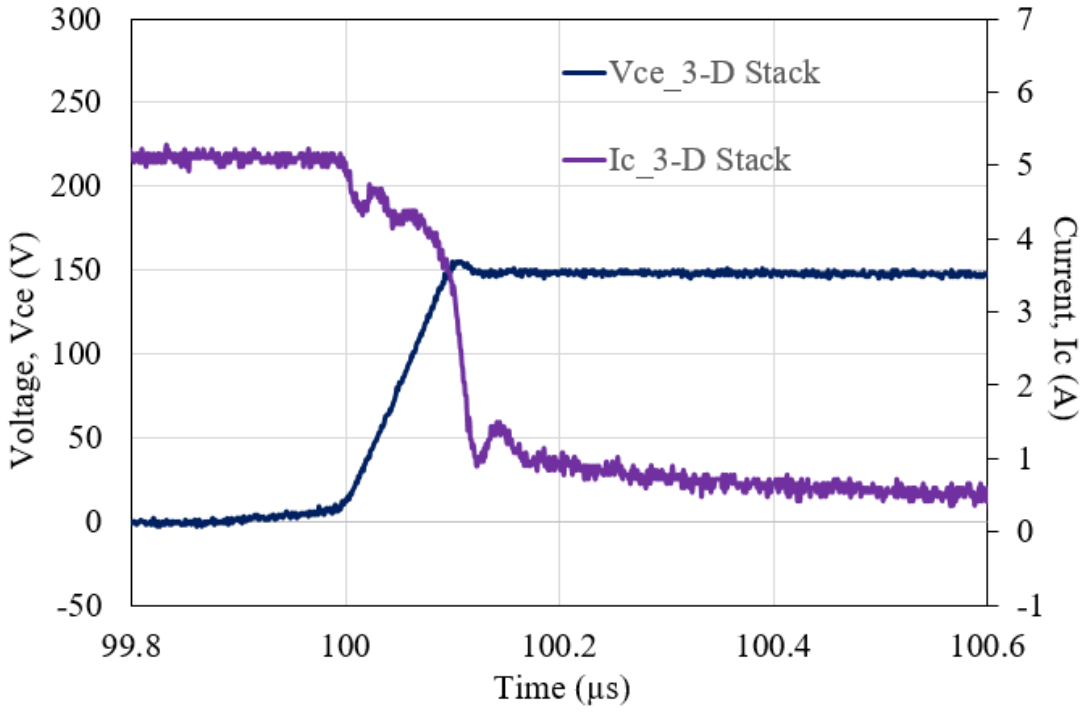

Fig. 6.4. Turn-off current and voltage waveform of the wire bondless 3-D stack (measured)

In order to investigate the switching waveform of the 3-D stack compared to a wire bonded counterpart, wire bonded half-bridge module is designed and fabricated. The wire bonded module is also tested using double pulse test setup using the same test conditions listed in Table 6.1. Fig. 6.5 shows the fabricated wire bonded half-bridge power module. Fig. 6.6 and Fig. 6.7 shows the turn-on and turn-off characteristics of the wire bonded power module respectively. As can be seen from Fig. 6.6 and Fig. 6.7 the switching current waveform at turn-on shows significant ringing compared to the wire bondless 3-D stack. Also, the turn-off voltage overshoot as can be seen from Fig. 6.7 is significantly higher than the 3-D stack module.

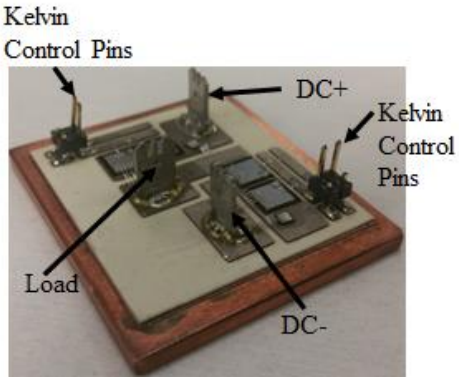

Fig. 6.5 Fabricated wire bonded half-bridge module

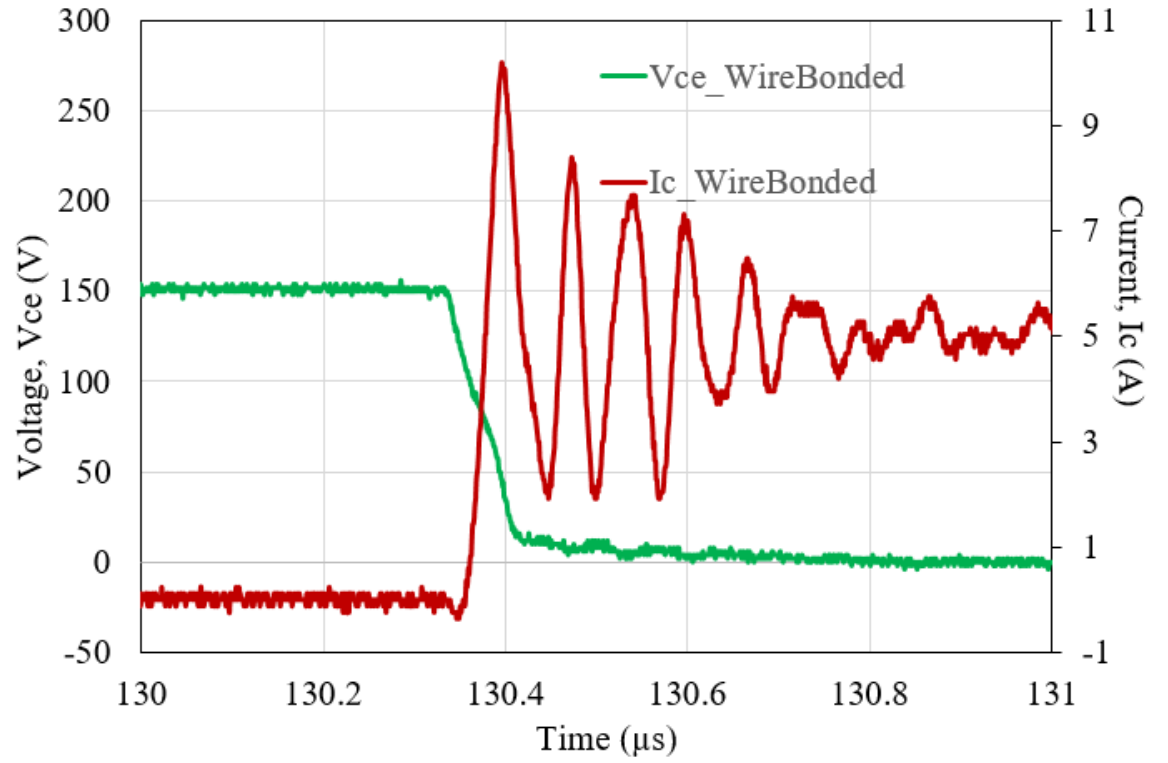

Fig. 6.6. Turn-on current and voltage waveform of the wire bonded module (measured)

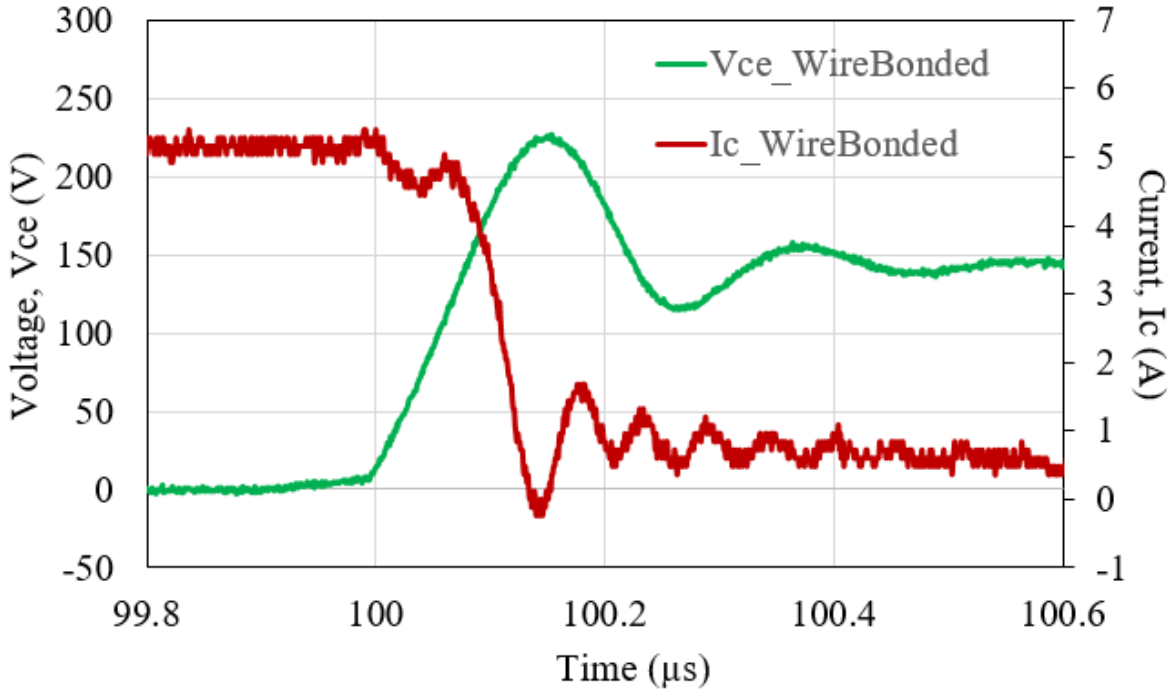

Fig. 6.7. Turn-off current and voltage waveform of the wire bonded module (measured)

Fig. 6.8 and Fig. 6.9 shows the switching characteristics comparison between the wire bonded and the wire bondless 3-D stack. As can be seen, significant performance improvement in terms of reduced turn-on and turn-off overshoot and ringing is achieved for the wire bondless 3-D stack. Fig. 6.8 compares the turn-on switching characteristics between the wire bonded and the wire bondless 3-D stack power module. As can be seen, the current overshoot at turn-on for the wire bonded power module is 10 A compared to 7 A of that of the 3-D stack. As such, 30% decrease in turn-on overshoot is achieved for the wire bondless 3-D stack. It can also be observed from Fig. 6.8 that there is 100 ns turn on delay for the wire bonded power module compared to the 3-D stack. This can be attributed to the higher gate loop parasitic inductance that results in delayed gate signals for the wire bonded module. Moreover, the settling time for the turn-on current ringing is significantly reduced for the wire bondless 3-D stack compared to the wire bonded counterpart. Fig. 6.9 compares the turn-off switching characteristics of the two modules. As can be seen, the voltage overshoot at turn-off is significantly reduced from 210 V to 160 V for the wire bondless 3-D stack that corresponds to 43% reduction in voltage overshoot compared to the wire bonded module. Moreover, as can be observed from Fig. 6.9, the turn-off current ringing reduces with lower settling time for the wire bondless 3-D stack. The reduction of turn-on and turn-off overshoot, ringing, settling time further verifies the lower overall inductance of the 3-D stack compared to the wire bonded counterpart.

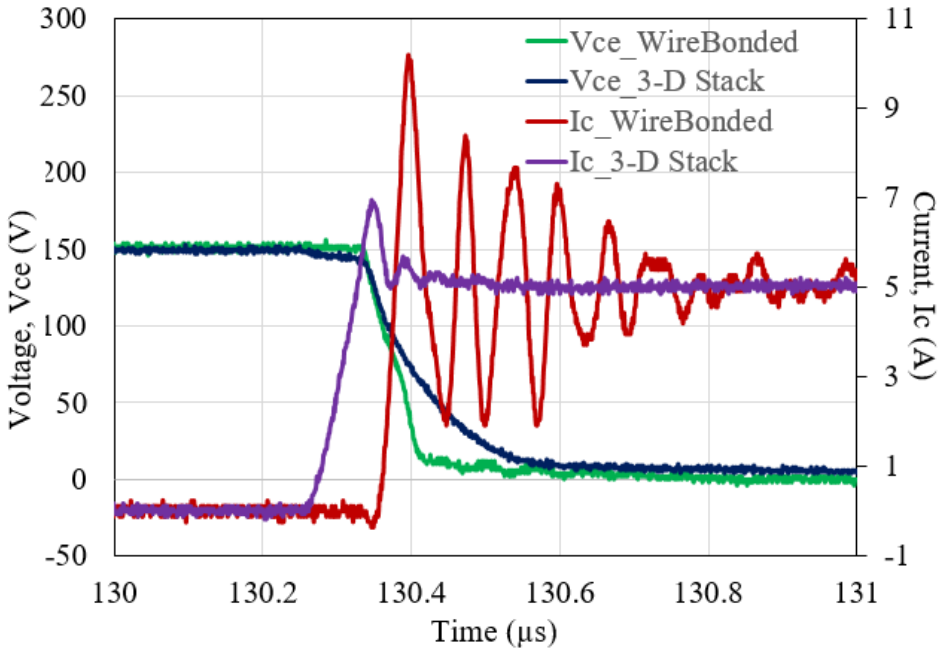

Fig. 6.8. Comparison of the turn-on voltage and current waveform between 3-D stack and wire bonded power module

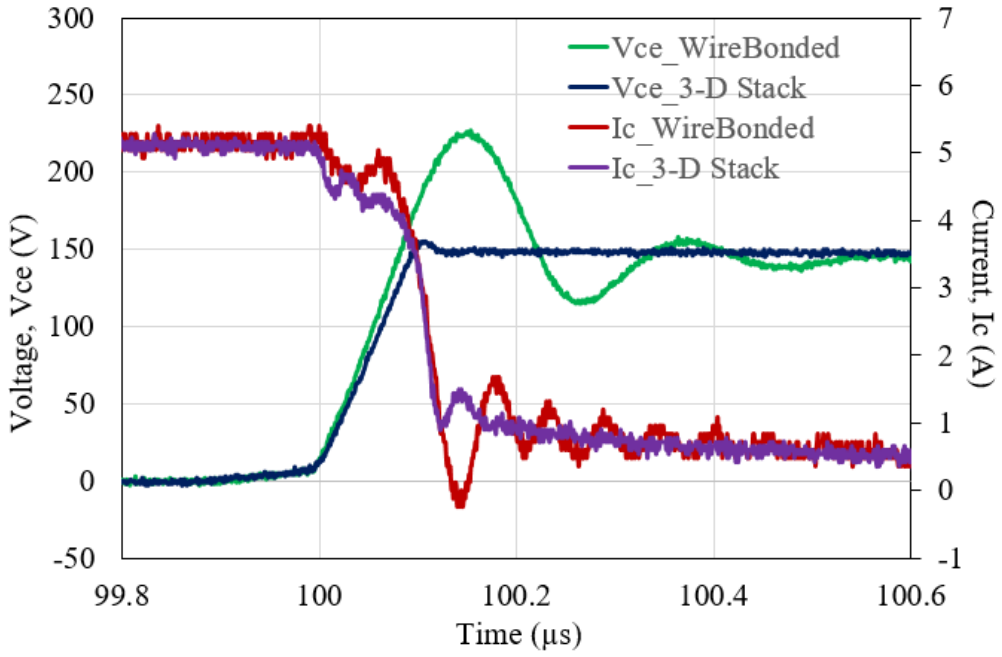

Fig. 6.9 Comparison of the turn-off voltage and current waveforms between 3-D stack and wire bonded power module

6.2 Static Characteristics of the 3-D Stack

The static characteristics of the wire bondless 3-D stack are performed to verify if the devices packaged inside each stand-alone power module are working. Fig. 6.10 and Fig. 6.11 represents the on-state characteristics of the top and the bottom module respectively under various gate voltages. As can be seen from Fig. 6.10 and Fig. 6.11, for 15 V gate voltage the peak current is 60 A with a collector-emitter voltage of 4.5 V. As such, the on-state resistance is calculated as 75 mΩ for the two paralleled IGBT devices. However, according to the manufacturer's datasheet, the on-state resistance of a single IGBT device is 60 mΩ. As such, assuming no package induced resistance the on-state resistance should be 30 mΩ for two paralleled devices. However, the increase in on-state resistance of the devices by 35 mΩ can be attributed to the relatively high resistivity of the LTCC silver metallization and via fill materials. Fig. 6.12 shows the forward characteristics of the anti-parallel diodes inside the stand-alone power modules.

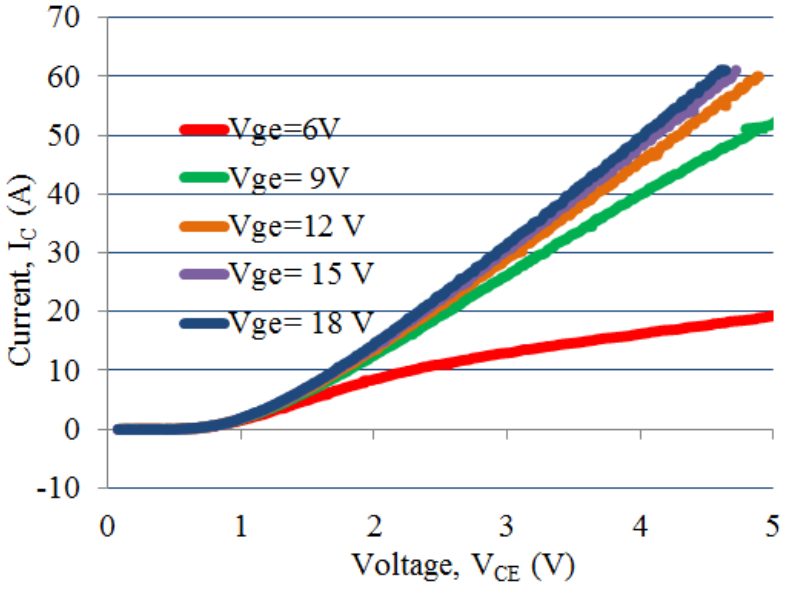

Fig. 6.10. On-state characteristics of top module

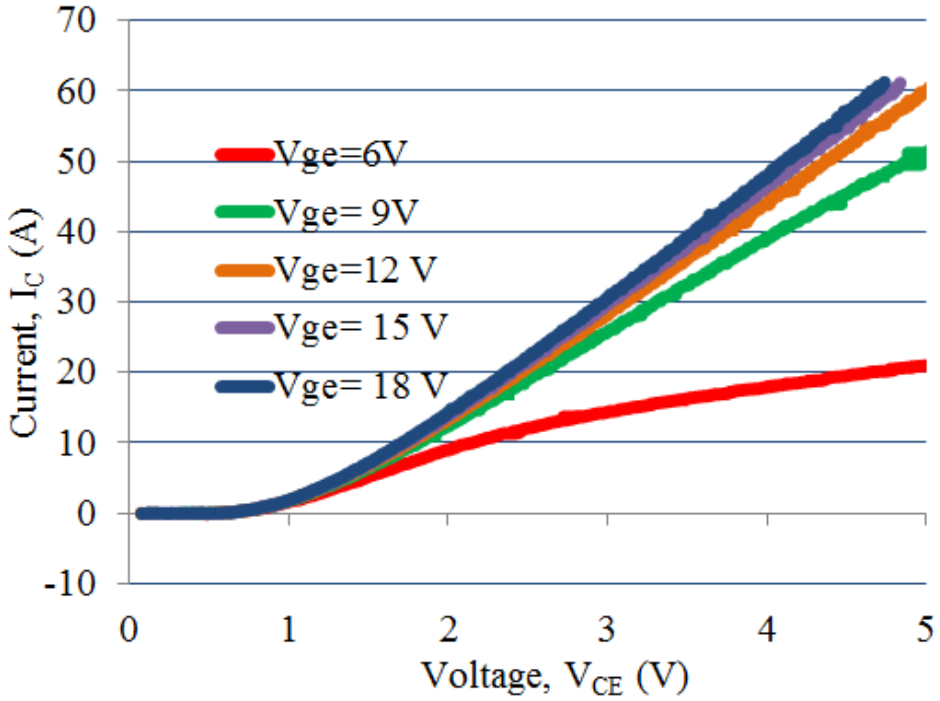

Fig. 6.11. On-state characteristics of bottom module

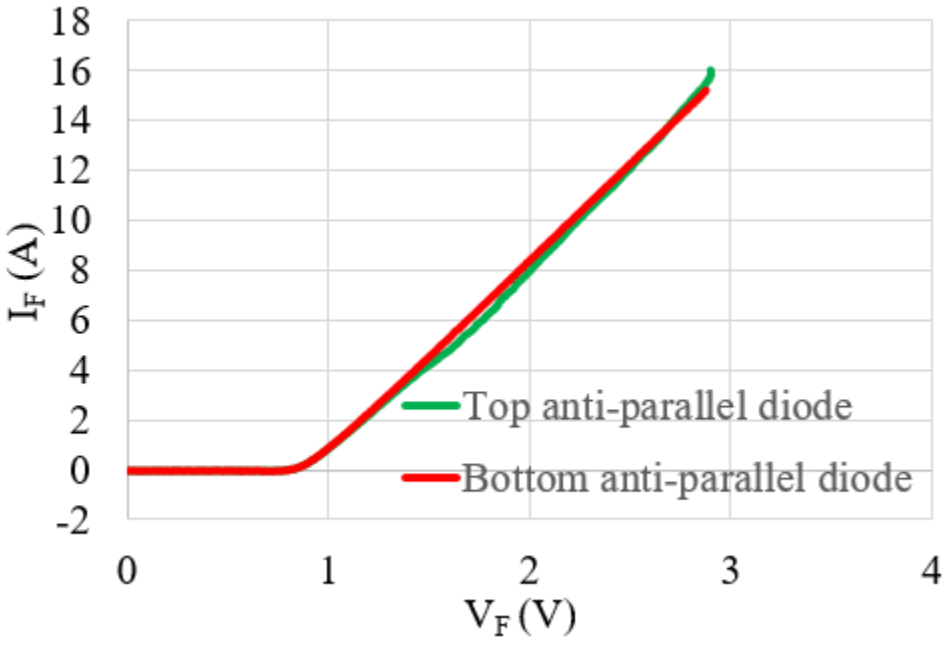

Fig. 6.12. Forward characteristics of the SiC Schottky barrier diode

6.3 Conducted Electromagnetic Interference Measurement

The 3-D wire bondless power module is characterized for its conducted electromagnetic interference (EMI) response. The conducted EMI response of the 3-D wire bondless half-bridge stack is compared to a wire bonded half-bridge power module. The 3-D wire bondless stack and the wire bonded half-bridge power module are shown in Fig. 5.48 and Fig. 6.5 respectively. The conducted EMI measurement setup includes a line impedance stabilization network (LISN), a power supply, a power line filter and a spectrum analyzer as shown in Fig. 6.13. A power line filter (CORCOM F7123) is used between the power supply (HP-E3630A) and the line impedance stabilization network. A spectrum analyzer (Rigol-DSA 815) is used to observe the EMI spectrum up to 30 MHz. The 3-D wire bondless and the wire bonded half-bridge power modules are both set up to operate as a half-bridge inverter to measure the conducted EMI from the power stage. Fig. 6.14 shows the circuit schematic of the half-bridge inverter.

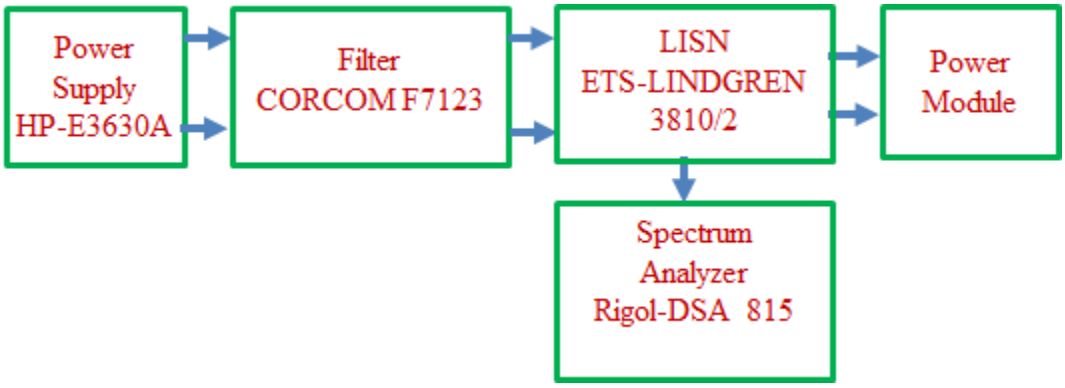

Fig. 6.13. Measurement setup for conducted EMI measurement

A set of capacitors, C1 and C2, are required to provide a neutral point for the output to maintain a constant output voltage of $V_{in}/2$. The value of the two capacitors, C1 and C2, are chosen to be 22 µF in this case for conducted EMI measurement. The high side (Q1, Q3) and the low side

(Q2, Q4) switches cannot be on simultaneously to avoid short circuit. To avoid the short circuit, the high side and the low side devices are turned on and off in alternative cycles. As such, two gate drivers are used to the turn on and turn off the high and the low side are complimentary to each other. The complementary gate signals to turn on and turn off the high side and the low side switches are generated from a Tektronix function generator (AFG 3102). In order to avoid short circuit by turning on the high and the low side switches together, a 10 ns dead time is assigned between the two complementary gate signals. An inductive load is used for the half-bridge inverter. The anti-parallel free-wheeling diodes provide current path continuity for the inductive load. The input DC voltage for this test is set at 30 V. The gate voltage of -5/+15 V is applied to the top and the bottom switches to turn on and turn off the devices at alternative cycles. The test is performed at 48% duty cycle.

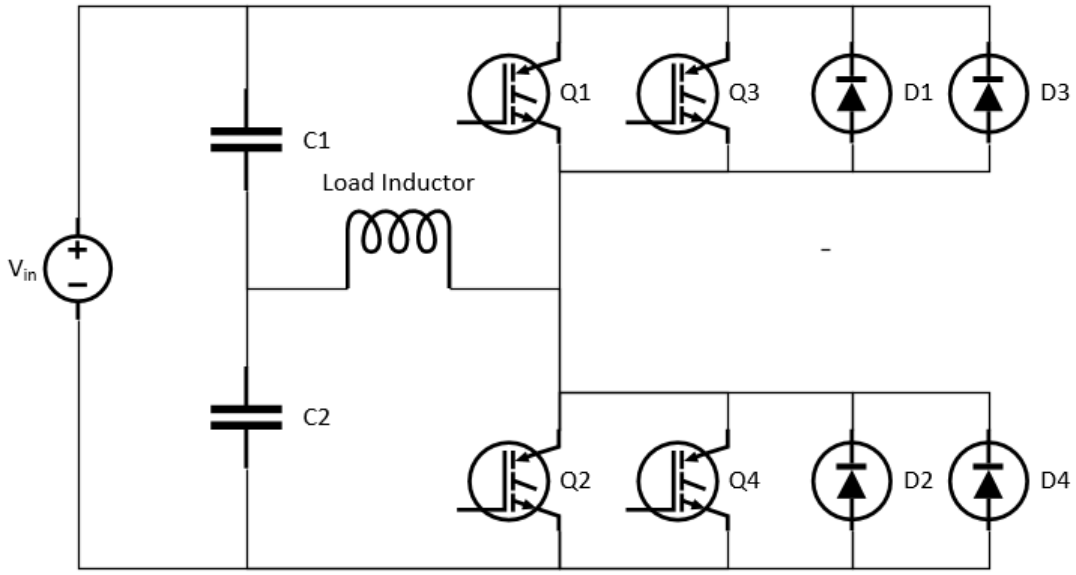

Fig. 6.14. Circuit schematic of a half-bridge inverter

The power devices are switched at different frequencies. Fig. 6.15 and Fig. 6.16 represent the inverter output voltage waveform of 3-D wire bondless half-bridge module and wire bonded half-bridge module respectively for 50 kHz switching frequency.

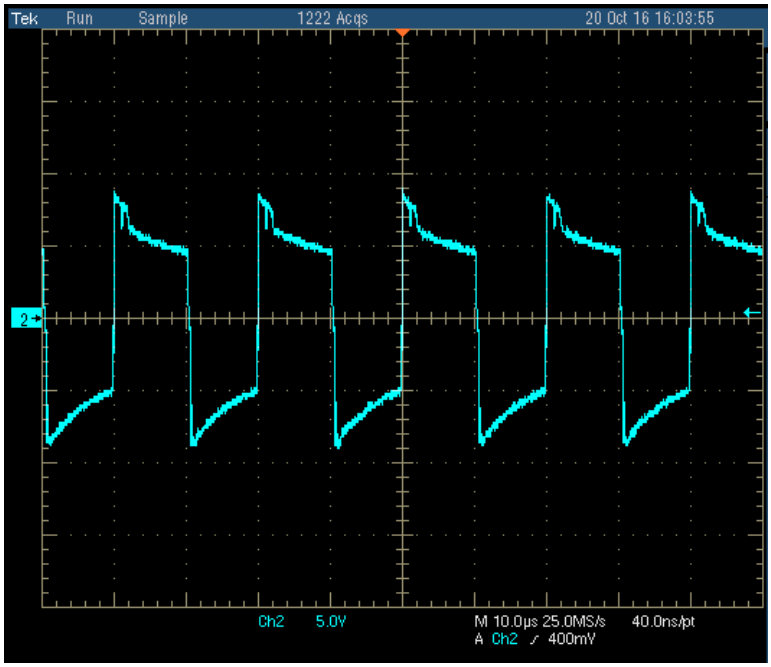

Fig. 6.15. Output voltage at 50 kHz switching frequency (3-D wire bondless half-bridge)

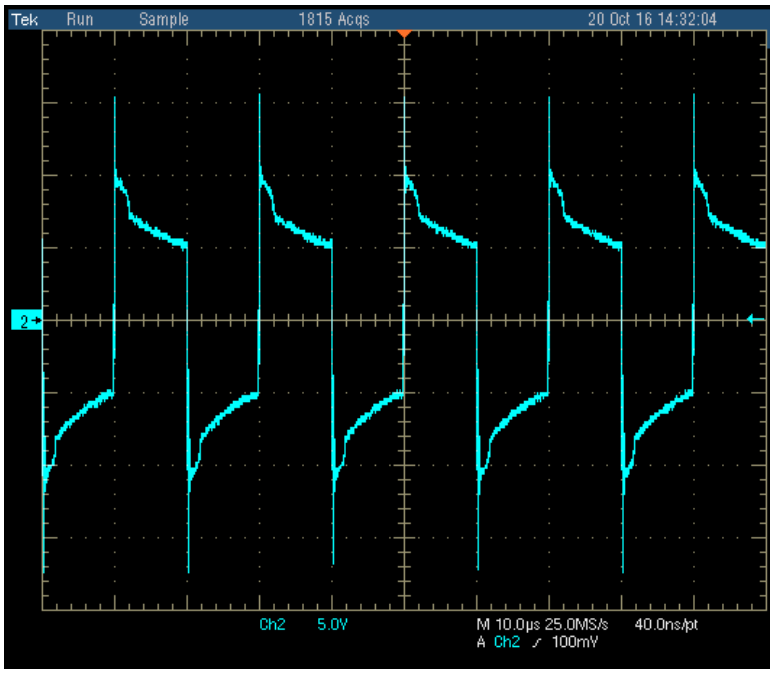

Fig. 6.16. Output voltage at 50 kHz switching frequency (wire bonded half-bridge)

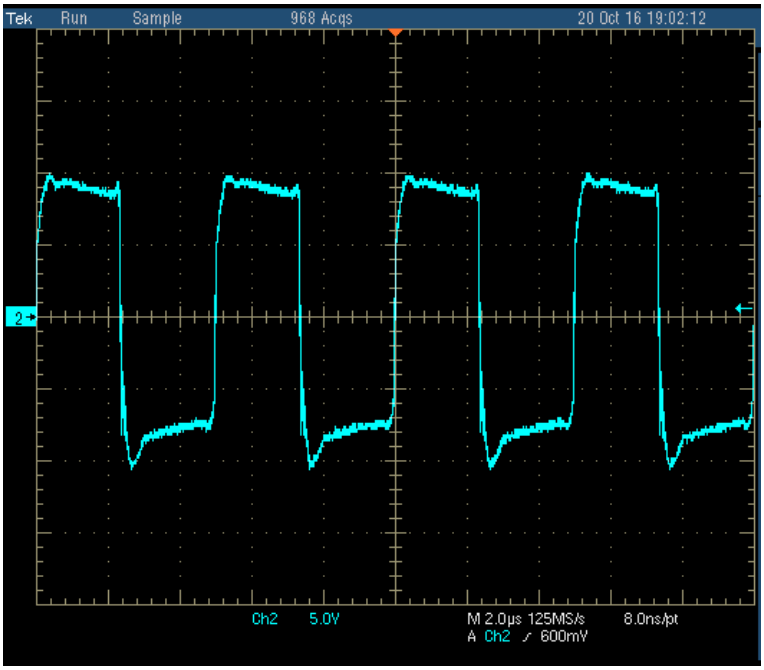

Fig. 6.17. Output voltage at 200 kHz switching frequency (3-D wire bondless half-bridge)

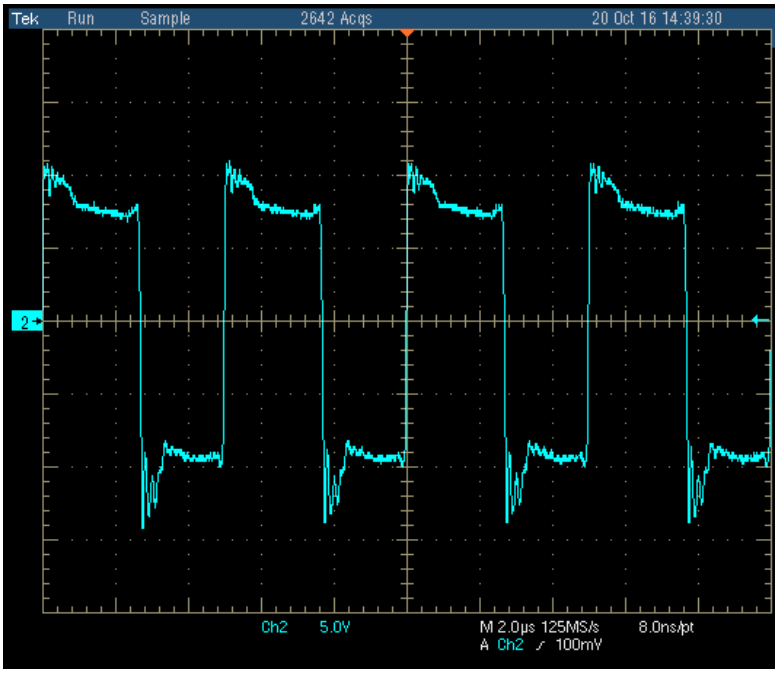

Fig. 6.18. Output voltage at 200 kHz switching frequency (wire bonded module)

Fig. 6.17 and Fig. 6.18 correspond to the inverter output voltage waveform of the 3-D wire bondless half-bridge and wire bonded half-bridge power module respectively for 200 kHz switching frequency. It is evident from Fig. 6.15, Fig. 6.16, Fig. 6.17 and Fig. 6.18, that the output voltage waveform for the 3-D wire bondless half-bridge inverter contains significantly lower ringing and overshoot compared to the wire bonded half-bridge inverter.

The conducted EMI measurement is performed using a line impedance stabilization network (LISN) in accordance with CISPR22 standards. The conducted EMI is generally measured between 150 kHz to 30 MHz frequency range. The LISN (ETS-LINDGREN, model-3810/2) used in the conducted EMI measurement has a frequency range from 9 kHz to 30 MHz. The LISN is generally a low pass filter that is used in between the power supply and the device under test to provide a stabilized line impedance of 50 Ω for conducted emissions measurement. It also helps eliminate the unwanted RF signals from the power supply to help reliable and repeatable conducted emissions measurements. To visualize the conducted EMI spectra a spectrum analyzer (Rigol DSA 815) is used. The output from the LISN is fed into the spectrum analyzer using a 50 Ω BNC cable. The conducted EMI is measured at different switching frequencies for both wire bondless and wire bonded half-bridge module to compare the conducted EMI response. Fig. 6.19, Fig. 6.20 and Fig. 6.21 corresponds to the total conducted EMI spectra comparison between the 3-D wire bondless half-bridge module and wire bonded half-bridge module at different switching frequencies of 50 kHz, 100 kHz and 200 kHz respectively. As can be seen from the comparison, the magnitude of the conducted EMI of 3-D wire bondless half-bridge power module is relatively lower compared to the wire bonded half-bridge module. Also, it can be observed from the comparison plots that most of the conducted EMI reduction is achieved in the 20 MHz-30 MHz range.

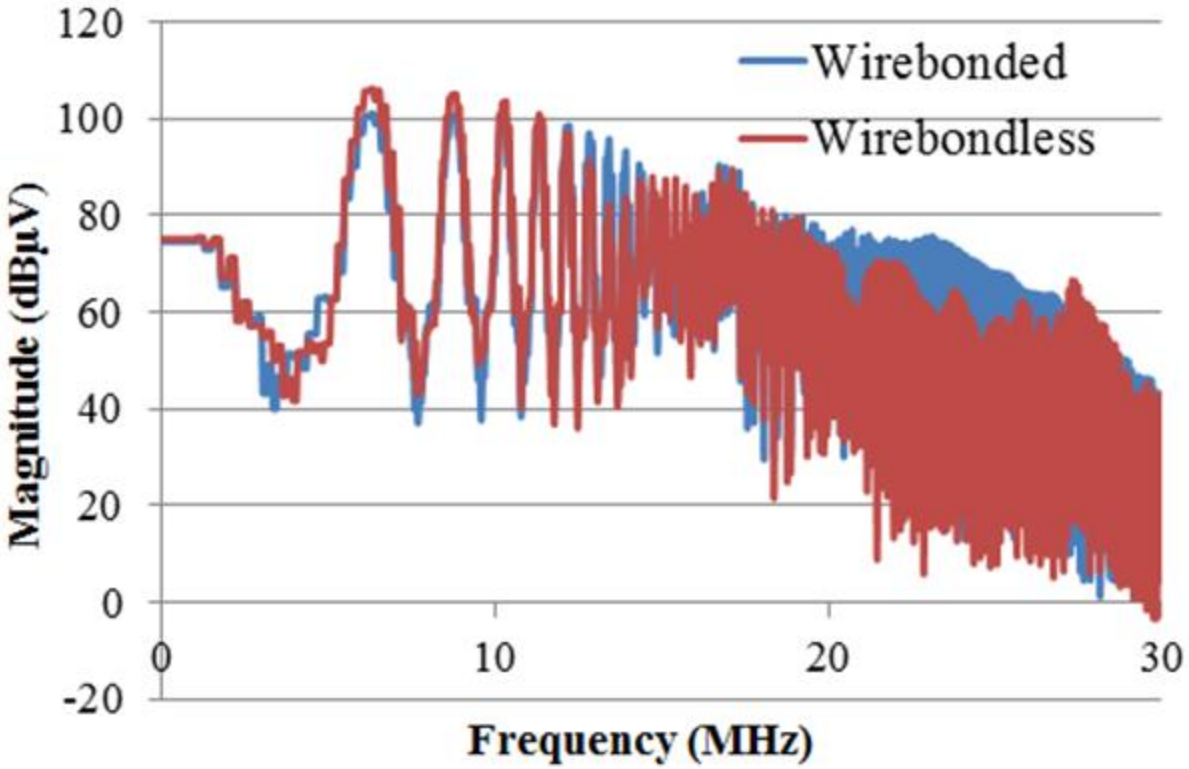

Fig. 6.19. Measured conducted EMI at 50 kHz [1]

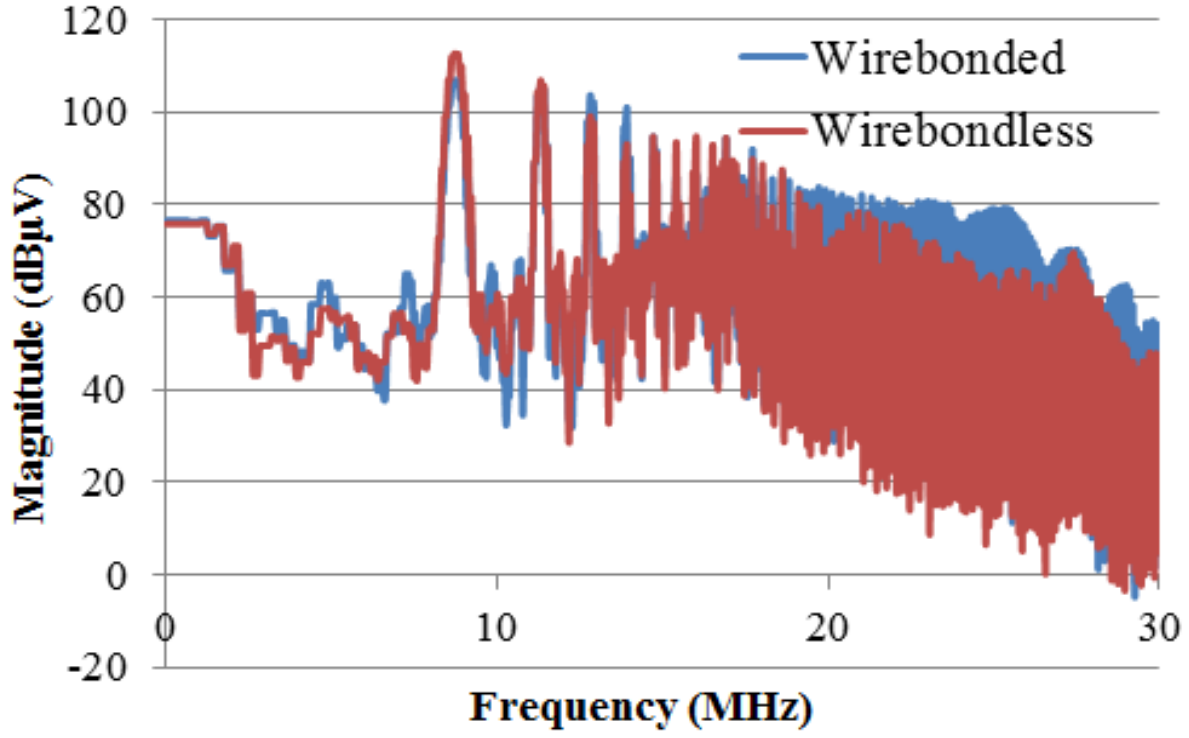

Fig. 6.20. Measured conducted EMI at 100 kHz [1]

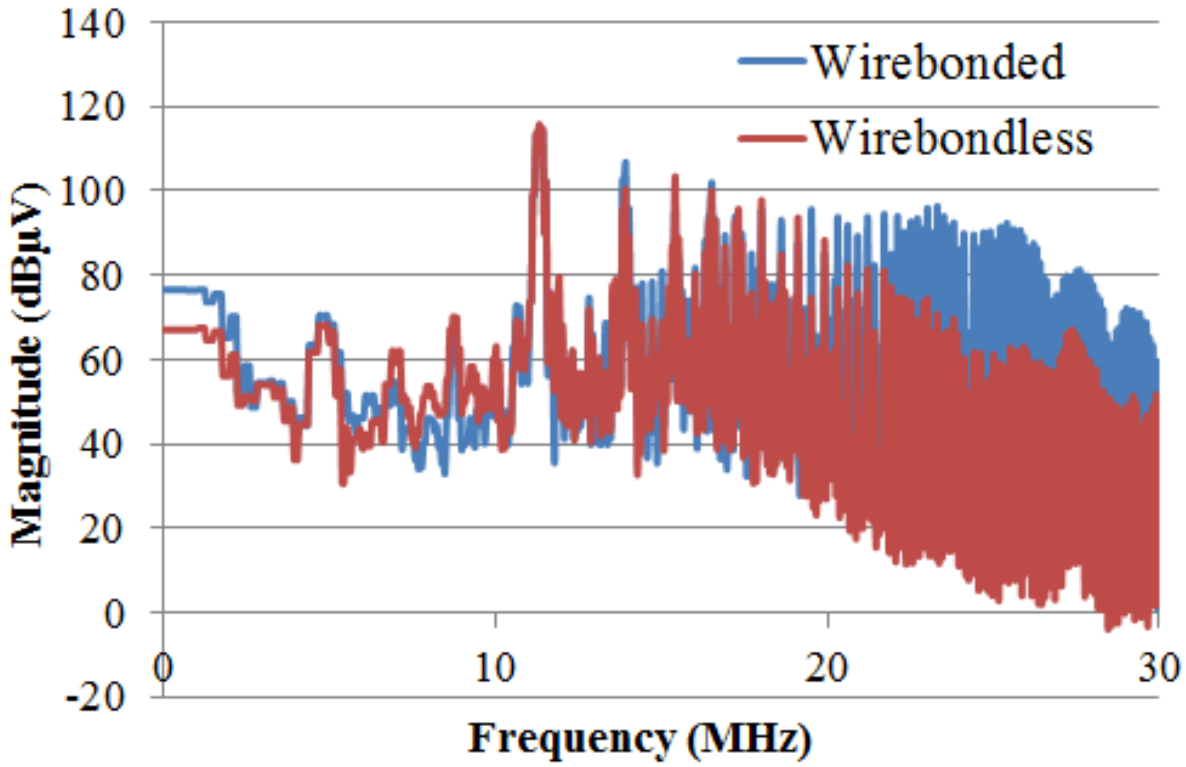

Fig. 6.21. Measured conducted EMI at 200 kHz [1]

6.4 Thermal Cycling Test

The reliability of the proposed 3-D wire bondless half-bridge power module largely depends on the reliability of the two stand-alone power modules that are interconnected to form the 3-D half-bridge stack. As such, the reliability of the stand-alone power modules is an important aspect that needs to be addressed. The thermal cycling reliability assessment test is performed to validate the proposed power module structure.

Two sets of dummy stand-alone power modules are fabricated to perform the thermal cycling test. One of the dummy modules prepared to perform the thermal cycling has all the terminals, i.e. gate, emitter and the collector, shorted. This module is prepared to observe if any delamination occurs during the thermal cycling. The shorting between all the terminals is verified using a multimeter prior to the start of the thermal cycles. The other dummy module

prepared for the thermal cycling test has all the terminals, i.e. gate, emitter, and collector, isolated from each other. This dummy module is prepared to observe if any shorting between the terminals occur during the thermal cycles. In order to fabricate the dummy power modules, Si dummy devices are prepared using the approach described in Chapter 5 in Section 5.2. One of the critical failure mechanisms is determined to be the approach taken to achieve the top surface metallization that is compatible and able to wet with the solder material as discussed in the section mentioned above. As discussed, the bottom side metallization of the devices from the manufacturers are Ti/Ni/Ag. In order to make the top side metallization compatible with the bottom side metallization, Ti/Ni/Ag is evaporated onto the gate and the emitter pads of the IGBT device and on the anode of the SiC Schottky barrier diode. This helps to reduce the CTE mismatch between the top and the bottom side metallization when the devices are attached using flip-chip die attach method. One of the main goal to perform the thermal cycling test is to verify if the top surface metallization holds up during the thermal cycles.

The temperature range for the thermal cycling is set from -45 °C to 125 °C. The dummy samples are placed inside an oven (DELTA 9023) as shown in Fig. 6.22. A thermocouple is placed near the dummy samples to monitor the temperature. Liquid nitrogen is used to achieve the lower end of the temperature i.e. -45 °C. The thermal cycling is carried out for 56 cycles to observe any shorting or delamination issues in the stand-alone dummy modules. After 56 cycles are completed, both the samples with shorted terminals and the isolated terminals are tested using a multimeter. It has been observed that the sample with isolated terminals remained isolated and the sample with shorted terminals remained shorted after 56 cycles.

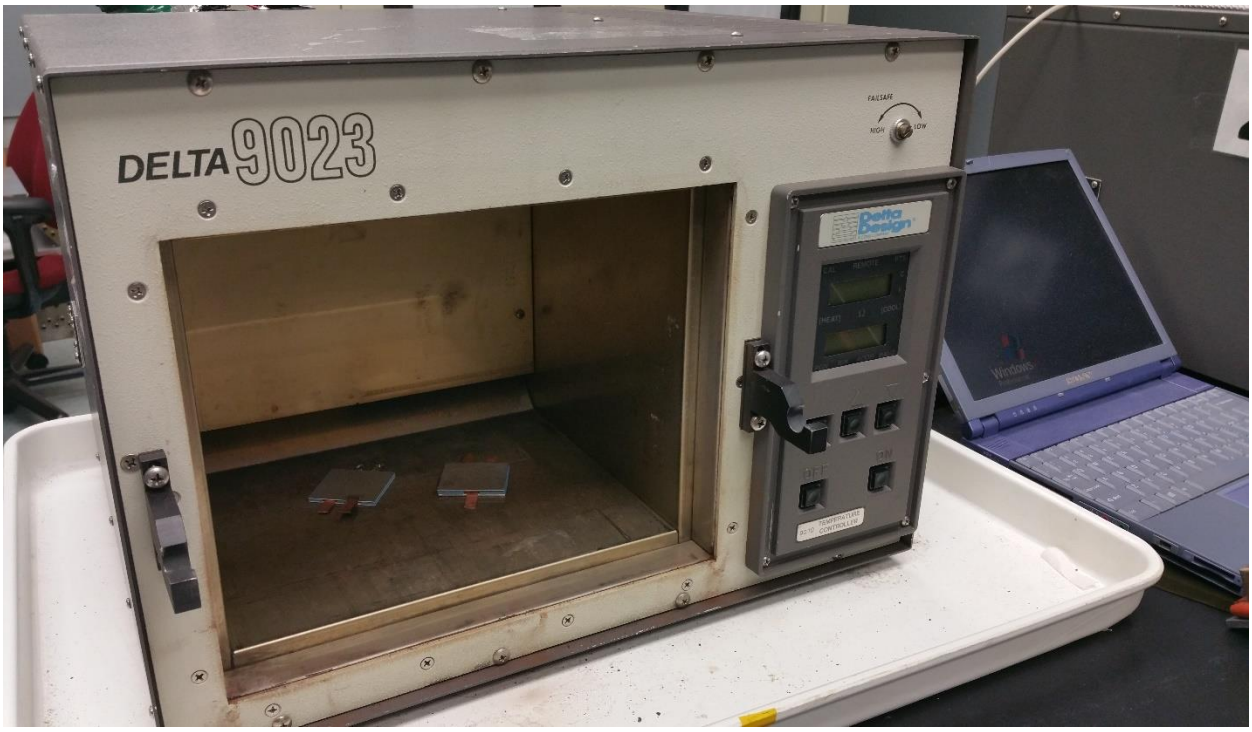

Fig. 6.22. Samples placed inside oven for thermal cycling experiment

6.5 Leakage Current Measurement

Leakage current measurement is performed to verify the influence of packaging approach on the leakage current of the power module package and validate the power module structure. In order to carry out leakage current test, Si dummy devices are prepared and packaged following the process presented in Chapter 5. A high voltage DC power supply (GLASSMAN FC Series) is used to carry out the leakage current test. In order to avoid any electrical hazard, the power modules under test are kept inside an enclosed DELTA oven as shown in Fig. 6.23. The current limit for the dielectric isolation test is set at 1 mA. The measurement is performed at room temperature. The leakage current is monitored using National Instrument's data acquisition system (DAQ) that is connected and configured with the high voltage DC power supply. The data acquisition system is configured to monitor leakage current using LABVIEW software interface using a computer. Fig. 6.24 represents the LABVIEW interface to perform data

acquisition for the test. In order to monitor the voltage and corresponding leakage current, two channels on the DAQ system are used. In this case, channel 1 is used for monitoring the voltage levels and channel 3 is used to monitor the current levels. The DAQ system converts the current levels to voltage levels using a 249 Ω shunt resistor across the channel input and the ground reference. As such, the data acquisition for the current levels is performed as voltage levels across the 249 Ω shunt resistor. The current levels through the device under test can be found by converting the voltage to a current by dividing the channel 3 DAQ voltage values by the shunt resistor using Ohm's law.

Fig. 6.23. Leakage current measurement setup

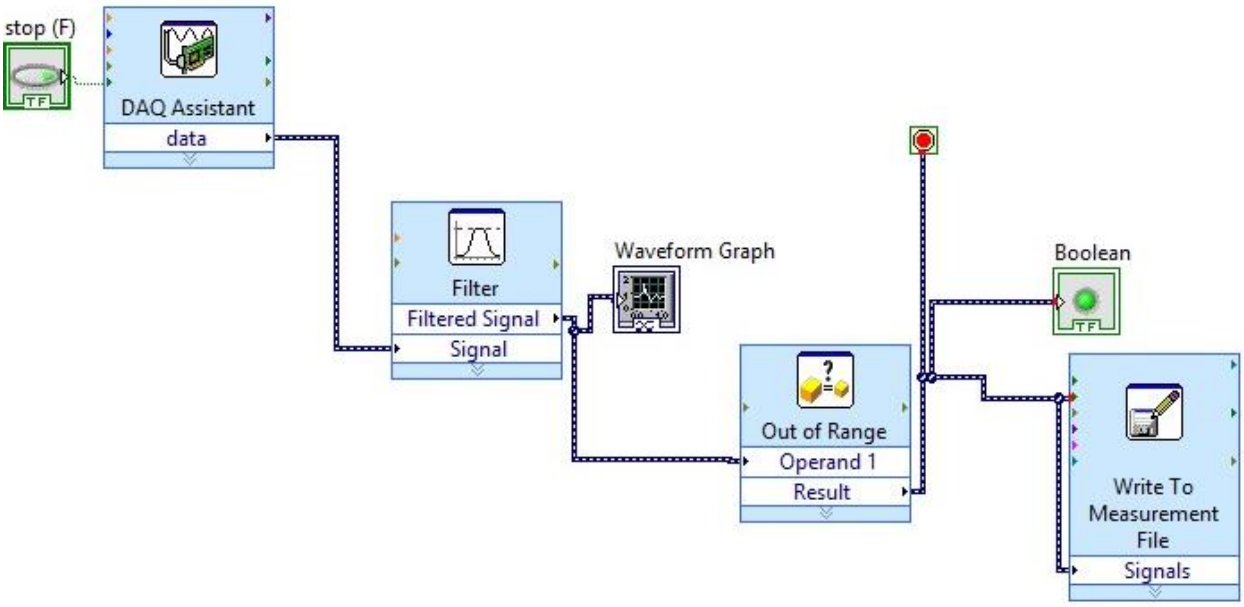

Fig. 6.24. LABVIEW interface to facilitate data acquisition using a DAQ system

A known resistor of 1 MΩ is used to calibrate the DAQ with the voltage levels of the high voltage power supply. The steps used to calibrate the voltage levels of DAQ corresponding to the high voltage power supply is provided below.

i. First, a known resistor with 1 MΩ value is connected between the positive and the negative leads of the high voltage power supply.

ii. The DAQ is connected to the voltage and current monitor pins of the high voltage power supply using pin headers.

iii. An USB cable is connected between the computer and the DAQ to transfer data.

iv. A LABVIEW interface is created to perform data acquisition

v. A comparator block diagram is used in the LABVIEW interface to set the threshold voltage with a loop condition. The loop condition is set such that if the voltage level of the high voltage power supply drops under a certain threshold that is pre-defined in the comparator block diagram in the LABVIEW interface, the data acquisition will stop.

vi. To start the data acquisition, the threshold of the comparator block is set at a lower level than the voltage level at the high voltage power supply.

vii. Once the data acquisition starts, the voltage level of the high voltage power supply is lowered gradually until it reaches the threshold set in the comparator block in the LABVIEW interface and the data acquisition stops. These two values, one from the high voltage power supply and the other one from the predefined threshold in the LABVIEW interface, are recorded. As such, the instant the data acquisition stops, the voltage level in the high voltage power supply corresponds to the predefined threshold set in the comparator block of LABVIEW interface.

viii. The upper threshold for these two values is also set following the same steps.

ix. The threshold point for various voltage levels in the range of 600 V to 2.2 kV is recorded. Table 6.2 lists the voltage levels of the high voltage power supply and the corresponding calibrated DAQ voltage threshold level.

Table 6.2 Calibrated voltage levels between high voltage power supply and DAQ voltage

Voltage level in high voltage power supply	Threshold voltage in DAQ
600 V	0.3 V
1.2 kV	0.6 V
1.6 kV	0.8 V
1.8 kV	0.9 V
2.0 kV	1.0 V
2.1 kV	1.1 V

After the calibration between the DAQ and the high voltage power supply is performed using a known resistor, the power module is connected to do the leakage current measurement test. The leads from the high voltage DC power supply is connected between the emitter and collector leads of the power module. The leakage current associated with the packaging is monitored at different voltage levels. The voltage levels are varied from 600 V to 4.5 kV range. Fig. 6.25 plots the DAQ voltage levels for channel 1 at different power supply voltages. The module under test is kept at each voltage level for 30 minutes to verify if there are any major fluctuations in voltage level. However, no major fluctuations in voltage level are observed up to 4.5 kV DC supply voltage. Fig. 6.26 corresponds to the channel 3 voltage levels across the 249 Ω shunt resistor of the DAQ system as discussed earlier. As channel 3 is monitoring the current levels through the power module, Ohm's law is implemented to convert the channel 3 voltage levels to current by dividing the channel 3 voltage by the shunt resistor. As can be seen from Fig. 6.26, the voltage across the shunt resistor is almost similar for DC supply voltages up to 4.5 kV. The peak channel 3 voltage is 0.2 mV approximately which corresponds to 0.8 μA of leakage current, which can be deemed as very negligible. As such, it can be concluded that the module is able with withstand 4.5 kV voltage without any breakdown.

The leakage current measurement is also performed using an automatic HIPOT tester (Valhalla Scientific, Model: 5880 A) to verify the test results found using the above-mentioned method. The high voltage isolation test is setup by defining different voltage levels. The current limit is set to 1 mA. The test duration is set for 30 seconds at each voltage level. The test is performed starting at 600 V all the way up to 4.5 kV. The HIPOT test also yielded no breakdown of the power module.

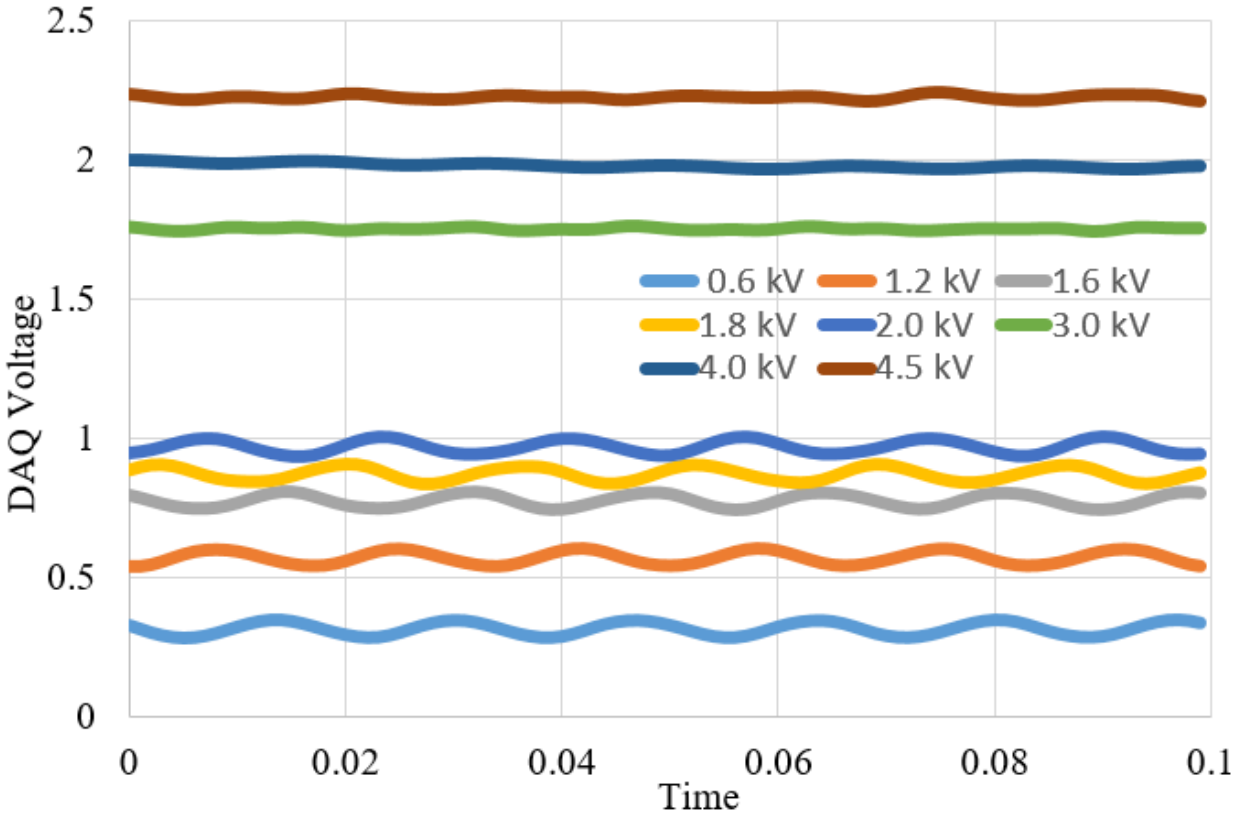

Fig. 6.25. Data acquisition system voltage levels of channel 1 in LABVIEW interface for corresponding high voltage DC supply

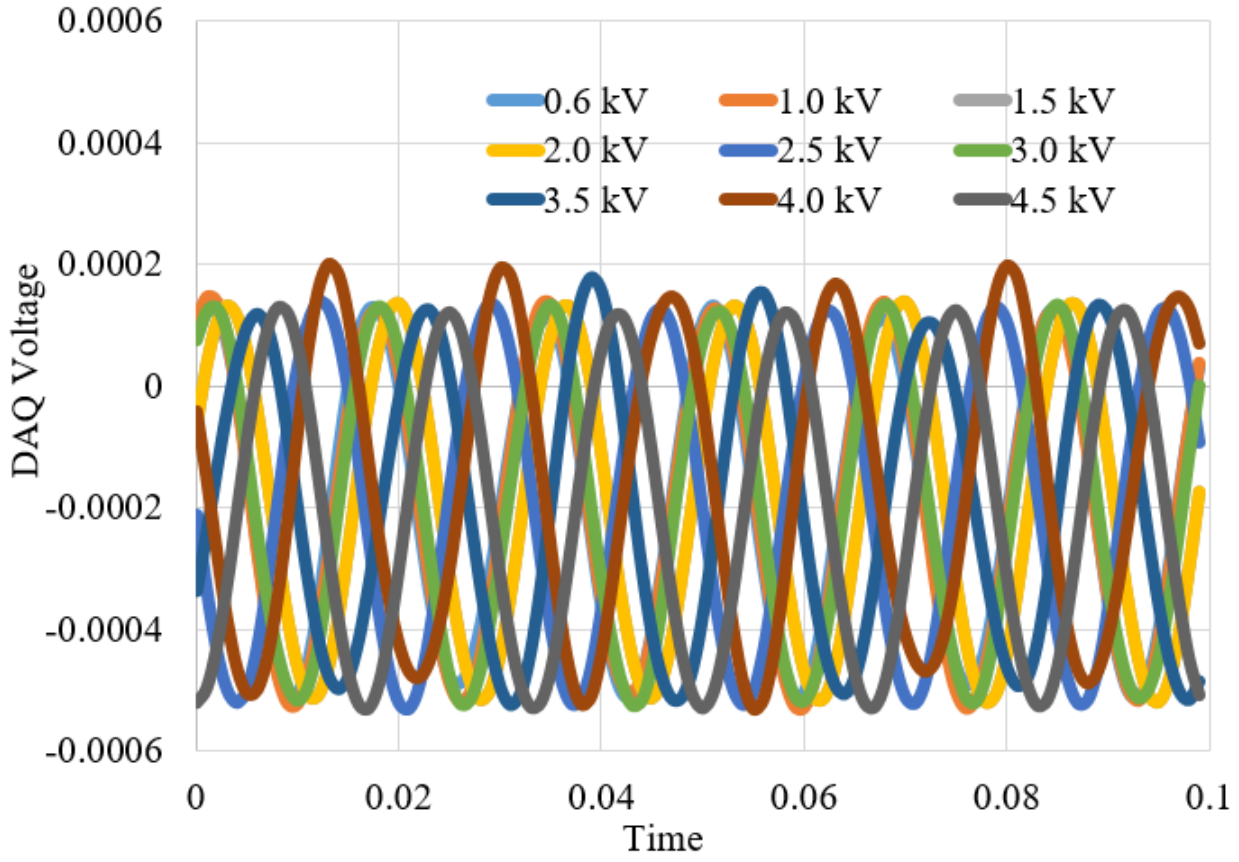

Fig. 6.26. Data acquisition system voltage levels of channel 3 (across 249 Ω shunt resistor) in LABVIEW interface corresponding to high voltage DC supply

6.6 Chapter Summary

In this chapter, characterization of the 3-D wire bondless half-bridge stacked power module is performed. The switching characteristics of the 3-D wire bondless half-bridge power module are compared to a traditional wire bonded half-bridge power module. It has been determined using double pulse test that the 3-D wire bondless power module exhibits less ringing, overshoot and shorter settling time for switching transients both at turn-on and turn-off for the 3-D wire bondless half-bridge stack. The static characteristics of the devices are measured after packaging to investigate the package influence on device characteristics. An increase in on-resistance for the Si-IGBT devices is observed. However, this can be attributed to the fact that the LTCC

metallization has higher resistance. As LTCC is used as a die carrier in the proposed design, further developments can be performed in terms of reducing the on-state resistance by implementing improved metallization on LTCC such as electroplating copper on LTCC. Electromagnetic interference measurement is performed using an LISN for both 3-D wire bondless half-bridge stack and the traditional wire bonded half-bridge module. Significant reduction in the magnitude of the EMI spectra is observed for the wire bondless stack compared to the wire bonded module. Thermal cycling of the power modules is performed in the range -45 °C to 125 °C to investigate any delamination and shorting issues to validate the module structure. The power module is also tested for leakage current at voltage level up to 4.5 kV. It has been observed that the leakage current for the proposed packaging approach is negligible up to 4.5 kV.

6.7 References

[1] Atanu Dutta, Simon Ang, “Effects of parasitic parameters on electromagnetic interference of power electronic modules,” *in 2017 IEEE Applied Power Electronics Conference and Exposition,* 2017

Chapter 7 Electromagnetic Interference Simulations for Wide Bandgap Power Electronic Modules

Chapter 7 consists of a published IEEE paper with the following citation:

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doi: 10.1109/JESTPE.2016.2573315

Electromagnetic Interference Simulations for Wide Bandgap Power Electronic Modules

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***Abstract*— A simulation methodology that incorporates co-simulation techniques using ANSYS EM tools is proposed to predict radiated and conducted electromagnetic interference (EMI) from power electronic modules. The radiated EMI for a coplanar wire bonded and wire bondless power electronic modules are simulated and compared. The instantaneous power levels conducting through the power devices in the wire bonded power module are significantly higher than those for the wire bondless power electronic module due to parasitic circuit element imbalance. These power levels occur for a very short duration at the turn-on and turn-off of the devices and can be considered as a potential source of radiated EMI emissions. Through the co-simulation technique, it is shown that the wire bondless power electronic module has a better EMC compliance**

compared to that of the coplanar wire bonded power electronic module. Conducted EMI measurements and simulations are also performed to predict the conducted EMI and validate the simulation methodology. The proposed co-simulation technique can be implemented during the initial design phase of power modules to reduce significant time to physically test module-level EMC/EMI.

***Index Terms*—Power electronic modules, electromagnetic interference, simulation methodology.**

7.1 Introduction

Fast switching, power dense, compact power electronic modules or power modules are in great demand for modern power electronic systems. In these power modules, wide bandgap power semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN), are increasingly being used for efficient fast switching and continuous operation at high temperatures. Recently, many research efforts are focused to understand the characteristics of these devices as well as utilize these fast switching devices in high power density modules for various applications [1]-[12]. Because of the high dv/dt and di/dt slew rates in these wide bandgap power semiconductor devices, they generate significant electromagnetic compatibility (EMC) concerns [13]-[15]. As such, it is necessary in the early design phase of these power modules to address electromagnetic interference (EMI). Mitigation of EMI in power converters using improved layout techniques has been discussed in [13], [16]-[18]. Various mathematical and numerical modeling approaches have been reported to understand EMI sources and generation mechanisms to predict both conducted and radiated EMI in power convert systems in [29]-[33]. However, their approaches

are limited by overly simplified device models and circuit approximations which eventually prevent precise prediction of EMI. The simulation methodology proposed in this paper directly addresses both radiated and conducted EMI, taking into consideration the non-ideal transient characteristics during the switching operation and corresponding power levels through each device. Typically, the EMI/EMC test for the power module is performed after the physical prototyping of the power module in an anechoic chamber [14]. Physical prototyping of the power modules to test for EMI issues can be a very long and costly engineering process. As such, a coherent simulation methodology to predict the EMI issues early in the design process is desired. In this paper, a simulation methodology that incorporates co-simulation techniques using ANSYS EM tools is proposed to predict the radiated and conducted EMI. The proposed simulation methodology is validated using radiated and conducted EMI measurements using a simple near-field measurement technique with near-field electromagnetic (EM) probes and line impedance stabilization network (LISN).

The magnitude of the current conducting through the physical traces during switching operation, parasitic circuit elements, and physical characteristics of the power semiconductor devices are important parameters that govern the switching characteristics of the power device [19]-[20]. These parameters are also important considerations to predict the EMI in a power module. The proposed simulation methodology commences with a static current conduction simulation on the power module layout using ANSYS MAXWELL [26]. Subsequently, a frequency dependent parasitic extraction of the physical traces on the power module is performed using ANSYS Q3D extractor [28]. The frequency dependent parasitic model is then dynamically linked to ANSYS SIMPLORER. Using physical model characteristics from device manufacturer's data sheet, the electrical characteristics of the power semiconductor device are re-produced using ANSYS

SIMPLORER's built-in semiconductor device characterization tool [27]. A frequency dependent parasitic model based circuit schematic of the power module is then constructed. From ANSYS SIMPLORER, the waveforms from transient simulations are then imported to ANSYS HFSS [28] to perform a full wave 3-D electromagnetic field simulation to analyze the radiated EMI. Furthermore, conducted EMI simulation is performed in ANSYS SIMPLORER incorporating the LISN model. The time domain line voltages of the LISN are recorded and mathematically converted to frequency domain using Fast Fourier Transform (FFT) in MATLAB. A flow chat of the simulation methodology is shown in Fig. 7.1.

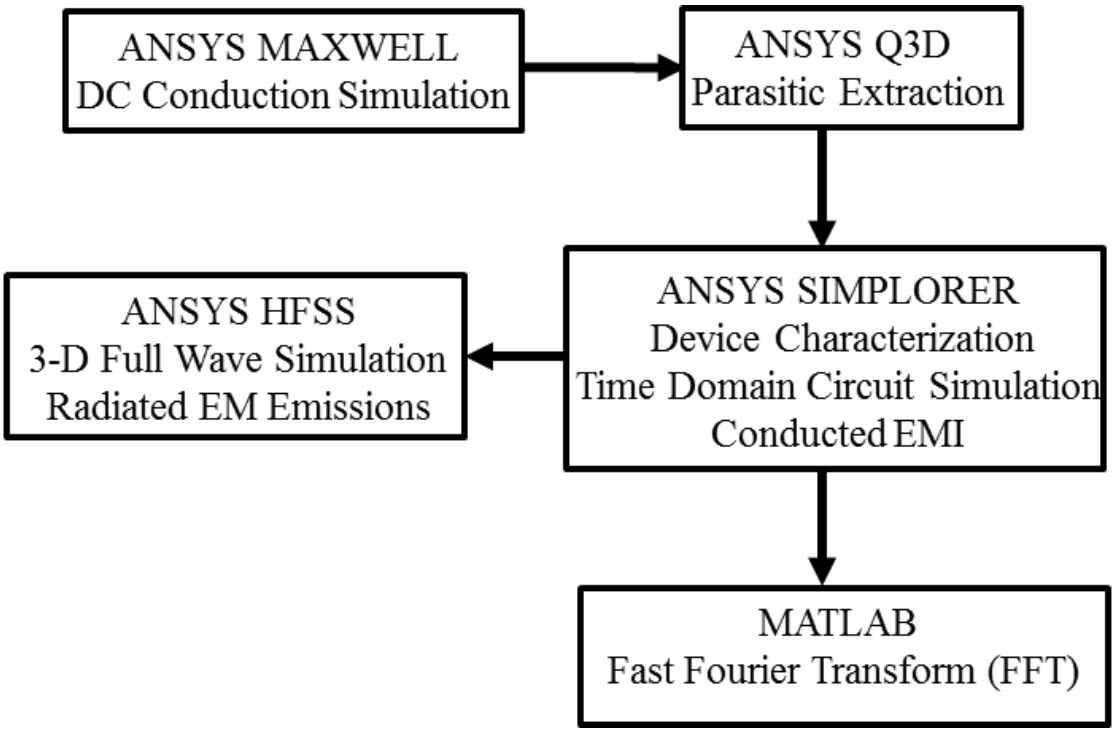


Fig. 7.1. Flow chart of the simulation methodology

7.2 Design and Layout of Power Module

To illustrate the simulation methodology, a simple power module of a single switching position of a half-bridge topology consisting of three 1200 V 36 A power MOSFETs (CREE part number CPM2-1200-0080B) in parallel with three 1200 V 20 A antiparallel SiC Schottky barrier diodes (CREE part number CPW4-1200-S020B) is used. Fig. 7.2 (a) and (b) show the layout of a coplanar wire bonded and wire bondless power modules, respectively. In the wire bonded power module, the power MOSFETs and the anti-parallel Schottky barrier diodes are positioned side by side as shown in Fig. 7.2 (a). The overall dimensions of the coplanar wire bonded power module are 19.5 mm × 34 mm. Electrical connection is achieved using multiple 127 μm aluminum wire bonds to increase the current handling capability and to reduce the parasitic inductance of the current path. For the wire bondless power module shown in Fig. 7.2 (b), the copper plate of the upper direct bond copper (DBC) substrate provides the electrical connection between the source, drain, and gate of the power devices through solder balls. The positive power supply (DC+), ground (GND), and the gate terminals are extended outside the power module to facilitate easier access to the input/output terminals. The overall module dimensions of the wire bondless power module are 19 mm × 19 mm. As can be seen, the overall module size for the wire bondless power module is reduced by 45% compared to that of the wire bonded power module. The reduction of the overall module size plays a significant role in reducing the parasitic inductance [21], which in turn, reduces EMI by reducing the switching noise of the power modules. The wire bondless power module can be designed to facilitate top and bottom current carrying conductors to cancel the magnetic fields by the opposing current directions to reduce electromagnetic emissions [22]-[23]. However, this is not easily accomplished for the wire bonded power module.

7.3 Static Current Distribution Analysis

Static current conduction simulation for the two module structures are performed using ANSYS MAXWELL. The DC conduction simulation is performed to understand the current density distribution on the power modules. For DC conduction simulation, a 60 A current excitation is assigned to the DC+ terminal. The current path is defined from the DC+ terminal to the GND terminal, which acts as the current sink. The power MOSFETs and the antiparallel diodes are assumed to be switched on and off alternatively. Fig. 7.3 (a) and (b) show the current density of the wire bonded and wire bondless power modules, respectively. As can be seen from the current density simulation of Fig. 7.3 (a), the power device MOSFET3 has the highest current density compared to the other two MOSFETs in the layout. Also, MOSFET2 has a higher current density compared to that of MOSFET1. This imbalance in current density can be explained by the proximity effect of the power devices to the DC+ terminal.

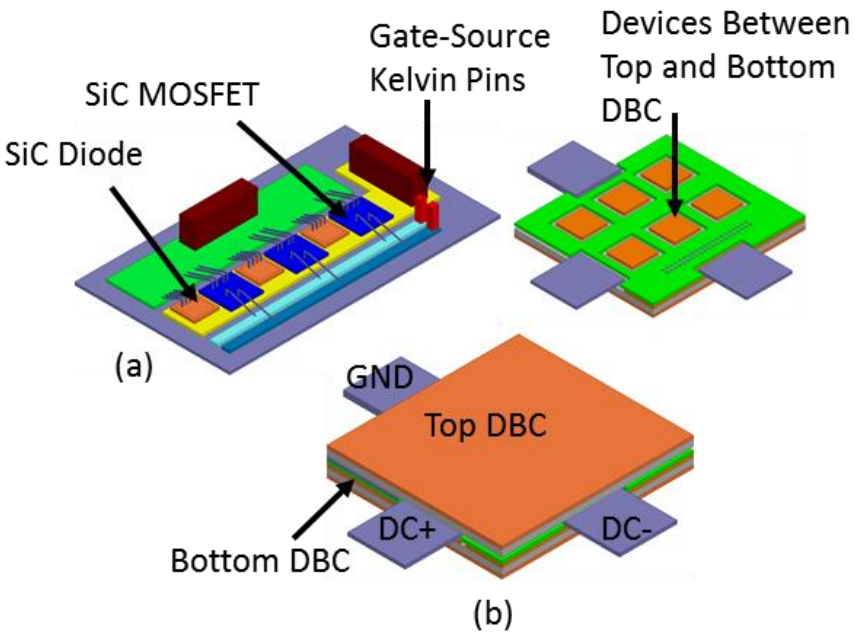


Fig. 7.2. (a) Coplanar wire bonded power module, (b) Wire bondless power module

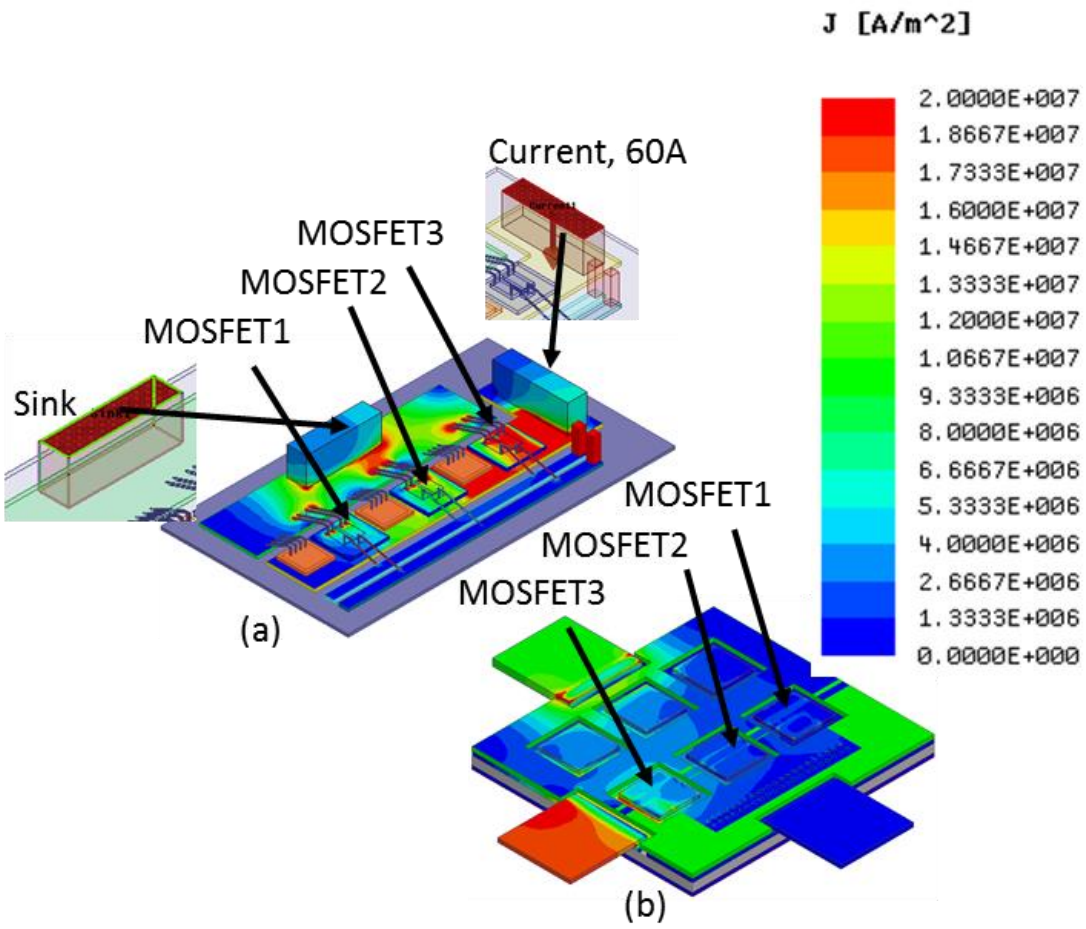


Fig. 7.3. DC conduction simulation (a) Wire bonded module (b) Wire bondless module

As can be seen from the current density plot of Fig. 7.3 (b), MOSFET3 has a slightly higher current density compared to MOSFET2 and MOSFET1, whereas, MOSFET2 and MOSFET1 have approximately similar current density distribution. As such, the imbalance in current density in the wire bondless module is reduced compared to that in the wire bonded power module**.** The imbalance in current density has a direct impact of the power levels through each of the devices in power module, which will be evident from the power level simulations.

7.4 Parasitic Extraction

The parasitic extraction for the power module is performed using ANSYS Q3D. To perform the parasitic extraction simulations, various current conducting nets are assigned in accordance with the switching sequence of the power module. For our case study, i.e., for a switching position with three MOSFETs in parallel, there are primarily three conducting nets that are of interest, the DC+, GND, and the gate-source loop nets. Fig. 7.4 and Fig. 7.5 show the conducting nets for the wire bonded and wire bondless power modules, respectively. The DC+ conducting nets in Fig. 7.4 (a) and Fig. 7.5 (a) consist of the inductance paths from the DC+ terminal to the drain of the SiC power MOSFETs and the cathode of the Schottky barrier diodes. The GND nets consist of the inductance paths from the source of the MOSFET to the GND terminal as shown in Fig. 7.4 (b) and Fig. 7.5 (b). The gate-source loop inductance is divided into two parts, one going from the gate of the devices to the Kelvin gate terminal and the other from the source of the power MOSFETs to the Kelvin source terminal. After assigning the desired conducting nets, a frequency sweep is performed to extract the frequency dependent parasitic inductance. The frequency of interest for the frequency sweep is determined by the rise time of the time domain signal. The SiC power MOSFETs have a rise time of 31 ns (t_r+$t_{d(on)}$) according to the datasheet provided by the manufacturer. For a time domain waveform with a rise time of 31 ns, we assume 6 samples within that time step are required to fully capture the signal in the frequency domain. So the maximum frequency sweep for the parasitic is:

$$F_{Max} = \frac{1}{5.16\ ns} = 200\ MHz \qquad (7.1)$$

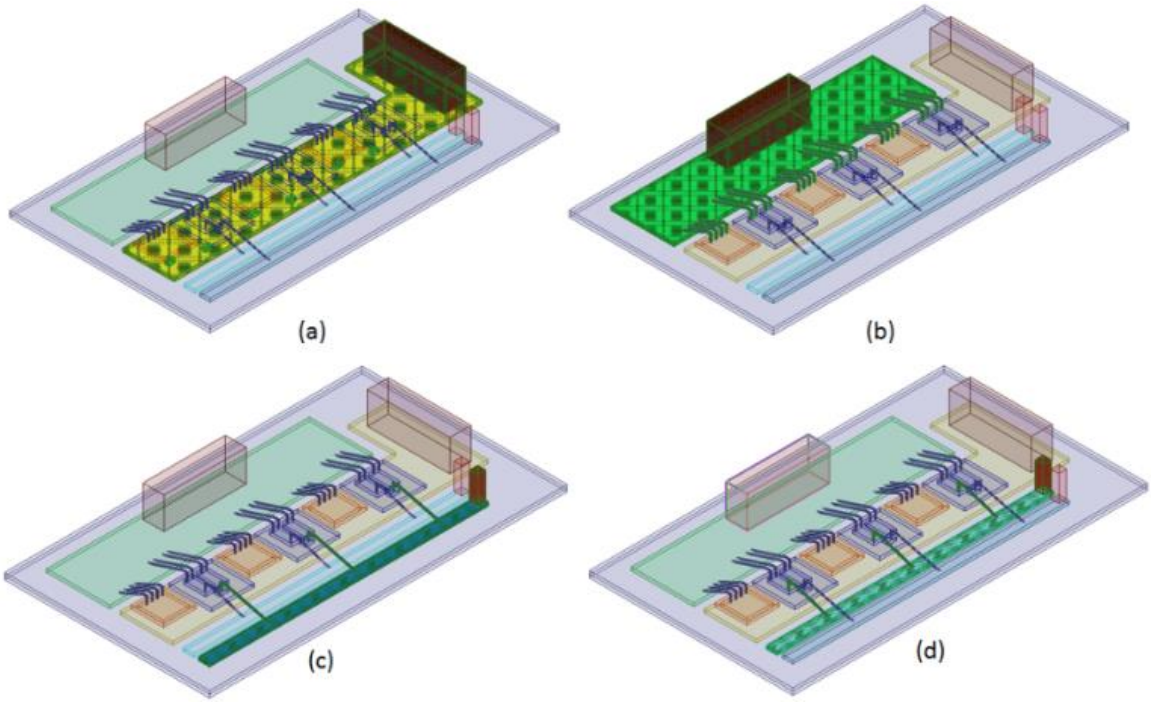


Fig. 7.4. Conducting nets in ANSYS Q3D for parasitic analysis (coplanar wire bonded module)

The parasitic inductance for the wire bondless power module is significantly less over the frequency range for all the assigned nets compared to that of the co-planar power module. The effect of these parasitic inductances on the switching performance of the power devices will be discussed in section VI of this paper.

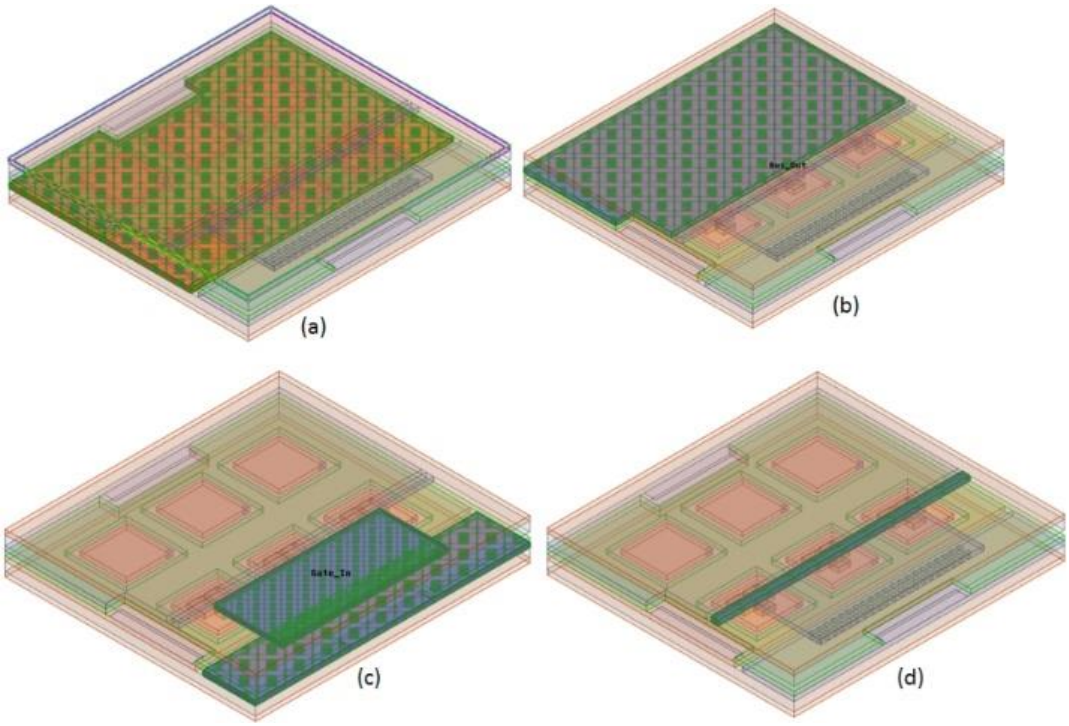


Fig. 7.5. Conducting nets in ANSYS Q3D for parasitic analysis (wire bondless module)

7.5 Device Characterization

The transient response, voltage and current overshoots, of the power devices during turn-on and turn-off primarily contribute to electromagnetic interference. As such, ANSYS SIMPLORER simulations are performed to understand the transient behaviors of these switching devices. A frequency dependent parasitic model (RLC) of the device is imported and dynamically linked from ANSYS Q3D to construct the circuit schematic of the power module in ANSYS SIMPLORER. The devices used to build the power module are characterized using the SIMPLORER's device characterization tool with parameters from the manufacturer's data sheet. ANSYS SIMPLORER's dynamic semiconductor characterization tool takes the dynamic measurement and nominal operating point conditions as inputs [27]. CREE's 1200 V 36 A power

MOSFETs (CPM2-1200-0080B) and 1200 V 20 A Schottky barrier diodes (CPW4-1200-S020B) are used in this study. The transfer and output characteristics are then fitted in SIMPLORER against several data points obtained from the data sheet of the device.

7.6 Circuit and System Simulation

After the device characterization, the circuit schematic of the power module is constructed for the frequency dependent parasitic model using the characterized power devices in SIMPLORER. To test the transient switching behaviors of an inductive switching, a test circuit is constructed for the power module with circuit parasitics. Fig. 7.6 shows the simplified circuit schematic for the switching simulation. The input DC voltage for the simulation is chosen to be 800 V. The inductive load for the inductive switching test is chosen to be 142 μH, which is the same value given in the manufacturer's datasheet for the inductive test circuit condition. The duty cycle and the switching frequency for the simulations are 50% and 50 kHz, respectively.

Fig. 7.7 (a) shows the frequency dependent parasitic model that is imported from ANSYS Q3D while Fig. 7.7 (b) shows the circuit model derived from the parasitic model used to study the switching behaviors of the power modules. As can be seen form Fig. 7.7 (b), the three paralleled MOSFETs and the three antiparallel diodes are all connected to the different pins in the parasitic model. The inductive load, DC supply, and the gate driver circuitry are added to complete the switching system. To obtain the drain current, drain-source voltage and the instantaneous power waveforms through the power devices at turn-on and turn-off, a watt meter is connected to each of the power MOSFETs as shown in Fig. 7.7 (b).

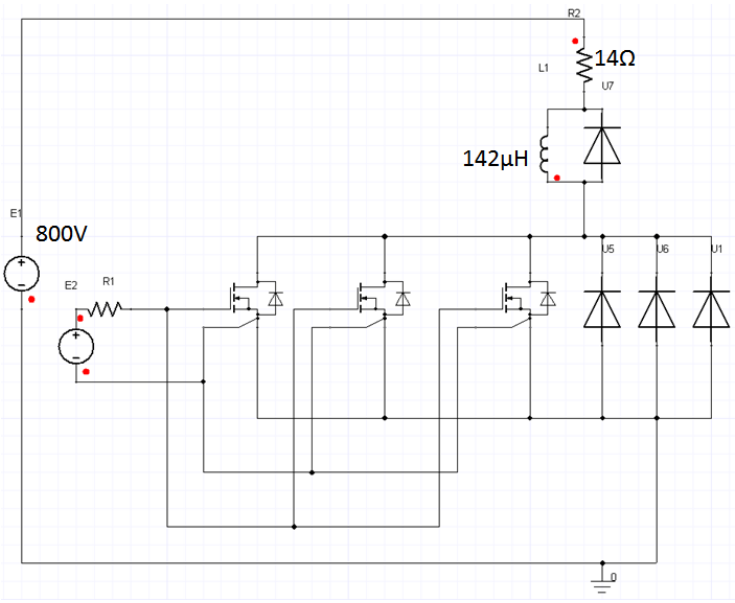


Fig. 7.6. Circuit schematic for switching simulations (without parasitc inductance)

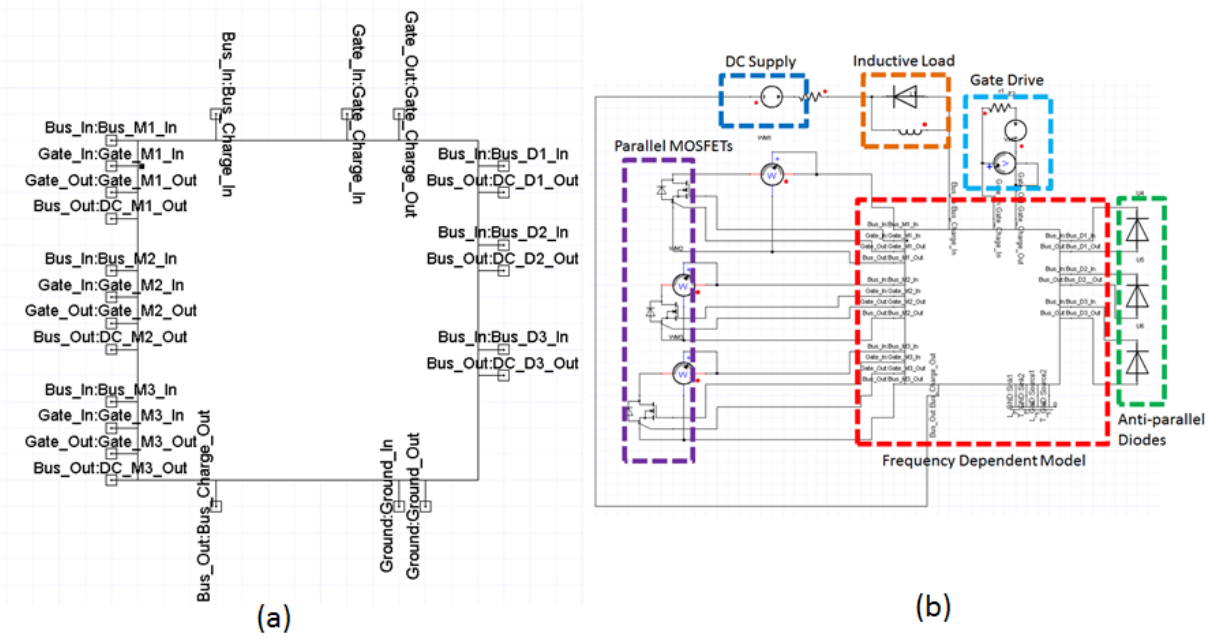


Fig. 7.7. (a) Frequency dependent circuit model, (b) Circuit schematic built around frequency dependent parasitic model

Fig. 7.8 and Fig. 7.9 show the instantaneous power levels conducting through the MOSFETs at a single switch-on instance for the wire bonded and wire bondless power modules, respectively. As can be seen from the power level plot in Fig. 7.8, MOSFET3 carries the highest power level compared to those of MOSFET2 and MOSFET1, which is consistent with the DC conduction simulation performed in section III. As shown, an instantaneous power of 17.5 kW is conducting through MOSFET3 in the wire bonded power module for a very short duration of time at the turn-on of the device and can be considered as a potential source of EMI. The instantaneous power levels conducting through the devices in the wire bonded power module are significantly higher than those in the wire bondless power module as shown in Fig. 7.9.

In order to understand the radiation behaviors of the power module, time domain instantaneous power waveforms are converted to frequency domain waveforms using FFT. Fig. 7.10 (a) and (b) show the spectral power distribution of the time domain instantaneous power waveform for a single switching (turn-on) instance for the wire bonded and wire bondless power modules, respectively. From these spectral plots, it can be observed that most of the higher power level frequencies are between 10-200 MHz, whereas, the power level above 200 MHz is very small.

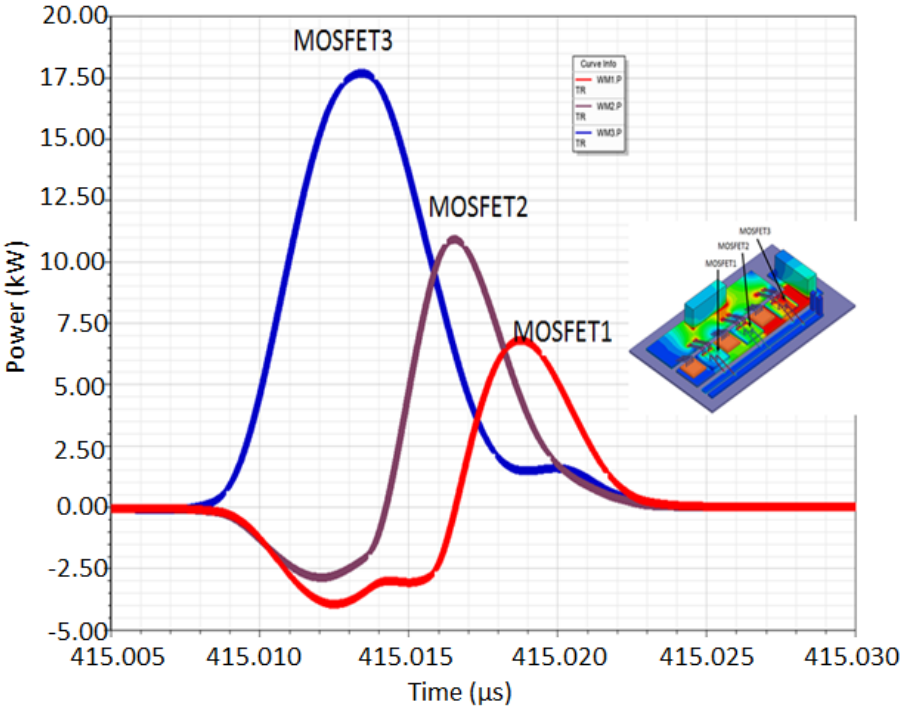


Fig. 7.8. Instantaneous power through paralleled power MOSFETs (coplanar wire bonded module)

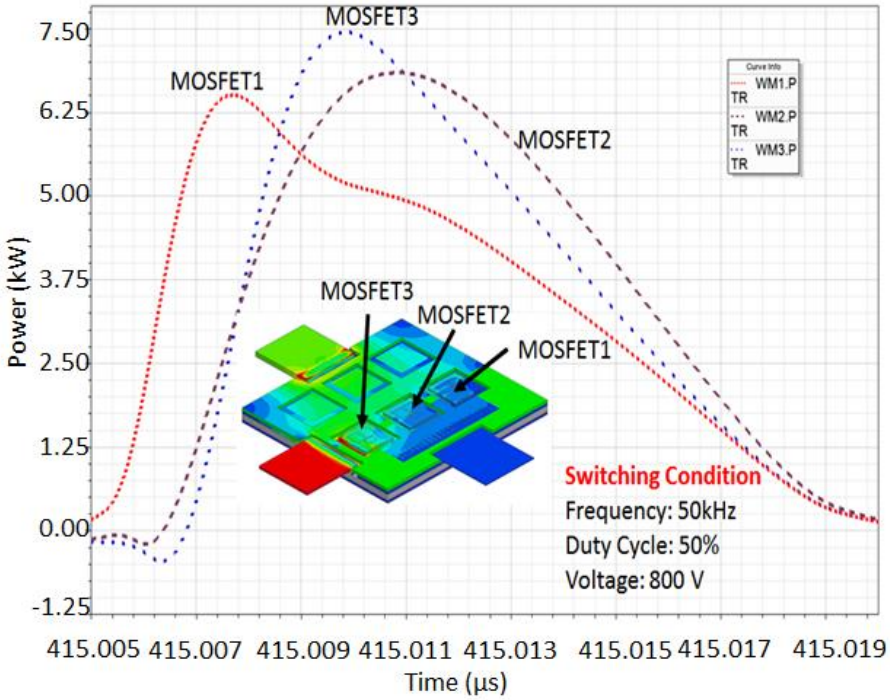
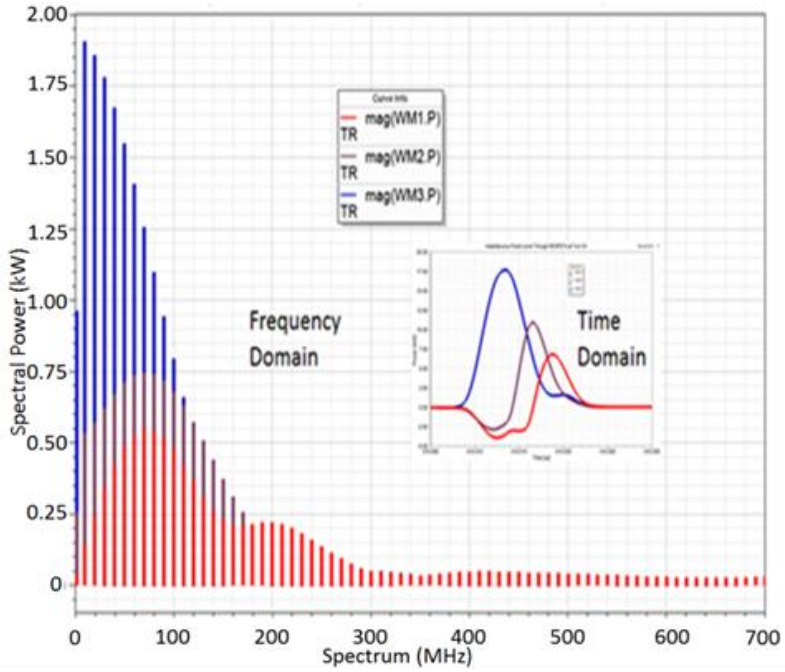


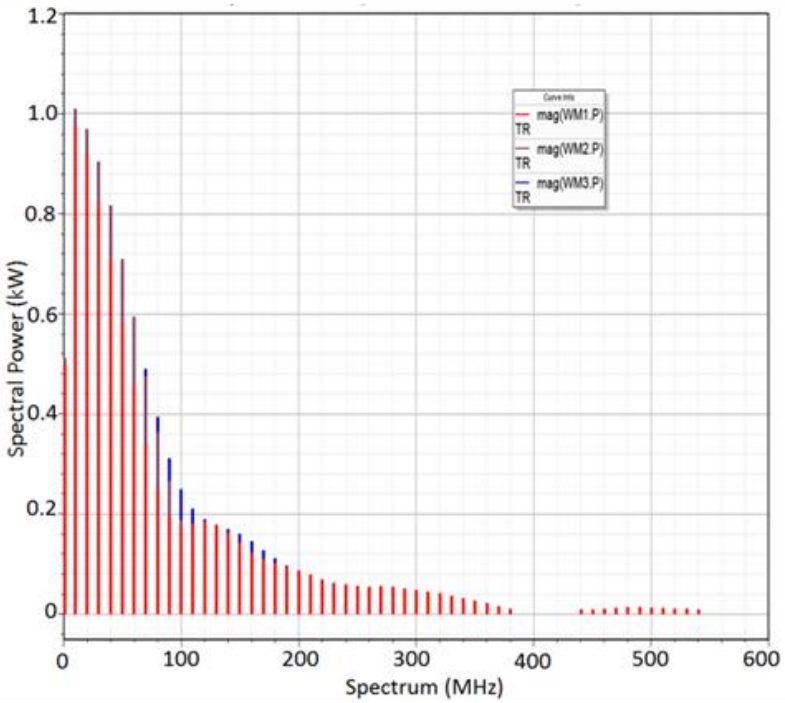
Fig. 7.9. Instantaneous power throug paralleled power MOSFETs (wire bondless module)

7.7 Full Wave Simulation

The frequency domain spectral power amplitudes are given as inputs for the ANSYS HFSS to perform 3D full wave electromagnetic simulations in order to analyze radiated fields from the power modules. In ANSYS HFSS, a driven modal solution is performed to simulate the electric field strength. The power levels are assigned to the device location on the physical layout using lumped ports. The lumped ports are assigned between the drain and source of the power MOSFETs.



(a)



(b)

Fig. 7.10. Spectral power levels through power MOSFETs (a) Wire bonded module, (b) Wire bondless module

Fig. 7.11 shows the electric field strength in volts per meter at different spectral frequencies of 10 MHz, 100 MHz and 200 MHz. From Fig. 7.10, it is evident that the power levels conducting through each MOSFET gradually decreases as frequency increases. The electric field strength also follows the same pattern and decreases as the power levels are decreasing at higher frequencies. As can be seen from Fig. 7.11, the electric field is highly localized for wire bondless power module compared to wire bonded power module. The high power levels due to the parasitic imbalance in wire bonded power module for a very short duration of time contribute towards higher electric field. On the contrary, the wire bondless power module utilizes the top and bottom DBC substrates to form a forward and return current path laid on top of each other in opposing directions. As such, the opposing current paths cancel the magnetic fields to yield a shielding mechanism to suppress the fields. As mentioned before, the dimensions are 19.5 mm × 34 mm and 19 mm × 19 mm for the wire bonded and wire bondless power modules, respectively. The frequency of interest is between 10 MHz to 200 MHz, which corresponds to wavelength ranging from 30 m to 1.5 m. Since the largest conductor should be at least $\lambda/4$ wavelength to yield effective radiation, both wire bonded and wire bondless modules itself will not radiate efficiently because the largest metallic conductor dimensions for both the modules are much smaller than their quarter wavelengths. However, in reality, power modules are part of larger power electronic systems surrounded by larger metallic objects that might radiate the electric field emitted from the power modules. So, for electromagnetic compatibility (EMC) compliance, it is important to suppress the electric field as close as possible to the power modules.

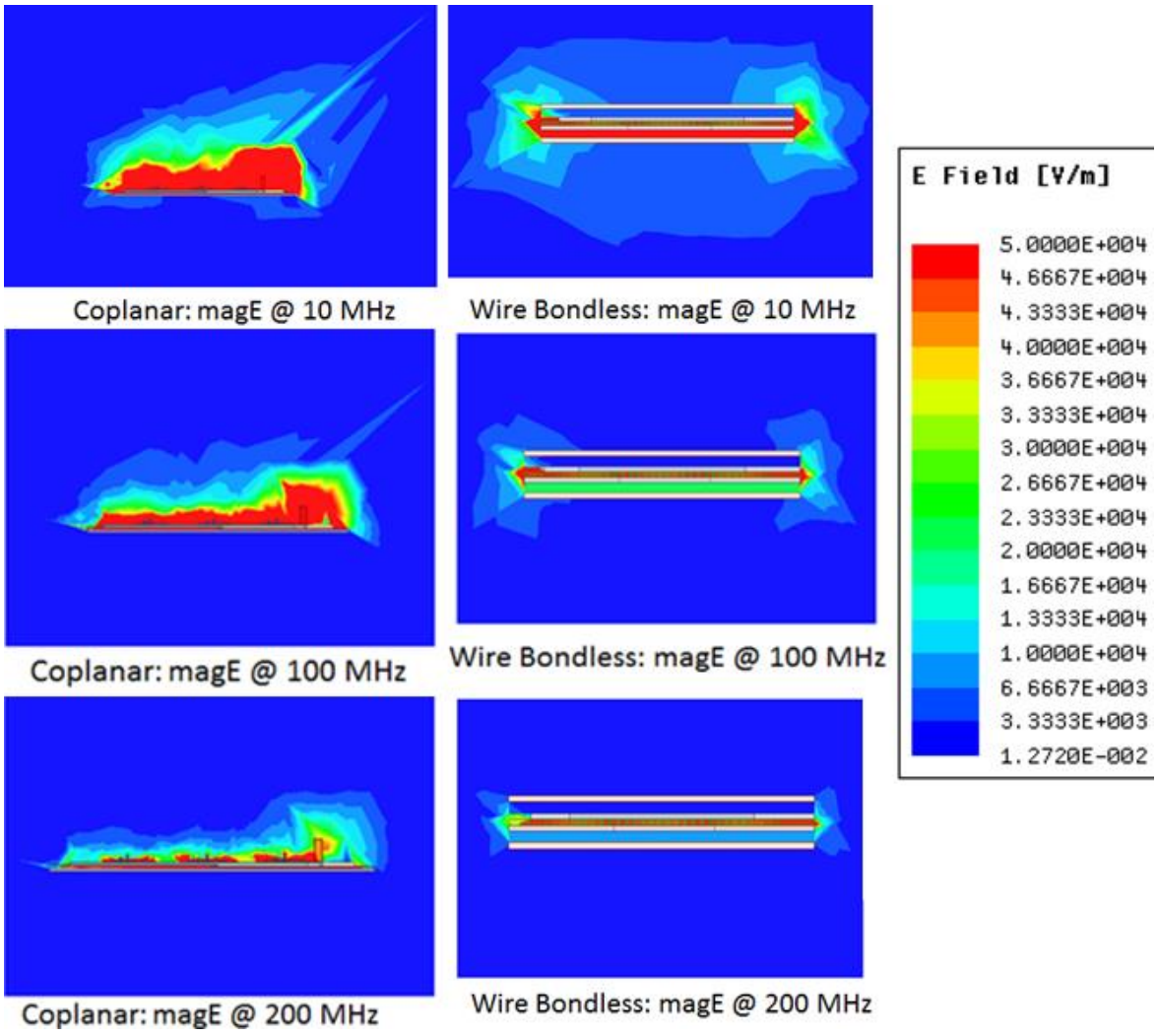


Fig. 7.11. E-field strength at different frequencies for wire bonded and wire bondless modules

The wire bondless power module structure with the top and bottom DBC substrates provides a shielding mechanism to suppress the fields within the module structure. The shielding effectiveness can be calculated from the skin depth of the confined metal. The skin depth of metal is given as [24]-[25],

$$Skin\ Depth, \delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \qquad (7.2)$$

where, δ= skin depth of the metal, f= frequency, μ=magnetic permeability, and σ=conductivity of metal. The copper layer thickness for the top and bottom DBC substrates is 304.8 µm. At 10 MHz, the calculated skin depth for copper is approximately 20.3 µm assuming the conductivity of copper is $5.7\times10^7\ S/m$. The total shielding effect can be found by summing the absorption and reflection losses given by the following expressions [24]-[25],

$$Absorption\ Loss, A\ (dB) = 20loge^{-\frac{t}{\delta}} \qquad (7.3)$$

where, t= thickness of the copper layer, δ= skin depth of copper

$$Reflection\ Loss, R\ (dB) = 20log\frac{\eta_0}{4\eta_s} \qquad (7.4)$$

where, η_0= intrinsic free space wave impedance, η_s= intrinsic impedance of copper

The intrinsic impedance of copper is given by [24]-[25],

$$\eta_s = \sqrt{\frac{2\pi f \mu}{\sigma}} \qquad (7.5)$$

Form the above expressions, the reflection and absorption losses for the 304.8 µm copper are calculated to be 98 dB and 127 dB, respectively. So, the total shielding effectiveness for the direct bond copper substrate is 225 dB in any one direction. As such, wire bondless power modules will provide better electromagnetic compliance compared to wire bonded power module.

7.8 Radiated EMI Validation

It this section, a simple validation process of our simulation methodology is performed. To verify the simulation methodology, a single device power module is fabricated using a 1200 V 36 A SiC power MOSFET (CPM2-1200-0080B) from CREE, similar to the device used for simulation. The test setup includes a power supply (HP-E3630A), a function generator (HP-33120A), a spectrum analyzer (Rigol-DSA 815) and a near-field EMC probe kit (Tekbox-TBPS01-TBWA2) as shown in Fig. 7.12. The near filed EMC probe kit consists of four EMC probes with three H-field probes of different loop diameters and one E-field probe. As the measurement is carried out on coplanar current carrying traces, the H-field probes are most sensitive to the radiated emissions from the power module. The near field EMC probe is positioned just above the power module to capture the maximum field strength from the switching test**.** The EMC probe is connected to the spectrum analyzer through a 40 dB wideband pre-amplifier to increase the dynamic range of the measurement. Three different H-field probes with 20 mm, 10 mm and 5 mm diameter are initially used to choose the most sensitive probe to the radiated fields. It is observed that the 5 mm diameter probe is most sensitive to the radiated fields and can locate precisely the source of the radiated emissions, which is mostly concentrated in the switching loop of the power device. The dimension of the supply and terminal leads are carefully chosen so that they are not self-radiating objects at the frequencies of interest. The device is switched at 50 kHz using a gate-source voltage V_{gs} of 20 V. The DC supply voltage provided for the switching test is 20 V. The resolution bandwidth for the spectrum analyzer is set at 1 MHz. The unit of measurement for the spectrum analyzer is set to measure in mV with a reference level of 100 mV. The impedance of the spectrum analyzer is 50 Ω. In order to maintain consistency, the impedance of all the cables connecting the near-field EM probes and the wide

band amplifier to the spectrum analyzer are chosen to be 50 Ω. As discussed earlier, the frequency range of interest is up to 200 MHz, as such, the frequency range for the spectrum analyzer is set from 10 kHz to 200 MHz.

To verify the measurement results, a simulation based study is performed on the fabricated power module using the same simulation methodology discussed earlier. Fig. 7.13 shows the simulated spectral power distribution in dBm for the fabricated power module under similar test conditions discussed above. In order to compare the spectrum analyzer measurement and SIMPLORER simulation, the simulated unit in dBm is converted to mW and subsequently to mV using the following equation assuming the impedance of the measurement is 50 Ω:

$$Power\ (mW) = \frac{|V|^2}{50\ \Omega} \qquad (7.6)$$

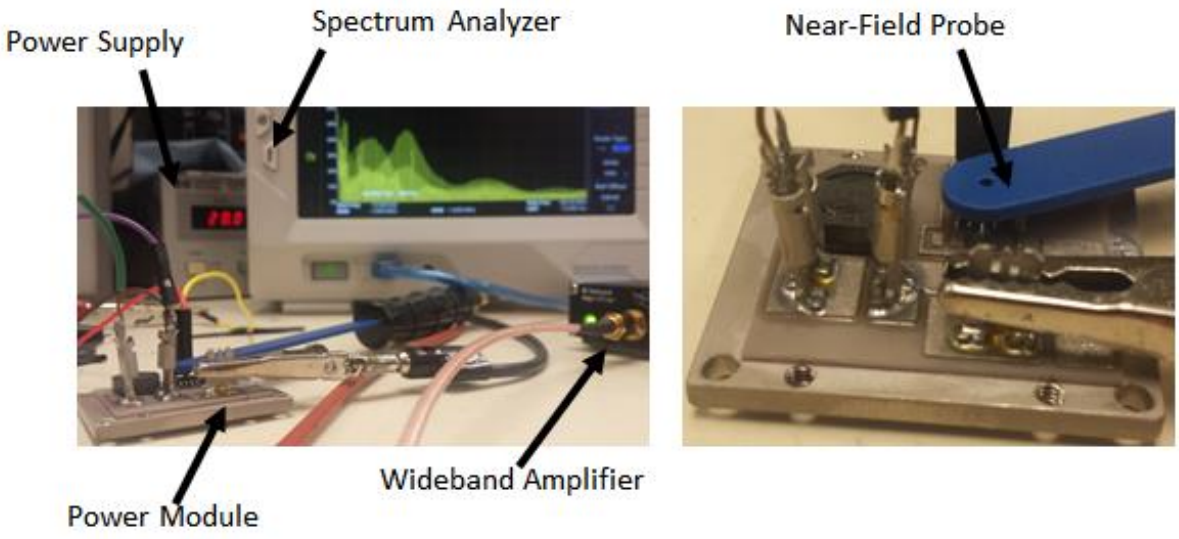


Fig. 7.12. Test setup for near-field measurement

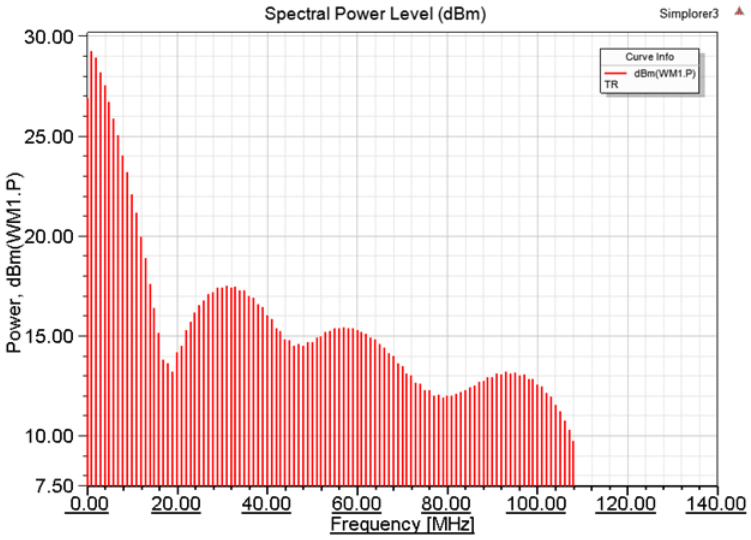


Fig. 7.13. Simulated spectral power for the fabricated single device module

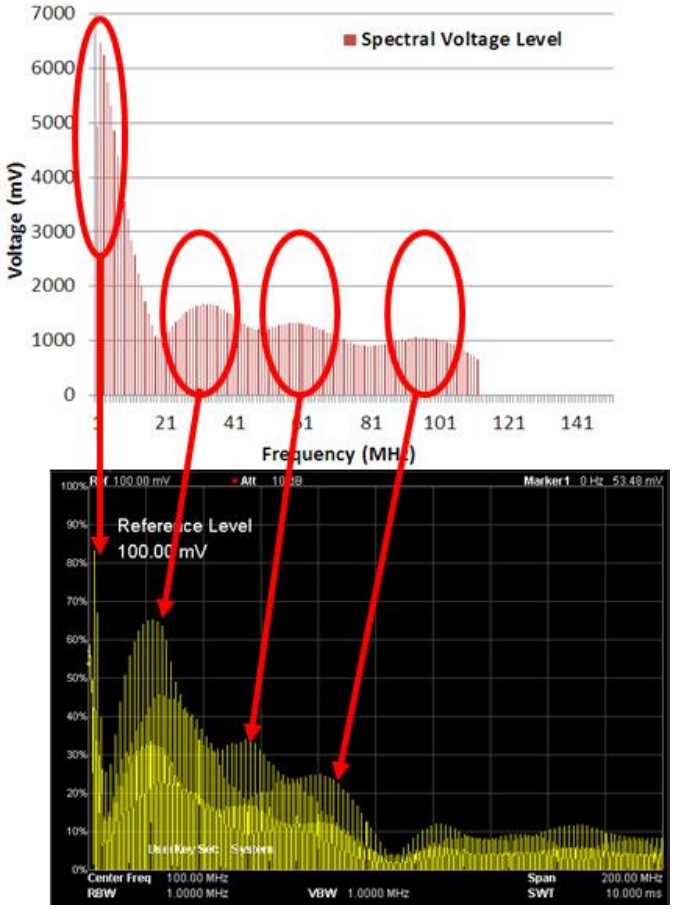


Fig. 7.14. Comparison between simulation (above) and measurement (below)

Fig. 7.14 shows the comparison between the simulation (above) and the measurement data (below). As can be seen from the measurement and simulation results, the spectral spikes occur at similar frequencies, even though the amplitudes for the measurement results are several orders of magnitude lower than those from simulation. It should be mentioned here that the measurement with the near field EM probe were performed at a distance away from the power module. On the contrary, the simulation results are spectral power levels conducting directly through the devices. As the near field probe is placed above the power module at some distance, the power levels diminish gradually since the radiated power captured by the EM probe depends strongly on its sensitivity and distance from the power module. As such, the magnitude captured by the EM probe is lower. Since the frequency spikes in the simulation and measurement occur at similar frequencies, these measurements validate the simulation methodology.

7.9 Conducted EMI Simulation and Validation

In order to perform conducted EMI measurements and validation of the simulation methodology, a single device power module consisting of CREE's 1200 V 36 A SiC power MOSFET (CPM2-1200-0080B) is fabricated. The power

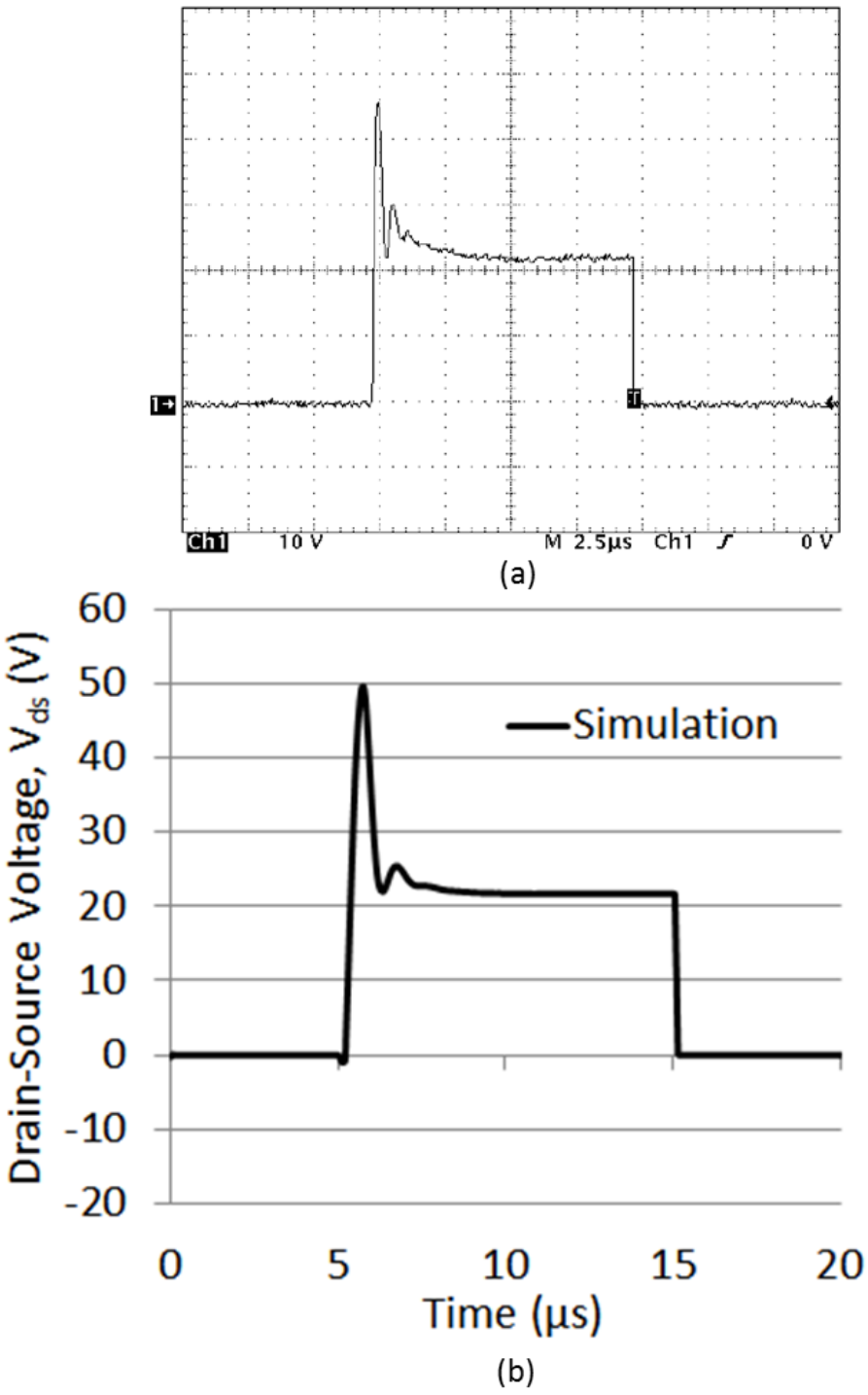


Fig. 7.15. Switching waveform (a) measurement , (b) simulation

module is first designed using ANSYS EM tools and simulated for its conducted EMI response. The frequency dependent parasitic extraction of the power module is performed using ANSYS Q3D and subsequently a switching simulation is performed using the frequency dependent parasitic model and the characterized SiC power MOSFET in ANSYS SIMPLORER. The clamped inductive switching test is performed on the fabricated power module under 20 V input DC voltage. Fig. 7.15 (a) and (b) shows the drain to source voltage waveforms under clamped inductive switching recorded from measurement and simulation, respectively. As can be seen, the simulated switching waveform matches with the measured waveform both in transient and the steady state.

A line impedance stabilization network (LISN) is implemented to simulate and measure the conducted EMI per CISPR22 [34]-[38]. The circuit model for the LISN is taken from the manufacturer's (ETS-LINDGREN, model-3810/2 LISN) provided user manual [39]. Fig. 7.16 shows the setup for the conducted EMI simulation and measurement. A power line filter (CORCOM F7129) is introduced in between the power supply and LISN in order to filter any noise coming from the power supply. The power module under test is kept on a non-conductive wooden table and the LISN is placed under the table and grounded properly according to the standards. The output of the LISN is fed to the spectrum analyzer to observe the conducted EMI noise.

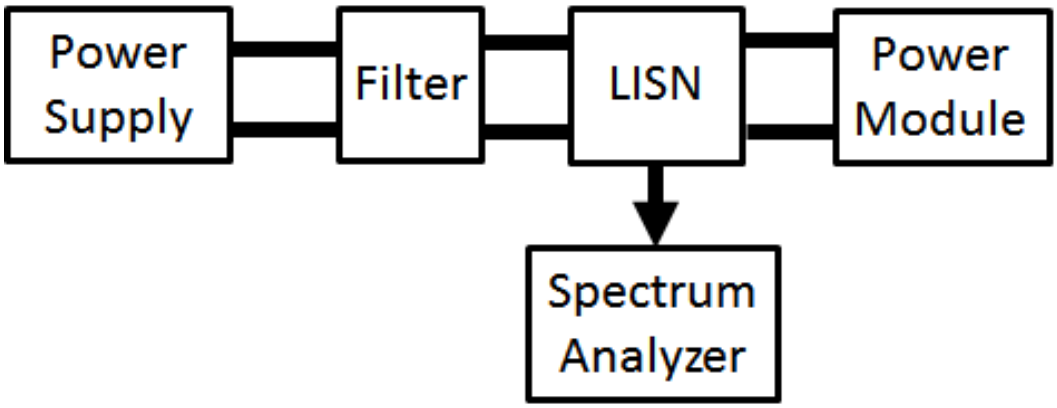


Fig. 7.16. Conducted EMI measurement setup

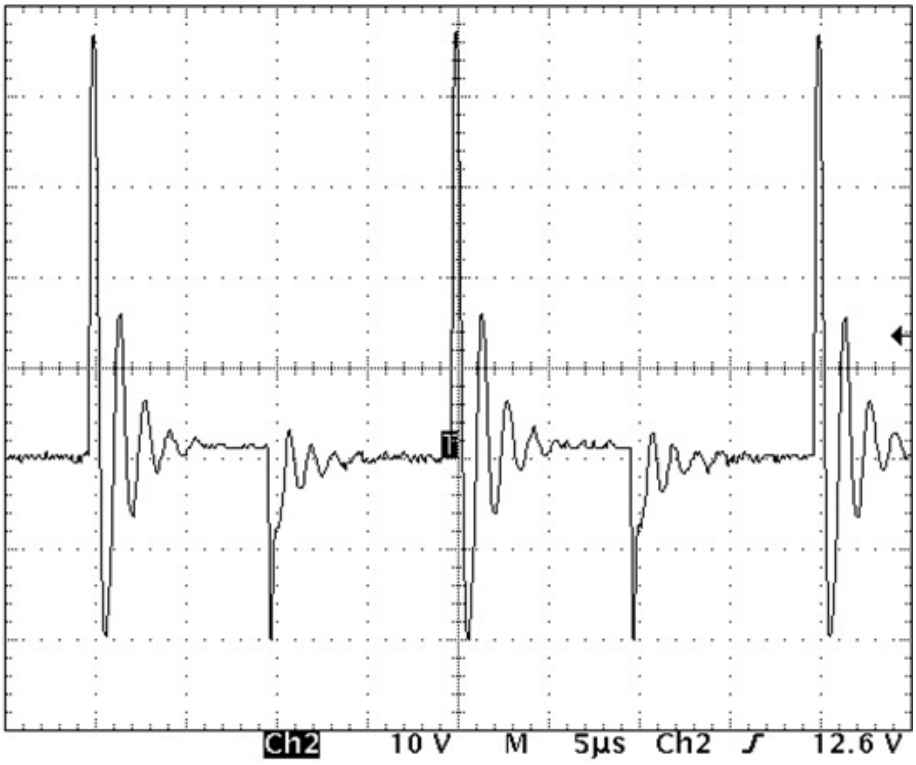


Fig. 7.17. Voltage level at line of LISN monitored from oscilloscope

Fig. 7.17 and Fig. 7.18 show the voltage levels at the two lines (line and neutral) of the LISN under the operating conditions monitored on oscilloscope. These voltage waveforms are fed into

the spectrum analyzer to obtain the frequency domain spectral distribution of the line and neutral voltages of the LISN.

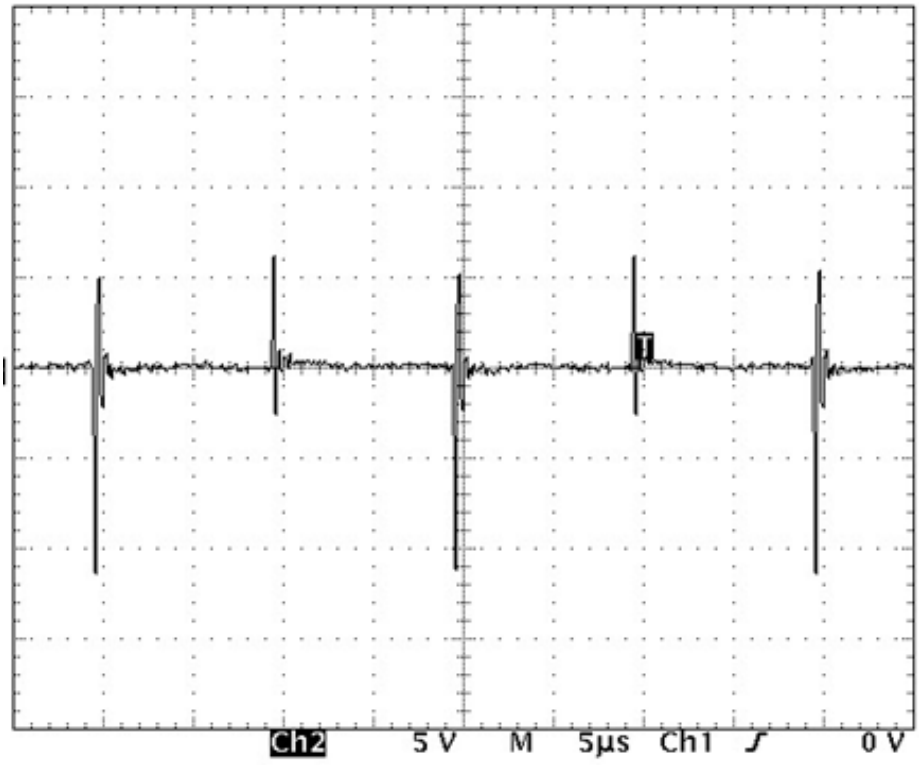


Fig. 7.18. Voltage level at neutral of LISN monitored from oscilloscope

Fig. 7.19 and Fig. 7.20 show the comparison between the simulated and measured spectral distribution of the line voltages from 150 kHz to 30 MHz. For the simulated spectrum, the voltages at two lines are first simulated using the frequency dependent parasitic model, cable configuration, and LISN model in ANSYS SIMPLORER. The FFT of the time domain waveforms are then performed using MATLAB to achieve the frequency domain response. As can be seen from Fig. 7.19 and Fig. 7.20, the simulated and measured spectra of the line voltages closely match in magnitude and spectral shape.

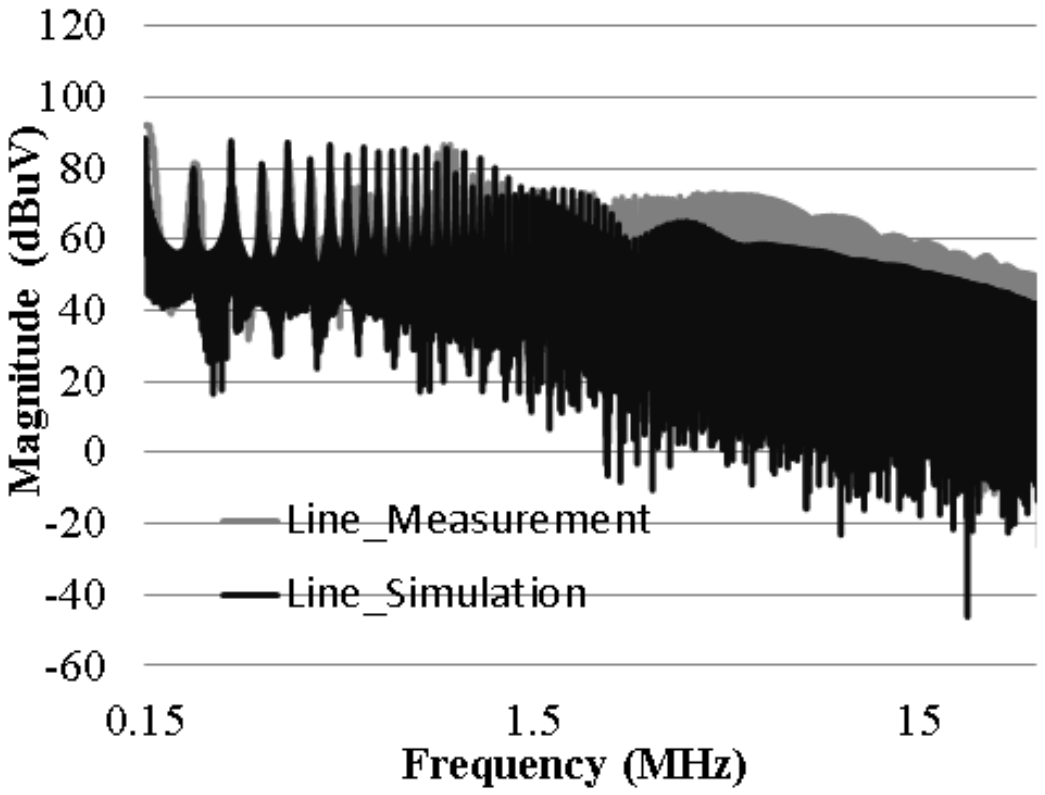


Fig. 7.19.Simulated and measured voltages at LISN line

Fig. 7.21 and Fig. 7.22 show the comparison of the simulated and measured differential and common mode LISN voltages. The differential and common mode voltages are mathematically separated using the following equations:

$$V_{DM} = (V_{Line} - V_{Neutral})/2 \qquad (7.7)$$

$$V_{CM} = (V_{Line} + V_{Neutral})/2 \qquad (7.8)$$

As can be seen, the simulated differential and common mode voltages match well with the measured results.

From Fig. 7.19, Fig. 7.20, Fig. 7.21 and Fig. 7.22, we can observe that the magnitudes of the low frequency spikes are similar. However at higher frequency, around 20-30 MHz the simulation amplitudes are about 8-10 dBμV lower than that of the measurement. This can be attributed to the round off error of

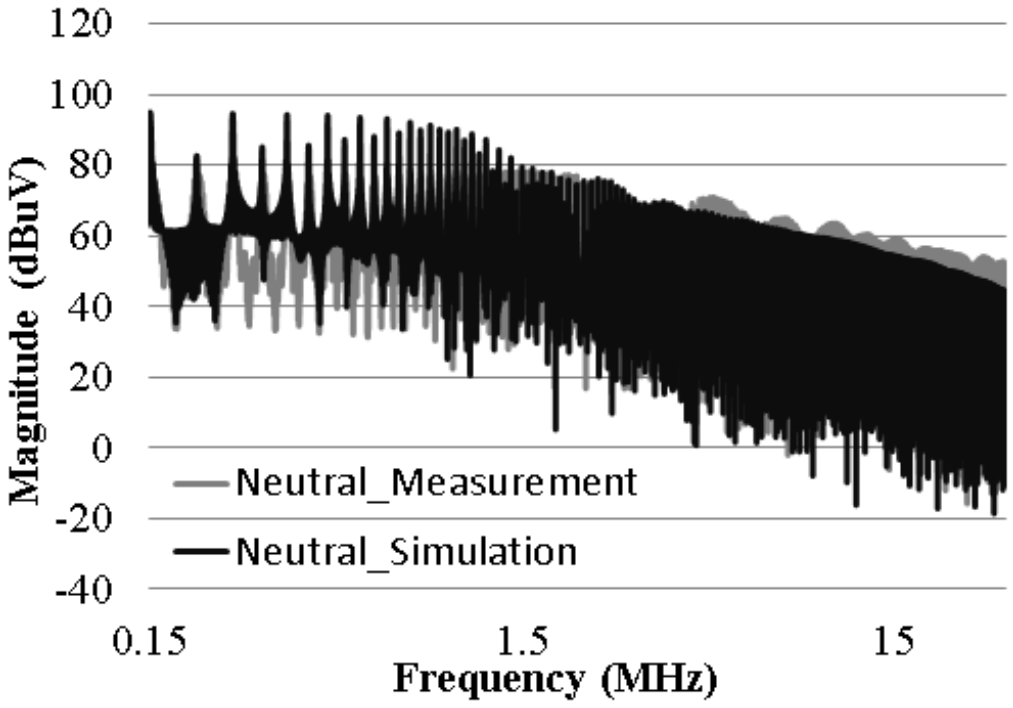


Fig. 7.20. mulated and measured voltages at LISN neutral

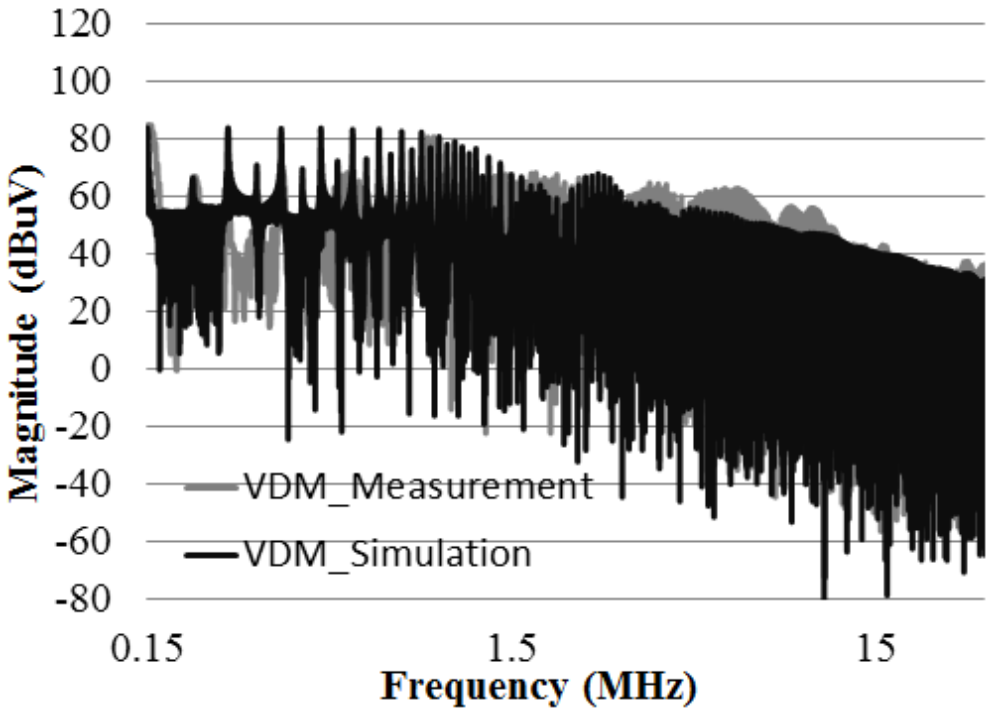


Fig. 7.21.Differential mode noise

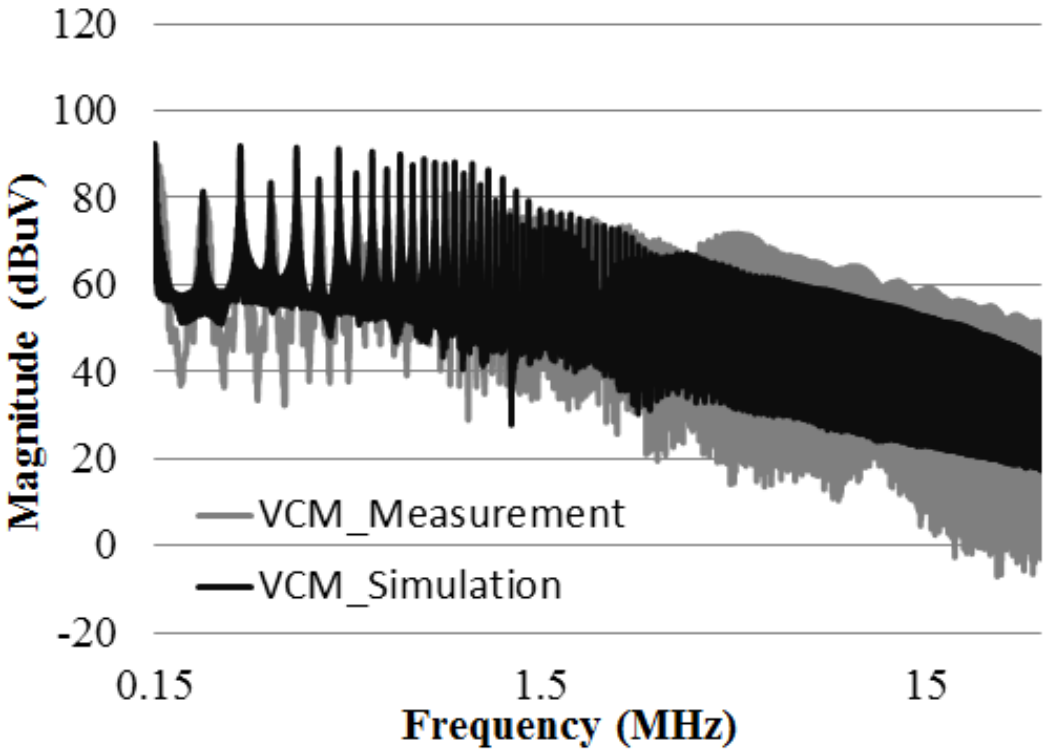


Fig. 7.22. Common mode noise

the FFT conversion. The correlation coefficient between the simulation and measurement is 0.73. The coefficient of determination (R^2) is calculated to be 53%. As such, 53% of the variation in the measurement results can be explained by the linear relationship between simulation and measurement, which is deemed acceptable given the highly non-linear behavior of the conducted EMI noise.

7.10 Conclusions

A simulation methodology that incorporates co-simulation techniques using ANSYS EM tools is proposed to predict both radiated and conducted electromagnetic interference (EMI) from power electronic modules. The radiated EMI for a coplanar wire bonded and wire bondless

power modules are simulated and compared. The instantaneous power levels conducting through the power devices in the wire bonded power module are significantly higher than those for the wire bondless power module due to parasitic imbalance. These power levels occur for a very short duration of time at turn-on of the devices and can be considered as a potential source of radiated EMI emissions. It has been demonstrated that a wire bondless power module shows a greater EMC compliance compared to a traditional wire bonded power module. Moreover, the simulation methodology used to reach this conclusion has been validated using a simple near field EMC measurement technique with EMC probes and a spectrum analyzer. The conducted EMI simulation for a single device power module was performed using the proposed simulation methodology. The simulation results were compared with the measurement results and they show good agreement both in shape and magnitude. As such, the simulation methodology proposed for radiated and conducted EMI can be incorporated into the initial design phase of the power modules to reduce the design cycle and costly engineering process to test for EMI/EMC.

7.11 Acknowledgement

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Chapter 8 Conclusion and Future Work

In this chapter, the contributions and significance of this dissertation research are highlighted. The key research contributions are summarized. The work performed as part of this dissertation research can be utilized as a platform to do further development in the 3-D wire bondless power module stack. Several other features such as thermal management can be included to improve and make the 3-D stack module more feasible. Several recommendations on possible future work are also highlighted.

8.1 Dissertation Contribution

As part of this dissertation research, a 3-D wire bondless half-bridge stacked power module is designed, fabricated and characterized. The wire bondless stacked solution for a half-bridge module is demonstrated by two stand-alone wire bondless modules. A novel interconnection scheme is developed using conductive clamps and an LTCC based spring loaded interposer to interconnect the two stand-alone power modules to maintain an anti-parallel current path configuration to yield a very low inductance half-bridge module. The proposed wire bondless 3-D stack module exhibit improved electrical performances compared to a traditional wire bonded half-bridge module. Parasitic inductances for the current conducting nets are extracted using ANSYS Q3D simulations and verified by parasitic measurement using an impedance analyzer. The parasitic inductance for all critical current conducting nets exhibits parasitic inductance of 3 nH or less at 100 kHz. The overall loop inductance is another parameter that is critical for a half-bridge power module. The proposed 3-D wire bondless module shows a 4 nH of parasitic inductance at 100 kHz for the DC+ to DC- loop, which is 71% lower compared to a wire bonded

power module. The low parasitic inductance is achieved using an anti-parallel current path configuration utilizing the multi-layer LTCC substrates.

The lower parasitic inductance improves the switching behavior of the 3-D wire bondless stack. A switching performance comparison between the 3-D wire bondless stack and a traditional wire bonded power module is performed. Due to the lower parasitic inductance, the switching characteristics of the 3-D wire bondless power module exhibits significantly lower ringing and overshoot, and lower settling time of the switching transients both during turn-on and turn-off. Both simulations and measurements are performed to verify the improvement in switching characteristics of the 3-D wire bondless power module. A performance improvement is achieved for both turn-on and turn-off characteristics of the 3-D wire bondless stack compared to the wire bonded half-bridge module with a 30% reduction in current overshoot at turn-on and 43% reduction in turn-off voltage overshoot.

A simulation methodology to predict electromagnetic interference of power module is developed using ANSYS EM tools [1]. Hardware verification of the simulation methodology is performed to validate the simulation methodology. The simulation methodology can be incorporated in the design phase of the power module to predict EMI and reduce the design cycle of power modules [1]. A co-simulation technique between various ANSYS EM software tools is used to develop the simulation methodology. The simulation result obtained by implementing the simulation methodology shows good agreement with the measured EMI spectra.

8.2 Future Work

As for all research and development, an improvement of the existing solutions is an ongoing activity. The work done as part of this dissertation research can be used as a groundwork to do

further development on the 3-D wire bondless stacked power modules. Parasitic inductance reduction by proposing a novel stacked power module structure along with its packaging architecture is of the primary focuses of this dissertation research. The usage of LTCC provides vertical design freedom which can be utilized to perform a higher level of integration. Gate driver chip and circuitry can be integrated on the LTCC substrate to reduce the gate loop parasitic inductance further from a package system standpoint. If available, bare die gate drivers can be implemented in very close vicinity to the semiconductor devices to further reduce the gate loop inductance and improve the switching performance of the power devices. This can be achieved by implementing vertical conducting vias on LTCC to shorten and optimize the interconnections to reduce parasitic inductance.

Even through LTCC can promote much compact and high-density designs there are a number of limitations that need further improvements as part of future work. Metallization on LTCC substrates is generally performed using a thick film screen printable paste. However, the screen printing of thick film silver and gold pastes usually results in thin conductors that are not suitable for high power applications. Moreover, the electrical and thermal conductivity of these screen-printed pastes are lower compared to the conventional evaporated, sputtered or electroplated metallization. As such, additional electrical and thermal resistances deteriorate the performance of the semiconductor devices. For high power and better current handling capability, the metallization on the LTCC substrate needs to be improved. Electroplating or electroless plating of copper on plateable screen printing paste can be a viable solution to increase the thickness of the LTCC metallization and increase the electrical and thermal conductivity to lower package influence on semiconductor device characteristics.

The thermal conductivity of LTCC is 3 W/mK, which is significantly lower compared to DBC substrate, which is predominantly used as power substrates for high power applications. As such, it is a significant challenge to overcome thermal management issues using LTCC as power substrates. However, unlike other power substrates, LTCC provides design freedom to incorporate active cooling mechanism into the substrate by implementing liquid microchannels. Thermal micro-channels are predominantly used in LTCC substrates, however, integrating these into a power substrate for active cooling of semiconductor devices for high power applications is very promising but challenging. Thermal vias filled with high thermally conductive materials are a predominant choice to remove heat from the operating junction for multilayer laminated substrates. As such thermal vias are a good choice for heat removal in LTCC. However, as a low thermally conductive material, the heat spreading in the horizontal direction is very low for LTCC substrates. However, due to the design freedom of LTCC shallow trenches can be designed and filled with high thermally conductive materials to realize thermal contours on the LTCC substrate to increase the heat spreading capability in the horizontal direction of LTCC.

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Appendix

V_{CE} = 1200 V
I_C = 25 A

IGBT-Die

5SMX 12E1280

Die size: 6.6 x 6.5 mm

Doc. No. 5SYA1306-03 04 14

- **Low loss, rugged SPT technology**
- **Smooth switching for good EMC**
- **Large bondable emitter area**
- **Passivation: Silicon Nitride plus Polyimide**
- **Optimized for high DC-link voltage applications**

Maximum rated values [1]

Parameter	Symbol	Conditions	min	max	Unit
Collector-emitter voltage	V_{CES}	V_{GE} = 0 V, $T_{vj} \geq$ 25 °C		1200	V
DC collector current	I_C			25	A
Peak collector current	I_{CM}	Limited by T_{vjmax}		50	A
Gate-emitter voltage	V_{GES}		-20	20	V
IGBT short circuit SOA	t_{psc}	V_{CC} = 900 V, $V_{CEM} \leq$ 1200 V $V_{GE} \leq$ 15 V, $T_{vj} \leq$ 125 °C		10	µs
Junction temperature	T_{vj}		-40	150	°C

[1] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747 - 9

IGBT characteristic values [2)]

Parameter	Symbol	Conditions		min	typ	max	Unit
Collector (-emitter) breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 1 mA, T_{vj} = 25 °C		1200			V
Collector-emitter saturation voltage	$V_{CE\ sat}$	I_C = 25 A, V_{GE} = 15 V	T_{vj} = 25 °C		2.15		V
			T_{vj} = 125 °C		2.35		V
Collector cut-off current	I_{CES}	V_{CE} = 1200 V, V_{GE} = 0 V	T_{vj} = 25 °C			100	µA
			T_{vj} = 125 °C		50		µA
Gate leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V, T_{vj} = 125 °C		-200		200	nA
Gate-emitter threshold voltage	$V_{GE(TO)}$	I_C = 1 mA, V_{CE} = V_{GE}, T_{vj} = 25 °C		4.5		6.5	V
Gate charge	Q_{ge}	I_C = 25 A, V_{CE} = 600 V, V_{GE} = -15 ..15 V			270		nC
Input capacitance	C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz, T_{vj} = 25 °C			1.9		nF
Output capacitance	C_{oes}				0.14		
Reverse transfer capacitance	C_{res}				0.08		
Internal gate resistance	R_{Gint}				10		Ω
Turn-on delay time	$t_{d(on)}$	V_{CC} = 600 V, I_C = 25 A, R_G = 47 Ω, V_{GE} = ±15 V, L_σ = 120 nH, inductive load	T_{vj} = 25 °C		145		ns
			T_{vj} = 125 °C		145		
Rise time	t_r		T_{vj} = 25 °C		60		ns
			T_{vj} = 125 °C		60		
Turn-off delay time	$t_{d(off)}$	V_{CC} = 600 V, I_C = 25 A, R_G = 47 Ω, V_{GE} = ±15 V, L_σ = 120 nH, inductive load	T_{vj} = 25 °C		400		ns
			T_{vj} = 125 °C		465		
Fall time	t_f		T_{vj} = 25 °C		75		ns
			T_{vj} = 125 °C		70		
Turn-on switching energy	E_{on}	V_{CC} = 600 V, I_C = 25 A, V_{GE} = ±15 V, R_G = 47 Ω, L_σ = 120 nH, inductive load, FWD: ½ 5SLX12E1200	T_{vj} = 25 °C		2.5		mJ
			T_{vj} = 125 °C		3.8		
Turn-off switching energy	E_{off}	V_{CC} = 600 V, I_C = 25 A, V_{GE} = ±15 V, R_G = 47 Ω, L_σ = 120 nH, inductive load	T_{vj} = 25 °C		1.5		mJ
			T_{vj} = 125 °C		2.5		
Short circuit current	I_{SC}	t_{psc} ≤ 10 µs, V_{GE} = 15 V, T_{vj} = 125 °C, V_{CC} = 900 V, V_{CEM} ≤ 1200 V			115		A

[2)] Characteristic values according to IEC 60747 - 9

Mechanical properties

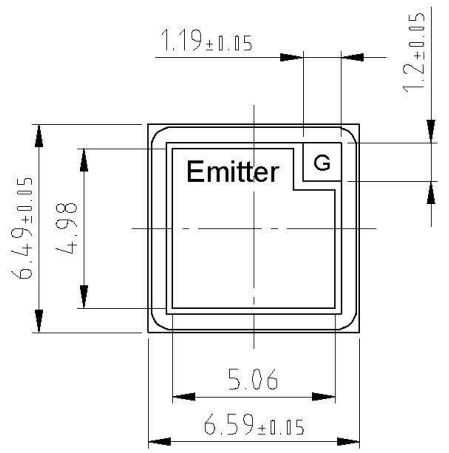
Parameter				Unit
Dimensions	Overall die	L x W	6.6 x 6.5	mm
	exposed front metal	L x W (except gate pad)	5.1 x 5.0	mm
	gate pad	L x W	1.2 x 1.2	mm
	thickness		140 ± 20	µm
Metallization [3]	front (E)	AlSi1	4	µm
	back (C)	Al / Ti / Ni / Ag	1.8	µm

[3] For assembly instructions refer to : IGBT and Diode chips from ABB Switzerland Ltd, Semiconductors, Doc. No. 5SYA 2033.

Form of delivery

Description	Part number
Unsawn 6'' wafer die	5SMX 76E1280
Sawn 6'' wafer die (on blue tape)	5SMX 86E1280

Outline drawing



Note: all dimensions are shown in mm

This is an electrostatic sensitive device, please observe the international standard IEC 60747-1, Chap. IX.

This product has been designed and qualified for Industrial Level.

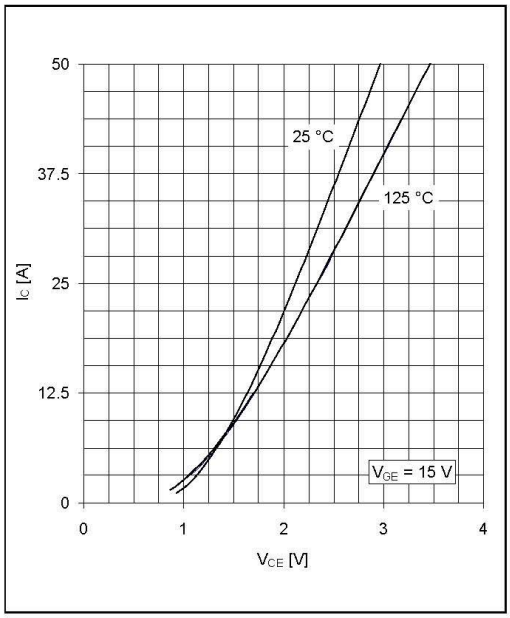


Fig. 1 Typical on-state characteristics

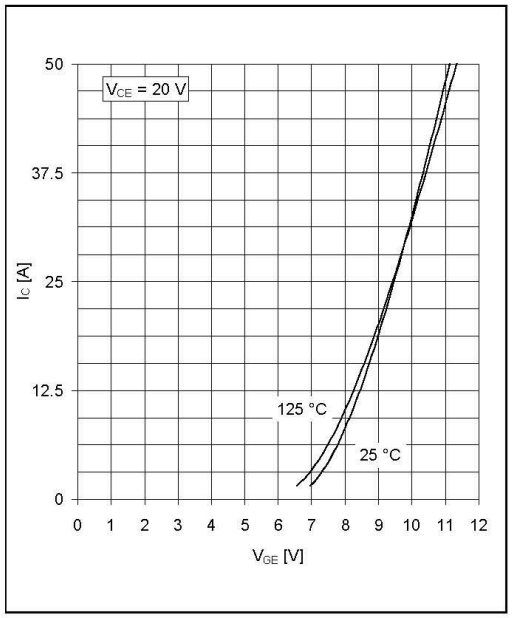


Fig. 2 Typical transfer characteristics

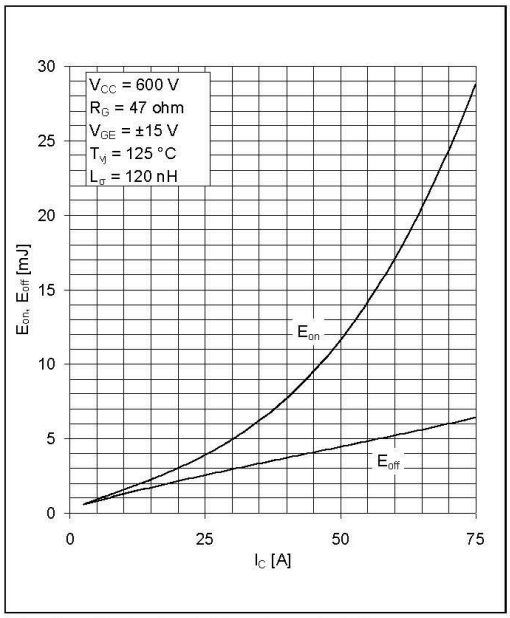


Fig. 3 Typical switching characteristics vs collector current

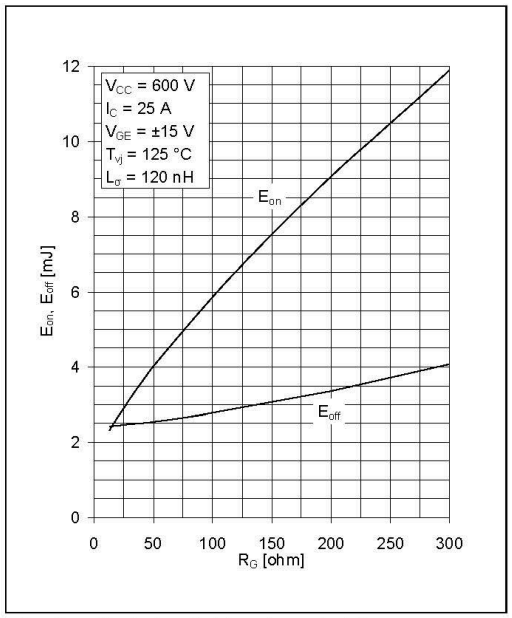


Fig. 4 Typical switching characteristics vs gate resistor

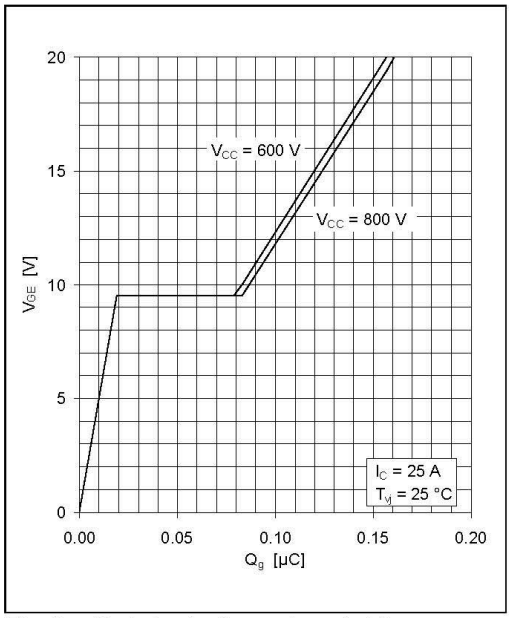


Fig. 5 Typical gate charge characteristics

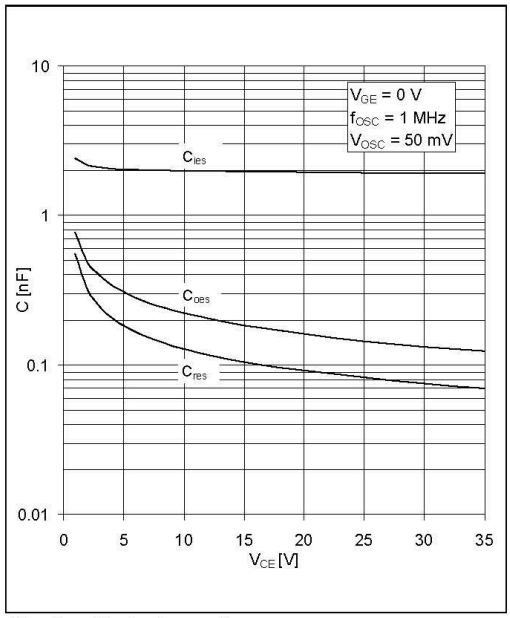


Fig. 6 Typical capacitances vs collector-emitter voltage

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Doc. No. 5SYA1306-03 04 14

CPW4-1200-S020B

Silicon Carbide Schottky Diode Chip

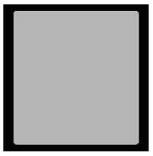
Z-Rec® Rectifier

V_{RRM}	=	1200 V
$I_{F(AVG)}$	=	20 A
Q_c	=	130 nC

Features

- 1.2kV Schottky Rectifier
- Zero Reverse Recovery
- Zero Forward Recovery
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

Chip Outline



Part Number	Die Size	Anode	Cathode
CPW4-1200S020B	3.08 x 3.08 mm^2	Al	Ni/Ag

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	1200	V		
V_{RSM}	Surge Peak Reverse Voltage	1300	V		
V_R	DC Peak Blocking Voltage	1200	V		
I_F	Continuous Forward Current	20	A	T_J=175˚C	1
I_{FRM}	Repetitive Peak Forward Surge Current	91 61	A	T_C=25˚C, t_P=10 ms, Half Sine Pulse T_C=110˚C, t_P=10 ms, Half Sine Pulse	1
I_{FSM}	Non-Repetitive Forward Surge Current	130 110	A	T_C=25˚C, t_P=10 ms, Half Sine Pulse T_C=110˚C, t_P=10 ms, Half Sine Pulse	1
$I_{F,Max}$	Non-Repetitive Peak Forward Current	1150 950	A	T_C=25˚C, t_P=10 ms, Pulse T_C=110˚C, t_P=10 ms, Pulse	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	˚C		
T_{Proc}	Maximum Processing Temperature	325	˚C	10 min. maximum	

1. Assumes $R_{\theta JC}$ Thermal Resistance of 0.62˚C/W or less

CREE

Electrical Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.5 2.2	1.8 3	V	I_F = 20 A T_J=25°C I_F = 20 A T_J=175°C	Fig. 1
I_R	Reverse Current	35 65	200 400	µA	V_R = 1200 V T_J=25°C V_R = 1200 V T_J=175°C	Fig. 2
Q_C	Total Capacitive Charge	99		nC	V_R = 800 V, I_F = 20 A di/dt = 200 A/µs T_J = 25°C	Fig. 3
C	Total Capacitance	1500 93 67		pF	V_R = 0 V, T_J = 25°C, f = 1 MHz V_R = 400 V, T_J = 25°C, f = 1 MHz V_R = 800 V, T_J = 25°C, f = 1 MHz	Fig. 4

Mechanical Parameters

Parameter	Typ.	Unit
Die Size	3.08 x 3.08	mm
Anode Pad Size	2.79 x 2.79	mm
Anode Pad Opening	2.51 x 2.51	mm
Thickness	377 ± 10%	µm
Wafer Size	100	mm
Anode Metalization (Al)	4	µm
Cathode Metalization (Ni/Ag)	1.4	µm
Frontside Passivation	Polyimide	

Typical Characteristics

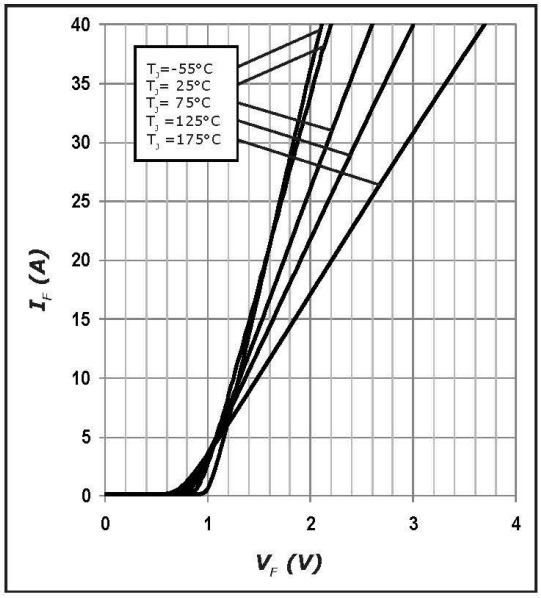


Figure 1. Forward Characteristics

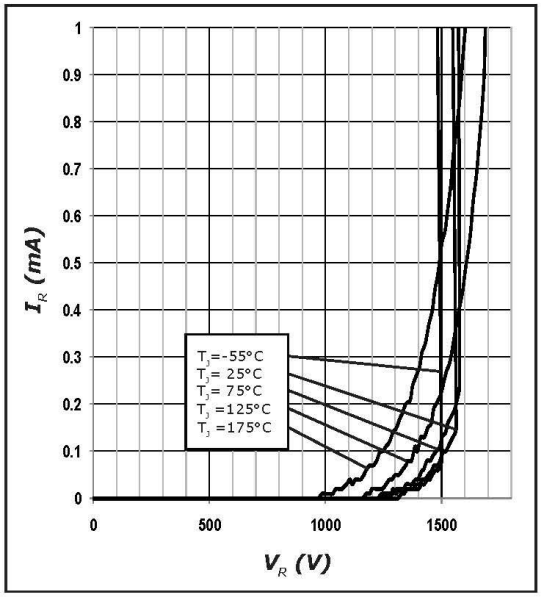


Figure 2. Reverse Characteristics

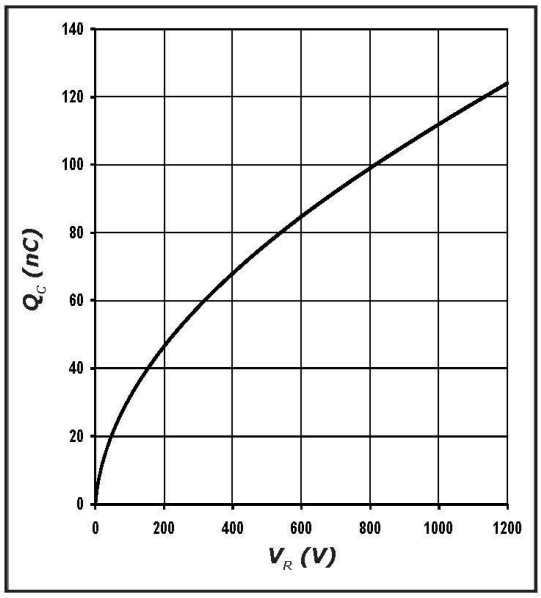


Figure 3. Total Capacitance Charge vs. Reverse Voltage

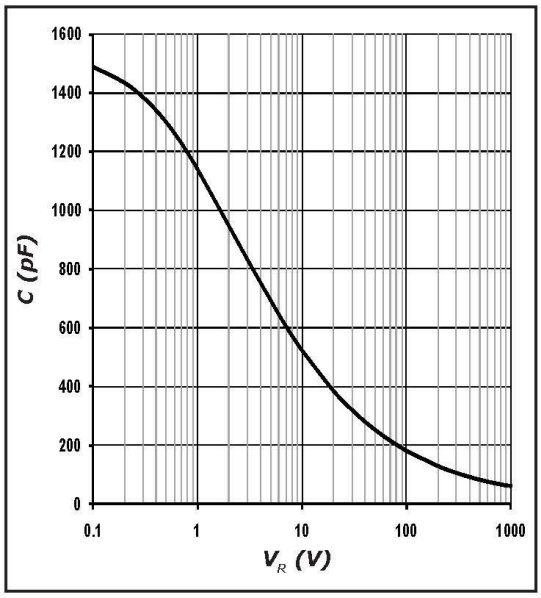
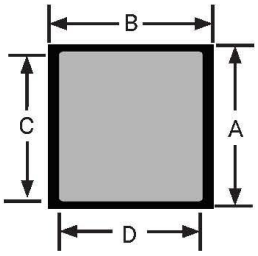


Figure 4. Capacitance vs. Reverse Voltage

Chip Dimensions



symbol	dimension	
	mm	inch
A	3.08	0.121
B	3.08	0.121
C	2.51	0.099
D	2.51	0.099

Notes

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Related Links

- Cree SiC Schottky diode portfolio: http://www.cree.com/diodes
- CPW4 Spice models: http://response.cree.com/Request_Diode_model
- SiC MOSFET and diode reference designs: http://response.cree.com/SiC_RefDesigns

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CPM2-1200-0080B

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	1200 V
$I_{D\ @\ 25^{\circ}C}$	36 A
$R_{DS(on)}$	80 mΩ

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness

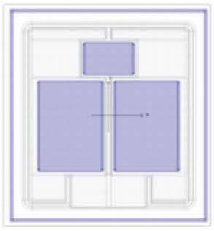
Benefits

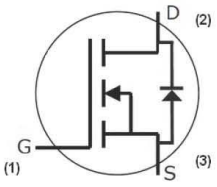
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives
- Switch Mode Power Supplies
- Pulsed Power applications

Chip Outline





Part Number	Die Size (mm)
CPM2-1200-0080B	3.10 x 3.36

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values, AC (f >1 Hz)	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	36	A	V_{GS} = 20 V, T_C = 25°C	Note 1
		27		V_{GS} = 20 V, T_C = 100°C	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width t_P limited by T_{jmax}	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C		
T_{Proc}	Maximum Processing Temperature	325	°C	10 min. maximum	

Note (1): Assumes a $R_{\theta JC}$ < 0.65 K/W

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS} , I_D = 5 mA	Fig. 11
			2.1		V	V_{DS} = V_{GS}, I_D = 5 mA, T_J = 175°C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		80	98	mΩ	V_{GS} = 20 V, I_D = 20 A	Fig. 4, 5, 6
			153			V_{GS} = 20 V, I_D = 20A, T_J = 175°C	
g_{fs}	Transconductance		8.1		S	V_{DS}= 20 V, I_{DS}= 20 A	Fig. 7
			7.7			V_{DS}= 20 V, I_{DS}= 20 A, T_J = 175°C	
C_{iss}	Input Capacitance		950		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		80				
C_{rss}	Reverse Transfer Capacitance		7.6				
E_{oss}	C_{oss} Stored Energy		45		µJ		Fig. 16
E_{AS}	Avalanche Energy, Single Pluse		1		J	I_D = 20A, V_{DD} = 50V	
E_{ON}	Turn-On Switching Energy		265		µJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 20A, $R_{G(ext)}$ = 2.5Ω, L= 142 µH (TO-247-3 Package)	Note 3
E_{OFF}	Turn Off Switching Energy		135				
$t_{d(on)}$	Turn-On Delay Time		11		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 20 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 40 Ω, Timing relative to V_{DS} Per IEC60747-8-4 pg 83 (TO-247-3 Package)	Note 3
t_r	Rise Time		20				
$t_{d(off)}$	Turn-Off Delay Time		23				
t_f	Fall Time		19				
$R_{G(int)}$	Internal Gate Resistance		4.6		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		15		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		23				
Q_g	Total Gate Charge		62				

Reverse Diode Characteristic

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = - 5 V, I_{SD} = 10 A	Fig. 8, 9, 10
		3.1		V	V_{GS} = - 5 V, I_{SD} = 10 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		36	A	T_C = 25°C	Note 2
t_{rr}	Reverse Recover time	32		ns	V_{GS} = - 5 V, I_{SD} = 20 A, V_R = 800 V dif/dt = 2400 A/µs	Note 2
Q_{rr}	Reverse Recovery Charge	192		nC		
I_{rrm}	Peak Reverse Recovery Current	10		A		

Note (2): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Note (3): For inductive and resistive switching data and waveforms please refer to datasheet for packaged device - Part Number C2M0080120D.

Typical Performance

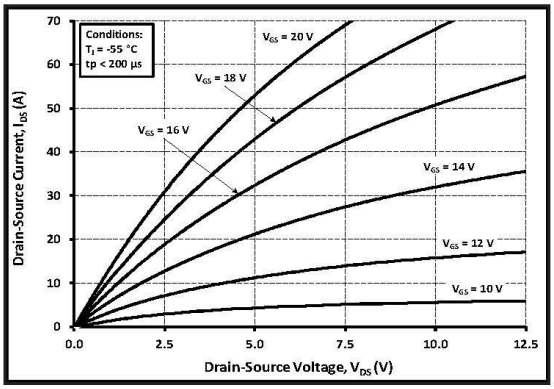


Figure 1. Output Characteristics T_J = -55 °C

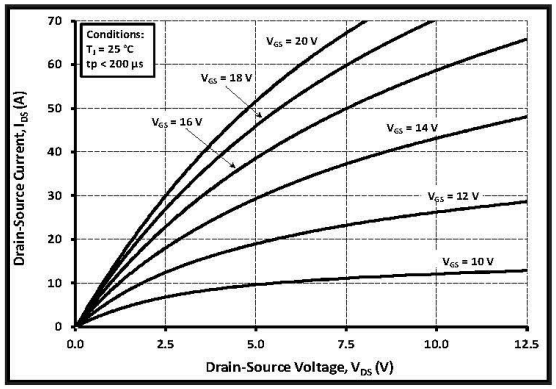


Figure 2. Output Characteristics T_J = 25 °C

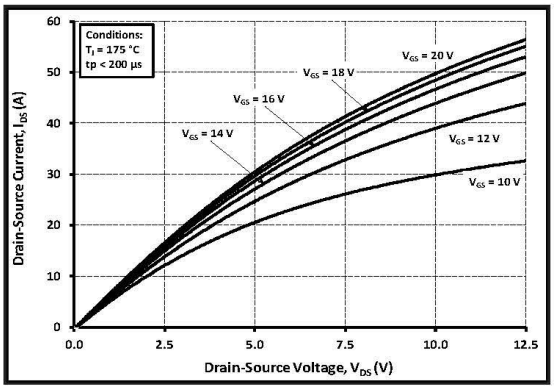


Figure 3. Output Characteristics T_J = 175 °C

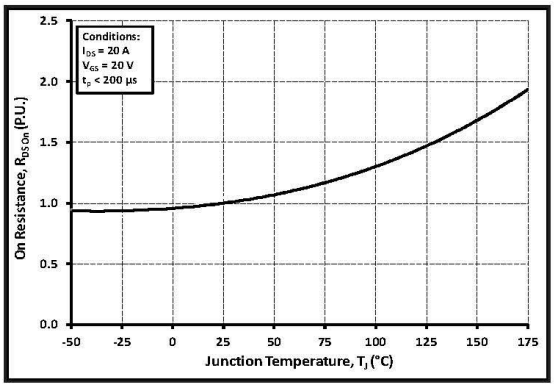


Figure 4. Normalized On-Resistance vs. Temperature

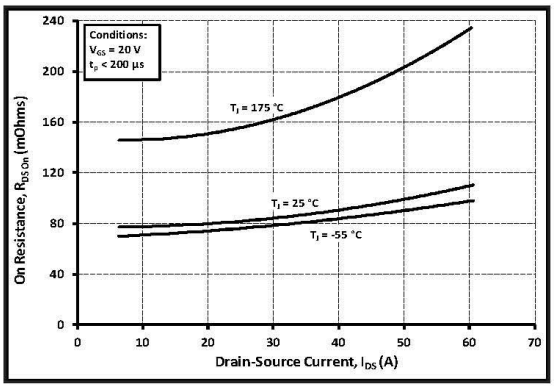


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

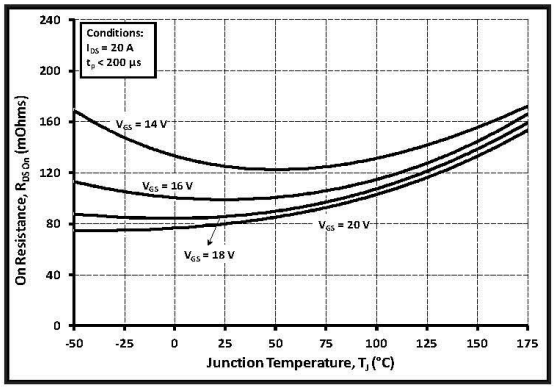


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

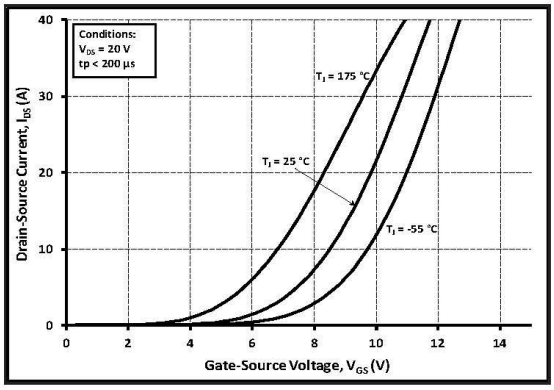


Figure 7. Transfer Characteristic for Various Junction Temperatures

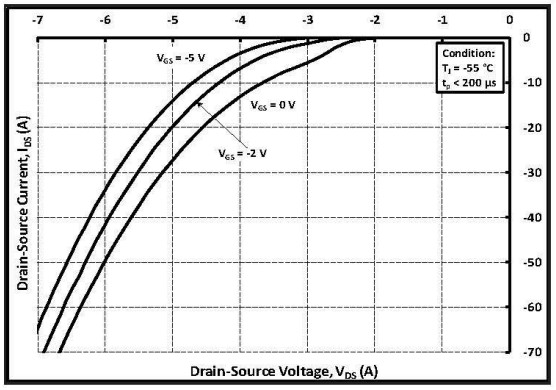


Figure 8. Body Diode Characteristic at -55 °C

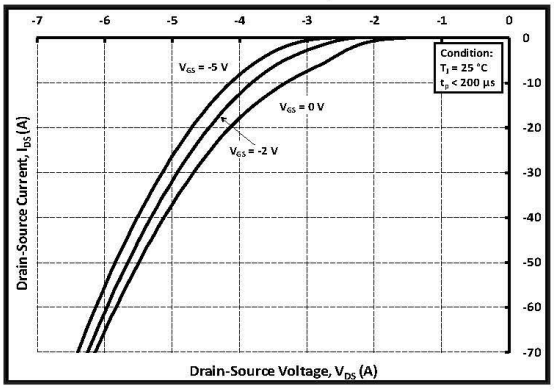


Figure 9. Body Diode Characteristic at 25 °C

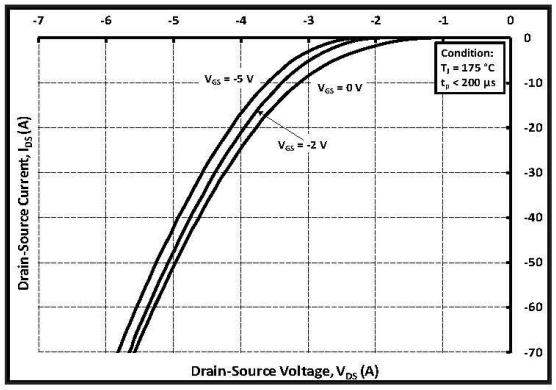


Figure 10. Body Diode Characteristic at 175 °C

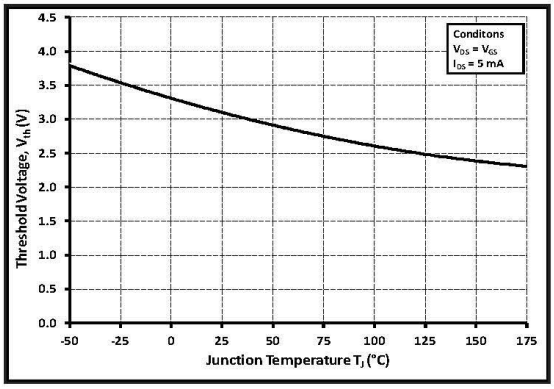


Figure 11. Threshold Voltage vs. Temperature

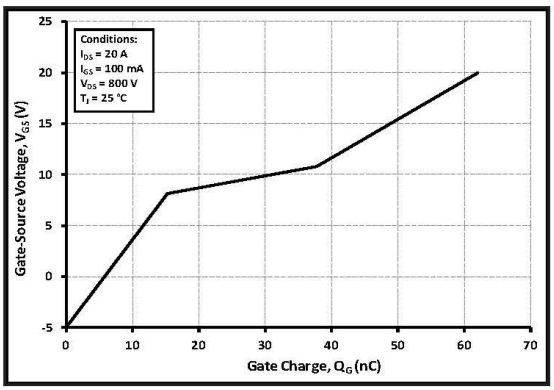


Figure 12. Gate Charge Characteristics

Typical Performance

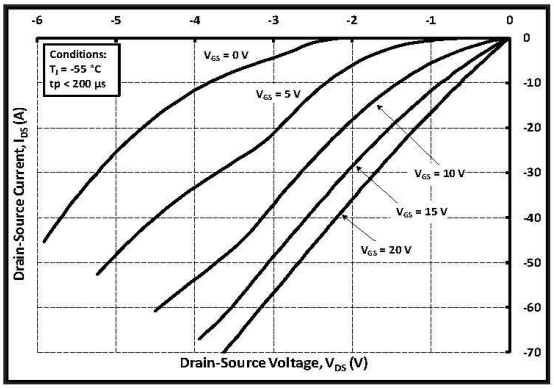


Figure 13. 3rd Quadrant Characteristic at -55 °C

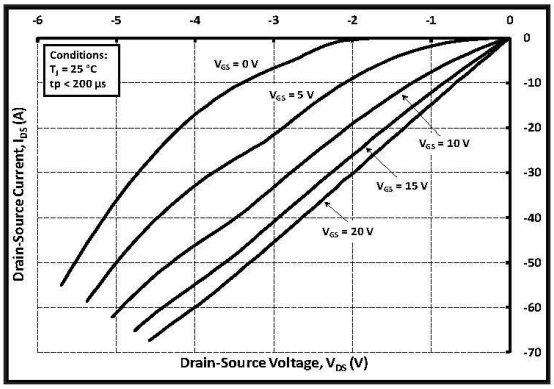


Figure 14. 3rd Quadrant Characteristic at 25 °C

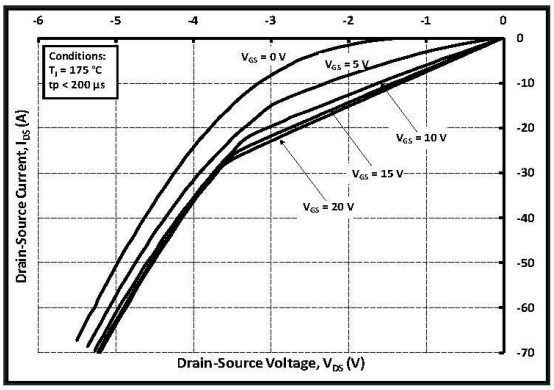


Figure 15. 3rd Quadrant Characteristic at 175 °C

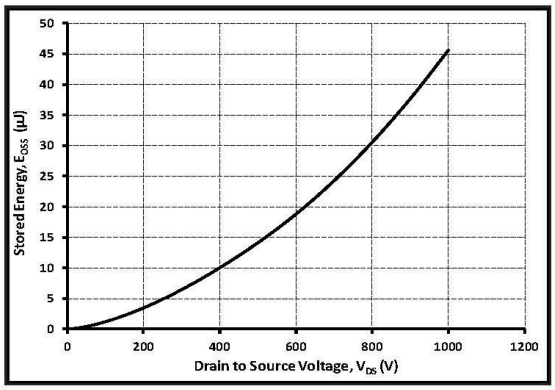


Figure 16. Output Capacitor Stored Energy

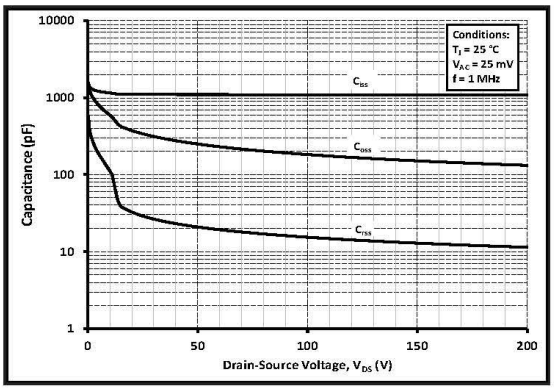


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

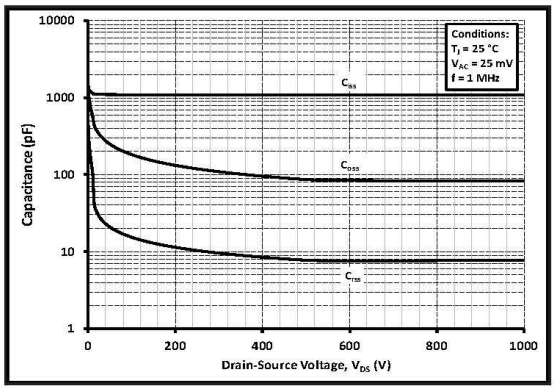
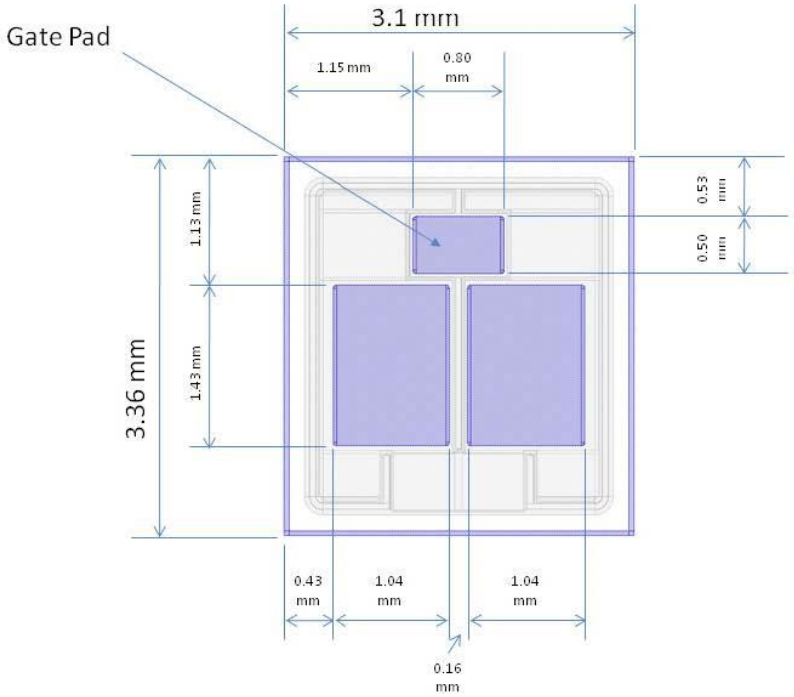


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Mechanical Parameters

Parameter	Typical Value	Unit
Die Dimensions (L x W)	3.10 × 3.36	mm
Exposed Source Pad Metal Dimensions (LxW) Each	1.04 × 1.43	mm
Gate Pad Dimensions (L x W)	0.80 × 0.50	mm
Die Thickness	180 ± 40	µm
Top Side Source metallization (Al)	4	µm
Top Side Gate metallization (Al)	4	µm
Bottom Drain metallization (Ni/Ag)	0.8 / 0.6	µm

Chip Dimensions



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Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

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