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Unbalanced Current Static Compensator

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ABSTRACT

The objective of this thesis is to present and evaluate a solution to the unbalanced current issue that can be found in three-phase electrical power grids. The solution is named unbalanced current static compensator (UCSC) and has the goal of balancing the currents at the source in order to mitigate adverse issues such as of negative- and zero-sequence currents that are generated by three-phase current unbalances.

The solution topology consists of three single-phase H-bridge converters that are controlled through an algorithm working in the $d-q$ frame of reference. The algorithm is divided in three different stages: the phase synchronization and reference current generator stage, the DC-link voltage and current controller stage, and the PWM stage. The design and functionality of the UCSC topology and algorithm is validated through MATLAB/SIMULINK™ simulations.

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I want to express my gratitude to God and my family for giving me the strength to keep moving forward every day.

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DEDICATION

Esta tesis va dedicada a mi madre Maria, mi padre Manuel, mi abuela Celia y a mis dos hermanas, Milena y Angie. Sin su apoyo nunca hubiera llegado hasta donde estoy hoy en día.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivations for This Research

The main systems of an electrical power grid are the generation, transmission, distribution and load systems [1]. The generation system is where the electrical energy is produced, then, the transmission system transports the electrical energy to the distribution system which delivers to the loads of the end users [1].

The distribution system delivers electrical energy to the loads through three-phase primary feeders that divide themselves into three- or single-phase branches and laterals as depicted in Fig. 1-1 [2]. There are three main types of loads [1]:

- residential loads that are mainly single-phase loads;
- commercial loads such as shopping malls, schools and hospitals that are a combination of single- and three-phase loads;
- industrial loads having electric motors, resistive loads, control panels and production equipment being mainly a combination of three- and single-phase loads.

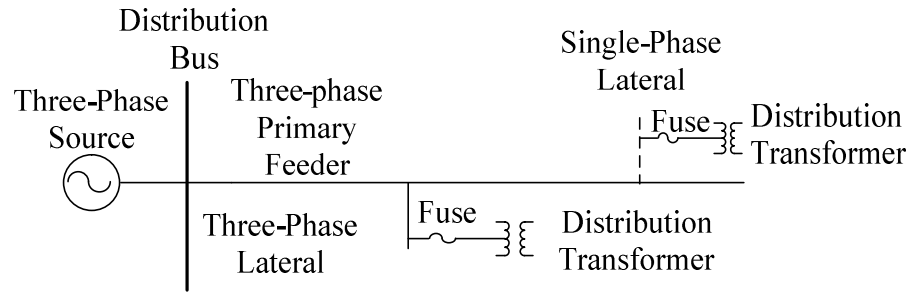

Fig. 1-1. A generic three-phase distribution system [2]

The diversity of the three- and single-phase loads leads to unbalanced loading of three-phase distribution feeders that can present issues such as the raise of the voltage level and circulating current in the neutral conductor of four-wire systems [3]. These two issues may lead to the interruption of power flow to end-user devices, unnecessary relay tripping and also safety concerns since the neutral conductor could be touched by humans [3], [4].

Steady-state unbalanced operation of three-phase systems results in positive- negative-, and zero-sequence components depending on the system wire configuration [5]. Unbalanced cases are studied using analytical tools such as the symmetrical component theory by decomposing the unbalanced three-phase variables such as currents and voltages into three sets of balanced components as illustrated in Fig. 1-2. For counter-clockwise rotation, the sets have following characteristics [6]:

- positive-sequence components consisting of three phasors having equal magnitudes and a 120° phase shifts between them;
- negative-sequence components consisting of three phasors having equal magnitudes and a 120° phase shifts between them;
- zero-sequence components consisting of three phasors having equal magnitudes and a 0° phase shifts between them.

Synchronous generators can also be affected by unbalanced loading of three-phase distribution feeders. The unbalance can produce a decrease in the generator efficiency due to the overheating of the rotor circuits [7], [8]. The damage to the rotor circuits may also happen because the negative-sequence current leads to the generation of a magneto motive force (MMF) which interacts with the MMF that is generated by the positive-sequence component of the currents.

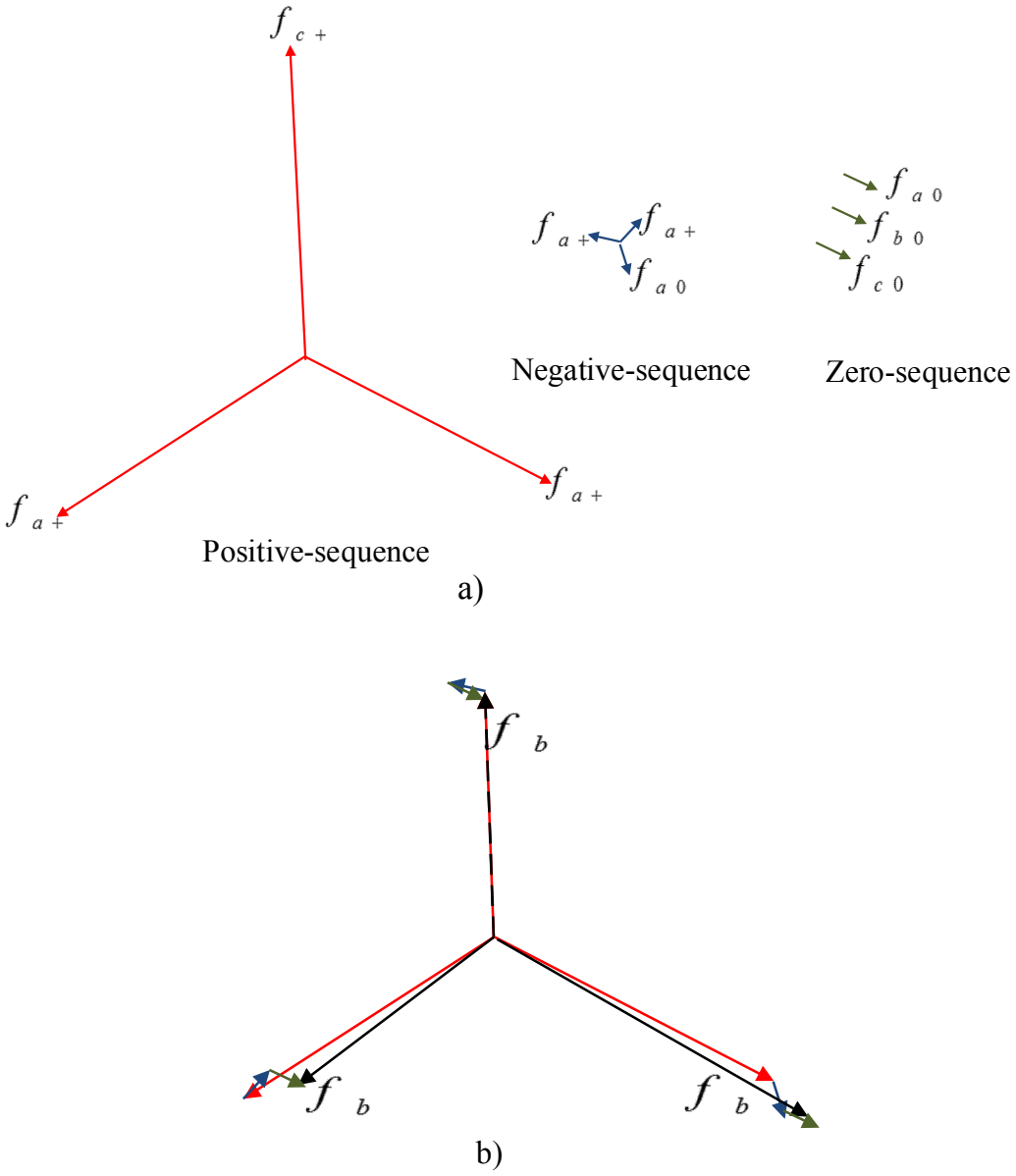

Fig. 1-2. a) Symmetrical components of an unbalanced three-phase set of variables. b) Addition of the symmetrical component phasors

This interaction produces a torque with a sinusoidal variation at a higher frequency than the fundamental frequency, and results in the velocity of the machine during steady-state condition not being constant [9].

Negative-sequence current components can also produce issues like supersynchronous resonance and subsynchronous resonance on generator turbine blades [8]. So, accidents could happen if the negative-sequence current caused by unbalanced systems is not reduced [8].

Likewise, induction motors are also affected by unbalanced voltages due to the negative-sequence currents. Some of the issues produced by negative-sequence currents are [10]:

- an heterogeneous distribution of heat in the stator due to unbalanced currents;
- additional copper losses in the rotor and stator circuits;
- increased noise;
- increased vibrations that can cause damage to insulation, bearings and interconnecting mechanical equipment.

Lastly, three-legged-core grounded wye-grounded wye transformers may experience tank heating during unbalanced scenarios due to the absence of iron-core return path for the zero-sequence fluxes that leads to the flow of zero-sequence fluxes through the transformer air gap and tank where fluxes induce eddy currents that cause tank heating [11].Another problem that may be caused by unbalanced currents in distribution feeders is an increase of investment and operating costs of the system [4].

Unfortunately, the unbalanced loading issue has been around for a long time and has not been fully addressed but some solutions to unbalanced currents are presented in the literature and will be briefly described in the next section [8], [12]-[14].

1.2 Existing Solutions to Three-Phase Unbalanced Currents

There are some solutions proposed in the literature that provide their own unique ways to correct unbalanced loading in distribution systems. Three of these solutions are the following:

- negative-sequence current reduction for generator/turbine protection [8];
- voltage and current unbalance compensation using a static var compensator [12];
- a solution for three-phase unbalanced system loading based on PWM AC choppers [13].

Negative-Sequence Current Reduction for Generator/Turbine Protection

The solution proposed in [7] consists in the application of a special-function static var compensator (SVC) that would compensate for only the reactive component in order to reduce the negative-sequence current at the generator terminals. According to [7], the main reasons to not compensate for the active component are:

- the control algorithm would be too complicated;
- high cost of installation and operation.

Reference [7] states that some utilities adopt passive solutions to this issue; for example:

- Generator units are disconnected from the system once the negative-sequence current level reaches a pre-established limit; this is not an attractive solution since other units would need to pick up the power deficit;
- A temporary rearrangement of the distribution system in order to achieve a balanced condition but it could generate issues with the protection scheme.

Voltage and Current Unbalance Compensation Using a Static Var Compensator (STATCOM)

The STATCOM solution proposed in [12] provides reactive compensating currents to correct the voltage and current unbalances. This is achieved by providing reactive power in three-phase three-wire systems with loads where the active component is balanced. The proposed

topology depicted in Fig. 1-3 consists of a three-phase inverter connected in parallel with the load through an L-C filter.

The compensation process is performed by three control schemes [12]:

- current control for unbalanced currents;
- voltage control for unbalanced voltages at the PCC;
- integrated control for both functions.

The three controller schemes in [12] are based on the reactive instantaneous compensation theory proposed in [14] instead of the $d-q$ frame of reference theory that is used in the UCSC system. The equations defining the instantaneous power theory are the following [12]:

$$p(t) = \boldsymbol{v}^T(t)\boldsymbol{i}(t) \tag{1-1}$$

$$P(t) = \frac{1}{T_c}\int_{t-T_c}^{t} p(\tau)d\tau \tag{1-2}$$

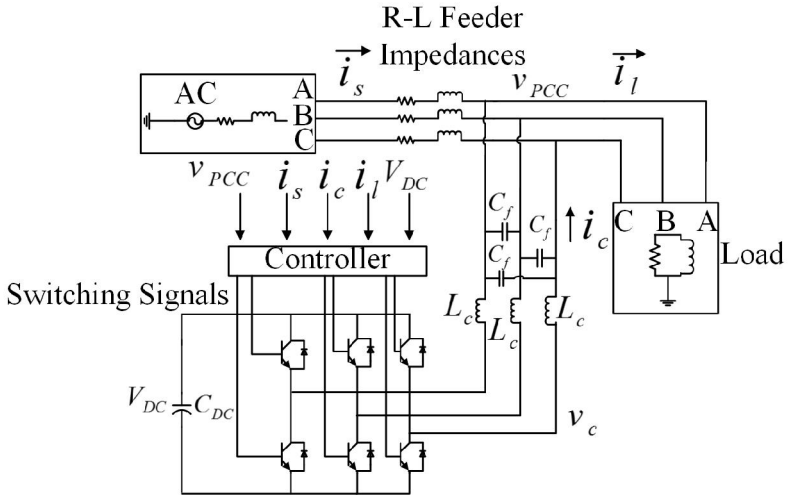

Fig. 1-3. Compensator configuration proposed in [12]

where

- $p(t)$ is the instantaneous power;
- $P(t)$ is the average power;
- $\boldsymbol{v}^T(t)$ is the transpose of the voltage vector;
- $\boldsymbol{i}(t)$ is the current vector;
- T_c is the averaging interval.

- ***Current Controller Scheme***

For the current control scheme depicted in Fig. 1-4, the compensator provides the reactive component in the load to balance the source currents and provide unity power factor [1]. The equation that defines the reactive component of the load current is the following [12]:

$$\boldsymbol{i}_{active}(t) = \frac{P(t)}{V_p^2(T)}\boldsymbol{v_p}(t) \tag{1-3}$$

$$\boldsymbol{i}_{reactive}(t) = \boldsymbol{i_l}(t) - \boldsymbol{i}_{active}(t) \tag{1-4}$$

where $\boldsymbol{v_p}(t)$ and $\boldsymbol{i_l}(t)$ are the reference voltage and load current vectors, respectively. $\boldsymbol{i}_{active}(t)$ and $\boldsymbol{i}_{reactive}(t)$ are the active and reactive instantaneous components of the load current. $V_p(t)$ is the rms value of $\boldsymbol{v_p}(t)$.

The compensating current is composed by the following two terms:

$$\boldsymbol{i}_c^* = \boldsymbol{i}_{c1}^* + \boldsymbol{i}_{c2}^* \tag{1-5}$$

where

- $\boldsymbol{i}_c^*$ is the total reactive compensating current vector;
- $\boldsymbol{i}_{c1}^*$ is the reactive current vector required to balance the currents at the source;

- $\boldsymbol{i}_{c2}^{*}$ is the active current vector absorbed by the STATCOM in order to regulate the DC-link voltage to a constant value.

The rest of the variables involved in the algorithm are the following:

- $\boldsymbol{v}_{PCC}$ is the voltage vector at the PCC;
- $\boldsymbol{i}_{l}$ is the load current vector;
- v_{DC} is the DC-link voltage;
- v_{DC}^{*} is the DC-link voltage reference;
- $\boldsymbol{v}_{c}^{*}$ is the generated control voltage vector for the generation algorithm of the switching signals.

This type of algorithm would only balance the currents measured at the source if the active component of the load is balanced. This is because the STATCOM only provides reactive compensating currents to the grid.

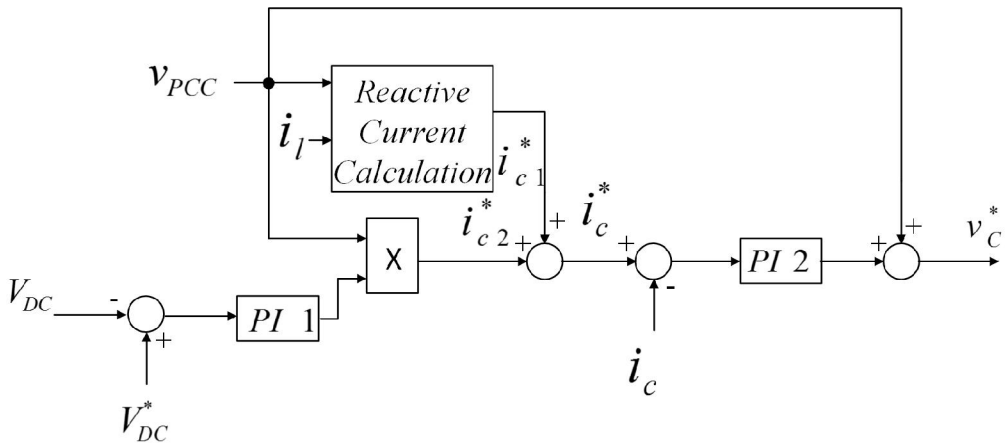

Fig. 1-4. Current controller scheme proposed in [12]

- ***Voltage Controller Scheme***

The other scheme proposed in [12] is the voltage controller scheme illustrated in Fig. 1-5. The principle of operation consists of having independent control of each phase voltage magnitude. The goal is to have equal magnitudes for v_{PCC} and v_c. This is accomplished by [12]:

a) absorbing reactive current from the grid when the magnitude of v_c is lower than the magnitude of v_{PCC}, or;

b) the STATCOM injects reactive power into the system when v_c is higher than v_{PCC}.

The phase-angle shift block is used to generate the necessary phase shift so that the controller absorbs active current to regulate the DC-link voltage [12]. This voltage regulation function at the PCC is not present in the UCSC system but could be designed and implemented in future work.

- ***Integrated Controller Scheme***

The integrated controller scheme proposed in [12] depicted in Fig. 1-6 performs both functions: current compensation and voltage compensation.

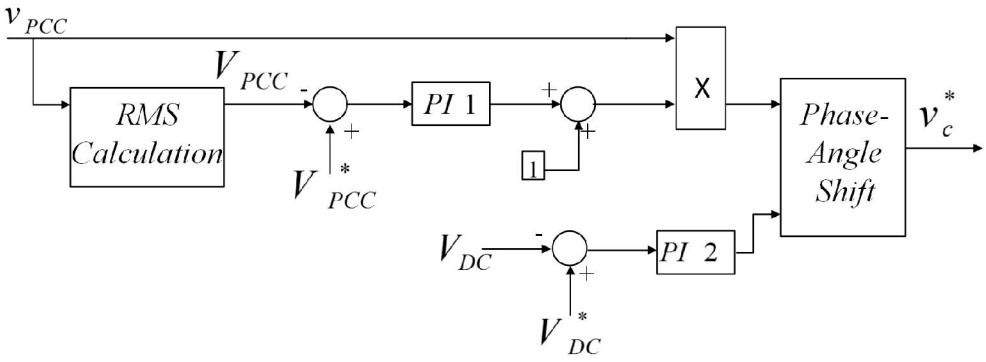

Fig. 1-5. Voltage controller scheme proposed in [12]

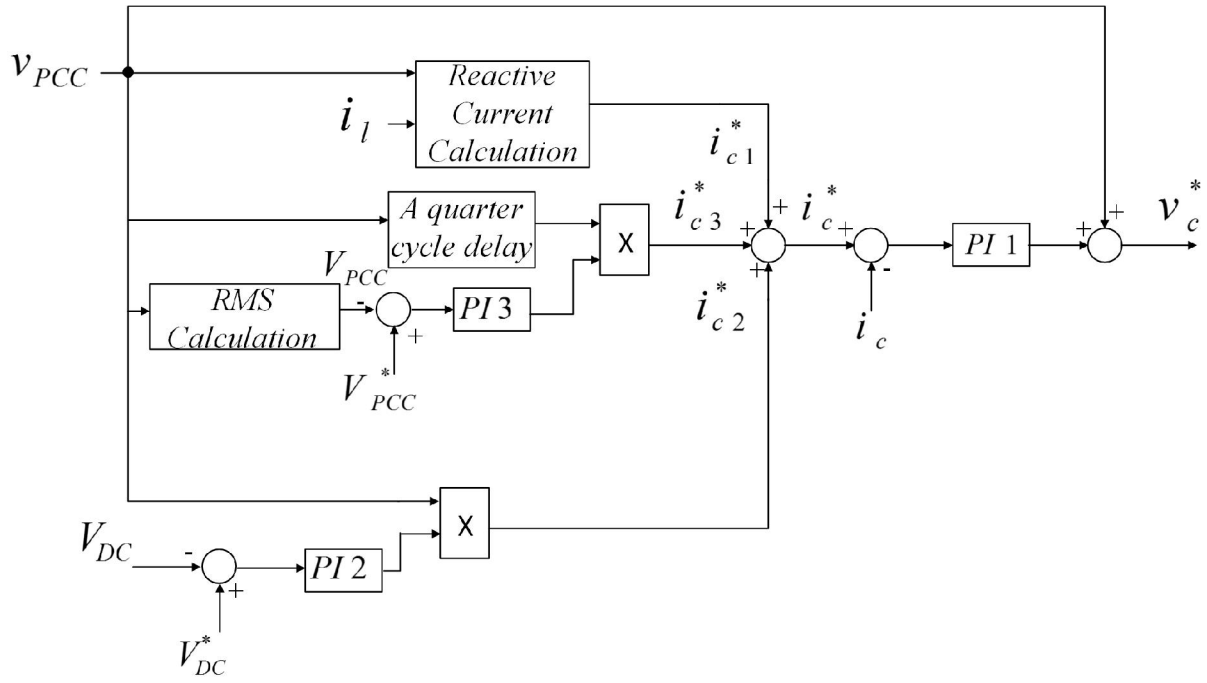

Fig. 1-6. Integrated controller scheme proposed in [12]

PWM AC Choppers for Three-Phase Systems with Load Unbalance

The solution presented in [13], is oriented for cases when users are connected only to two phases as depicted in Fig. 1-7 a. Reference [13] mentioned that the issue of unbalanced systems can be solved by applying the Steinmetz Bridge [15] that is illustrated in Fig. 1-7 b from [13]. The bridge consists of capacitors and reactors that balance the source currents.

However, the Steinmetz Bridge has the drawback of requiring tuning the load current changes; that is the compensator elements need to change in order to re-balance the system. This issue can be addressed by having variable compensator capacitor and reactor banks [13]. However, other issues arise with this approach. Transients due to the switching of the compensator elements plus over-voltages and over-currents potentially generated due to the inductors and capacitors [13].

The PWM AC chopper solution illustrated in Fig. 1-8 is proposed in [13] in order to avoid the issues that come with the switching of capacitor and inductor banks. This approach is based on the DC/DC buck converter and the output voltage is dependent of the duty cycle as illustrated in the following equations [13]:

$$I_a = \frac{V_{AB}\alpha_1^2}{\frac{1}{j2\pi f C_{comp}} + j2\pi f L_{out}} \tag{1-6}$$

$$I_b = \frac{V_{BC}\alpha_1^2}{\frac{1}{j2\pi f L_{comp}}} \tag{1-7}$$

$$\alpha_1 = \sqrt{\frac{I_a\left(\frac{1}{2\pi f C_{comp}} + 2\pi f L_{out}\right)}{V_{AB}}} \tag{1-8}$$

$$\alpha_2 = \sqrt{\frac{I_b(2\pi f L_{comp})}{BC}} \tag{1-9}$$

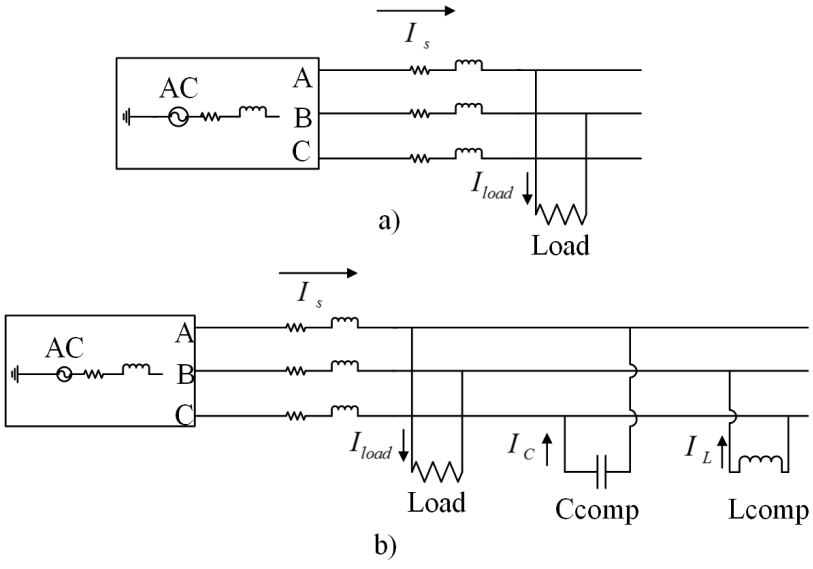

Fig. 1-7. a) Unbalanced system schematic [13]. b) Steinmetz Bridge from [13]

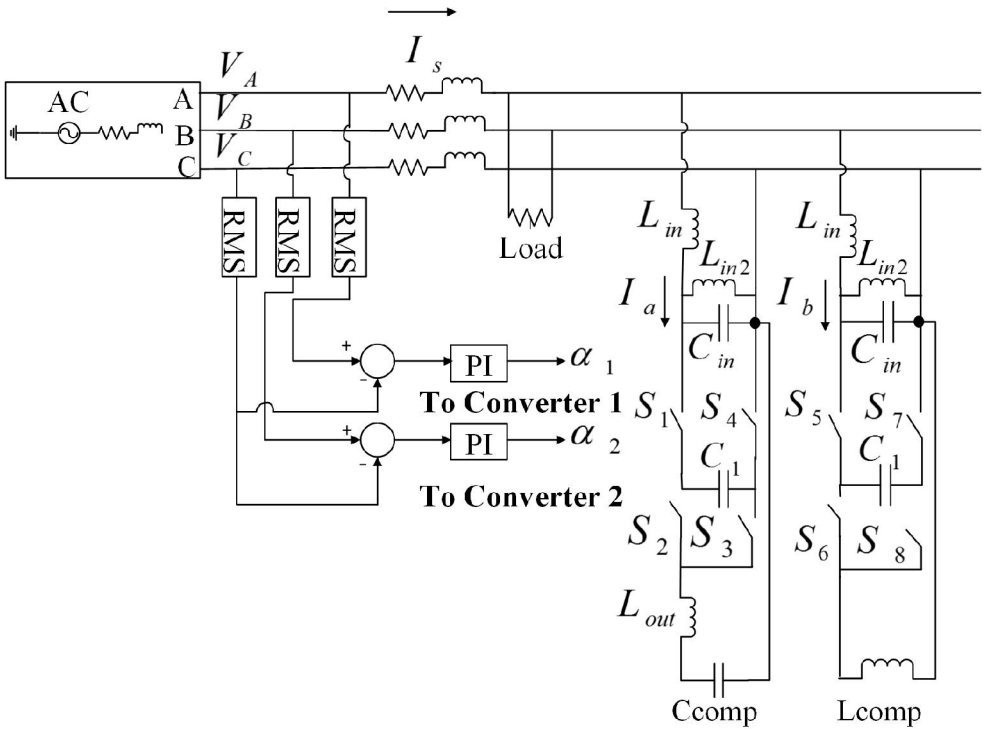

Fig. 1-8. AC-choppers solution proposed in [13]

This solution while being cheap and robust as noted in [13], is only applicable f or specific cases with loads connected only to two phases.

The solutions proposed in [8], [12] and [13] approach the unbalanced current issue from different perspectives. Also, these solutions are designed to provide reactive compensating currents; therefore for cases where the active component of the load is unbalanced the application of these solutions is limited.

By finding a solution to the unbalanced load issue, power systems would be more reliable, secure and efficient leading to costs savings for the utilities. Future load growths and interconnection with the main grid of isolated circuits would also become easier to handle for the utilities. Furthermore the generation of energy with higher power quality and lower electricity

prices should attract more customers to a particular area. All this will help utilities to become more competitive [10].

1.3 Thesis Objectives

The main objective of this thesis is to develop a solution that would be able to balance the source currents in a power system having unbalanced loads. The solution will be called: Unbalanced Current Static Compensator (UCSC). In order to accomplish this objective, the following enabling objectives should be accomplished:

- an understanding of the theoretical background of the UCSC system;
- a knowledge of the p-q theory as applied to single-phase systems;
- the design of voltage controller for the DC link of the UCSC;
- MATLAB/SIMULINK^{TM} simulations of an unbalanced three-phase four-wire system coupled with the UCSC solution;
- an evaluation of the simulation results.

1.4 Case Study of a Distribution System with Unbalanced Loading

A case study must be selected in order test the proposed ideas for the unbalanced loading issue. The case study is based on a 34.5 kV unbalanced three-phase four-wire distribution system fed from a power substation.

The current unbalance for the case study is based on the current profile depicted in Fig. 1-9. At the 22h:00m:00s, the values of the phase currents are 45.99 A, 36.27 A and 38.33 A for phases *a*,*b* and *c*, respectively.

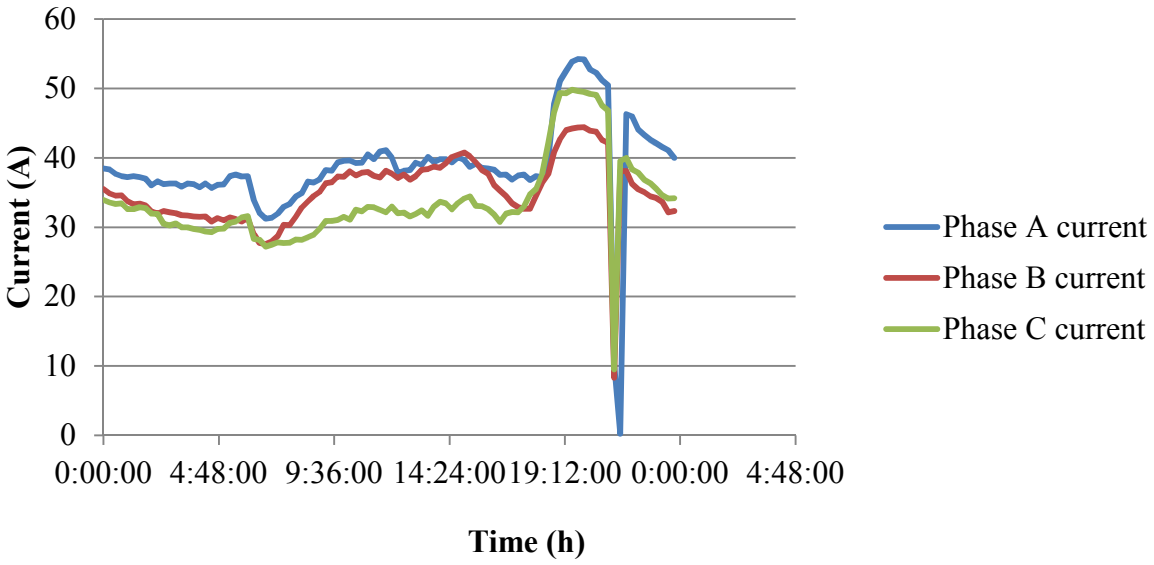

Fig. 1-9. Current profile of an unbalanced 34.5 kV three-phase distribution feeder

This unbalance leads to a difference of 9.72 A and 7.66 A between phases *a*-*b* and *a*-*c*, respectively. This unbalanced condition generates negative- and zero-sequence current magnitudes of 4.43 A and 5.14 A, respectively, that can cause the issues discussed in section 1-1.

In order to address this unbalance, a topology for the UCSC system must be chosen. During the initial stage of the UCSC project, several topologies were being considered as broadly classified in Fig. 1-10:

- three-phase three-legged converters (refer to Fig. 1-11 and Fig. 1-12;
- three-phase four-legged converter (refer to Fig. 1-13).
- three single-phase H-bridge converters (refer to Fig. 1-14);

The topology of Fig. 1-11 is implemented in the solution proposed by [12] and analyzed in section 1.2. The topologies depicted in Figs. 1-12 and 1-13 are presented in [16] and [17] to be used as the source for unbalanced loads.

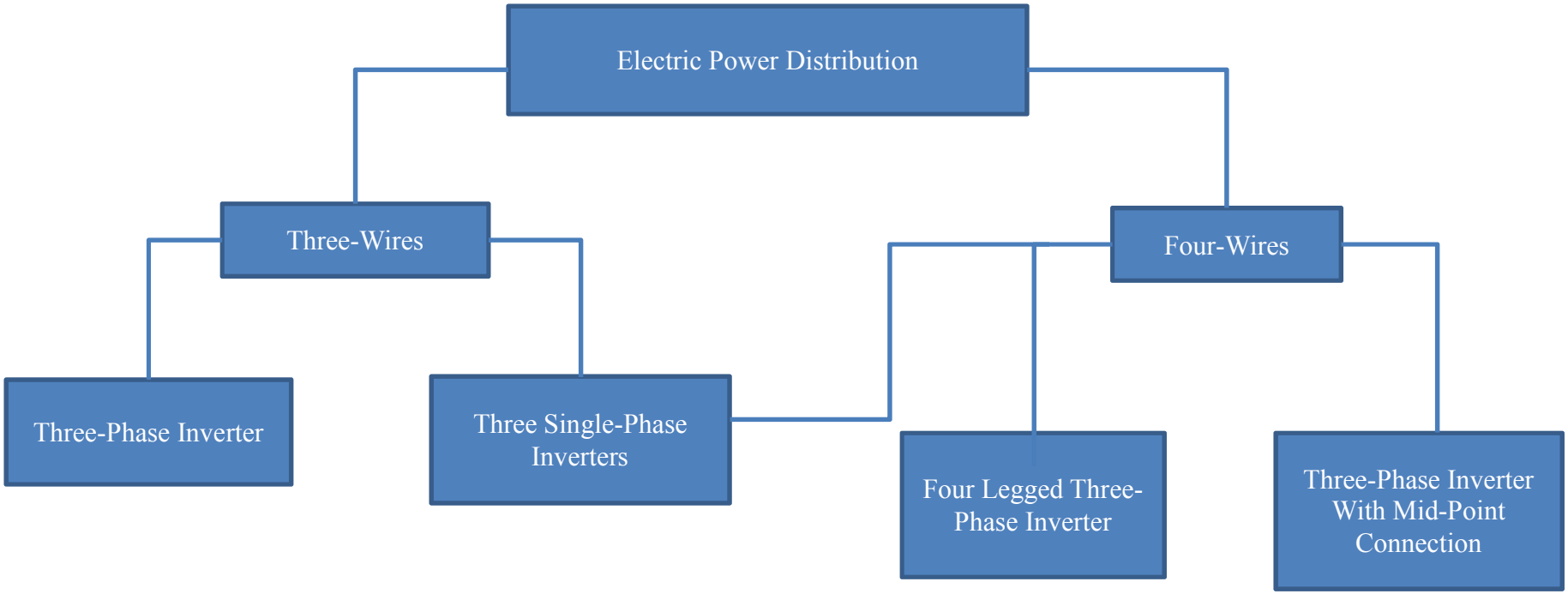

Fig. 1-10. Inverter topologies

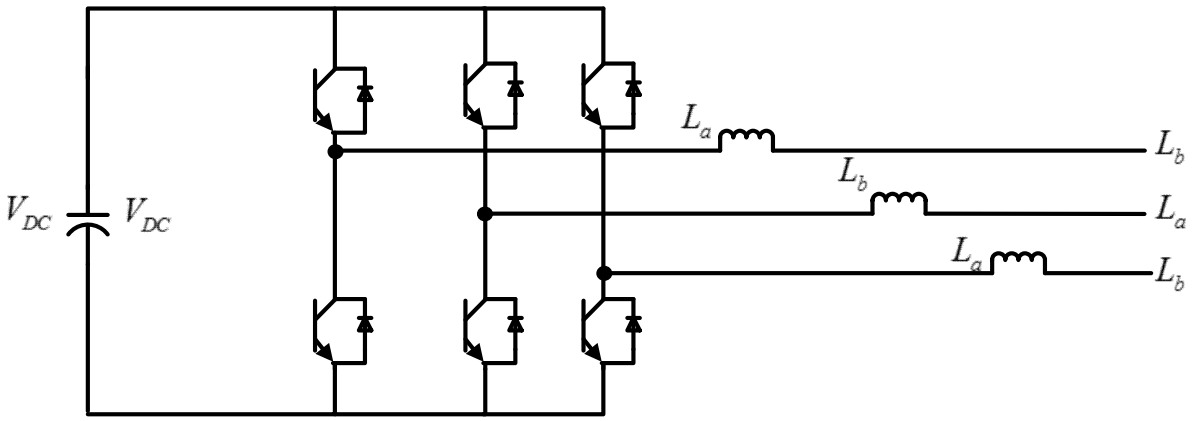

Fig. 1-11. Three-phase three-wire inverter topology

The three-phase three-wire inverter of Fig. 1-11 has six switches and also one capacitor in the DC link. Because the case study is based on a three-phase four-wire system, this type of topology is not suitable for the UCSC project.

Only the three-phase four-wire with mid-point, the four-leg inverter and the three single-phase inverters topologies are suitable for the UCSC project. The converter of Fig. 1-12 needs to have two capacitors instead of one. The neutral point connection of the topology presented in Fig. 1-12 has the goal of making the three phases independent of each other [18]. This topology has the following drawbacks when supplying unbalanced loads [17], [18]:

- distortion in the symmetrical output voltage for unbalanced loads;
- large capacitors and high DC-link voltage are needed to mitigate the voltage ripple generated by the zero-sequence current that flows across the capacitor;
- small utilization of the DC-link voltage;
- the dependency of the modulation factor of the load current. According to [18], the modulation factor is dependent of the load current. The maximum value is reached when the load is balanced and it's reduced when the load becomes unbalanced [18].

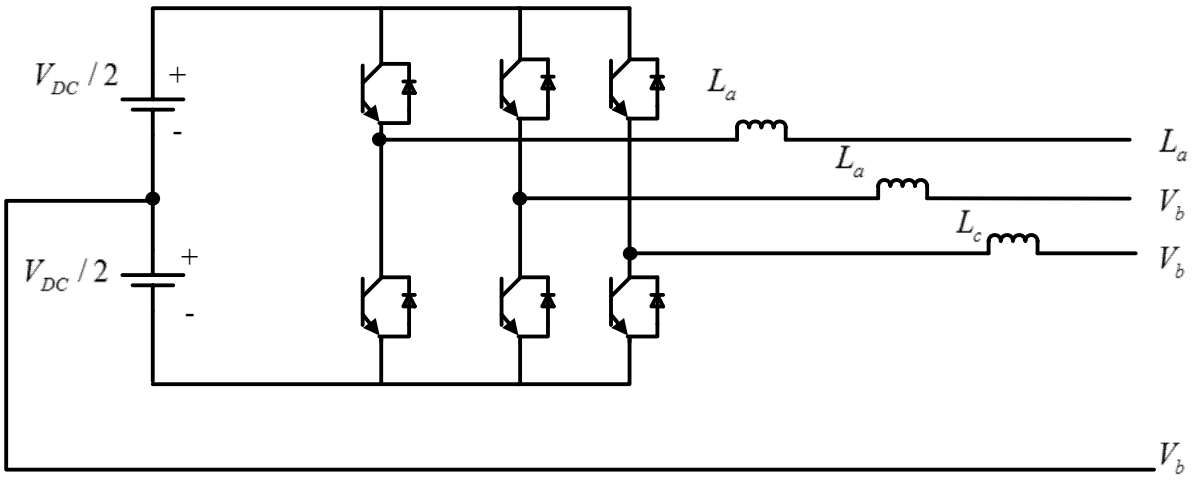

Fig. 1-12. Three-phase four-wire inverter topology

- superposition of a DC component with the output AC voltage;
- power losses due to the zero-sequence current in the DC link.

The three-phase four-leg inverter consists of eight switches and one capacitor in the DC link. The advantages of the three-phase four-leg inverter are the following [18], [19]:

- small DC-link capacitor;
- no zero-sequence current across the DC-link capacitor;
- more DC-link voltage utilization in comparison with the three-phase three-legged converter with mid-point connection. This is due to the fact that the maximum line-to-neutral output voltage that can be reached is $0.577V_{DC}$in comparison with the $0.5V_{DC}$ value that can be reached in a three-phase inverter with mid-point connection.

The main drawback for the three-phase four-legged converter is that the control algorithm is more complex than the algorithm required for a conventional three-legged converter [19]. This is one of the reasons that makes the three single-phase H-bridge converters more attractive since the control approach is simpler. Other reasons are the independent control of each phase current

the higher DC-link voltage utilization just like the three-phase four-legged inverter topology. The drawback is that 12 switches are required. Taking all of the above into account, this thesis focuses on the topology composed of three single-phase H-bridge converters as the starting point for the quest for a cost-effective solution for unbalance loading of distribution feeders.

After presenting the unbalanced case and the UCSC topology, the one-line diagram of the case study and its elements are illustrated in Fig.1-14:

- the 34.5 kV power substation;
- the feeder impedances for segment 1 and 2;
- the three-phase unbalanced load;
- the single-phase UCSC-coupling transformers T1, T2 and T3;
- the UCSC system.

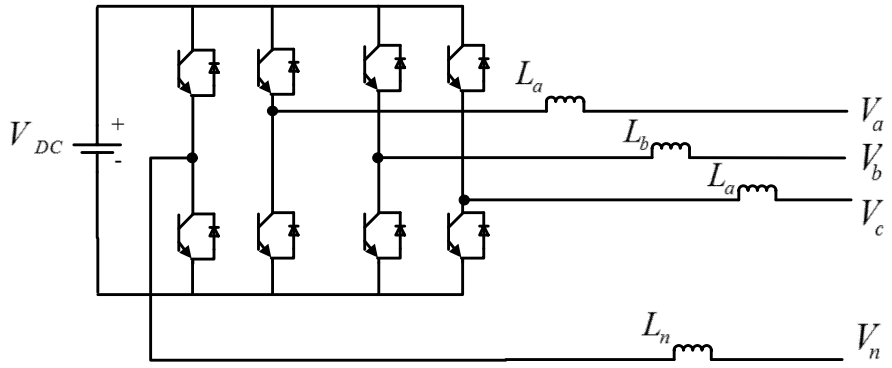

Fig. 1-13. Three-phase four-legged inverter topology

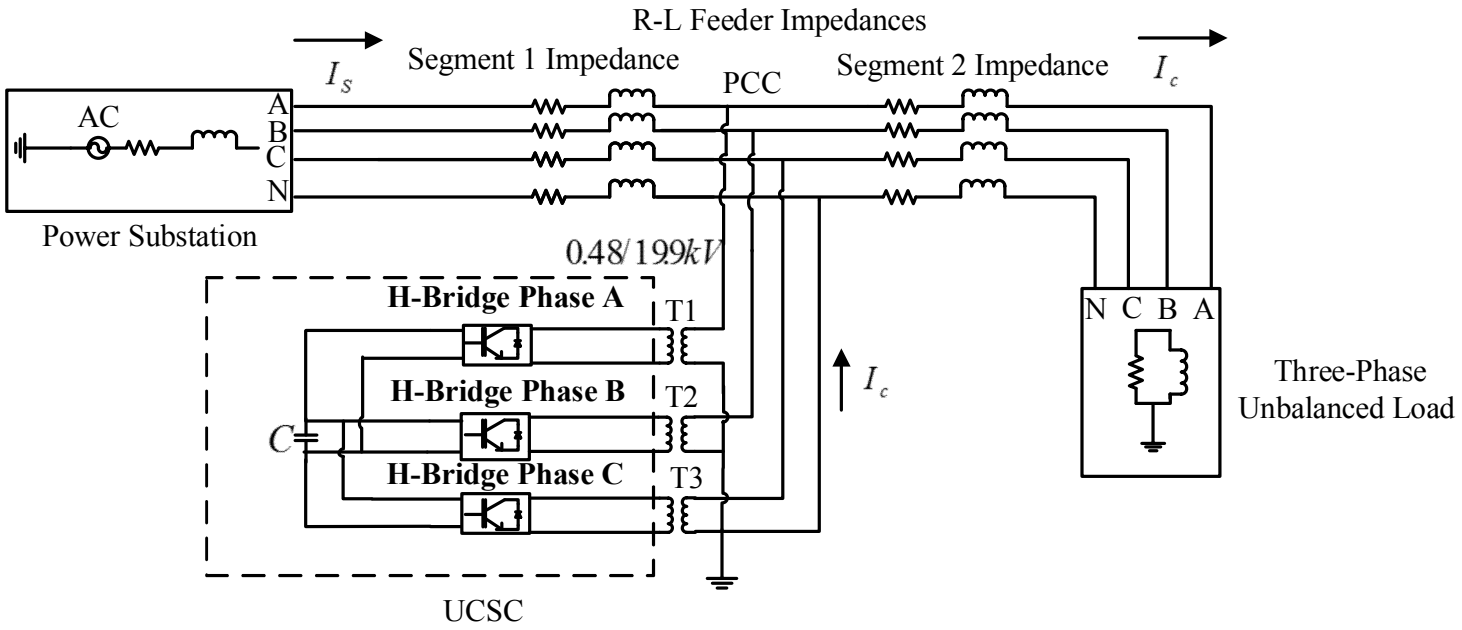

Fig. 1-14.One-line diagram for the case study

1.5 Thesis Organization

A theoretical background of the system elements will be presented in chapter 2 that starts with an overview of reference frame theory followed by brief descriptions of the components and modes of operation of the H-Bridge. A description of the UCSC and its control algorithm are given in chapter 3.

The model parameters and the analysis of the MATLAB/SIMULINKTM simulations are presented and evaluated in chapter 4. Models of the three-phase four-wire distribution systems and the UCSC control algorithm are presented. These models are built using MATLAB/SIMULINKTM blocks. The conclusions and the recommendations for future work are presented in chapter 5.

1.6 Conclusions

The following conclusions can be drawn from chapter 1:

- the diversity of the three- and single-phase loads leads to unbalanced loading of three-phase distribution feeders [3];
- steady-state unbalanced operation of three-phase systems results in positive-negative-, and zero-sequence components depending on the system wire configuration [5].
- synchronous generators and induction motors are affected by the negative- and zero-sequence currents generated by unbalanced loading;
- the solutions presented in this chapter are limited to cases where only the reactive compensating currents are needed to balance the source currents.

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CHAPTER 2

SYSTEM FUNDAMENTAL CONCEPTS

2.1 Background Concepts Related to Power Electronic Converters

An overview of fundamental concepts used in the development and analysis of the proposed UCSC solution should be presented before a detailed description of the case study. Hence, this chapter focuses on the description of the modes of operation and control algorithm for single-phase inverters.

Power electronic converters can be defined as multiport circuits composed of semiconductor switches and are used to interface subsystems that cannot be connected directly because of their different characteristics such as voltage level or type, frequency, phase angle and number of phases. This interface is necessary so that the subsystems are able to exchange electric power between them [1]. Power electronic converters can be classified as follows [1]:

- AC/AC converters interfacing two AC subsystems;
- DC/DC converters interfacing DC subsystems;
- the DC/AC converters where a DC subsystem is interfaced with an AC subsystem.

The DC/AC converter category can be further divided into rectifiers and inverters. The power flows from the AC-side to the DC-side in rectifiers and power flows in the opposite direction (from the DC-side to the AC-side) in inverters [1]. So, the converters are composed of power semiconductor devices (switches) that are controlled (turned on and off) by gating signals that determine the current flow through a circuit branch [1].

Power electronic converters can be further classified depending on the switching method [2]:

- *line frequency (naturally commutated) converters*: the switching process is started by the change of polarity of the AC voltage [1]. The switching frequency on this case has the same value of the line frequency [2].
- *Switching (forced commutated) converters*: The three main characteristics are [1],[2]
    - the switching frequency is higher than the line frequency;
    - the turn on/off is a controlled process;
    - switches must have gate turn-off capability.
- *Resonant and quasi-resonant converters*: The switching is performed at zero voltage and/or zero current.

Another aspect used to classify the converters is the DC-side waveforms. If the DC-side current direction is changed in order to control the power flow, then, it is named a voltage-sourced converter (VSC). If the DC-side current remains constant and the DC-side voltage direction is changed to control the power flow, then, it is named a current-sourced converter (CSC) [1]. The VSC is the most suitable option given the fact that one of the goals of the UCSC project is to have independent control of the phase currents. Thus, the rest of the chapter focuses on VSCs that can be further classified as follows [2]:

- *Pulse-width-modulated (PWM) inverters:* This type of converter is characterized by output AC voltages were the magnitude and frequency are controlled by pulse-width-modulated switches. The input DC voltage remains constant during the converter operation [2].
- *Square-wave inverters*: Instead of using PWM techniques, square-wave converters modify the input DC voltage to control the magnitude of the output AC voltages. Only the frequency is controlled through the switching devices [2].

- *Single-phase inverters with voltage cancellation*: This type of converter is used when the input DC voltage is constant and when PWM is not applied. A combination of the PWM and square-wave control techniques is required to control the magnitude and the frequency of the output AC voltage [2].

The converters can be also classified as single- or three-phase converters and two of the most common topologies are half H-bridge or full H-bridge [1]. Section 2.2 addresses the full H-bridge single-phase converter which will be referred to as H-bridge converter hereinafter. The schematic of the H-bridge converter is given in Fig. 2-1.

2.2 H-Bridge: Rectifier and Inverter Operations

One of the characteristics of the UCSC system is that it is capable of absorbing and injecting active and reactive powers into a three-phase system. This means that the converters of the UCSC system should be able to operate as rectifiers and also as inverters. Based on Fig. 2-1, the converter operates as a rectifier when i_g (in blue) and v_t (in red) have opposite signs and as an inverter when the signs are equal [2].

PWM Algorithm

The rectifier/inverter operation is controlled by the switching signals of the semiconductor switches. One of the methods to generate the switching signals is the PWM switching scheme commonly called "sine-triangle" PWM technique [2]. The PWM scheme generates the switching signals by comparing a sinusoidal signal that has the desired frequency

fundamental f_1 with a triangular signal whose frequency is the switching frequency f_{sw} of the converter, also called the carrier frequency.

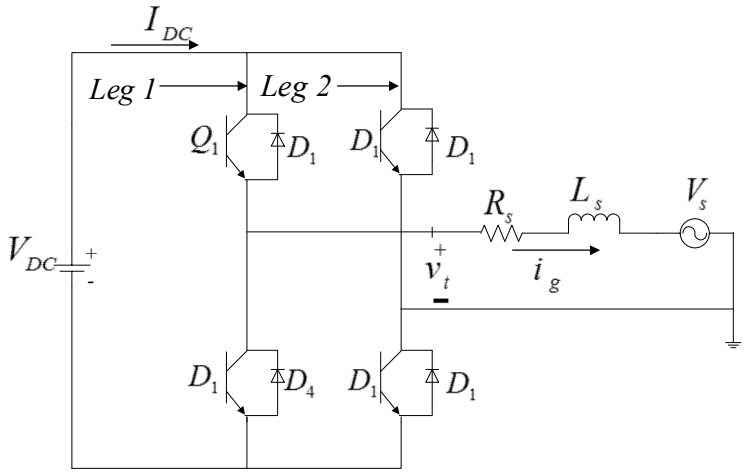

Fig. 2-1. Single-phase H-bridge converter

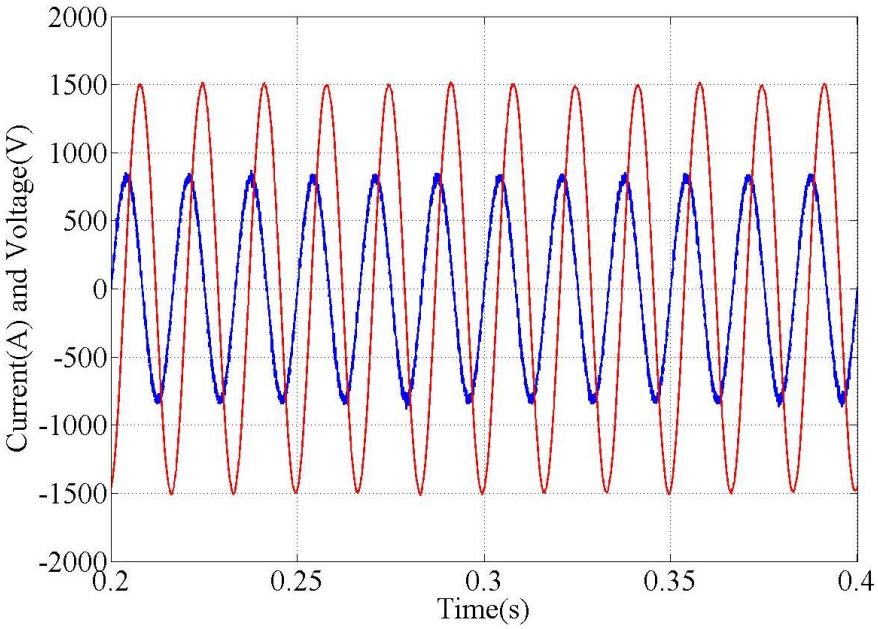

Fig. 2-2. Filtered single-phase H-bridge output waveforms [2]

The sinusoidal signal (control signal) and the triangular signal are related by two modulation ratios: the amplitude modulation ratio (m_a) and the frequency modulation ratio (m_f) where m_a and m_f can be defined as follows [2]:

$$m_a = \frac{\hat{V}_{sin}}{\hat{V}_{tri}} \tag{2-1}$$

$$m_f = \frac{f_{sw}}{f_1}. \tag{2-2}$$

where

- $\hat{V}_{sin}$ is the peak magnitude of the sinusoidal control signal;
- $\hat{V}_{tri}$ is the peak magnitude of the triangular waveform signal;

The following guidelines for m_a and m_f values should be taken into consideration for the design of a converter system [2]:

- m_a should be less or equal than 1 in order for the amplitude of the fundamental-frequency component to vary linearly with m_a. Values of m_a above 1 end up in distorted output voltages that are undesirable in applications such as uninterruptible power supplies [2].
- In order to avoid subharmonics, the value of m_f should be an integer. An odd integer is preferred in most cases except when working with single-phase converters controlled by PWM unipolar voltage switching scheme [2].

The reduced harmonic content is an important reason to choose the unipolar PWM voltage switching scheme over the bipolar PWM voltage switching scheme [2]. Other characteristics of the unipolar PWM switching scheme are the following [2]:

- The output voltages of legs 1 and 2 are controlled independently. The sinusoidal control signal (v_{sin}), is compared to the triangular signal (v_{tri}) to control leg 1. In order to control leg 2, $-v_{sin}$ is compared with v_{tri} in order to generate the switching signals.
- Contrary to the case of the bipolar PWM switching scheme where the output voltage varies between the positive and negative values of V_{DC}, the output voltage for unipolar PWM changes between V_{DC} and zero or between zero and $-V_{DC}$ as illustrated in Fig. 2-3.

Another important topic that must be studied in order to understand the operation of the UCSC system is the current control scheme that is addressed in section 2.3.

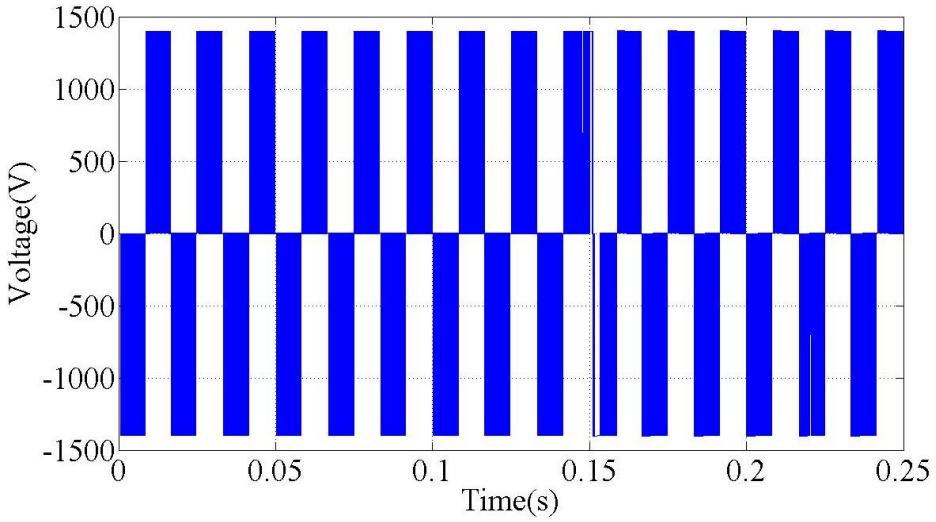

Fig. 2-3. Unipolar PWM voltage switching scheme

2.3 Current Control of a H-Bridge

Section 2.2 presented an overview of the single-phase H-bridge converter operating concepts whose understanding is important in order to implement the current control techniques covered in this section. A typical current controller for a single-phase H-bridge converter is illustrated in Fig. 2-4. According to [1], a proportional-integral (PI) compensator can be used in the algorithm if:

- i_{ref} signal is step type;
- V_S is a DC voltage.

The compensator block from Fig. 2-4 can be expressed as follows:

$$K(s) = k_p + \frac{k_i}{s} \tag{2-3}$$

with (2-3) and the diagram of Fig. 2-4, the closed loop gain of the system can be defined as follows [1]:

$$G = \frac{k_p}{L}\left(\frac{s + \frac{k_i}{k_p}}{s + \frac{R}{L}}\right). \tag{2-4}$$

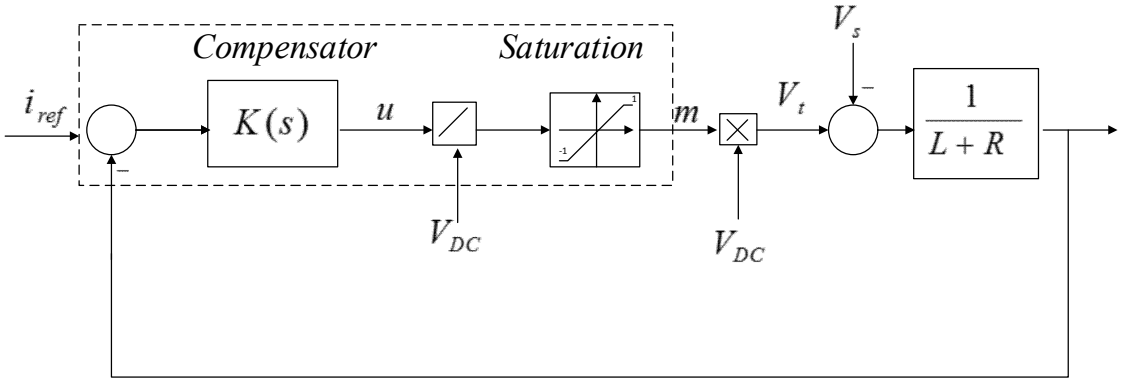

Fig. 2-4. Closed-loop current control diagram

The gains of the PI compensator are defined by [1]:

$$\frac{k_i}{k_p} = \frac{R}{L} \tag{2-5}$$

$$\frac{k_p}{L} = \frac{1}{\tau_i} \tag{2-6}$$

where R and L resistor and inductor interfacing the inverter with the grid, and k_i, k_p, τ_i are the integral, integral gain, proportional gain and the time constant of the system. In most applications the value range for τ_i is between 0.5-5.0 ms [1].

A MATLAB/SIMULINK™ simulation is presented in order to illustrate the concept of a single-phase H-bridge current controller. The parameters for the simulation are shown in Table 2-1 [1]. The MATLAB/SIMULINK™ H-bridge model and control block are illustrated in Fig. 2-5 and 2-6, respectively. The main issue that can be observed on the system response of Fig. 2-7 is that the system experiences an undershoot response due to initial conditions

Table 2-1. Current controller example parameters [1]

Parameter	**Value**
Resistance (mΩ)	**5**
Inductance (μH)	**690**
V_{DC} (V)	**1200**
V_s (V)	**400**
f_{sw} (Hz)	**1620**

This is due to fact that the system starts from a zero-state and the value of V_t is equal to 0 and while V_s is negative. This leads to a negative value of i until it gets regulated to 0 by the controller [1].

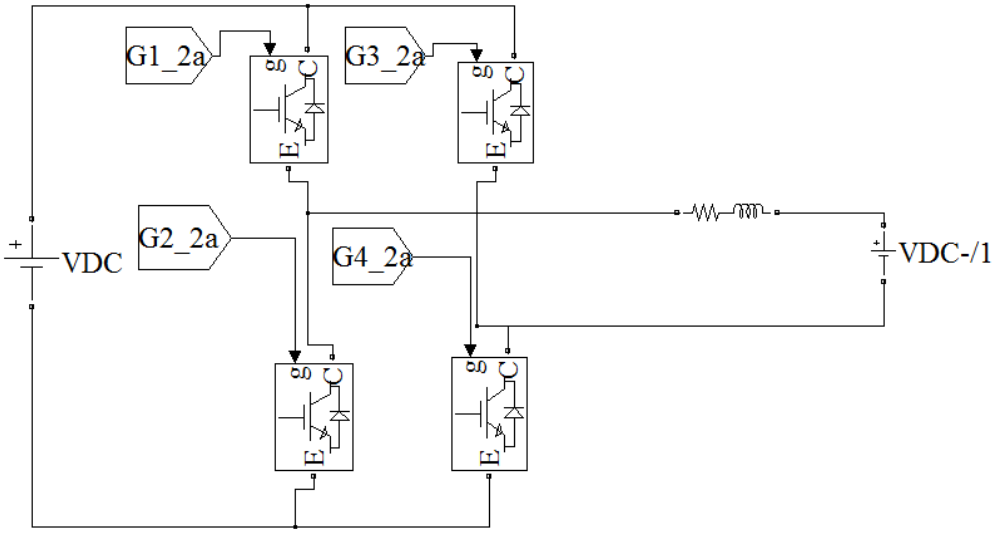

Fig. 2-5. MATLAB/SIMULINK™ H-bridge model.

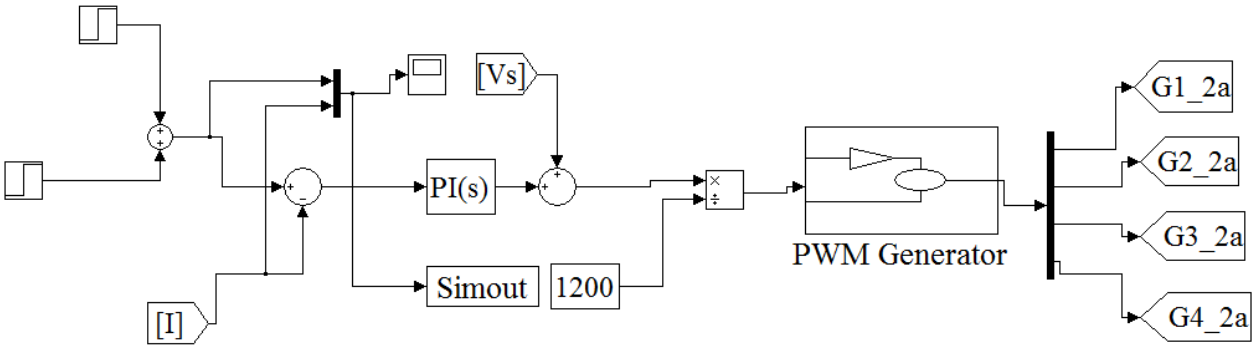

Fig. 2-6. MATLAB/SIMULINK™ control algorithm block diagram.

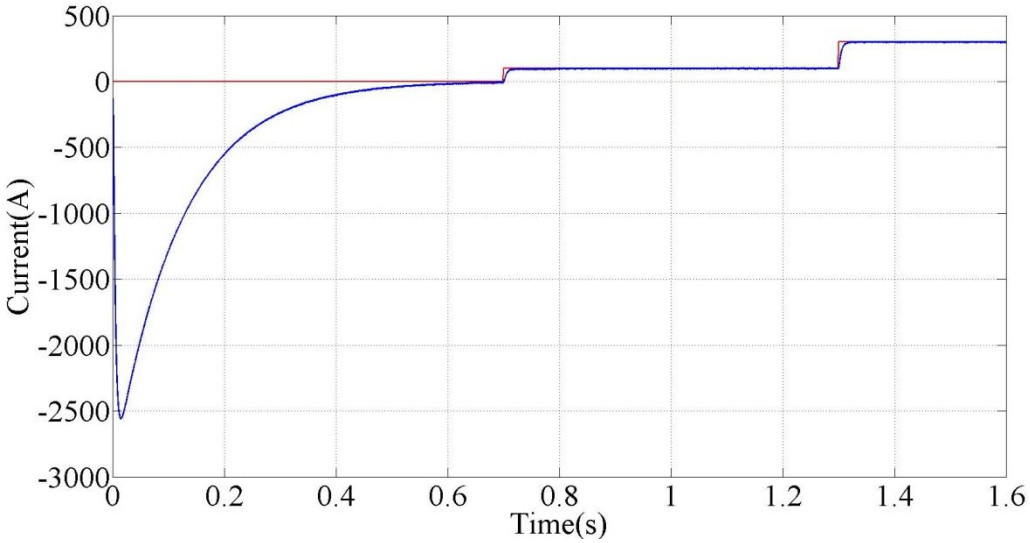

Fig. 2-7. Output current i (blue) and reference current i_{ref} (red) waveforms

The maximum reached value due to the undershot is 2566 A. This condition should be avoided; otherwise, the H-bridge must be designed in such a way that I can withstand the large amount of current generated during the system start up process. The system response settling time is of 0.7 s approximately. When the current goes from 0 A to 100 A at 0.75 s, the system response is over-damped because it does not oscillate to reach the reference signal. The same behavior is observed when the second step is introduced at 1.3 s. The approximate settling time for both cases is of 0.011 s (0.66 cycles) and 0.014 s (0.84 cycles), respectively. The system response can be improved if a feed forward compensation [1] is applied to the control loop as is shown in Fig. 2-8 and the improved response of the system is depicted in Fig. 2-9.

The results depicted on Fig. 2-9 illustrate the improvement of the system response after applying a feed forward compensation technique to the original controller. The undershoot response of the system observed in Fig. 2-7 is mitigated and the settling time is greatly improved as shown in Fig. 2-9. The next section presents the fundamental concepts of reference frame theory that is normally used in three-phase systems.

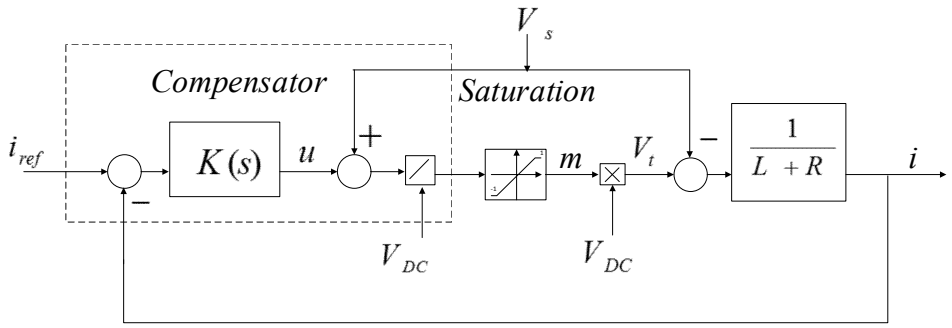

Fig. 2-8. Closed-loop current control diagram with feed forward compensation

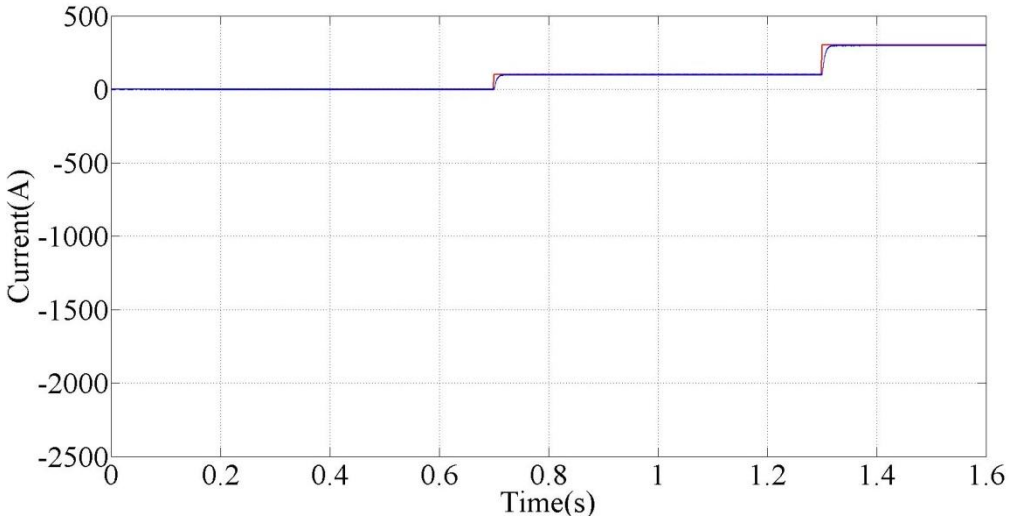

Fig. 2-9. Output current i (blue) and reference current i_{ref} (red) waveforms with feed forward compensation

2.4 Reference Frame Theory

A current controller with a PI compensator can follow a reference with a small or no steady-state error as long as the reference signals are constant or slowly varying [1]; otherwise a very high switching frequency would be required. Because the UCSC system is a solution for three-phase four-wire systems, the reference command in the *abc* frame will not be a constant or

slow varying value and the controller output will have errors in magnitude and phase [1]. This issue can be solved if the *abc* variables are transformed to the synchronous reference frame by applying Park's transformation [3], [4].

The Park's transformation refers stator variables such as currents, flux linkages and voltages of a synchronous machine to a frame reference fixed on its synchronous-rotating rotor so the variation of the inductance values as function of the position of the rotor can be eliminated [4]. This reference frame is the so-called synchronous-rotating reference frame [4].

Even though Park's transformation was envisioned to work in the study of AC machines, it can also be implemented in other constant-parameter power-system components [4]. The Park's transformation equation can be expressed as follows [4]:

$$\left[\mathbf{f}_{\mathrm{qd0s}}\right] = [\mathbf{K}_{\mathrm{s}}][\mathbf{f}_{\mathrm{abcs}}]. \tag{2-7}$$

where and **f** could be current, voltage, flux linkage or electric charge, and $[\mathrm{K_s}]$ is given by:

$$[\mathrm{K_s}] = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2-8}$$

with its inverse $[\mathrm{K_s}]^{-1}$ matrix is given by:

$$[\mathrm{K_s}]^{-1} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{2-9}$$

where $\theta = \omega_s t + \theta_0$ with $\omega_s t$ is the grid angular speed, t time and θ_0 the initial angle [4].

The relationship between the *abc* variables and the $d-q$ axes is illustrated in Fig. 2-10a [4]. Another important transformation of variables used to design current controllers of converter systems is the Clarke's transformation, also known as the $\alpha-\beta-0$ transformation. This transformation in matrix form is given by [5]:

$$[\mathbf{f}_{\alpha\beta 0}] = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2-10}$$

where the variables in the *abc* frame are transformed or referred to the $\alpha-\beta$ stationary axes as illustrated in Fig. 2-10b.

This transformation is derived from the Park's transformation by making $\theta = 0$ in (2-8) (i.e., $\omega_s = 0$). The so-called stationary reference frame was used by Akagi *et al.* [6], [7] to generate the p-q theory as stated in [8] in order to design controllers for active power filters.

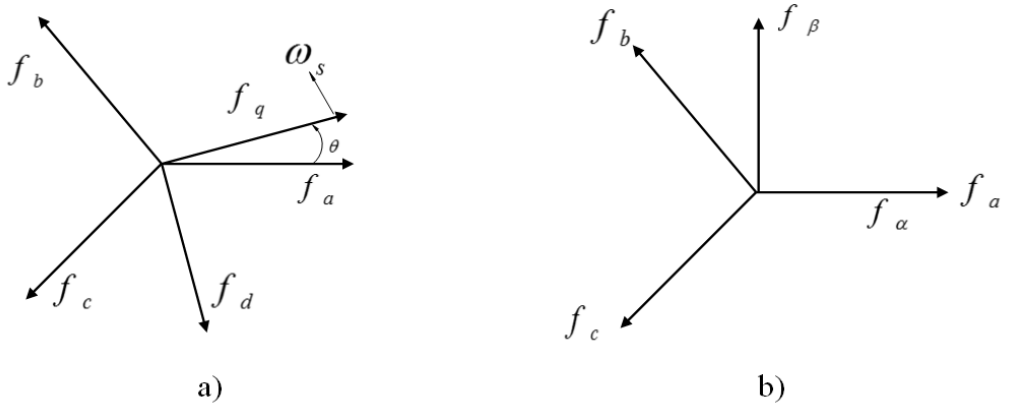

Fig. 2-10. a) Representation of the *abc* and the $d-q$ variables. b) Representation of the *abc* and the $\alpha-\beta$ variables

However, as stated in [9], working on the $d-q$ synchronous-rotating reference frame gives more accurate results. The transformation of variables is an important mathematical technique that will be used to design the control algorithm of the UCSC system that will be presented in the following chapter.

2.5 Conclusions

An overview of power electronic concepts was presented in this chapter in order to provide the necessary background information to design the UCSC system. It was learned that depending on the flow of power, AC to DC side or DC- to AC side, power electronic converters can be classified into rectifiers and inverters, respectively. The type of converters that was chosen for the UCSC topology is the single-phase H-bridge VSC, which can operate as a rectifier and as an inverter. The reason for choosing the VSC is that it provides the capability of having independent control of the phase currents.

The control of an H-bridge was illustrated with a MATLAB/SIMULINK^{TM} simulation and it was concluded that PI controllers work well with constant or slow variable signals. The concepts of the reference frame theory, Park's and Clarke's transformation was presented in order to address the control H-bridges in AC systems. Chapter 3 will focus on presenting the development of the UCSC system topology and control algorithm.

2.6 References

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CHAPTER 3

UNBALANCED CURRENT STATIC COMPENSATOR: COMPONENTS AND CONTROL ALGORITHM

3.1 Introduction

The main objective of the UCSC system is to control the flow of currents in a three-phase four-wire distribution feeder at a selected point of common coupling (PCC) in such a way that the currents injected from the power substation are balanced in magnitude and in phase with their associated voltages. This objective is accomplished by having three single-phase H-Bridge converters that will control the flow of current for each phase independently.

The main components of the case study are described in the first part of the chapter and the control is given in the second part of the chapter. Appendix A.1 illustrates the MATLAB/SIMULINK™ models used for the single-phase $\alpha - \beta/d - q$ transformation.

3.2 UCSC System Description

The case study of distribution system unbalanced loading was presented on section 1.3. As previously mentioned, the UCSC system is connected to a 34.5 kV three-phase four-wire distribution system. For ease of reference, Fig. 1-11 is here repeated as Fig. 3-1. The main components in Fig. 3-1 are the following:

a) Power substation **-** The rated values are:

- Line-to-line rms voltage = 34.5 kV;
- Rated power = 6 MVA;
- Frequency = 60 Hz.

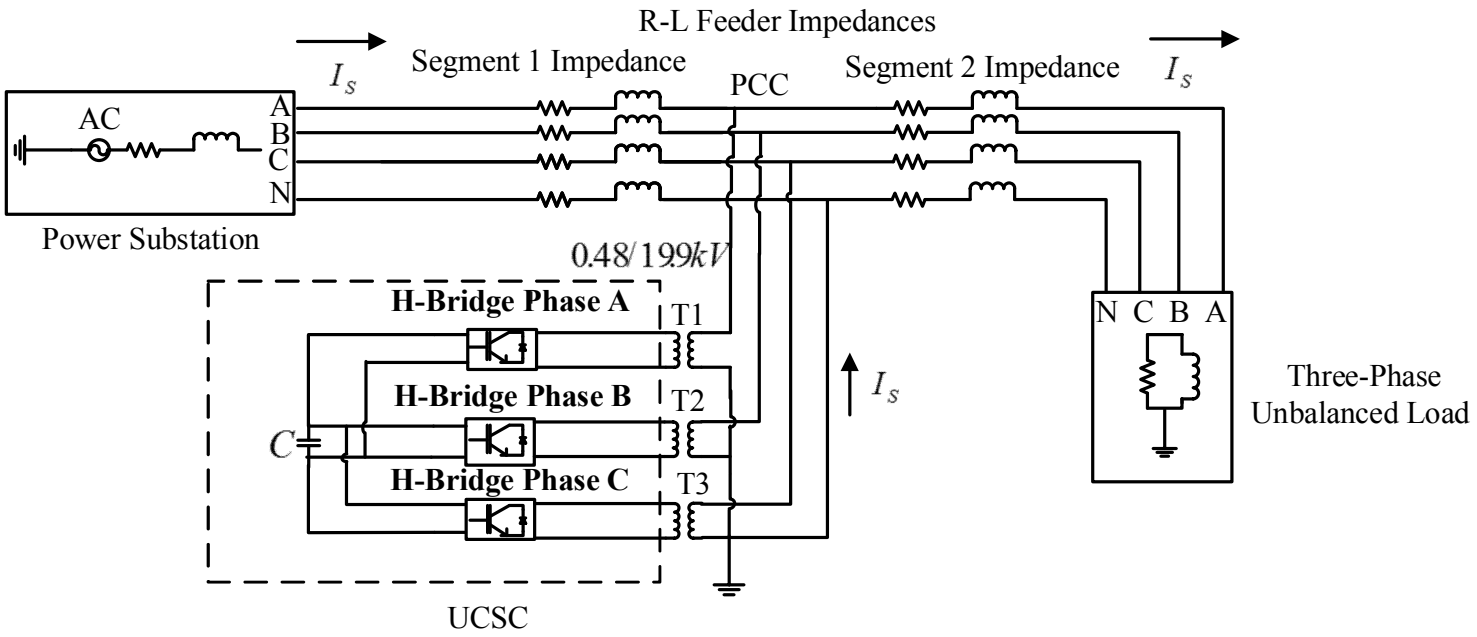

Fig. 3-1.One-line diagram for the UCSC case study

b) Feeder impedances **-** The impedances for segments 1 and 2 are calculated based on the characteristics of a 266,800 AWG aluminum cable from Table A.5 of [1]. These characteristics are the following:

- $r_a = 0.385\ \Omega/\text{mile}$;
- $x_a = 0.465\ \Omega/\text{mile}$;
- segment 1 distance = 0.621371 miles (1 km);
- segment 2 distance = 31.1 miles (50 km);
- pole configuration as per Fig. 3-2.

The positive-sequence impedance of segment 1 is calculated as follows [1]:

$$dp = (Dab \times Dbc \times Dca)^{1/3} \tag{3-1}$$

$$dp = \sqrt[3]{(46inches \times 86inches \times 132inches)} \times \frac{0.0833\ \text{ft}}{1\ \text{inch}} \tag{3-2}$$

$$dp = 6.71\ \text{ft} \tag{3-3}$$

$$X_{dp} = 0.05292\ log_{10}dp\ \ \Omega/1000\ \text{ft} \tag{3-4}$$

$$X_{dp} = 0.044\ \Omega/\ 1000\text{ft} \tag{3-5}$$

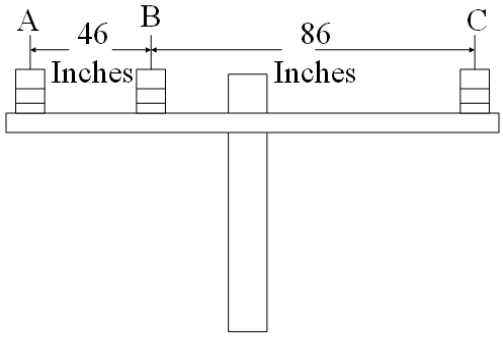

Fig. 3-2. Pole configuration for segments 1 and 2 of the considered three-phase system [2]

$$Z_{segment1} = r_{ap} + j\left(x_a + x_{dp}\right)\Omega/1000\ ft \tag{3-6}$$

$$Z_{segment1} = 0.24 + j0.14\ \Omega. \tag{3-7}$$

The same procedure is applied for the calculation of segment 2. The result is the following:

$$Z_{segment2} = 11.96 + j7.19\ \Omega. \tag{3-8}$$

c) System loads - The system loads are aggregated and represented by of parallel resistors and inductors whose values are given in chapter 4.

d) UCSC Coupling transformers - The step-up distribution transformers have voltage ratings of $0.48 - 19.9\ kV$ and the power capacity for the case study will be based on three single-phase 1 MVA transformers. The ratings were selected based on the current profile of Fig. 1-3 from section 1.3. Information about transformers that can be used for the UCSC system can be obtained from [3] and [4].

e) UCSC system - The main components which are depicted on Fig. 3-3 are:

- energy storage capacitor in the DC link;
- three single-phase H-Bridge converters;
- three LCL output filters.

DC-Link Energy-Storage Capacitor

The capacitance is calculated using the following equation from [4]:

$$C_{DC} = \frac{I_2}{4\sqrt{2}(\Delta V_{dc}\%)V_{DC}f_{sw}} \tag{3-9}$$

where

- $\Delta V_{DC}\%$ is the desired percentage DC-link voltage ripple;
- V_{DC} is the rated DC-link voltage;
- I_2 is the peak AC-side current;
- f_{sw} is the switching frequency.

The parameters to calculate the energy storage capacitor are illustrated in Table 3-1 and the criteria to select the DC-link voltage level and the switching frequency are the following:

- to avoid PWM over-modulation the DC-link voltage must satisfy $V_{DC} \geq 2V_t$; where V_t is the terminal AC voltage depicted in Fig. 3-3. Over-modulation can increase the harmonics content in the output voltage [5], [6];
- the switching frequency f_{sw} should be less than 6 kHz to avoid high switching losses, or above 20 kHz to be outside the audible range [6];
- the modulation ratio $mf = \left(\frac{f_{sw}}{f_1}\right)$ should be an even integer if possible [6].

Single-Phase H-Bridge Converters

The topology for each of the single-phase H-Bridge converters is illustrated in Fig. 3-4. Based on the specifications from Table 3-1, the semiconductor switching devices must have a maximum current capability of 2083 A or more for continuous current, with a DC voltage rating of 1400 V or more. Another important factor that must be taken into consideration when selecting the switching devices is the inrush current. According to [8], the inrush current in a

distribution system is not easy to determine due to the diversity of the loads but an estimation of 4 times the full load current (I_g) is a good approximation.

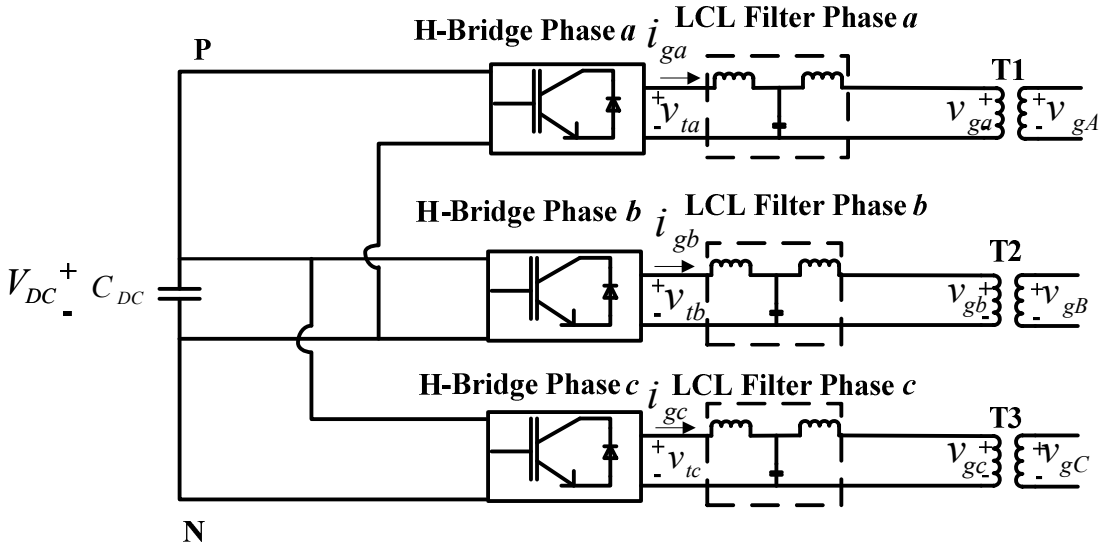

Fig. 3-3. Unbalanced current static compensator system

Table 3-1. UCSC system parameters

Parameter	Value
DC-link voltage level V_{DC} (V)	**1400**
DC-link voltage ripple ΔV_{DC}%	**1**
Switching frequency f_{sw} (Hz)	**5400**
UCSC voltage V_t (V rms)	**480**
Peak grid side current I_2 (A)	**2945**
Rated Current Magnitude I_g (A rms)	**2083**
Energy storage capacitor C_{DC} (mF)	**4.90**

The IGBT devices (CM2400HC-34N) from MITSUBISHI ELECTRIC® [9] are one of the options currently available to build the H-Bridge converters. The main parameters of the IGBT switches are illustrated in Table 3-2 [8]. A switch position will be realized by connecting 4 modules in parallel.

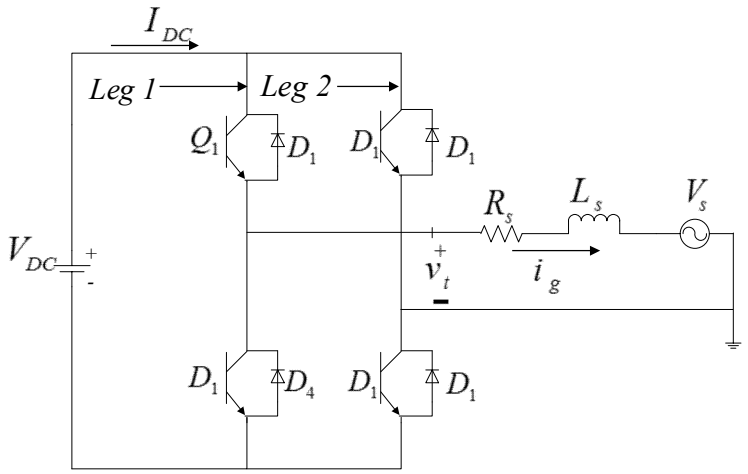

Fig. 3-4. UCSC single-phase H-Bridge converter topology schematic

Table 3-2. IGBT's parameters

Parameter	Value
Collector Emitter Voltage V_{ce} (V)	**1700**
Collector Current I_c (A)	**2400**
Peak Collector Current I_c (pulse) (A)	**4800**

LCL Output Filters

LCL filters were designed to improve the total harmonic distortion (THD) at the outputs of the H-Bridge converters. A schematic of one LCL filter is depicted in Fig. 3-5 where L_{inv}, L_g, C_f represent the inverter-side inductance, grid-side inductance and the filter's capacitance, respectively. The considerations for the design of the filter are [10], [11]:

- The value for the capacitor is restricted by a decrease of the power factor of no more than 5%. In this case a 2% value was chosen as suggested in [11]. The following equation gives the value of C_f.

$$C_f = 2\% \times \frac{S}{3 \times 2\pi f_1 V_{lg}^2} \tag{3-10}$$

where

  - S is the VSC rated power in kVA
  - f_1 is the grid frequency
  - V_{lg} is the line to ground voltage in kV.

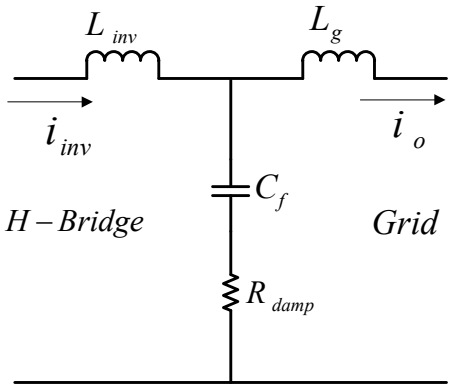

Fig. 3-5. LCL filter schematic

- The equation for selecting the value of the inverter-side inductance is:

$$\Delta i = \frac{V_{DC}}{8 L_{inv} f_{sw}} \leq 20\% I_n \tag{3-11}$$

where

  - Δi is the ripple current;
  - I_n is the rated current;
  - f_{sw} is the switching frequency.

- The grid-side inductance is related to the inverter-side inductance as follows [10]:

$$L_g = r L_{inv} \tag{3-12}$$

where the constant r is calculated using the following:

$$\frac{i_o(h_s)}{i_{inv}(h_s)} = \frac{1}{\left|1 + r\left(1 - L_{inv} C_f (2\pi f_{sw})^2\right) \times 2\%\right|} \tag{3-13}$$

where $i_o(h_s)$ and $i_{inv}(h_s)$ are the output and inverter-ripple currents, respectively.

- The resonant frequency should comply with the following condition:

$$10 f_1 \leq f_{res} \leq \frac{1}{2} f_{sw} \tag{3-14}$$

- The value of the damping resistor ($\mathrm{R_{damp}}$) in series with the filter capacitor, can be calculated as follows [10]:

$$R_{damp} = \frac{1}{3 \times \omega_{res} \times C_f} \tag{3-15}$$

$$\omega_{res} = \sqrt{\frac{L_{inv} + L_g}{L_{inv} \times L_g \times C_f}}. \tag{3-16}$$

The calculated parameters values are given in Table 3-3. The table includes the values for the inductors, capacitors and resistors for each phase LCL filter.

Table 3-3. LCL filter parameters

Parameter	Value
L_{inv} (µH)	73.33
L_g (µH)	40.65
C_f (mF)	0.144 (12.5 kVAR)
R_{damp} (Ω)	0.15

3.3 UCSC Control Algorithm

An overview of current controllers for single-phase H-Bridge converters, the reference frame theory, Park's and Clarke's transformation was presented in section 2.3 [12]-[15]. All of these concepts are used in the development of the UCSC control algorithm shown in Fig. 3-6.

The algorithm is divided into three main stages:

a) phase synchronization and reference current generator stage;

b) current and DC-link voltage controller stage;

c) PWM stage.

a) Phase Synchronization and Reference Current Generator Stage

This stage has two objectives:

- to obtain the phase-angle from each phase voltage at the PCC.
- to generate the reference current inputs for each of the three single-phase H-Bridge converters current controllers;

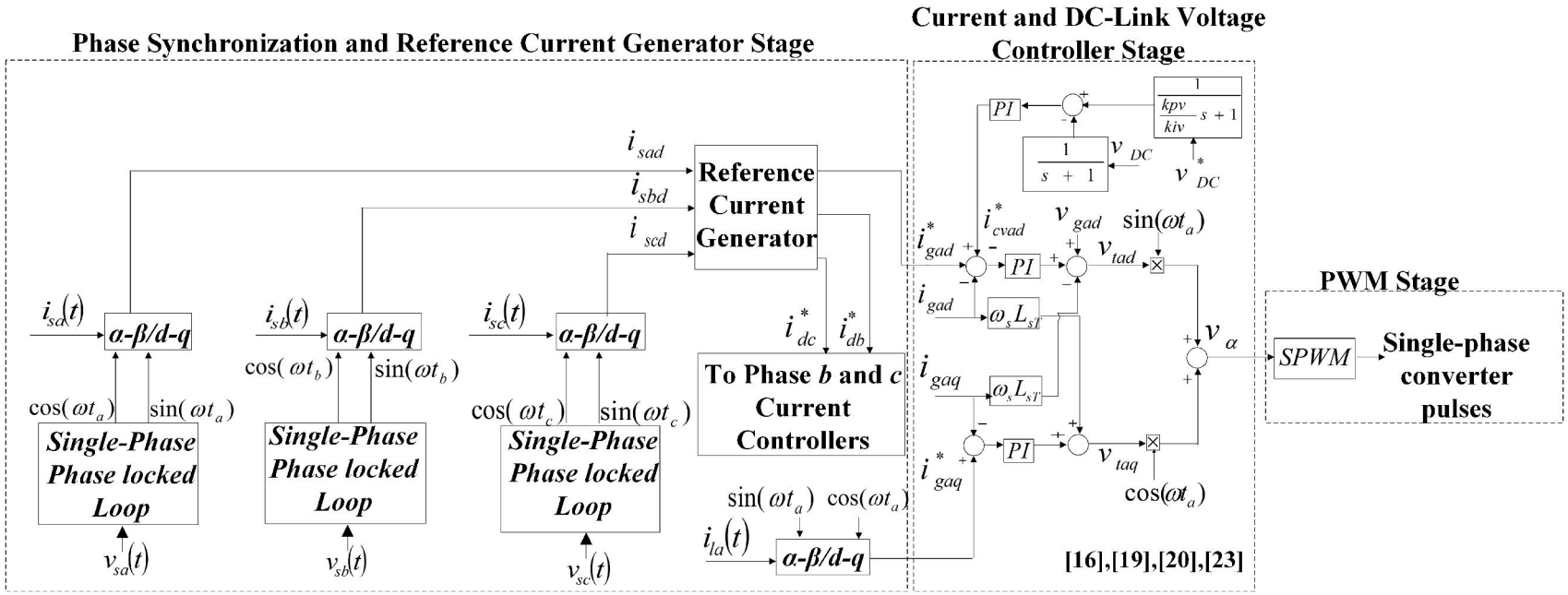

Fig. 3-6. Multi-stage UCSC control algorithm block diagram

Phase Synchronization

The phase synchronization process extracts the phase-angle from each phase voltage at the PCC through the single-phase phase-locked loop blocks that are depicted in Fig. 3-6. The phase-angle is used as the input signal for the $\alpha - \beta \ / \ d - q$ and $d - q \ / \ \alpha - \beta$ transformation blocks. By doing this, the output voltage generated by each single-phase H-Bridge converter of the UCSC system is in-phase with the corresponding grid voltage at the PCC.

A typical single-phase phase-locked loop algorithm has three components and the algorithm used in the UCSC system is depicted in Fig. 3-7 [17], [18]. The phase-locked loop components are the following [17], [18]:

- a phase detector that combines the input signal with the internal oscillator signal that serves as the input for the variable frequency mean value block. The variable frequency mean value block generates the DC component of the mixed signal that is used as the input for the compensator block;

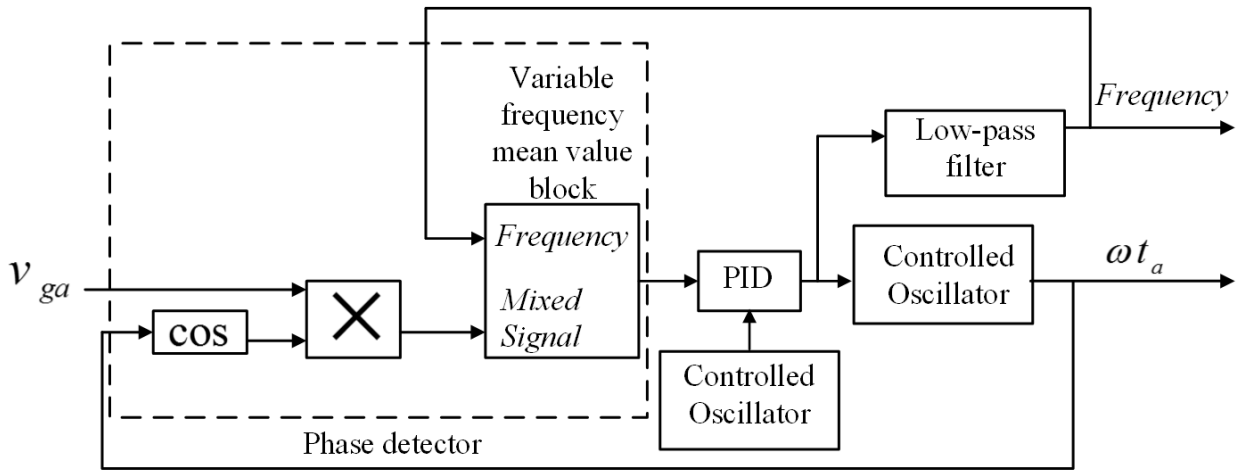

Fig. 3-7. Phase-locked control algorithm block [18]

- a compensator that can be a proportional-integral-derivative controller that generates the necessary inputs for the controlled oscillator and the low pass filter to keep the error signal or phase difference to 0;
- a controlled oscillator that generates the feedback signal for the phase detector.

Reference Current Generation

As shown in Fig. 3-6, before the current inputs are fed into the reference current generator block, the phase currents must be transformed from the *abc* reference frame to the $d-q$ reference frame.

As stated in [19], the transformation from the *abc* frame to the $d-q$ frame is typical of three-phase systems. Because the UCSC control algorithm has been designed with three independent current controllers, one for each phase, the guidelines presented in [19] to perform the reference frame transformation from *abc* axes to the $d-q$ axes must be followed.

The "change-of-variable" transformation process starts by moving from the $\alpha-\beta$ axes to the $d-q$ axes for each phase. For phase a, the H-Bridge converter output current, i_{ga}, from Fig. 3-8, is the α component and i_{ga} delayed by a quarter cycle (i.e., 90°) is the β component. The same concept can be applied to phases *b* and *c* [20], [21].

When the two orthogonal components have been defined, the $\alpha-\beta/d-q$ transformation equations can be performed by applying the following equations [14]:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) & 0 \\ \cos(\theta) & \sin(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix} \tag{3-17}$$

Once the phase currents are transformed from the $\alpha - \beta$ axes to the $d - q$ axes, the I_d currents for each phase enter the reference current generator block illustrated in Fig. 3-9 where the subscript "*s*" stands for source, "*a*", "*b*" and "*c*" for the grid phases and *d* for the direct axis.

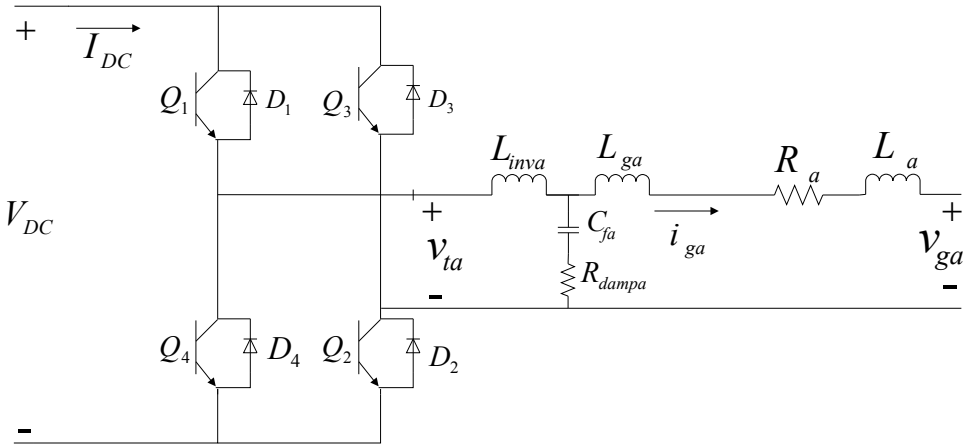

Fig. 3-8. Phase *a* H-Bridge converter

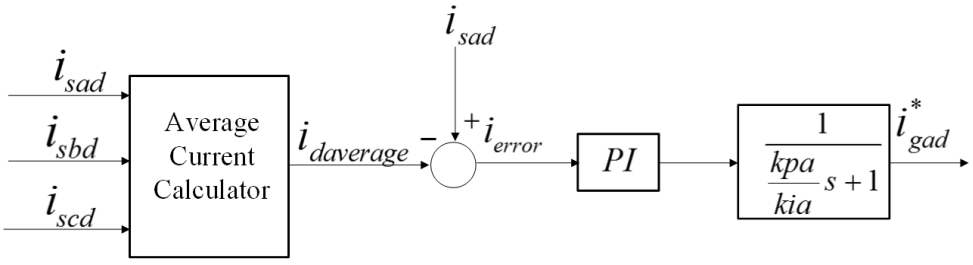

Fig. 3-9. Phase *a* reference current generator block

The reference current generator block calculates the average of the three currents in the *d*-axis; and the resulting average current, $i_{daverage}$, is subtracted from each phase current creating an error signal that is used as the input for a PI controller that generates the reference current for the current controller of each phase as depicted in Fig. 3-10.

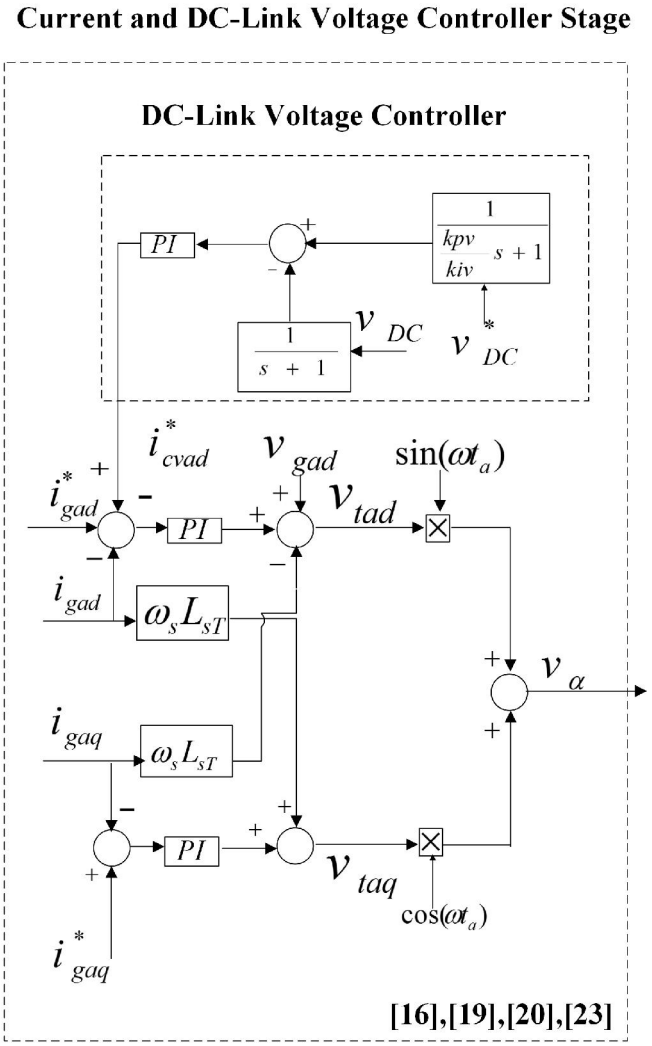

Fig. 3-10. Current controller stage for phase *a*

The PI controller gains can be calculated by following the procedure presented in section 2-3 based on the work of [5], and for ease of reference, the equations are presented here [5]:

$$\frac{k_{ia}}{k_{pa}} = \frac{R_a}{L_a^*} \tag{3-18}$$

$$\frac{k_{pa}}{L_a^*} = \frac{1}{t_i} \tag{3-19}$$

where:

- k_{ia} is the integral gain;
- k_{pa} is the proportional gain;
- R_a is the grid resistance for phases *a*, *b* or *c*;
- L_a^* is equal to the addition of L_{inva}, L_{ga} and L_{sa};
- τ_i is the time constant.

For the *q*-axis reference current, the load current of each phase are measured and then transformed into the $d-q$ axes. The resulting signal is sent to the current and DC-link voltage controller stage. By doing this, the UCSC system will provide all the demanded *q*-axis current by the load. This leads to a unity power factor correction at the PCC since the *q*-axis current is the current component producing reactive power [20].

b) Current and DC-link Voltage Controller Stage

The control loops of the current and DC-link voltage controller stage of Fig. 3-10 are [23], [24]:

- the current control loop or inner loop;
- the DC-link voltage control loop or outer loop.

The bandwidth of the current controller must be at least 10 times faster than the bandwidth of the voltage controller. The current controller bandwidth should also be at least 5 times smaller than the switching frequency in rad/s [24]. The selected values for the current controller and the voltage controller were 400 Hz and 12 Hz, respectively.

Current Controller: Active and Reactive Powers

The main objective of the current controller is to have independent control of the *d*- and *q*- axis currents depicted in Fig. 3-11. In order to achieve the main objective, the current controller must first fulfill the enabling objective of decoupling the voltages in the $d-q$ axes in order to achieve independent control of the active and reactive powers that can be derived as follows [20]:

$$v_{ga} = \hat{V}_{ga}\cos(\omega_s t) \tag{3-20}$$

$$i_{ga} = \hat{I}_{ga}\cos(\omega_s t - \varphi) = \hat{I}_{gad}\cos(\omega_s t) - j\hat{I}_{gaq}\sin(\omega_s t) \tag{3-21}$$

where

- v_{ga} and i_{ga} are the phase *a* grid voltage and the phase *a* H-Bridge converter output current respectively; $\hat{V}_{ga}$, $\hat{I}_{ga}$ represent the peak values of $v_{ga}$and i_{ga}, respectively;
- $\hat{I}_{gad}$ and $\hat{I}_{gaq}$ represent the maximum values for the phase *a* H-Bridge converter output current along the $d-q$ axes, respectively:

$$\hat{I}_{gad} = \hat{I}_{ga}\cos(-\phi) \tag{3-22}$$

$$\hat{I}_{gad} = \hat{I}_{ga}\sin(-\phi). \tag{3-23}$$

Assuming that the voltage on phase *a* is along the *d* axis, equations (3-20)-(3-23) can be used to define the active and reactive powers for phase *a* in the $d-q$ axes [20]:

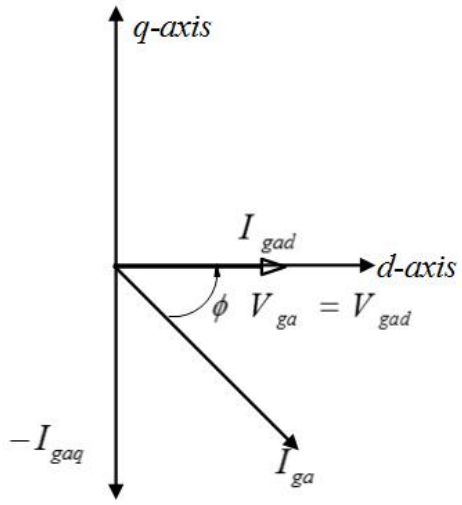

Fig. 3-11. Phase *a* H-bridge converter output current and voltage phasor diagram

$$P = \frac{\hat{V}_{ga}}{\sqrt{2}}\frac{\hat{I}_{ga}}{\sqrt{2}}\cos(\phi) = \frac{1}{2}\hat{V}_{gad}\hat{I}_{gad} \tag{3-24}$$

$$Q = -\frac{\hat{V}_{ga}}{\sqrt{2}}\frac{\hat{I}_{ga}}{\sqrt{2}}\sin(\phi) = -\frac{1}{2}\hat{V}_{gad}\hat{I}_{gaq} \tag{3-25}$$

Equations (3-24) and (3-25) illustrate that by having an independent control of i_{gad} and i_{gaq}, the UCSC is able to control the power flow between the single-phase H-Bridge converters and the grid.

The reference signals that are used to control the active and reactive powers are the following:

- i^*_{gad} is the *d*-axis reference current generated in the phase synchronization and reference current generator stage;
- i^*_{cvad} is the *d*-axis reference current generated by the DC-link voltage controller [16];
- i^*_{gaq} is the reference current for the *q*-axis.

Once the reference signals enter the current and voltage controller stage, the algorithm performs the calculations to generate the H-Bridge converter output voltages v_{tad} and v_{taq}. The

voltages signals are transformed into the $\alpha - \beta$ axes generating the v_α signal that is used for the control of the PWM stage.

The feedback signals used in the current and DC-link voltage controller stage are:

- i_{gad} is the H-Bridge phase *a* converter output current in the *d*-axis;
- i_{gaq} is the H-Bridge phase *a* converter output current in the *q*-axis.
- $i_{la}(t)$ is the load current for phase *a*.

Current Controller: Mathematical Model

The derivation of the current controller mathematical model consists of performing a Kirchhoff's voltage law (KVL) analysis the equivalent H-Bridge single-phase converter circuit of Fig. 3-12.

According to [21], the LCL filter's capacitor branch can be neglected in the control analysis. The KVL equations in the $\alpha - \beta$ axes are the following [20]:

$$\begin{bmatrix} v_{ta\alpha} \\ v_{ta\beta} \end{bmatrix} = R_a \begin{bmatrix} i_{ga\alpha} \\ i_{ga\beta} \end{bmatrix} + L_a^* \frac{d}{dt} \begin{bmatrix} i_{ga\alpha} \\ i_{ga\beta} \end{bmatrix} + \begin{bmatrix} v_{ga\alpha} \\ v_{ga\beta} \end{bmatrix} \tag{3-26}$$

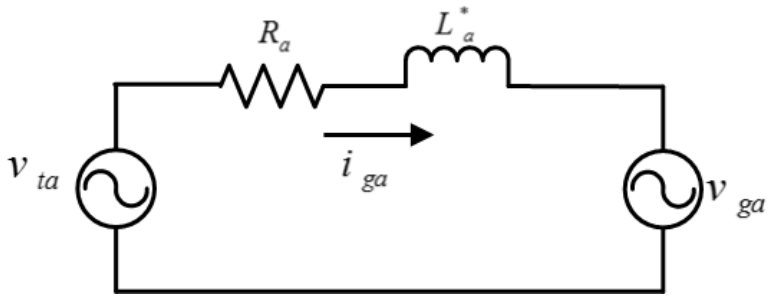

Fig. 3-12. H-Bridge converter phase *a* equivalent circuit

where

$v_{ta\alpha}$, $v_{ta\beta}$, $v_{ga\alpha}$, $v_{ga\beta}$, $i_{ga\alpha}$ and $i_{ga\beta}$ are the H-Bridge converter output voltages, the phase *a* grid voltages and the H-Bridge converter currents in the $\alpha - \beta$ axes, respectively.

The same equations can be represented in the $d - q$ axes as follows [20]:

$$\begin{bmatrix} v_{tad} \\ v_{taq} \end{bmatrix} = R_a \begin{bmatrix} i_{gad} \\ i_{gaq} \end{bmatrix} + L_a^* \frac{d}{dt} \begin{bmatrix} i_{gad} \\ i_{gaq} \end{bmatrix} + \begin{bmatrix} 0 & -\omega_s L_a^* \\ \omega_s L_a^* & 0 \end{bmatrix} \begin{bmatrix} i_{gad} \\ i_{gaq} \end{bmatrix} + \begin{bmatrix} v_{gad} \\ v_{gaq} \end{bmatrix} \tag{3-26}$$

where

v_{tad}, v_{taq} , v_{gad}, v_{gaq}, i_{gaq} and i_{gaq} are the H-Bridge converter output voltages, the phase *a* grid voltages and the H-Bridge converter currents in the $d - q$ axes, respectively.

The cross-coupling between the voltages in the $d - q$ axes can be addressed by making the input transformation suggested in [20],[22] and rewriting equation (3-26) as follows:

$$v_{tad} = v'_d - \omega_s L_a^* i_{gaq} + v_{gad} \tag{3-27}$$

$$v_{taq} = v'_q + \omega_s L_a^* i_{gad} + v_{gaq} \tag{3-28}$$

where

$$v'_d = R_a i_{gad} + L_a^* \frac{di_{gad}}{dt} \tag{3-29}$$

$$v'_q = R_a i_{gaq} + L_a^* \frac{di_{gaq}}{dt} \tag{3-30}$$

Once the input transformation is performed the voltages v_{tad} and v_{taq} are no longer cross-coupled and v'_d and v'_q can be controlled through PI controllers [20]:

$$v'_d = K_{p1}\left({i_{gad}}^* - i_{gad}\right) + K_{i1} \int \left({i_{gad}}^* - i_{gad}\right) dt \tag{3-31}$$

$$v'_q = K_{p2}\left({i_{gaq}}^* - i_{gaq}\right) + K_{i2} \int \left({i_{gaq}}^* - i_{gaq}\right) dt \tag{3-32}$$

where ${i_{gaq}}^*$ and ${i_{gad}}^*$ are the reference values for the *q*- and *d*- axis currents.

Voltage controller

The UCSC system has been designed to have a capacitor as the energy storage medium instead of battery energy storage in order to control the real and reactive power flows of the UCSC system. This is possible because the UCSC system takes current from the system and re-distributes it in such a way that the currents seen by the power substation are balanced and at unity power factor.

However, the system has losses so the voltage controller from Fig. 3-10 was implemented in order to maintain a constant DC-link voltage [16], [23]. The main concept behind the controller is to create a small amount of active power exchange with the grid by producing a reference current for the *d*-axis which has a direct influence over the active power exchange as depicted by the equation (3-24).

In order to improve the controller response, the error between the voltage signal v_{DC} and the reference signal v_{DC}^{*} are processed by a pre-filter [23] and a low-pass filter, respectively. After that, an error signal is generated as the input for a PI controller that must have a slower bandwidth than the PI controllers from the inner current control loop in order for the current controller to track the reference without errors [24]. The PI compensator gains of the voltage controller can be obtained based on the work of [23] where the transfer function of the voltage controller can be derived as follows:

$$C_{DC}\frac{dv_{DC}}{dt} = k_{vp}(v_{DC}^{*} - v_{DC}) + k_{vi}\int(v_{DC}^{*} - v_{DC})dt. \tag{3-33}$$

Working in the Laplace domain yields:

$$sC_{DC}v_{DC} = k_{vp}\,v_{DC}^{*} - k_{vp}v_{DC} + \frac{k_{vi}}{s}v_{DC} - \frac{k_{vi}}{s}v_{DC}^{*} \tag{3-34}$$

$$v_{DC}\left(C_{DC}s^{2} + k_{vp}s + k_{vi}\right) = v_{DC}^{*}(k_{vp}s + k_{vi}) \tag{3-35}$$

$$G_v(s) = \frac{v_{DC}}{v_{DC}^*} = \frac{k_{vp}}{C_{DC}} \frac{(s+k_{vi}/k_{vp})}{\left(s^2+\frac{k_{vp}}{C_{DC}}s+\frac{k_{vi}}{C_{DC}}\right)} \quad (3\text{-}36)$$

where

- C_{DC} represents the capacitance of the DC energy-storage capacitor;
- v_{DC} represents the voltage at the DC link;
- v_{DC}^* represents the reference voltage for the DC link;
- k_{vp} represents the proportional gain for the voltage PI controller;
- k_{vi} represents the integral gain of the voltage PI controller.

Finally, the equations determining the PI controller gains are the following [22]:

$$kvp = 2\xi\omega_{vc}C_{DC} \quad (3\text{-}37)$$

$$kvi = {\omega_{vc}}^2 C_{DC} \quad (3\text{-}38)$$

where

- ξ represents the damping factor with a value of $\frac{\sqrt{2}}{2}$ in order to make the controller bandwidth equal to the natural frequency [23]; and ω_{vc} represents the natural frequency of the controller expressed as $\omega_{vc} = 2\pi f_{sv}$ with $f_{sv} = 1/\tau_v$, and τ_v the time constant of the voltage controller expressed in seconds.The gain values for each controller are depicted in Table 3-4.

Table 3-4. Controller parameters for case B

Current Controller		**Reference Current Generator**		**Voltage Controller**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
Proportional gain K_{pi}	**0.53**	**Proportional gain K_p**	**2.14**	**Proportional gain K_{vp}**	**0.64**
Integral gain K_{ii}	**15**	**Integral gain K_i**	**60**	**Integral gain K_{vi}**	**34**

c) PWM Stage

The function of the PWM stage is to generate the switching signals for the IGBT devices. The switching signals are generated by comparing the voltage signal calculated in the current and DC-link voltage controller stage with a triangular waveform. The triangular waveform frequency, f_{sw}, has a value of 5400 Hz. This value was chosen in accordance to the guidelines for single-phase converters with the unipolar PWM switching scheme presented in section 2-3.

The control algorithm used in the PWM stage is the one provided by the MATLAB/SIMULINK™ software. The block diagram representing this algorithm is illustrated in Fig. 3-13.

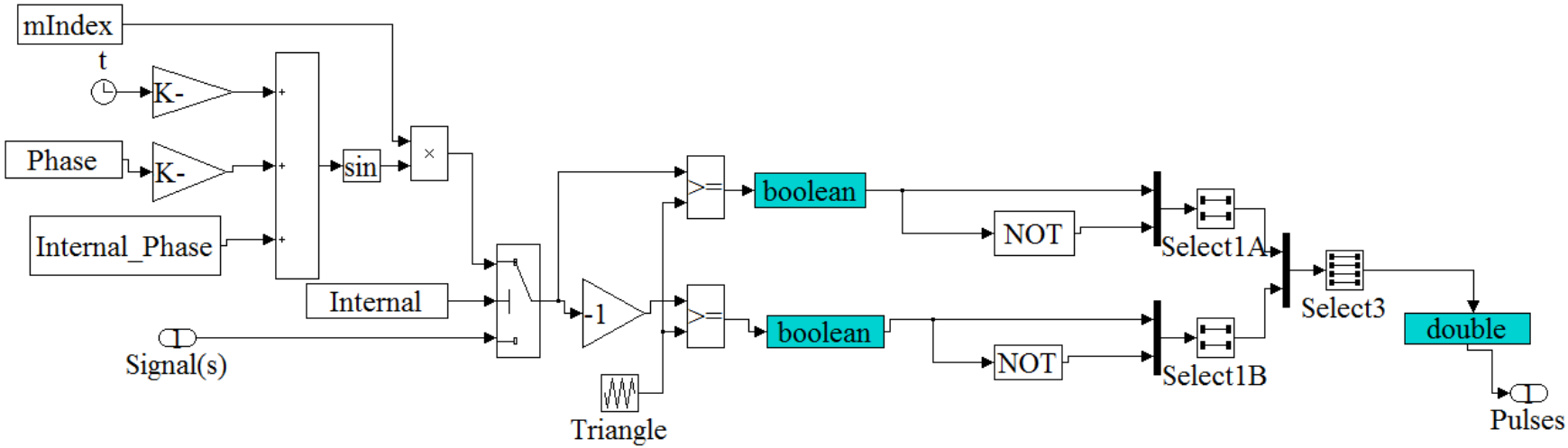

Fig. 3-13. PWM control algorithm [25]

3.4 Conclusions

The development of the UCSC system topology and control algorithm was presented. The UCSC system consists of three single-phase H-bridge converters with an energy-storage capacitor in the DC link. The converters are interfaced with the distribution system through three single-phase step-up transformers.

The algorithm of each converter consists of three different stages:

a) phase synchronization and reference current generator stage;

b) current and DC-link voltage controller stage;

c) PWM stage.

The controllers work in the $d-q$ frame of reference that was presented in chapter 2. The cross-coupling issue between the voltages in the $d-q$ axes found in the mathematical model of the current controller stage was solved. This was necessary in order to be able to have independent control of the $d-q$ axes currents. A voltage controller was added in the current controller stage in order to have a constant DC-link voltage.

The functionality of the topology and controller design will be evaluated and validated through MATLAB/SIMULINK™ simulations in chapter 4.

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APPENDIX A.1

UCSC CASE STUDY: MATLAB/SIMULINK™ MODELS

On this section the following MATLAB/SIMULINK™ models will be presented:

- phase *a* H-bridge output current $\alpha - \beta$ to $d - q$ transformation
- phase *a* *d*-axis reference current generator
- Phase *a* source current $\alpha - \beta$ to $d - q$ transformation
- phase *a* load current $\alpha - \beta$ to $d - q$ transformation

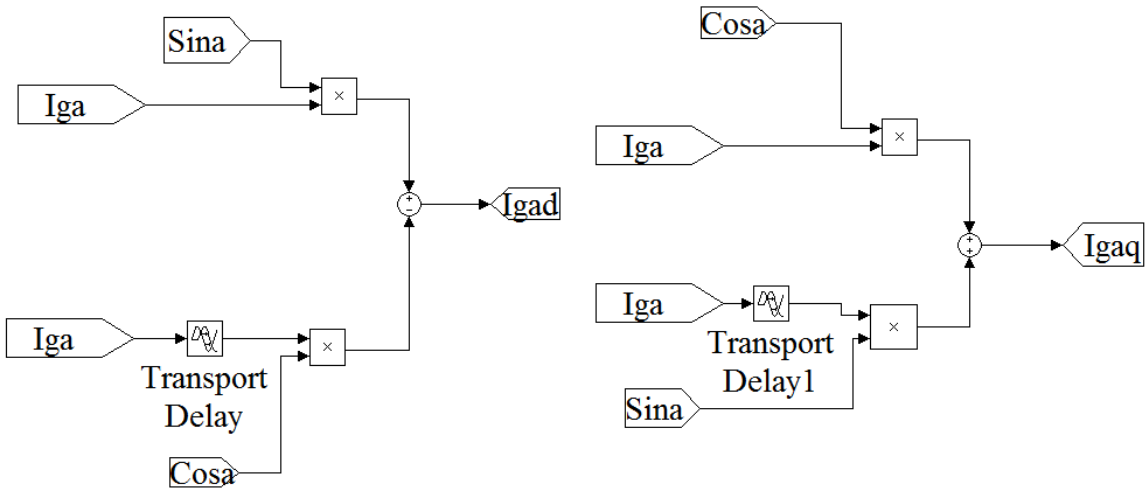

Fig. A-1. Phase *a* H-bridge output current $\alpha - \beta$ to $d - q$ transformation

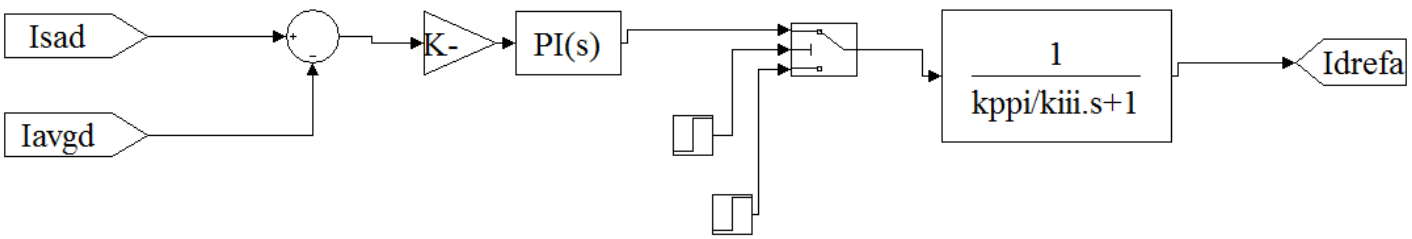

Fig. A-2. Phase *a* *d*-axis reference current generator

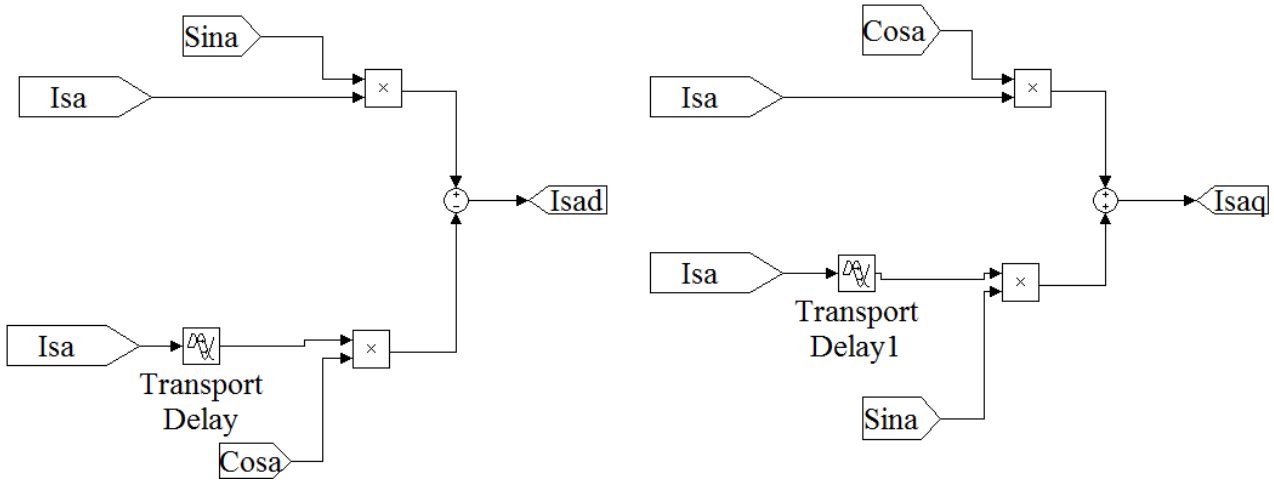

Fig. A-3. Phase *a* source current $\alpha - \beta$ to $d - q$ transformation

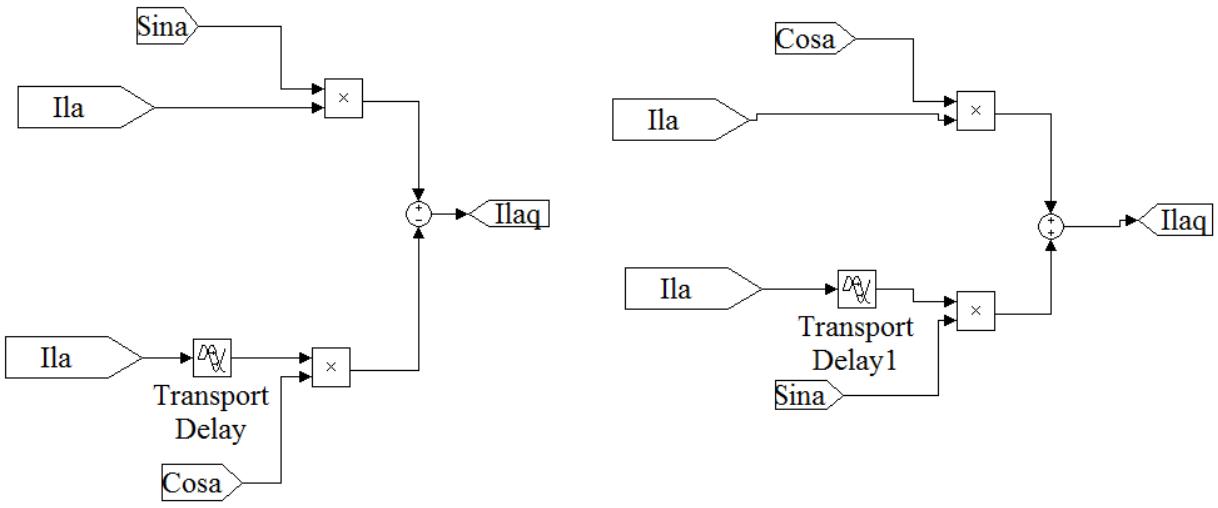

Fig. A-4. Phase a load current $\alpha - \beta$ to $d - q$ transformation

CHAPTER 4

SIMULATION RESULTS AND ANALYSIS OF THE UCSC CASE STUDY

4.1 Introduction

The main objective of this chapter is to analyze the simulation results of the UCSC case study presented in chapter 3. Three cases are presented to illustrate the functionality of the UCSC algorithm development. The simulation procedure and the system parameters for each case will be presented together with the advantages and disadvantages by making use of the results in the form of figures and tables. The analysis of the results and the conclusions are at the end of the chapter.

4.2 Simulation Cases

A set of simulations are presented in this chapter in order to proof the functionality of the UCSC system. The considered three different cases are the following:

- Case A: ideal DC link
- Case B: capacitor-based DC link
- Case C: capacitor-based DC link with enhanced UCSC control algorithm

The functionality of the UCSC system will be evaluated in every case by addressing:

- the percentage of unbalance;
- the percentage voltage drop across the impedance between the power substation and the PCC, before and after the UCSC system is operational;
- the UCSC controller algorithm speed response.

The procedure, parameters, results and analysis for each case are presented in the following sections. All the results are presented in the form of figures and tables. The three different cases are analyzed individually and a comparison between them is presented in the conclusions.

4.3 Case A – Ideal DC Link: Results and Analysis

This section presents the procedure and the parameters for case A. Furthermore, the results from the MATLAB/SIMULINK™ simulations are presented and analyzed in order to validate the functionality of the UCSC topology and control algorithm. The MATLAB/SIMULINK™ models and results are also presented. The three-phase four-wire, the UCSC MATLAB/SIMULINK™ and the phase *a* H-bridge models used for the simulations are depicted in Fig. 4-1, 4-2 and 4-3, respectively.

- ***Simulation Procedure***

The simulation conditions for case A are the following:

- ideal DC voltage source at the DC link;
- the current controller references are preset values; that is, inactive reference current generator;
- the voltage controller is also inactive due to having an ideal DC voltage source.

These conditions are set in order to study the performance of the UCSC control algorithm. Cases B and C will be used to analyze the complete UCSC control algorithm under more realistic conditions. The MATLAB/SIMULINK™ UCSC control algorithm model used for the simulation is illustrated in Fig. 4-4.

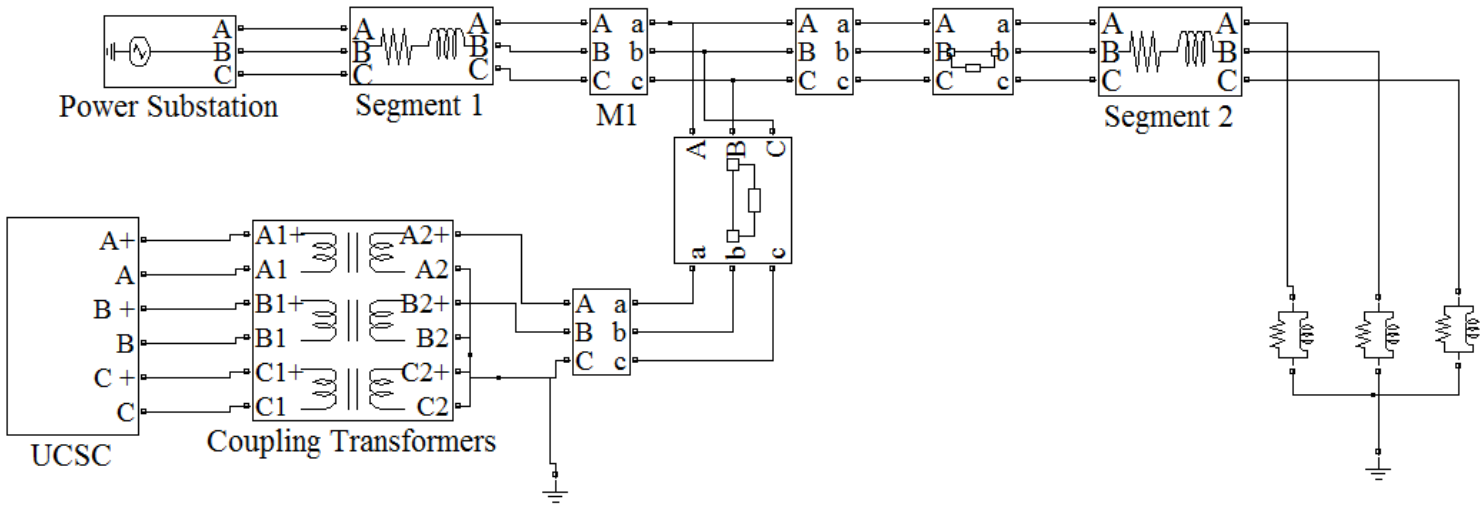

Fig. 4-1. Three-phase four-wire MATLAB/SIMULINK™ model

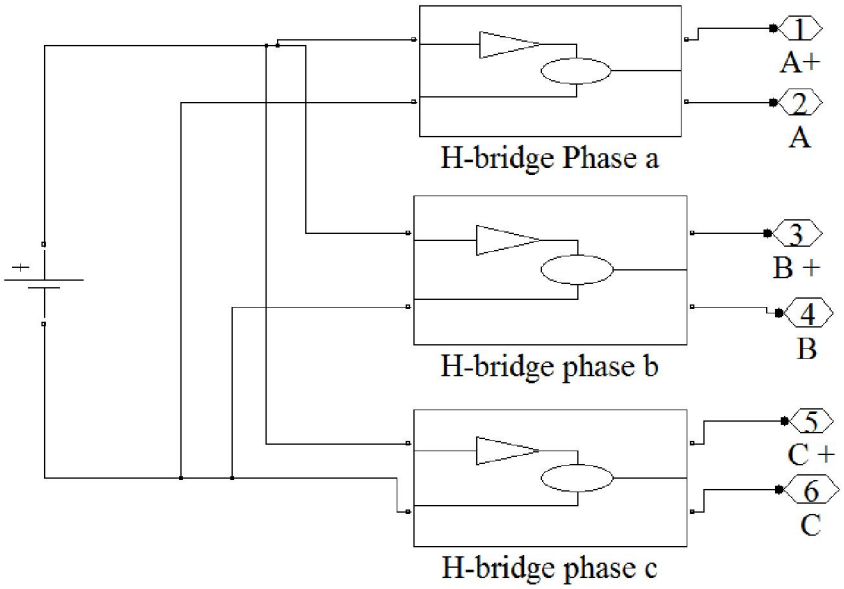

Fig. 4-2. UCSC MATLAB/SIMULINK™ model for case A

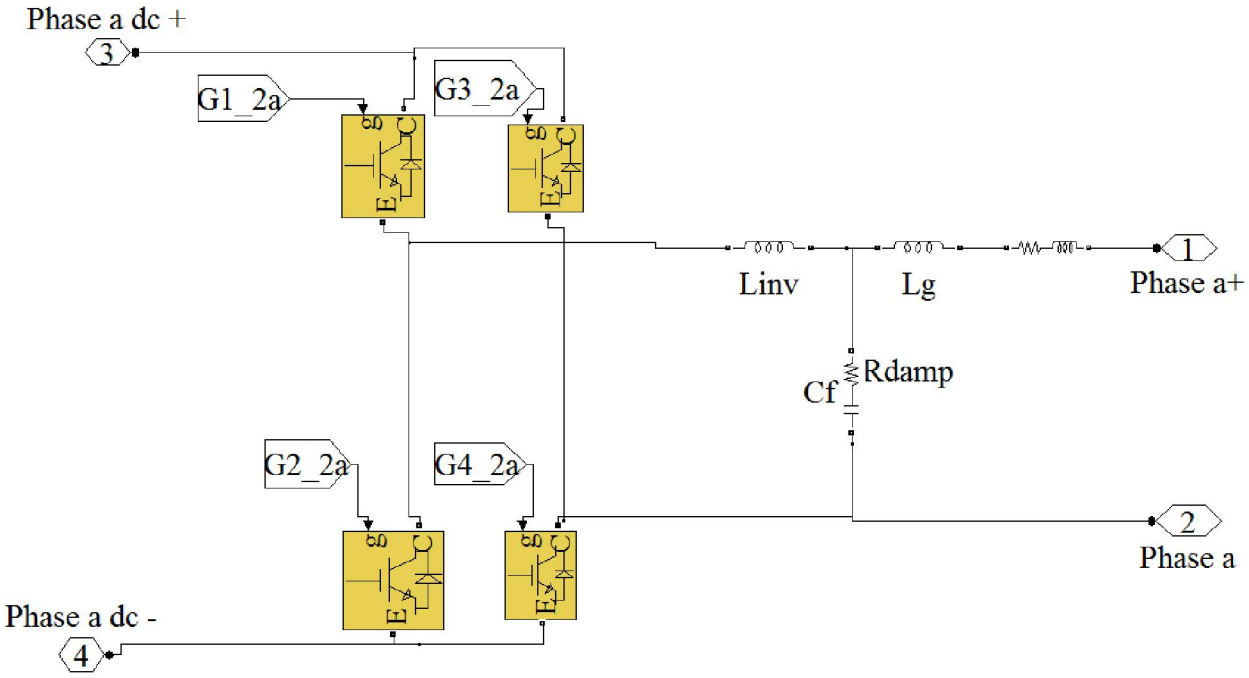

Fig. 4-3. Phase *a* MATLAB/SIMULINK™ H-bridge model

The references preset values for the UCSC are calculated based on the load values presented in Table 4-1. Taking in consideration that MATLAB/SIMULINK™ performs the calculations with peak values, the load reactive current magnitudes are the following:

$$I_{lar} = \frac{\sqrt{2} \times 0.5\ MVAR}{19.9\ kV} = 35.53\ A \tag{4-1}$$

$$I_{lbr} = \frac{\sqrt{2} \times 0.3\ MVAR}{19.9\ kV} = \ 21.32\ A \tag{4-2}$$

$$I_{lcr} = \frac{\sqrt{2} \times 0.4\ MVAR}{19.9\ kV} = 28.43\ A. \tag{4-3}$$

Given the fact that the UCSC will provide all the load reactive power, the active component reference magnitudes are calculated as follows:

$$I_{sa} = \frac{\sqrt{2} \times 0.877\ MW}{19.9\ kV} = 63.25\ A \tag{4-4}$$

$$I_{sb} = \frac{\sqrt{2} \times 0.707\ MW}{19.9\ kV} = 50.24\ A \tag{4-5}$$

$$I_{lsc} = \frac{\sqrt{2} \times 0.753\ MW}{19.9\ kV} = 53.51\ A. \tag{4-6}$$

Where the average is the following:

$$I_{average} = \frac{63.25 + 50.24 + 53.51}{3} = 55.34\ A \tag{4-7}$$

and the preset values for the active components are:

$$I_{ra} = 63.25\ A - 55.34\ A = 6.92\ A \tag{4-8}$$

$$I_{rb} = 50.24\ A - 55.34\ A = -5.09\ A \tag{4-9}$$

$$I_{rc} = 53.51\ A - 55.34\ A = -1.82\ A. \tag{4-10}$$

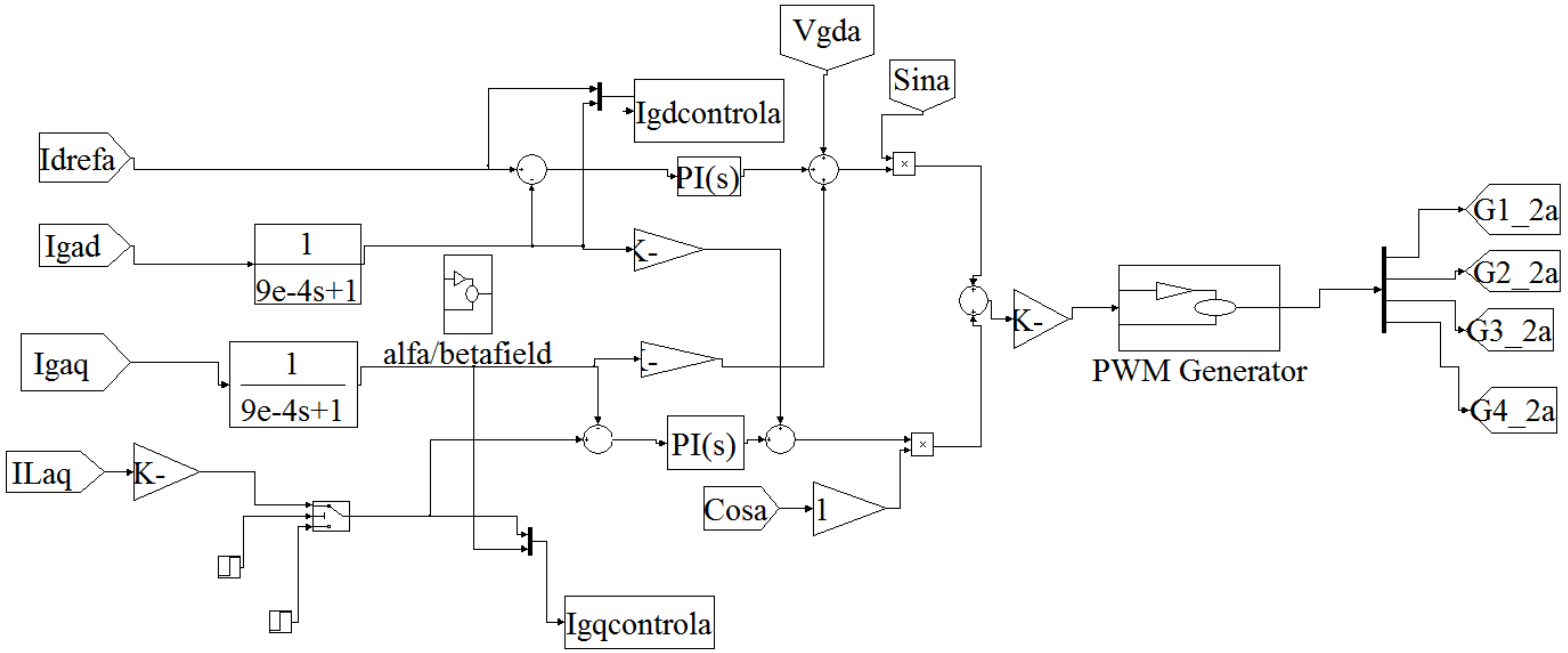

Fig. 4-4. UCSC control algorithm MATLAB/SIMULINK^{TM} mode for case A

The reactive and active preset values on the low voltage side of the coupling transformers are the following:

$$i_{gaq}^{*} = 35.53\ A \times \frac{19900V}{480V} = 1473.01\ A \tag{4-11}$$

$$i_{gbq}^{*} = 21.32\ A \times \frac{19900V}{480V} = 883.89\ A \tag{4-12}$$

$$i_{gbq}^{*} = 28.43\ A \times \frac{19900V}{480V} = 1178.66\ A \tag{4-13}$$

$$i_{gad}^{*} = 6.92\ A \times \frac{19900V}{480V} = 286.89\ A \tag{4-14}$$

$$i_{gbd}^{*} = -5.09\ A \times \frac{19900V}{480V} = -211.023\ A \tag{4-15}$$

$$i_{gbd}^{*} = -1.82\ A \times \frac{19900V}{480V} = -75.45\ A. \tag{4-16}$$

The simulation steps for the three cases are the following:

- interval I - from t = 0.00 s to t < 0.150 s the UCSC system is not operational;
- interval II - from t = 0.150 s to t = 0.6 s the UCSC system is operational.

➢ ***Simulation Parameters***

The UCSC, load and current controller parameters are illustrated in Tables 4-1, 4-2, and 4-3, respectively.

Table 4-1. UCSC system parameters

Parameter	Value
DC-link voltage level V_{DC} (V)	**1400**
Switching frequency f_{sw} (Hz)	**5400**
Phase voltage V_T (Vrms)	**480**
Energy storage capacitor C_{DC} (mF)	**4.90**

Table 4-2. Load parameters

Phase	MW	MVAR	Power Factor
a	**0.877**	**0.5**	**0.87 lagging**
b	**0.707**	**0.3**	**0.92 lagging**
c	**0.753**	**0.4**	**0.88 lagging**

Table 4-3. Current controller parameters for case A

Parameter	Value
Proportional gain K_{pi}	**1.19**
Integral gain K_{ii}	**75**

➢ ***Simulation Results and Analysis***

The DC-link voltage from Fig. 4-5 depicts the ideal case of a constant DC-link voltage. The next set of waveforms consists of the $d-q$ axes output currents ($i_{gabcd,}, i_{gabcq,}$) following the references (i^*_{gabcd}, i^*_{gabcq}) as depicted from Fig. 4-6 to Fig. 4-11.

From 0.00 s to t < 0.150 the UCSC the reference current for $d-q$ axes are set to 0 A. The controller response for phase *a* the *d*-axis current experiences an undershoot of -359 A and an overshoot of 521 A, respectively. From t = 0.150 s to t= 0.6 s the response has undershoot and overshoot values of -797.4 A and 853 A, respectively. All of these values are presented in Table 4-4.

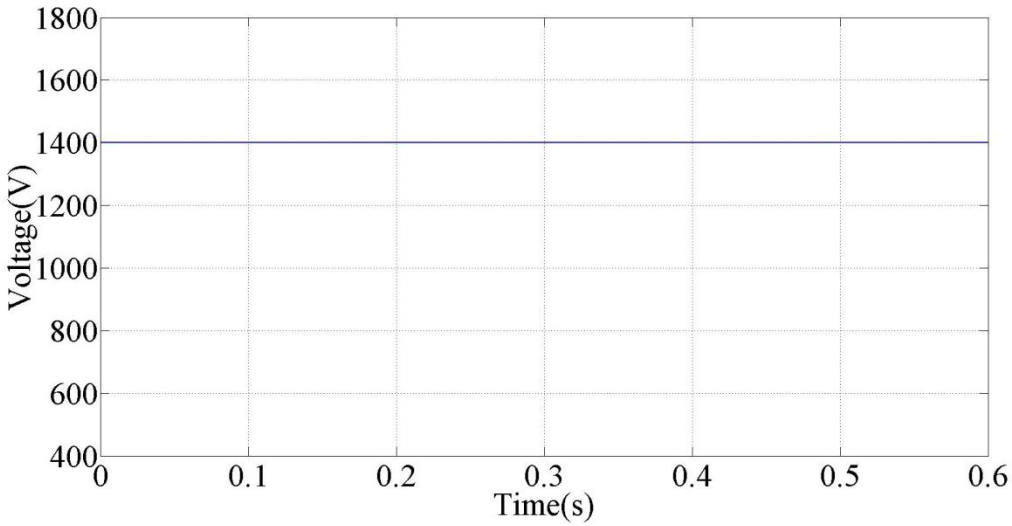

Fig. 4-5. DC-link voltage waveform for case A

Table 4-4. Undershoot, overshoot and values for the $\boldsymbol{d-q}$ axes control currents for case A

Current	Undershoot (A)		Overshoot (A)	
	Interval I	Interval II	Interval I	Interval II
i_{gad}	-359	-797.4	521	853
i_{gaq}	-177	-87.23	337	-2032
i_{gbd}	-458	479	678	-564
i_{gbq}	-168.5	0	119.7	-1229
i_{gcd}	-391.2	620.3	539	-305.2
i_{gcq}	-390.3	0	239.6	-1574

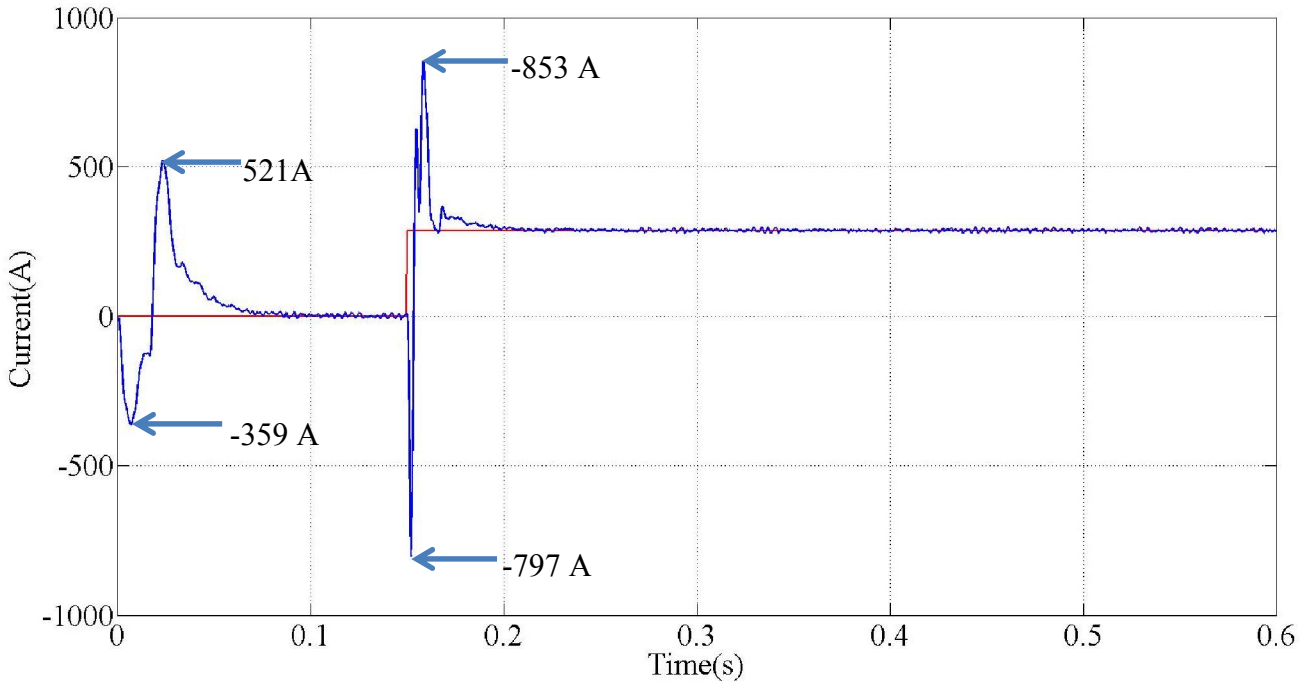

Fig. 4-6. Current i_{gad} and i_{gad}^{*} waveforms for case A

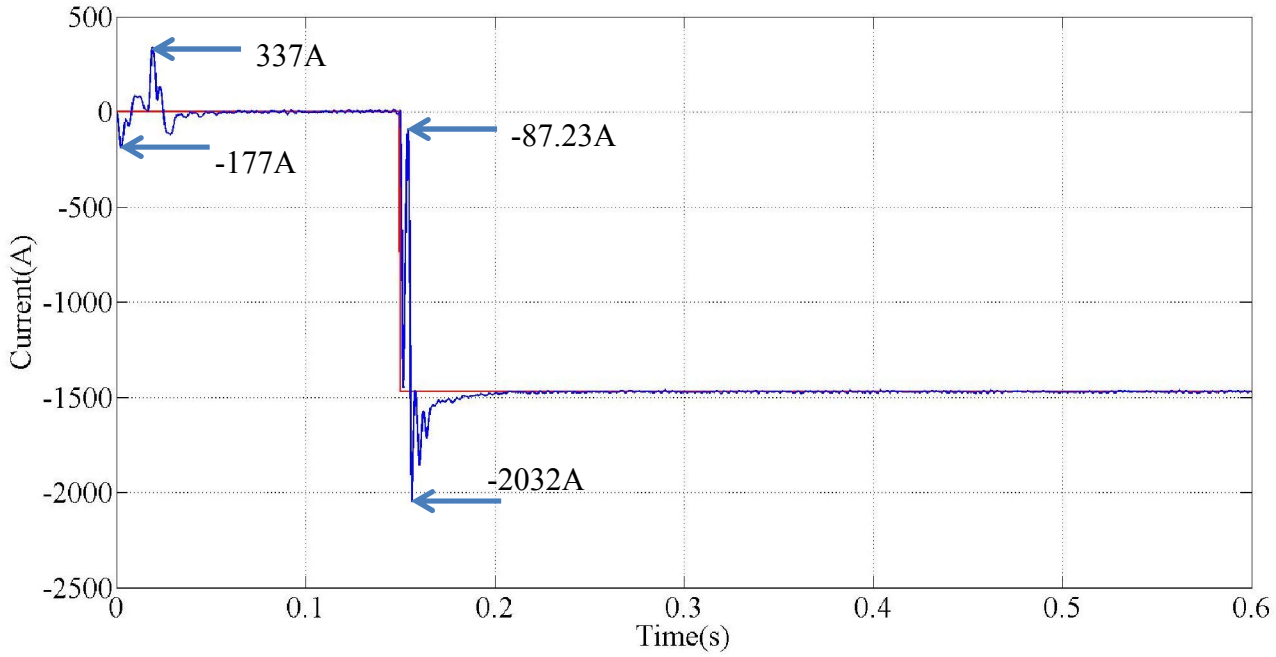

Fig. 4-7. Current i_{gaq} and i_{gaq}^{*} waveforms for case A

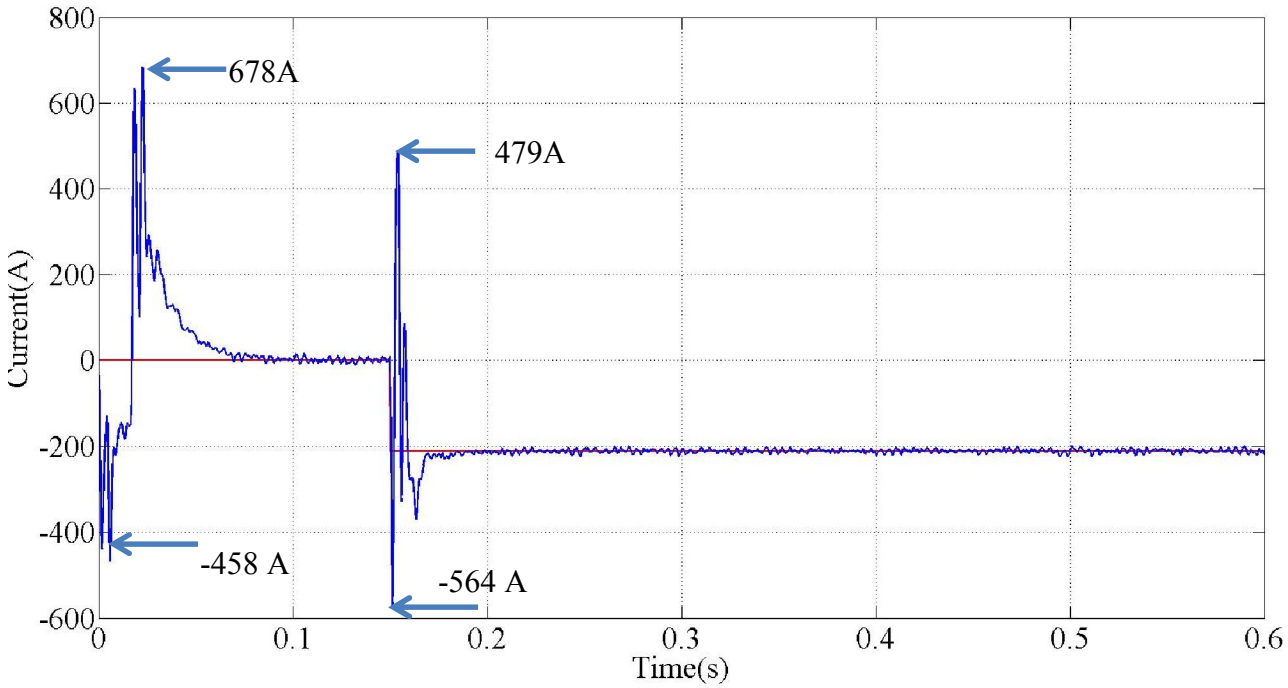

Fig. 4-8. Current i_{gbd} and i_{gbd}^{*} waveforms for case A

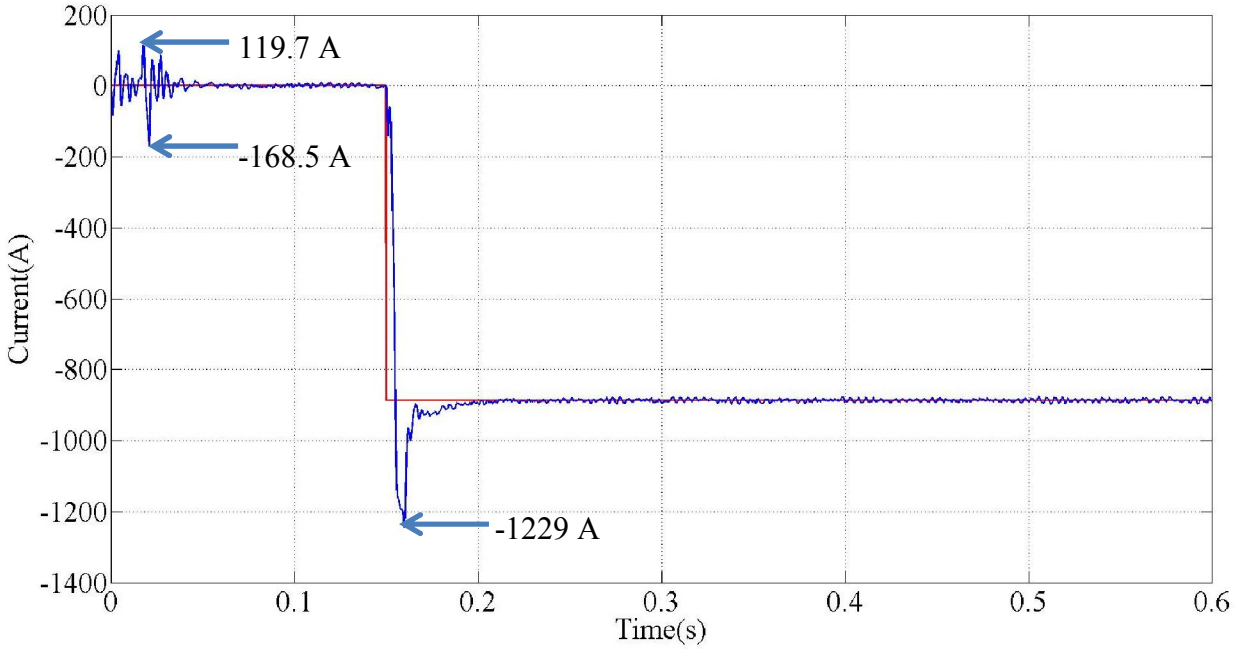

Fig. 4-9. Current i_{gbq} and i^*_{gbq} waveform for case A

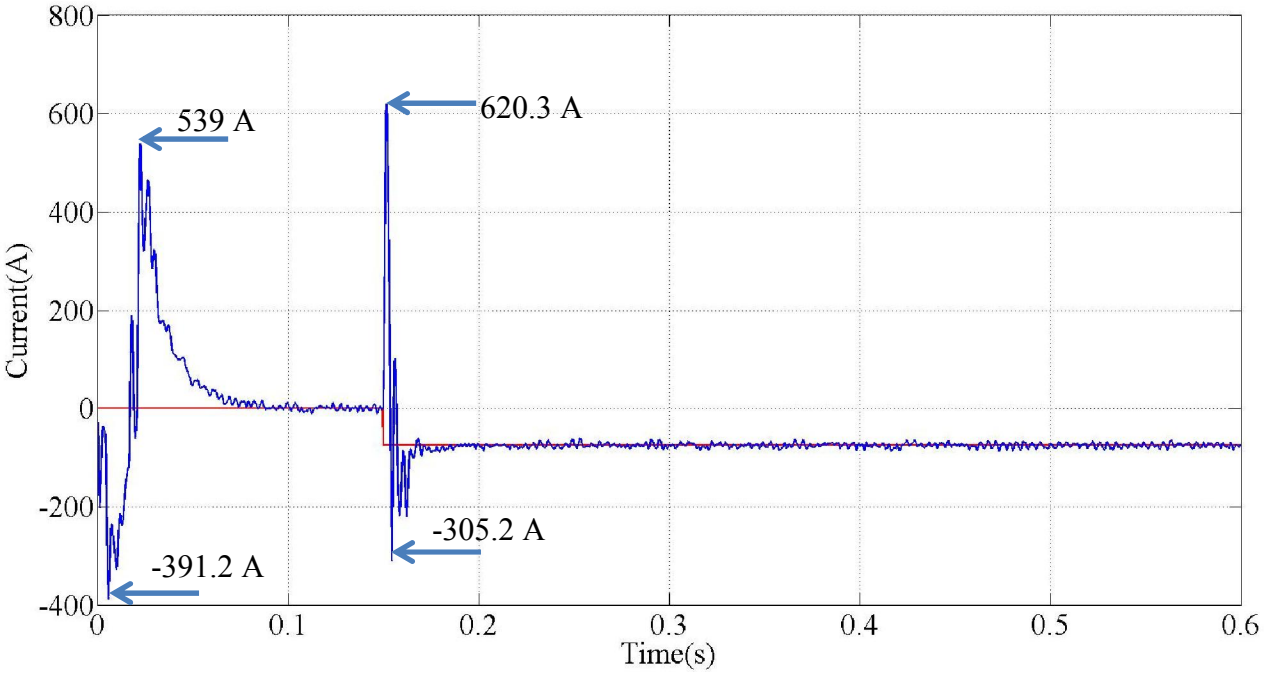

Fig. 4-10. Current i_{gcd} and i^*_{gcd} waveforms for case A

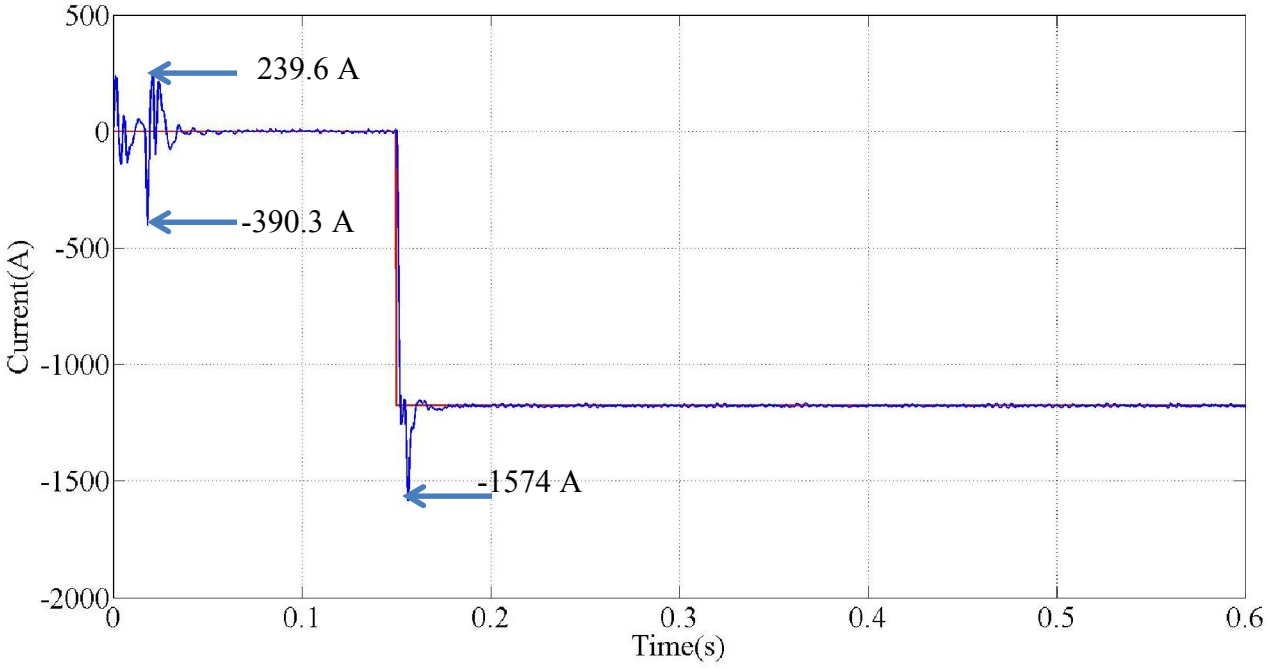

Fig. 4-11. Current i_{gcq} and i_{gcq}^{*} waveforms for case A

The compensating current waveform for phase a (i_{ca}) is shown in Fig. 4-12, and the compensating phasors ($\boldsymbol{I_{ca}}$, $\boldsymbol{I_{cb}}$, **and** $\boldsymbol{I_{cc}}$) values are given from Table 4-5 through Table 4-8, respectively.

Table 4-5. UCSC current phasor values for case A

Variable	**Value**
$\boldsymbol{I_{ca}}$	$\mathbf{36.08\angle -79.03^{\circ}}$ **A**
$\boldsymbol{I_{cb}}$	$\mathbf{21.98\angle 136.53^{\circ}}$ **A**
$\boldsymbol{I_{cc}}$	$\mathbf{28.45\angle 26.27^{\circ}}$ **A**

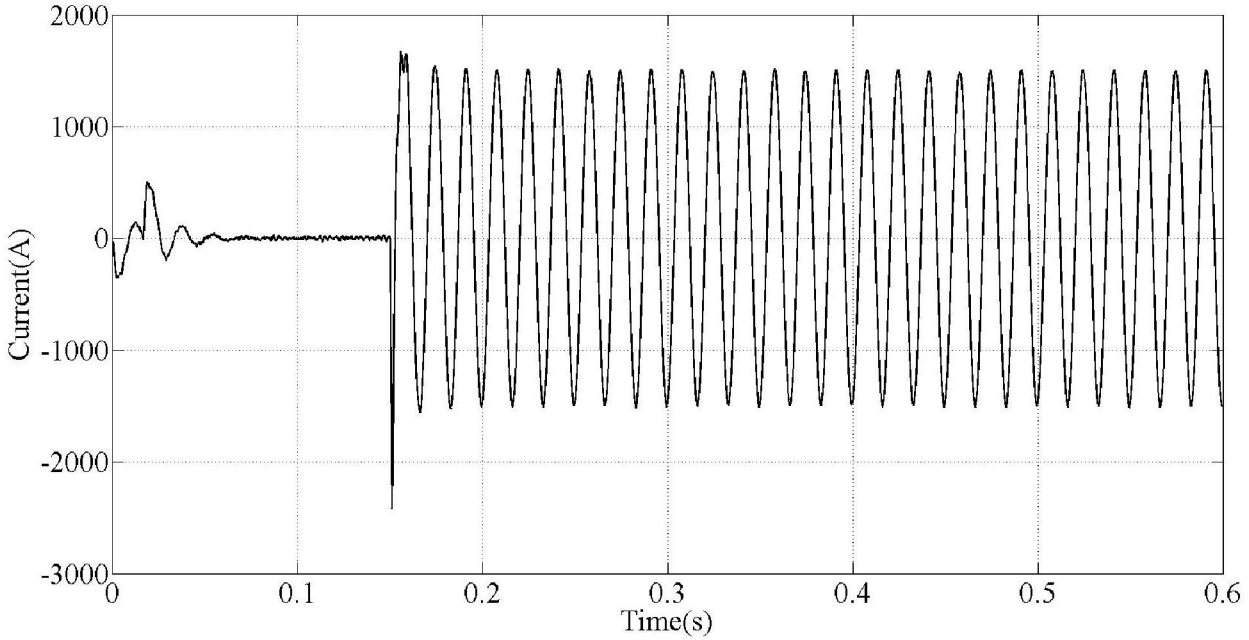

Fig. 4-12. UCSC current waveforms for case A

Table 4-6. UCSC positive-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	**0 A**	$\boldsymbol{I_1}$	$\boldsymbol{28.39\angle -90.07°}$**A**

Table 4-7. UCSC negative-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	**0 A**	$\boldsymbol{I_2}$	$\boldsymbol{4.68\angle -72.27°}$ **A**

Table 4-8. UCSC zero-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	**0 A**	$\boldsymbol{I_0}$	$\boldsymbol{6.04\angle -25.13^\circ}$ **A**

Before the UCSC is operational, the following unbalance conditions are present in the source currents as illustrated in Table 4-9:

- the difference in magnitude between phases *a* and *b* went from 17.12 A to 0.19 A. This means that the current in phase *a* was 31% higher than the current in phase *b* before UCSC operation;
- For phases *b* and *c* the difference went from 6.05 A to 0.02 A. The current in phase *c* was 11% higher than the current in phase *b* before the UCSC operation;
- Between phases *a* and *c* the difference in current magnitude decreased from 11.07 A to 0.17 A where the current in phase *a* was 18% higher than the current in phase *c* before UCSC operation.
- The overall current unbalance % can be calculated as follows [1]:
  - Before the UCSC is in operation:

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 27.53\% \qquad (4\text{-}17)$$

Once the compensating currents are injected into the electrical power grid, the currents at the source are balanced in magnitude and in phase with their associated voltages as illustrated in

Table 4.9. The waveform for phase *a* source current is presented in Fig. 4-13 and the three phases together in Fig. 4-14.

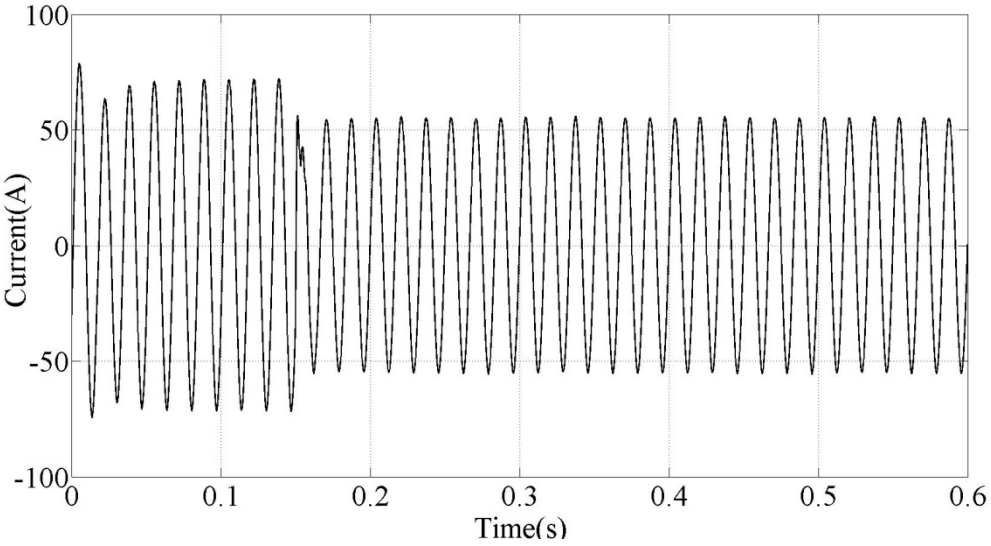

Fig. 4-13. Phase *a* source current waveform for case A

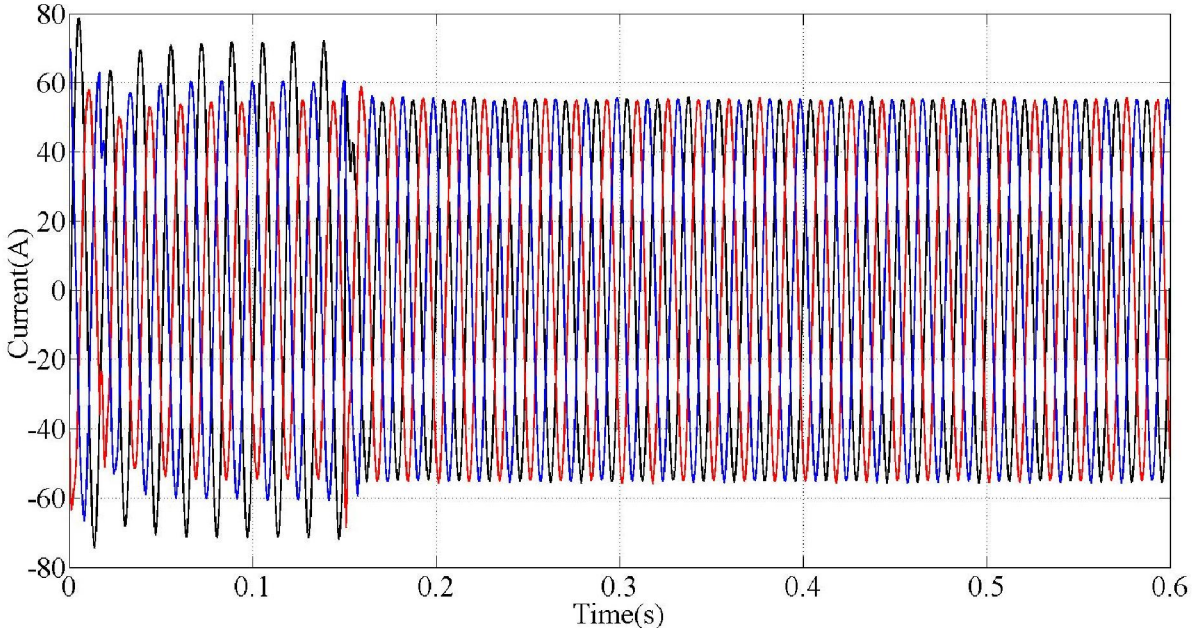

Fig. 4-14. Source current waveforms for case A

Table 4-9. Current phasors values at source for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_{sa}}$	$\mathbf{71.57\angle -29.72°}$ **A**	$\boldsymbol{I_{sa}}$	$\mathbf{55.27\angle 0}$
$\boldsymbol{I_{sb}}$	$\mathbf{54.45\angle -143°}$ **A**	$\boldsymbol{I_{sb}}$	$\mathbf{55.26\angle -119.92}$
$\boldsymbol{I_{sc}}$	$\mathbf{60.50\angle 92.05°}$ **A**	$\boldsymbol{I_{sc}}$	$\mathbf{55.25\angle 120}$

Due to the injection of the compensating currents of Table 4-5, the percentage of unbalance changed as follows:

- After the UCSC is in operation

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 0.04\% \quad (4\text{-}18)$$

Another aspect that can be analyzed is the difference in voltage drop along the impedance of segment 1 with and without current compensation. The difference can be calculated as follows:

- Before the UCSC is in operation

$$\boldsymbol{V}_{dropa} = (71.57\angle -29.72°)(0.24 + j0.14) = 19.88\angle 0.54\, V \quad (4\text{-}19)$$

$$\boldsymbol{V}_{dropb} = (54.45\angle -143°)(0.24 + j0.14) = 14.74\angle -112.74\, V \quad (4\text{-}20)$$

$$\boldsymbol{V}_{dropc} = (60.50\angle 92.05°)(0.24 + j0.14) = 16.42\angle 121.76\, V \quad (4\text{-}21)$$

- After the UCSC is in operation

$$\boldsymbol{V}_{dropa} = (55.27\angle 0°)(0.24 + j0.14) = 15.36\angle 30.26°\, V \quad (4\text{-}22)$$

$$\boldsymbol{V}_{dropb} = (55.56\angle -120°)(0.24 + j0.14) = 15.35\angle -89.74\, V \quad (4\text{-}23)$$

$$\boldsymbol{V}_{dropc} = (55.43\angle 120°)(0.24 + j0.14) = 15.35\angle 150.26\, V \quad (4\text{-}24)$$

where

- $\boldsymbol{V}_{dropa}$ is the voltage drop in segment 1 for phase *a*;
- $\boldsymbol{V}_{dropb}$ is the voltage drop in segment 1 for phase *b*;
- $\boldsymbol{V}_{dropc}$ is the voltage drop in segment 1 for phase *c*.

Once the UCSC is connected, the current unbalance in the system is reduced between the three phases which leads to equal voltage drops in the three phases as a result of balanced currents at the source (in magnitude and phase) when the UCSC is in operation.

Another important aspect that should be analyzed is the amount of negative- and zero-sequence at the source. The results are illustrated from Fig. 4.15 to Fig. 4-17 and from Table 4-10 through Table 4-12.

The following conclusions can be drawn from the symmetrical components current phasor values:

- the magnitude of the negative- and zero-sequence currents went from 4.61 A and 6.1 A to 0.08 A and 0.05 A, respectively. This is a decrease of 58 and 122 times the original unbalanced current for the negative- and zero-sequence, respectively;
- the negative- and zero-sequence currents reached a value below 1 A in 0.026 s (1.6 cycles) and 0.021 s (1.3 cycles), respectively;
- the current unbalance was reduced from 27.53 % to 0.04 %, respectively.

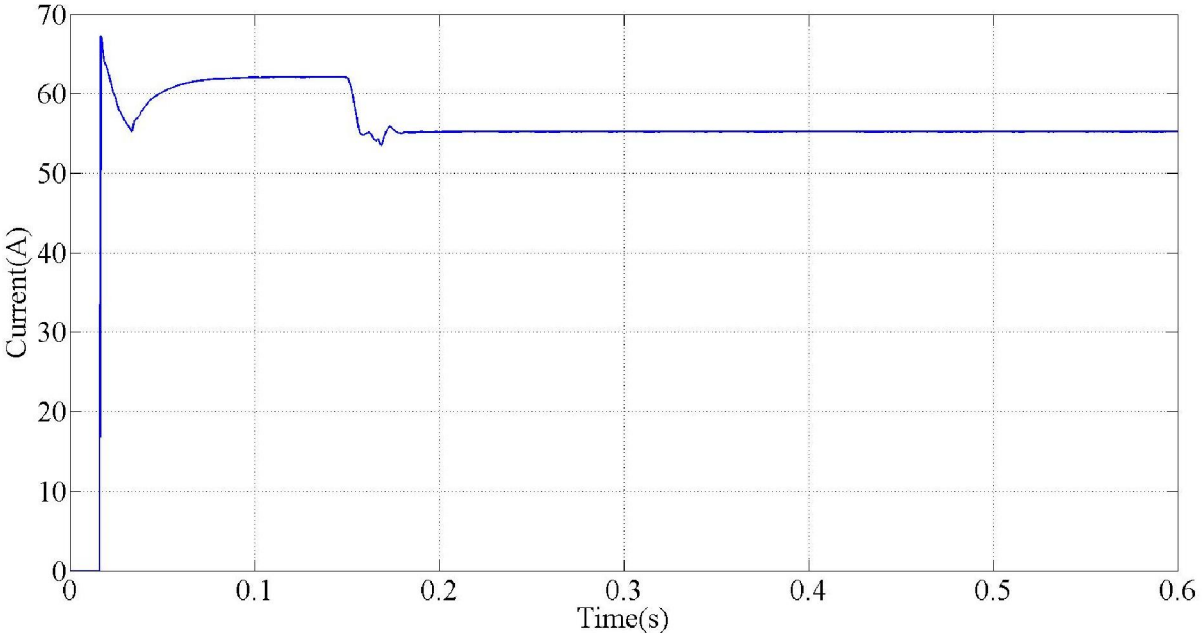

Fig. 4-15. Positive-sequence current magnitude at the source for case A

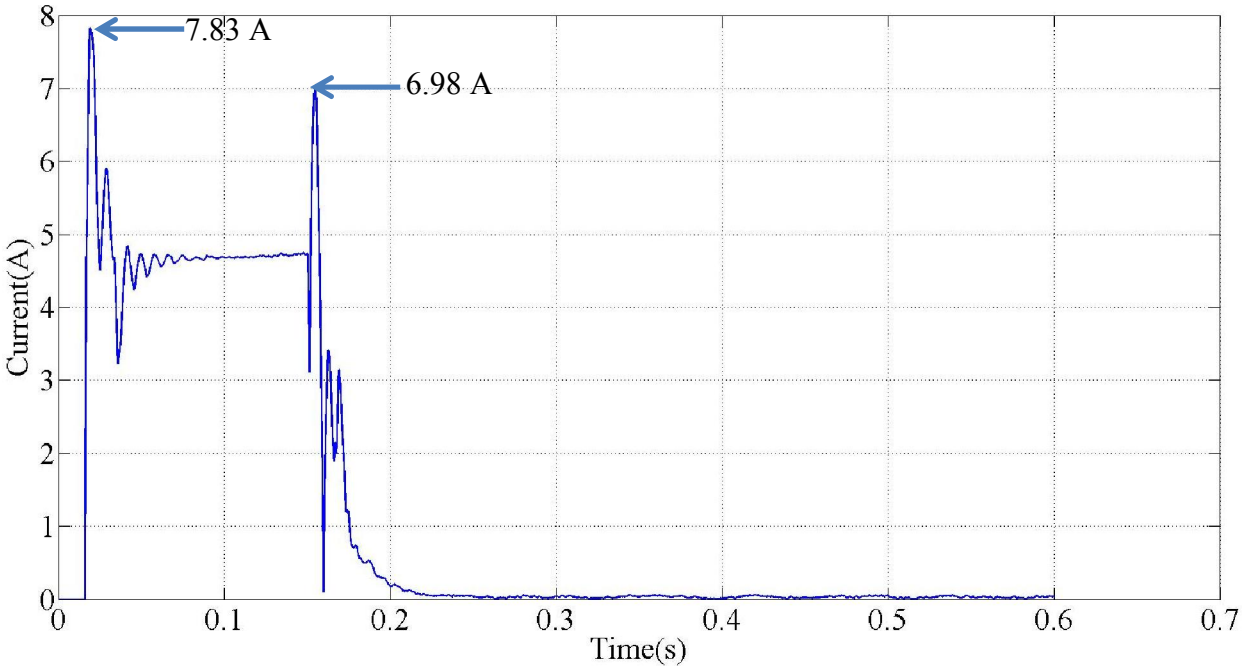

Fig. 4-16. Negative-sequence current magnitude at the source for case A

Two transients are depicted in Fig. 4-16, one during the start of the simulation and another one when the UCSC starts operating at 0.150 s. The magnitudes that are reached in both cases are 7.83 A and 6.98 A, respectively.

Table 4-10. Positive-sequence current phasor values at the source for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{62.1\angle -27.2^\circ}$ **A**	$\boldsymbol{I_1}$	$\mathbf{55.26\angle 0}$ **A**

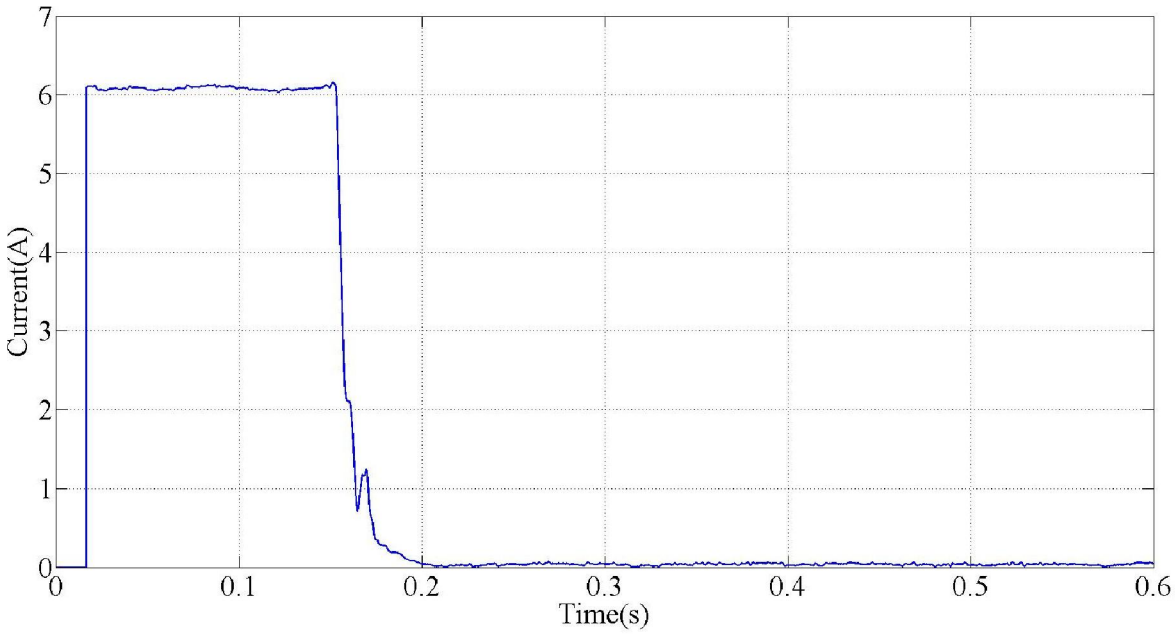

Fig. 4-17. Zero-sequence current magnitude at the source for case A

Table 4-11. Negative-sequence current phasor values at the source for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.61\angle -75.2°A}$	$\boldsymbol{I_2}$	$\mathbf{0.03\angle -117.16°\ A}$

Table 4-12. Zero-sequence current phasor values at the source for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.10\angle -25.7°\ A}$	$\boldsymbol{I_0}$	$\mathbf{0.04\angle -50.93\ A}$

For illustration purposes, the phasor values, the symmetrical components and waveforms of the load currents ($\boldsymbol{I_{la}, I_{lb}, I_{lc}}$) are illustrated from Table 4-13 through Table 4-16 and in Fig. 4.18, respectively

Table 4-13. Load current phasor values for case A

Variable	**Value**
$\boldsymbol{I_{la}}$	$\mathbf{71.55\angle -29.7°A}$
$\boldsymbol{I_{lb}}$	$\mathbf{54.46\angle -143°\ A}$
$\boldsymbol{I_{lc}}$	$\mathbf{60.48\angle 92°\ \ A}$

Table 4-14. Load positive-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20^\circ}$ **A**	$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20^\circ}$ **A**

Table 4-15. Load negative-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54^\circ}$**A**	$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54^\circ}$**A**

Table 4-16. Load zero-sequence current phasor values for case A

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32}$ **A**	$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32}$ **A**

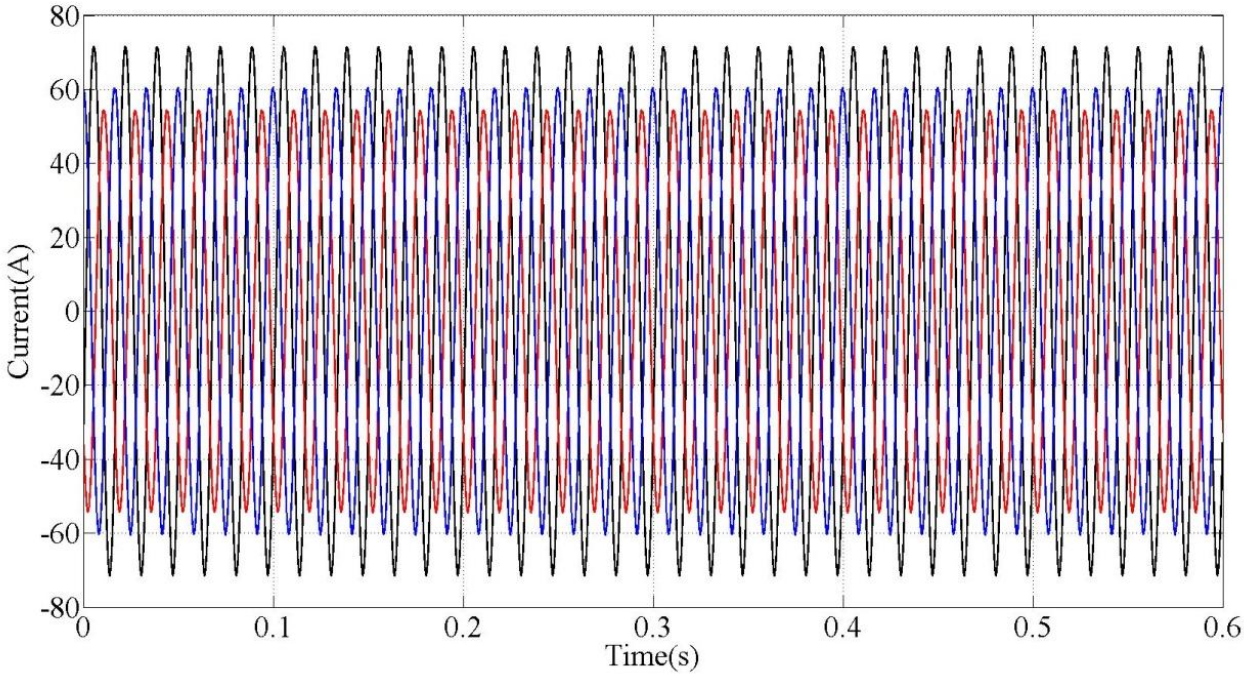

Fig. 4-18. Load current waveforms for case A

4.4 Case B – Capacitor-based DC Link

This section will present the simulation procedure, the system parameters and the simulation results and analysis for case B. A comparison between the results from cases A and B is presented.

- ***Simulation Procedure***

For case B, the ideal DC voltage source is replaced by an electrolytic capacitor having the capacitance value selected in section 3.2. The remaining conditions for case B are the following:

- the voltage controller is active;
- the reference current generator algorithm is active.

The MATLAB/SIMULINK^{TM} UCSC and control algorithm models are depicted in Figs. 4.19 and 4.20, respectively.

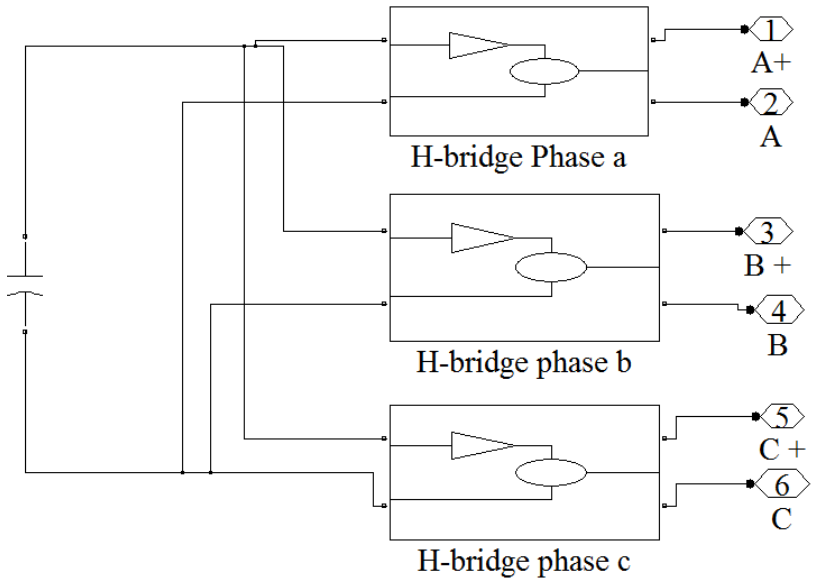

Fig. 4-19. UCSC MATLAB/SIMULINK™ model for case B

- ***Simulation Parameters***

The controller parameters for cases B and C are presented in Table 4.17. The results and analysis is presented in the next section.

Table 4-17. Controller parameters for cases B and C

Current Controller		**Reference Current Generator**		**Voltage Controller**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
Proportional gain K_{pi}	**0.53**	**Proportional gain K_p**	**2.14**	**Proportional gain K_{vp}**	**0.64**
Integral gain K_{ii}	**15**	**Integral gain K_i**	**60**	**Integral gain K_{vi}**	**34**

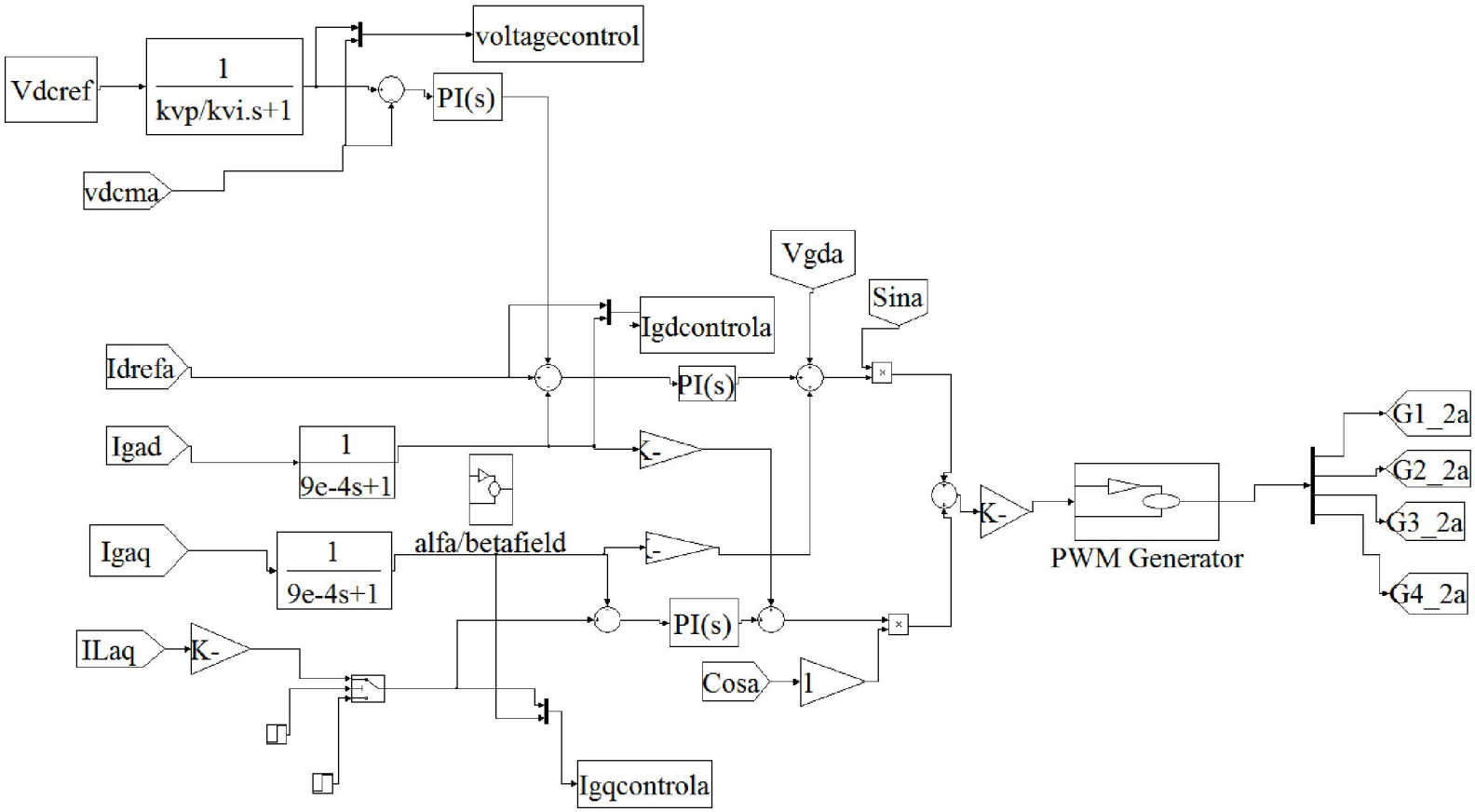

Fig. 4-20. UCSC control algorithm MATLAB/SIMULINK^{TM} mode for case B

➢ ***Simulation Results and Analysis***

The DC-link voltage waveform is depicted in Fig. 4-21 and the first difference noticed when comparing it with the DC-link voltage waveform from Fig. 4-5 is that the voltage contains a voltage ripple produced by the second harmonic component of the DC-side current [4]. Assuming lossless devices and fictitious filters, the following mathematical equations describe this issue [4]:

$$V_{DC} i_{DC}(t) = v_{ga}(t) i_{ga}(t) = \sqrt{2} V_{ga} \sin(\omega_s t) \sqrt{2} I_{ga} \sin(\omega_s t - \phi) \tag{4-25}$$

$$i_{DC}(t) = \frac{V_{ga} I_{ga}}{V_{DC}} \cos(\phi) - \frac{V_{ga} I_{ga}}{V_{DC}} \cos(2\omega_s t - \phi) \tag{4-26}$$

$$i_{DC}(t) = I_{DC} - \sqrt{2} I_{DC2} \cos(2\omega_s t - \phi) \tag{4-27}$$

where

- V_{DC} is the DC-link voltage;
- $i_{DC}(t)$ is the DC-side current;
- V_{ga} is the grid-side voltage magnitude for phase a;
- I_{ga} is the grid-side current magnitude for phase a;
- I_{DC} is the DC component of the DC-side current;
- I_{DC2} is the magnitude of the second harmonic component of the DC-side current;
- ω is the fundamental frequency in radians per second.

Equation (4-27) illustrates that the DC-side current contains an AC component at twice the fundamental frequency [4]. The $d-q$ axes control waveforms from Fig. 4-22 through Fig. 4-27 illustrate the fact that the voltage ripple gets introduced into the control algorithm. This issue can cause distortions in the output current waveforms of the single-phase H-Bridge converters [5]. The undershoot, and overshoot values for the interval I and II of the simulation

are illustrated in Table 4-18. The frequency of the DC-voltage ripple and the frequency of the control signals in the $d-q$ axes are 125 and 243 Hz, respectively.

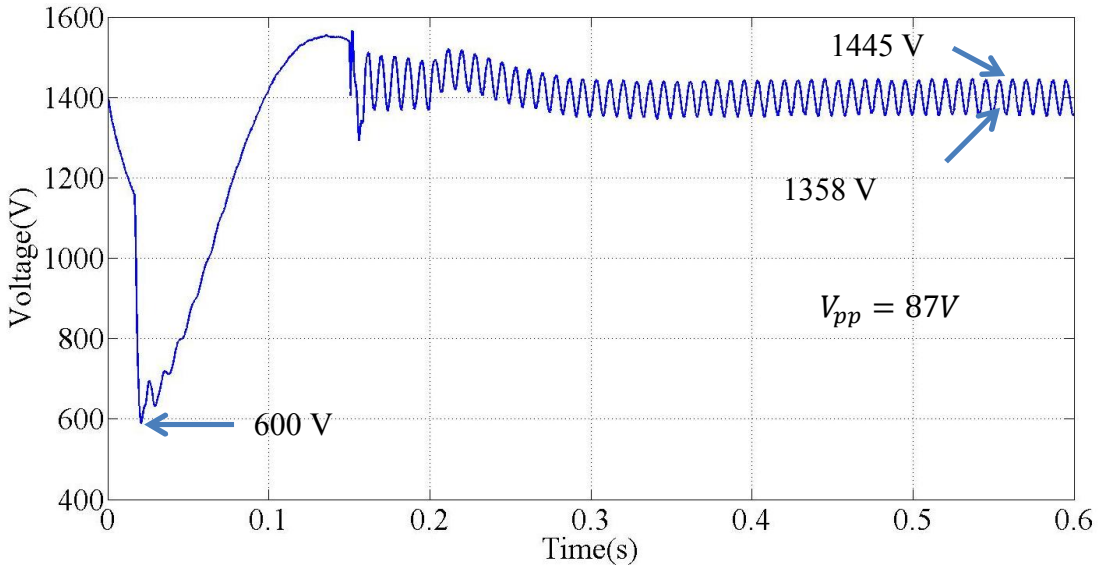

Fig. 4-21. DC-link voltage waveform for case B

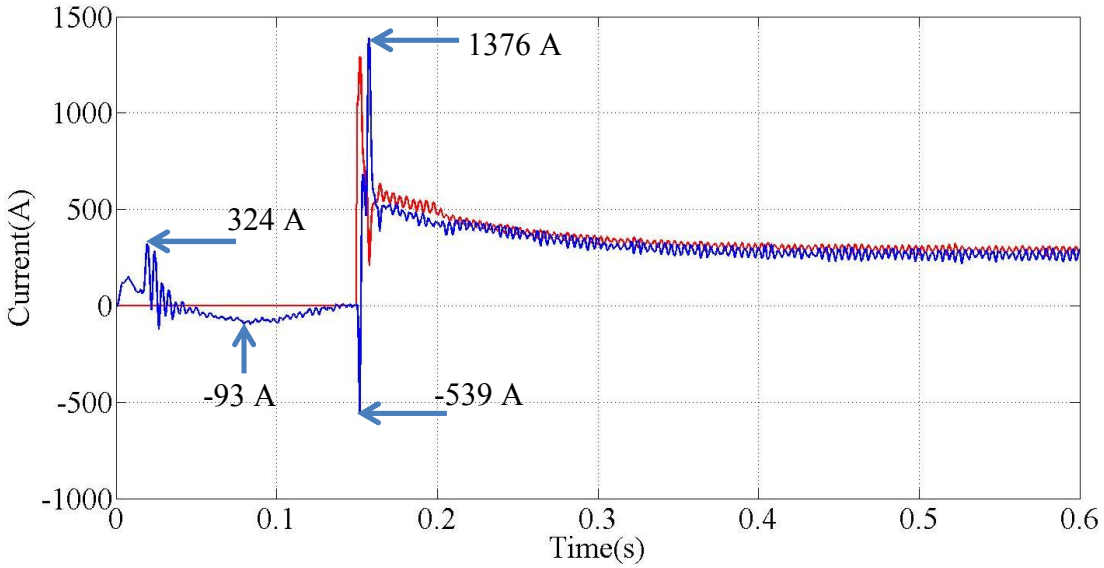

Fig. 4-22. Current i_{gad} and i_{gad}^{*} waveforms for case B

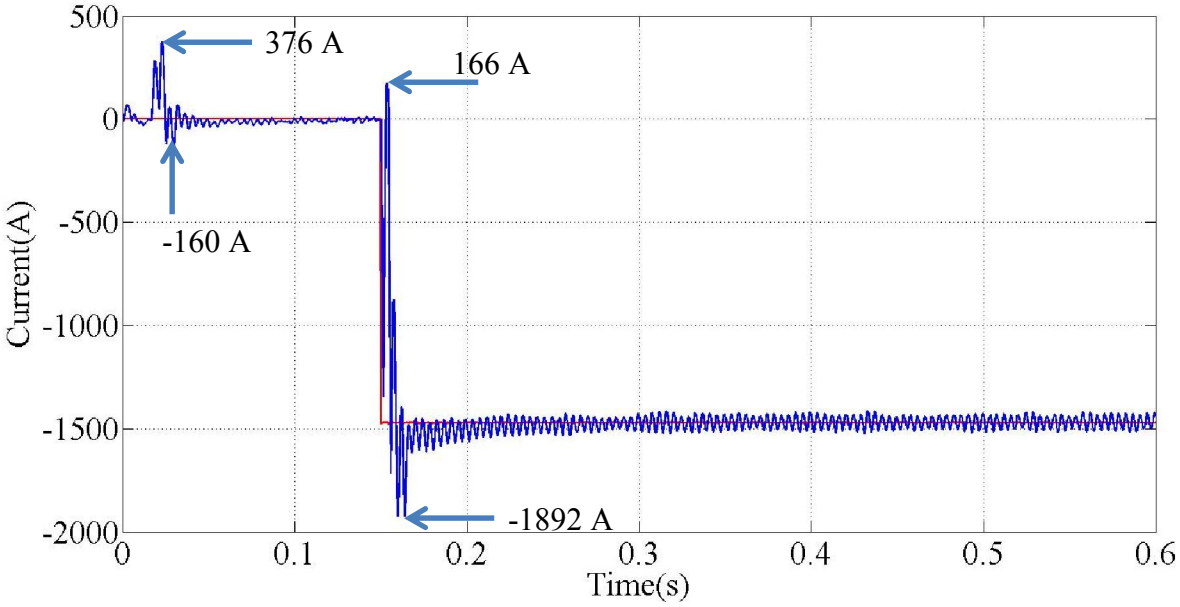

Fig. 4-23. Current i_{gaq} and i_{gaq}^{*}waveforms for case B

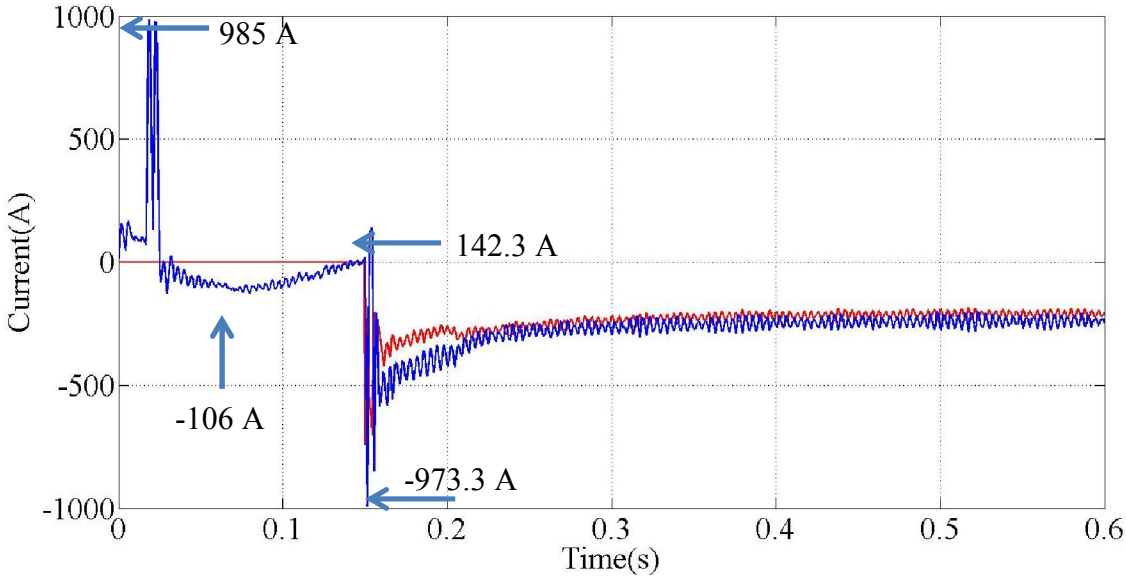

Fig. 4-24. Current i_{gbd} and i_{gbd}^{*} waveforms for case B

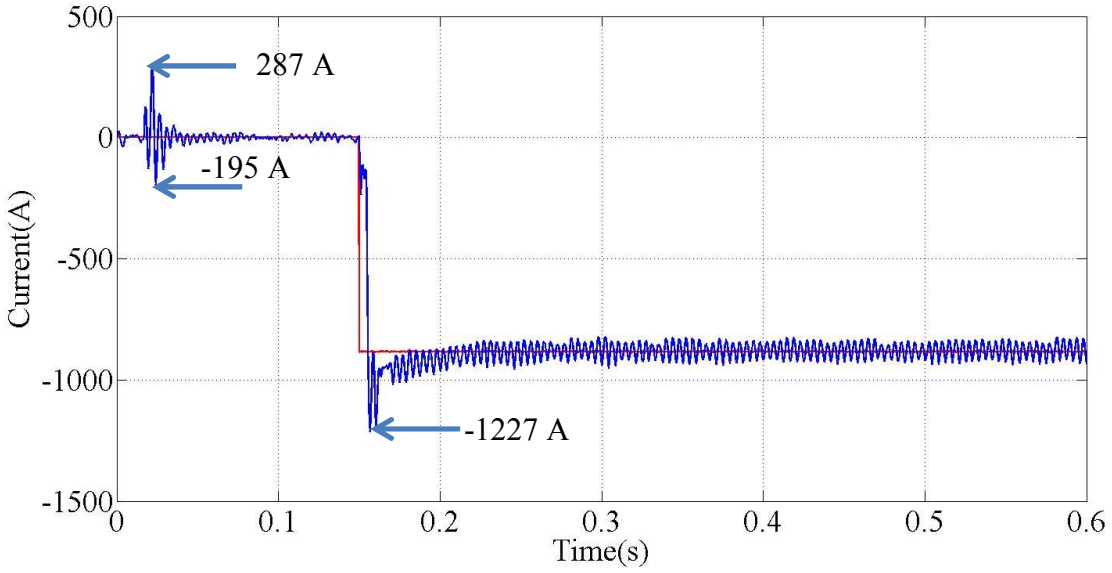

Fig. 4-25. Current i_{gbq} and i^*_{gbq}waveforms for case B

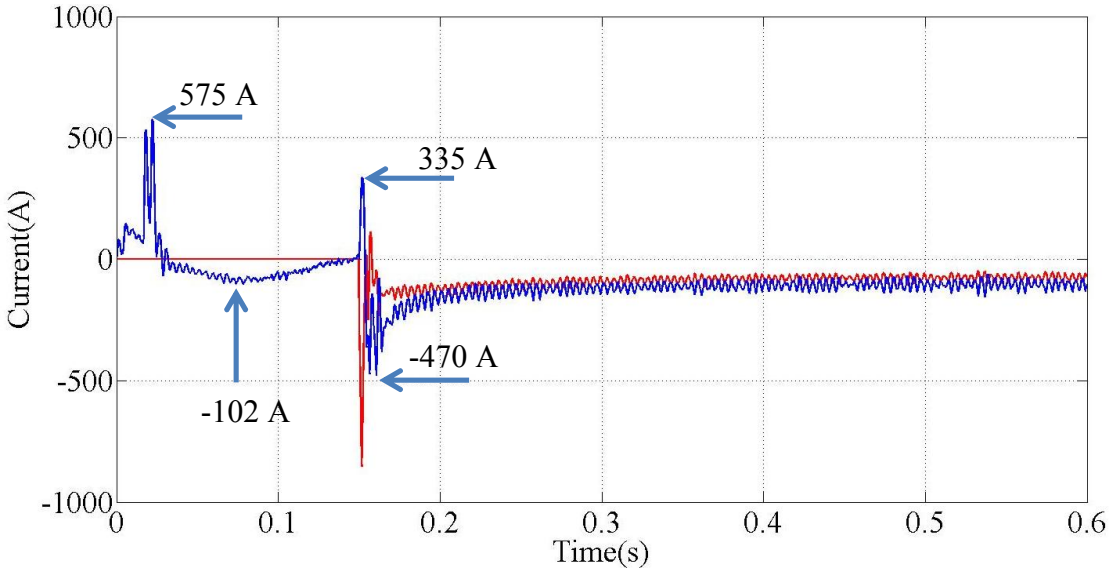

Fig. 4-26. Current i_{gcd} and i^*_{gcd}waveforms for case B

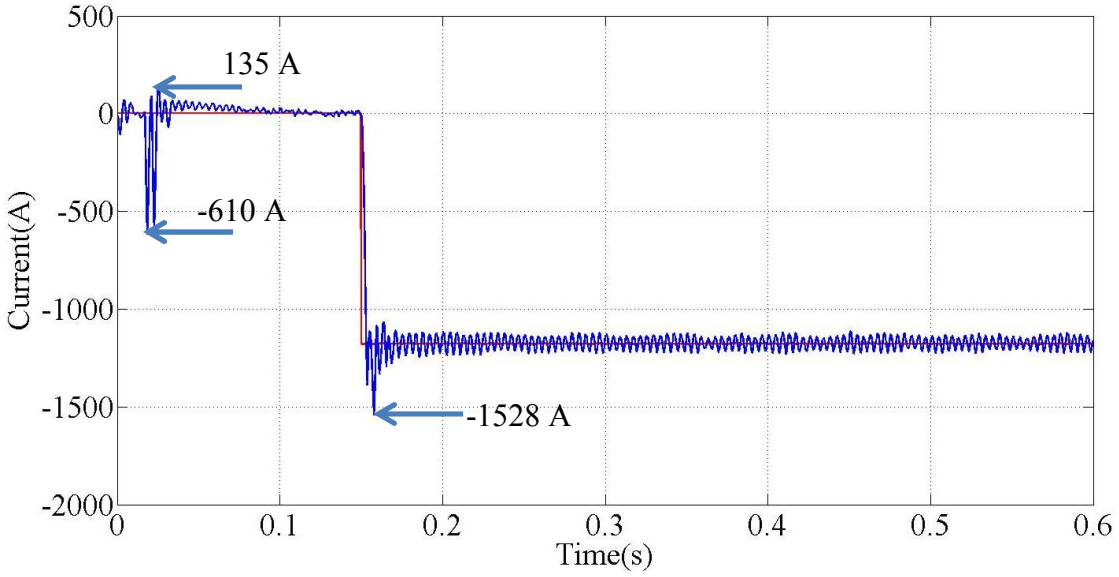

Fig. 4-27. Current i_{gcq} and i_{gcq}^{*}waveforms for case B

Table 4-18. Case B undershoot, overshoot values for the $\boldsymbol{d-q}$ axes control currents for

Current	Undershoot (A)		Overshoot (A)	
	Interval I	Interval II	Interval I	Interval II
i_{gad}	-93	-539	324	1376
i_{gaq}	-160	166	376	-1892
i_{gbd}	-106	142.3	985	-973.3
i_{gbq}	-195	0	287.3	-1227
i_{gcd}	-102	335	575	-470
i_{gcq}	-610	0	135	-1528

The compensating current phasors generated by the UCSC system are illustrated in Table 4-19 and the waveform for the phase *a* compensating current in Fig. 4-28. The positive-, negative- and zero-sequence phasors values are presented in Table 4-18 through Table 4-20, respectively.

Table 4-19. UCSC current phasor values for case B

Variable	Value
$\boldsymbol{I_{ca}}$	$\mathbf{36.04\angle -79.96°A}$
$\boldsymbol{I_{cb}}$	$\mathbf{21.99\angle 134.55°\ A}$
$\boldsymbol{I_{cc}}$	$\mathbf{28.43\angle 24.79°\ A}$

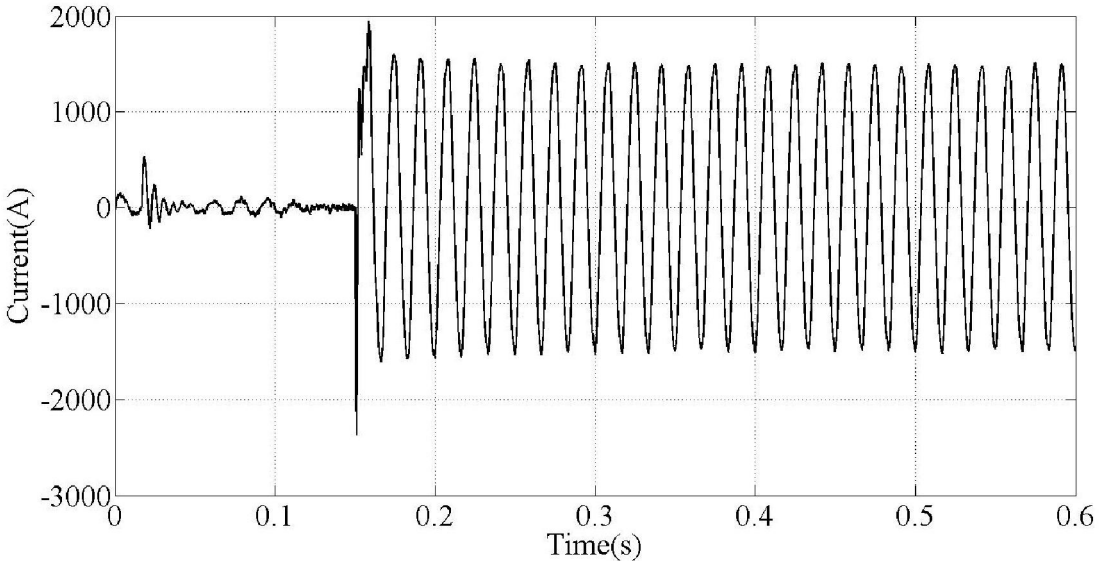

Fig. 4-28. UCSC phase *a* current waveforms for case B

Table 4-20. UCSC positive-sequence current phasor values for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	**0 A**	$\boldsymbol{I_1}$	$\boldsymbol{28.34\angle -91.45°}$**A**

Table 4-21. UCSC negative-sequence current phasor values for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	**0 A**	$\boldsymbol{I_2}$	$\boldsymbol{4.75\angle -72.29°}$ **A**

Table 4-22. UCSC zero-sequence current phasor values for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	**0 A**	$\boldsymbol{I_0}$	$\boldsymbol{6.15\angle -25.37}$ **A**

The values for the current phasors at the source before and after the UCSC is connected to the system are depicted in Table 4-23. The values are obtained through the waveforms illustrated in Fig. 4-29 and 4-30, respectively. It is concluded that the UCSC control algorithm managed to balance the currents at the source in magnitude and be in phase with their associate phase voltages.

The unbalance between the phase currents is the following:

- the difference in magnitude between phases *a* and *b* went from 16.93 A to 0.13 A. This means that the current in phase *a* was 31% higher than the current in phase *b*.
- For phases *b* and *c* the difference went from 5.98 A to 0.01 A; leading to current in phase *c* being 11% higher than the current in phase *b*. For phases *a* and *c* the difference in current magnitude decreased from 10.95 a to 0.12 A. The current in phase *a* was 18% higher than the current in phase *c*.
- The overall current unbalance % can be calculated as follows [1]:
  - Before the UCSC is in operation:

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 27.53\ \% \qquad (4\text{-}28)$$

  - After the UCSC is in operation

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 0.23\ \% \qquad (4\text{-}29)$$

Table 4-23. Current phasors at the source for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_{sa}}$	$\mathbf{71.47\angle -28.63°\ A}$	$\boldsymbol{I_{sa}}$	$\mathbf{55.86\angle 0}$
$\boldsymbol{I_{sb}}$	$\mathbf{54.54\angle -143°\ A}$	$\boldsymbol{I_{sb}}$	$\mathbf{55.99\angle -120}$
$\boldsymbol{I_{sc}}$	$\mathbf{60.52\angle 91.92°\ A}$	$\boldsymbol{I_{sc}}$	$\mathbf{55.98\angle 119.84}$

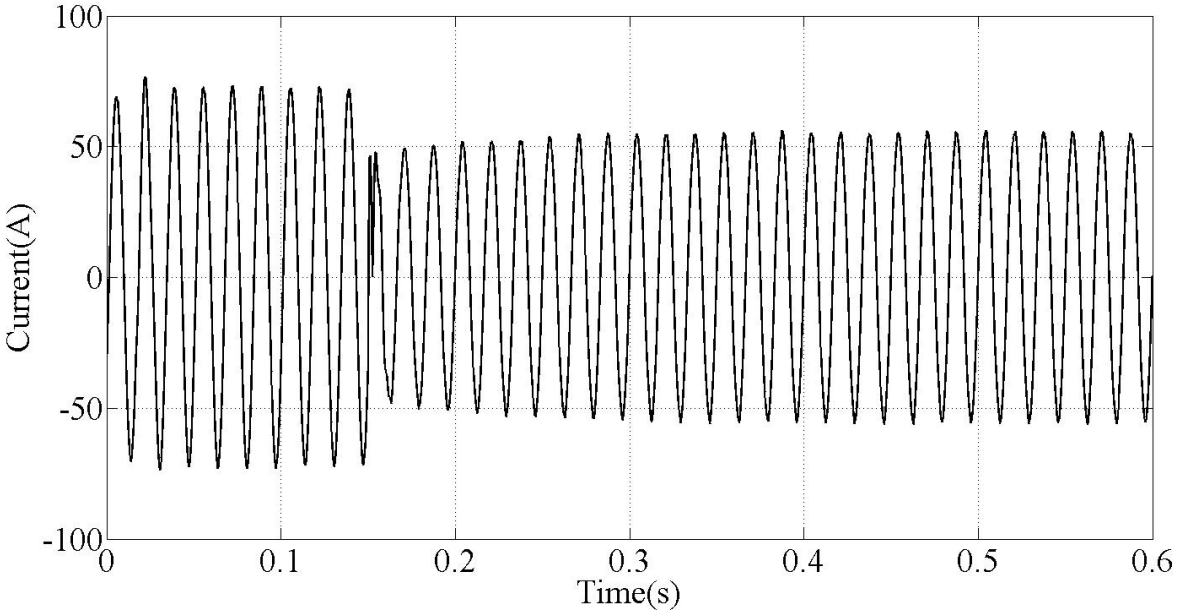

Fig. 4-29. Phase *a* source current waveform for case B

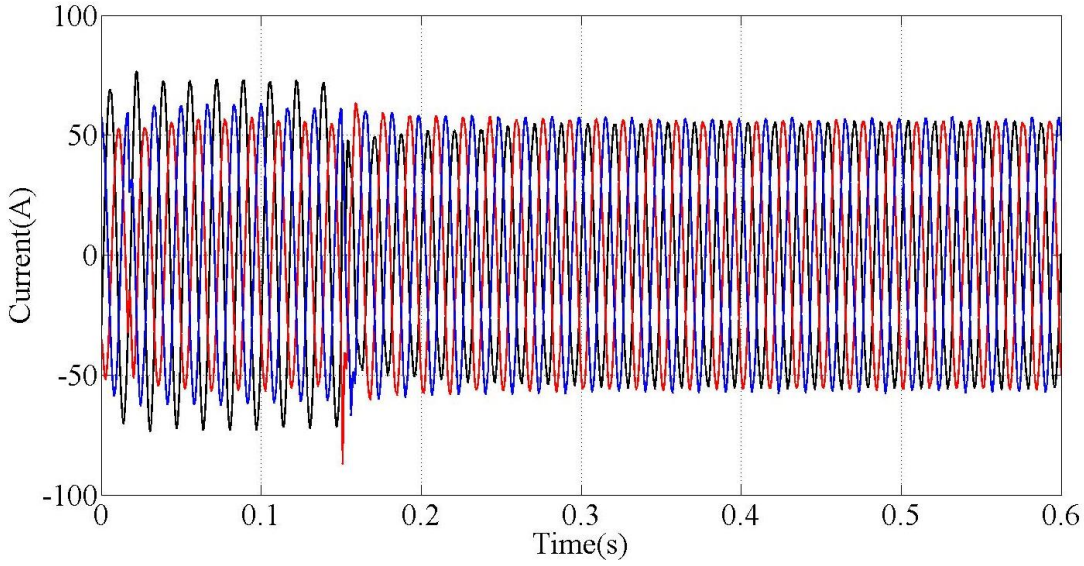

Fig. 4-30. Source current waveforms for case B

The voltage drops along the impedance of segment 1 for each phase are the following:

- Before the UCSC is in operation

$$\boldsymbol{V}_{dropa} = (71.47\angle -28.63°)(0.24 + j0.14) = 19.86\angle 1.63\, V \quad (4\text{-}30)$$

$$\boldsymbol{V}_{dropb} = (54.54\angle -143°)(0.24 + j0.14) = 15.15\angle -112.74\, V \quad (4\text{-}31)$$

$$\boldsymbol{V}_{dropc} = (60.52\angle 91.92°)(0.24 + j0.14) = 16.82\angle 122.18\, V \quad (4\text{-}32)$$

- After the UCSC is in operation

$$\boldsymbol{V}_{dropa} = (55.86\angle 0°)(0.24 + j0.14) = 15.52\angle 30.26°\, V \quad (4\text{-}33)$$

$$\boldsymbol{V}_{dropb} = (55.99\angle -120°)(0.24 + j0.14) = 15.56\angle -89.74\, V \quad (4\text{-}34)$$

$$\boldsymbol{V}_{dropc} = (55.98\angle 120°)(0.24 + j0.14) = 15.55\angle 150.26\, V \quad (4\text{-}35)$$

The waveforms depicting the magnitudes of the positive-, negative- and zero-sequence components are depicted from Fig. 4-31 through Fig. 4-33, respectively. The symmetrical-component phasor values of the source currents are illustrated from Table 4-24 to Table 4-26.

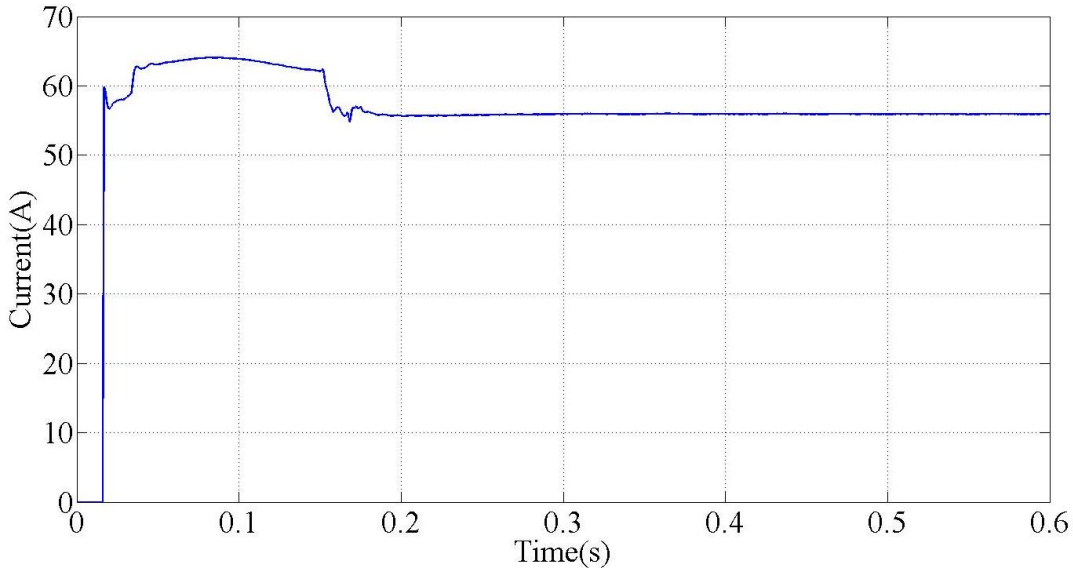

Fig. 4-31. Positive-sequence current magnitude at the source for case B

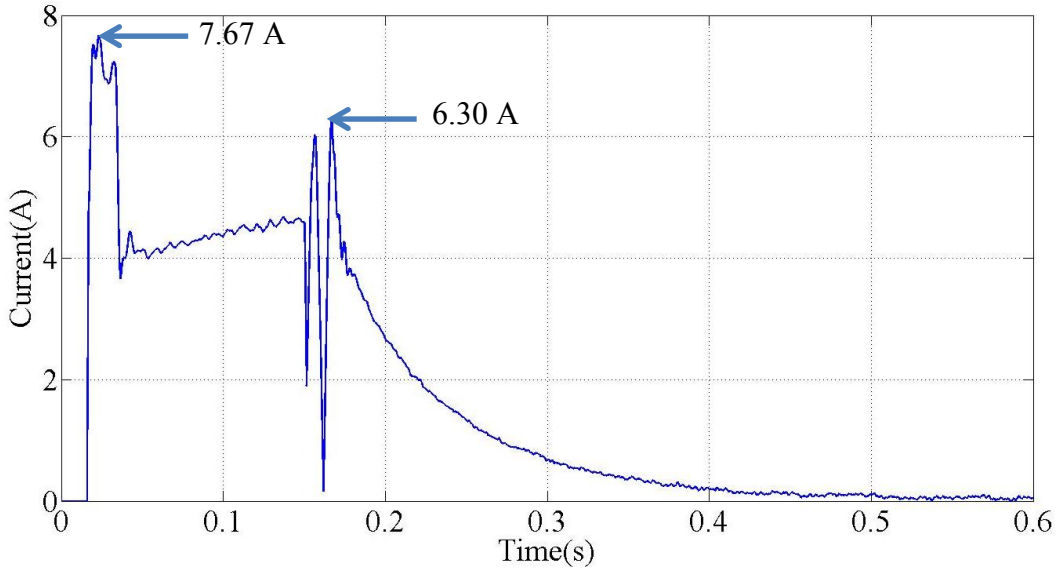

Fig. 4-32. Negative-sequence current magnitude at the source for case B

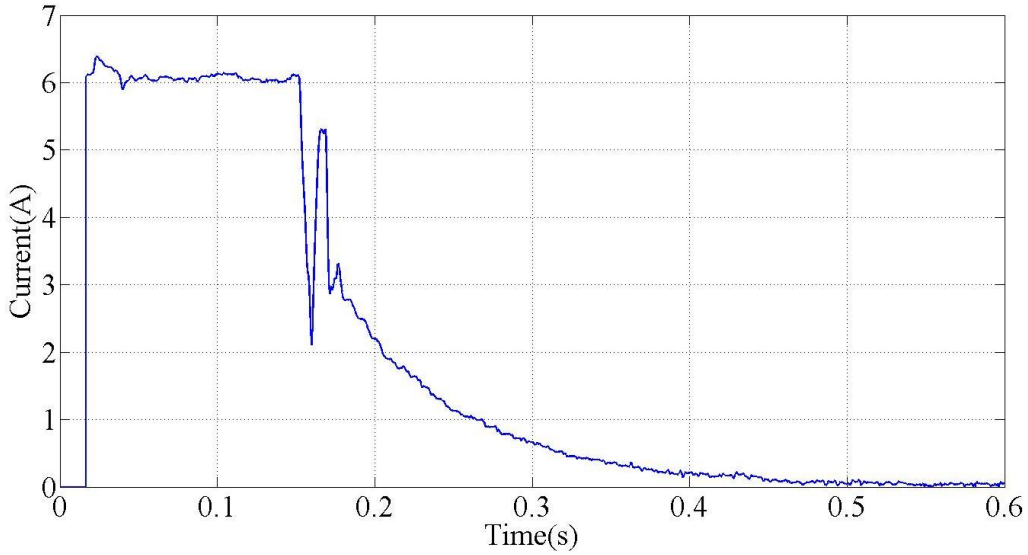

Fig. 4-33. Zero-sequence current magnitude at the source for case B

On Fig.4-32 two transients are illustrated. During interval I the transient reaches a value of 7.67 A and during interval II the transient reaches a value of 6.30 A. Both transients last 0.04 s

(2.4 cycles) and 0.02 s (1.2 cycles), respectively. The transient of Fig. 4-33 last 0.011 s (0.67 cycles).

Up to this point the following can be mentioned:

- once the UCSC system is operating, the currents at the source are balanced in magnitude and in phase with their associated voltages;

Table 4-24. Positive-sequence current phasor values at the source for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{62.10\angle -27.20^\circ}$ **A**	$\boldsymbol{I_1}$	$\mathbf{55.94\angle 0.1}$ **A**

Table 4-25. Negative-sequence current phasor values at the source for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.65\angle -74^\circ}$**A**	$\boldsymbol{I_2}$	$\mathbf{0.05\angle 131^\circ}$ **A**

Table 4-26. Zero-sequence current phasor values at the source for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.1\angle -25.20^\circ}$ **A**	$\boldsymbol{I_0}$	$\mathbf{0.06\angle 149}$ **A**

- the magnitude of the negative- and zero-sequence currents went from 4.65 A and 6.1 A to 0.05 A and 0.06 A, respectively. This means that UCSC system manage to decrease the negative- and zero-sequence current magnitudes 93 and 122 time respectively;
- the magnitudes of the negative- and zero-sequence currents at the source are below 1 A in 0.121 s (7.23 cycles) and 0.114 s (6.83 cycles), respectively;
- the voltage drop across each phase is equal once the UCSC is operating.

The phasor values, symmetrical components and waveforms of the load currents are illustrated in from Table 4-27 to Table 4-30 and Fig. 4-34, respectively.

Table. 4-27. Load current phasor values for case B

Variable	Value
$\boldsymbol{I_{la}}$	$\mathbf{71.55\angle -29.7°A}$
$\boldsymbol{I_{lb}}$	$\mathbf{54.46\angle -143°\ A}$
$\boldsymbol{I_{lc}}$	$\mathbf{60.48\angle 92°\ \ A}$

Table 4-28. Load positive-sequence current phasor values for case B

Before the UCSC is in operation		After the UCSC is in operation	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20°\ A}$	$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20°\ A}$

Table 4-29. Load negative-sequence phasor current values for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54°A}$	$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54°A}$

Table 4-30. Load zero-sequence current phasor values for case B

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32°\ A}$	$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32°\ A}$

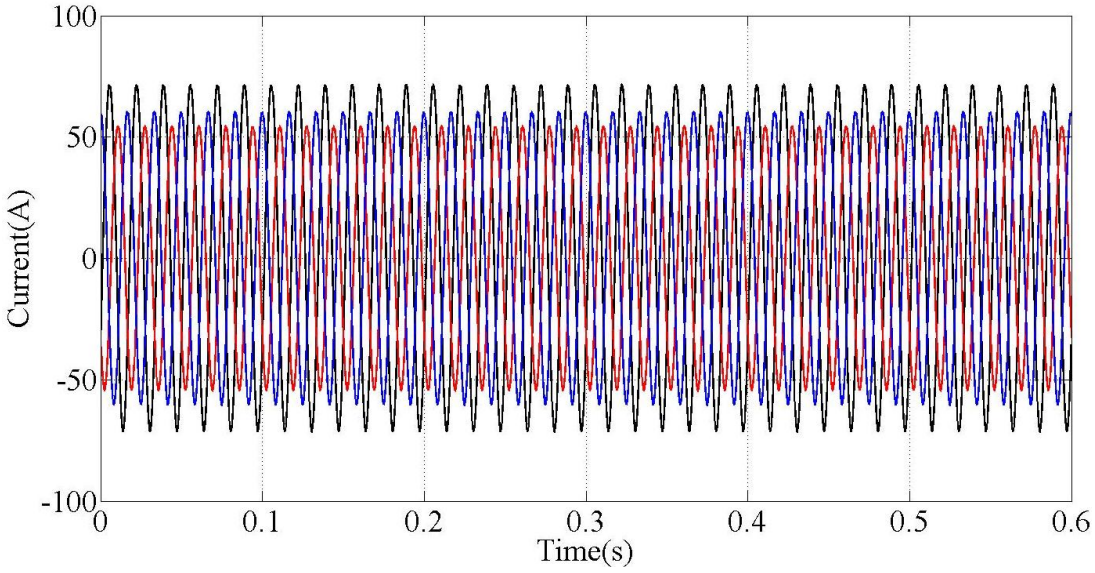

Fig. 4-34. Load current waveforms for case B

4.5 Case C – Capacitor-based DC Link Enhanced UCSC Controller

The first part of this section will illustrate the simulation procedure, parameters and MATLAB/SIMULINK™ models used for the simulation. The last part consists of an analysis of the results and conclusions.

- ***Simulation Procedure***

For case C, the conditions are the same as in case B but with two modifications added to the control algorithm:

- a pre-filter [2], [3] is added to the path of the *d*-axis reference current as illustrated in Fig. 4-35;
- a low-pass filter in the path of v_{DC} is added as illustrated in Fig. 4-36. The rest of the algorithm remains unchanged. The MATLAB/SIMULINK™ model is depicted in Fig. 4-37.

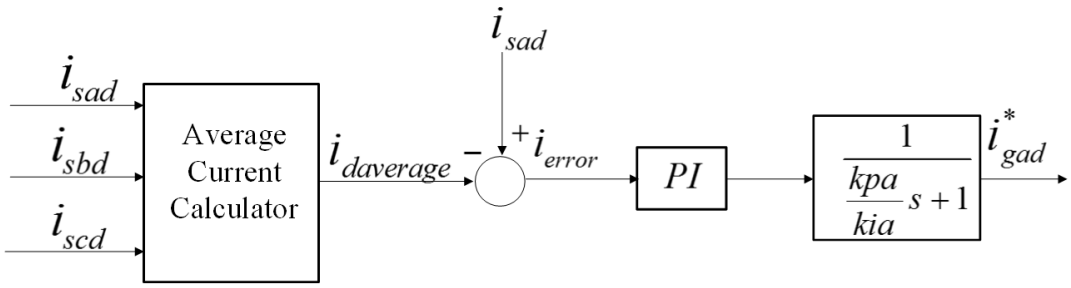

Fig. 4-35. Modified *d-axis* current generator algorithm

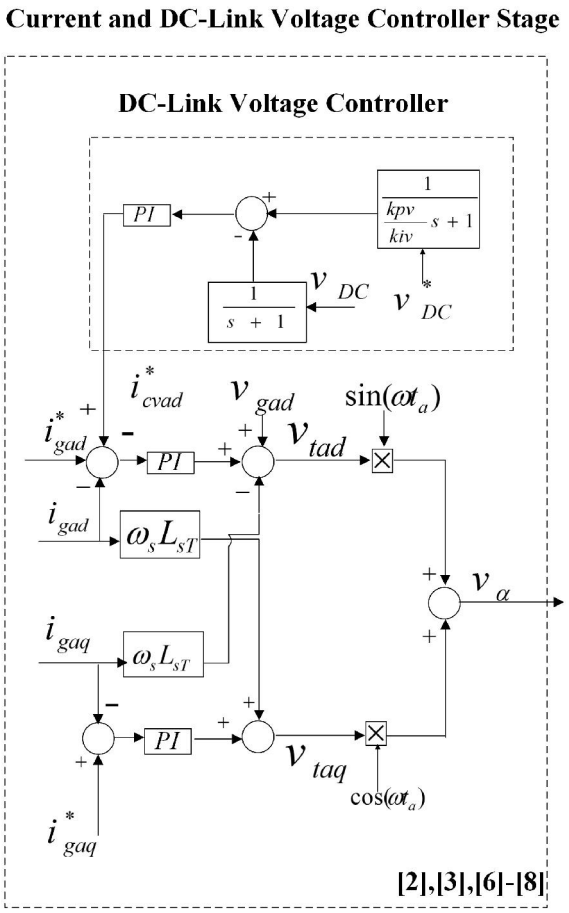

Fig. 4-36. Low-pass filters added to the DC-link voltage controller

- ***Simulation Parameters***

The parameters for this case remain the same as the parameters for case B. The load, UCSC and controller parameters are illustrated in Table 4-1, 4-2 and 4-17, respectively.

- ***Simulation Results and Analysis***

The DC-link voltage and the $d-q$ axes control current waveforms for this case are depicted in Fig. 4-38 and from Fig. 4-41 to Fig. 4-46, respectively. The compensating current phasors generated by the UCSC are presented in Fig. 4-47.

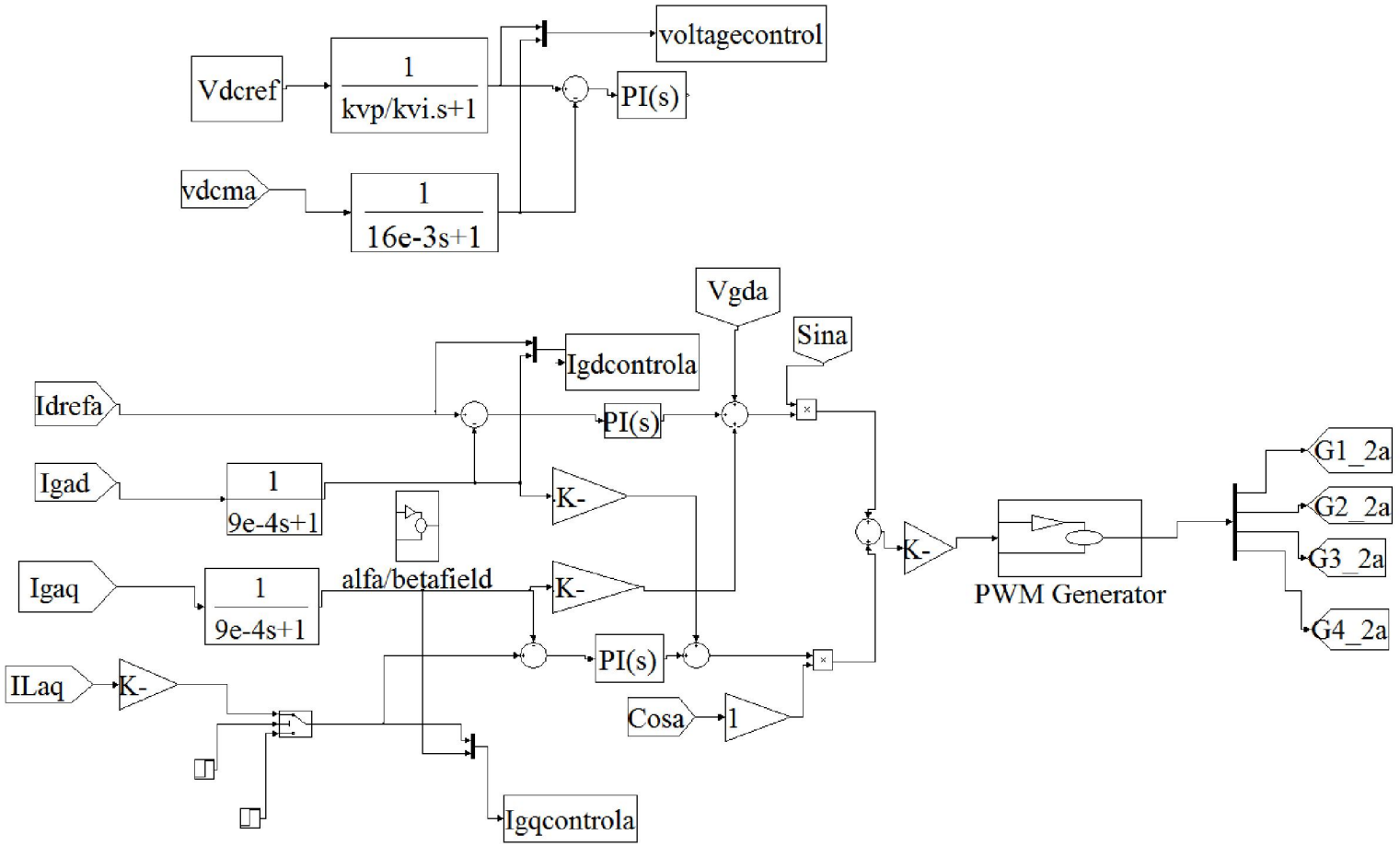

Fig. 4-37. UCSC control algorithm MATLAB/SIMULINK^{TM} mode for case C

In order to analyze the effect of the low-pass filter addition, the value of the ripple signal introduced into the UCSC control algorithm must be evaluated. The waveforms depicting the ripple signal with and without the filter are presented in Figs. 4-38 and 4-39, respectively.

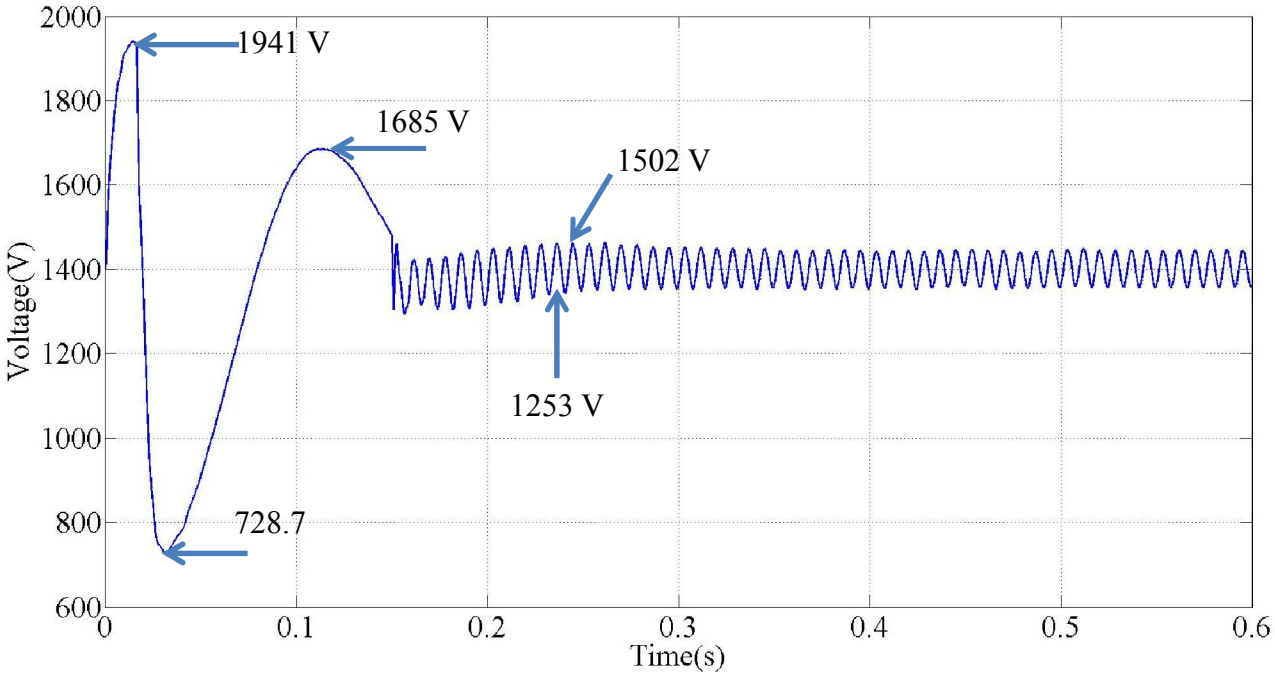

Fig. 4-38. DC-link voltage waveform for case C

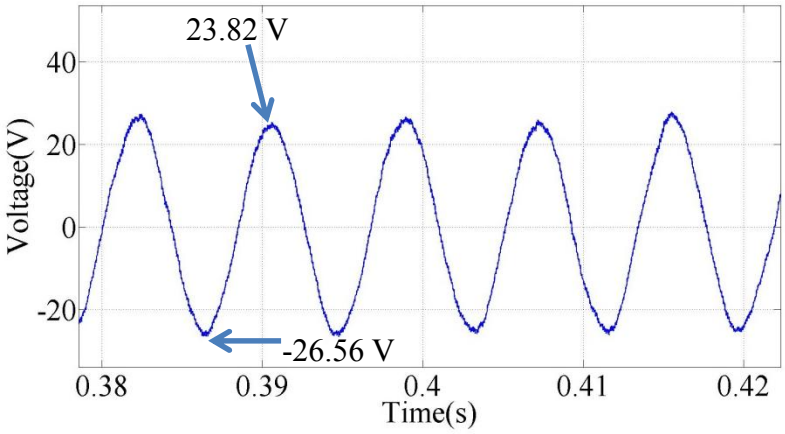

Fig. 4-39. Ripple signal without low-pass filter for case C

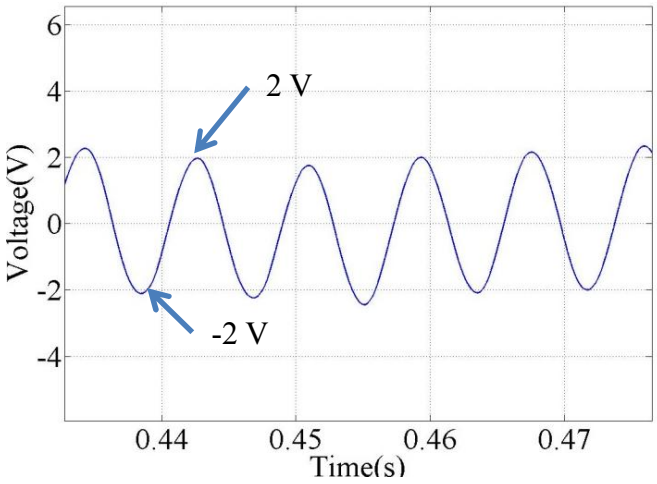

Fig. 4-40. Ripple signal with low-pass filter for case C

The results show that the addition of the low-pass filter attenuate the 40 V ripple depicted in Fig. 4-39 to a value of 2 V as illustrated in Fig. 4-40. This attenuation in the ripple signal translates into a reduction of the THD (%) for the UCSC currents as illustrated in Table 4-31. In chapter 3, the equation that was used to design the energy-storage capacitor had a target of 1% for the voltage ripple (14 V) but a value of 2.86% (40 V) was obtained through the simulation.

The $d-q$ axes current control waveforms illustrate overshoots and undershoots during intervals I and II of the simulations. The overshoot and undershoot of interval I are due the start of the system and the ones on interval II are generated when the UCSC starts compensating the source currents. The values are illustrated in Table 4-32.

Table 4-31. THD values for the UCSC phase *a* output current

Without low-pass filter		**With low-pass filter**	
Variable	**Value**	**Variable**	**Value**
%THD	**3.68**	**%THD**	**2.31**

Table 4-32. Case C undershoot, and overshoot values for the $\boldsymbol{d-q}$ axes control currents

Current	Undershoot (A)		Overshoot (A)	
	Interval I	Interval II	Interval I	Interval II
i_{gad}	**-635.5**	**-798.7**	**1179**	**544**
i_{gaq}	**-364**	**0**	**702**	**-2049**
i_{gbd}	**-948**	**574**	**1750**	**-504**
i_{gbq}	**-300**	**0**	**320**	**-1193**
i_{gcd}	**-670**	**643.4**	**1234**	**-257.8**
i_{gcq}	**-936.3**	**0**	**457**	**-1528**

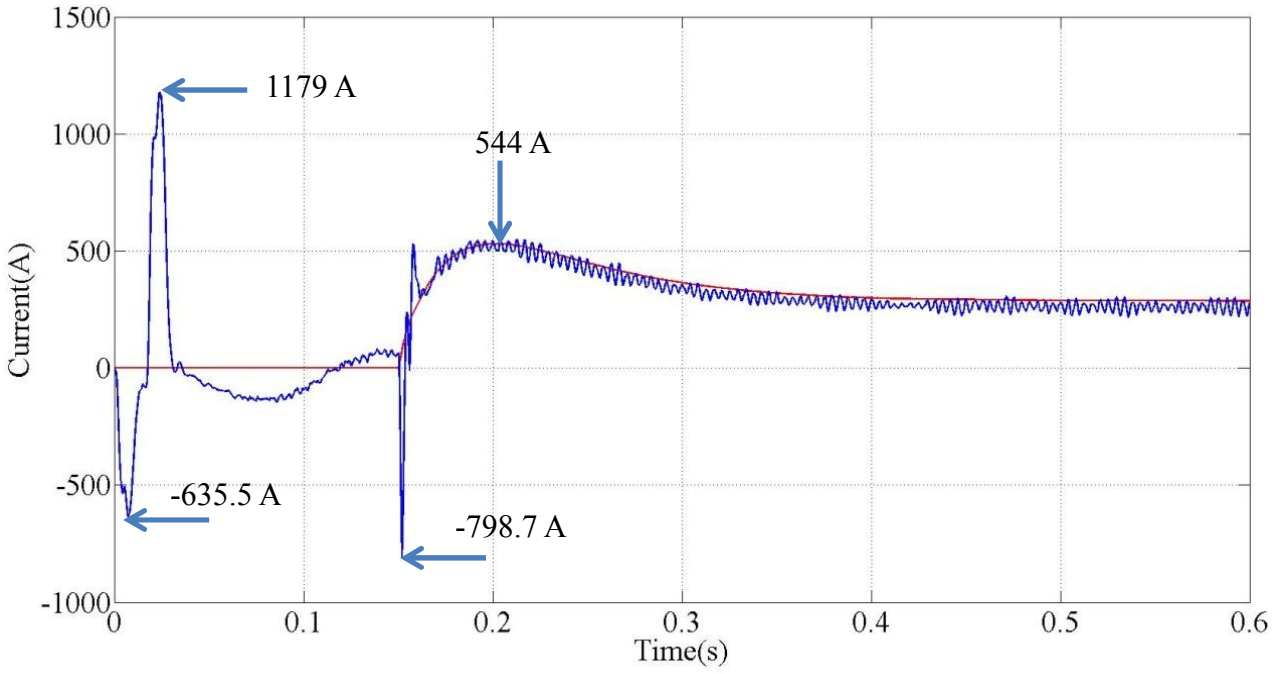

Fig. 4-41. Current i_{gad} and i_{gad}^{*}waveforms for case C

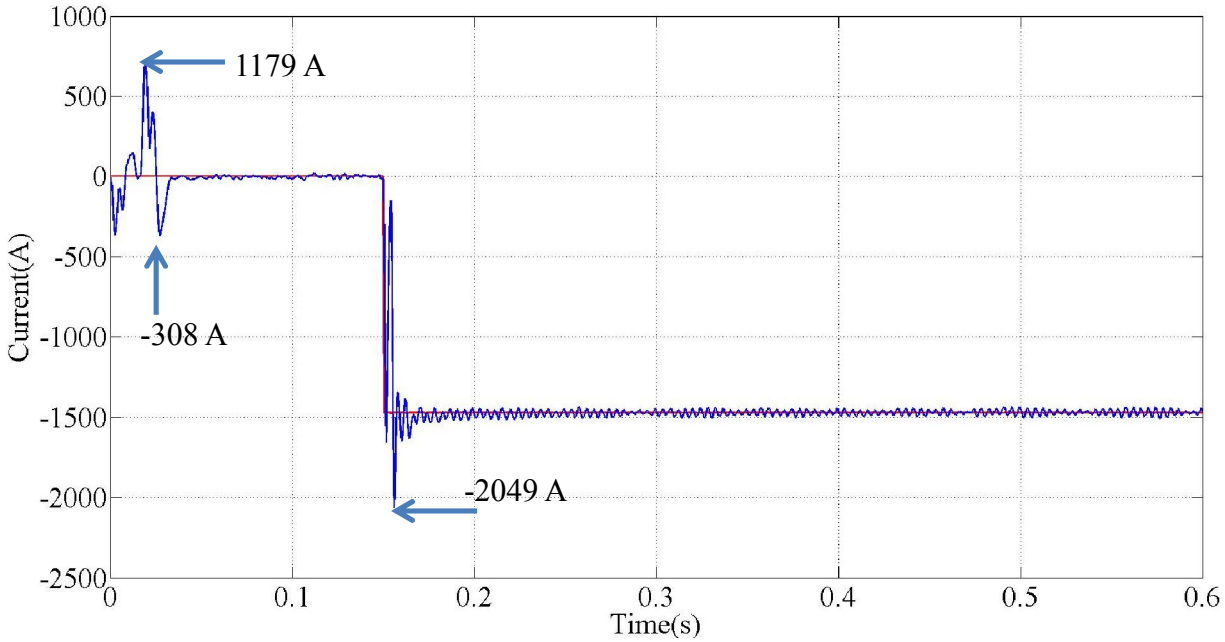

Fig. 4-42. Current i_{gaq} and i_{gaq}^{*}waveforms for case C

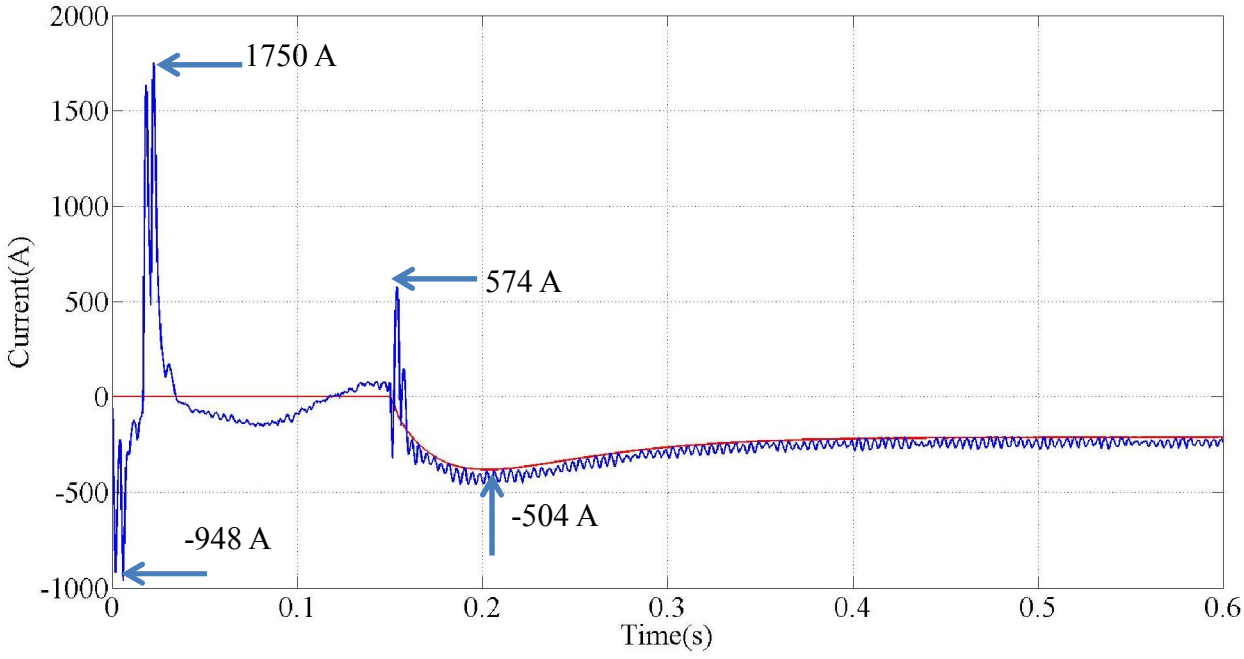

Fig. 4-43. Current i_{gbd} and i_{gbd}^{*}waveforms for case C

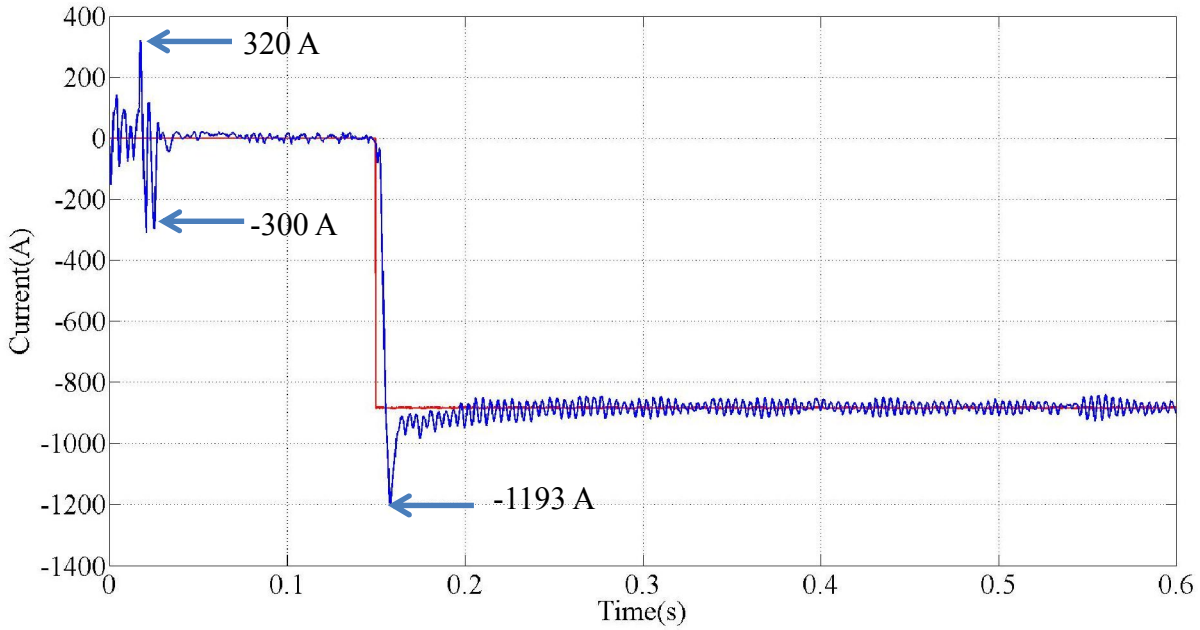

Fig. 4-44. Current i_{gbq} and i^*_{gbq}waveforms for case C

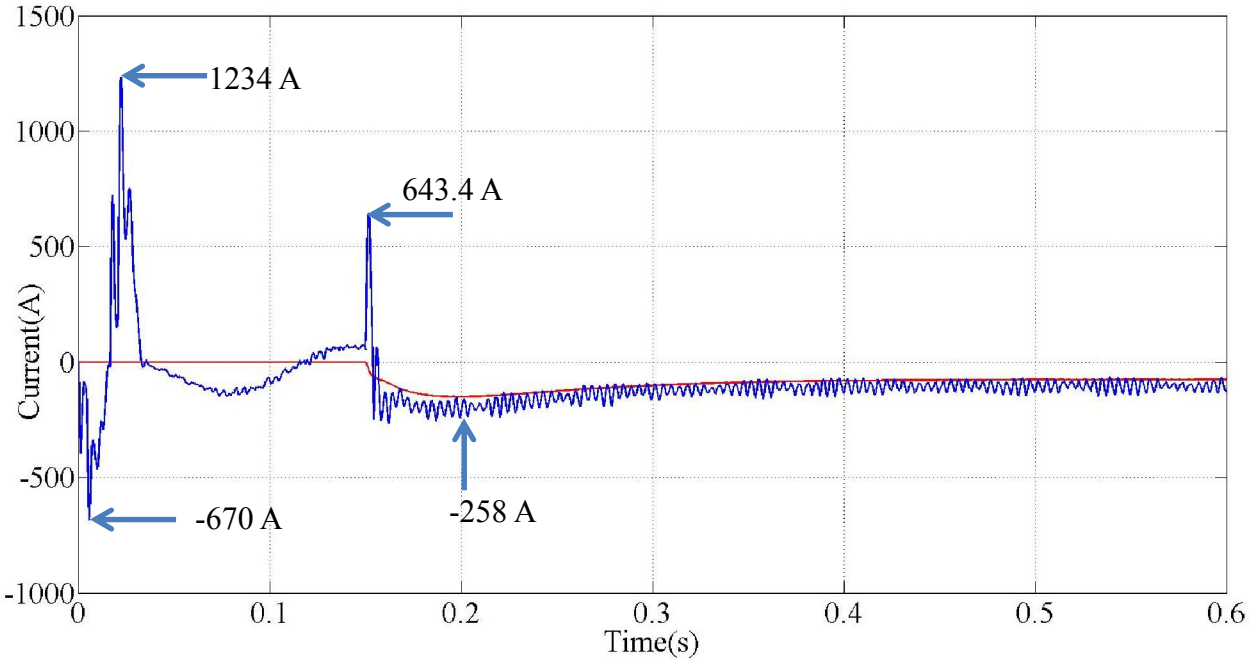

Fig. 4-45. Current i_{gcd} and i^*_{gcd}waveforms for case C

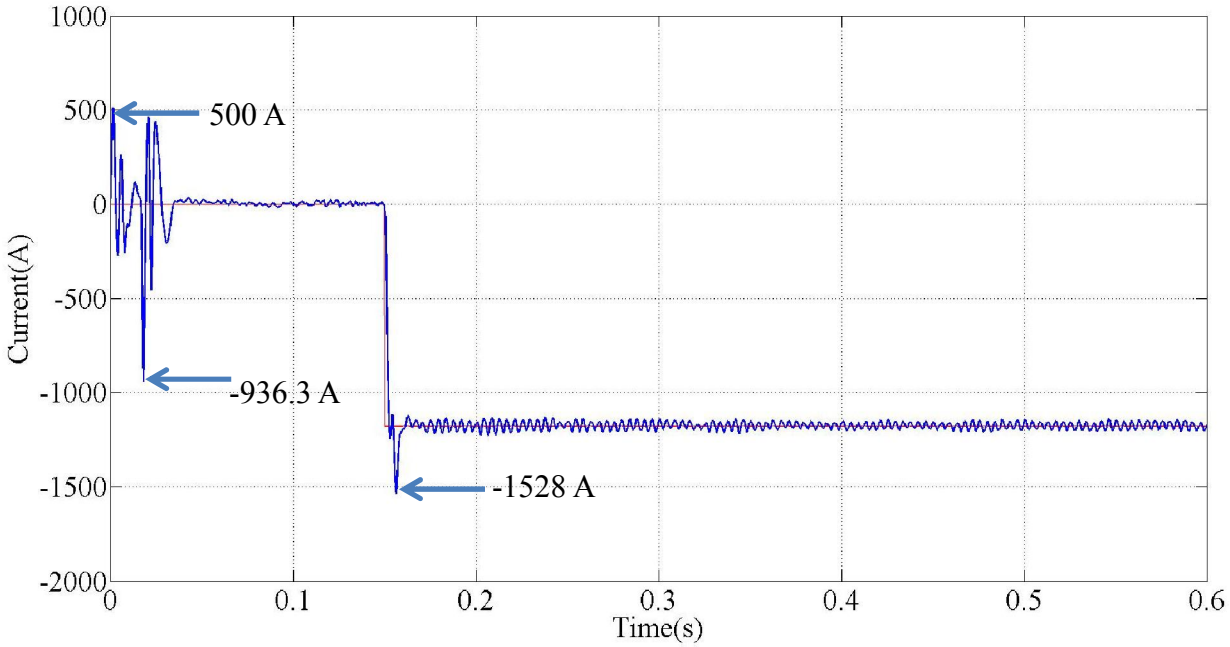

Fig. 4-46. Current i_{gcq} and i_{gcq}^{*} waveforms for case C

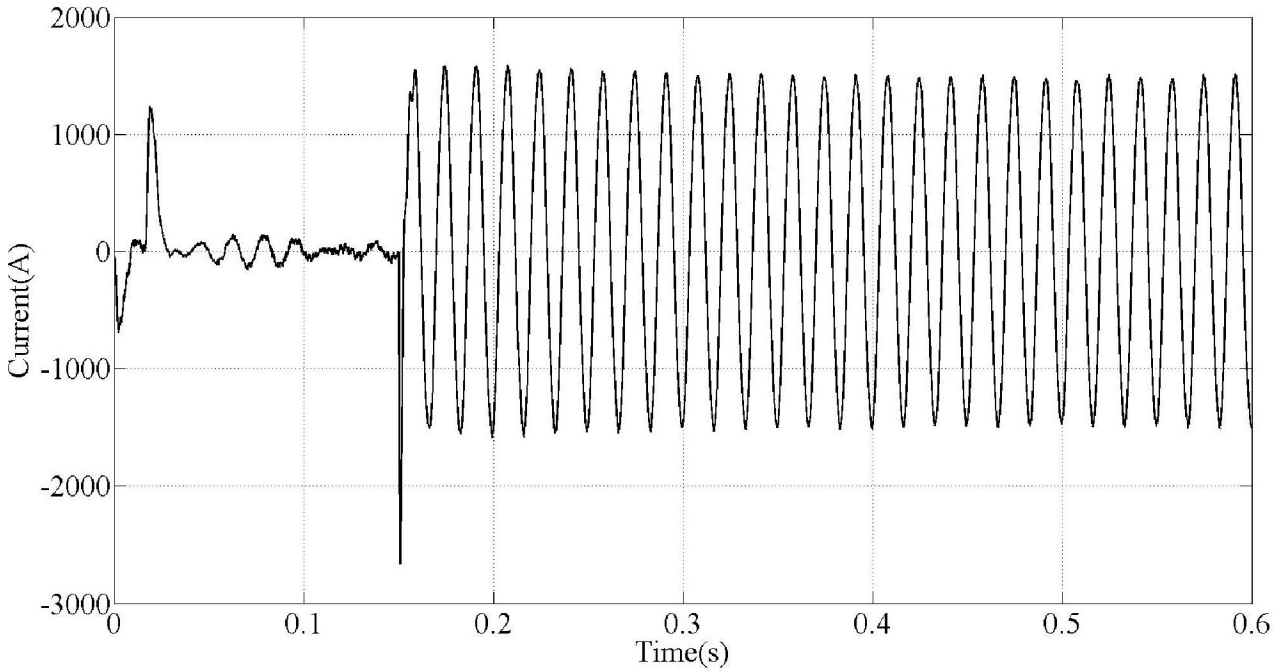

Fig. 4-47. UCSC phase *a* current waveforms for case C

The phasor values for $\boldsymbol{I_{ca}}$, $\boldsymbol{I_{cb}}$, $\boldsymbol{I_{cc}}$ and the symmetrical components for those currents are illustrated from Table 4-33 to Table 4-36.

Table 4-33. UCSC current phasor values for case C

Variable	Value
$\boldsymbol{I_{ca}}$	$\boldsymbol{35.98\angle -79.94°}$**A**
$\boldsymbol{I_{cb}}$	$\boldsymbol{21.97\angle 134.81°}$ **A**
$\boldsymbol{I_{cc}}$	$\boldsymbol{28.49\angle 24.84°}$ **A**

Table 4-34. UCSC positive-sequence current phasor values for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	**0 A**	$\boldsymbol{I_1}$	$\boldsymbol{28.34\angle -91.37°}$**A**

Table 4-35. UCSC negative-sequence current phasor values for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	**0 A**	$\boldsymbol{I_2}$	$\boldsymbol{4.69\angle -91.37°}$ **A**

Table 4-36. UCSC zero-sequence current phasor values for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	**0 A**	$\boldsymbol{I_0}$	$\boldsymbol{6.14\angle -25.31}$ **A**

The addition of the low-pass filter in Fig. 4-36 does not interfere with the objective of balancing the system as depicted in Table 4-37. The current difference between the phases is the following:

- the difference in magnitude between phases *a* and *b* went from 17.08 A to 0.04 A. This means that the current in phase *a* was 32 % higher than the current in phase *b*.
- For phases *b* and *c* the difference went from 6.03 A to 0.07 A. For this case the current in phase *c* was 11% higher than the current in phase *b*.
- Between phases *a* and *c* the difference in current magnitude decreased from 10.95 A to 0.12 A where the current in phase *a* was 19% higher than the current in phase *c*.
- The overall current unbalance % can be calculated as follows [1]:
  - Before the UCSC is in operation:

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 28.10\,\% \qquad (4\text{-}36)$$

  - After the UCSC is in operation

$$\%\, Unbalance = \frac{max\{|I_{sa} - I_{sb}|, |I_{sb} - I_{sc}|, |I_{sc} - I_{sa}|\}}{\frac{I_{sa} + I_{sb} + I_{sc}}{3}} \times 100 = 0.20\,\% \qquad (4\text{-}37)$$

The waveforms and the symmetrical components for the source currents are shown from Fig. 4-48 to Fig. 4-52 and the phasor values from Table 4-38 to Table 4-40.

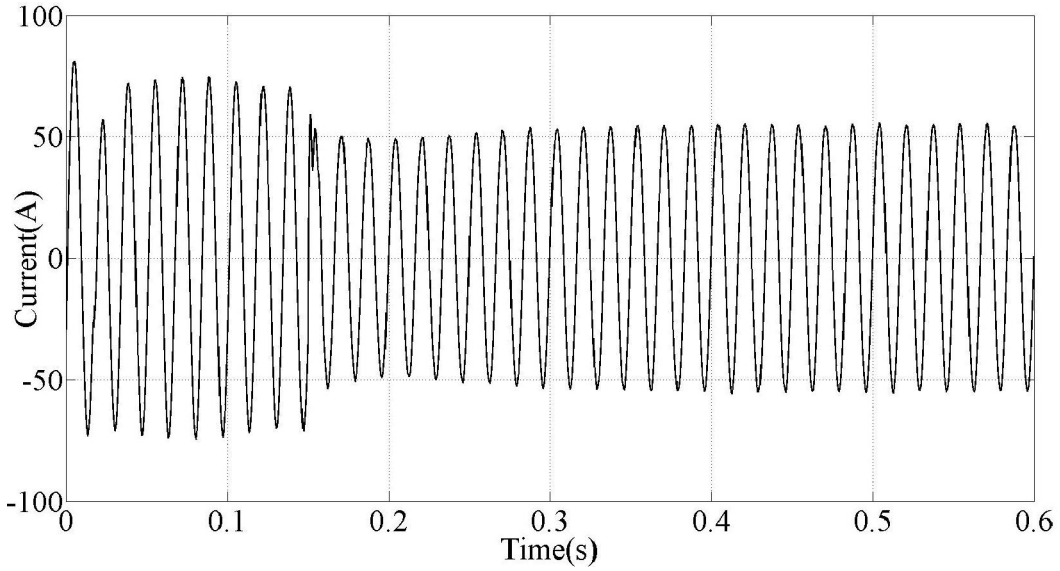

Fig. 4-48. Phase *a* source current waveform for case C

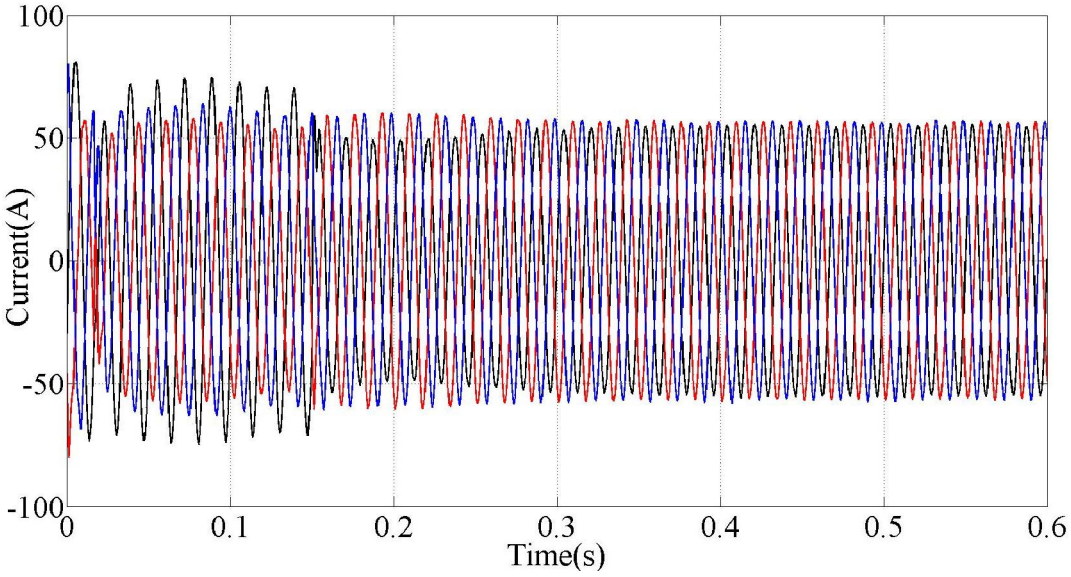

Fig. 4-49. Current waveforms at the source for case C

Table 4-37. Current phasor values at source for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_{sa}}$	$\mathbf{70.15\angle -30.35°}$ **A**	$\boldsymbol{I_{sa}}$	$\mathbf{55.85\angle 0}$ **A**
$\boldsymbol{I_{sb}}$	$\mathbf{53.07\angle -143°}$ **A**	$\boldsymbol{I_{sb}}$	$\mathbf{55.89\angle -120.10}$ **A**
$\boldsymbol{I_{sc}}$	$\mathbf{59.10\angle 91.5°}$ **A**	$\boldsymbol{I_{sc}}$	$\mathbf{55.96\angle 119.98}$ **A**

The differences in voltage drop along the impedance of segment 1 in an unbalanced and in a balanced case scenario are:

- Before the UCSC is in operation:

$$\boldsymbol{V}_{dropa} = (70.15\angle -30.35°)(0.24 + j0.14) = 19.49\angle -0.1\, V \quad (4\text{-}38)$$

$$\boldsymbol{V}_{dropb} = (53.07\angle -143°)(0.24 + j0.14) = 14.74\angle -112.74\, V \quad (4\text{-}39)$$

$$\boldsymbol{V}_{dropc} = (59.10\angle 91.5°)(0.24 + j0.14) = 16.42\angle 121.76\, V \quad (4\text{-}40)$$

- After the UCSC is in operation:

$$\boldsymbol{V}_{dropa} = (55.85\angle 0°)(0.24 + j0.14) = 15.52\angle 30.26°\, V \quad (4\text{-}41)$$

$$\boldsymbol{V}_{dropb} = (55.89\angle -143°)(0.24 + j0.14) = 15.53\angle -89.74\, V \quad (4\text{-}42)$$

$$\boldsymbol{V}_{dropc} = (55.96\angle 120°)(0.24 + j0.14) = 15.55\angle 150.26\, V \quad (4\text{-}43)$$

In Fig. 4-51, a transient of 0.04 s (2.4 cycles) where the highest current is 11.54 A is observed. This is due to the initial conditions of the system. The second transient due to the start of the UCSC system has a maximum current of 7.416 A and last 0.0171 s (1 cycle).

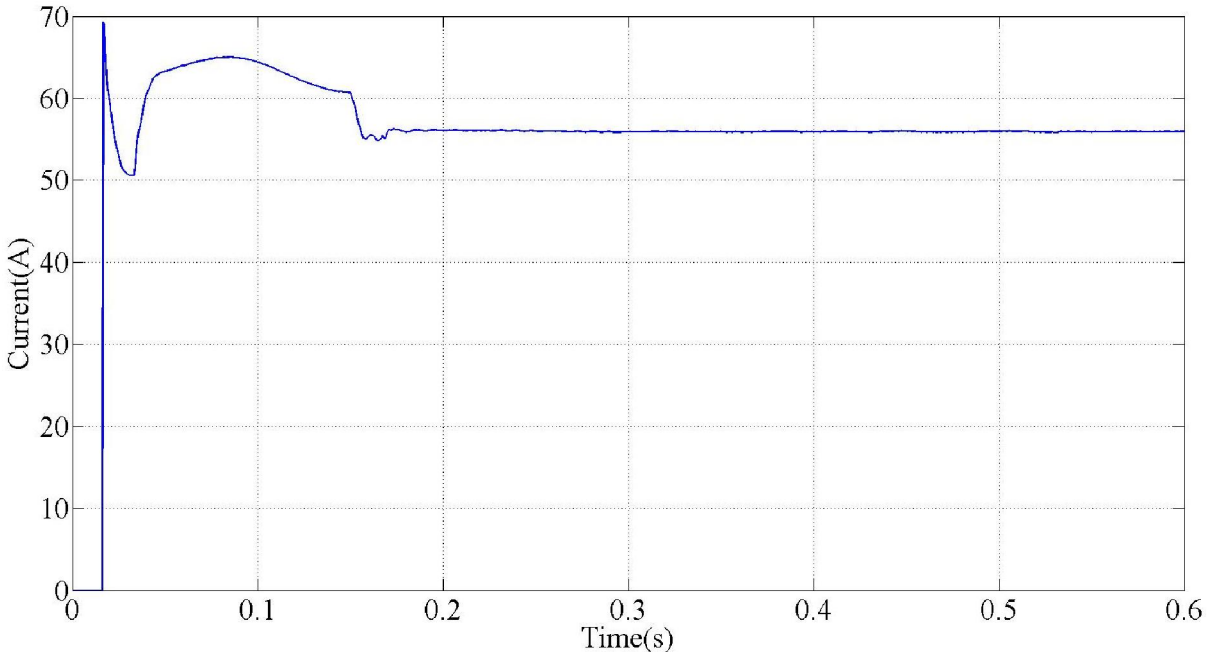

Fig. 4-50. Positive-sequence current magnitude at the source for case C

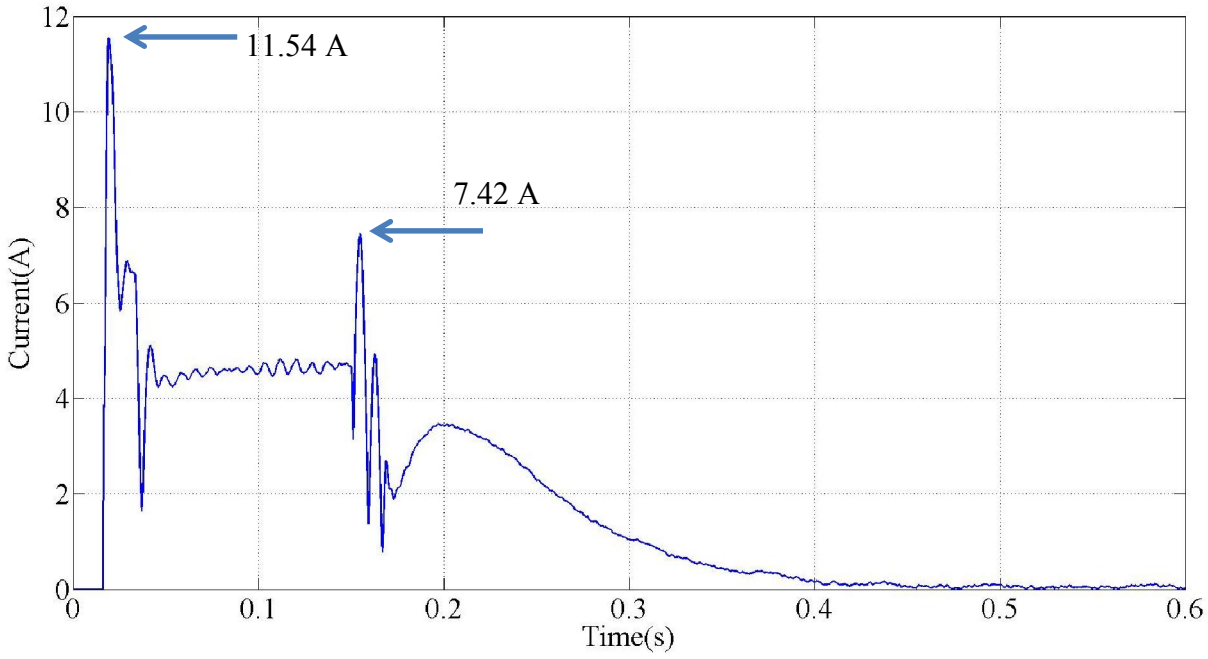

Fig. 4-51. Negative-sequence current magnitude at the source for case C

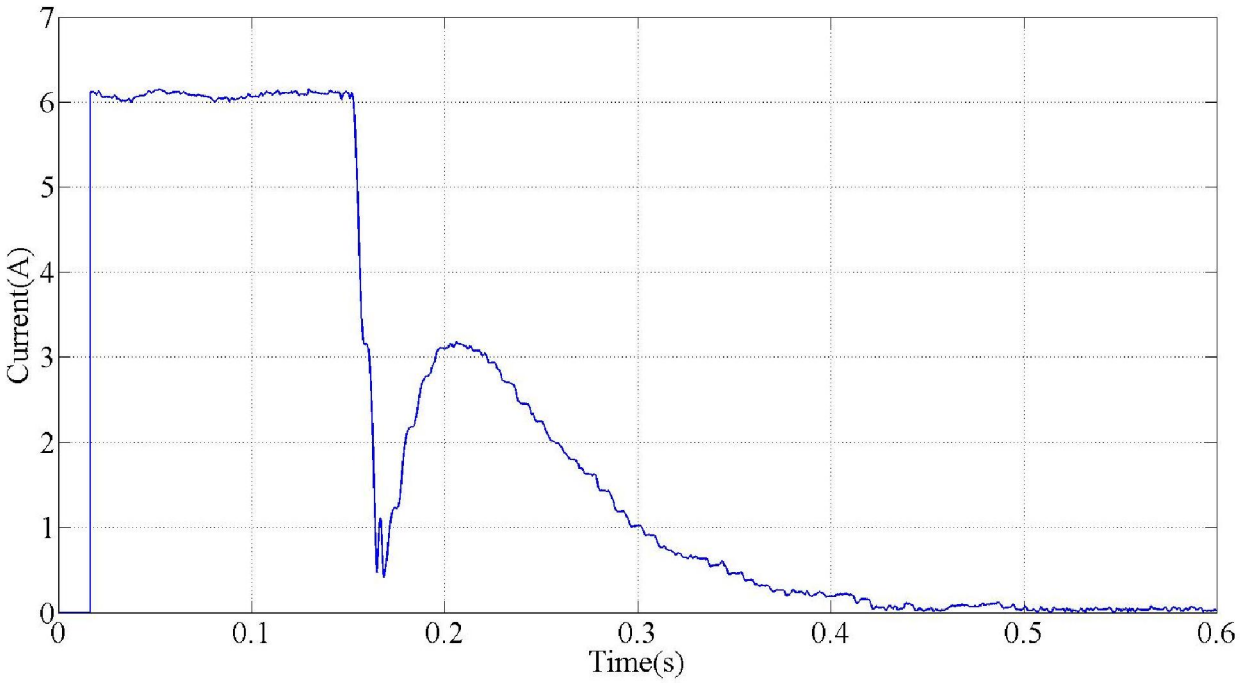

Fig. 4-52. Zero-sequence current magnitude at the source for case C

Table 4-38. Positive-sequence current phasor values at the source for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{60.7\angle -27.82^\circ}$ **A**	$\boldsymbol{I_1}$	$\mathbf{55.94\angle 0.1}$ **A**

Table 4-39. Negative-sequence current phasor values at the source for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.67\angle -73^\circ}$**A**	$\boldsymbol{I_2}$	$\mathbf{0.02\angle 43.02^\circ}$ **A**

Table 4-40. Zero-sequence current phasor values at the source for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.1\angle 1.54°\ A}$	$\boldsymbol{I_0}$	$\mathbf{0.02\angle -159.87\ A}$

Just like in case B, currents at the source are balanced in magnitude and in phase with their associated voltages. However, due to the addition of the low-pass filter and the pre-filter, the negative- and zero-sequence current go below 1 A in 0.227 s (13.61 cycles) and 0.221 s (13.25 cycles), respectively.

This makes for a difference of 0.106 s (6.36 cycles) and 0.107 s (6.42 cycles) between the overall controller response in case B and case C, where the algorithm of case B is faster but with 1.37 % more THD than the algorithm in case C. The magnitude of the negative- and zero-sequence currents went from 4.67 A and 6.1 A to 0.02 A and 0.02 A, respectively. It is worth mentioning that the large overshoot in the d-axis control currents at the moment when the UCSC is connected is reduced due to the addition of the pre-filter. For i_{gad}, the value gets reduced from 1376 A to 544 A. For i_{gbd}, the overshoot in the negative direction goes from -973.3 A to -459 A. For i_{gcd}, the overshoot goes from -470 A to -257.8 A. The waveforms and phasors for the load currents are illustrated in Fig. 4-53 and from Tables 4-41 to 4-44.

The voltage waveforms and phasor values at the PCC are illustrated in Fig. 4-54 and Table 4-45, respectively. The results indicate that the voltages remain balanced the entire time.

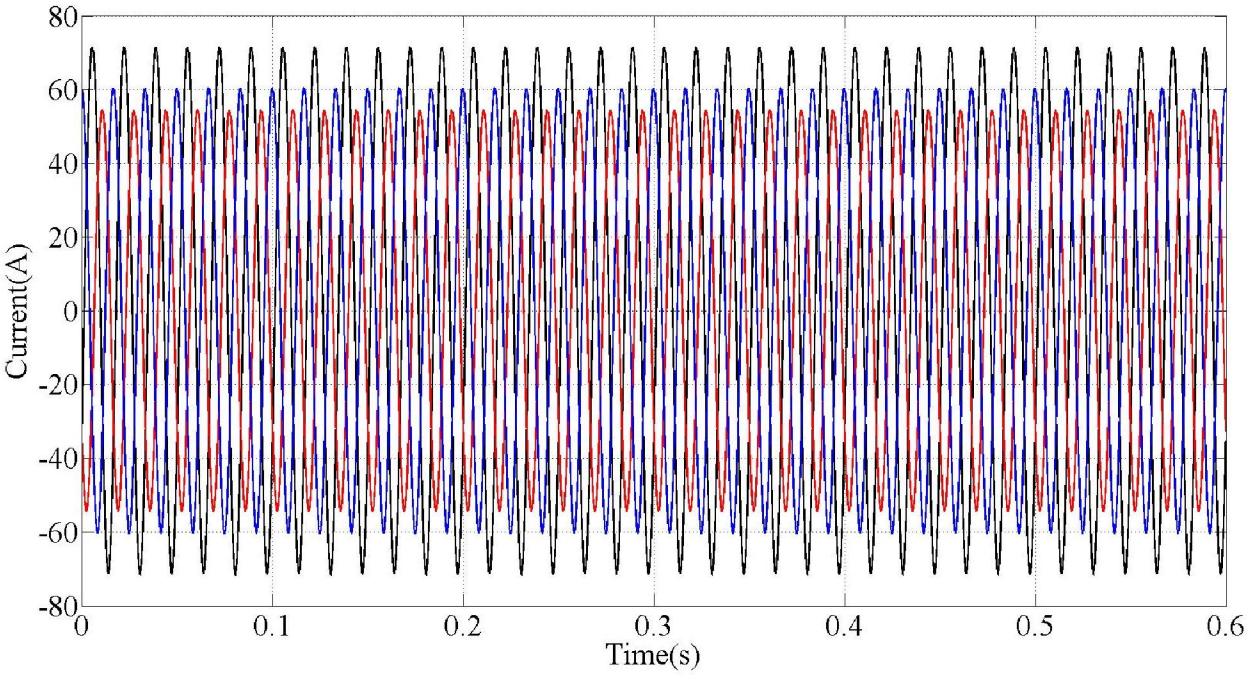

Fig. 4-53. Load current waveforms for case C

Table 4-41. Load current phasors values for case C

Variable	Value
$\boldsymbol{I_{la}}$	$\mathbf{71.55\angle -29.7°A}$
$\boldsymbol{I_{lb}}$	$\mathbf{54.46\angle -143°\ A}$
$\boldsymbol{I_{lc}}$	$\mathbf{60.48\angle 92°\ \ A}$

Table 4-42. Load positive-sequence current phasors values for case C

Before the UCSC is in operation		After the UCSC is in operation	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20°\ A}$	$\boldsymbol{I_1}$	$\mathbf{62.09\angle -27.20°\ A}$

Table 4-43. Load negative-sequence current phasors values for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54°A}$	$\boldsymbol{I_2}$	$\mathbf{4.7\angle -72.54°A}$

Table 4-44. Load zero-sequence current phasor values for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32\ A}$	$\boldsymbol{I_0}$	$\mathbf{6.07\angle -25.32\ A}$

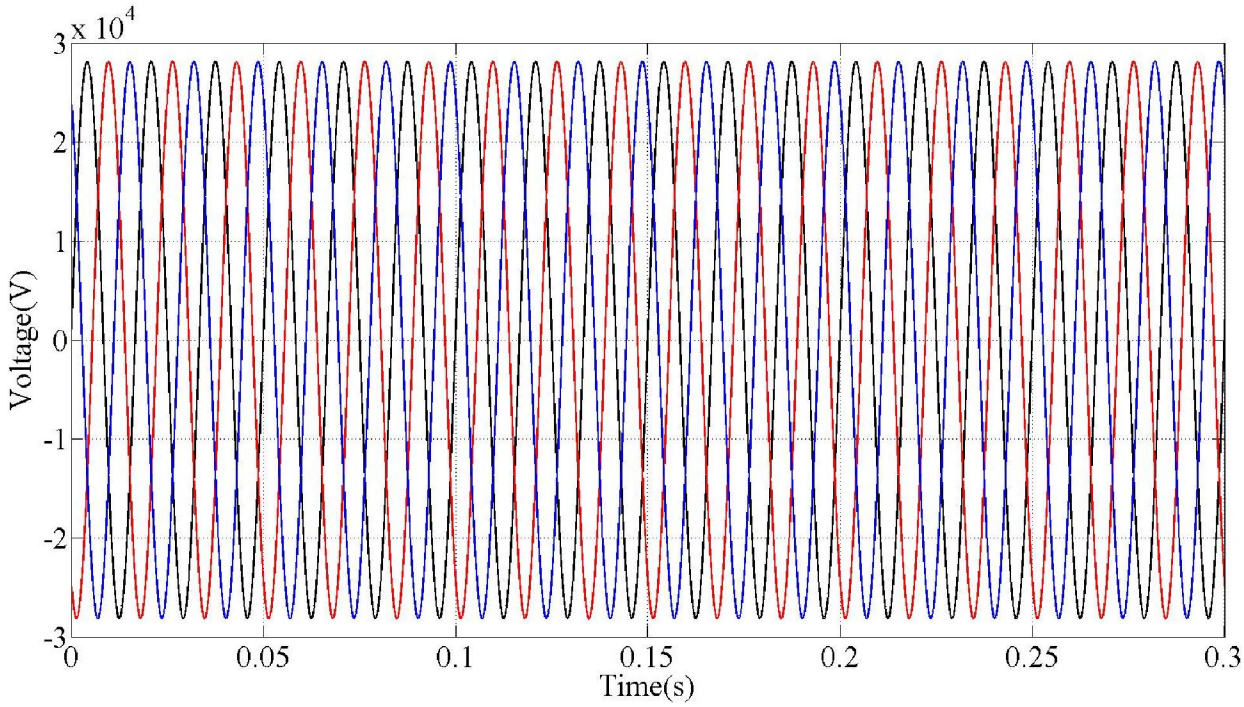

Fig. 4-54. Voltage waveforms at the PCC

Table 4-45. RMS voltage phasor values at PCC for case C

Before the UCSC is in operation		**After the UCSC is in operation**	
Variable	**Value**	**Variable**	**Value**
$\boldsymbol{V_{PCCa}}$	$\boldsymbol{28.16\angle 0\ kV}$	$\boldsymbol{V_{PCCa}}$	$\boldsymbol{28.16\angle 0\ kV}$
$\boldsymbol{V_{PCCb}}$	$\boldsymbol{28.16\angle -120\ kV}$	$\boldsymbol{V_{PCCb}}$	$\boldsymbol{28.16\angle -120\ kV}$
$\boldsymbol{V_{PCCc}}$	$\boldsymbol{28.16\angle 119.98\ kV}$	$\boldsymbol{V_{PCCc}}$	$\boldsymbol{28.16\angle 119.98\ kV}$

4.6 Conclusions

The MATLAB/SIMULINK™ simulations of the case study presented in chapter 3 were performed in section 4.2. Three different cases of the UCSC algorithm were presented in order to study the functionality of the UCSC algorithm. The simulation results were satisfactory for the all the cases in particular since, the algorithm was capable of driving the value for the negative-sequence current at the source below 1 A in 0.121 s (7.25 cycles) and 0.227 s (13.62 cycles) for the fastest and slowest responses, respectively. For the zero-sequence the values are 0.114 s (6.84 cycles) and 0.221 s (13.26 cycles) for the fastest and slowest responses.

Also, the system presented equal voltage drops in all phases from the source to the PCC. The unbalance of the source was reduced from 28% to 0.23% and 0.2% for cases B and C, respectively. For the load currents, the unbalance % remains the same since the load configuration stays the same.

The addition of a low-pass filter in the DC-link voltage controller in order to attenuate the ripple signal injected by the reference current generated by the DC-link voltage controller translated into an reduction of 1.37 % for the THD(%) at the phase *a* UCSC output current.

4.7 References

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CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.1 Conclusions

Two issues presented in chapter 1 generated by unbalanced loading of three-phase four-wire distribution systems are the negative- and the zero-sequence currents. Synchronous generators and induction motors connected to an unbalanced grid can be adversely affected by negative- and zero-sequence currents. For synchronous generators the main issues are [1], [2]:

- decrease in the efficiency;
- supersynchronous resonance in turbine blades of associated prime mover;
- subsynchronous resonance and damage to the rotor of motors.

For induction motors increased noise and uneven distribution of heat in the stator are two of the issues generated by unbalanced currents [3].

In chapter 2 concepts about power electronics were presented in order to establish the background for the UCSC system design. These concepts were applied to the development of the UCSC system that was presented in chapter 3 where the topology and the elements of the UCSC system were chosen. Also, the information presented in chapter 2 was used to design the UCSC control algorithm. The algorithm to control each converter is identical and it consists of three stages:

a) phase synchronization and reference current generator stage;

b) current and DC-link voltage controller stage;

c) PWM stage.

In chapter 4 three simulation cases were presented with their parameters and respective simulation procedures. The simulation results in chapter 4 demonstrated the functionality of the proposed UCSC topology and control algorithm. The main conclusions drawn from the simulation results are the following:

- With the application of the UCSC system to the case study of a simple 34.5 kV three-phase four-wire distribution system, the currents at the source are balanced in magnitude and in phase with their associated voltages.
- It was proved that the single-phase $\alpha - \beta / d - q$ transformation can be applied to three-phase systems in order to have independent control of single-phase converters
- The unbalance was reduced from 28% to 0.23% and 0.2% for cases B and C, respectively.
- The magnitudes of the negative- and zero-sequence currents were reduced from 4.65 A and 6.1 A to 0.05 A and 0.06 A, respectively, for case B. The reduction for the negative- and zero-sequence currents were from 4.67 A and 6.1 A to 0.04 A and 0.04 A, respectively, for case C. This reduction in the negative-sequence current can be translated into less losses in synchronous generator:

$$P_{losses1} = 4.65A \times {R_2}^2 \tag{5-1}$$

$$P_{losses2} = 0.05A \times {R_2}^2 \tag{5-2}$$

$$P_{losses1} = 4.65 \times \frac{P_{losses2}}{0.05} = 93P_{losses2} \tag{5-3}$$

where $P_{losses1}$, $P_{losses2}$ are the losses in the synchronous generator with and without the UCSC in operation, respectively. R_2 is the negative-sequence resistance. The same procedure can be applied to the values of case C.

- A voltage ripple is generated on the DC-link when the ideal DC source gets replaced by an electrolytic capacitor. This ripple voltage gets introduced in the current controller algorithm via the DC-link voltage controller.
- A low-pass filter was added to the path of the DC-link voltage feedback in order to attenuate the ripple signal and a reduction of 1.37 % in the output currents THD of the single-phase H-bridge converters was obtained.
- The THD (%) improvement comes with a trade-off in the UCSC control algorithm response. The model without the low-pass filter reduces the negative- and zero-sequence currents below 1 A in 0.121 s (7.3 cycles) and 0.114 s (6.84 cycles), respectively. The model with the low-pass filter performs the same function in 0.227 s (13.6 cycles) and 0.221 s (13.26 cycles), respectively.
- The THD % in the inverters output voltages were 3.36 %, 3.55% and 3.52% for phases *a*, *b*, and *c*, respectively. For the output currents, the values were 2.31%, 3.94% and 3.39% for phases *a*, *b*, and *c*, respectively. These values comply with the limits established by the IEEE 519 standard.

5.2 Recommendations for Future Work

The following are recommendations for future work:

- Addition of a control function to specify the power factor at the PCC.
- Addition of a control function to control the voltage level at the PCC.
- Application of the UCSC solution to a more complex three-phase four-wire distribution system.

- Additionally, the implementation of the UCSC control algorithm on three-phase inverters could be researched. Three topologies that could be studied are illustrated in Fig. 5-1, 5-2 and 5-3. The topology from Fig. 5-1 is used in [4] and was analyzed in chapter 1. It was concluded that the solution is only applicable to cases were only reactive current compensation is necessary in order to balance the currents at the source. The topology of Fig. 5-2 is presented in [5] and it's used for:
  - load sharing;
  - uninterruptible power supply.
- Besides researching the possibility of the application of the UCSC algorithm to three-phase converters, it is important to study the effects of generating unbalanced currents in the three-phase converters. A comparison between the proposed solution and the three-phase inverter with a mid-point connection in the dc link and the four-legged three-phase inverter should be performed.

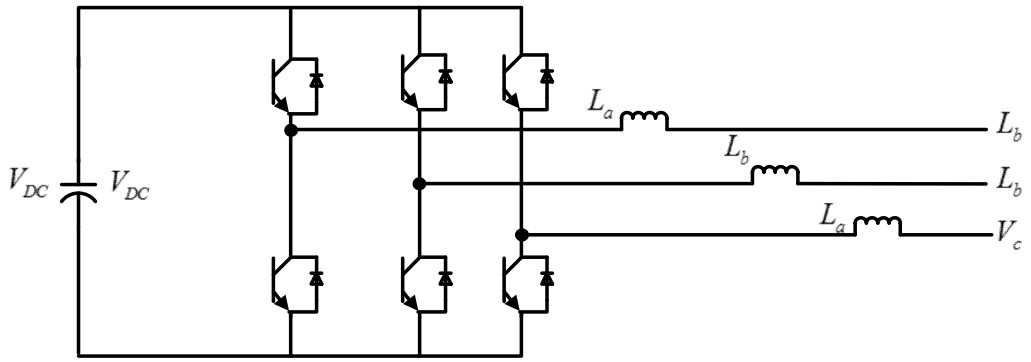

Fig. 5-1. Three-phase three-wire inverter topology

- The last recommendation is to build a prototype in order to validate the simulation results through experimental results.

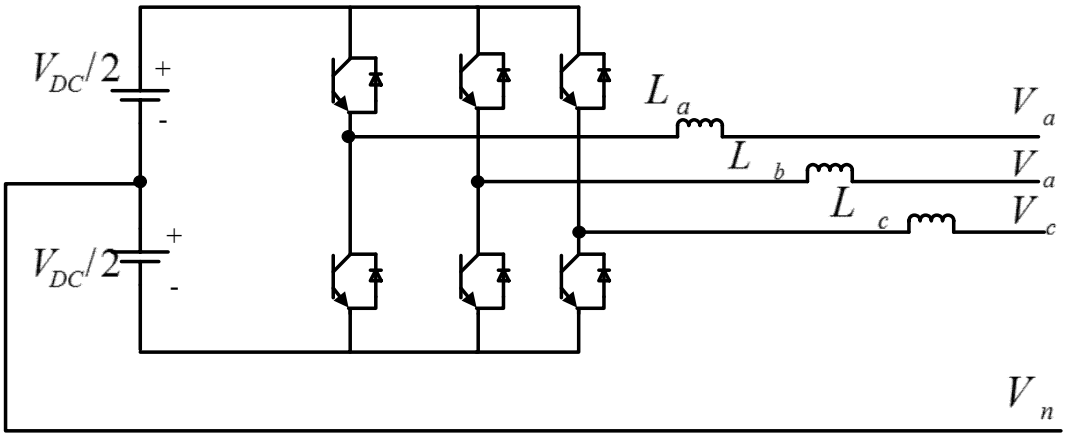

Fig. 5-2. Three-phase four-wire inverter topology

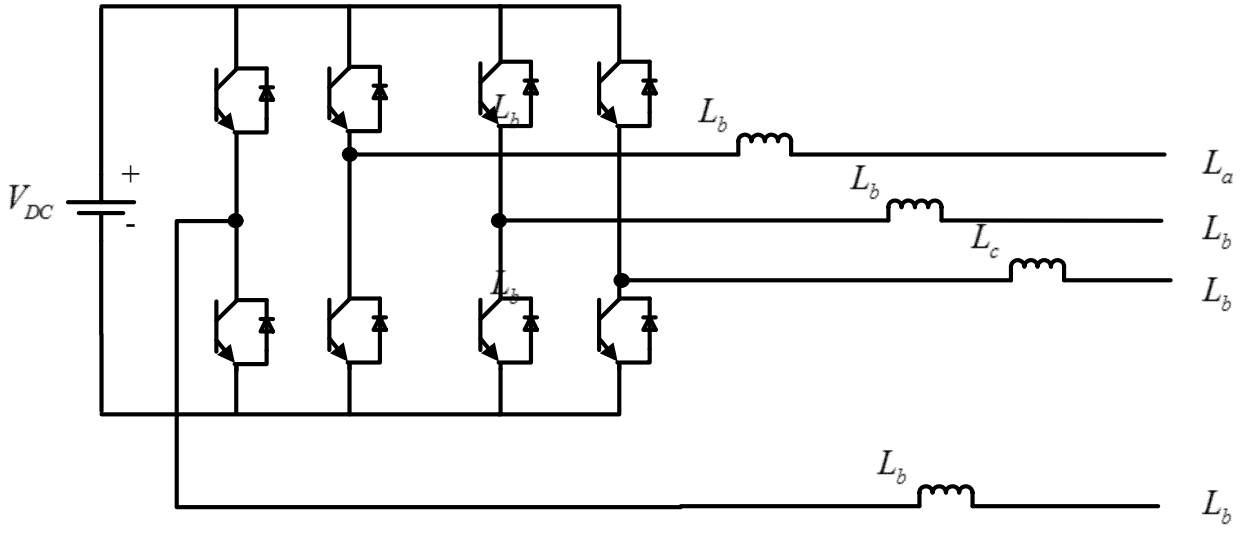

Fig. 5-3. Three-phase four-legs inverter topology [6]

5.3 References

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