2017 IEEE Applied Power Electronics Conference (APEC '17)

Design and Evaluation of a Reconfigurable Stacked Active Bridge dc/dc Converter for Efficient Wide Load-Range Operation

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***Abstract*— This paper presents the design and implementation of a large-step-down soft-switched dc-dc converter based on the active bridge technique which overcomes some of the limitations of the conventional Dual Active Bridge (DAB) converter. The topology comprises a double stacked-bridge inverter coupled to a reconfigurable rectifier through a special three-winding leakage transformer. This particular combination of stages enable the converter to run in an additional low-power mode that greatly increases light-load efficiency by reducing core loss and extending the zero-voltage switching (ZVS) range. The converter is implemented with a single compact magnetic component, providing power combining, voltage transformation, isolation, and energy transfer inductance. A 175 kHz, 300 W, 380 V to 12 V GaN-based prototype converter achieves 95.9% efficiency at full load, a peak efficiency of 97.0%, an efficiency above 92.7% down to 10% load and an efficiency above 79.8% down to 3.3% load.**

Keywords— dc/dc converter; dc distribution; dual active bridge; stacked bridge; high-efficiency; wide-load range; low power mode; 3-winding transformer

I. INTRODUCTION

There is a growing need for high-efficiency, large-step-down dc-dc converters as dc loads and distribution systems become more prevalent. Dc-dc converters allow for easier integration with dc systems such as solar panels, micro-grid interfaces, LED lighting, and electric vehicle battery systems [1-3]. In addition, they are also used in dc distribution systems for data centers, where a high voltage (e.g. 380 V) must be converted down to a much lower voltage (e.g. 12 V) to provide power to server racks. These converters must maintain high efficiency across a wide load range, as servers can often remain in low-current or idle states depending on computational demand.

High-voltage (here, hundreds of volts) large conversion-ratio converters required by these applications face several challenges, such as large device switching loss and magnetic core loss. Soft switching techniques such as zero-voltage switching (ZVS) or zero-current switching (ZCS) are often used to minimize switching losses. However, for many soft-switched converters, soft-switching can only be achieved under specific operating conditions, and the converters will lose soft-switching when operating outside of these conditions.

One popular topology for these applications is the Dual Active Bridge (DAB) converter, which consists of two phase-shifted bridges connected across a transformer and energy transfer inductance. The DAB is popular due to its ability to operate bi-directionally, its high power density, low component count, soft switching capability on input and output bridges, isolation, and high efficiency [4-5]. In addition, it can be operated at a fixed frequency under a simple phase-shift control scheme [4]. The DAB converter achieves very high efficiencies at high power where the converter achieves ZVS. However, core loss stays constant (for a given voltage conversion ratio) as power decreases, and the DAB can lose ZVS at low currents, or when the operating voltage ratio deviates substantially from the ideal transformation ratio as described in [5]. Many of these applications experience large input voltage or load variation, making it difficult to achieve ZVS over all desired operating conditions using the traditional DAB topology.

There has been a significant amount of work done to extend the soft-switching range of the DAB in order to increase efficiency at light-loads, including more complex control schemes, dead-time optimization, variable inductance or frequency techniques, and burst mode control; these are reviewed below.

A. Alternative Control Schemes

Standard phase shift control can result in high conduction and switching losses when operating away from nominal conditions [6]. There are various waveform shaping control methods (e.g., [6-8]) that involve generating three-level transformer voltages with arbitrary duty cycles; these are designed to reduce reactive power in the transformer and decrease switching loss. The control schemes can also introduce switching states where the inductor current is zero in order to achieve ZCS. However, these control schemes may not apply to the entire operating range. Additionally, though the soft-switching range is extended, it is often done through ZCS

The authors gratefully acknowledge sponsorship of this work by the MIT-SkTech Program and by the National Science Foundation under Award Number 1307699.

transitions, which eliminate overlap losses but not necessarily losses associated with the charging and discharging of device output capacitances. Finally, many of these control schemes are designed for full-bridge topologies, which may prevent the use of stacked-bridge architectures designed to reduce switch stress and allow for the use of lower-voltage rated devices with better switching performance.

B. Dead-time Control

As described in [9-10], the actual value of the switching dead-times can have a large impact on efficiency, especially at low loads or where the voltage transfer ratio is far from the nominal transformer turns ratio. This is because the dead-time can contribute to the total effective phase shift, and at low powers, can dramatically affect the actual output power delivered. Additionally, if the dead-time is longer than the amount of time required to charge or discharge the device output capacitances given the inductor current, the converter can experience additional losses due to body diode conduction or partial hard-switching due to switch drain-to-source resonant ring down. There are therefore several methods to adaptively control the dead-time as a function of output power, (e.g., [9-11]), but these increase control and sensing circuitry complexity.

C. Variable Inductance and Frequency Control

The leakage inductance value also heavily influences the DAB's ZVS capability, as achieving ZVS requires that the stored energy in the leakage inductance at the switching transition must be equal to or higher than the stored energy in the output parasitic capacitances of the devices being switched [12]. However, a high leakage inductance can have a higher RMS-to-average current ratio, resulting in higher conduction losses and lower efficiency at full load. Therefore, work has been done to try to vary the leakage inductance and current as a function of the load to allow the DAB converter to be optimized for high-efficiency at both full load and over a wide operation range [12].

Some methods involve physically reconfiguring the leakage inductance, which requires additional control and physical components [12-13], while other methods involve varying the frequency as a function of desired output power, so that lower frequencies are used at higher powers to reduce the required phase shift, and therefore RMS currents, while higher frequencies are used at lower powers to increase the required phase shift, and allow the inductor current to ramp up to a high enough value to achieve ZVS [12]. However, this makes it harder to optimize the magnetics and filter design [14].

D. Burst Control

Another method to increase the current at the switch transition at low powers is burst control. Here, the converter is turned on and off at a burst frequency that is much lower than the converter's switching frequency. Burst mode for the DAB converter is explored in [12] and [15]. Using burst mode, the converter is made to operate in its full-load condition during the on-time, so that the leakage inductor current is high enough to achieve ZVS, increasing the efficiency of the converter at light loads. However, there can be significant transient events when the converter turns on and off, and these transient waveforms can deviate substantially from the ideal operating waveforms. Additionally, at very low powers where the converter is only on for a small percentage of the burst period, these transients can represent a significant portion of the converter on time, resulting in decreased efficiency.

E. The Proposed Approach

This paper proposes a new converter topology that is optimized for efficiency both at high power as well as under light-load conditions, and as such is especially attractive for the 380 V to 12 V conversion required for data center applications. The topology presented here provides a number of benefits resulting from its stacked inverter design, reconfigurable rectifier, and compact single-core three-winding leakage transformer. These components also allow for operation in a low-power operating mode designed to increase light-load efficiency. Additionally, the converter prototypes presented here are all operated at a fixed dead-time, greatly simplifying the control (though more complex control techniques such as adaptive dead-time, variable-frequency operation, and burst-mode control could be applied if desired).

II. THEORY OF PROPOSED ARCHITECTURE

Fig. 1 shows a conventional single-phase DAB topology [4], which consists of two full bridges that are phase shifted from each other across a transformer with some leakage inductance, L. The phase shift ϕ is used to control output power, which can be expressed as:

$$P_{out} = \frac{V_p V_s N}{2\pi f_s L} \phi \left(1 - \frac{\phi}{\pi}\right) \quad (1)$$

where V_p is the effective primary voltage, V_s is the effective secondary voltage, N is the transformer turns ratio, f_s is the switching frequency in Hz, L is the primary-referred leakage inductance, and ϕ is the phase shift in radians.

A limitation of the traditional DAB is that it can lose ZVS in light-load conditions when the current is insufficient to provide the required voltage transitions given the device output capacitance [5]. The proposed topology, referred to here as the Double Stacked Active Bridge (DSAB) converter, addresses this limitation, and can achieve high efficiency over a wide power range because 1) its stacked inverter design allows for the use of lower-voltage rated devices that have lower device capacitance, allowing the converter to achieve ZVS at lower currents, and 2) the converter can operate in a low-power mode which both reduces core loss and further extends the ZVS range.

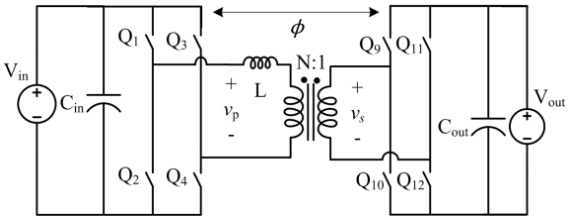


Fig. 1. A DAB converter with a full-bridge input and output. The two bridges are phase-shifted from each other across a transformer and an inductance, L.

The DSAB topology is shown in Fig. 2. It comprises a double stacked-bridge inverter coupled to a reconfigurable rectifier via a special three-winding leakage transformer, represented here by the model given in the dashed red box. Each stacked full-bridge inverter feeds into a primary winding. Both primary windings couple to a single secondary winding that feeds into a reconfigurable rectifier.

A. Double Stacked-Bridge Inverter

The converter uses "double stacking" of two stacked full-bridge inverters to achieve efficient high-voltage conversion. A double stacked inverter has multiple benefits: 1) it decreases the individual inverter device voltage ratings, providing improvements in overall device performance, and decreases energy stored in the device capacitance, making ZVS easier to achieve for lower inductor currents; and 2) having two stacked inverters (e.g., as a double stack) enables additional switching patterns for a low-power mode designed to increase light-load efficiency.

The decrease in inverter device rating can be seen by comparing Figs. 1-3. The devices Q_1-Q_4 in Fig. 1 must be rated for the full input voltage, V_{in}. For high voltage applications, this switch stress is very high and the conventional DAB suffers from losses due to poor switch characteristics. By comparison, Q_1-Q_4 for the single stacked-bridge inverter shown in Fig. 3 are rated for $V_{in}/2$, while Q_1-Q_8 for the proposed double-stacked topology in Fig. 2 are only rated for $V_{in}/4$. These lower-voltage rated devices can demonstrate much better switching performance due to lower parasitic resistance, capacitance, or both.

In order to evaluate the overall performance of a switch in this topology, the product $R_{ds,on}C_{oss}$ was chosen as a figure-of-merit for switching performance. This figure-of-merit precisely relates to the conduction loss in some high-frequency inverters, such as the classical Class E inverter [16], and is a useful qualitative metric for the ZVS bridge inverters and rectifiers considered here. It represents two main loss mechanisms in the proposed topology's switches: 1) a higher $R_{ds,on}$ results in higher conduction loss, and 2) higher C_{oss} results in more energy stored in the parasitic device output capacitances. For hard-switched applications, this means more power dissipated to charge and discharge C_{oss} during switch transitions. In soft-switched applications such as the DSAB, C_{oss} is charged and discharged inductively (i.e. some inductance resonating with the output capacitance), so this energy will not contribute to power loss in the switch. However, a higher C_{oss} will require a greater amount of current to complete the necessary voltage transitions on the output capacitance in the given dead-time. Therefore, switches with high C_{oss} can lose ZVS at higher output powers compared to switches with lower C_{oss}, due to the lower current available to charge and discharge this capacitance.

In addition, common device technologies in general can be said to experience an increase in the figure-of-merit $R_{ds,on}C_{oss}$ proportional to $BV_{DSS}{}^{k}$, where BV_{DSS} is the breakdown voltage of the device (which determines its voltage rating) and an exponent k, where $k>2$ [17]. As this relationship grows superlinearly, stacking more devices can still have lower loss

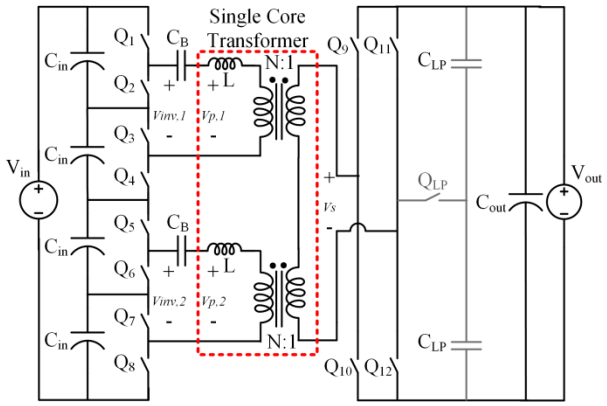


Fig. 2. The Double Stacked Active Bridge (DSAB) topology. The dashed red box contains an equivalent circuit model for the single magnetic component. Each of the stacked bridges feeds the primary winding of a single-core, three-winding transformer. An auxiliary switch, Q_{LP}, in the rectifier allows for a mode switch into a low power mode. A blocking cap, C_B, is used to remove the DC component in the square-wave output of each stacked-bridge. The total primary-referred leakage inductance is split between the two primaries (with L on each primary).

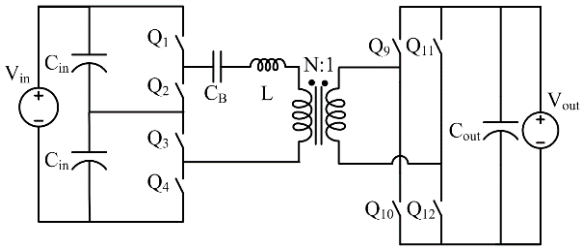


Fig. 3. A DAB convert with a stacked full-bridge on the input and a full-bridge on the output. A blocking cap, C_B, is used to remove the DC component in the square-wave output of the stacked-bridge.

associated with the switches due to the lower (and more favorable) figures-of-merit. Stacked topologies are especially attractive at higher input voltages, such as the 380 V application for which this converter is designed.

B. Single Magnetic Component

The transformer structure in the DSAB converter is a special three-winding transformer which provides power combining, voltage transformation, isolation, and energy transfer leakage inductance all in a single compact planar PCB magnetic structure. This three-winding, three-core-leg transformer has two primary windings, both of which are coupled to the same secondary winding. This can be physically realized in a single magnetic structure by winding each primary around the outer leg of an E-I core, and winding the secondary around the middle leg, as shown in Fig. 4. The transformer windings have a turns ratio of N_1: N_2: N_3 where $N_1 = N_2 = N$, and $N_3 = 1$.

A simplified magnetic circuit model neglecting reluctance paths outside the core is shown in Fig. 5. $N_1 i_1$ through $N_3 i_3$ represent the magnetomotive forces of each winding, while $\mathcal{R}_1$ through $\mathcal{R}_3$ represent the reluctances of the core for each leg. In the limit when the core reluctances are very small, we get the relation $Ni_1 = Ni_2 = i_3$, where $N_1 = N_2 = N$ and $N_3 = 1$. Analysis

of this simple magnetic circuit yields idealized voltage relations as follows:

$$\frac{v_1}{N_1}+\frac{v_2}{N_2}+\frac{v_3}{N_3}=\frac{v_p}{N}+\frac{v_p}{N}-\frac{v_s}{1}=0 \qquad (2)$$

where v_1 through v_3 and N_1 through N_3 are defined as in Fig. 5, v_p is the voltage on each primary winding, v_s is the voltage on the secondary winding, and N is the primary-secondary turns ratio as shown in Fig. 2. Equation (2) can be rearranged to arrive at the following relationship, which states that the secondary voltage is the sum of the two primary voltages, transformed by the turns-ratio N:

$$\frac{2v_p}{N}=v_s \rightarrow \frac{2v_p}{v_s}=N \qquad (3)$$

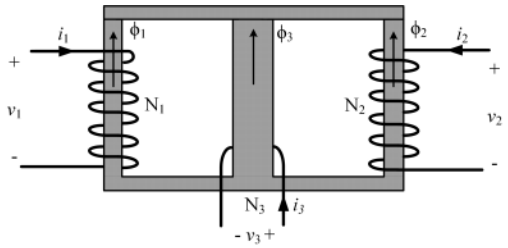


Fig. 4. A winding diagram of the three-winding transformer. The primary windings are wound around the outer legs (windings 1 and 2), while the secondary is wound around the middle leg (winding 3) of an E-I core. In standard operation, let $v_1 = v_2 = v_p$, $v_3 = -v_s$, $N_1 = N_2 = N$ and $N_3 = N$.

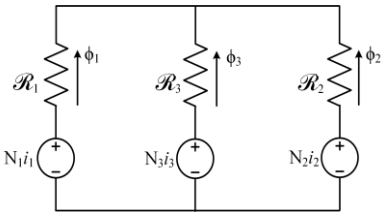


Fig. 5. A magnetic circuit model for the three-winding transformer. N_1i_1, N_2i_2, and N_3i_3 represent the magnetomotive forces of each winding, while $\mathcal{R}_1$, $\mathcal{R}_2$, and $\mathcal{R}_3$ represent the reluctances of the core for each leg.

The leakage inductance is also realized by the same physical structure, yielding an equivalent circuit model as shown in the dashed red box in Fig. 2. In this model, each primary winding is assigned an identical leakage inductance L. A more complicated model for multi-winding transformers could be used (e.g. see the cantilever model in [18]), but the symmetric topological structure and drive of this transformer make this model adequate for this analysis. The leakage inductance arises from the fact that a substantial portion of each primary winding lies outside the core, resulting in substantial fringing fields in that region. More details on physical implementation of this leakage inductance are provided in Section III.

C. Operating Modes

The DSAB converter can be operated in both a full-power mode (normal operation) and a low-power mode designed to decrease switching and core losses. The mode can be changed by adjusting the inverter and rectifier switching patterns and either opening or closing an auxiliary switch Q_{LP}, shown in Fig. 2.

1) Full-Power Mode

From (3), it is apparent that the effective primary voltage is the sum of the voltages applied to each primary winding. The effective secondary voltage is that applied by the rectifier. For an input V_{in}, each stacked full-bridge inverter output ($V_{inv,1}$ and $V_{inv,2}$ in Fig. 2, before the blocking capacitor C_B) will swing from 0 to $+V_{in}/2$, assuming the two bridges have evenly balanced input voltages. After the dc offset is removed by the blocking capacitor, the voltage on each primary will swing between $-V_{in}/4$ and $+V_{in}/4$, so that $v_p = V_{in}/4$. For a full-bridge rectifier, the ac voltage is a square wave of amplitude $v_s = V_{out}$. Therefore, under full-power mode operation with both stacked-bridge inverters operating in square-wave mode and the rectifier operating as a full-bridge rectifier, the output power characteristic is given by:

$$P_{out,FP}=\frac{\left(\frac{V_{in}}{4}+\frac{V_{in}}{4}\right)V_{out}N}{2\pi f_s(2L)}\phi\left(1-\frac{\phi}{\pi}\right) \qquad (4)$$

where $2L$ is the total primary-referred leakage inductance of the transformer as shown in Fig. 2, V_{in} is the dc input voltage, V_{out} is the dc output voltage, f_s is the switching frequency in Hz and ϕ is the phase shift between the inverter and rectifier in radians.

Fig. 6 shows the switching waveforms for the inverter gate drive signals $V_{gate1} - V_{gate8}$ for inverter devices $Q_1 - Q_8$, and the resulting primary waveforms V_{p1} and V_{p2}. Both primaries are energized with in-phase square waves of the same amplitude, and these individual primary waveforms are summed to produce an effective primary voltage of amplitude $V_{in}/2$. The dead-time between inverter switches is labeled dt_{inv}.

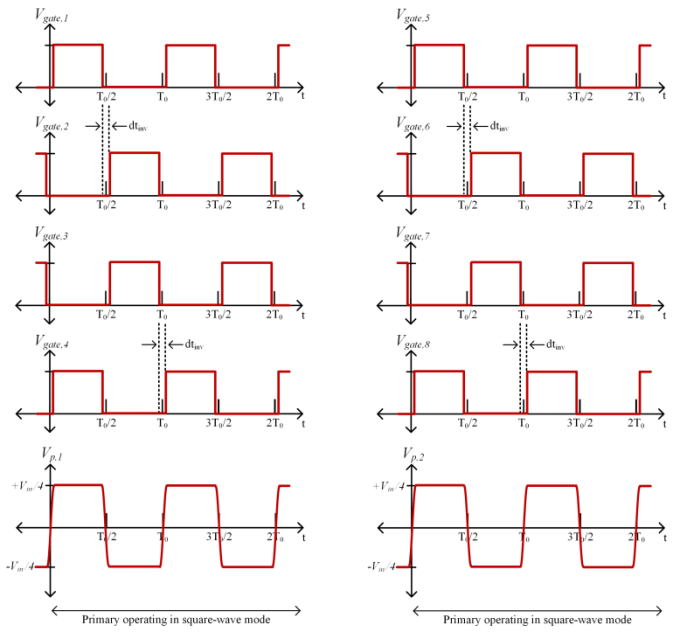


Fig. 6. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the full-power mode.

and is required to prevent shoot-through and allow time for ZVS transitions (i.e. for the voltage on the device capacitances to fully transition).

Fig. 7 (a) shows the full-power mode switching waveforms for the rectifier gate drive signals $V_{gate9} - V_{gate12}$ for rectifier devices $Q_9 - Q_{12}$. The rectifier is driven as a full-bridge, and the auxiliary switch Q_{LP} is held open ($V_{gate,QLP} = 0\ V$) during full-power mode operation. The rectifier waveforms are shifted from the inverter waveforms by a time t_{shift}, which is related to the phase shift by the expression $\phi = 2\pi t_{shift}/T_0$, where T_0 is the switching period. The dead-time between rectifier switches is labeled dt_{rect}, and also prevents shoot-through and allows for ZVS transitions.

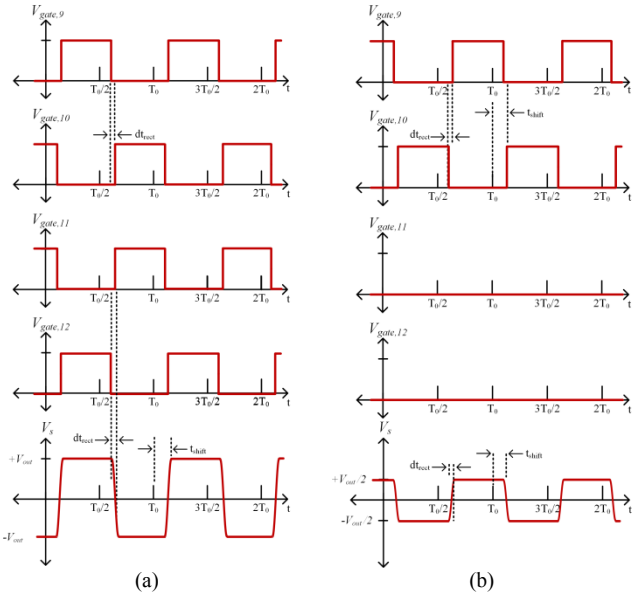


Fig. 7. Switching diagram for the rectifier secondary voltage, while the converter is operating in (a) full-power mode and (b) low-power mode.

2) Low-Power Mode

A challenge of the traditional DAB converter is that as the power decreases, so too does the current available to ensure ZVS transitions. The proposed converter can be configured in a low-power mode that takes advantage of the two-primary magnetic structure in order to energize the primaries in a different manner, which could not be achieved with a single inverter with one primary winding.

Power reduction is achieved by effectively halving the net voltages at the transformer primary and secondary. The inverter is configured to only energize one primary at a time while holding zero voltage on the other primary. To maintain charge balance on the input capacitors as well as to fully utilize the transformer core, the proposed control scheme alternates which primary is energized or shorted out (held at zero voltage) every other switching period, but this could be done on a longer time basis. To maintain a proper voltage transformation ratio, the rectifier is reconfigured to operate as a half bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP}.

Fig. 8 shows the low-power mode switching waveforms for the inverter gate drive signals $V_{gate1} - V_{gate8}$ for inverter devices $Q_1 - Q_8$. Primary voltage V_{p1} is shown being held at zero voltage for the first switching period. This is achieved by leaving Q_2 and Q_4 closed while Q_5-Q_8 are switched in a normal stacked full-bridge fashion. (Note, Q_1 and Q_3 could be held closed instead, which would simply result in a change in polarity of the primary voltage waveform). To hold zero voltage on the primary voltage V_{p2} during the second switching period, Q_6 and Q_8 are held closed while Q_1-Q_4 are switched. Since one primary is always held at zero, the total effective primary voltage is now half that of the full-power mode.

Fig. 7 (b) shows the low-power switching waveforms for the rectifier gate drive signals $V_{gate9} - V_{gate12}$ for rectifier devices $Q_9 - Q_{12}$. The rectifier is configured as a half-bridge rectifier by leaving Q_{11} and Q_{12} open and closing Q_{LP} ($V_{gate,QLP} = 5\ V$) so that the bottom terminal of the secondary winding is now connected to the midpoint of two series-connected capacitors, which are connected across the output so that each holds $V_{out}/2$. The rectifier ac voltage now swings from $-V_{out}/2$ to $+V_{out}/2$.

The inverter and rectifier voltages are therefore both halved as compared to the full-power mode, thereby maintaining the correct voltage transformation ratio. The new total effective primary to secondary voltage ratio is given by the following expression, which is equivalent to that given in (3):

$$\frac{v_p}{\frac{v_S}{2}} = N \tag{5}$$

As shown in (5), by shorting a primary winding of the transformer structure in the low-power mode, the total effective primary voltage is now v_p instead of $2v_p$. If the rectifier were not reconfigured as a half-bridge, the transformer voltage

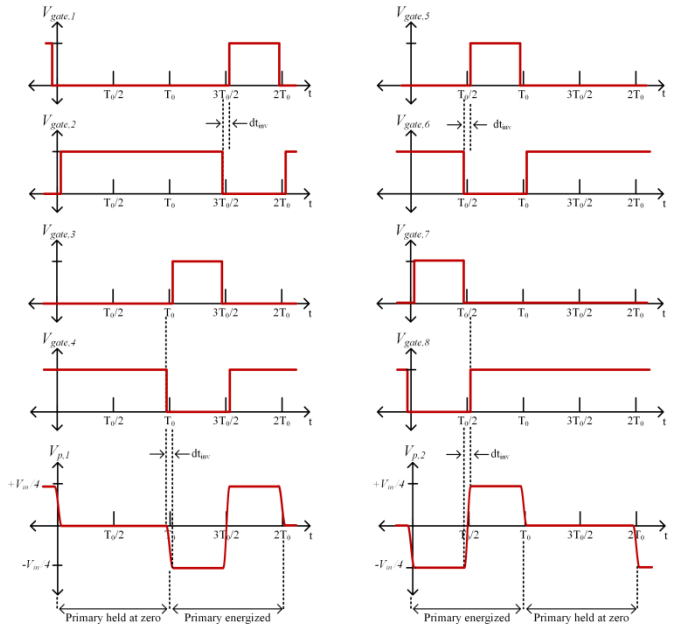


Fig. 8. Switching diagram for the inverter and primary winding voltages, while the converter is operating in the low-power mode.

transformation ratio would be $N = v_p/v_s$, rather than the full-power mode's $N = 2v_p/v_s$. The physical transformer turns ratio is designed to equal $2v_p/v_s$ for full-power operation. Without the reconfigurable rectifier, the DSAB converter operating in low-power mode would experience a large mismatch in its voltage transformation ratio, and would lose ZVS, as occurs in the traditional DAB topology.

The output power characteristic for the low-power mode can be found by substituting in the new values for the effective primary and secondary voltages, and is given by:

$$P_{out,LP} = \frac{\left(\frac{V_{in}}{4}+0\right)\left(\frac{V_{out}}{2}\right)N}{2\pi f_s(2L)}\phi\left(1-\frac{\phi}{\pi}\right) \quad (6)$$

As can be seen from (6), $P_{out,LP} = ¼P_{out,FP}$, so the converter in low-power mode naturally delivers a quarter of the normal mode power for a given phase shift $ø$.

a) Core Loss in the Low Power Mode

In the traditional DAB converter topology, core loss remains constant over the entire load range for a given voltage transformation ratio, and therefore accounts for a substantial portion of total loss at low loads. The low-power mode proposed here decreases core loss by only energizing one primary at a time. This also results in reduced flux density in the center leg of the core, due to the single-primary drive of the low-power mode.

A magnetic circuit model for the transformer operating in the low-power mode is given in Fig. 9. For simplicity, the leakage flux outside of the core is ignored. This circuit model represents the case where primary winding 2 is shorted. The winding will therefore carry whatever current is necessary to keep flux from flowing through it. This ideally results in an effective open circuit in the flux path. Nonidealities, such as winding resistance, will appear as a large transference (the magnetic circuit analog of inductance) in the magnetic circuit model [19].

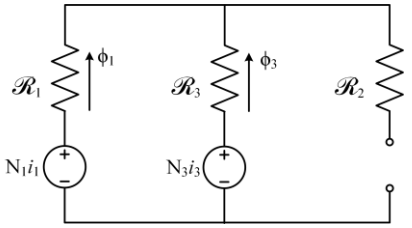
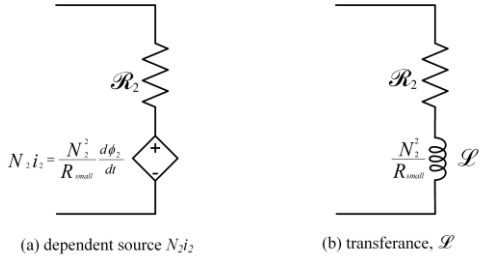


Fig. 9. Simplified magnetic circuit model for the three-winding transformer operating in the low-power mode, for the case when primary winding 2 is held at zero voltage by shorting it.



(a) dependent source N_2i_2 (b) transferance, $\mathscr{L}$

Fig. 10. (a) A model of the shorted winding, represented as a dependent source that produces a current i_2 to effectively cancel all flux in that leg. Nonidealities such as path resistance are represented by some small resistance R_{small}. (b) Equivalent transferance model for the shorted winding, modeling it with some transferance $\mathscr{L} = \frac{N_2^2}{R_{small}}$.

Fig. 10 shows a more detailed model of the open-circuited flux path in Fig. 9. While the total flux through winding 2 is zero, there is a current N_2i_2. However, the shorted winding acts as a dependent source that generates the necessary current to cancel the flux flowing through its corresponding core leg, as shown in Fig. 10 (a). Assuming some small resistance R_{small} in the flux path, this can be modeled by some transference $\mathscr{L} = N_2^2/R_{small}$. The shorted winding can be treated as providing an open-circuit to the flux path for purposes of simplified modeling, and therefore yields zero voltage on the winding.

b) Switching Loss in the Low Power Mode

The low-power mode naturally increases the converter currents for a given output power, thereby extending the range of powers for which ZVS is achieved and increasing efficiency at light-loads. Additionally, as can be seen by comparing Figs. 6 and 8, the low-power mode has fewer switching transitions on the inverter, which can further reduce switching losses at very low powers where ZVS is not possible (as hard-switching losses are proportional to CV^2f). Furthermore, rectifier gating losses can be reduced because only one half-bridge is operated. Because relatively low power is delivered in this mode, conduction losses are also not severe.

III. Experimental Validation

To illustrate the value of the proposed approach, we present results from multiple converters, all using the same core and PCB windings and designed for a nominal operating point of 380 V input, 12 V output at 300 W and operating at 175 kHz. The three prototypes each have a different inverter stage, to allow for comparisons between device technology as well as between a single-stacked inverter design and a double-stacked inverter design. These variations are: 1) the proposed double-stacked topology with 200 V EPC GaN devices; 2) the proposed double-stacked topology with 200 V Fairchild Si MOSFETs; and 3) a dual-active bridge with a stacked inverter (see Fig. 3), using the same transformer design but with the two primaries connected in series to form one primary winding, and with 550 V Infineon Superjunction Si MOSFETs.

The inverter devices were selected on the basis of minimizing the product $R_{ds,on}C_{oss}$ while preferentially selecting devices with low C_{oss} to allow the converter to achieve ZVS at lower powers. 200 V devices were chosen for the double-stacked converter to allow for some headroom on the blocking voltage. 550 V Si Superjunction devices were chosen for the single-stacked topology even though the single-stacked full bridge inverter devices only needed to block (380 V)/2 = 190 V. This was because the Superjunction devices offered a better $R_{ds,on}C_{oss}$ product than the available 250 V – 300 V MOSFETs, and their standard DPAK package also allowed the same Si-based DSAB converter PCB to be used, minimizing prototyping costs. Evaluating the performance of GaN devices rated for greater than 200 V would have required an additional PCB layout.

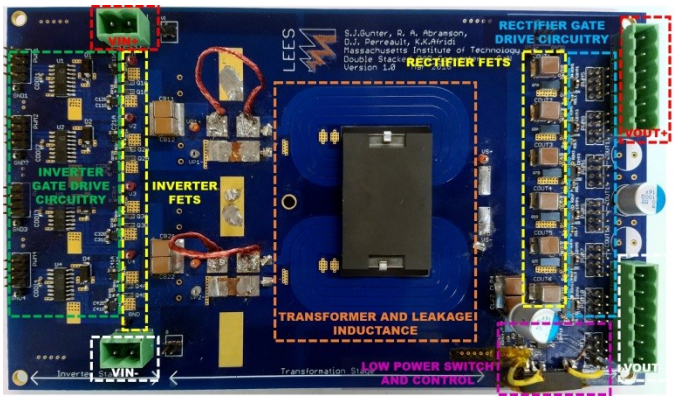


Fig. 11. Top side of the GaN-based DSAB prototype. The inverter and rectifier devices and control circuitry are labeled, as is the single-core magnetic component.

TABLE I. COMPONENTS FOR PROTOTYPE CONVERTERS

Component	Description		Value / Device
Q_1-Q_8	Inverter switch	DSAB GaN	EPC2012C
		DSAB Si	FQD10N20L
		Single-Stacked DAB Si	IPD50R280CE
Q_9-Q_{12}	Rectifier switch	3x EPC2023 30V/60A eGaN FETs (connected in parallel)	
Q_{LP}	Low-power switch	2x EPC2023 30V/60A eGaN FETs (source connected) 2 sets in parallel	
N	Transformer turns ratio	16:1	
L	Leakage inductance	16 µH on each primary[a], EPCOS EILP43-N49 core 8-layer PCB, 4oz copper internal layers, 2oz copper outer layers	
C_{in}	Input capacitors	DSAB	3x 3.3 µF 250 V
		Single-Stacked DAB	4x 2.2 µF 450 V All ceramic
C_{out}	Output Capacitors	12x 100 µF 16 V ceramic	
C_{LP}	Low-power capacitors	2x 100 µF 16 V ceramic 1x 1000 µF 16 V electrolytic	
C_B	Blocking capacitors	DSAB	2x 3.3 µF 250 V
		Single-Stacked DAB	2x 2.2 µF 450 V All ceramic
C_{bal}	Balancer capacitors	1 µF 250 V ceramic	
D	Balancer diodes	Diode Array 300 V 225 mA (2 Pair Series Connection)	

[a] As measured by an impedance analyzer and verified based on experimental power transfer

The design of each prototype is summarized in Table I, and the top side of the GaN converter is shown in Fig. 11.

A. Transformer Design

A single core magnetic component was used to provide the three-winding transformer, with leakage inductance used to realize the energy transfer inductor; the design realizes the function modeled in Fig 2. The nominal operating point of the DSAB converter was chosen to satisfy the requirements for a 380 V dc bus in data centers with dc distribution, with a 380 V nominal input voltage (with 350 V to 410 V input voltage range) and a constant 12 V output voltage [20]. Using (3) and the values of 380 V and 12 V for the system input and output

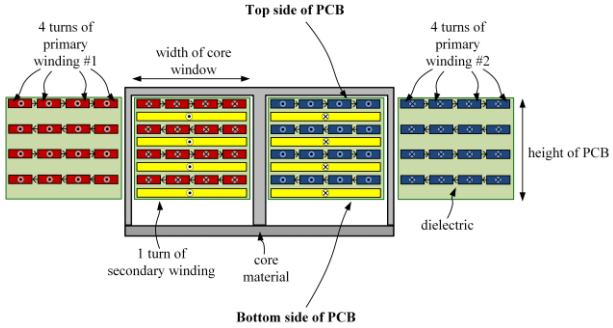


Fig. 12. Cross-sectional view of the magnetic core and PCB layer stack-up for the three-winding transformer. Primary windings are in red and blue, and the secondary winding is in yellow. Primary and secondary windings are interleaved.

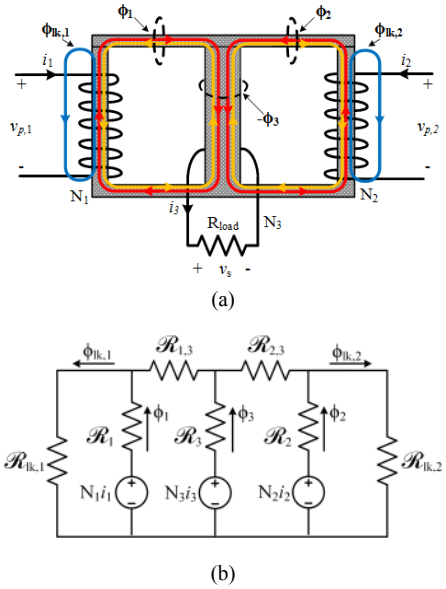


Fig. 13. (a) Diagram of the flux paths of the three-winding transformer. Fluxes ϕ_1 and ϕ_2 in the outer legs link the secondary, and $-\phi_3$ is the flux through the center leg. Fluxes $\phi_{lk,1}$ and $\phi_{lk,2}$ are the primary winding leakage fluxes that do not link to the secondary. (b) The equivalent magnetic circuit model that includes the primary-side leakage paths, as well as the main flux paths through the core legs.

voltages, the transformer turns ratio was designed for the nominal condition so that:

$$N = \frac{v_{p,tot}}{v_s} = \frac{190\ V}{12\ V} = 15.833 \approx 16 \qquad (7)$$

where 16 was chosen as the closest integer value. The primary-to-secondary turns ratio was then found to be 16:1.

For the reasons summarized in [21], a planar winding design was chosen to implement the three-winding leakage transformer. An 8-layer PCB stack-up was used to allow for interleaving between the primary and secondary windings to reduce ac resistance, as well as to allow for paralleled secondary windings to increase current carrying capability and decrease dc resistance. A simplified representation of the PCB stack-up is shown in Fig. 12. The primary windings are shown in red and blue and wrap around the outer legs; the secondary winding is shown in yellow and wraps around the center leg. The primary and secondary windings are interleaved inside the

core window, but the primary windings on the outside of the core are not interleaved as there is no secondary winding in that section of PCB. Each primary winding has 16 turns and the secondary consists of only one turn. Each primary has four dedicated PCB layers, and each layer contains four turns. The four layers are then connected in series to form a total of 16 turns, as required. The secondary winding is also split over four layers. However, because it carries high current and only requires one turn, each trace is made almost as wide as the core window and the four secondary layers are then paralleled to further decrease dc resistance by increasing trace cross-sectional area. To reduce proximity effect and decrease ac resistance, the secondary and primary layers are fully interleaved. 4 oz. copper was used on the six internal PCB layers to mitigate skin effects, while 2 oz. copper was used on the external layers to allow for the required trace spacing and width in the footprints of the GaN devices.

The leakage inductance is also realized by this structure. A significant portion of the leakage arises due to the sections of primary winding that are outside the core window. These outside sections of winding generate magnetic field lines which do not link to the secondary, increasing leakage inductance. Fig. 13 (a) shows the main flux paths for the transformer, including these leakage paths. Fig. 13 (b) shows the corresponding magnetic circuit model.

The resulting leakage was measured on an impedance analyzer to be approximately 32 µH when referred to the primary side, so that L = 16 µH in Fig. 2. To verify this, the value of the total leakage was also found experimentally by running the converter and using the power characteristic of (4) to back -solve for L, given all other parameters.

B. Prototype Performance

Waveforms of the GaN-based DSAB converter operating at the nominal operating point of 380 V input and 12 V output at 300 W and running in the full-power mode are shown in Fig. 14. The top and bottom primary voltages can be seen to be right on top of each other, showing good voltage balancing between the inverters without the need for active balancing circuits. Passive balancing circuits are used within each individual stacked full-bridge inverter (but not between the two inverters), as illustrated in Fig. 15; these circuits processed negligible power. The current waveform is the desired flat-topped trapezoid.

Operating waveforms were also taken of the converter at one quarter of the rated output power. Fig. 16 shows a comparison of the waveforms for the GaN DSAB converter operating at 75 W (the quarter-power point) in (a) the full-power mode and (b) the low-power mode. In the low-power mode, the primaries are alternately driven in square mode and held at zero voltage, and the rectifier is configured as a half-bridge. As can be seen, the low-power mode results in an increase in the peak inductor current relative to the full-power mode, as $\phi_{75W,LP}$ is larger than $\phi_{75W,FP}$ (8.1° (.141 rad) compared

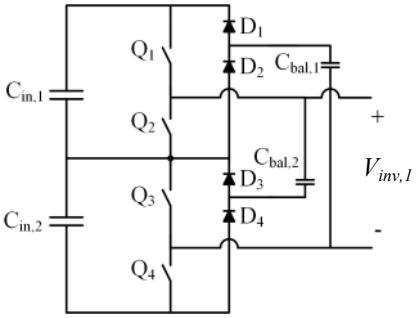


Fig. 15. Balancer circuit used to balance the input capacitors within one stacked full-bridge inverter. $C_{in,1}$ and $C_{in,2}$ are balanced with respect to each other using $C_{bal,1}$ and $C_{bal,2}$. Only the top inverter, connected to $V_{inv,1}$ is shown here; the same circuit is used on the bottom inverter.

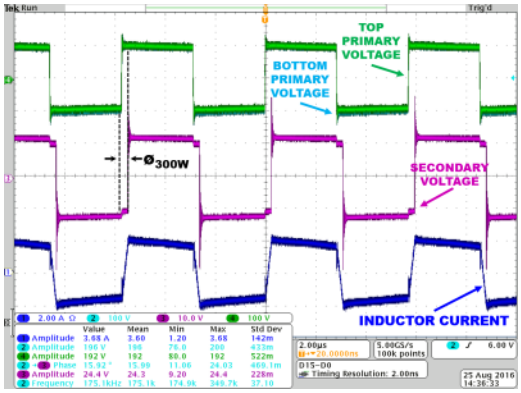
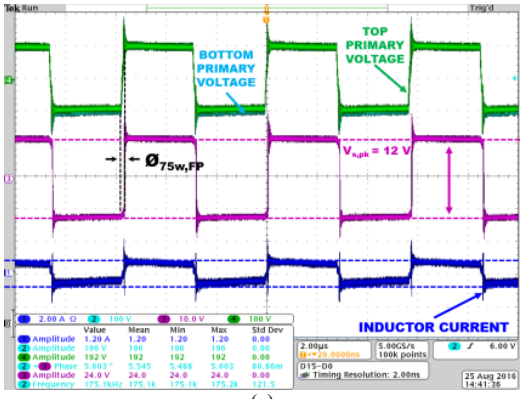
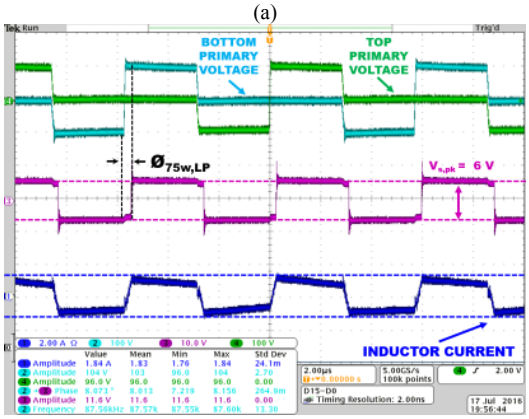


Fig. 14. Operating waveforms for the GaN DSAB converter operating in full-power mode with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 17.2° to deliver 300 W (100% load).



(a)

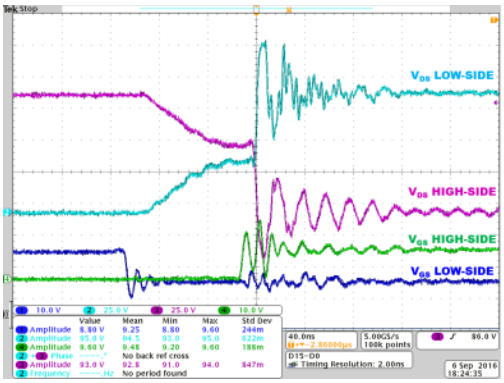


(b)

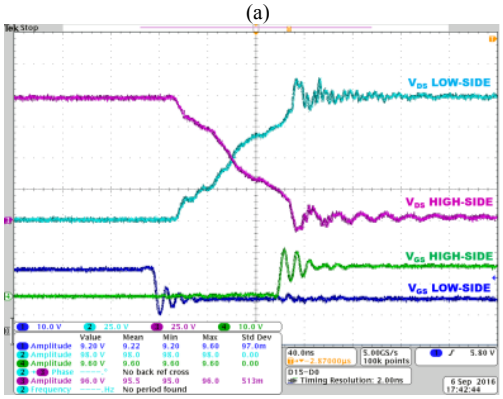
Fig. 16 Operating waveforms for the GaN DSAB converter with an input voltage of 380 V, an output voltage of 12 V, and an output power of 75 W in (a) full-power mode at a phase shift of 8.1° (.141 rad), and (b) low-power mode at a phase shift of 18.0° (.314 rad).

to 18.0° (.314 rad)), so the inductor current is allowed to ramp longer and therefore reaches a higher peak value. This results in the converter achieving ZVS down to a lower output power.

Fig. 17 shows a comparison of the switch transitions for the GaN DSAB converter in both full-power and low-power mode, by showing the V_{ds} and V_{gs} waveforms for the high-side and low-side devices in one inverter half-bridge. Fig. 17 (a) shows the transition for the converter operating in full-power mode at an output power of 75 W. The switches are hard-switched (with only a fraction of device capacitive energy saved), as evidenced by the large ringing on the V_{ds} waveform, and the fact that the V_{ds} voltage does not rise or fall all the way to its final value by the end of the dead-time (the time when both top- and bottom-side V_{gs} signals are zero). Fig. 17 (b) shows the converter operating in the low-power mode, also at 75 W. In the low-power mode, it was observed that the rise and fall transitions on the inverter devices had slightly different ZVS capability, possibly due to the asymmetry in the primary drive signals. Here, we show the transition that soft-switches the least amount. As can be seen, however, most of the transition is still soft-switched, with only slight ringing on the V_{ds} waveform. The low-power mode was able to maintain ZVS on at least one of the rise and/or fall transitions down to 52 W, while the full-power mode started to lose ZVS around 150 W, showing that the low-power mode was successful at maintaining ZVS down to a much lower power than the full-power mode.



(a)



(b)

Fig. 17. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the GaN DSAB converter operating at 75 W in (a) the full-power mode and (b) the low power mode. The low-power mode is able to mostly achieve soft-switching, while the full-power mode experiences substantial hard-switching.

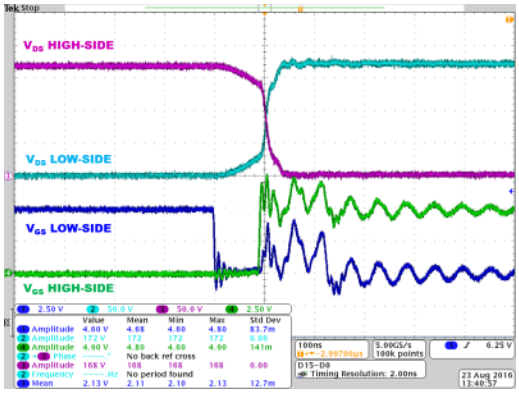


Fig. 18. V_{ds} and V_{gs} waveforms for an inverter half-bridge in the Si single-stacked DAB converter operating with an input voltage of 380 V, an output voltage of 12 V, and a phase shift of 14.7° (.257 rad) to deliver 150 W. The switches are hard-switched for most of the switch transition.

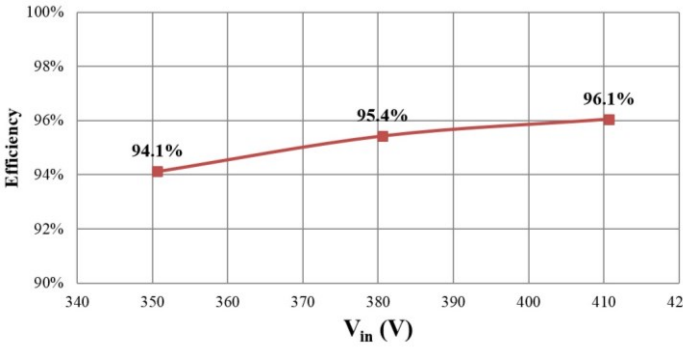
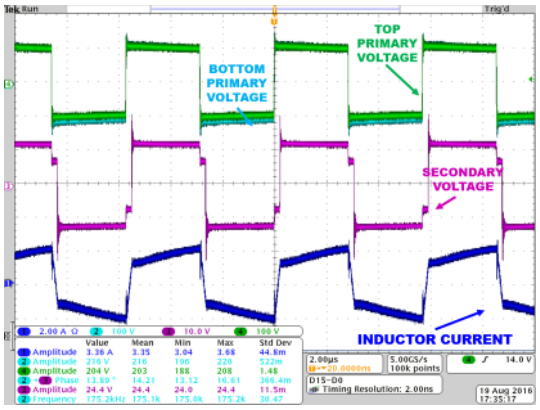


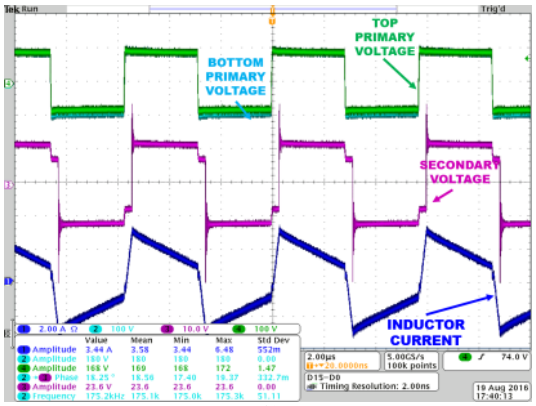
Fig. 19. Experimental efficiency of the Si DSAB converter delivering 300 W over an input voltage range of 350 V to 410 V.

The single-stacked DAB converter's ZVS performance was also investigated, and performed worse than either the full-power or low-power modes of the GaN DSAB. While the single-stacked DAB was able to achieve ZVS at full-power, by 50% load (150 W), the converter switches were hard-switched for most of the switch transitions, as shown in Fig 18.

The converter efficiency was tested over a wide input range of 350 V to 410 V to match the standard input voltage variation expected in a data center application. Fig. 19 shows the experimental efficiency of the Si DSAB converter from 350 V to 410 V at an output power of 300 W. The efficiency stays above 94% over the entire voltage range, and increases with increasing voltage, due to the lower RMS currents at the high end of the input voltage range. Fig. 20 shows the operating waveforms for the Si DSAB converter at (a) 410 V input and (b) 350 V input at an output power of 300 W. At 410 V, the inductor current slopes up because the input voltage is higher than the nominal voltage. At 350 V the inductor current slopes downward, and has a very steep slope due to the voltage transformation ratio mismatch. Because the current slopes downward, the actual current value at the inverter switch transition has decreased, and as the input voltage is further decreased, the converter will lose ZVS due to the shape of the current waveform, a well-known limitation of the traditional DAB converter. While this converter can still be operated across a reasonably wide input voltage range with high



(a)



(b)

Fig. 20. Si DSAB converter operating waveforms at an input voltage of (a) 410 V and (b) 350 V, both at an output voltage of 12 V and an output power of 300 W.

efficiency, the true benefit of the proposed topology and control scheme is seen across a very wide output power range.

Efficiency curves for operation across a wide output power range were obtained for all three topologies mentioned above, as well as for the low power modes for the double-stacked topologies (the single stacked converter is not capable of low-power mode operation). As shown in Fig. 21 and Table II, the three converters' efficiencies are close above 250 W (but favoring the double-stacked (DS) GaN design); however, below this, the efficiency of the single-stacked (SS) designs drops dramatically. Simulations also showed that a traditional full-bridge DAB converter would have shown even worse efficiency performance [22-23].

Below 20% load, the DSAB's low-power mode significantly improves the efficiency of the converter as compared to the full-power mode, increasing the efficiency from 66.0% to 79.8% for the GaN DSAB converter, which represents a roughly 40% reduction in loss; see Table III. The GaN-based double-stacked topology has an efficiency of greater than 92.7% down to 10% load. In comparison, the single-stacked topology drops to 69.5% across this range. The double-stacked GaN design in low power mode is 79.8% efficient at 3.3% load, while the single-stacked is only 41.4% efficient, highlighting the proposed topology's ability to achieve high-efficiency operation across a wide power range.

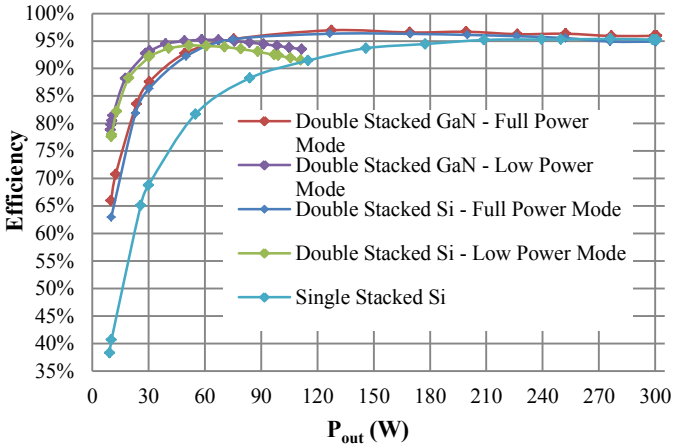


Fig. 21. Experimental efficiency curves across output power for double stacked converters populated with GaN and Si switches operating in full power and low-power modes, as well as a curve for a single stacked converter with Superjunction Si switches.

TABLE II
EFFICIENCY AT 300 W (100% LOAD)

Topology	P_{OUT} (W)	Efficiency
DS GaN – full-power mode	299.6	95.9%
DS Si – full power mode	299.7	94.9%
SS Si	299.1	95.2%

TABLE III
EFFICIENCY AT 10 W (3.3% LOAD)

Topology	P_{OUT} (W)	Efficiency
DS GaN – full-power mode	9.97	66.0%
DS GaN – low-power mode	10.01	79.8%
DS Si – full-power mode	10.07	62.9%
DS Si – low-power mode	10.19	77.6%
SS Si	10.20	41.4%

Both the Si and GaN DSAB converters had ~10-22% lower percent loss compared to the Si single-stacked converter.

Additionally, the GaN DSAB converter showed better performance compared to the Si DSAB converter at high powers due to its lower $R_{ds,on}$, achieving 0.8-1.2% lower percent loss (or equivalently a roughly 20% reduction in loss).

Using Si devices, the DSAB converter was able to achieve an efficiency of 94.9% at full load, a peak efficiency of 96.3%, an efficiency above 92.3% down to 10% load, and an efficiency above 77.6% down to 3.3% load. By comparison, the GaN-based DSAB converter was able to achieve an efficiency of 95.9% at full load, a peak efficiency of 97.0%, an efficiency above 92.7% at 10% load, and an efficiency above 79.8% at 3.3% load.

IV. CONCLUSIONS

This paper has presented the design and implementation of a new converter topology designed to achieve high efficiency both at full-load as well as during light load conditions. This was done through 1) the use of a double stacked-bridge inverter, which allowed for the use of lower-voltage rated devices that can provide better ZVS performance; 2) a compact

single-core three-winding leakage transformer; and 3) a reconfigurable rectifier and alternative switching patterns providing a low-power mode that reduces core loss and extends the ZVS range of the converter. The low-power mode is implemented with an auxiliary switch and a change in inverter and rectifier drive signals, which can be pre-programmed into a controller for easy configuration. The converter is operated with simple phase shift control and with fixed dead-times for both modes. This paper also presented experimental results from three prototype converters: GaN and Si DSAB converters, as well as a Si Superjunction single-stacked converter. The GaN DSAB topology proved to be the most efficient over the entire load range, and was capable of achieving a peak efficiency of 97%, an efficiency greater than 92.7% down to 10% load, and an efficiency greater than 79.8% down to 3.3% load.

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