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High-Frequency Isolated ac-dc Converter with Stacked Architecture

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***Abstract*—This paper presents a new isolated ac-dc power converter achieving both high power factor and converter miniaturization suitable for many low power ac-dc applications. The proposed ac-dc converter architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a multi-input isolated bus converter. Among many suitable circuit implementations, the prototype system utilizes the resonant-transition buck converter as a regulating converter, and the capacitively-aided isolated bus converter for the isolated bus converter. The converter is miniaturized by operating at high frequency (1 – 10 MHz range), and it buffers the ac-line frequency energy with a pair of stacked ceramic capacitors (1 μF and 150 μF, 100 V rating) without a requirement for electrolytic capacitors. The prototype converter is implemented to operate from 120 V_{ac} to 12 V, and up to 50 W output as an example isolated ac-dc converter for power supply applications. The prototype converter demonstrates with 88 % efficiency and 0.86 power factor, and provides 50 W/in^3 power density, which is five times higher than the power density of typical conventional designs.**

I. Introduction

Achieving high efficiency and high power density are definite goals for the ac-dc power supplies. Moreover, while power factor has been traditionally considered important mainly at high power levels to best convey real power from the ac grid to a dc load [1], [2], it is of increasing concern at low power levels as well (e.g., 10s of watt) to reduce the conduction loss and voltage distortion in the grid.

To explore the performance of conventional ac-dc converters, we investigated a group of commercial isolated ac-dc portable device / laptop battery chargers as shown in Table I. The measured specifications illustrate that most of the commercial converters do not achieve both high efficiency and high power factor (e.g., efficiencies in the range of 73 – 88 % and power factors of 0.59 – 0.63); Moreover, isolated ac-dc converters at this power level remain bulky and the power densities are in the range of 10 W/in^3 and below though research designs are starting to appear that have higher power density [3].

Most of the ac-dc isolated converters at 10's of watts utilize the flyback converter topology operated from a line-rectified dc bus. This flyback design, however, provides low power factor and is largely dominated by passive components including the EMI filter, energy buffer capacitor, magnetic transformer, and output capacitors, and thus results in large volume. At higher power levels (e.g., 75 watts and above) and in specific applications such as LED drivers, there are requirements on harmonic content or power factor [4], [5]. One common method to achieve better line waveforms is to cascade a "Power Factor Correction (PFC)" circuit, a large electrolytic capacitor, and a dc-dc converter as illustrated in [1], [2]. In this approach, a front-end PFC circuit modulates the switch(es) so that it shapes the input current waveform over the ac-line cycle for high power factor (often providing a sine-wave or clipped-sine-wave input current waveform), and the associated twice-line frequency power fluctuation is then buffered by its large output capacitor (typically implemented with an electrolytic capacitor). The following dc-dc converter then takes the voltage across the energy buffer capacitor and supplies and regulates the system output voltage.

TABLE I
Measured Specifications of Commercial ac-dc Chargers

	Sony	Apple	Apple	Apple
Output Power	50 W	10 W	45W	56W
Input Voltage	Universal ac voltage 100 – 240 Vac			
Frequency	92.1 kHz	57 kHz	103.6 kHz	105 kHz
Efficiency	86 %	73 %	88 %	86.5 %
Power Factor	0.59	0.61	0.56	0.63
Power Density	10.4 W/in^3	7 W/in^3	10.4 W/in^3	11.5 W/in^3

There are many converter topology options for the front-end PFC circuit including the boost converter [1], [2], [6] and buck converter [7]–[10]. However, these approaches are not amenable to converter miniaturization because: 1) it is hard to greatly reduce the volume of the converter through high-frequency operation owing to loss limits, large inductance (i.e., high characteristic impedance level), and large parasitic capacitance levels (e.g., large output capacitance of the switch) [11]–[13]; 2) the volume of the energy buffer capacitor is large, and 3) for a boost front end, the following dc-dc converter must operate at high voltage when it is tied to the stepped up (high) voltage after the boost PFC converter, and has a large step-down voltage conversion ratio (especially for low output voltage application), so that it is again difficult to be realized at high frequency with small volume.

Here we present an isolated ac-dc converter with a stacked architecture [14], [15] and utilizing a inverted resonant transition buck converter and a capacitively-aided isolated bus converter [16] to provide galvanic isolation and voltage transformation. The proposed ac-dc converter addresses converter miniaturization through high-frequency operation while main-

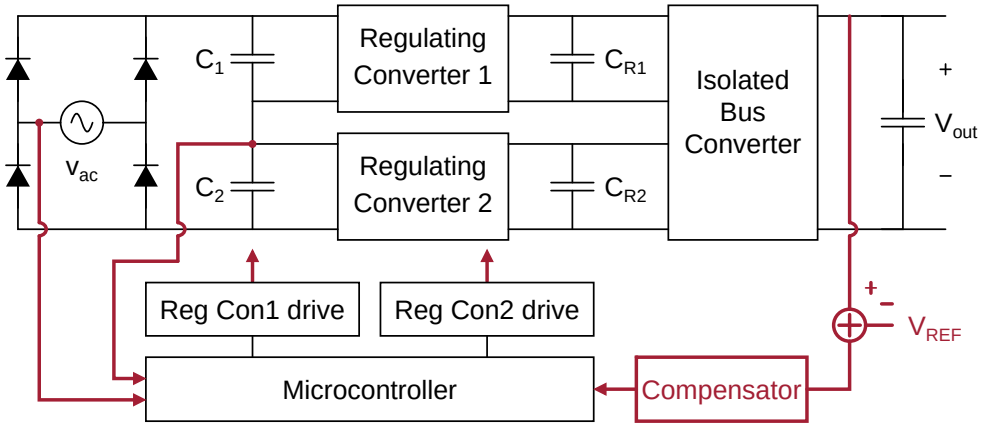

Fig. 1. The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter.

taining good efficiency, and achieves reasonably high power factor consistent with line harmonic requirements [5], while dynamically buffering twice-line frequency energy at moderate voltages with large voltage swings [17]–[23]. Section II of the paper describes the structure and operation of the proposed stacked ac-dc architecture. Section III and IV of the paper present a circuit implementation and experimental results demonstrating the proposed system. Finally, Section V concludes the paper.

II. Stacked ac-dc Converter Architecture

The proposed stacked ac-dc architecture is illustrated in Fig. 1 along with the feedback approach used to provide output voltage control [15]. The system architecture comprises a line-frequency rectifier, a stack of capacitors across the rectifier output, a set of regulating converters having inputs connected to capacitors on the capacitor stack, and a multi-input isolated bus converter that combines the power from the outputs of the regulating converters to provide a single output.

The line-frequency rectifier draws current from the grid during a portion of the cycle, based on how the regulating converters are controlled. The converter can provide high power factor while capacitor C_2 (which is much larger than capacitor C_1) provides the twice-line-frequency energy buffering over the line cycle.

Regulating converters provide regulated outputs and ultimately regulate the system output under control of the feedback circuitry. Because the regulating converters operate from voltages that are much smaller than the total line voltage, they can be designed to switch at much higher frequencies than conventionally used for converter miniaturization (e.g., as described in [12] [24]). Among many regulating converter topology options, the resonant-transition inverted buck converter can be very effectively utilized [24]. This topology enables converter miniaturization with high-frequency operation (3 – 10 MHz), high efficiency, low device voltage stress, small component size, and good control capability without the need for a current sensor..

The isolated bus converter has two inputs connected to the outputs of the regulating converters, wherein it draws energy from the two regulating converter outputs. The isolated bus converter provides galvanic isolation, voltage transformation while delivering combined power to the converter system output. With the stacked ac-dc architecture and the feedback control of the regulating converters, the isolated converter operates from a low / narrow-range input voltage, and does not need to provide regulation capability; thus the isolated converter can be designed to be very compact operating at high frequency [11] using a capacitively-aided isolated bus converter [16]. The selected capacitively-aided isolated bus converter maintains ZVS condition for all the primary and secondary switches independent of the power level, which thus provides high efficiency with high frequency operation.

A. Operation

Before introducing an example implementation with a specific regulating and isolated bus converter circuit topology, we show how the stacked ac-dc converter structure operates while buffering twice-line-frequency energy at capacitor C_2. This approach is related to that of our earlier work [15].

Fig. 2 shows the operating states of the proposed converter with the example operating waveforms. During state 1, the instantaneous amplitude of the ac input voltage is lower than the total voltage of the stacked capacitors; the full-bridge rectifier is off and there is no current drawn from the grid. During this state, the bottom regulating converter (regulating converter 2) delivers and supplies the system power using the stored energy in the energy buffer capacitor C_2. When the instantaneous amplitude of the ac input voltage reaches the total capacitor stack voltage, the full-bridge turns on and the circuit enters state 2. During state 2, the top regulating converter (regulating converter 1) delivers the power while the total voltage of stack capacitors tracks the rectified ac input voltage. The full-bridge turns on and conducts the input current, and capacitor C_2 charges up during state 2. After a certain conduction time, the top regulating converter is turned

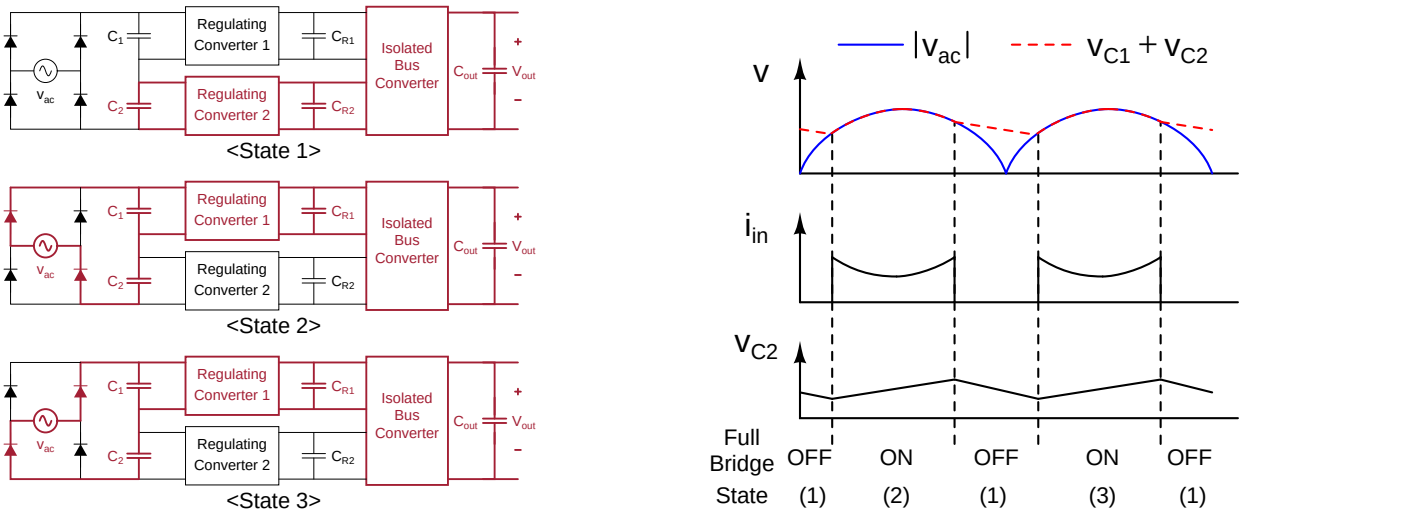

Fig. 2. The figure illustrates the three states and operation of the stacked ac-dc converter system. The waveform shows input current and voltage across capacitor C_2 waveform across the line cycles.

off and the bottom regulating converter is turned on, and the circuit enters state 1 and the cycle repeats (In state 3, the ac voltage is simply opposite polarity to the state 2, but the converter operation is the same as in state 2).

The proposed architecture accomplishes three functions: First, it draws power from the line with large conduction duration with good power factor. Second, it dynamically buffers twice-line-frequency energy from the line on the capacitor C_2, with a significant swing on the voltage of C_2 enabling utilization of a large percentage of its energy storage capability in buffering twice-line-frequency power variations from the line. Lastly, while it is not explicitly shown above, the regulating converter steps down the large input voltage, and provides narrow-range regulated outputs (i.e., regulates system output voltage) for the following isolated converter.

B. System Characteristics, Design Tradeoffs, and Converter Design

The proposed grid interface architecture we adopt has significant advantages for converter miniaturization through high frequency operation. In addition, there are many tradeoffs among the design parameters including stack capacitance values, power level, capacitor voltage swing variation over line cycle, regulating converter operating range, and power factor. Thus, selecting appropriate topologies, design values, and operating voltage / current waveforms is essential.

One key design parameter is selection of the stack capacitor value C_1. A preferred approach is to size the capacitors asymmetrically (one large, one small), such that one of the capacitors (e.g., large C_2) buffers most of the twice-line-frequency energy, while the other capacitor (e.g., small C_1) is much smaller and simply acts as a bypass capacitor for its associated high-frequency switching stage. One capacitor (e.g, C_2) is thus sized principally based on line-frequency energy buffering, while the other capacitor (e.g., C_1) can be designed to have a small value and is used for filtering the converter's switching ripple current. In addition, it should be noted that there is a motivation not to make this bypass capacitor (C_1) too large, as the capacitor draws an input current component owing to the ac voltage envelope as illustrated in equation (1), and (capacitively) degrades power factor.

$$i_{C1}(t) \text{ when stack of capacitor tracks ac voltage envelop} = C_1 \frac{dv_{c1}}{dt} \simeq C_1 \omega_{ac} V \cos\omega_{ac} t \ll P_o/V \quad (1)$$

Fig. 3 further describes the relation between achievable power factor and the C_1 values for a given output power (e.g, $K_{c1p} = C_1 / P_{out}$) when the $K_{c2p} = C_2 / P_{out} = 2\,[\mu F/W]$ and it operates at 120 Vac line voltage. This example shows the detailed effect of C_1 capacitance values on the achievable power factor, such that larger C_1 value degrades power factor for a given power level and C_2 capacitance value. Based on the considerations shown in equation (1) and Fig. 3, it is desirable to make this bypass capacitor (C_1) small enough that this capacitive current component is small compared to the active line current that is drawn. We typically select the bypass capacitor to be $K_{c1p} = C_1 / P_{out} = 0.01 - 0.1$. (e.g., for the 50 W ac-dc voltage regulated system implementation shown in section III, we used a capacitor in the range of 1 μF for C_1.)

Next, several design factors need to be considered for the energy buffer capacitor C_2. Capacitor C_2 mainly buffers the twice-line-frequency energy of the converter, and the voltage across it fluctuates over the line cycle. We select its value such that it can buffer the needed amount of energy at maximum power operation while having an acceptable voltage swing across which the following regulating converters can operate. If we make the simplifying assumption of ideal unity power factor, the voltage fluctuation follows equation (2):

$$\text{ac buffer energy} = P_0/\omega_{ac} = \frac{1}{2} C_2 V_{max}^2 - \frac{1}{2} C_2 V_{min}^2 \quad (2)$$

Fig. 4 further describes the detailed simulation results between voltage swing and the main energy buffer capacitor C_2 value (e.g, $K_{c2p} = C_2 / P_{out}$) of the proposed architecture shown in

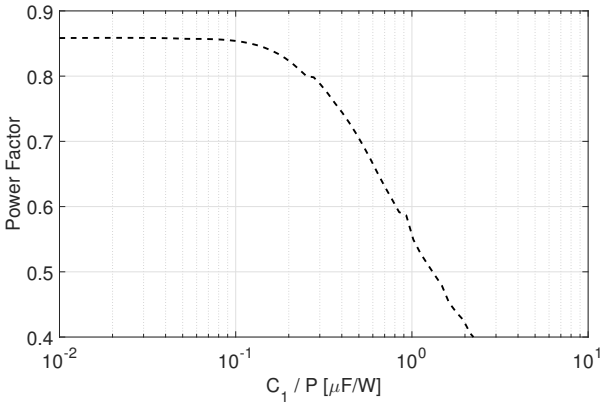

Fig. 3. The figure shows the achievable power factor of the voltage-regulated system with different C_1 values at the given power level (e.g, $K_{c1p} = C_1 / P_{out}$) when $K_{c2p} = C_2 / P_{out} = 2$ [μF/W]. This figure illustrates the effect of small capacitance values (i.e., C_1, the capacitor stacked with the main energy buffer capacitor C_2) on the achievable power factor. It can be seen that larger C_1 values degrades power factor for a given power level and C_2 capacitance value.

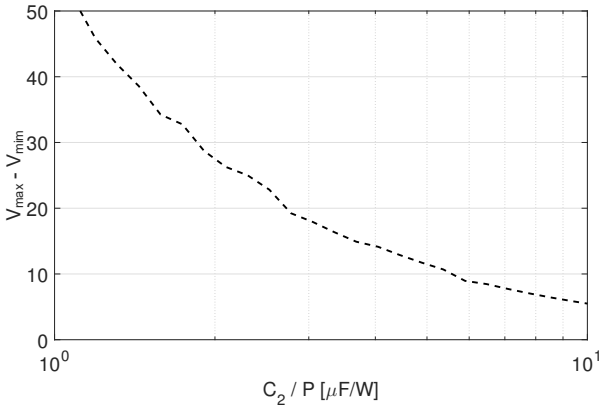

Fig. 4. This figure illustrates the relation between the voltage swing across the energy buffer capacitor and its capacitance (e.g, $K_{c2p} = C_2 / P_{out}$) when the $K_{c1p} = C_1 / P_{out} = 0.2$ [μF/W] and the converter operates at 120 V_{ac} input voltage and dc output power P_{out}. As shown in the graph, a smaller energy buffer capacitor increases the voltage fluctuation over the line cycle, such that the following regulating converters need to operate across wider voltage ranges.

Fig.1 when the $K_{c1p} = C_1 / P_{out} = 0.2$ [μF/W]. As shown in Fig. 4 and equation (2), a smaller energy buffer capacitor C_2 value increases the voltage swing across the energy buffer capacitor over the line cycle. The regulating converters then need to be operated over this wider voltage range, which can degrade the size and performance of the regulating converters. In contrast, the value of the capacitor C_2 can be selected to be very large so that its voltage swing is small over the line cycle, but results in large buffering capacitor volume and reduces power density. Thus, the energy buffer capacitor (C_2) can be scaled down as long as the capacitor voltage swings within the input voltage range of the selected regulating converter. Approximately up to a 2:1 (Vmax:Vmin) voltage swing provides a good tradeoff, such that we utilize up to approximately 75% of the capacitor energy storage capability. In practice, one can start with $K_{c2p} = C_2 / P_{out} = 1-2$ as a lower bound to size the capacitance, and then scale the capacitor value up to account for capacitor nonlinearity, and to provide design margin.

Furthermore, there is a possibility to achieve higher performance utilizing a complex converter topology and control method. For example, selecting a bi-directional topology for the regulating converter can improve the achievable power factor of the system and reduce the required size of the buffer capacitor, but it makes the design of the regulating converters much more challenging. Another example is designing power combining converter with regulation capability and having some portion of twice-line-frequency ac-energy buffered at the regulating converter outputs. This opens up the possibility to design ac-dc converters with higher power factor (above 0.95), but likewise it increases complexity of the converter. Lastly, among the wide range of input current waveform patterns that can meet these broad goals (for reasonable values of power factor and voltage swing across energy buffer capacitor), one can select complicated control and optimize the size and performance of the converter along with bi-directional topology and distributed energy buffer. However, in general it significantly increases the complexity of the converter and it is hard to design with simple converter topologies in this case.

Overall, there are tradeoffs among stack capacitor values, voltage swing across the stack capacitors, regulating converter topology, power factor, and power level, and all of these characteristics are intermingled. The proposed architecture thus should be designed with desired component parameters and topologies after detailed simulation considering all the tradeoffs.

III. Implementation

Fig. 5 illustrates the implementation of the ac-dc isolated converter. It comprises a line-frequency rectifier, an EMI filter, a stack of capacitors, a set of inverted resonant buck converters having inputs connected to the stack capacitors, and a capacitively-aided isolated bus converter [16]. The two power flow paths from the stacked regulating converters are coupled capacitively with dc blocking capacitors in the isolated bus converter, which combines the power from the regulating converters to supply a single system output. The converter operates at 120 Vac and supplies up to 50 W power at 12 V output, which fits isolated ac-dc applications such as power supplies.

To address the design considerations and achieve high efficiency and high power density, the regulating converters are designed as inverted resonant-transition buck converters as shown in Fig. 5. The regulating converter is designed with single switch, diode, and small inductor, and operates around 3 – 10 MHz frequency similar to the regulation-stage design illustrated in [12], [13], [15]. It is an "inverted" circuit in the sense that it is designed with "common positives" (i.e., the positive node of the converter's input voltage is common

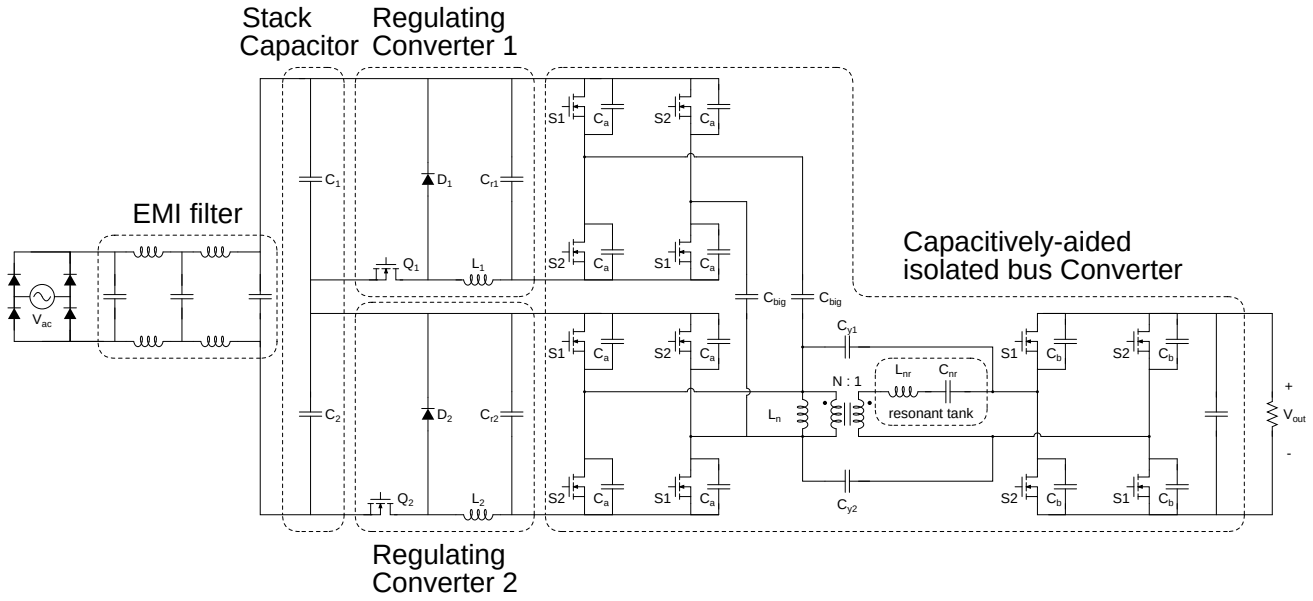

Fig. 5. This figure shows the implementation of the ac-dc isolated converter using a stacked grid interface architecture [15]. The regulating converters are designed as resonant-transition inverted buck converters operating at high frequency, and a multi-input capacitively-aided bus converter is utilized as a dc transformer [16]. The isolated bus converter is coupled with capacitor to combine the power from two regulating converters and supply the single system output.

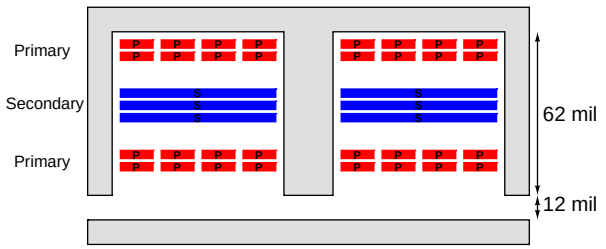

Fig. 6. The figure shows the layer configuration of the planar transformer for the isolated bus converter (prototype shown in Fig. 9), with the windings implemented as pcb traces in the 12-layer board (with 2 oz/in^2 of copper). The primary side is realized as 8 turns around the core by parallel-connecting two sets of 2 layers, each having 4 turns/layer, and the secondary is wound with 3 turns by series connecting 3 single turn traces on different layers.

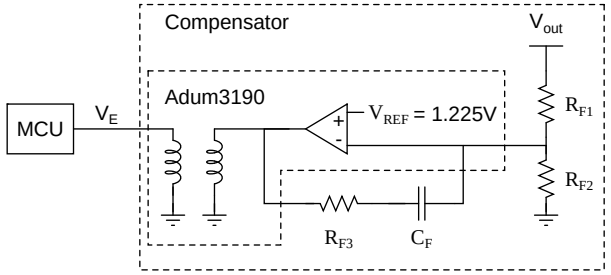

Fig. 7. The figure shows the PI compensator design with isolated error amplifier (Adum3190 from Analog devices which also provides a 1.225 V reference voltage). The voltage divider values are selected such that $R_{F1}/(R_{F1}+R_{F2})$ V_{out} = 1.225 V and the transfer function of this compensator is as shown in Fig. 8.

with the positive node of its output voltage.) For much of its operating range, the topology acts like a quasi-square-wave ZVS buck converter with a low ratio of switching to resonant frequency [25]. Each regulating converter takes as an input one of the capacitor voltages (from the stack of capacitors) and provides a regulated voltage across its output capacitor.

This regulating converter design has several benefits. First, it operates efficiently with ZVS or near-ZVS switching conditions across a wide 35 – 100 V input voltage range. Second, the single common-referenced switch (referenced to a slowly-moving potential) makes it suitable for operation at HF (3 – 30 MHz). It should be noted that in our prototype converter, the regulating converter is designed with a flip-chip Gallium nitride (GaN) on silicon switch; this yields small on-resistance and parasitic capacitance and a compact device size, facilitating high frequency operation. Third, it requires only a single, small-valued inductor. Furthermore, it has very fast response

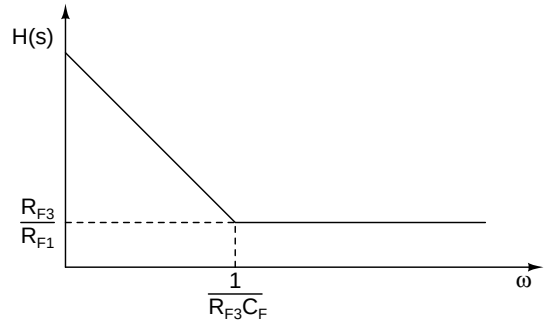

Fig. 8. This figure shows the asymptotes and intercept of the transfer function of the proposed PI compensator (H(s)) shown in Fig. 7.

(near single cycle) to input voltage transients and changes in the output current command. Finally, for a given input voltage, the output current is directly related (roughly proportional) to

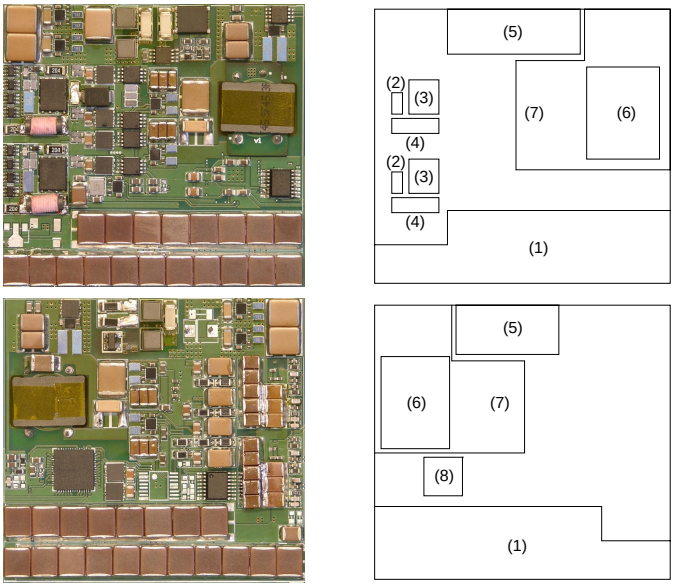

Fig. 9. The ac-dc isolated converter is implemented on a 2.1 in (x) × 1.95 in (y) × 0.22 in (z) converter box volume using the ceramic energy buffer capacitors. This figure shows the top and bottom side of the PCB illustrating several components: (1) energy buffer capacitor, (2) GaN transtors, (3) Silicon Schottky diode, (4) regulating converter inductor, (5) Full-bridge and EMI filter, (6) planar transformer, and (7) capacitively-aided isolated converter.

TABLE II
SPECIFICATIONS AND COMPONENTS OF THE AC-DC ISOLATED CONVERTER

Specification	
Input Voltage	120 Vac
Output Voltage	12 Vdc
Output Power	48 W
ac Energy Buffer	
Energy Buffer Capacitor	570 μF (15 μF × 38) X7S 100V Ceramic capacitor
Regulating Covnerters	
Switch	GaN switch EPC 2010C EPC
Diode	Silicon Schottky diode STPS30120DJF ST
Inductor	800 nH; 10 turns on a Micrometals P68-106 core
Power Combining Converter	
Inverter	GaN switch EPC 2014C Coss ≃ 150 pF
Rectifier	GaN switch EPC 2015C Coss ≃ 700 pF
C_{y1}, C_{y2}	1000 pF Y3 X7R 250 Vac (rating) and 1500 Vac (withstand), Johanson Dielectrics
Switching Frequency	1.4 MHz
Dead time	16.66 ns
Transformer Core	Ferroxcube 3F45 EQ13 with 0.28 mm gap
Transformer Number of Turns	8 : 3 (i.e, N=8/3)
Transformer Winding	Planar structure with 62 (31+31) mil thickness PCB 12 (6+6) layers of 2 oz copper
L_N	5 μH (measured from primary side)
L_{nr}	40 nH (estimated)
C_{nr}	0.33 μF C0G/NPO 50V, TDK
Control	
Microcontroller	TMS320F28035, TI
Feedback isolated error amplifier	ADuM3190, Analog Device

transistor on-time, allowing a variety of control schemes to be employed. The details of the design including operation and drive circuitry is well illustrated in [15].

For the isolated bus converter, we selected an 8:3 transformer turns ratio and designed a planar transformer as illustrated in Fig. 6. The turns ratio of the transformer also sets the voltage transformation ratio of the capacitively-aided isolated bus converter, such that the input of the isolated bus converter (e.g., output of the inverted resonant-transition buck converter) is roughly around 32 V at 12 V system output voltage. It was found that for fixed input voltage, the output voltage of the power combining converter decreases at heavy load (e.g., load regulation) such that the input voltage of the power combining converter increases up to 36 V to regulate the system output voltage to 12 V at heavy load. Even though the intermediate voltage (e.g., the output voltage of the regulating converter / input voltage of the power combining converter) changes at different power levels, the feedback circuitry regulates the system ouptut voltage independent of power level.

In this isolated ac-dc prototype converter implementation, we designed feedback circuitry to regulate the system output voltage. The feedback circuit senses the system output voltage and processes it with a PI compensator and microcontroller; Then microcontroller regulates the system output voltage using switch drive circuitry over the line cycle using either the top or bottom regulating converter at any given time. Fig. 7 illustrates how the feedback circuitry is designed to cross the galvanic isolation barrier. The system output voltage is sensed, compared, and processed with the compensator, and the processed information is then delivered to the microcontroller across isolation barrier. To accomplish this, we utilized an isolated PI compensator with the isolated error amplifier IC (ADuM3190, Analog Device) as illustrated in Fig. 7. We used a simple PI compensator; its transfer function is shown in Fig. 8. It should be noted that the sensed output voltage information and compensator circuitry should cross the galvanic isolation and control the front-end regulating converters with microcontroller and switch drive circuitry, such that voltage isolation is also required for the compensator circuitry.

Fig. 9 shows a photograph of the prototype converter along with a description of the components; and the prototype converter is implemented within a 2.1 in(x) × 1.95 in(y) × 0.22 in(z) converter "box volume". We used 570 μF 100 V (e.g., 38×15μF) ceramic capacitors to buffer twice-line-frequency energy, which acts as approximately 140 μF when it is biased at 75 V. As can be seen, the size of the inductors for the regulating converters are very small owing to the high frequency operation of the front-end regulating converters. Table II describes all the utilized components of the prototype converter.

IV. EXPERIMENTAL RESULTS

The ac-dc isolated prototype converter is tested from a 120 V_{ac} ac power source (Agilent, 6812B) into an resistive load. One external 5V power supply (xantrex, XPH series) is used for the hotel power supply to drive logic components, and used this voltage to bootstrap and make the floating 5V logic voltages. The voltage, current, power, and power factor are measured with an ac power meter (Yokogawa, WT1800), and an oscilloscope (Tektronix, MSO4104) and

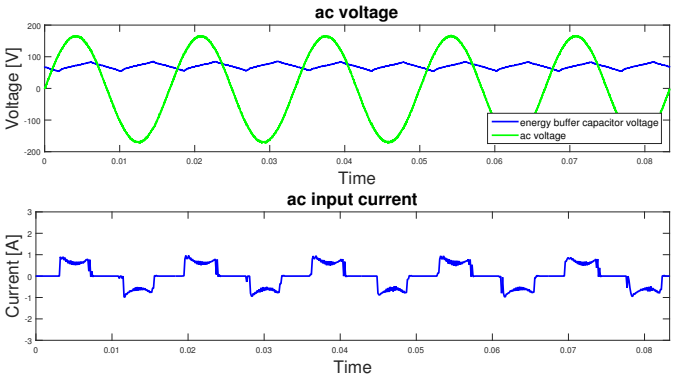

Fig. 10. The figure shows the measured waveforms when the converter operates at 120 V_{ac} and supplies 48 W at 12 V_{dc} system output. The waveform shows the ac line voltage, the voltage across the energy buffer capacitor, and the input ac line current waveform over the line cycle.

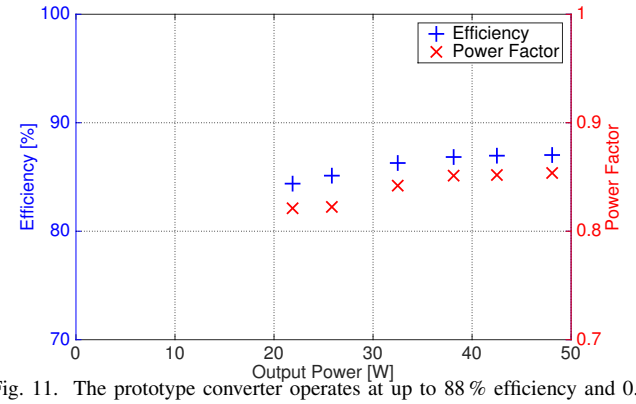

Fig. 11. The prototype converter operates at up to 88 % efficiency and 0.86 power factor and maintains good performance over a wide load range.

probes (Tektronix, TPP0500 and P5205A) are used to measure prototype converter operation.

Measurement of the voltage waveforms of the energy buffer capacitors with 120 V_{rms} 60 Hz ac line voltage waveform are shown in Fig. 10. The figure shows the voltage swing across energy buffer capacitor over the line cycle, and the input current waveform when the converter supplies 48 W power to the 12 V output. The voltage of energy buffer capacitor C_2 fluctuates across a wide voltage range (about 30 V) over the line cycle as the converter buffers the twice-line-frequency ac energy. The power factor of this waveform was measured to be 0.85.

The prototype converter was demonstrated to provide up to 88% efficiency with up to 0.86 power factor across a moderate load range as illustrate in Fig. 11. The box volume of the prototype converter yields a "box power density" of 50 W/in^3. It is notable that the achieved power density is about five times higher than the power density found for typical commercial ac-dc isolated converters (e.g., below 10 W/in^3) as shown in Fig. 12 (though we note that this version of the prototype system does not handle the universal input voltage range). This improvement in power density and converter miniaturization are the main advantage derived from the substantially higher frequency operation of the proposed ac-dc converter as

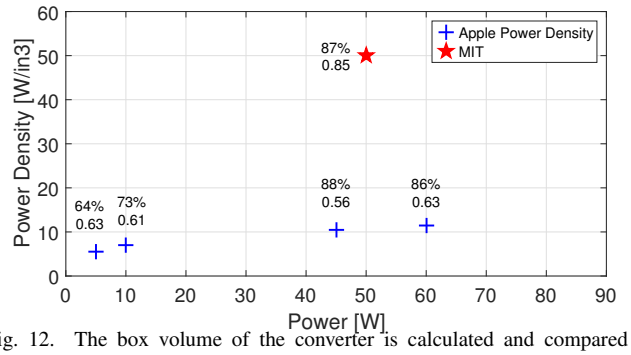

Fig. 12. The box volume of the converter is calculated and compared to the conventional isolated ac-dc converters for applications such as battery chargers from Apple. The prototype converter can achieve five times higher power density with 30 – 100 times higher switching frequency operation.

compared to conventional converters. Furthermore, as can be seen in the photograph in Fig. 9, a large area of the PCB is allocated for the microcontroller, bootstrap circuit, discrete IC components, and signal isolator; Consequently, there is further opportunity to reduce the size of converter by integrating the control circuitry into one or more ICs.

Table III illustrates the performance of the prototype converter relative to various academic studies for ac-dc isolated converters. As compared to the other designs, it can be seen that the proposed approach provides higher operating frequencies, smaller numerical values and sizes of magnetic components, and achieves higher power density. Furthermore, it achieves both good efficiency and power factor.

V. Conclusion

In this paper, we propose an isolated ac-dc converter for power supply applications that uses a stacked grid interface architecture operating at high frequency. This helps address the need for both high power density and good efficiency in ac-dc applications. The proposed approach can achieve reasonably high power factor above 0.8, while dynamically buffering twice-line frequency energy using small capacitors operating with large voltage swings over the ac line cycles without requiring electrolytic capacitors. Regulating converters are designed with the inverted resonant buck converters and operated at high-frequency (3 – 10 MHz) with significantly reduced voltage stress of the active and passive devices and zero-voltage switching (ZVS) conditions, enabling significant converter size reduction while maintaining high efficiency. The galvanic isolation stage is designed with a capacitively-aided isolated bus converter achieving ZVS for all the primary and secondary switches. Experimental prototypes have been built and evaluated from 120 V_{ac} and 12 V, 50 W output, and the converter shows that excellent combinations of power density, efficiency, and power factor can be realized with this approach.

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TABLE III
PERFORMANCE COMPARISON OF THE ISOLATED AC-DC CONVERTERS

Reference	[26]	[27]	[28]	[3]	**This work**
Topology	boost PFC + isolated Converter	clamped series resonant	Flyback	boost PFC + LLC isolated	stacked resonant buck + isolated bus
Input voltage	120 V_{ac}	120 – 240 V_{ac}	120 – 240 V_{ac}	90 – 265 V_{ac}	120 V_{ac}
Output voltage	12 V_{dc}	12 V_{dc}	19.5 V	20 V	12 V_{dc}
Output power	120 W	45 W	65 W	65 W	50 W
Switching frequency	135 kHz	[1] 40 kHz	1 MHz	800 kHz	3 – 10 MHz (buck dc-dc) 1.4 MHz (Isolated Converter)
Transformer	250 μH, 20 μH	345 μH	unknown	12 μH, 95 μH	5 μH
capacitor	200 μF electrolytic (estimated)	76 μF electrolytic	94 μF electrolytic	33 μF	570 μF ceramic
Peak Efficiency	91 %	92 %	92 %	94 %	**88 %**
Power factor	0.99	0.99	0.6 (estimated)	unknown	**0.85**
Box Power density	13 W / in^3	7.5 W / in^3	25 W / in^3	44 W / in^3	**50 W / in^3**

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