

2018

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Drummond, K. P.; Back, D.; Sinanis, M. D.; Janes, D. B.; Peroulis, D.; Weibel, J. A.; and Garimella, S V., "A Hierarchical Manifold Microchannel Heat Sink Array for High-Heat-Flux Two-Phase Cooling of Electronics" (2018). *CTRC Research Publications*. Paper 320. <http://dx.doi.org/10.1016/j.ijheatmasstransfer.2017.10.015>

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# A Hierarchical Manifold Microchannel Heat Sink Array for High-Heat-Flux Two-Phase Cooling of Electronics<sup>1</sup>

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**Abstract:** High-heat-flux removal is necessary for next-generation microelectronic systems to operate more reliably and efficiently. Extremely high heat removal rates are achieved in this work using a hierarchical manifold microchannel heat sink array. The microchannels are imbedded directly into the heated substrate to reduce the parasitic thermal resistances due to contact and conduction resistances. Discretizing the chip footprint area into multiple smaller heat sink elements with high-aspect-ratio microchannels ensures shortened effective fluid flow lengths. Phase change of high fluid mass fluxes can thus be accommodated in micron-scale channels while keeping pressure drops low compared to traditional, microchannel heat sinks. A thermal test vehicle, with all flow distribution components heterogeneously integrated, is fabricated to

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<sup>1</sup> Submitted for review to the *International Journal of Heat and Mass Transfer*

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demonstrate this enhanced thermal and hydraulic performance. The  $5\text{ mm} \times 5\text{ mm}$  silicon chip area, with resistive heaters and local temperature sensors fabricated directly on the opposite face, is cooled by a  $3 \times 3$  array of microchannel heat sinks that are fed with coolant using a hierarchical manifold distributor. Using the engineered dielectric liquid HFE-7100 as the working fluid, experimental results are presented for channel mass fluxes of 1300, 2100, and 2900  $\text{kg/m}^2\text{s}$  and channel cross sections with nominal widths of 15  $\mu\text{m}$  and nominal depths of 35  $\mu\text{m}$ , 150  $\mu\text{m}$ , and 300  $\mu\text{m}$ . Maximum heat flux dissipation is shown to increase with mass flux and channel depth and the heat sink with 15  $\mu\text{m} \times 300\text{ }\mu\text{m}$  channels is shown to dissipate base heat fluxes up to 910  $\text{W/cm}^2$  at pressure drops of less than 162 kPa and chip temperature rise under 47  $^{\circ}\text{C}$  relative to the fluid inlet temperature.

**Keywords:** high-flux; boiling; two-phase; manifold; microchannel; intrachip electronics cooling

## Nomenclature

$A$ area	$Q_{loss}$ heat loss to the ambient
$Bl$ boiling number ( $q''_{base} / (h_{fg} \dot{m})$ )	$R$ thermal resistance
$c_p$ specific heat	$Re$ Reynolds number ( $Re = G d_H / \mu$ )
$d_b$ base thickness	$T$ temperature
$d_c$ channel depth	$w$ width
$d_H$ channel hydraulic diameter	$x$ thermodynamic quality
$d_{wafer}$ wafer thickness	$z$ location along channel length
$G$ channel mass flux ( $G = \dot{m} / (A_c N)$ )	<i>Greek Letters</i>
$h$ heat transfer coefficient	$\eta_f$ fin efficiency
$h_{fg}$ latent heat of vaporization	$\eta_o$ overall surface efficiency
$I$ electrical current	$\mu$ fluid dynamic viscosity
$k$ thermal conductivity	$\rho$ fluid density
$L$ length	<i>Subscripts</i>
$L_{flow}$ channel flow length	$avg$ average
$\dot{m}$ mass flow rate	$b$ base
$N$ number of channels	$c$ channel
$P_{el}$ electrical power input ( $P_{el} = V I$ )	$chip$ chip
$V$ electrical voltage	$div$ divider
$q''_{base}$ base heat flux	$eff$ effective
$q''_w$ wall heat flux	$f$ fin
$Q_{net}$ net heat input to channels	$fl$ fluid

<i>i</i>	individual	<i>Si</i>	silicon
<i>in</i>	heat sink inlet	<i>SiO<sub>2</sub></i>	silicon dioxide
<i>out</i>	heat sink outlet	<i>wall</i>	wall
<i>ref</i>	reference	<i>wet</i>	wetted
<i>sat</i>	saturation		

## 1 Introduction

The continuing miniaturization of electronics components of ever greater performance and functionality has led to severely increased thermal management challenges. For example, heat fluxes in excess of 1000 W/cm<sup>2</sup> must be dissipated in next-generation radar, power electronics, and high-performance computing systems [1,2]. Electronic devices have traditionally been cooled through the attachment of standalone heat sinks. In this ‘remote cooling’ architecture, the total temperature rise across the thermal management solution is governed by parasitic interfacial, conduction, and spreading resistances between the device and heat sink. The deterioration of electrical performance characteristics and thermomechanical reliability at high device temperatures calls for the development of transformative ‘intrachip cooling’ strategies, with coolant channels deployed directly in the electronic device, to enable improved functionality. Dielectric working fluids are preferred for such systems because they minimize the threat for electrical shorting, do not interfere with RF signals, are non-corrosive, and are available at a variety of saturation temperatures.

In a pioneering study by Tuckerman and Pease [3], a 10 mm × 10 mm silicon microchannel heat sink with 50 μm wide and 300 μm deep channels was shown to dissipate 790 W/cm<sup>2</sup> at chip temperature rises of less than 71 °C above the fluid inlet temperature and pressure drops less than 186 kPa, using single-

phase water as the working fluid. Single-phase microchannel heat sinks have since been widely studied for electronics cooling applications [4]. In general, increasing channel depth, decreasing channel width, and increasing fluid flow rate all allow for larger heat dissipation at a given chip temperature. However, there are practical limits to how deep and thin these channels can be made. Additionally, pressure drop along the length of the channels leads to intractably large pumping power requirements at the extremely small channel widths and high flow rates necessary to dissipate extreme heat fluxes on the order of  $1000 \text{ W/cm}^2$ .

Two-phase evaporative cooling in microchannel heat sinks offers improved surface temperature uniformity and increased heat dissipation compared to single-phase microchannel heat sinks at a given pumping power [5–7]. For most working fluids, the latent heat of vaporization is orders of magnitude larger than the specific heat capacity; hence, evaporative cooling systems can operate at lower chip temperature rises and at reduced flow rates to dissipate the same amount of heat as single-phase systems. However, a significant fraction of the liquid must be evaporated before exiting the channel to realize the full potential of evaporative cooling. In most microchannel systems, intermittent dryout of the liquid film or flow instabilities causing premature critical heat flux (CHF) can lead to reduced performance well before a high exit quality can be reached. For flow boiling in microchannels, CHF has been found to increase with increasing channel wetted area, mass flux, and channel hydraulic diameter, as well as decreasing channel length [8]. Channel wetted area can be increased by decreasing channel pitch (*i.e.*, decreasing channel and fin widths to increase the number of channels) or increasing channel depth. Because pressure drop scales with  $L/d_H^2$  [9], decreasing the channel width while holding flow length constant results in prohibitive increases in pressure drop. A variety of heat sink designs have been employed to dissipate larger heat fluxes by delaying CHF or reducing the pressure drop in two-phase operation compared to a conventional design with straight, parallel channels fed by a single header. These designs have implemented one or more of features such as vapor venting [10], pin-fins and interrupted channels of various shapes and configurations [10–12], wick structures to aid in thin

film evaporation [13–15], microchannels with reentrant cavities and/or inlet restrictors [16], microgaps [17], arrays of jets [18–21], diverging channels [22,23], microchannels fed with tapered manifolds [24], and stacked heat sinks [25]. Heat fluxes as high as 1127 W/cm<sup>2</sup> have been dissipated with dielectric fluids [26] using a 10 mm × 20 mm copper heat sink that incorporated both flow boiling in microchannels and jet impingement. In this demonstration, the surface temperature at the highest heat flux exceeded 200 °C for a refrigerated fluid inlet temperature of -20 °C, which would present significant implementation challenges in electronics cooling applications.

Even with advances in performance achieved via evaporative cooling in current state-of-the-art heat sink designs, the maximum heat dissipation remains limited by impractically large pressure drops at high flow rates and vapor fractions. Manifold microchannel heat sinks address these challenges by distributing the flow through the microchannel heat sink in multiple parallel flow paths of decreased effective flow length. While channel length in traditional microchannel heat sinks is set by the length of the device being cooled, manifold microchannel heat sinks decouple flow length from the device size by delivering the fluid intermittently along the channel length.

Harpole and Eninger [27] developed a thermal model for single-phase flow in manifold microchannel heat sinks to optimize geometric parameters of a silicon heat exchanger using a water-methanol mixture as the working fluid. Their models predicted that steady-state heat fluxes greater than 1000 W/cm<sup>2</sup> were achievable with a fluid-to-chip temperature rise of less than 30 °C and a pressure drop of 101 kPa using high-aspect-ratio microchannels (channel widths from 7 μm to 14 μm and heights of 167 μm). Most research on manifold microchannel heat sinks for electronics cooling has continued to focus on single-phase operation. A variety of researchers have conducted numerical studies to identify optimized geometries and operating conditions for both the fluid distribution manifold and microchannel heat sink [28–32]. These studies concluded that 1) at a fixed pumping power, there is an optimal channel height, channel width, and



flow length for which thermal resistance is minimized, 2) the flow length should be minimized to minimize pressure drop for a fixed heat flux until manifold pressure drop governs the overall pressure drop at extremely short flow lengths, and 3) decreasing the channel width and increasing the flow rate both increase the heat transfer rate at the cost of increased pressure drop. While the optimal geometric and operational parameters depend on the working fluid, desired heat flux, and allowable pumping power, these studies have shown that manifold microchannel heat sinks can increase heat dissipation without significantly increasing pressure drop when compared to traditional microchannels. For example, Ryu *et al.* [29] found that single-phase manifold microchannel heat sinks can dissipate >50% higher heat fluxes than a conventional microchannel heat sink at the same allowable pressure drop. Several experimental studies have confirmed that, in single-phase operation, manifold microchannel heat sinks can dissipate high heat fluxes at moderate pressure drops [33–35].

Few studies have considered two-phase operation of manifold microchannel heat sinks. Using a manifold microchannel heat sink having 42  $\mu\text{m}$  wide and 483  $\mu\text{m}$  deep channels, Baummer *et al.* [36] demonstrated a dissipation of 300 W/cm<sup>2</sup> over a 1 cm<sup>2</sup> area with a chip temperature rise less than 50 °C using HFE-7100 as the two-phase working fluid.

The present work focuses on designing, fabricating, and characterizing a hierarchical manifold microchannel array for intrachip evaporative cooling with a dielectric fluid. Extreme heat flux dissipation from electronic devices at low pressure drops and low chip temperatures has not been previously demonstrated using dielectric fluids. A  $3 \times 3$  array of heat sinks—each containing 50 parallel, high-aspect-ratio ( $AR = 2.7$  to  $19.1$ ), small hydraulic diameter ( $\sim 20$  to  $30 \mu\text{m}$ ) microchannels—are fabricated in a single silicon chip over a  $5 \text{ mm} \times 5 \text{ mm}$  area. The intrachip microchannels are etched directly into the substrate of the heat source (also  $5 \text{ mm} \times 5 \text{ mm}$ ) to limit conduction and contact resistances, allowing for higher heat

flux removal. Fluid is delivered to the microchannels through a hierarchical manifold designed to provide uniform flow to each heat sink in the array throughout two-phase operation.

## **2 Test vehicle design and fabrication**

### *2.1 Hierarchical manifold microchannel concept*

Manifold microchannel heat sinks are designed to distribute fluid through multiple inlets and outlets along the heat sink so that the flow length through any single set of microchannels is significantly reduced. This concept is extended to achieve greatly improved performance in the current work by using a hierarchical manifold to feed an array of intrachip microchannel heat sinks featuring high-aspect-ratio channels. Direct liquid cooling minimizes conduction resistances and eliminates contact resistances that result from approaches relying on separately attached heat sinks. Figure 1 shows a schematic diagram of the hierarchical manifold microchannel heat sink array concept used in the current work. The silicon microchannel plate contains a 2D array of microchannel heat sinks, with each heat sink containing 50 microchannels in parallel, as well as resistance heaters and thermometers, as discussed later. The manifold routes a single flow inlet into the individual inlets to the microchannel heat sinks (blue regions in Figure 1). Fluid from the manifold arrives normal to each heat sink through a rectangular inlet centered along the length of each microchannel. Within each microchannel, the flow impinges on the channel base, splits in two directions, travels along the remaining channel flow length and exits into the manifold. Within the manifold, the flow from the array of microchannel heatsinks is combined into a single outlet stream (red regions in Figure 1).

### *2.2 Test vehicle design*

A thermal test vehicle, with all coolant distribution components heterogeneously integrated, is fabricated to demonstrate the thermal and hydraulic performance of the microchannel cooling approach

(Figure 2(a)). The system consists of a manifold base, manifold distributor, plenum interface plate, microchannel plate, and printed circuit board (PCB). The base serves as an interface between the flow loop and the hierarchical manifold distributor and contains ports for inlet and outlet pressure and temperature measurements. The manifold distributor splits the single coolant inlet into 9 parallel flow streams that enter a  $3 \times 3$  array of microchannel heat sinks covering a  $5 \text{ mm} \times 5 \text{ mm}$  chip area and also recombines the 18 flow streams exiting the heat sinks into a single coolant outlet (Figure 2(b)). Each heat sink cools a footprint area of  $1667 \text{ } \mu\text{m} \times 1667 \text{ } \mu\text{m}$ , with 50 parallel channels occupying a central area of  $1500 \text{ } \mu\text{m} \times 1500 \text{ } \mu\text{m}$ ; the flow enters at the center of the channel length resulting in an effective flow length of  $750 \text{ } \mu\text{m}$ . The purpose of the plenum plate is to provide an interface for sealing between the manifold distributor and the microchannels and to define the inlet and outlet regions to the microchannels; the plenum plate matches the manifold features, providing a smooth surface to seal against. The plenum interface plate is designed to have equal total inlet and outlet flow areas. Previous designs in the literature that were optimized for single-phase flows found the optimal inlet-to-outlet area ratio to be approximately 1.5:1 to 3.5:1 [29,32]; an increased outlet plenum size was incorporated in the current design to limit contraction of the high-velocity two-phase mixture at the channel outlet. One side of the plenum plate is mated to a  $10 \text{ } \mu\text{m}$ -thick double-sided adhesive and brought into contact with the manifold; the opposite side of the plenum plate is bonded to the microchannel plate (Figure 2). The top side of the microchannel plate is instrumented with heaters and sensors to evaluate the thermal performance. The PCB provides a convenient electrical interface to the heaters and sensors.

The current design is based on self-similar hierarchical manifold features that distribute flow using multi-level bifurcation (Figure 1). The design and the fabrication methods employed can be easily scaled to shorter flow paths or to cover larger heated areas as desired.

### *2.3 Test vehicle fabrication*

The fabrication and assembly of each test vehicle component is described in detail in this section. All fabrication steps were performed on 4-inch (100 mm), double-side polished silicon wafers in the Birck Nanotechnology Center at Purdue University.

### *2.3.1 Microchannel plate fabrication*

To begin the fabrication process, a 350 nm-thick SiO<sub>2</sub> layer was thermally grown (wet oxide, 1000 °C) on both sides of a silicon wafer (Figure 3(a)); the wafer thicknesses for Samples A, B, and C were 220 µm, 300 µm, and 385 µm, respectively. This oxide layer functions as an insulation layer for the heaters and resistance temperature detectors (RTDs), and also as a sacrificial hard mask used during dry etching of the microchannels. Microchannel fabrication (Figure 3(a)-(c)) began by spinning and soft-baking a 7 µm-thick layer of AZ9260 (AZ Electronic Materials) positive photoresist (PR) on one side of the wafer. The PR layer was exposed using a mask containing patterns for the microchannel features (MA6, Karl Suss), and developed in a 1:3 solution of AZ400K (AZ Electronic Materials) diluted in deionized (DI) water. The masked oxide layer was dry-etched (Advanced Oxide Etch System, Surface Technology Systems (STS)) and the channels were deep reactive ion etched (DRIE) into the silicon via the Bosch process (Advanced Silicon Etch System, STS). The PR layer was then stripped (PRS2000, Avantor Performance Materials) and the oxide was removed from the channel-side of the wafer using a buffered oxide etch (BOE).

Scanning electron microscopy (SEM) images (JEOL JCM-6000, NeoScope) of the three different fabricated channel geometries are shown in Figure 4. The critical channel dimensions measured from SEM images are summarized in Table 1. For simplicity, the test chips will be referred to by their nominal channel depths (*i.e.*, A: 15 µm × 35 µm; B: 15 µm × 150 µm; and C: 15 µm × 300 µm) throughout the discussion. The measured channel cross-sectional area,  $A_c$ , and channel wetted area,  $A_{wet}$ , are based on the actual perimeter along the channel boundary, which accounts for the taper in the channel sidewalls and curvature at the bottom of the channels. The fin pitch is constant at 30 µm for all channel depths.

Heater and sensor features were then fabricated on the side of the wafer surface opposite the microchannels (Figure 3(d)-(f)). Serpentine heaters were patterned on the chip, matching the footprint of the  $3 \times 3$  grid of microchannel heat sinks, and the RTDs were positioned near the center of each heat sink. The same procedures as described in the previous paragraph were used to produce a patterned AZ9260 mask layer for the serpentine heaters and RTDs. A 5-nm-thick layer of Ti and a 20 nm layer of Pt were successively deposited using e-beam evaporation. The lift-off process was completed by stripping the PR using PRS2000. The same lift-off process was repeated to fabricate the heater and RTD lead-wire traces (5 nm Ti and 200 nm Au). The traces were used to wire the nine serpentine heaters in parallel and to route the signals to the wire-bond pads at the periphery of the chip.

### *2.3.2. Plenum plate fabrication*

The plenum plate was fabricated from an oxidized silicon wafer using the processing steps shown in Figure 5. The same PR and oxide layer patterning and etching steps that were employed for the microchannel features were used to produce a masking layer for the plenum plate inlets and outlets (Figure 5(b)). The plenum features were etched completely through the wafer using DRIE. The PR was then stripped off the wafer using PRS2000 and the oxide was removed from both sides of the wafer using BOE (Figure 5(c)).

### *2.3.3 Microchannel-plenum plates bonding*

The microchannel and plenum plates were thermo-compression bonded to each other for proper sealing at the interface. To create the interfacial bonding layer, a 400 nm-thick Au layer was sputtered on top of a 100 nm Ti layer (QPrep Series, Mantis Deposition Ltd.). The wafers were then aligned, pressed into contact, and clamped in place in the bonding equipment (SB6e, Karl Suss). The wafers were bonded at 450 °C and 5000 mbar for 60 min. Once bonded, the wafers were diced (DAD-2H/6, Disco) into 20 mm  $\times$  20 mm chips with the heaters and RTDs occupying a 5 mm  $\times$  5 mm area at the center. Figure 6(a) shows an

SEM image of the isometric view of a plenum plate bonded to the microchannel plate; the image is taken from the channel side of the test chip such that the microchannels are visible through the plenum inlet and outlet flow ports.

#### *2.3.4 Test chip assembly*

A custom PCB was designed to allow connection of lead wires to the heaters and RTDs on the top side of the chip. The outer edge of the channel plate was fixed to the underside of the PCB using epoxy. Electrical traces terminating in contact pads on the chip were wire-bonded to Au contact pads on the PCB. The nine serpentine heaters were wired in parallel to provide uniform heating over the  $5\text{ mm} \times 5\text{ mm}$  area; the nine 4-wire RTDs were individually powered. Figure 6(b-d) show a microscope image of the heaters and RTDs and photographs of the assembled test chip mounted to a PCB and wire-bonded.

#### *2.3.5 Manifold fabrication*

The manifold distributor contains the hierarchical network of channels that serve as the interface between the flow loop and the array of microchannel heat sinks, as shown in Figure 2(a). The manifold consists of four laser-cut (PLS65MW, Universal Laser Systems), 3 mm-thick, clear acrylic sheets. The manifold plate closest to the base contains one inlet feature and one outlet feature; this plate matches the base flow features and is used to seal the manifold to the base using a silicone gasket. The plate closest to the plenum plate contains individual inlet and outlet channels for each heat sink, with adjacent channel exits combined into a single exit, as shown in Figure 2(b); this is done to increase the bonding feature sizes at the interface between the manifold and plenum plate. The two interior plates discretize the flow from the single inlet and outlet into the  $3 \times 3$  array. These sheets are joined using 10  $\mu\text{m}$ -thick adhesive film preforms that are laser-cut to match the flow features. The acrylic base serves as an interface between the flow loop and the manifold and contains ports for thermocouples and pressure taps at the inlet and outlet streams. During testing, the onset of boiling is verified by observing for the presence of vapor at the outlet of the test section,

which is easily visualized through the transparent acrylic plates. A silicone gasket seals the manifold to the base.

#### *2.3.6. Test vehicle assembly*

For final assembly of the test vehicle, stainless steel fittings are inserted into the manifold for fluid connections, as are fittings for thermocouples and pressure transducers. A 10  $\mu\text{m}$ -thick double-sided adhesive (5601, Nitto Denko) is laser-cut to match the footprint features of the manifold distributor. The adhesive is aligned with the manifold using guide pins and attached. The test chip is then aligned to the manifold using the guide pins and bonded using the adhesive. Insulation blocks (PEEK) are placed on top of the PCB and below the manifold. The bottom insulation block is mounted on an optical table and a pneumatic ram presses down on the top insulation block to compress the test vehicle assembly with a constant pressure. The test chip heaters are wired to a programmable DC power supply (XG100-8.5, Sorensen) using 16-gauge wire with an inline shunt resistor (HA-5-100, Empro) to measure the electrical current. The RTDs are wired to a constant-current power supply using a ribbon cable.

### **3 Experimental methods**

#### *3.1 Test chip calibration*

The RTDs patterned directly on the microchannel plate were calibrated in a laboratory oven at temperatures spanning the operational range. A Pt100 RTD (PR-10-3-100, Omega) was placed in the oven with the test chip and was used as the reference temperature for the calibration. A linear regression was used to interpolate the temperature-dependence of electrical resistance and develop a unique calibration for each of the nine sensors. Heat flux uniformity across the chip was estimated by measuring the resistance of each of the nine individual heaters at ambient temperature prior to testing. The resistance variation across the chip

surface was measured to be less than 1 % for all samples, and hence, variations in heat flux would be negligible when fixing the voltage drop across the heaters during testing.

The heat lost by natural convection and radiation from the test vehicle assembly,  $Q_{loss}$ , was estimated by applying a heat input via the serpentine heaters on the chip without any fluid in the test section. Once the system reached a steady-state condition, the temperature of each RTD on the chip surface was recorded. The temperatures were then averaged spatially and temporally to determine the average chip temperature,  $T_{chip,avg}$ . This procedure was repeated for heat inputs that resulted in a range of chip temperatures experienced during the experiments. A best-fit line to the temperature-dependent heat loss in the test setup used in this work gave the equation:  $Q_{loss} = 0.02576 (T_{chip,avg} - 21.52)$ .

### 3.2 Flow loop

A flow loop (Figure 7) was constructed to facilitate evaluation of the chip temperature rise and pressure drop across the heat sink array for a specified channel mass flux and fluid temperature at the test section inlet. A reservoir with an adjustable volume contains excess fluid and sets the system pressure during testing; cartridge heaters installed in the reservoir are used to vigorously boil the working fluid prior to testing. A magnetically-coupled gear pump (GB-P23, Micropump) circulates fluid through the test section and the fluid mass flow rate is measured using a Coriolis mass flow meter (CMF010M, Micromotion). The test section inlet and outlet gage pressures are measured in the manifold base (Figure 2) with pressure transducers (S-10, WIKA) and the pressure drop across the test section is measured with a differential pressure transducer (PX2300, Omega). Inlet and outlet temperatures are measured using T-type thermocouples (Figure 2). The fluid temperature at the test section inlet is controlled using an inline heater. Fluid exiting the test section is cooled using a liquid–liquid heat exchanger and then returned to the reservoir.

### 3.3 Test procedure



Performance of the test vehicle was evaluated at three channel mass fluxes: 1300 kg/m<sup>2</sup>s, 2100 kg/m<sup>2</sup>s, and 2900 kg/m<sup>2</sup>s for each of the three channel geometries. Table 2 shows the volumetric flow rates and Reynolds numbers ( $Re = d_H G / \mu$ ) for each case. Fluid flow rates ranged from 19 mL/min to 540 mL/min, with channel Reynolds numbers between 71 and 238; the low Reynolds numbers result from the extremely small hydraulic diameters of the channels tested.

Prior to testing, dissolved noncondensable gas (*viz.*, air) was removed from the working fluid, HFE-7100, via vigorous boiling of fluid in the reservoir and subsequent recollection of condensate. Removing the dissolved gasses from dielectric fluids is critical to achieving repeatable and predictable results during two-phase testing [37]. Once degassed, fluid was circulated at the desired mass flux, and the volume of the reservoir was adjusted to maintain an outlet pressure of 123 kPa. The power to the preheater was adjusted to maintain an inlet temperature of 59 °C (7 °C below the saturation temperature at the test section outlet). Power to the test chip heater was incremented from zero until a maximum chip temperature of ~125 °C was reached. This temperature limit was chosen conservatively to guarantee that the heaters and wire bonds were not damaged during testing. For some of the experiments, the heater power was shut off due to critical heat flux being reached where a sudden temperature excursion was observed (*i.e.*, the chip temperature spiked suddenly, or slowly increased with time without reaching a steady-state value). Other experiments reached steady-state operating points at chip temperatures near 120 °C; heat fluxes that would lead to higher chip temperatures were not attempted to avoid the risk of damage to the test vehicle. Once steady-state conditions were reached for a fixed power level, the data were collected at a rate of 6000 Hz for 2 min. These data were time-averaged to yield a single steady-state data point corresponding to each power level. All data are collected using a National Instruments data acquisition (DAQ) system (cDAQ-9178, National Instruments) and are monitored and recorded through a LabVIEW interface.

### 3.4 Data reduction

Electrical power supplied to the serpentine heaters,  $P_{el}$ , was calculated using the measured voltage and current. The net heat input was calculated by subtracting the heat loss,  $Q_{loss}$ , from the supplied electrical power as  $Q_{net} = P_{el} - Q_{loss}$ . The heat flux,  $q''_{base}$ , was calculated by dividing the total heat input by the base footprint area,  $A_b$ . The effective overall thermal resistance,  $R_{eff}$ , was calculated based on the average chip temperature rise above the fluid inlet temperature,  $T_{fl,in}$

$$R_{eff} = \frac{A_b (T_{chip,avg} - T_{fl,in})}{Q_{net}}. \quad (1)$$

This represents an effective resistance that includes the caloric resistance of the fluid and conduction resistance through the channel base.

The heat transfer coefficient was estimated using:

$$h_{wall} = \frac{Q_{net}}{\eta_o A_{wet} (T_{base,avg} - T_{fl,ref})}. \quad (2)$$

To calculate the fluid reference temperature, the thermodynamic quality of the fluid at the channel exit was calculated using an energy balance:

$$x_{out} = \frac{Q_{in} - \dot{m} c_p (T_{fl,out} - T_{fl,in})}{\dot{m} h_{fg}}. \quad (3)$$

For heat fluxes at which  $x_{out} \leq 0$ ,  $T_{ref}$  is taken as the average of the fluid inlet and outlet temperatures. For  $x_{out} > 0$ , the location where the saturation temperature is reached,  $z_{sat}$ , is estimated using an energy balance; the fluid temperature is assumed to increase linearly up to the local saturation temperature at  $z_{sat}$  and decrease as the local pressure decreases along the remaining length of the channel. For this calculation, the pressure drop in the channel is assumed to be linear throughout and the heat flux is uniform along the length of the channel. The reference temperature is calculated by taking a length-weighted average of these temperatures:

$$T_{ref} = \begin{cases} \frac{T_{fl,in} + T_{fl,out}}{2} & ,if \ x_{exit} \leq 0 \\ \left( \frac{T_{fl,in} + T_{sat,x_{sat}}}{2} \right) \frac{z_{sat}}{L} + \left( \frac{T_{sat,x_{sat}} + T_{sat,out}}{2} \right) \frac{(L - z_{sat})}{L} & ,if \ x_{exit} > 0 \end{cases} \quad (4)$$

The temperature at the base of the channels is calculated accounting for conduction resistances across the heat sink base layers as:

$$T_{base,avg} = T_{chip,avg} - \frac{Q_{net}}{A_b} \left( \frac{d_b}{k_{Si}} + \frac{d_{SiO_2}}{k_{SiO_2}} \right) \quad (5)$$

Overall surface efficiency is defined as:

$$\eta_0 = 1 - \frac{NA_f}{A_{wet}} (1 - \eta_f), \quad (6)$$

where  $\eta_f$  is the fin efficiency and is defined as:

$$\eta_f = \frac{\tanh(md_c)}{md_c}, \quad \text{where} \quad m = \sqrt{\frac{2h_{wall}}{k_{Si}w_f}}. \quad (7)$$

The heat transfer coefficient is first solved assuming a fin efficiency of unity; fin efficiency is then iterated until the calculated heat transfer coefficient value converged.

### 3.5 Uncertainty

The measurement uncertainties of each instrument in the experimental test facility are listed in Table 3. The listed uncertainties were obtained from the manufacturers' specifications sheets except in the case of the custom RTDs; the uncertainties for the chip temperatures were conservatively estimated using the accuracy of the reference RTD used for the calibration, the linearity of the sensor calibration, and the repeatability of the sensors over time. The uncertainties of calculated values were determined using the method outlined in Ref. [38] and are also listed in Table 3. The maximum uncertainties in heat flux, effective

thermal resistance, and heat transfer coefficient occur at low heat fluxes (and low chip temperatures) and generally decrease with increasing heat flux.

## 4 Results and discussion

### 4.1 Temperature distribution across the test chip

Figure 8 shows the steady-state temperatures measured across the chip surface by the nine RTDs, each located near the center of the corresponding heat sink, and the average chip temperature, for the  $15\ \mu\text{m} \times 150\ \mu\text{m}$  channels (Sample B) at a mass flux of  $1300\ \text{kg/m}^2\text{s}$ . At low heat fluxes ( $< 75\ \text{W/cm}^2$ ), the heat input is less than the value required to reach the saturation temperature; the working fluid therefore remains in a liquid state at the outlet (*i.e.*, in the single-phase regime). The temperature variation remains below  $3\ ^\circ\text{C}$  in the single-phase regime, which can be attributed to uniform fluid delivery to each heat sink by the hierarchical manifold during single-phase operation. As heat flux is further increased, boiling is initiated in each zone (not necessarily simultaneously). Outlet flow in the manifold is monitored for vapor to visually confirm two-phase operation. While flow inside the channel cannot be monitored directly, the onset of boiling at different locations can be inferred from small ( $\sim 1\text{-}2\ ^\circ\text{C}$ ), sudden drops in the local transient chip temperature data, due to the excess superheat required for vapor nucleation in highly wetting fluids. For the data shown in Figure 8, for example, vapor was first seen in the manifold at  $100\ \text{W/cm}^2$ , and the individual RTDs showed signatures of boiling onset for a range of heat fluxes between  $100\ \text{W/cm}^2$  and  $175\ \text{W/cm}^2$ . Despite this spatially non-uniform onset of boiling, the RTD temperatures remain relatively consistent across the chip surface ( $< 5\ ^\circ\text{C}$  variation) up to  $220\ \text{W/cm}^2$ . As the heat flux is further increased, the chip temperature variation increases. The spatial non-uniformity becomes severe at the highest heat fluxes; for example, at the maximum heat flux of  $410\ \text{W/cm}^2$  in Figure 8, the temperatures on the chip ranged from  $95\ ^\circ\text{C}$  to  $122\ ^\circ\text{C}$ .

This experiment was discussed as a representative case and similar trends are observed for all test chips and flow rates. Chip temperatures are relatively uniform in single-phase operation and for a range of heat fluxes beyond incipience. The chip temperatures steadily diverge as heat flux is further increased, with the maximum temperature variation occurring at the highest heat flux tested. For a single test chip, the pattern of the temperature non-uniformity remains consistent (*e.g.*, the highest temperature location remains the same for all mass fluxes). However, the locations change for each different sample (*e.g.*, the highest temperature location is not the same for Sample A as it is for Sample B or Sample C). Therefore, the temperature divergence is attributed to manufacturing variations and assembly tolerances in the manifold, which are exacerbated in the two-phase regime, rather than to inherent flow maldistribution due to the manifold design.

#### *4.2 Boiling curves*

The boiling curves for each different channel geometry at mass fluxes of 1300, 2100, and 2900 kg/m<sup>2</sup>s are shown in Figure 9. Single-phase fluid is delivered to the heat sink array at an inlet temperature 7 °C below the saturation temperature of the fluid based on the outlet pressure. For low heat fluxes, the fluid remains in a single-phase state through the channel length, resulting in a linear temperature rise with increasing heat flux. The slope of the boiling curve in the single-phase region increases with increasing mass flux and channel depth; increasing channel depth provides more surface area for heat transfer while increasing mass flux provides higher inlet velocities and longer developing flow length. The heat input required to reach the saturation temperature increases with increasing fluid flow rates, which results in the single-phase regime being extended to higher heat fluxes for deeper channels and larger mass fluxes. It has been observed in the literature that increasing mass flux leads to increased wall superheats at incipience in straight microchannels [39]. This trend is also observed in the current system, where all three samples begin

boiling at chip superheats of 8 – 10 °C for a mass flux of 1300 kg/m<sup>2</sup>s and 14 – 22 °C for a mass flux of 2900 kg/m<sup>2</sup>s.

Boiling incipience in the channels results in an increase in slope of the boiling curve; this increase is most dramatic for low mass fluxes where the convective heat transfer is weakest. The boiling curves do not show a sharp transition at the onset of boiling due to the many parallel flow paths that each boil at slightly varying heat fluxes as described in Section 4.1. Sample A (15 µm × 35 µm), which has the shallowest channels and, therefore, the least wetted area, has significantly higher chip temperatures at any given base heat flux or mass flux, and reaches CHF at a much lower heat flux. For low heat fluxes, the temperature rise for Sample C (15 µm × 300 µm) is consistently lower than that for Sample B for a given mass flux and heat flux (except for one region where Sample B (15 µm × 150 µm) entered the two-phase region before Sample C), which can be attributed to the increased wetted area of Sample C. In absolute terms, the temperatures for Sample C and Sample B remain close at low heat fluxes. For example, at a mass flux of 1300 kg/m<sup>2</sup>s, Samples B and C yield chip temperatures within 5 °C of each other for heat fluxes up to 200 W/cm<sup>2</sup>; for mass fluxes of 2100 kg/m<sup>2</sup>s and 2900 kg/m<sup>2</sup>s, chip temperatures remained within 5 °C of each other up to 600 W/cm<sup>2</sup> and 500 W/cm<sup>2</sup>, respectively.

The performance of Samples B and C begin to deviate from each other at higher heat fluxes, and this difference in performance is most pronounced where Sample B reaches its lower critical heat flux. For example, the highest heat flux dissipated by Sample B at a mass flux of 1300 kg/m<sup>2</sup>s is 410 W/cm<sup>2</sup> and results in a chip temperature rise of 34 °C; at this same heat flux, the chip temperature rise is only 21 °C at a mass flux of 2900 kg/m<sup>2</sup>s. The maximum heat flux dissipated increases significantly with increasing mass flux, especially for Samples A (15 µm × 34 µm) and B (15 µm × 150 µm) that were tested to CHF; this trend is not as apparent for Sample C (15 µm × 300 µm) because testing was stopped due to a temperature cut-off being reached before CHF. Maximum heat flux dissipation also increases significantly with channel depth,

as shown in Table 4, which lists the maximum heat fluxes dissipated for each of the experiments. Critical heat flux has been shown to scale with mass flux and wetted area during flow boiling in straight microchannels [8]. Harirchian and Garimella [40] found that the suppression of nucleate boiling and partial wall dryout lead to decreased heat transfer at high heat fluxes in straight microchannels, which leads to increased wall temperatures; this mechanism has been found to occur at large wall heat fluxes ( $q''_w = Q_{net}/(A_w*N)$ ) and large boiling numbers ( $Bl = q''_w/(G*h_{fg})$ ). For a given base heat flux, the wall heat flux decreases with increasing channel depth, which in turn leads to a decrease in boiling number; boiling number also decreases with increasing mass flux, leading to a higher CHF. These trends are both seen in Figure 9 where CHF increases for increasing channel depth (decreasing wall heat flux) and increasing mass flux (decreasing boiling number).

#### 4.3 Heat transfer coefficient

Wall heat transfer coefficient, calculated using the procedure detailed in Section 3.4, as a function of outlet thermodynamic quality for mass fluxes of 1300, 2100, and 2900 kg/m<sup>2</sup>s is illustrated in Figure 10. In general, heat transfer coefficients remain relatively constant throughout the single-phase regime ( $x_{out} < 0$ ) for a fixed channel geometry and mass flux. Single-phase heat transfer coefficient shows a strong dependence on mass flux, where increasing mass flux results in an increased single-phase heat transfer coefficient for all three channel geometries. Ryu *et al.* [29] found that the local heat transfer coefficient along the length of manifold microchannel heat sink channels is strongly dependent on the inlet jet region and the region immediately downstream of the inlet where the thermal boundary layer is smallest in thickness and developing. They also found that the boundary layer is developing for a significant portion of the total flow length for manifold microchannel heat sinks of similar dimensions as the current study. Therefore, it is expected that heat transfer coefficient would strongly depend on inlet velocities and channel mass fluxes. A

clear correlation between the channel cross section and single-phase heat transfer coefficient is not seen here for the channel geometries tested.

Once boiling is initiated ( $x_{out} \approx 0$ ), and heat is also removed by phase-change, the heat transfer coefficients increase. For a fixed mass flux, all three samples have similar heat transfer coefficients in the low-quality regime ( $0 < x_{out} < 0.1$ ); for highly confined two-phase flows in small hydraulic diameter channels, such independence of the heat transfer coefficient on channel geometry has been shown in straight, parallel channels for low wall heat fluxes [40]. In this region, heat transfer coefficients steadily rise with increasing outlet quality as film thicknesses decrease and mean velocities increase due to increased vapor generation. Table 4 lists the maximum heat transfer coefficient calculated for each experiment. For Sample A ( $15 \mu\text{m} \times 35 \mu\text{m}$ ), the maximum two-phase heat transfer increases significantly with mass flux. For deeper channels (Samples B and C), this trend is not observed and maximum heat transfer coefficient remains nearly constant for all mass fluxes tested.

At higher outlet qualities ( $x_{out} > 0.1$ ), the slope of the boiling curve begins to reduce, leading to a decrease in heat transfer coefficient. This degradation of performance is triggered by vapor blanketing causing local and intermittent dryout at the wall, and has been previously observed in flow boiling experiments for microchannels [41,42]. Because the hydraulic diameter of all three channel geometries is of the same order of magnitude as the bubble departure diameter, the flow is expected to be highly confined; boiling starts in the confined slug regime at the onset of boiling and transitions to annular flow at higher heat fluxes [43]; this can cause intermittent dryout at relatively low qualities after incipience. The heat transfer coefficient declines more gradually for lower mass fluxes, which is also consistent with behavior observed in straight, parallel microchannels [44]. Critical heat flux occurred between outlet qualities between 0.18 and 0.28 for Samples A and B; Sample C, which did not reach CHF, exhibited significantly lesser degradation in heat transfer coefficients, even at heat fluxes above  $900 \text{ W/cm}^2$ .



#### 4.4 Effective thermal resistance

Figure 11 shows the calculated effective thermal resistance as a function of exit thermodynamic quality. For all mass fluxes tested, thermal resistance values for Sample A ( $15\ \mu\text{m} \times 35\ \mu\text{m}$ ) are significantly larger than those for Samples B and C and are therefore shown on a different scale in the top row of Figure 11. This difference can be attributed to the significantly reduced wetted area for Sample A. Note that the conduction thermal resistance through the silicon base is slightly different for each sample due to differences in base thicknesses; the resistances due to conduction for Samples A, B, and C are  $1.5 \times 10^{-6}$ ,  $1.2 \times 10^{-6}$ , and  $0.73 \times 10^{-6}\ \text{m}^2\text{K/W}$ , respectively. These values contribute 2 – 7 % of the total effective thermal resistance for Sample A, 9 – 16 % for Sample B, and 8 – 13 % for Sample C.

For a fixed channel geometry and mass flux, because the conduction resistance is constant and the heat transfer coefficient remains relatively constant in the single-phase regime, the effective thermal resistance is also relatively constant. Figure 11 shows that single-phase thermal resistance decreases with increasing mass flux and channel depth, which agrees with prior studies of manifold microchannel heat sinks [30,31,33]; in these studies, the largest contribution to the decrease was the reduced temperature rise of the fluid with increasing flow rates, especially at low flow rates. In the current study, it is difficult to separate the impingement and developing flow effects from the decrease in caloric resistance, which would all contribute to a lower thermal resistance with increasing flow rates. Similarly, the decrease in thermal resistance with channel depth can also be attributed to the increase in wetted area.

The increase in heat transfer coefficient in the low-quality regime ( $0 < x_{out} < 0.1$ ) results in decreased thermal resistances for all channel geometries and mass fluxes. Thermal resistance is found to depend on both channel depth and mass flux, especially for shallow channels. Comparing Sample B ( $15\ \mu\text{m} \times 150\ \mu\text{m}$ ) to Sample A ( $15\ \mu\text{m} \times 35\ \mu\text{m}$ ), for a 77% decrease in wetted channel area, the minimum thermal resistance increases 160% from  $7.66 \times 10^{-6}\ \text{m}^2\text{K/W}$  to  $19.9 \times 10^{-6}\ \text{m}^2\text{K/W}$ . Sample C ( $15\ \mu\text{m} \times 300\ \mu\text{m}$ ) has a minimum

thermal resistance of  $5.60 \times 10^{-6} \text{ m}^2\text{K/W}$ , a 27% decrease compared to Sample B for a 100% increase in surface area. Deeper channels provide diminishing return due to the decreased fin efficiency for deep channels (as low as 58 % for Sample C), making the added heat transfer area less effective.

The decreases in thermal resistance from single-phase to two-phase operation are more drastic at low fluid mass fluxes where the single-phase thermal resistance is greater. As mass flux is increased, single-phase convective thermal resistance decreases, but thermal resistances in the two-phase regime are largely unchanged. For higher exit qualities, the thermal resistance increases, mirroring the heat transfer coefficient trends at high exit qualities. The increase is not observed for Sample C because the experiments were terminated (due to the chip temperature limit) while the quality was relatively low.

#### *4.5 Pressure drop*

The pressure drop as a function of heat flux is plotted in Figure 12. This differential pressure includes contraction into and expansion out of the channels as well as flow splitting and contraction/expansion resistances in the manifold.

For each experiment, pressure drop remains relatively constant in the single-phase region. In conventional microchannels, single-phase pressure drop scales with  $L/d_H^2$ , which would result in the shallowest channels having the highest pressure drop; however, it is observed that the pressure drops for the deeper channels (which also have larger hydraulic diameters) are larger for a given channel mass flux. While the channel velocities are equal for all channel geometries at a fixed mass flux, the velocities in the manifold are not constant because the manifold dimensions remain the same for all channel geometries. This results in the deeper channels (which have higher flow rates for a fixed mass flux) having higher pressure drops due to higher fluid velocities in the manifold. To approximate the contribution of the flow in the manifold to the overall pressure drop, a first-order estimate of the pressure drop in the channel was made assuming fully developed, laminar flow in a pipe [45] with the length equal to the center-to-center distance of the

manifold inlets and outlets (*i.e.*, 650  $\mu\text{m}$ ). These values were then subtracted from the measured total pressure drop for each experiment to estimate the manifold pressure drop. The estimated manifold pressure drops were then plotted as a function of flow rate and a quadratic polynomial was fit to the data with the intercept forced to zero; the resulting fit had an  $R^2$  value of 0.97. For the flow rates delivered to Sample A (19 – 42 mL/min), the manifold pressure drop is only  $\sim 0.1 - 0.5$  kPa; this increases to  $\sim 4 - 20$  kPa for Sample B (115 – 245 mL/min) and  $\sim 20 - 100$  kPa for Sample C (245 – 540 mL/min). These first-order estimates provide insight into the relative contribution of the manifold to the total pressure drop. For the highest flow rates tested, as much as 90% of the total single-phase pressure drop is estimated to come from losses due to sudden expansions, sudden contractions, and flow friction in the manifold; at the lowest flow rates tested, the relative contribution of the manifold to the total pressure drop is negligible ( $<2\%$  for all flow rates for Sample A).

After entering the two-phase regime, the pressure drop monotonically increases; this is caused by the increase in velocity with increasing vapor quality and boiling occurring further upstream in the channel at higher heat fluxes. For a fixed mass flux, the slope of the pressure drop curve is steeper for the shallower channels. This occurs because pressure drop largely depends on flow quality, and shallower channels have a higher quality for a given base heat flux.

## 5 Conclusions

Two-phase, intrachip manifold microchannel heat sinks were successfully designed, fabricated and tested. Each test vehicle used a hierarchical manifold to feed an array of microchannel heat sinks with high-aspect-ratio channels. The nominal channel depth test vehicles A, B, and C were: 35  $\mu\text{m}$ , 150  $\mu\text{m}$ , 300  $\mu\text{m}$ , respectively, while the nominal channel width was 15  $\mu\text{m}$  for all three samples. A heated chip area of 5 mm  $\times$  5 mm was cooled by a discretized 3  $\times$  3 grid of microchannel heat sinks. Each heat sink contained a bank

of 50 microchannels; because the manifold directs flow into the center of the channels and out of both ends, the effective flow length in any flow passage is 750  $\mu\text{m}$ .

The single-phase heat transfer coefficient was found to increase with increasing channel mass flux, which was attributed to impingement and developing flow effects. In the two-phase regime, heat transfer coefficient strongly depends on exit quality and weakly depends on channel depth and mass flux. For all channel depths and mass fluxes, heat transfer coefficient increases with increasing exit quality until a maximum is reached; after this point, the heat transfer coefficient decreases with exit quality until critical heat flux is reached. These trends match the general trends experienced in traditional microchannel heat sinks. The heat sink with the smallest channel depth (Sample A,  $15\ \mu\text{m} \times 35\ \mu\text{m}$ ) provided the highest heat transfer coefficient, 43,300  $\text{W}/\text{m}^2\text{K}$ , at a mass flux of 2900  $\text{kg}/\text{m}^2\text{s}$  and an exit quality of 0.16. The maximum heat transfer coefficients for Samples B ( $15\ \mu\text{m} \times 150\ \mu\text{m}$ ) and C ( $15\ \mu\text{m} \times 300\ \mu\text{m}$ ) were 31,000  $\text{W}/\text{m}^2\text{K}$  ( $G = 1300\ \text{kg}/\text{m}^2\text{s}$ ,  $x_{out} = 0.22$ ) and 29,000  $\text{W}/\text{m}^2\text{K}$  ( $G = 2200\ \text{kg}/\text{m}^2\text{s}$ ,  $x_{out} = 0.14$ ).

Effective thermal resistance was found to decrease with increasing channel depth and increasing mass flux. While the heat sink with the smallest channel depth provided the highest heat transfer coefficients, it also provided the highest thermal resistance due to the significantly reduced wetted area compared to the deeper channels. The decrease in thermal resistance provided by increasing the mass flux was minimal compared to the significant increase in pressure drop for deep channels. For a 150  $\mu\text{m}$  channel depth, the minimum thermal resistance decreased from  $9.2 \times 10^{-6}\ \text{m}^2\text{K}/\text{W}$  to  $7.7 \times 10^{-6}\ \text{m}^2\text{K}/\text{W}$  while pressure drop increased from 41 kPa to 112 kPa when mass flux was increased from 1300  $\text{kg}/\text{m}^2\text{s}$  to 2900  $\text{kg}/\text{m}^2\text{s}$ . However, increasing the mass flux did increase the maximum heat flux dissipated from 411  $\text{W}/\text{cm}^2$  to 705  $\text{W}/\text{cm}^2$ . The cooling approach provided a minimum effective heat sink thermal resistance of  $5.6 \times 10^{-6}\ \text{m}^2\text{K}/\text{W}$  for the sample with channel depths of 300  $\mu\text{m}$  at a mass flux of 2900  $\text{kg}/\text{m}^2\text{s}$ .

This work successfully demonstrated fabrication, heterogeneous integration, and characterization of hierarchical manifold microchannel heat sinks operating in the two-phase regime. Intrachip cooling using small hydraulic diameter, high-aspect-ratio microchannels is shown to dissipate extreme heat fluxes over a  $5 \times 5$  mm heated area. Heat fluxes up to  $910 \text{ W/cm}^2$  were dissipated at pressure drops less than 162 kPa and chip-to-fluid inlet temperature rises less than  $47^\circ\text{C}$  using  $15 \mu\text{m} \times 300 \mu\text{m}$  channels. The maximum heat fluxes dissipated for heat sinks with  $15 \mu\text{m} \times 150 \mu\text{m}$  and  $15 \mu\text{m} \times 35 \mu\text{m}$  channels were  $705 \text{ W/cm}^2$  and  $142 \text{ W/cm}^2$ , respectively.

### **Acknowledgements**

This material is based upon work supported by the Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office's (MTO) Intrachip/Interchip Enhanced Cooling (ICECool) Fundamentals program under Cooperative Agreement No. HR0011-13-2-0010. The content of the information does not necessarily reflect the position or the policy of the Government, and no official endorsement should be inferred. Distribution Statement A—Approved for public release; distribution unlimited.

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## Tables

Table 1. Summary of microchannel test sample dimensions.

Sample	$w_c$ ( $\mu\text{m}$ )	$d_c$ ( $\mu\text{m}$ )	$d_H$ ( $\mu\text{m}$ )	$AR$ (-)	$A_c$ ( $\mu\text{m}^2$ )	$A_{wet}$ ( $\mu\text{m}^2$ )
A	12.0	34	19.6	2.7	360	$5.59 \times 10^4$
B	14.7	153	28.8	10.4	2275	$2.41 \times 10^5$
C	16.2	310	31.7	19.1	5000	$4.83 \times 10^5$

Table 2. Experimental operating conditions.

<b>Sample</b>	<b><math>G</math> (kg/m<sup>2</sup>s)</b>	<b>Flow Rate (mL/min)</b>	<b><math>Re</math> (-)</b>
A	1300	19	71
	2100	31	112
	2900	42	147
B	1300	115	97
	2100	178	156
	2900	245	216
C	1300	240	107
	2100	395	172
	2900	540	238

Table 3. Uncertainty in measured and calculated values.

<b>Measured Value</b>	<b>Instrument</b>	<b>Uncertainty</b>
Chip temperature	RTDs (calibrated)	$\pm 1.0\text{ }^{\circ}\text{C}$
Heater voltage	Voltage divider circuit	$\pm 1.0\text{ }\%$
Heater current	Shunt resistor	$\pm 0.1\text{ }\%$
Fluid inlet temperature	T-type thermocouple (calibrated)	$\pm 0.25\text{ }^{\circ}\text{C}$
Fluid outlet temperature	T-type thermocouple (calibrated)	$\pm 0.25\text{ }^{\circ}\text{C}$
Outlet pressure	Gage pressure transducer	$\pm 0.3\text{ kPa}$
Pressure drop	Differential pressure transducer	$\pm 0.17\text{ kPa}$
Mass flow rate	Coriolis mass flow meter	$\pm 0.1\text{ }\%$
<b>Calculated Value</b>	<b>Uncertainty</b>	
Heater flux	$\pm 0.6 - 2\text{ }\%$	
Effective thermal resistance	$\pm 5 - 10\text{ }\%$	
Heat transfer coefficient	$\pm 7 - 15\text{ }\%$	

Table 4. Summary of thermal performance metrics for the three channel geometries at each mass flux tested (\*experiment stopped due to high steady-state temperature rather than CHF).

Sample	Mass flux, $G$ (kg/m <sup>2</sup> s)	Maximum heat flux dissipation, $q''_{base}$ (W/cm <sup>2</sup> )	Maximum heat transfer coefficient, $h_{wall}$ (W/m <sup>2</sup> K)	Minimum thermal resistance, $R_{eff}$ (m <sup>2</sup> K/W)
A (15 $\mu\text{m} \times 35 \mu\text{m}$ )	1300	68.5	$33.7 \times 10^3$	$27.4 \times 10^{-6}$
	2100	104	$35.9 \times 10^3$	$24.2 \times 10^{-6}$
	2900	142	$43.3 \times 10^3$	$19.9 \times 10^{-6}$
B (15 $\mu\text{m} \times 150 \mu\text{m}$ )	1300	411	$26.9 \times 10^3$	$9.22 \times 10^{-6}$
	2100	641	$31.0 \times 10^3$	$7.73 \times 10^{-6}$
	2900	705	$30.7 \times 10^3$	$7.66 \times 10^{-6}$
C (15 $\mu\text{m} \times 300 \mu\text{m}$ )	1300	761*	$28.7 \times 10^3$	$5.90 \times 10^{-6}$
	2100	873*	$27.0 \times 10^3$	$5.83 \times 10^{-6}$
	2900	910*	$28.2 \times 10^3$	$5.60 \times 10^{-6}$



## Figures

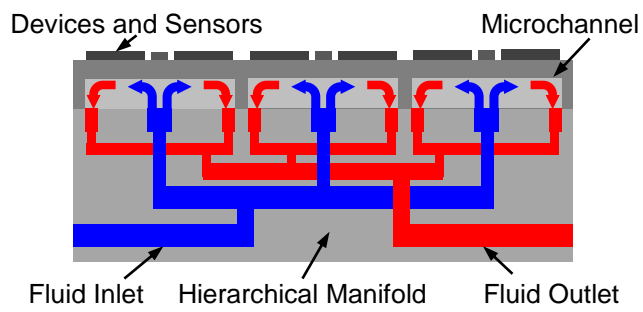


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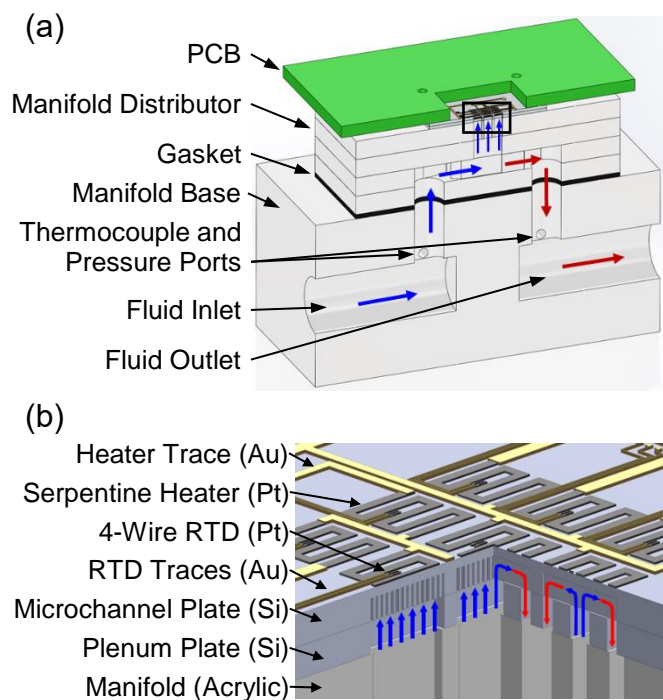


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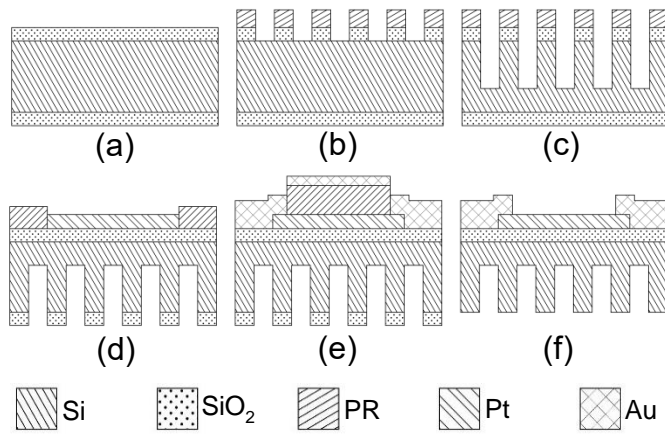


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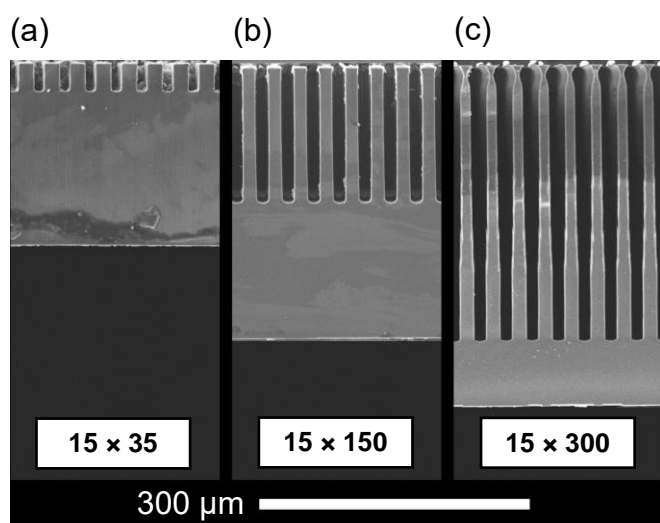


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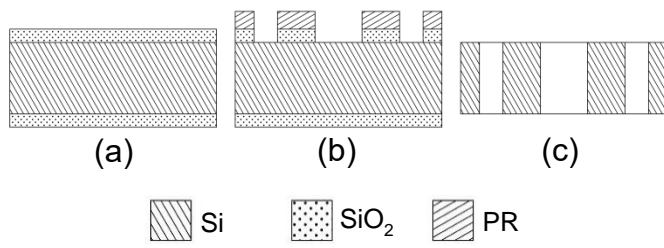


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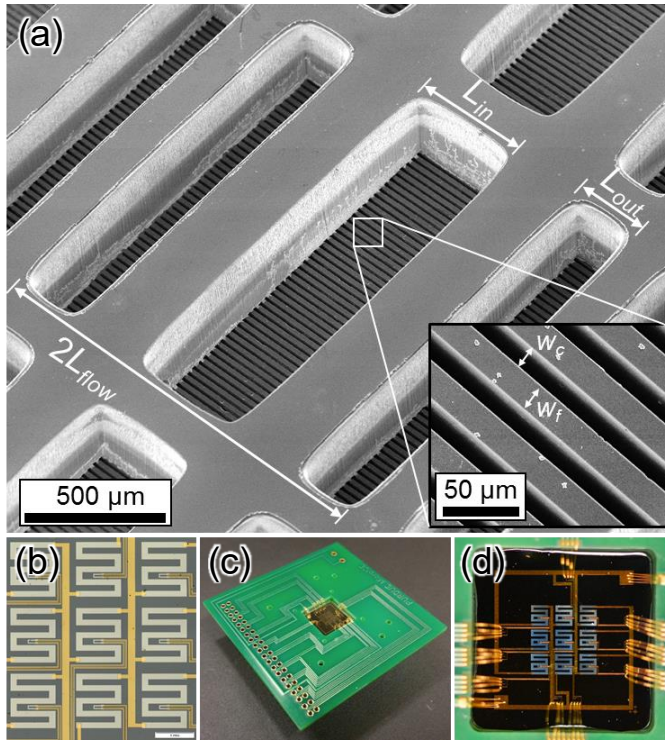


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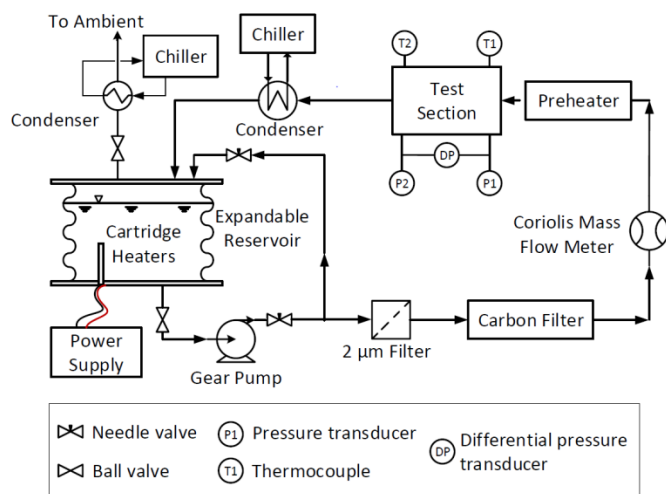


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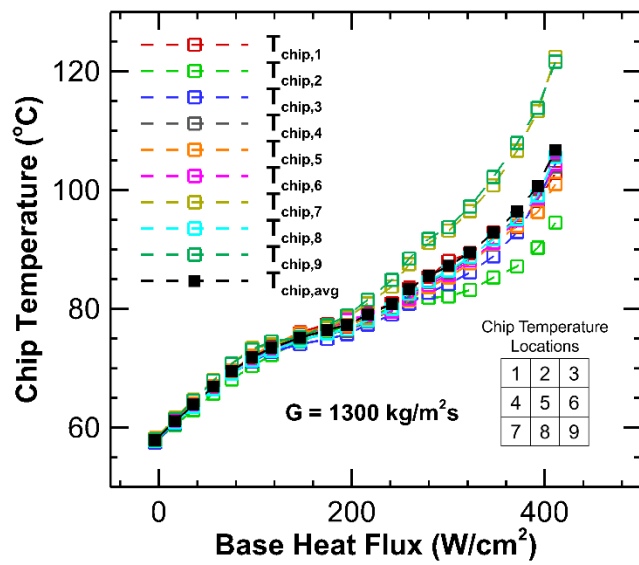


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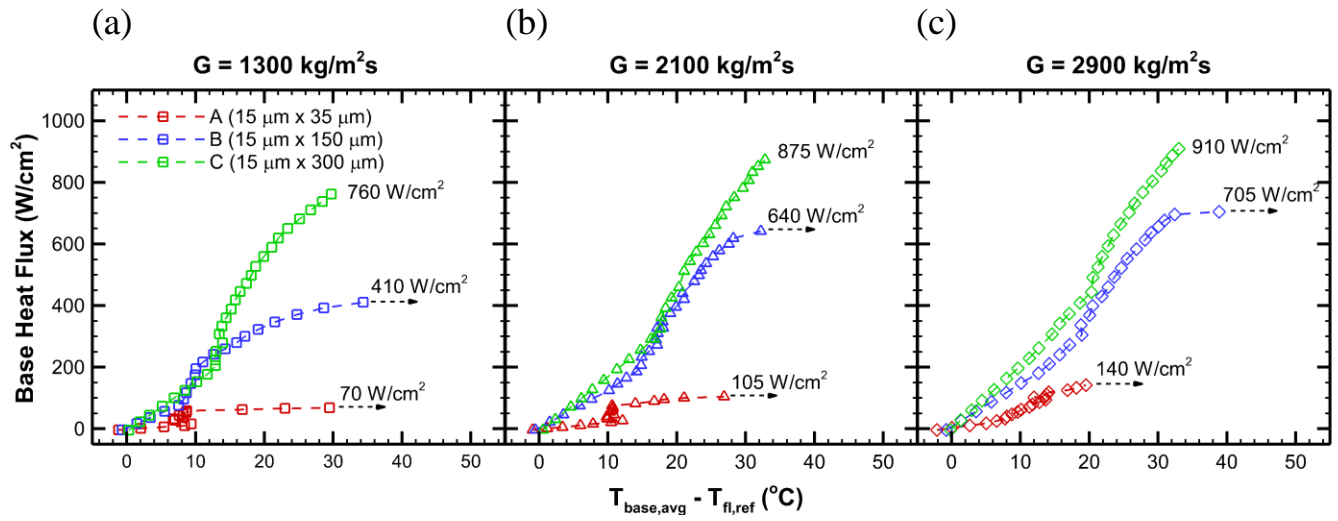


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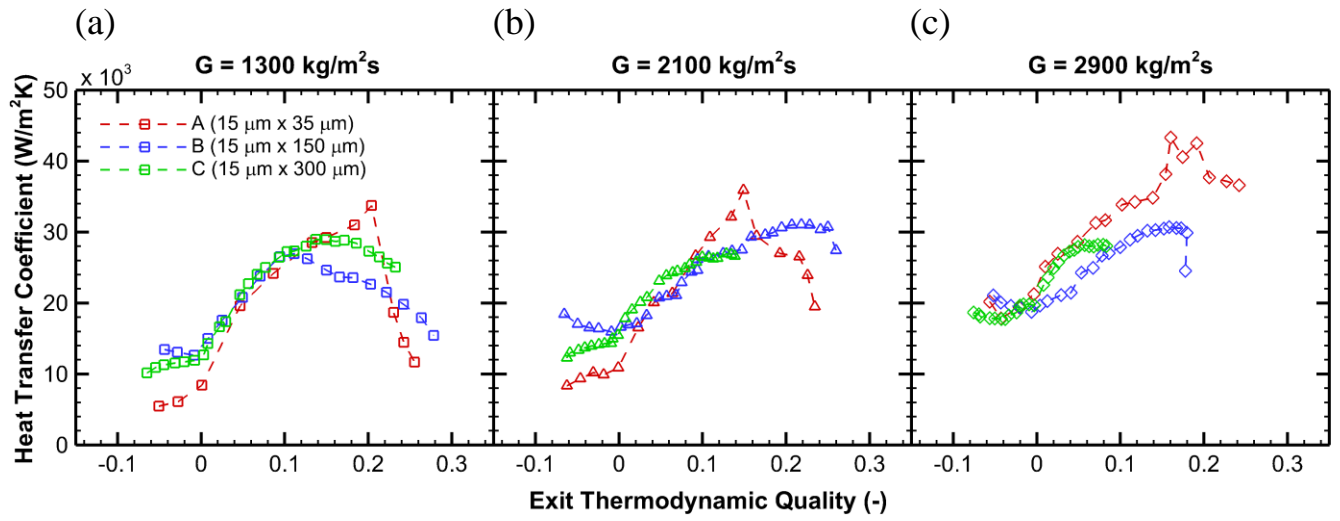


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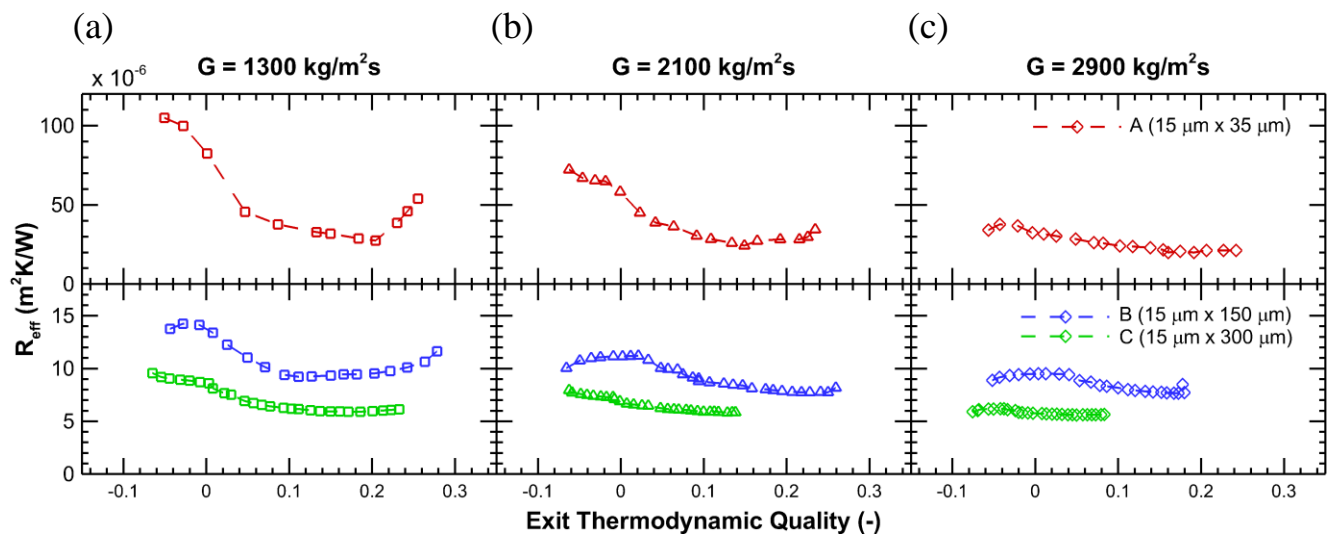


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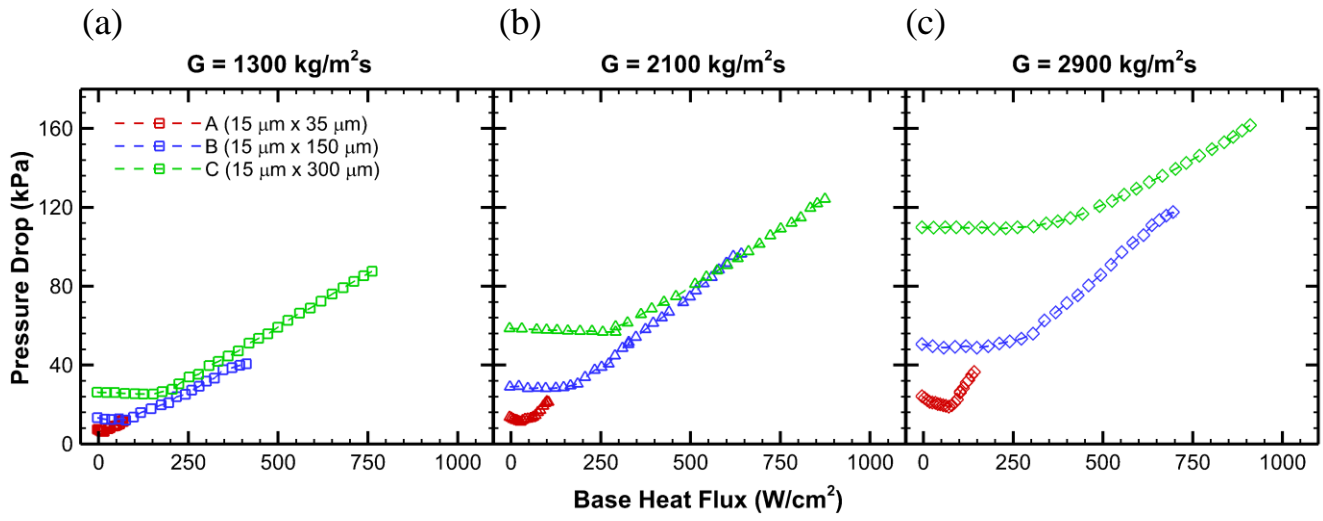


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