Fourth-Order Discrete-Time Variable Centre Frequency Bandpass Sigma-Delta Modulator

Y. Zhu, S.F. Al-Sarawi, C. C. Lim, and M.J. Liebelt

***Abstract*—A design for a variable centre frequency bandpass Sigma-Delta modulator is presented. The modulator is based on a tunable discrete-time resonator using only one control parameter. The noise transfer function of the modulator is controlled by a 4-bit digital signal, which provides nine different centre frequencies distributed between 0.1-0.4 normalized frequencies. The measurement results show a stable modulator at all centre frequencies.**

***Index Terms*—ADC, BPSDM, SNR, NTF.**

I. Introduction

Analog-to-digital converters (ADC) play important roles in digital HF receivers. The received signal is directly digitized at RF, then downconverted utilizing digital downconversion techniques, and further processed by either hardware or software DSP engines, such as software defined radio systems. Bandpass Sigma-Delta modulator (BPSDM) ADCs are able to achieve good performance using comparatively simple circuitries for digitizing passband signals. The main idea is to use a loop filter to shape the quantization noise power out of the band of interest; hence a better signal-to-noise ratio (SNR) is obtained. In contrast, conventional ADCs lower the entire quantization noise floor at the cost of a large number of comparators and digital correction logic. However for a BPSDM, once the noise transfer function (NTF) is decided, the centre frequency, where the RF or IF signal is located, is then fixed without changing the sampling frequency, and therefore prevents the application of a BPSDM for a multiple frequency channel HF receiver system. This issue results in the motivation of developing a BPSDM with variable centre frequencies (VCF).

Early work on VCF BPSDMs using continuous-time (CT) loop filters have been reported [1][2]. However, a CT SDM is a combined *z* and *s*-domain system, which makes it difficult to control the NTF when tuning the centre frequency; hence the modulator order and noise shaping efficiency are limited. Another approach is to use a discrete-time (DT) loop filter based on a tunable resonator expressed in the *z*-domain as

$$R(z)=\frac{Y(z)}{X(z)}=-\frac{az+1}{z^2+2az+1}, \tag{1}$$

where a is the only tuning parameter between -1 and 1, resulting in the corresponding resonance frequency changing from DC to half of the sampling frequency. The resonator can be realized in two different topologies as shown in Fig. 1, based on unit delay elements. This VCF BPSDM algorithm was first presented in [3], then a similar approach was reported in [4] and recently implemented in [5] using double sampling techniques. The purpose of this paper is to present a new NTF synthesis method with controlled out-of-band-gain (OOBG), and the switched-capacitor circuit realization.

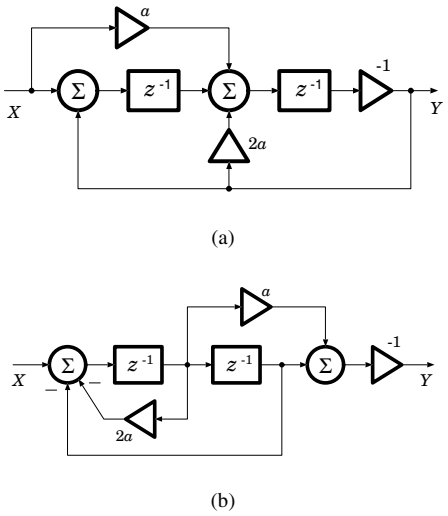

Fig. 1. Topologies of the tunable resonator of (1).

II. NTF synthesis

The VCF BPSDM design procedure starts by firstly synthesizing a stable fourth-order NTF, and then realizing the NTF using the variable frequency resonator $R(z)$ [3]. A fourth-order NTF with OOBG = 1.5 and Butterworth type zeros and poles is synthesized using Schreier's MATLAB toolbox [6] as

$$NTF(z)=\frac{(z^2+1)^2}{z^4+1.255z^2+0.4414}. \tag{2}$$

The next step is to map (2) to a fourth-order BPSDM topology using the resonator $R(z)$, as shown in Fig. 2. The

gain parameters c_1 and c_2 provide two degrees of freedom to realize the desired NTF. Using the linear model of the quantizer, the NTF of the fourth-order BPSDM can be derived as

$$NTF(z) = \frac{(z^2 - 2az + 1)^2}{(z^2 + 2az + 1)^2 + c_1c_2(az + 1)^2 - c_2(az + 1)(z^2 + 2az + 1)}. \quad (3)$$

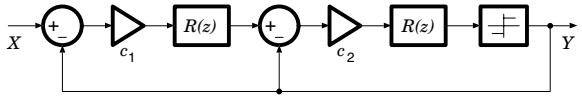

Fig. 2. Architecture of the 4th-order VCF BPSDM using the resonator of (1).

Since the OOBG at DC and 0.5 (normalized frequency) is independent of the tuning parameter a, it is convenient to set $a = 0$ to calculate the parameters c_1 and c_2, while still satisfying Lee's stability rule of thumb [7]. The NTF with $a = 0$ is given by

$$NTF(z) = \frac{(z^2 + 1)^2}{z^4 + (2 - c_2)z^2 + 1 + c_1c_2 - c_2}. \quad (4)$$

Comparing (4) to (2) and solving for c_1 and c_2 yields

$$[c_1,\ c_2] = [0.2792,\ 0.775]. \quad (5)$$

Substituting the coefficients c_1 and c_2 into (3) results in the final NTF of the fourth-order VCF BPSDM as

$$NTF(z) = \frac{(z^2 - 2az + 1)^2}{(z^2 + 2az + 1)^2 + 0.2164(az + 1)^2 - 0.775(az + 1)(z^2 + 2az + 1)}. \quad (6)$$

The calculated frequency response of (6) and simulated VCF BPSDM spectrums with different values of a are shown in Fig. 3. Since the OOBG is controlled at less then 2, Lee's stability rule of thumb [7] is always satisfied, therefore as expected the modulator remains stable throughout the tuning range of a from -0.95 to 0.95, corresponding to the normalized centre frequency changing from 0.05 to 0.45.

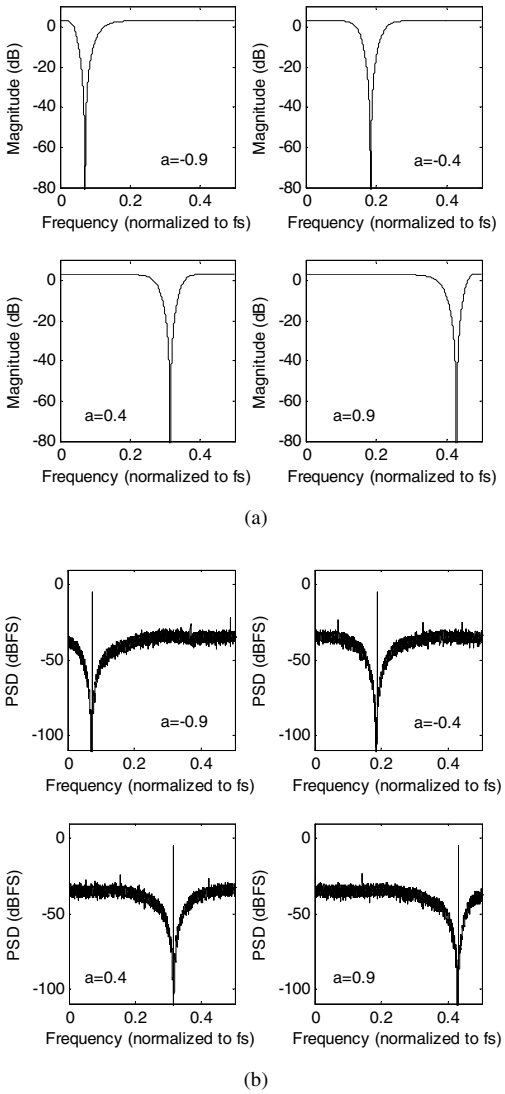

Fig. 3. (a) Calculated NTF frequency responses, and (b) Simulated power spectrum densities (PSDs) of the 4th-order VCF BPSDM, normalized to the sampling frequency f_s.

III. Circuit Design and Measurement

The resonator architecture shown in Fig. 1(a) can be implemented using fully differential switched-capacitor circuitry as illustrated in Fig. 4. Longo's unit delay structure [8] is used to realize the resonator. A two-phase clock and its delayed version, labeled as "1", "2" and "1d", "2d" in the schematic diagram, control the unit delay and feedback paths. NMOS switches are applied at the junctions, which are connected to the virtual ground. CMOS switches are used for the rest on the signal paths. The delayed clock scheme makes the CMOS switches operate slightly later than the NMOS ones, in order to reduce the clock noise injection effect [6]. This is because the summing junctions at the amplifier input nodes are disconnected by the NMOS switches, when the CMOS switches start operating with large clock noise injection. The feedback paths are controlled by switches *Sa+* and *Sa-*, corresponding to positive and negative values of the tuning parameter a, respectively.

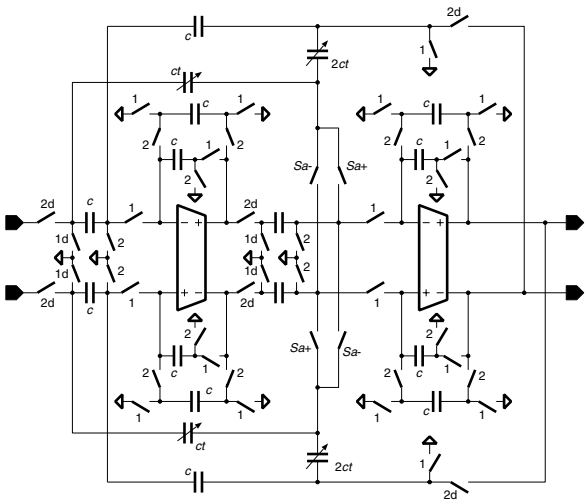

Fig. 4. Switched-capacitor circuitry realization of the resonator shown in Fig. 2.

The fourth-order VCF BPSDM layout, implemented in a 1.5 µm standard CMOS process, is shown in Fig. 5. Two extra amplifiers are used for subtraction of the feedback signals from the input before the input signals are fed into the resonators. The value of a, c_1 and c_2 are realized using ratios of capacitances. The whole chip contains six cascaded unity delay cells, a single-bit quantizer, switch and capacitor arrays, and a non-overlapped clock generator. The centre frequency is tuned by a 4-bit control word that provides total 9 different centre frequencies, distributed between 0.1 and 0.4 normalized frequencies.

The fabricated chip operates at 1 MHz sampling frequency, and drains 40 mA current from ±2.5 V voltage supplies. The measured output spectrums at the nine different centre frequencies are show in Fig. 6. The correct quantization noise shaping validates the algorithm and design methodology. The SNR is 61 dB, calculated from the output spectrum at the centre frequency of 400 kHz, and an oversampling ratio of 64.

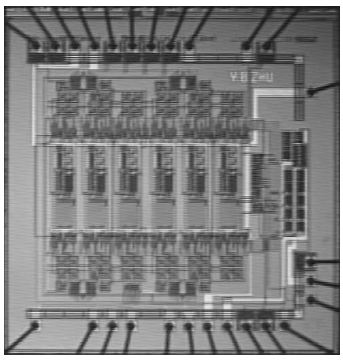

Fig. 5. Microscope image of the modulator.

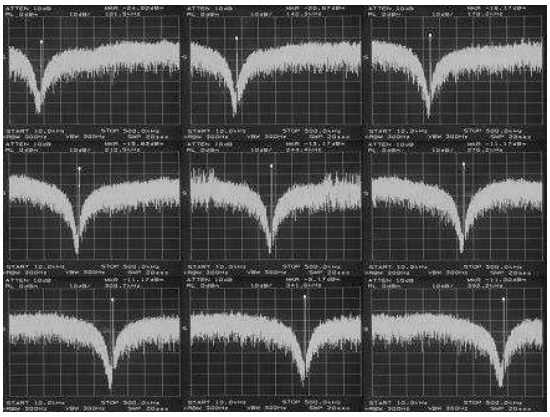

Fig. 6. Measured PSD of the 4th-order VCF BPSDM at 9 different centre frequencies (10dB/div).

IV. Conclusions

The design of a fourth-order VCF BPSDM is described in this paper. The modulator is based on a tunable resonator controlled by a single parameter, which is feasible for circuit realization. The prototype chip implemented in a 1.5 µm CMOS process presented a stable modulator at the nine different centre frequencies. By using the proposed algorithm, design methodology, and a more advanced fabrication process, a much faster bandpass modulator operating at 100 MHz for a monolithic multi-channel HF digital receiver is indeed achievable.

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